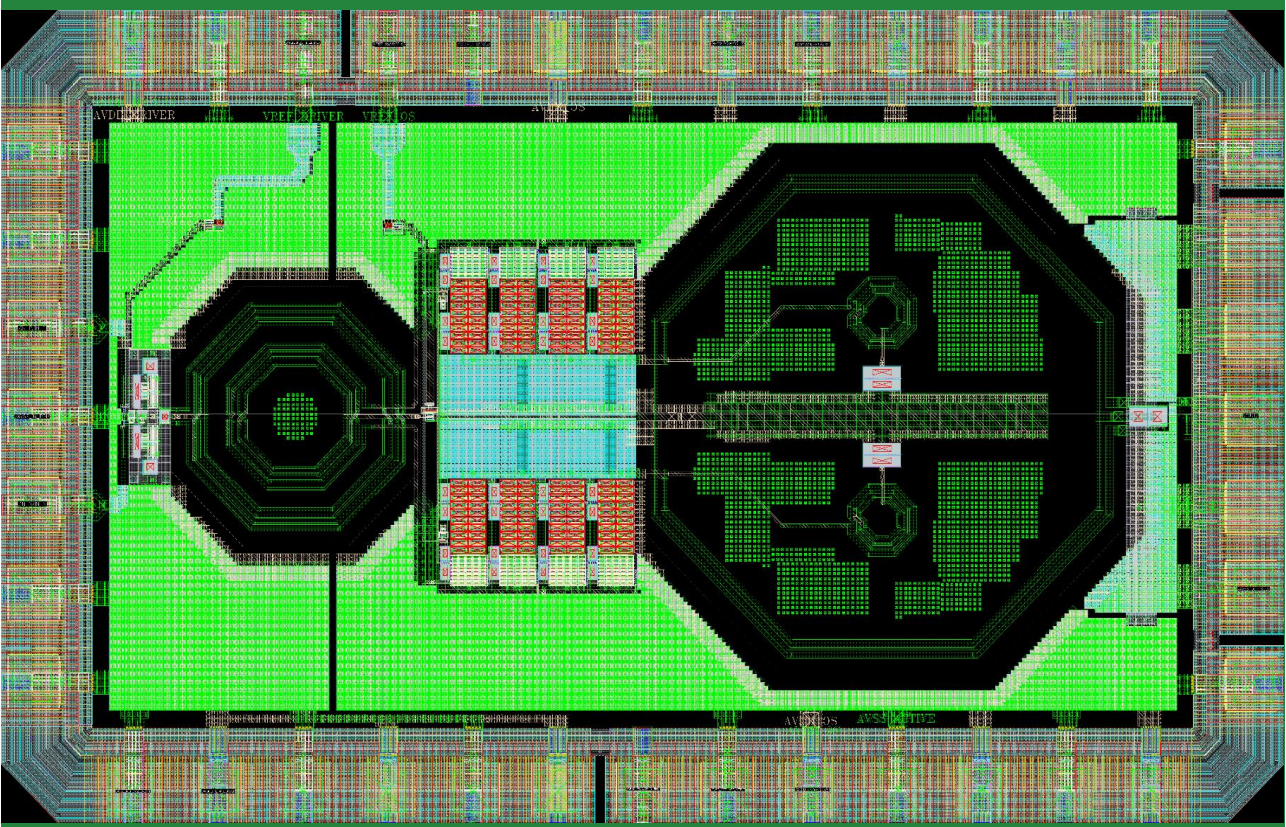
# Linear and Efficient Power Amplifier for WiFi

Anil Kumar Kumaran



TU Delft

# Linear and Efficient Power Amplifier for WiFi

## Thesis

to obtain the degree of Master
at Delft University of Technology,
publicly defended on Tuesday, August 25, 2020 at 2:00 PM

by

**Anil Kumar Kumaran**

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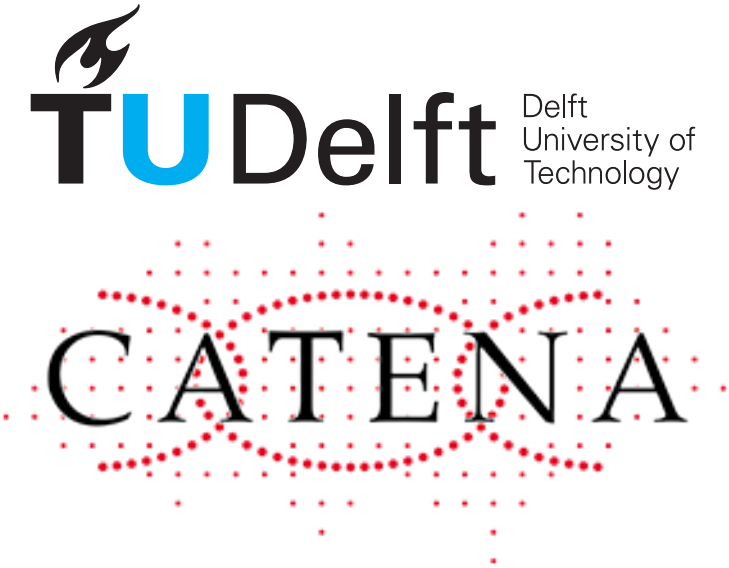


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*To my lovely parents, Kumaran and Sasikala*
*To my handsome brother, Arun and his wife Deepa*
*And last, but not least, to our beautiful angel Nitara.*

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*Anil Kumar Kumaran*
*Delft, August* $25^{th}$ *2020*

# Contents

# Summary

CMOS technology is one of the feasible solutions to meet the world's growing demand for high data rates because it offers the prospect of SoC at a low cost. But, the PA forms the major bottleneck in making SoC because the PAs in high data rate wireless communication systems have the requirement of high-efficiency and good linearity even at backed-off power levels. Currently, PAs are mostly of classes A and B. Both of these are linear, but their peak efficiencies are only *50%* and *78%* respectively.

This thesis focuses on implementing Continuous Class F (CCF) PA for **WiFi 802.11n** over the bandwidth *2.1 - 2.7 GHz*, which meets the requirement of high-efficiency and good linearity even at backed-off power levels. The CCF PA overcomes Class F's disadvantage of limited bandwidth as well as maintains peak efficiency of *90.7%*[1] over the entire bandwidth. The designed PA has four main blocks: the driver, inter-stage matching, output network, and output stage. The procedure to implement each of these blocks is explained extensively in chapters 3, 4, 5, and 6. The layout of the chip is carried out in TSMC *40 nm*, and the chip size is *1.4* $mm^2$. From post layout simulations, the CCF PA has a maximum efficiency of *30%* and EVM of *-25 dB* at *3* dB back-off across the bandwidth *2.1 - 2.7 GHz*. The tapeout of the chip is planned in *March 2021*. Later, the chip can be tested, and simulation results shall be validated. To the best knowledge of the author, this is the first CCF chip at *2.4 GHz* band.

[1] when *3* harmonics in voltage are considered

# 1

# Introduction

In today's scenario, there is a growing demand for high-speed transmissions at low cost in the area of Wireless Local Area Networks (WLANs) and home audio-visual networks. So, wireless communication systems like Wireless Fidelity (WiFi) are undergoing a brisk growth to fulfill this requirement. Every wireless communication system consists of a radio frequency (RF) transmitter and receiver. An RF transmitter comprises functional blocks such as digital to analog converter (DAC), an up-conversion mixer, an oscillator, a power amplifier (PA), and a bandpass filter (BPF) (refer Figure 1.1). Among all these blocks, the PA is the most vital and crucial module because its performance considerably influences the overall performance of the RF transmitter. Moreover, PA is the most power-hungry component, as well as the linearity limiting block in the RF transmitter. The basic functional requirement of PAs is to amplify the input signal to the required output power so that the signal propagates the desired distance to reach the receiver.

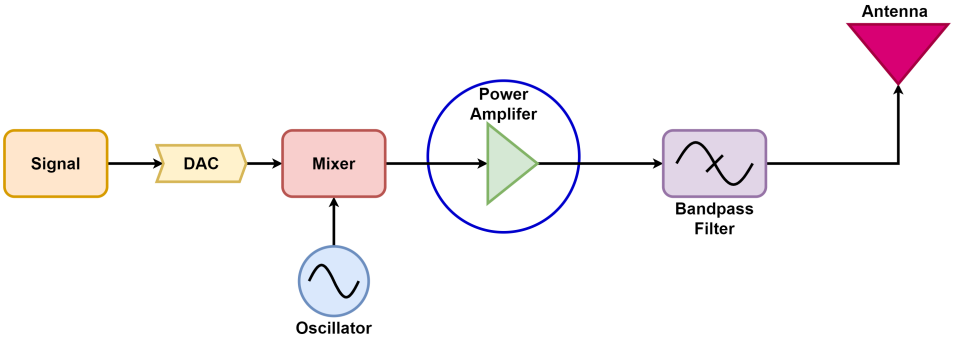


**Figure 1.1:** Basic block diagram of radio frequency (RF) transmitter [1]

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The advancements in complementary metal–oxide semiconductor (CMOS) technology has helped wireless communication systems significantly to achieve high data rates at low cost. CMOS technology is advantageous compared to other technologies like gallium arsenide (GaAs) and gallium nitride (GaN), because it operates at a lower power supply, thus reducing power dissipation in the circuit and also lower fabrication cost. Moreover, CMOS also offers the prospect of integrating RF/digital/analog functions on a single chip at a lower cost. Thus, leading to a highly integrated system on chip (SoC) which is of high demand these days.

However, CMOS PAs are a major roadblock in these efforts to create highly integrated SoC, due to both the low breakdown voltage of the transistor and lossy substrate. The PAs developed especially for high data rate wireless communication systems are required to have high efficiency and good linearity even at the backed-off power levels to efficiently amplify a multiplexing signal with a high peak-to-average power ratio.

Besides the roadblocks, the CMOS PA is a promising candidate for contemporary wireless devices to satisfy these demands and enable it to create highly integrated SoC. So at present, the research is focused on making the CMOS PA operate at lower power while generating a relatively high output power with high efficiency and good linearity even at backed-off power [1] [2].

Therefore, this thesis is focused on designing a CMOS PA for a specific application **WiFi 802.11n (LBPA_11n)** using TSMC *22 nm* ULL[1]. Firstly, in this chapter, an overview of existing classes of PAs and their advantages and disadvantages are discussed briefly. Further, this chapter summarizes the project specifications for the **WiFi 802.11n** application and consequently the problem statement. This is followed by the section which discusses PA architecture in detail. Finally, the chapter elucidates the division of the thesis report.

## 1.1. Types of power amplifiers

PAs can be classified into *3* types based on the operation of the transistor. The fourth category, mixed mode PAs are a combination of *2* classes of PAs.

- Transistor operated as a dependent current source;
- Transistor operated as a switch;
- Transistor operated in over-driven mode (partially as a dependent source and partially as a switch);
- Mixed mode PAs. [3].

### 1.1.1. Transistor operated as a dependent current source

In Class A, B, AB, and C, the transistor is operated as a dependent current source. This type of operation is suitable for linear PAs. The difference between these classes lies in the biasing point and conduction angle. This is shown in Table 1.1.

[1] Since the tapeout in **TSMC *22 nm* ULL** was canceled by *CATENA MICROELECTRONICS B.V.*, the design was ported to **TSMC *40 nm***, so that tapeout could happen through TU Delft in *March 2021*

| | Class A | Class AB | Class B | Class C |
|---|---|---|---|---|
| **Conduction angle** | $360^\circ$ | $180^\circ - 360^\circ$ | $180^\circ$ | $<180^\circ$ |
| **Drain efficiency ($\eta_D$)** | <50% | <78% | <78% | <100% |
| **Gain** | Maximum by matching | Moderate | Poor | Poor |
| **Linearity** | Good | Moderate | Poor | Poor |

**Table 1.1:** Conduction angle, peak drain efficiency, gain and linearity of Class A, AB, B and C PAs

### 1.1.2. Transistor operated as a switch

The main motivation to use the transistors as switches is to achieve high drain efficiency ($\eta_D$). When the transistor conducts a high drain current $I_D$, the drain-to-source voltage $V_{DS}$ is low. Thus, resulting in low power loss.

1. Class D [3]
   - There are *2* types in Class D: Voltage Mode (VM) and Current Mode (CM);
   - CM eliminates switching losses due to the device output shunt capacitance;
   - VM has low voltage stress since the voltage across each transistor is equal to supply voltage;
   - Peak factor of *1* and *3.14* for VM and CM respectively;
   - Less switching power dissipation from the transistors in VM mode;
2. Class E (ZVS and ZCS) [3]
   - There are *2* types in Class E: Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS)
   - In ZVS, the transistor turns on at zero voltage, and the transistor may turn on at zero derivatives. The transistor output capacitance, the choke parasitic capacitance, and the stray capacitance are absorbed into the shunt capacitance C;
   - In ZCS, the transistor turns off at zero current, reducing turn-off switching loss to zero. Even if, the transistor switching time is an appreciable fraction of the cycle of the operating frequency;
   - Class E has a simple load network;
   - Switching speed is limited only by the active device if optimum parameters of the load network are set.

- Peak factor is *3.6* times $V_{DD}$. Thus, creating an issue in the breakdown voltage.
- Class-E operation is based on the elimination of the current–voltage overlap region at the device turn-on transient, but it does not provide any solution for the large overlap region at the device turn-off;
- Disadvantages of ZCS is that output capacitance is not absorbed, turn on power loss, and lower efficiency.

Class D and E have very high efficiency (ideally *100%*) but linearity is poor. It is useful for constant envelope signals.

### 1.1.3. Transistor operated in overdriven mode

There are *2* types of PAs when the transistor is operated in overdriven mode:

1. Class F and Inverse Class F

   - Efficiency is *100%* and linearity is better than switching PAs;
   - Complex circuit due to different harmonic termination;
   - Switching speed limited by active devices and number of the controlled harmonic components composing the collector voltage and current waveforms.

Table 1.2 shows the main differences between Class F and Inverse Class F.

| Class F | Inverse Class F |
|---|---|
| Odd harmonics are open and even harmonics are short | Odd harmonics are short and even harmonics are open |
| Maximum drain voltage is $2V_{DC}$ | Maximum drain voltage is $\pi V_{DC}$ |
| Current in the transistor goes up to $\pi I_{DC}$ | Current in the transistor goes up to $2I_{DC}$[4] |
| The active device is biased near the cut off region | Active device is biased at half the maximum expected current |
| DC current and the output optimum load depends on the input power | Irrespective the input power value, the DC current and the output load optimum value remains constant |
| AM/AM response has a gain expansion and then compression | Double compression in AM/AM response [5] |

**Table 1.2:** Main differences between Class F and Inverse Class F

2. Class J/J* [6]
    - Uses reactive loading for fundamental and second harmonic, namely

$$Z_{Fund\_J} = R_{Fund\_B}(1 \pm j), \qquad Z_{Sec\_J} = \mp j\frac{3\pi}{8}R_{Fund\_B} \tag{1.1}$$

    with $R_{Fund\_B} = \frac{2V_{DD}}{I_{peak}}$;
    - In Class J, it is inductive fundamental loading where in Class J*, it is capacitive fundamental loading;
    - All higher harmonic are shorted;
    - Voltage swing of $2\sqrt{2}V_{DS}$ on the active device;
    - Exactly the same efficiency as Class B;
    - Since Class J PAs don't require harmonic resonators to achieve the maximum efficiency, there is a potential for increasing PA efficiency bandwidth compared with other linear amplifiers [7].

### 1.1.4. Mixed mode power amplifier

Mixed Mode PA comprises of *2* classes of PA. This is done to overcome limitations in one of the classes.

1. Class DE [3] [8]
    - Use dead time to reduce power losses and extend to higher operating frequency than Class D;
    - Operating frequency lower than Class E;
    - It is switching class so linearity is poor.
2. Class E/F [8]
    - Uses Class E and Inverse Class F;
    - Lower peak factor than both the classes;
    - Higher operating frequency than Class E as it can tolerate more shunt capacitor;
    - It is switching class so linearity is poor.
3. Bi-harmonic EM Class [8]
    - Degradation in the efficiency of Class E at a higher frequency. This is due to the increased switching power losses with increasing values of the turn-off switching time;
    - Allow power flow in the system at two or more harmonically related frequencies;
    - It needs *2* amplifiers.
    - Less input drive since it can tolerate slower switching time.

1

## 1.2. Project specification for WiFi 802.11n (LBPA_11n)

| Application | WiFi 802.11n (LBPA_11n) | |
|---|---|---|
| Average $P_{OUT}$ @-30 dB EVM | >16.5 | dBm |
| Error vector magnitude (EVM) | <-30 | dB |
| Operating band | 2.4 - 2.5<br>But targeted bandwidth is from **2.1 - 2.7 GHz** (25%) so as to cover LTE band | GHz |
| Channel bandwidth (max) | 40 | MHz |
| Peak power | >25 | dBm |
| Output 1dB compression point | >22 | dBm |
| Voltage gain | 20 - 25 | dB |
| Supply voltage | 2.7 | V |
| Technology | TSMC 22 nm-ULL | |

**Table 1.3:** Specifications for the project

Table 1.3 shows specifications that the PA has to meet in order to be used in application **WiFi 802.11n (LBPA_11n)**. The bandwidth is chosen from *2.1 - 2.7 GHz* so that PA can be used for **WiFi 802.11n**, as well as **LTE**. Thus, making it a multipurpose PA. Since the project was carried out in collaboration with the company *CATENA MICROELECTRONICS B.V.*, it was planned to design this PA such that it can be directly inserted into their existing WiFi chip. Owing to the previous decision, the concepts like Predistortion, Envelope Elimination and Restoration, Envelope Tracking, Doherty and Out-phasing [9] which are used to improve linearity and efficiency were not considered in this design as it will require a significant change in the WiFi chip.

## 1.3. Problem statement

The problem statement is very well defined and straight forward in this thesis. It is to design a fully CMOS PA in TSMC *22 nm* ULL with a supply voltage of *2.7 V* which meets linearity requirement for **WiFi 802.11n**, as well as be energy efficient for the bandwidth of *2.1 - 2.7 GHz*.

## 1.4. Class F

Based on the PAs discussed in section 1.1 and project statement presented in section 1.3, the Class F PA is the best choice to obtain high efficiency with good linearity which is the main requirement of the problem statement. The main motivation for this decision was that Class F has a higher efficiency (*90.7%* when three harmonics are considered which is shown in Table 1.4) than Classes A, B, AB, and J/J*. It has better linearity than Class C and switching PAs because the transistor can be biased

in Class B region. Moreover, linearity improvement techniques like Predistortion can't be used. In Class F, higher harmonics are used to shape waveform such that overlap between current and voltage is lower. In addition, Class F has a lower peak factor than Inverse Class F. Thus, Class F PA has been chosen for the application of **WiFi 802.11n** with the targeted bandwidth.

| **Number of harmonics in current (*m*)** | **Number of harmonics in voltage used in the matching network (*n*)** | | | |
|---|---|---|---|---|
| | n = 1 | n = 3 | n = 5 | n = ∞ |
| 1 | 0.5 | 0.5774 | 0.6033 | 0.637 |
| 2 | 0.7071 | 0.8165 | 0.8532 | 0.9003 |
| 4 | 0.7497 | 0.8656 | 0.9045 | 0.9545 |
| ∞ | 0.785 | 0.9069 | 0.9477 | 1 |

**Table 1.4:** Maximum efficiency capability of Class F PA [10]

From Table 1.4, it is seen that with $n = 3$ and $m = \infty$, efficiency of *90.7%* can be reached. Using higher harmonics in *n* doesn't increase efficiency much (For eg. for $n = 5$, efficiency increases only by *4%*). Moreover, using higher harmonic increases the complexity of circuit and component losses which in turn reduces efficiency. So it is better to use up to $3^{rd}$ harmonic in the voltage waveform.

Generalized drain source ($V_{DS}$) voltage containing all frequencies up to third harmonic [11] is given by:

$$V_{DS} = 1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos 3\theta \tag{1.2}$$

Drain current ($I_{DS}$) which is half sine wave is given by

$$I_{DS} = \frac{1}{\pi} + \frac{1}{2}\cos\theta + \frac{2}{3\pi}\cos 2\theta - \frac{2}{15\pi}\cos 4\theta \tag{1.3}$$

$I_{DS}$ has its peak at $0°$. It is shifted by $90°$. Load impedance at fundamental, second and third harmonic bands

$$\begin{aligned} Z_{1f} &= \frac{4}{\sqrt{3}} \\ Z_{2f} &= 0 \\ Z_{3f} &= \infty \end{aligned} \tag{1.4}$$

In Figure 1.2, amplitude is normalised to $V_{DD}$. It is seen from Figure 1.2 that peak factor is *2*.

Class F PAs can operate with an efficiency of *90.7%* when considering up to third harmonic but are limited to narrow bandwidths (typically *10%*) due to the

stringent requirement of short and open circuit harmonic terminations. But the bandwidth requirement here is around *25%*. So, the continuous mode concept has been introduced and illustrated to overcome the bandwidth limitation [12]. This is explained in detail in chapter 2.

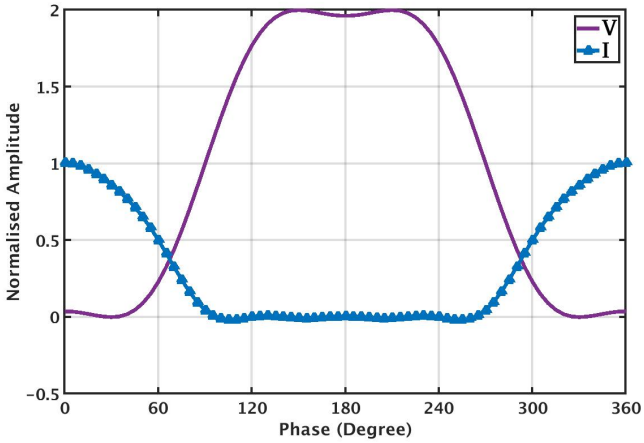


**Figure 1.2:** Voltage (V) and current (I) waveform for Class F PA

## 1.5. Power amplifier architecture

The architecture of PA is shown in the Figure 1.3.

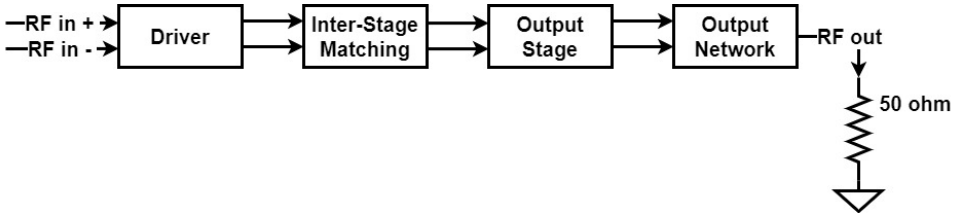


**Figure 1.3:** Architecture of designed PA

It was decided to have a push-pull (differential) PA compared to single-ended PA due to the following reasons:

- The common-mode noise and the substrate coupling is reduced since the current is discharged to the ground twice per cycle. Also, the interference problem is reduced since the substrate noise component is removed twice in the circuit;
- Output power was doubled compared to a single-ended configuration, and the optimum load was also reduced. The matching losses were consequently reduced;

- The transistor size and the current flowing through it can be reduced by using a differential configuration. Since the drain output voltage can be spread over both transistors, nearly twice the supply voltage can be handled without having issues in breakdown voltage [1];
- Second-order nonlinearities are reduced. If a differential circuit is balanced, then ideally, no even order nonlinearities are present and no even order harmonic and intermodulation products are generated [13].

Push-pull PAs also have a few disadvantages. One main disadvantage is that the circuit needs to be analyzed in common mode separately for stability issues unlike single ended circuits. Also, push-pull PAs have more complex circuitry compared to single-ended ones [1]. Since the advantages are more, it was chosen to have push-pull PA.

## 1.6. Division of thesis report

The thesis report consists of *10* chapters in total including introduction. The chapter 2 explains in detail about the concept and critical details of Continuous Class F (CCF). The chapters 3, 4, 5 and 6 explains the step by step process to design the output network, output stage, driver and inter-stage matching which all together forms the PA cell. The chapter 7 shows the results of the PA with schematics. The chip layout and post-layout results are reviewed in chapter 8 and 9. Finally, chapter 10 shows the future work.

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# 2

# Continuous Class F

This chapter illustrates the theoretical concept of Continuous Class F (CCF) and equations governing it. It further describes the different variants existing in CCF based on the termination of fundamental ($Z_{1f}$) and second harmonic ($Z_{2f}$) impedance. Lastly, the chapter also explains which variant is the best candidate for the design of fully CMOS differential PA targeted for the specifications of the *WiFi 802.11n* application.

## 2.1. Continuous Class F

Generalized drain source voltage ($V_{DS}$) containing all frequencies up to fourth harmonic [1] is given by:

$$V_{DS} = (1 - \alpha \cos\theta)^2 (1 + \beta \cos\theta)(1 - \gamma \sin\theta) \tag{2.1}$$

where $\theta$ is the conduction angle. Variables $\alpha$, $\beta$, and $\gamma$ will be solved in this section. On expanding the above equation,

$$\begin{aligned} V_{DS} = {} & \left(1 + \frac{\alpha^2}{2} - \alpha\beta\right) - \left(2\alpha - \beta - \frac{3}{4}\alpha^2\beta\right)\cos\theta + \gamma\left(\frac{\alpha\beta}{2} - 1 - \frac{\alpha^2}{4}\right)\sin\theta - \\ & \left(\alpha\beta - \frac{\alpha^2}{2}\right)\cos 2\theta + \gamma\left(\alpha - \frac{\beta}{2} - \frac{\alpha^2\beta}{4}\right)\sin 2\theta - \left(\frac{\alpha^2\beta}{4}\right)\cos 3\theta + \\ & \gamma\left(\frac{\alpha\beta}{2} - \frac{\alpha^2}{4}\right)\sin 3\theta - \frac{\alpha^2\beta\gamma}{8}\sin 4\theta \end{aligned} \tag{2.2}$$

Second harmonic impedance must be kept reactive (real part = *0*) to achieve the maximum drain efficiency ($\eta_D$):

$$\Longrightarrow \ \beta = \alpha/2$$

Then, differentiate voltage amplitude of fundamental to find its maximum peak

$$\Longrightarrow \alpha = \frac{2}{\sqrt{3}}$$

Now, $V_{DS}$ after substitution is shown below:

$$V_{DS} = \underbrace{1}_{\text{DC}} \underbrace{- \frac{2}{\sqrt{3}} \cos\theta - \gamma \sin\theta}_{\text{Fundamental}} + \underbrace{\frac{7\gamma}{6\sqrt{3}} \sin 2\theta}_{\text{Second harmonic}} + \underbrace{\frac{1}{3\sqrt{3}} \cos 3\theta}_{\text{Third harmonic}} \tag{2.3}$$

Drain current ($I_D$) is a half sinusoid which is similar to Class F and is given by:

$$I_D = \underbrace{\frac{1}{\pi}}_{\text{DC}} + \underbrace{\frac{1}{2} \cos\theta}_{\text{Fundamental}} + \underbrace{\frac{2}{3\pi} \cos 2\theta}_{\text{Second harmonic}} - \underbrace{\frac{2}{15\pi} \cos 4\theta}_{\text{Fourth harmonic}} \tag{2.4}$$

It is clearly seen that $V_{DS}$ and $I_D$ are chosen in such a way that no power is dissipated at higher harmonics [2].

### 2.1.1. Drain efficiency of Continuous Class F

DC power:

$$P_{DC} = 1 * \frac{1}{\pi} = \frac{1}{\pi} \tag{2.5}$$

Fundamental power:

$$P_{FUND} = \frac{1}{2}\left(\frac{2}{\sqrt{3}}\right)\left(\frac{1}{2}\right) = \frac{1}{2\sqrt{3}} \tag{2.6}$$

Power dissipated in device:

$$P_{\text{DEV}} = \frac{1}{2\pi}\int_0^{2\pi} V_{DS} I_D = \frac{1}{2\pi}\left(\frac{1}{\pi} * 2\pi - \frac{2}{\sqrt{3}} * \frac{1}{2} * \int_0^{2\pi} \frac{1+\cos 2\theta}{2}\right) = \frac{1}{\pi} - \frac{1}{2\sqrt{3}} \tag{2.7}$$

All terms comprising of $\cos n\theta$ and $\sin m\theta$ (where *n = 1, 2, 3, 4* and *m = 1, 2*) will evaluate to *0* under the integral *0* to $2\pi$ except $\cos^2\theta$.
Drain efficiency ($\eta_D$):

$$\eta_D = \frac{P_{FUND}}{P_{DC}} = \frac{\pi}{2\sqrt{3}} = 90.7\ \% \tag{2.8}$$

From Equation 2.8, it is seen that $\gamma$ doesn't affect $\eta_D$ mathematically. But voltage waveform's shape (peak factor) depends on $\gamma$ which is shown in Figure 2.1. But in reality, $I_D$ depends on $V_{DS}$, so $\eta_D$ will have an impact with respect to $\gamma$. This is shown in Figure *2* in [3] which is a device simulation. Thus, $\eta_D$ reduces as $\gamma$ increases in a practical scenario.

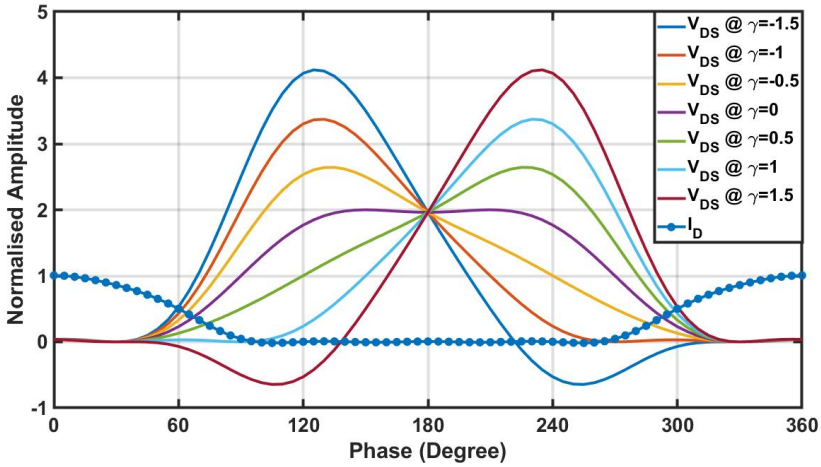



**Figure 2.1:** $V_{DS}$ and $I_D$ waveform for CCF with *-1.5 < $\gamma$ < 1.5*

From Figure 2.1, it is seen that at $\gamma$ = *0*, waveform is identical to Class F. Also, $V_{DS}$ remains positive for the range $-1 < \gamma < 1$. It is necessary to keep $V_{DS}$ positive so that it doesn't perform as switching PA and has a good linearity. Figure 2.1 indicates that peak factor increases if $\gamma \neq 0$ and reaches a value of *3.12* times supply ($V_{DD}$) when $\gamma$ = *-1* or *1*.

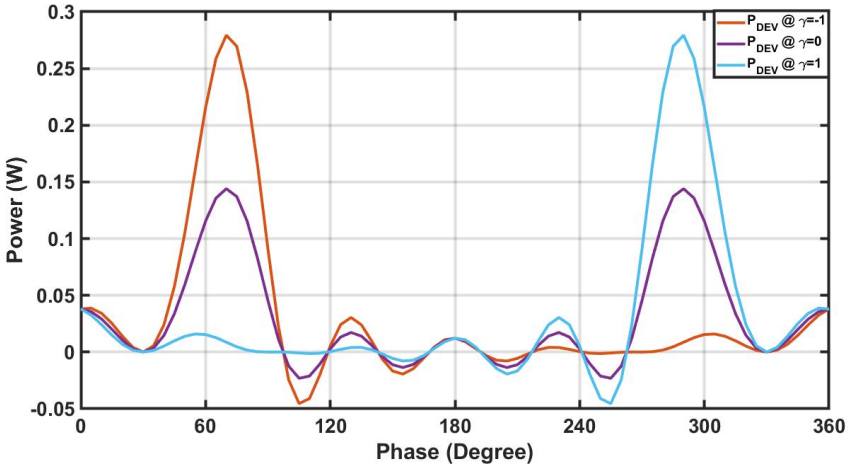



**Figure 2.2:** Device power ($P_{DEV}$) for CCF with $\gamma$ = *-1, 0 ,1*

From the Figure 2.2, it is evident that power consumed by transistor, $P_{DEV}$ (area under the curve) is constant for $\gamma$ = *-1, 0, 1*. Thus, proving that $\eta_D$ in CCF is independent of $\gamma$.

From Equation 2.3 and 2.4, load impedance at fundamental ($Z_{1f}$), second ($Z_{2f}$) and third harmonic ($Z_{3f}$) bands are [4]

$$\begin{aligned} Z_{1f} &= \frac{4}{\sqrt{3}} + j2\gamma = \frac{2}{\sqrt{3}}R_{CCF} + jR_{CCF}\gamma \\ Z_{2f} &= 0 - j\frac{\pi}{2}\frac{7\sqrt{3}}{6}\gamma = 0 - j\frac{\pi}{2}R_{CCF}\gamma \\ Z_{3f} &= \infty \end{aligned} \tag{2.9}$$

In Equation 2.9, $\frac{7\sqrt{(3)}}{6} = 2.02$ and $R_{CCF}$ can be assumed as *2*.

In CCF, $Z_{3f}$ remains open-circuited similar to Class F. Meanwhile, $Z_{1f}$ and $Z_{2f}$ has a reactive part, unlike Class F. From the Figure 2.3, it is observed that if the reactive part of $Z_{1f}$ decreases, then the reactive part of $Z_{2f}$ increases. Thus, showing that the reactive part of $Z_{1f}$ is inversely proportional to the reactive part of $Z_{2f}$.

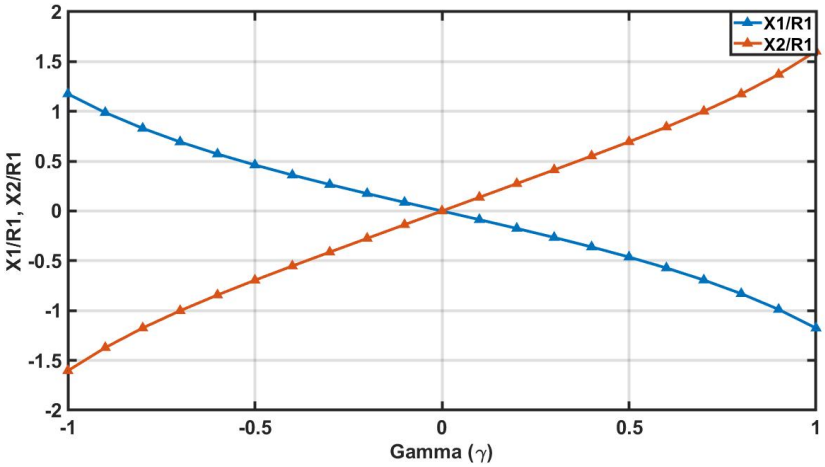



**Figure 2.3:** Fundamental reactive impedance (X1) and second harmonic reactive impedance (X2) normalized to fundamental real impedance (R1) as a function of $\gamma$

Figure 2.4 explains that

- $Z_{1f}$ is on constant resistance circle. Reactive part of $Z_{1f}$ changes from inductive to capacitive as $\gamma$ increases;
- $Z_{2f}$ is on edge of the smith chart. Thus, confirming that it has only a reactive part. Also, reactive changes from capacitive to inductive as $\gamma$ increases;
- $Z_{3f}$ is open-circuited.

The key point in this new PA mode lies in varying the reactive part of the $Z_{1f}$ and $Z_{2f}$ in accordance with Equation 2.9. By doing so, voltage waveform can be main-

tained above zero and also maintain a constant high-efficiency state and maximum output power.

This set of viable loads gives a new design space which increases flexibility in PA design. The most important observation to highlight is that PA designers don't necessarily need to provide a short-circuit at $Z_{2f}$, but have a choice of a significantly wider design space over which maximum $\eta_D$ is maintained. Thus, helping to operate in a wider bandwidth [2].



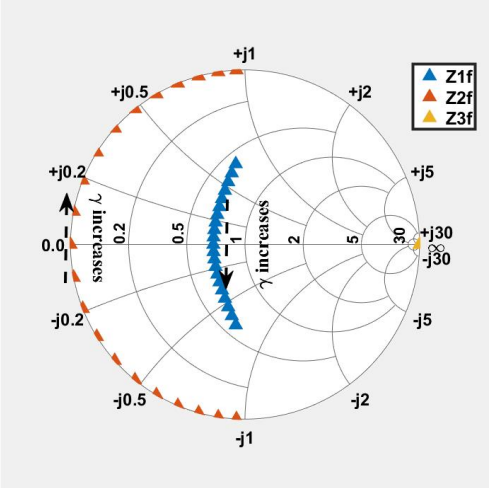



**Figure 2.4:** Smith chart showing variation of $Z_{1f}$, $Z_{2f}$, $Z_{3f}$ for *-1 < γ < 1*

## 2.2. Extended Continuous Class F

Drain source voltage ($V_{DS}$) in Equation 2.1 is

$$V_{DS} = (1 - \alpha \cos\theta)^2 (1 + \beta \cos\theta)(1 - \gamma \sin\theta)$$

In Extended Continuous Class F (ECCF), $\alpha$ and $\beta$ are also varied instead of choosing $\alpha = \frac{2}{\sqrt{3}}$ and $\beta = \frac{\alpha}{2}$. This gives us a larger design space while designing CCF.
There are *2* cases:

- If $\beta = \frac{\alpha}{2}$, then the $Z_{2f}$ will be on edge of the smith chart;
- If $\beta > \frac{\alpha}{2}$, then the $Z_{2f}$ will move into the smith chart.

### 2.2.1. Drain efficiency of Extended Continuous Class F

Similar to subsection 2.1.1, $\eta_D$ of ECCF is calculated from $V_{DS}$ (Equation 2.2) and $I_D$ (Equation 2.4).
DC power:

$$P_{DC} = \frac{1}{\pi}\left(1 + \frac{\alpha^2}{2} - \alpha\beta\right) \tag{2.10}$$

Fundamental power:

$$P_{FUND} = \frac{1}{2}\left(\beta - 2\alpha + \frac{3\alpha^2\beta}{4}\right) \tag{2.11}$$

Drain efficiency ($\eta_D$):

$$\eta_D = \frac{P_{FUND}}{P_{DC}} = \frac{\frac{1}{2}\left(\beta - 2\alpha + \frac{3\alpha^2\beta}{4}\right)}{\frac{1}{\pi}\left(1 + \frac{\alpha^2}{2} - \alpha\beta\right)} \tag{2.12}$$

From Equation 2.12, it is seen that $\eta_D$ depends on $\alpha$ and $\beta$. The section 2.1 shows CCF which delivers the maximum $\eta_D$ because the value of $\alpha = \frac{2}{\sqrt{3}}$ was chosen in order to represent the standard Class F condition, having an $\eta_D$ of *90.7%*. In ECCF, by varying $\alpha$, $\beta$ and $\gamma$, $\eta_D$ (for example greater than *75%*) can be maintained over a wider design space than CCF explained in section 2.1.

### 2.2.2. Extended Continuous Class-F with second harmonic impedance on the edge of the smith chart ($\beta = \frac{\alpha}{2}$)

In order to avoid that $V_{DS}$ waveform drop below *0*, for $\beta = \frac{\alpha}{2}$ , the below conditions must be achieved:

$$\begin{aligned} &-2 \le \alpha \le 2, \quad \alpha \neq 0 \\ &-1 \le \gamma \le 1 \end{aligned} \tag{2.13}$$

The range of $\alpha$ and $\beta$ shown in Equation 2.13 will be smaller taking into account different values of $\beta$.

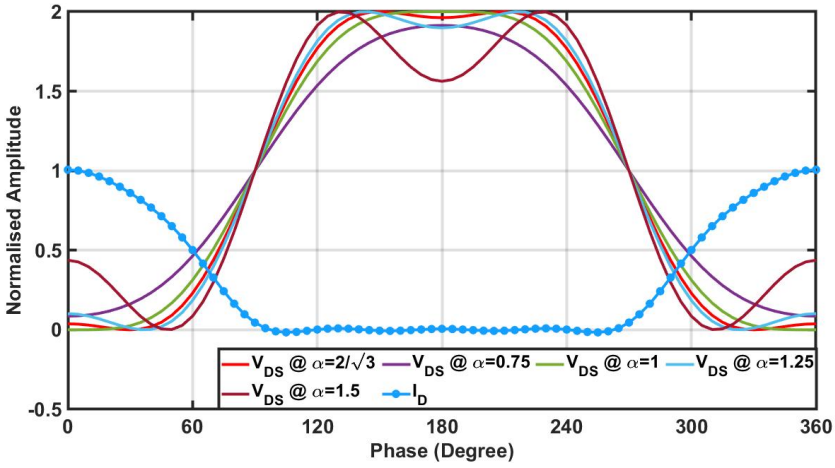



**Figure 2.5:** $V_{DS}$ and $I_D$ waveform for ECCF with *0.75* < $\alpha$ < *1.5*, $\beta = \alpha/2$ and $\gamma$ = *0*

From Figure 2.5, we can see that with increasing values of $\alpha$, bigger "troughs" are formed in the $V_{DS}$ waveform. This means lower fundamental voltage which directly leads to a lower $\eta_D$.

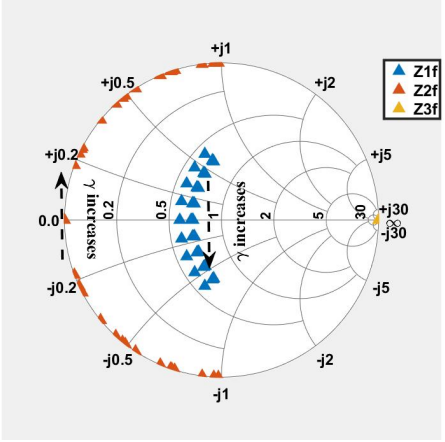



**Figure 2.6:** Smith chart showing variation of $Z_{1f}$, $Z_{2f}$ and $Z_{3f}$ for *0.75 < α < 1.25*, $\beta = \frac{\alpha}{2}$ and *-1 < γ < 1*

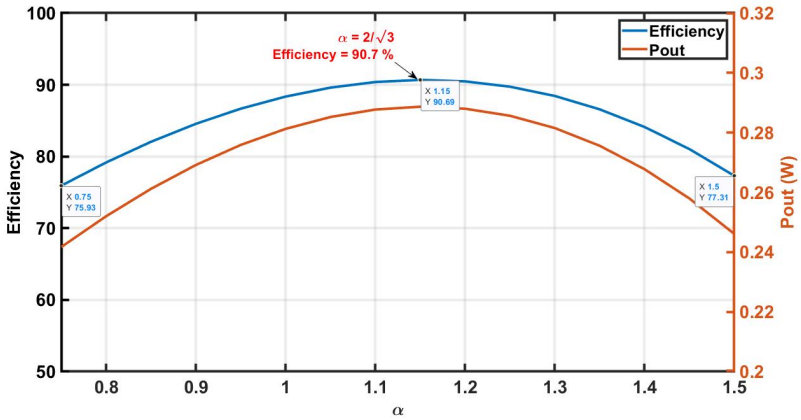



**Figure 2.7:** Drain efficiency ($\eta_D$) and $P_{OUT}$ for constant $\beta = \alpha/2$ and $\gamma = 0$ as a function of $\alpha$, where *0.75 < α < 1.5*

Assuming a constant value of $\beta = \frac{\alpha}{2}$ and varying the $\alpha$ and $\gamma$ shows that the $Z_{2f}$ still varies on the edge of the smith chart, while the $Z_{1f}$ varies both in magnitude and phase as shown in Figure 2.6. For *0.75 < α < 1.5*, efficiencies are above *75%* which is shown in Figure 2.7. In Figure 2.7, the highest $\eta_D$ is achieved for $\alpha = \frac{2}{\sqrt{3}}$,

which is the Class F condition. But there exists a larger design space from which a range of $Z_{1f}$ can be chosen, which still provides efficiencies greater than *75%*. Those theoretical values of output power ($P_{OUT}$) and $\eta_D$ remain constant over the range of *-1* < $\gamma$ < *1*.

$V_{DS}$ waveform can be maintained above *0*, if the parameter $\alpha$ satisfy criteria specified in Equation 2.13. But, to maintain $\eta_D$ greater than the specified value (for example *75%*), the range of $\alpha$ has to be further reduced which is shown below.

$$0.75 \leq \alpha \leq 1.5$$

### 2.2.3. Extended Continuous Class-F with second harmonic impedance inside the smith chart ($\beta > \frac{\alpha}{2}$)

In this case, $\beta$ is not restricted to $\beta = \frac{\alpha}{2}$ as in the previous section. These conditions deliver a larger range of design space which provides $\eta_D$ greater than *75%*.

| $\beta = \alpha/2$ | $\beta = \alpha/1.9$ | $\beta = \alpha/1.8$ | $\beta = \alpha/1.7$ | $\beta = \alpha/1.6$ | $\beta = \alpha/1.5$ | $\beta = \alpha/1.4$ |
|---|---|---|---|---|---|---|
| 0.75<$\alpha$<1.5 | 0.75<$\alpha$<1.45 | 0.8<$\alpha$<1.45 | 0.8<$\alpha$<1.35 | 0.85<$\alpha$<1.3 | 0.9<$\alpha$<1.2 | $\alpha$=1.05 |
| -1<$\gamma$<1 | -1<$\gamma$<1 | -1<$\gamma$<1 | -0.9<$\gamma$<0.9 | -0.5<$\gamma$<0.5 | -0.2<$\gamma$<0.2 | $\gamma$=0 |

**Table 2.1:** Design space for which the $V_{DS}$ is positive and the drain efficiency ($\eta_D$) is greater than *75%* [2]

Table 2.1 shows a span of $\alpha$ and $\gamma$ values which gives a non-zero crossing $V_{DS}$ waveform and a minimum $\eta_D$ of *75%*. It is seen that as $\beta$ increases, the range of $\alpha$ and $\gamma$ to achieve non-zero $V_{DS}$ waveform and $\eta_D$ of *75%* reduces.

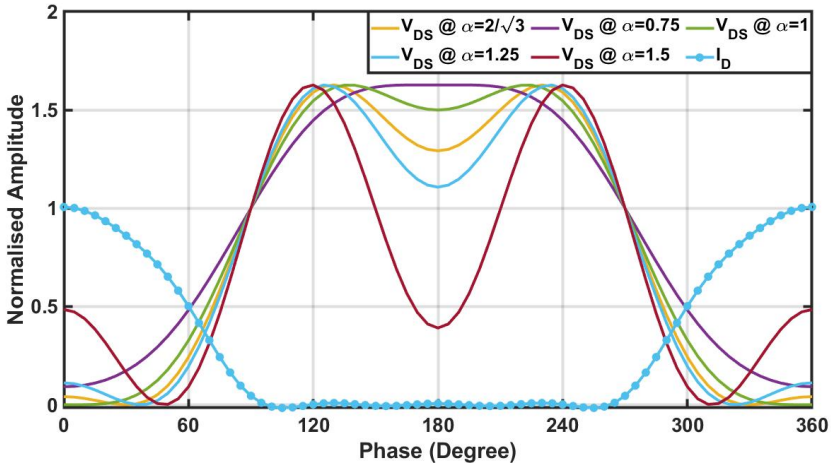



**Figure 2.8:** $V_{DS}$ and $I_D$ waveforms for constant $\beta = \alpha/1.6$ and $\gamma = 0$ as a function of $\alpha$, where *0.75* < $\alpha$ < *1.5*

Figure 2.8 shows that with an increasing value of $\alpha$, bigger troughs are formed in the $V_{DS}$ waveforms which leads to lower $\eta_D$.

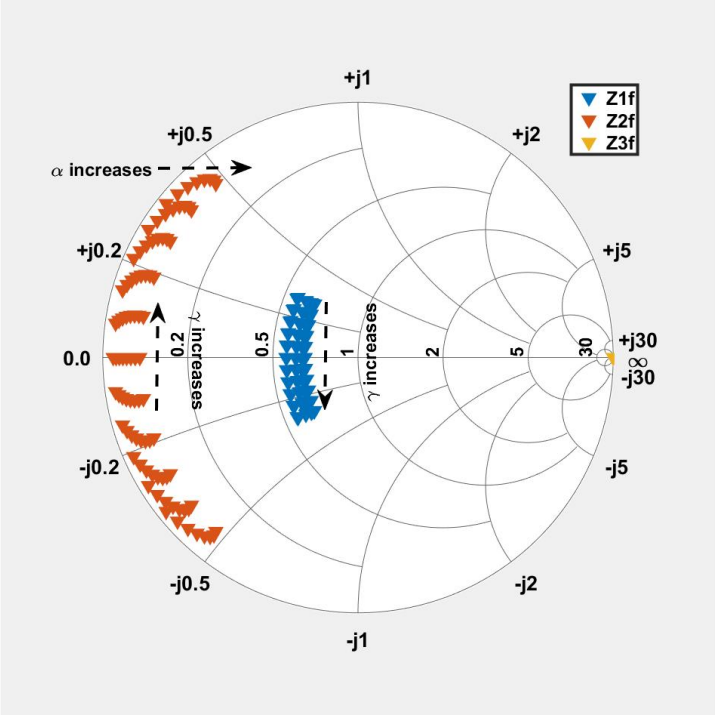



**Figure 2.9:** Smith chart showing variation of $Z_{1f}$, $Z_{2f}$ and $Z_{3f}$ for $\beta = \alpha/1.9$ when varying *0.75* < $\alpha$ < *1.45* and *-1* < $\gamma$ < *1*

Figure 2.9 shows load impedance for *-1* < $\gamma$ < *1* and *0.75* < $\alpha$ < *1.45* and it confirms that

- $Z_{1f}$ is not on constant resistance circle anymore;
- $Z_{2f}$ is inside the smith chart which validates it has a real part too. It is also seen that as $\alpha$ increases, $Z_{2f}$ moves inside. Thus, increasing real part of $Z_{2f}$;
- $Z_{3f}$ is open-circuited.

From Figure 2.9, it is seen that each $Z_{1f}$ has its appropriate $Z_{2f}$. By choosing these values, we can achieve $\eta_D$ above *75%*.

Since $\beta$ value has increased, the range of $\alpha$ to achieve non-zero $V_{DS}$ waveform and $\eta_D$ above *75%* has reduced from *0.75* < $\alpha$ < *1.5* to *0.85* < $\alpha$ < *1.3*, as shown in Figure 2.10. For the case of $\beta = \alpha/1.4$, there is only one point of $\alpha$ and $\gamma$ which provides nonzero $V_{DS}$ waveform and $\eta_D$ above *75%*.

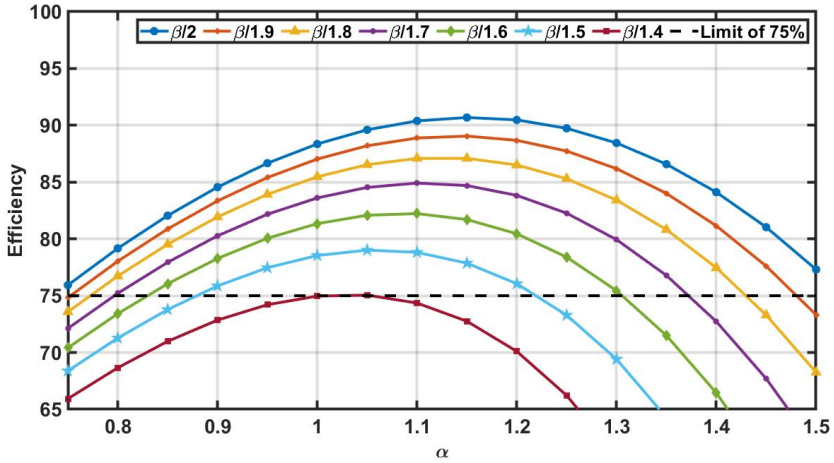



**Figure 2.10:** Drain efficiency ($\eta_D$) as a function of $\alpha$ and $\beta$ for constant $\gamma = 0$

Figure 2.11 shows the maximum $\eta_D$ as a function of $\beta$ for a given optimum $\alpha$. It is seen that the $\eta_D$ decreases with increasing values of $\beta$, but efficiencies greater than *75%* are still maintained [2].

This variant of ECCF allows us to have a real part at $Z_{2f}$, unlike CCF explained in section 2.1 and ECCF explained in subsection 2.2.2. Thus, further increasing design space and flexibility for PA designers.

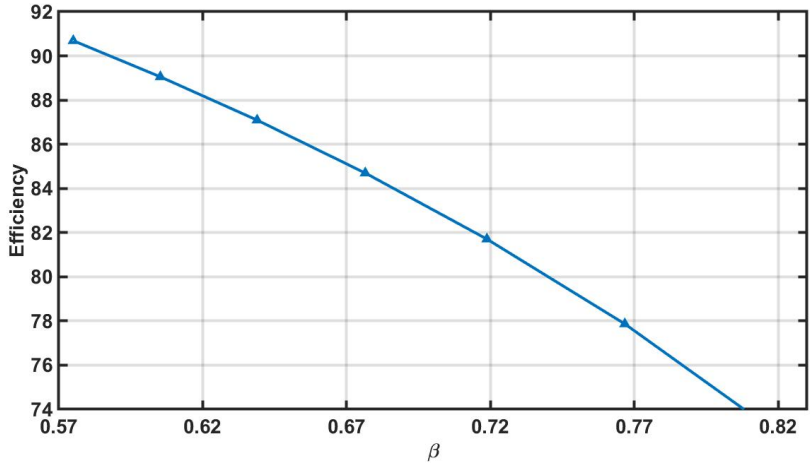



**Figure 2.11:** Drain efficiency ($\eta_D$) of ECCF as a function of $\beta$ for $\gamma = 0$ and optimum value of $\alpha = 1.15$

## 2.3. Conclusion

This chapter explained the concept of Continuous Class F (CCF) and Extended Continuous Class F (ECCF). After understanding and analyzing different classes of PA for $\eta_D$ and linearity, CCF (considering up to $3^{rd}$ harmonic) will be the best candidate for the *WiFi 802.11n* application with targeted bandwidth of *2.1 - 2.7 GHz* (*600 MHz*). It has a higher $\eta_D$ (*90.7%*) than Class A, B, and AB. Also, it is more linear than Class C, and switching PAs like Class D and E. ECCF provides the flexibility of the real part in $Z_{2f}$ and variable real part in $Z_{1f}$. But this happens at the cost of $\eta_D$. Since $\eta_D$ and linearity is the most critical and crucial factors, CCF has been chosen over ECCF.



## References

[1] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt, *On the continuity of high efficiency modes in linear rf power amplifiers,* IEEE Microwave and Wireless Components Letters **19**, 665 (2009).

[2] V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, *On the extension of the continuous class-f mode power amplifier,* IEEE Transactions on Microwave Theory and Techniques **59**, 1294 (2011).

[3] N. Tuffy, L. Guan, A. Zhu, and T. J. Brazil, *A simplified broadband design methodology for linearized high-efficiency continuous class-f power amplifiers,* IEEE Transactions on Microwave Theory and Techniques **60**, 1952 (2012).

[4] S. N. Ali, P. Agarwal, S. Gopal, S. Mirabbasi, and D. Heo, *A 25–35 ghz neutralized continuous class-f cmos power amplifier for 5g mobile communications achieving 26% modulation pae at 1.5 gb/s and 46.4% peak pae,* IEEE Transactions on Circuits and Systems I: Regular Papers **66**, 834 (2019).

# 3

# Design of output network

This chapter unravels the design of four output networks which satisfies the requirements of CCF. Before explaining the design of each output network, the calculation for the impedance that is needed to be presented at the drain of the differential pair to obtain the required peak output power ($P_{OUT}$) is described below.

## 3.1. Impedance calculation

Assuming there is a *2 dB* loss in the output network and the peak $P_{OUT}$ requirement is *25 dBm*, then *27 dBm* should be considered as the peak $P_{OUT}$ in the ideal case to meet the requirement.

As explained in the previous chapter, only up to the $3^{rd}$ harmonics in voltage are considered.

Peak output power:

$$\text{Peak } P_{OUT} = 27\ dBm$$

$$\text{Peak } P_{OUT} = 501.19\ mW$$

Supply voltage ($V_{DD}$),

$$V_{DD} = 2.7\ V$$

Single ended voltage swing

$$V_{FUND}(SE) = \frac{2}{\sqrt{3}} V_{DD} = 3.12\ V \tag{3.1}$$

Since only *3* harmonics are considered, $V_{DD}$ is multiplied by $\frac{2}{\sqrt{3}}$ and not $\frac{4}{\pi}$ as in ideal Class F with all harmonics considered [1].

Differential ended voltage swing:

$$V_{FUND}(DE) = 2^{*} V_{FUND}(SE) = 6.24\ V$$

Impedance to be seen at the drains of the differential pair to get the required peak $P_{OUT}$ of *27 dBm* is

$$R_D(DE) = \frac{V_{FUND}(DE)^2}{2 * \text{Peak } P_{OUT}} = 38.7\ \Omega \tag{3.2}$$

## 3.2. Output network requirements



| Class of Operation | First Harmonic ($\omega_0$) | Second Harmonic ($2\omega_0$) | Third Harmonic ($3\omega_0$) |
|---|---|---|---|
| **Class F (2.4 GHz)** | $\Re(Z_D)$ = 38.7 Ω | $\Re(Z_D)$= 0 Ω | $\|Z_D\|$ needs to be high (≈ 1000 Ω). |
| | $\Im(Z_D)$ = 0 Ω | $\Im(Z_D)$ = 0 Ω | |
| **CCF (2.1 - 2.7 GHz)** | $\Re(Z_D)$ = 38.7 Ω | $\Re(Z_D)$ = 0 Ω | $\|Z_D\|$ needs to be high (≈ 1000 Ω). |
| | $\Im(Z_D)$ need to change from + to - OR $\Im(Z_D)$ need to change from - to + | $\Im(Z_D)$ need to change from - to + OR $\Im(Z_D)$ need to change from + to - | |

**Table 3.1:** Output network requirements at $1^{st}$, $2^{nd}$ and $3^{rd}$ harmonic

From Table 3.1, it is seen that the PA operates in the standard Class F mode at *2.4 GHz* with a short at $2^{nd}$ harmonic and an open at $3^{rd}$ harmonic. But, for all other frequencies, the PA performs in the CCF mode. One main conclusion that can be drawn from the above table is that if the reactive part at $1^{st}$ harmonic changes from inductive to capacitive, then the reactive part at $2^{nd}$ harmonic needs to change from capacitive to inductive. Thus, suggesting that the reactive part at the $1^{st}$ and $2^{nd}$ harmonic needs to have an inverse relation.

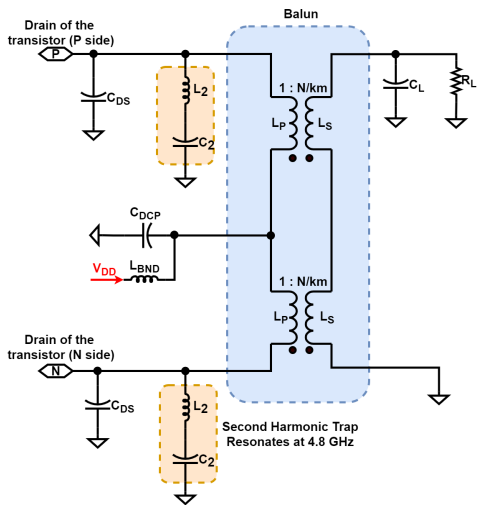
The four output networks which satisfy CCF are given below (refer Figure 3.1):

- *Design A*
  It has a balanced to unbalanced (balun), second harmonic trap ($L_2C_2$) and output load capacitance ($C_L$);
- *Design B*
  It has a balun and output load capacitance ($C_L$);
- *Design C*
  It has a balun, RF choke, second harmonic trap ($L_2C_2$) and output load capacitance ($C_L$);
- *Design D*
  It has a balun, RF choke and output load capacitance ($C_L$).

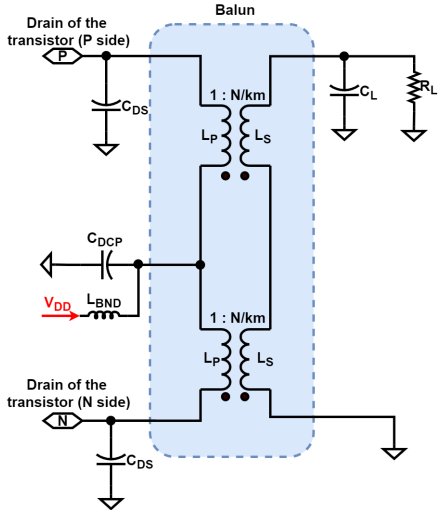
The balun and $C_L$ are present in all the four designs (refer Figure 3.1). Since it is a differential PA, the balun does the necessary function of converting differential-

ended signal (balanced) to a single-ended signal (unbalanced) as the load (antenna) is single-ended. The significance of $C_L$ is explained in the section 3.3.

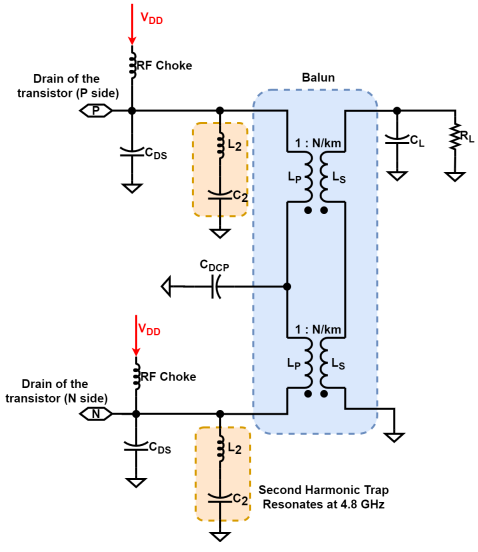




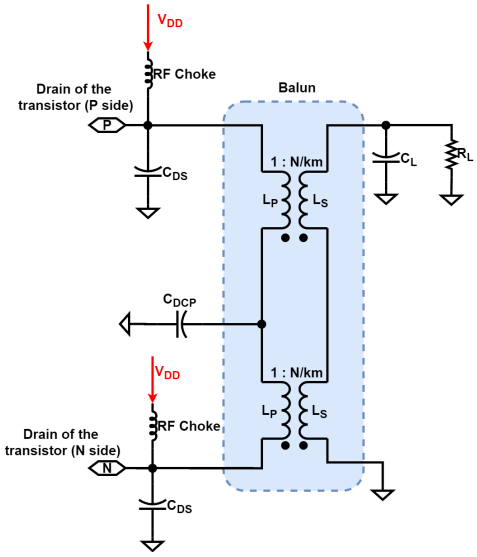

**(a)** *Design A* (no RF choke and with $L_2C_2$)




**(b)** *Design B* (no RF choke and no $L_2C_2$)




**(c)** *Design C* (with RF choke and with $L_2C_2$)




**(d)** *Design D* (with RF choke and no $L_2C_2$)

**Figure 3.1:** Output network designs

## 3.3. Design A (Balun, second harmonic trap and output capacitance)

Drain source capacitance of the transistor ($C_{DS}$) is *1.87 pF* in Figure 3.2. This is calculated in the Appendix A after the output stage was designed and it remains the same for the design of all other output networks. $C_{DCP}$ = *100 pF* is the decoupling capacitor which is added to provide RF ground and blocks DC. $L_{BND}$ is used to model bond wire inductance from the $V_{DD}$, and the value is approximated as *1 nH*. $V_{DD}$ is fed through the center tap of the balun. The second harmonic trap ($L_2C_2$) is a series resonator at second harmonic (*4.8 GHz*) and thereby, creating a short at the same frequency. The balun is modelled using ideal transformer, magnetizing inductance ($L_m$), leakage inductance ($L_k$) and coupling coefficient ($km$) as explained in [2]. $L_m$ and $L_k$ are related to primary inductance ($L_P$) by the below formula.

$$L_k = (1 - km^2) * L_P \tag{3.3}$$

$$L_m = km^2 * L_P \tag{3.4}$$

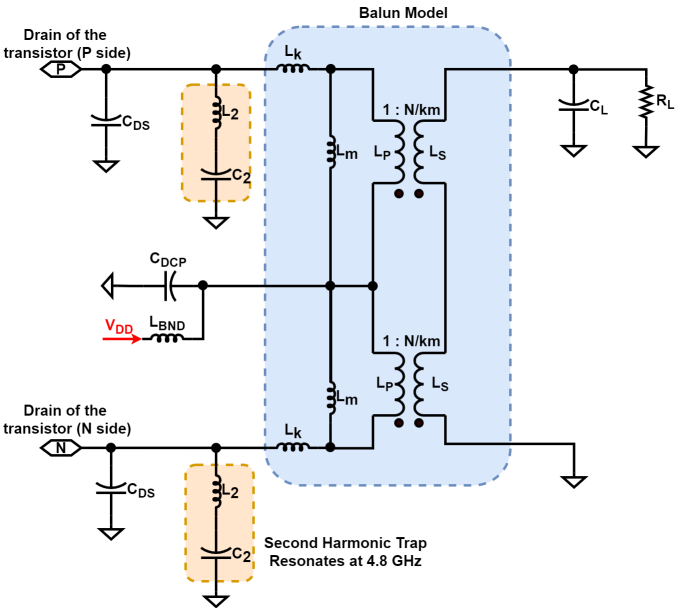



**Figure 3.2:** Schematics of *Design A* (balun, $L_2C_2$ and $C_L$)

From Figure 3.3, it is seen that the following conditions have to be satisfied to obtain real part of the drain impedance ($R_D$) as *38.7* Ω and reactive part of the drain impedance ($X_D$) as *0* Ω at $\omega_0$ (*2.4 GHz*). $Z_{SB}$ represents the total impedance of second harmonic trap ($L_2C_2$) and balun.

$$R_{SB}(\omega_0) = 29.83\ \Omega \tag{3.5}$$

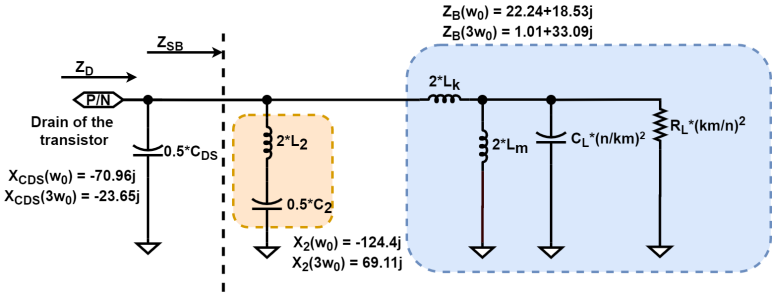



**Figure 3.3:** Differential mode equivalent circuit of *Design A* (balun, $L_2C_2$ and $C_L$)

$$X_{SB}(\omega_0) = 16.63\ \Omega \tag{3.6}$$

In order to obtain high impedance at the drain of the transistor at $3\omega_0$ (*7.2 GHz*), $C_{DS}$ needs to resonate out with the reactive part ($X_{SB}$) of $Z_{SB}$ (total impedance of $L_2C_2$ and balun).

$$X_{SB}(3\omega_0) = 24.96\ \Omega \tag{3.7}$$

Ideally, the real part should be *0* to obtain high impedance at $3^{rd}$ harmonic. As seen in Figure 3.4, as the value of the real part increases, the magnitude of impedance at $3^{rd}$ harmonic reduces exponentially. Figure 3.4 also shows the significance of $C_L$ as it is required to short the load resistance $R_L$ (*50* $\Omega$). Thus, helping to obtain high impedance at $3^{rd}$ harmonic. That's why, all four designs have $C_L$.

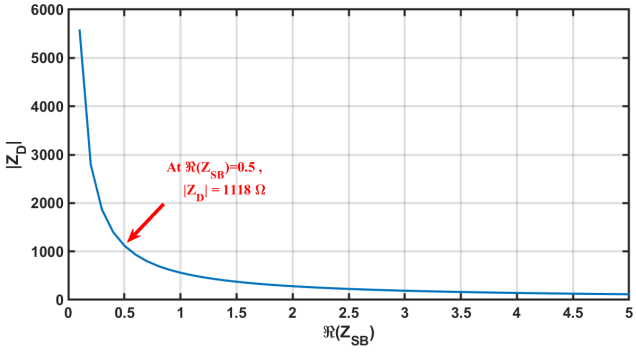
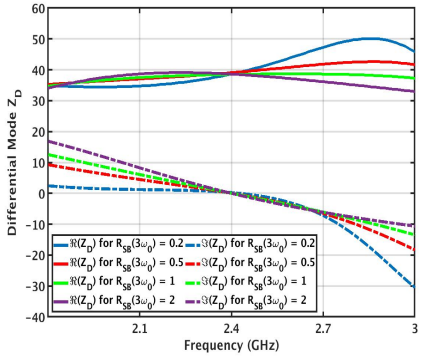
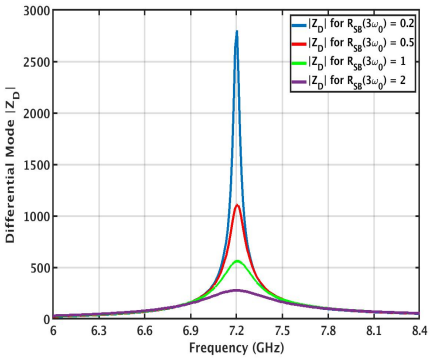



**Figure 3.4:** Magnitude of $Z_D$ versus the real part of $Z_{SB}$ at $3^{rd}$ harmonic

From Figure 3.5a, it is seen that having a larger $R_{SB}(\omega_0)$ helps to have a more flatter real part at $1^{st}$ harmonic, thus helping to get constant $P_{OUT}$ across the band-width of *2.1 - 2.7 GHz*. But this is at the expense of lower impedance at $3^{rd}$ harmonic. Also, increasing $R_{SB}(3\omega_0)$ helps to get a more linear imaginary part at $1^{st}$ harmonic.




**(a)** Real part ($\Re$) and reactive part ($\Im$) at $1^{st}$ harmonic




**(b)** Magnitude at $3^{rd}$ harmonic

**Figure 3.5:** Impedance ($Z_D$) at $1^{st}$ and $3^{rd}$ harmonic for different values of $R_{SB}(3\omega_0)$

The assumption is made to obtain *1000* Ω at $3^{rd}$ harmonic for all designs. This assumption helps to compare all the designs on the same scale and reduce the effect of $3^{rd}$ harmonic. In section 4.4, it is demonstrated that $3^{rd}$ harmonic impedance doesn't have much influence on important parameters like maximum drain efficiency ($\eta_D$) and output 1 dB compression point ($OP1dB$).
*1000* Ω can be achieved with

$$R_{SB}(3\omega_0) = 0.5\ \Omega \tag{3.8}$$

There are *5* unknowns in the circuit: transformer coupling ($km$), turn ratio in the transformer ($N$), primary inductance ($L_P$), capacitor for second harmonic trap ($C_2$), and output capacitance ($C_L$). Assuming $km = 0.8$ (variation of $km$ is explained in section 7.2) and using four Equation 3.5, 3.6, 3.7 and 3.8, the remaining unknowns can be calculated. *Maple 2018.2* is used to find solutions of the above-mentioned equations.

$$N = 1.34$$

$$L_P = 2.2\ nH$$

$$C_L = 0.9\ pF$$

$$C_2 = 1.5\ pF$$

From Figure 3.6, it is evident that $L_2C_2$ should have a series resonance at $2\omega_0$ (*4.8 GHz*) to get short at the same frequency.

$$L_2 = \frac{1}{4 * \omega_0^2 * C_2} = 0.73\ nH \tag{3.9}$$

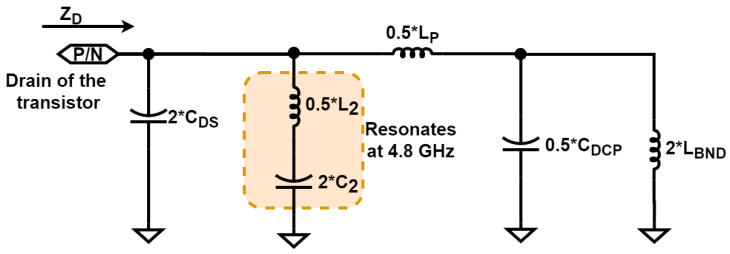



**Figure 3.6:** Common mode equivalent circuit of *Design A* (balun, $L_2C_2$ and $C_L$)



## 3.4. Design B (Balun and output capacitance)

In this design, $L_2C_2$ is removed. The $V_{DD}$ is provided through the center tap of the balun and bond wire ($L_{BND} \approx 1$ *nH*) as in the previous design.

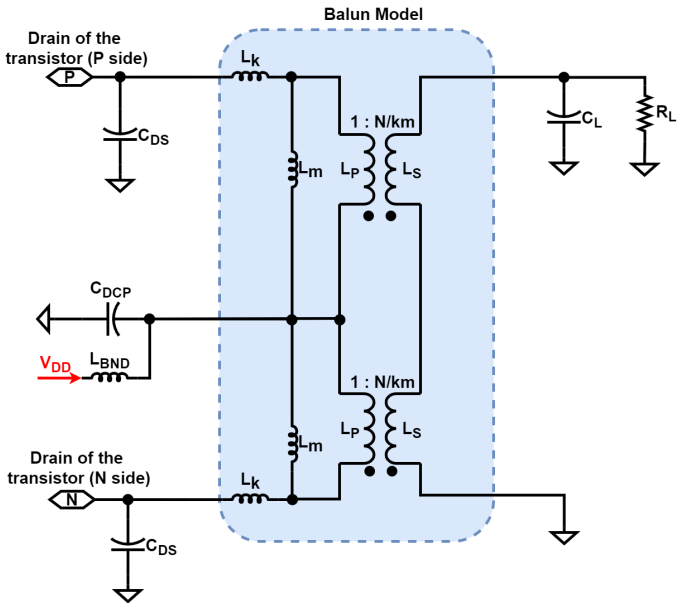



**Figure 3.7:** Schematics of *Design B* (balun and $C_L$)

The following criteria have to be satisfied to obtain $R_D = 38.7\ \Omega$ and $X_D = 0\ \Omega$ at $\omega_0$ (*2.4 GHz*).

$$R_B(\omega_0) = 29.83\ \Omega \tag{3.10}$$

$$X_B(\omega_0) = 16.27\ \Omega \tag{3.11}$$

In order to obtain high impedance at the drain of the transistor at $3\omega_0$ (*7.2 GHz*), $C_{DS}$ needs to resonate out with the reactive part of $Z_B$.

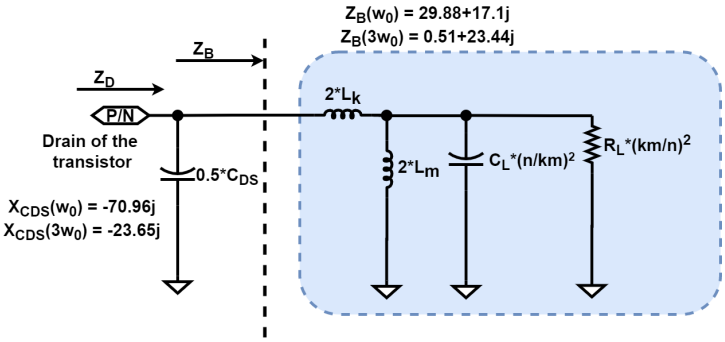



**Figure 3.8:** Differential equivalent half circuit of *Design B* (balun and $C_L$)

$$X_B(3\omega_0) = 23.65\ \Omega \tag{3.12}$$

The below mentioned condition has to be met to obtain *1000* $\Omega$ at $3^{rd}$ harmonic as discussed in the previous design.

$$R_B(3\omega_0) = 0.5\ \Omega \tag{3.13}$$

There are *4* unknowns in the circuit: $km$, $N$, $L_P$ and $C_L$. Using four Equation 3.10, 3.11, 3.12 and 3.13, the above-mentioned unknowns can be computed.

$$km = 0.72$$

$$N = 0.9$$

$$L_P = 0.63\ nH$$

$$C_L = 3.96\ pF$$

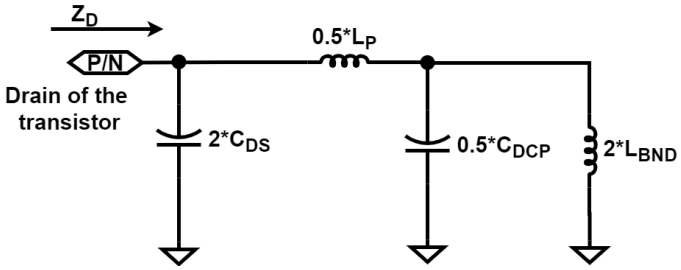



**Figure 3.9:** Common mode equivalent circuit of *Design B* (balun and $C_L$)

From Figure 3.9, $C_{DCP}$ can be tuned such that $C_{DCP}$ resonates with $L_P$, $L_{BND}$ and $C_{DS}$ to provide a short at $2\omega_0$ (*4.8 GHz*). Apart from this task, $C_{DCP}$ also provides RF ground and blocks DC.

$$C_{DCP} = 4.58\ pF \tag{3.14}$$

## 3.5. Design C (Balun, RF choke, second harmonic trap and output capacitance)

The main motivation to use RF choke in *Design C* and *Design D* is that *CATENA MICROELECTRONICS B.V* already had a well-designed RF choke. Also, their earlier products had RF choke so replacing the old PA with the new one in the WiFi chip will be easier. In Figure 3.10, RF chokes have inductance of *5 nH* each. $C_{DCP}$ *= 100 pF* is the decoupling capacitor which is added to provide RF ground and to block DC.



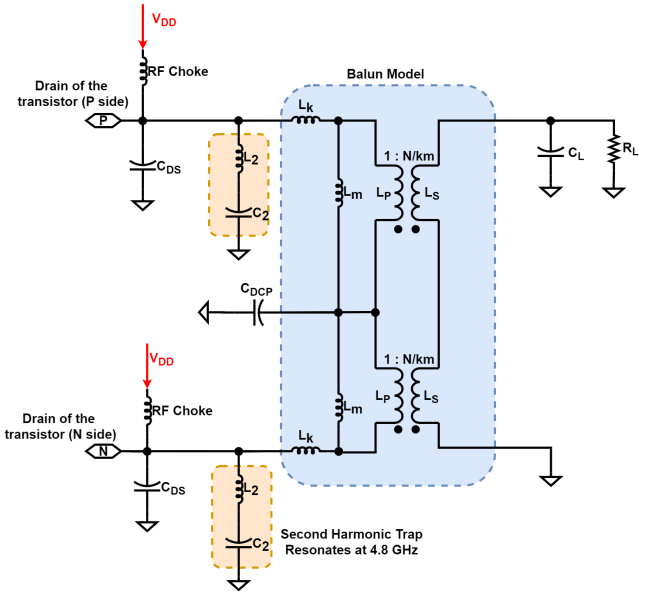



**Figure 3.10:** Schematics of *Design C* (balun, RF choke, $L_2C_2$ and $C_L$)

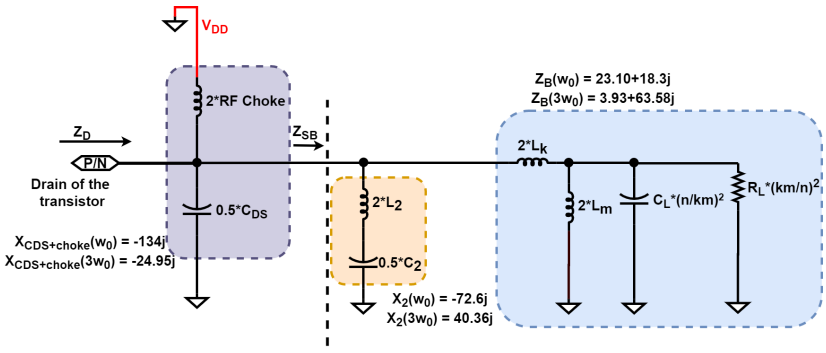



**Figure 3.11:** Differential mode equivalent circuit of *Design C* (balun, RF choke, $L_2C_2$ and $C_L$)

The following constraints have to fulfilled to obtain $R_D$ = *38.7* Ω and $X_D$ = *0* Ω at $\omega_0$ (*2.4 GHz*).

$$R_{SB}(\omega_0) = 35.72\ \Omega \tag{3.15}$$

$$X_{SB}(\omega_0) = 10.3\ \Omega \tag{3.16}$$

In order to achieve high impedance at the drain of the transistor at $3\omega_0$ (*7.2 GHz*), $C_{DS}$ needs to resonate out with the reactive part of $Z_{SB}$ and RF choke.

$$X_{SB}(3\omega_0) = 24.96\ \Omega \tag{3.17}$$

The value of $R_{SB}(3\omega_0)$ is chosen to achieve *1000* Ω at $3^{rd}$ harmonic.

$$R_{SB}(3\omega_0) = 0.6\ \Omega \tag{3.18}$$

There are *5* unknowns in the circuit: $km$, $N$, $L_P$, $C_2$, $C_L$. Using four Equation 3.15, 3.16, 3.17 and 3.18 and assuming $km$ = *0.8*, the remaining unknowns can be solved.

$$N = 1.14$$

$$L_P = 2.23\ nH$$

$$C_L = 1.10\ pF$$

$$C_2 = 1.37\ pF$$

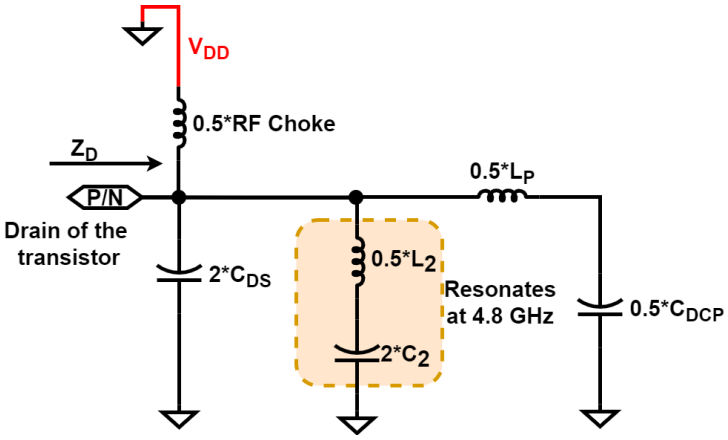



**Figure 3.12:** Common mode equivalent circuit of *Design C* (balun, RF choke, $L_2C_2$ and $C_L$)

From Figure 3.12, it is evident that to get short at $2\omega_0$ (*4.8 GHz*), $L_2C_2$ should have a series resonance at $2\omega_0$.

$$L_2 = \frac{1}{4 * \omega_0^2 * C_2} = 0.8\ nH \tag{3.19}$$

## 3.6. Design D (Balun, RF choke and output capacitance)

Compared to the previous design, $L_2C_2$ is removed in this design and RF choke is not fixed to *5 nH*.

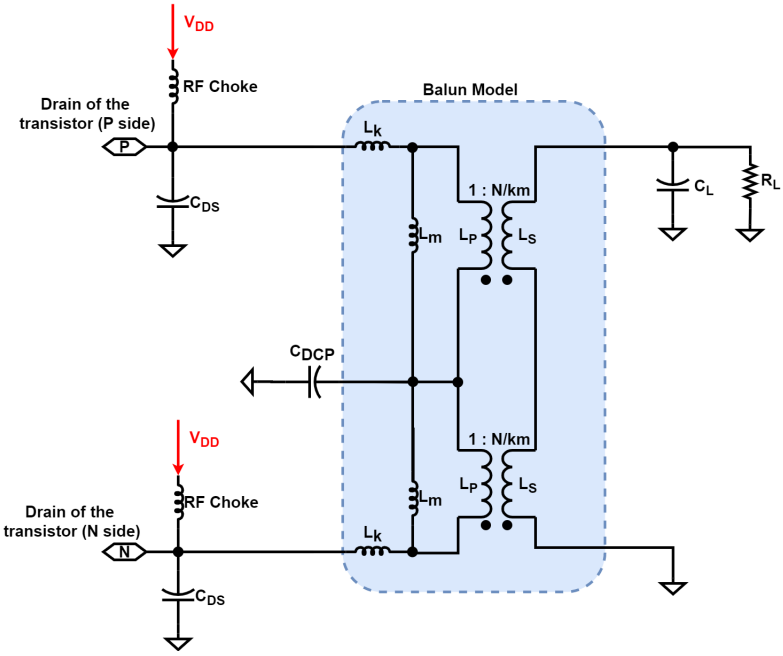



**Figure 3.13:** Schematics of *Design D* (balun, RF choke and $C_L$)

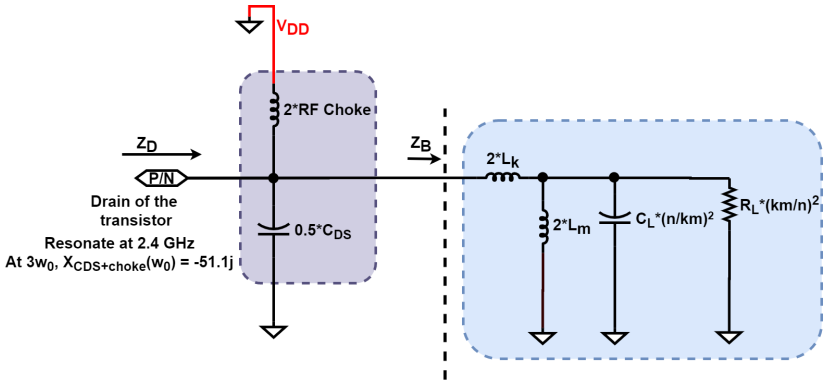



**Figure 3.14:** Differential mode equivalent circuit of *Design D* (balun, RF choke and $C_L$

Since RF choke is not fixed, it can be calculated if $C_{DS}$ resonates with it at $1^{st}$ harmonic.

$$\text{RF choke} = \frac{1}{\omega_0^2 C_{DS}} = 2.35\ nH \tag{3.20}$$

To achieve the required $P_{OUT}$, impedance of *38.7* Ω is needed at the drain of the transistor.

$$R_B(\omega_0) = 38.7\ \Omega \tag{3.21}$$

$$X_B(\omega_0) = 0\ \Omega \tag{3.22}$$

In order to obtain high impedance at the drain of the transistor at $3\omega_0$ (*7.2 GHz*), $C_{DS}$ needs to resonate out with the reactive part of $Z_B$ and RF choke.

$$X_B(3\omega_0) = 26.61\ \Omega \tag{3.23}$$

The value of $R_B(3\omega_0)$ is chosen to achieve *1000* Ω at $3^{rd}$ harmonic.

$$R_B(3\omega_0) = 0.6\ \Omega \tag{3.24}$$

There are *4* unknowns in the circuit: $km$, $N$, $L_P$ and $C_L$. Using four Equation 3.21, 3.22, 3.23 and 3.24, the four unknowns can be solved.

$$N = 0.84$$

$$L_P = 0.86\ nH$$

$$C_L = 3.95\ pF$$

$$km = 0.77\ pF$$

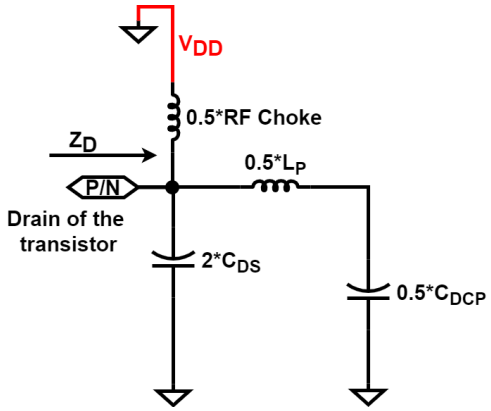


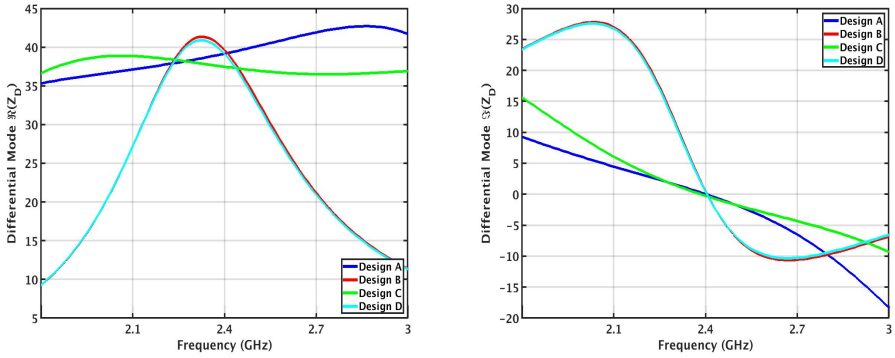

**Figure 3.15:** Common mode equivalent circuit of *Design D* (balun, RF choke and $C_L$)

From Figure 3.15, $C_{DCP}$ can be tuned to provide a short at $2\omega_0$ (*4.8 GHz*) similar to *Design B*.

$$C_{DCP} = 2.56\ pF \tag{3.25}$$

# 3.7. Comparison of output networks

## 3.7.1. Impedance at first harmonic ($\omega_0$)




**(a)** Real part of $Z_D$ ($\Re(Z_D)$) **(b)** Reactive part of $Z_D$ ($\Im(Z_D)$)

**Figure 3.16:** Impedance ($Z_D$) at $1^{st}$ harmonic ($\omega_0$)

From Figure 3.16a, it is seen that the real part at $1^{st}$ harmonic is flatter in the bandwidth *2.1 - 2.7 GHz* for *Design A* and *C* unlike *Design B* and *D*. This, in turn, leads to constant $P_{OUT}$ in the specified bandwidth. The reason for the constant real part of *Design A* and *C* is due to the presence of $L_2C_2$. $L_2C_2$ is a series resonance at $2^{nd}$ harmonic, thus it acts as a varying capacitor at $1^{st}$ harmonic (Figure 3.17).

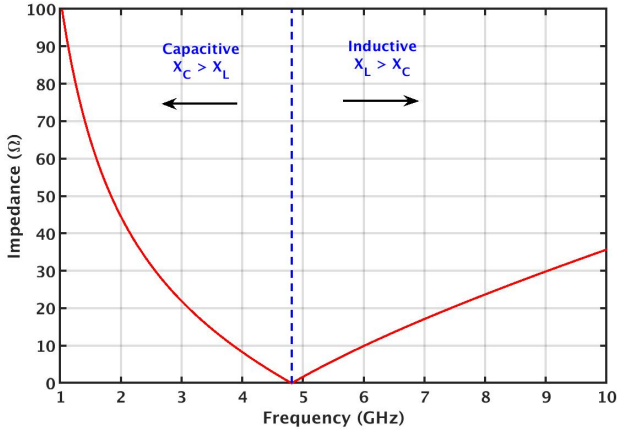
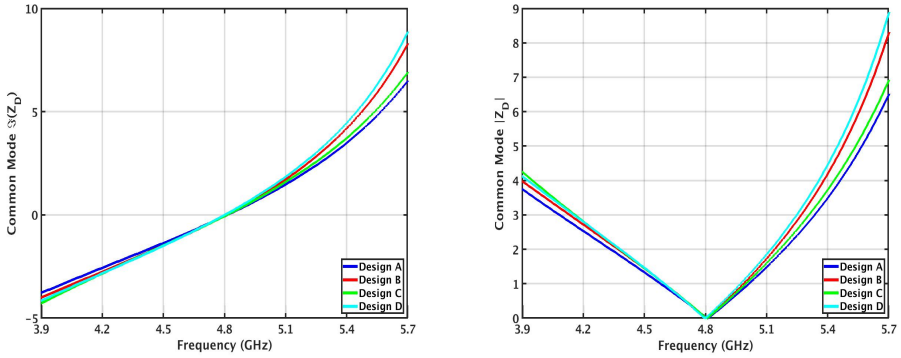



**Figure 3.17:** Series Resonance ($L_2C_2$)

*Design B* and *D* have a high reactive part at $1^{st}$ harmonic as compared to *Design A* and *C* (Figure 3.16b) which is due to the presence of the $L_2C_2$ in *Design A* and

*C*. Since reactive part at $1^{st}$ harmonic for *Design B* and *D* have higher slope, the corresponding $\gamma$ value will also be high, (refer Equation 2.9) which directly relates to higher maximum drain voltage (refer Figure 2.1).

### 3.7.2. Impedance at second harmonic ($2\omega_0$)




**(a)** Reactive part of $Z_D$ ($\Im(Z_D)$) **(b)** Magnitude of $Z_D$

**Figure 3.18:** Impedance ($Z_D$) at $2^{nd}$ harmonic ($2\omega_0$)

From Figure 3.18a and 3.18b, it is seen that all 4 design have similar response at $2^{nd}$ harmonic.

### 3.7.3. Impedance at third harmonic ($3\omega_0$)

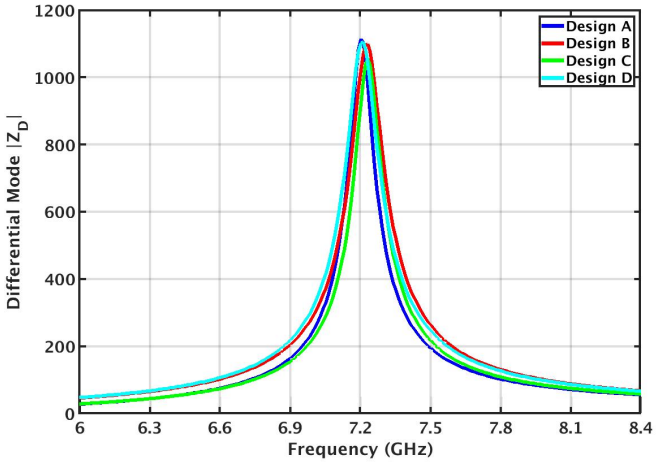
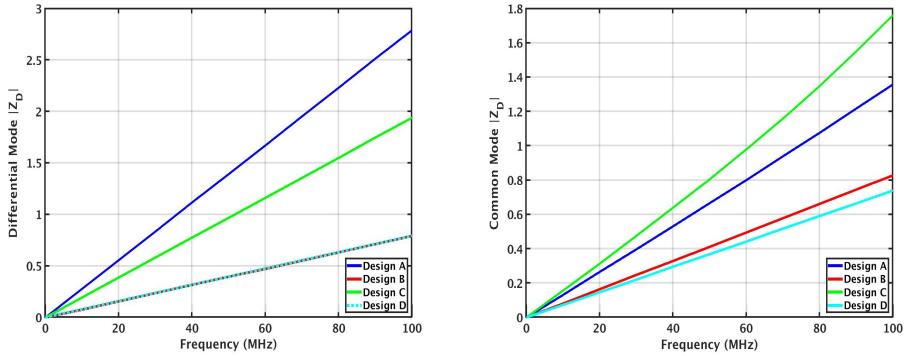



**Figure 3.19:** Magnitude of $Z_D$ at $3^{rd}$ harmonic ($3\omega_0$)

As designed, four output networks have an impedance of *1000* Ω at $3^{rd}$ harmonic. It is also seen that impedance at *2.1 GHz* and *2.7 GHz* is less than *200* Ω for all four designs.

### 3.7.4. Impedance at low frequency (0-100 MHz)




**(a)** Differential mode impedance **(b)** Common mode impedance

**Figure 3.20:** Impedance at low frequency

Figure 3.20a and 3.20b shows that differential and common mode impedance isn't large (less than *4* Ω) between *0 - 100 MHz*. In case, the impedance was large, it can reduce third order intercept point ($IP_3$) due to indirect mixing [3] [4] [5].

| **Designs** | RF choke / $L_{BND}$ (*nH*) | $L_P$ (*nH*) | $N$ | $km$ | $L_S$ (*nH*) | $C_L$ (*pF*) | $L_2$ (*nH*) | $C_2$ (*pF*) | $C_{DCP}$ (*pF*) |
|---|---|---|---|---|---|---|---|---|---|
| **A** (no RF choke & with $L_2C_2$) | 1 | 2.22 | 1.32 | 0.8 | 3.87 | 0.93 | 0.74 | 1.48 | 100 |
| **B** (no RF choke & no $L_2C_2$) | 1 | 0.63 | 0.9 | 0.72 | 0.51 | 3.96 | - | - | 4.58 |
| **C** (with RF choke & with $L_2C_2$) | 5 | 2.23 | 1.14 | 0.8 | 2.9 | 1.1 | 0.8 | 1.37 | 100 |
| **D** (with RF choke & no $L_2C_2$) | 2.35 | 0.86 | 0.84 | 0.77 | 0.61 | 3.95 | - | - | 2.56 |

**Table 3.2:** The value of components in all *4* output network designs

## 3.8. Conclusion

This chapter explained the procedure to design the four output networks using lossless capacitors and inductors, namely *Design A* (no RF Choke and with $L_2C_2$), *Design B* (no RF Choke and no $L_2C_2$), *Design C* (with RF Choke and with $L_2C_2$) and *Design D* (with RF Choke and no $L_2C_2$). The balun and $C_L$ is common for all the designs. Except at $1^{st}$ harmonic, the response of all four output networks is very much identical. In terms of the number of components, *Design B* has the least (only balun and $C_L$). But *Design A* and *C* outperform others at $1^{st}$ harmonic by having a flatter real part as well as a smaller reactive part in the bandwidth *2.1 - 2.7 GHz*.

The final decision of selecting the output network will be carried out after designing the output stage which is explained in the subsequent chapter and measuring few parameters like $\eta_D$, peak $P_{\text{OUT}}$, $OP1dB$, and $IM3$.

## References

[1] A. Grebennikov and N. Sokal, *Switchmode RF Power Amplifiers. 1st ed.* (Elsevier Inc., 2007).

[2] J. R. Long, *Monolithic transformers for silicon rf ic design,* IEEE Journal of Solid-State Circuits **35**, 1368 (2000).

[3] J. Brinkhoff, A. E. Parker, and M. Leung, *Baseband impedance and linearization of fet circuits,* IEEE Transactions on Microwave Theory and Techniques **51**, 2523 (2003).

[4] J. Brinkhoff and A. E. Parker, *Implication of baseband impedance and bias for fet amplifier linearization,* in *IEEE MTT-S International Microwave Symposium Digest, 2003*, Vol. 2 (2003) pp. 781–784 vol.2.

[5] J. Brinkhoff and A. E. Parker, *Effect of baseband impedance on fet intermodulation,* IEEE Transactions on Microwave Theory and Techniques **51**, 1045 (2003).

# 4

# Design of output stage

In this chapter, the design of the output stage is elucidated. Since CCF has a higher peak factor (around *3.12* for $\gamma$ = *+/-1*) than other classes of PA, breakdown voltage of the transistor becomes the main bottleneck. One way to mitigate this is to select voltage supply ($V_{DD}$) equal to half of the breakdown voltage of the transistor in Class A and B. But, the lower headroom limits the linear voltage range of the transistor. Also, the drain efficiency ($\eta_D$) reduces since output current ($I_D$) increases proportionally leading to a greater loss in the output matching network [1]. Added to this, the device is also larger to handle the larger current. Thereby increasing more losses in the device.

Maximum $V_{DD}$ of the thick oxide and the nominal device is *1.98 V* and *1.05 V* respectively in TSMC *22 nm* ULL technology. Using the rule of thumb that breakdown voltage is $\sqrt{2}V_{DD}$, then the breakdown voltage of the thick oxide and the nominal device is *2.8 V* and *1.5 V* respectively. **Cascode** [1], **Self biasing cascode** [2] and **Stacked** [3] [4] are few techniques in the literature to counter breakdown voltage issue. The first two techniques use two transistors on top of each other, bottom one being nominal device and upper one being thick oxide. Since the type of PA is CCF and targeted peak output power ($P_{\text{OUT}}$) is *27 dBm* (ideal case), these techniques fail to bring the voltage swing below the breakdown voltage requirement. Thus, the concept of stacked transistor is a promising candidate to solve breakdown voltage which is discussed briefly in the below section.

## 4.1. Stacked transistor

The capacitors $C_2$ and $C_3$ in Figure 4.1 allows drain and source to sustain large voltage swings in a way that each transistor has the same drain source voltage ($V_{DS}$), gate source voltage ($V_{GS}$) and drain gate voltage ($V_{DG}$) swings unlike the scenario of cascoded transistors. This way, the $V_{DS}$, $V_{GS}$, and $V_{DG}$ swings can be designed to be within breakdown voltage limits. The output voltage swings of all three transistors are added in phase so that the total voltage swing at the top

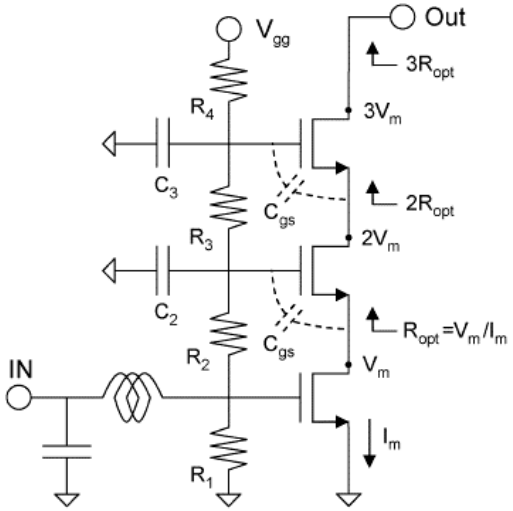



**Figure 4.1:** Schematic of triple-stacked field-effect transistor (FET) PA [3]

transistor's drain is three times higher than the maximum available $V_{DS}$ swing for a single transistor with a constant current swing. It is made sure that each transistor delivers the same power. The optimum load impedance increases linearly with the number of transistors ($n$) in series. Thus, the stacked design has $n$ times lower input capacitance. So, a larger device can be used with tolerable input capacitance to minimize the knee voltage effect on the $P_{\text{OUT}}$ and $\eta_D$. By doing so, the stacked transistor can overcome two major limitations of metal-oxide semiconductor field-effect transistor (MOSFET), namely, low breakdown voltage, and high knee voltage [3].

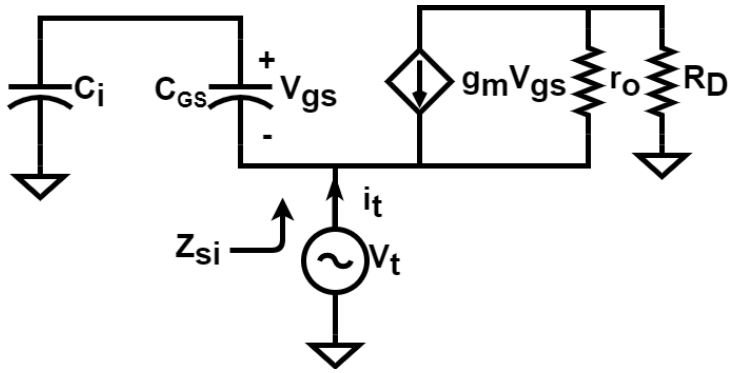



**Figure 4.2:** Small signal model of stacked transistors (common gate transistors)

Figure 4.2 shows small signal model of stacked transistors (Figure 4.1).

$$Z_{si} \approx (1 + \frac{C_{GS}}{C_i})(\frac{1}{g_m} || \frac{1}{sC_{GS}})$$

$$\omega_T = \frac{g_m}{C_{GS}}, s = j\omega_c$$

$$Z_{si} = \frac{1}{g_m}(1 + \frac{C_{GS}}{C_i}), f_o << f_t \tag{4.1}$$

$$A_v = \frac{g_{m1}R_D}{\left(1 + \frac{sC_{GS2}}{g_{m2}}\right)\left(1 + \frac{sC_{GS3}}{g_{m3}}\right)\left(1 + \frac{sC_{GS4}}{g_{m4}}\right)} \approx g_{m1}R_D, f_o < f_t \tag{4.2}$$

Equation 4.1 shows that if $C_i \gg C_{GS}$, then it becomes a cascoded transistor. To operate transistor as a stacked transistor, $C_{GS}$ has to be comparable to $C_i$ (preferably *0.5* to *2* times).

| Parameter | Single FET | n-Parallel FET | n-Stacked FET |
|---|---|---|---|
| Peak drain current | $I_m$ | $n.I_m$ | $I_m$ |
| Peak drain voltage | $V_m$ | $V_m$ | $n.V_m$ |
| Input capacitance | $C_g$ | $n.C_g$ | $C_g$ |
| Output impedance | $R_{opt}$ | $\frac{R_{opt}}{n}$ | $n.R_{opt}$ |
| Output power | $\frac{1}{8}.V_m.I_m$ | $\frac{1}{8}V_m.n.I_m$ | $\frac{1}{8}.n.V_m.I_m$ |
| Voltage gain | $g_m.R_{opt}$ | $n.g_m.\frac{R_{opt}}{n}$ | $g_m.n.R_{opt}$ |

**Table 4.1:** Comparison of parallel and stacked-transistor configurations [4]

From Table 4.1, it is seen that the $n$ stacked FET PA has $n$ times higher voltage gain and power gain. The input and output impedance are $n$ times and $n^2$ times higher than $n$ parallel transistor PA respectively. This leads to improved input and output matching in the specified bandwidth as well as less power loss in the output matching network [4].

One main disadvantage of the stacked transistor is that $C_{GS}$ is non-linear in nature and impedance of stacked transistor depends on $C_{GS}$, thus leading to a reduction in linearity. In CMOS, body effect and source bulk capacitance ($C_{SB}$) progressively reduce the gain of the transistors in the upper sections of the stack. Also, the breakdown voltage of the drain–bulk junction diode limits the maximum allowable voltage swing in the stacked transistor. To overcome this, a triple-well CMOS process can be used if it is available in the technology.

The stacked transistor also leads to lower $\eta_D$ compared to cascode. The reason behind this is that each transistor has $C_{GD}$ and this capacitance leads to a shift in current compared to voltage (refer Figure 4.4). This leads to a larger overlap between current and voltage thereby reducing $\eta_D$. The overlap is directly proportional to the number of transistors in the stack. So it is better to have the least number of transistors to satisfy the breakdown voltage criteria. The design of having *3* transistors (*2* nominal devices and *1* thick oxide device) is chosen as shown in Figure 4.3. The reason for not choosing *1* nominal and *2* thick oxide devices is that thick oxide has larger capacitance than nominal device, thereby leading to a larger shift in current and larger overlap in current and voltage. Subsequently, reducing $\eta_D$.

Instead of the nominal device, ultra-low or low threshold devices can be used since it has higher transconductance. But linearity is inferior for those devices, thus the nominal device was used.

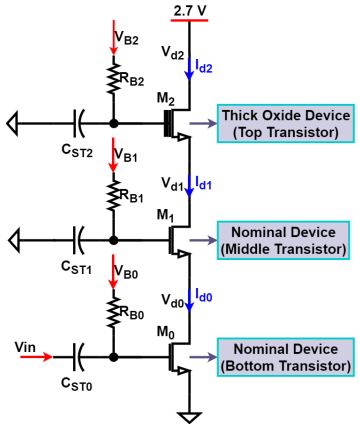



**Figure 4.3:** Schematics of stacked transistor

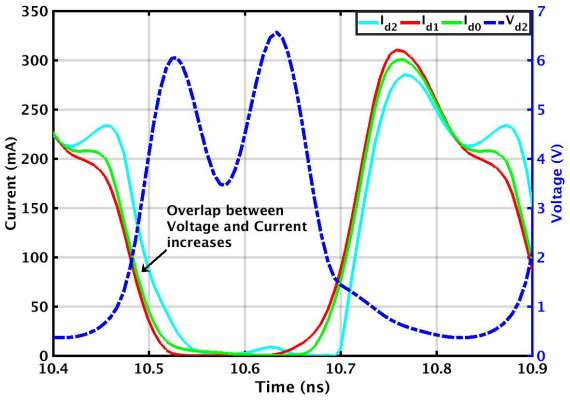



**Figure 4.4:** Plot showing current and voltage overlap

## 4.2. Output stage design

In this section, aspect ratios ($W/L$) and the biasing voltages ($OS\_V_{B2}$, $OS\_V_{B1}$ and $OS\_V_{B0}$) for the transistors in the output stage are discussed extensively.
Differential impedance ($R_D(DE)$) between the drains of the output stage was calculated in Equation 3.2 to be

$$R_D(DE) = 38.7\ \Omega$$

Single ended ($SE$) impedance to be seen at the drain of the differential pair to get required $P_{\text{OUT}}$ of *27 dBm* is

$$R_D(SE) = \frac{R_D(DE)}{2} = 19.39\ \Omega \tag{4.3}$$

Single ended current swing in the fundamental band

$$I_{FUND}(SE) = \frac{V_{FUND}(SE)}{R_D(SE)} = 160.76\ mA \tag{4.4}$$

Maximum current in the fundamental band

$$I_{FUND\_MAX}(SE) = I_{FUND}(SE) = 160.76\ mA \tag{4.5}$$

DC current ($I_{DC}$) is calculated by [5]

$$I_{DC}(SE) = \frac{2}{\pi} I_{FUND\_MAX}(SE) = 102.34\ mA \tag{4.6}$$

DC power ($P_{DC}$) dissipated is given by

$$P_{DC} = 2 * V_{DD} * I_{DC}(SE) = 552.64\ mW \tag{4.7}$$

Drain efficiency ($\eta_D$) is given by

$$\eta_D = \frac{P_{\text{OUT}}}{P_{DC}} = 90.7\ \% \tag{4.8}$$

### 4.2.1. Design of top and bottom transistors

This subsection describes the procedure to design the top transistors ($M_2$ & $M_5$) and the bottom transistors ($M_0$ & $M_3$) shown in Figure 4.5.

$W/L$ and biasing voltages for the top and bottom transistors are calculated by plotting the load-line. Figure 4.6 shows $I_D$ vs $V_{DS}$ of bottom transistor on left hand side (nominal device) and $I_D$ vs $V_{DS}$ of top transistor on right hand side (thick oxide device). Table 4.2 shows the aspect ratio of the top and bottom transistors. Load-line is drawn using $V_{FUND}(SE)$ and $I_{FUND}(SE)$ which is calculated in Equation 3.1 and 4.4. DC line is plotted using $I_{DC}(SE)$ calculated from Equation 4.6. From this, the aspect ratio as well as the biasing voltage of the top and bottom transistors are calculated. Deep N well is used in the top transistor (thick oxide) to counter drain-bulk breakdown. Deep N well is connected to $V_{DD}$ via *2 KΩ* since it helps in increasing efficiency (refer Figure C.1). Moreover, N well capacitance is in series with channel capacitance, thereby reducing the total parasitic capacitance [6].

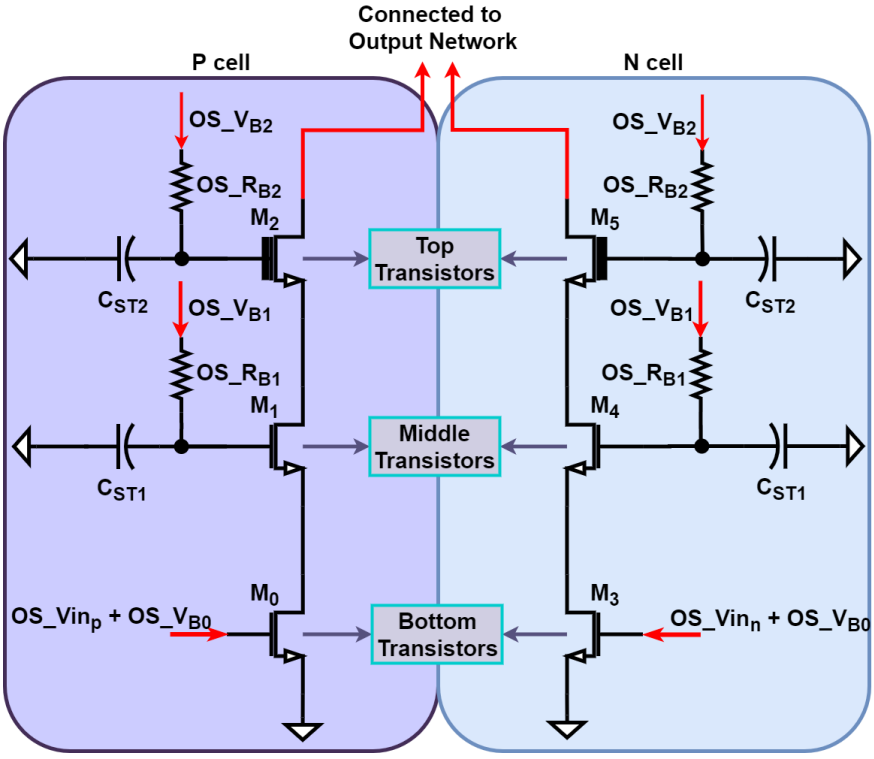



**Figure 4.5:** Schematics of the output stage

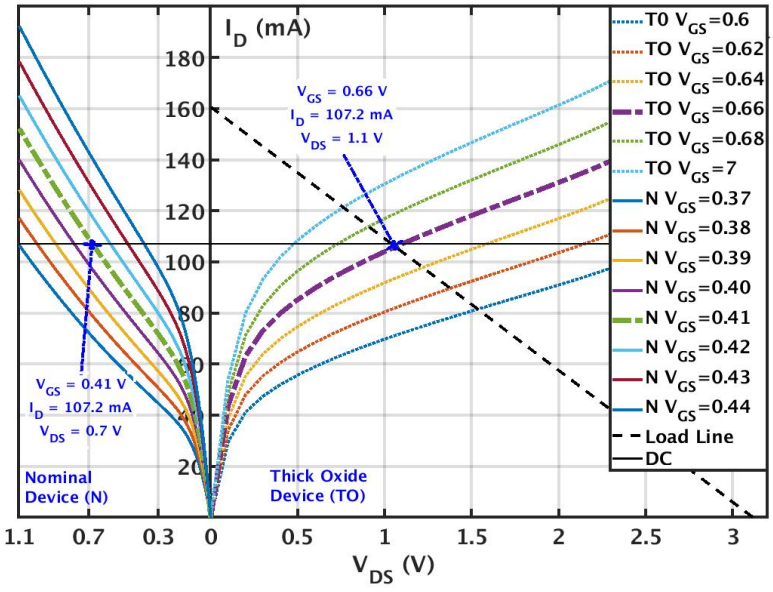



**Figure 4.6:** Load-line for the output stage

| Transistors | Top transistor ($M_2$ & $M_5$) Thick oxide | Bottom transistor ($M_0$ & $M_3$) Nominal |
|---|---|---|
| **Finger width ($W$)** | 1 um | 1 um |
| **Fingers ($F$)** | 32 | 32 |
| **Multiplier ($M$)** | 80 | 50 |
| **Total Width ($W_T$)** | 2.56 mm | 1.6 mm |

**Table 4.2:** Aspect ratio ($W/L$) of the top and bottom transistors in the output stage



### 4.2.2. Design of middle transistor

Since biasing voltages of top and bottom transistors are known, $V_{DS}$ of middle transistor ($M_1$ & $M_4$) can be calculated. For each multiplier, corresponding $V_{GS}$ can be be found from Figure 4.8. The simulation was carried out to see effect of middle transistor's aspect ratio and biasing voltage on $\eta_D$ and peak $P_{OUT}$ which is shown in Table 4.3.

The multiplier for the middle transistor is chosen as *50* even though *40* has slightly better performance. The reason behind this is that the multiplier of the bottom transistor is *50* and having multiplier of middle transistor similar to this helps in the layout. Note that $C_{ST1}$ and $C_{ST2}$ are kept large (*100 pF*) so that it acts as cascode so as to get maximum $\eta_D$.

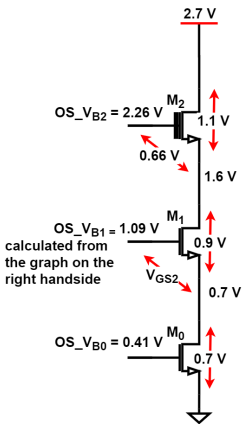



**Figure 4.7:** $V_{DS}$ calculation for $M_1$

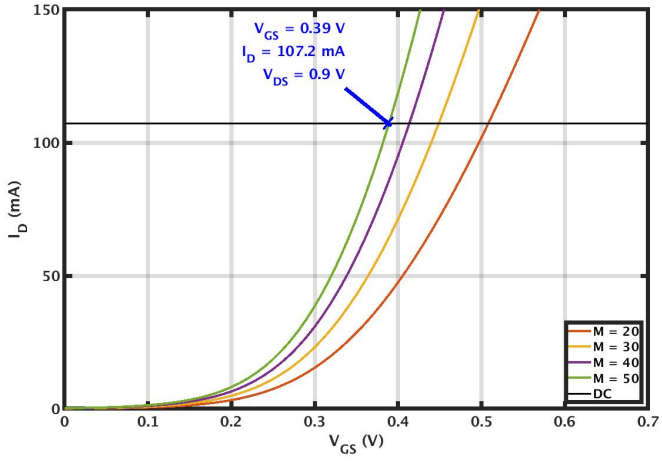



**Figure 4.8:** $I_D$ vs $V_{GS}$ at $V_{DS} = 0.9\ V$ for $M_1$ for different values of multiplier

| Multiplier (M) | $V_{GS}$ (V) | $\eta_D$ (%) | $P_{OUT}$ (dBm) |
|---|---|---|---|
| 50 | 0.39 | 77.7 | 27.5 |
| 40 | 0.41 | 78 | 27.4 |
| 30 | 0.45 | 77.9 | 27.3 |
| 20 | 0.51 | 76.9 | 27.2 |

**Table 4.3:** Drain efficiency ($\eta_D$) and peak $P_{OUT}$ for different values of multiplier



### 4.2.3. Design of $C_{ST1}$ and $C_{ST2}$

As discussed in section 4.1, to obtain stacked operation, $C_{ST}$ should be *0.5 - 2* times of $C_{GS}$. $C_{GS}$ of the middle transistors ($M_1$ & $M_4$) and the top transistors ($M_2$ & $M_5$) are *0.47 pF* and *1.56 pF*, respectively.

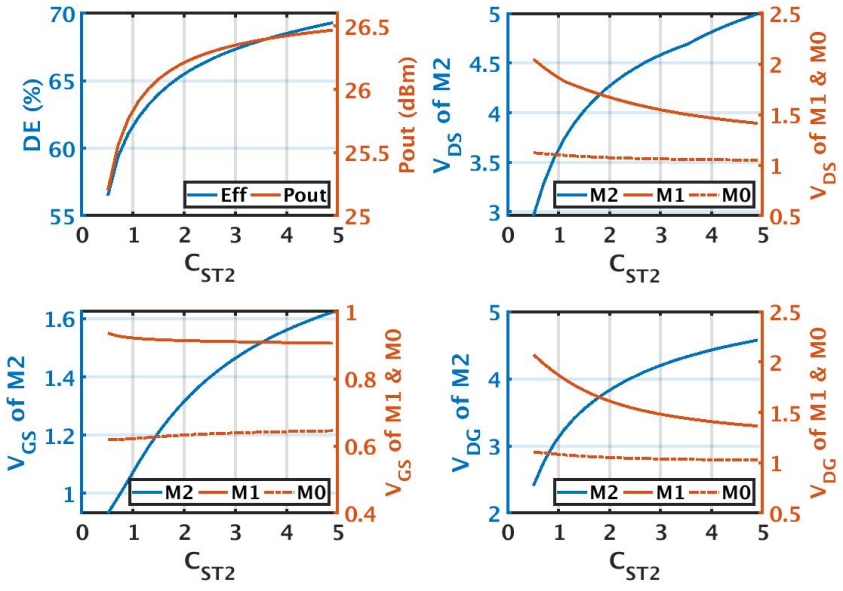



**Figure 4.9:** Drain efficiency ($\eta_D$), $P_{OUT}$, $V_{DS}$, $V_{GS}$,$V_{GD}$ versus $C_{ST2}$

Input power level is kept *1 dB* higher than the input compression point for this analysis ($P_{in}$ = *5 dBm*). X axis in the Figure 4.9 denotes the factor that needs to be multiplied with $C_{GS2}$ to obtain the value of $C_{ST2}$ in *pF*. From Figure 4.9, it is seen that $\eta_D$ and $P_{OUT}$ increases as $C_{ST2}$ increases. This confirms the result that cascode has higher $\eta_D$ than stacked. Also, it is seen that $V_{DS}$, $V_{GS}$ and $V_{GD}$ is lower in stacked

operation (when value of $C_{ST2}$ is lower). This means there is a trade off between efficiency and nodal voltages while choosing the value of $C_{ST2}$. Note that during this optimization, value of $C_{ST1}$ is kept as *100 pF*.

$$C_{ST2} = 1.5 * C_{GS2} \approx 2.4\ pF$$

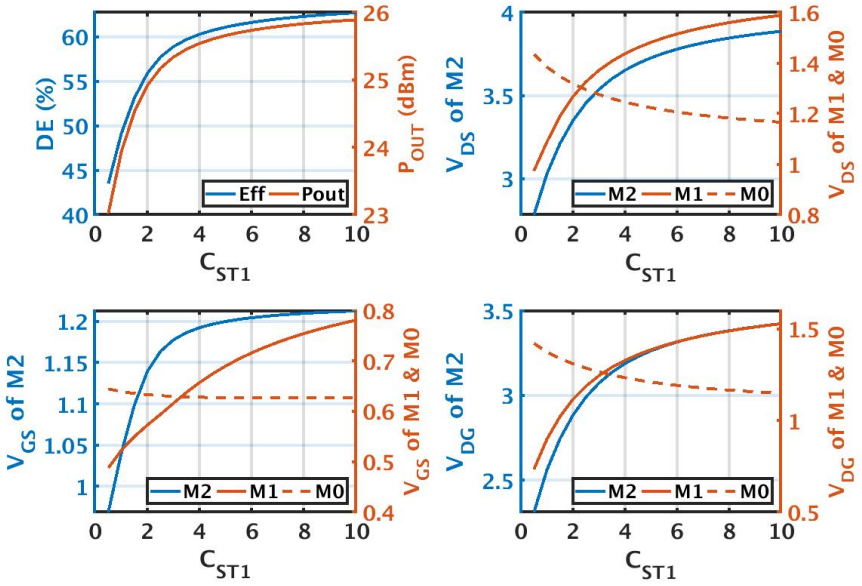



**Figure 4.10:** Drain efficiency ($\eta_D$), $P_{\text{OUT}}$, $V_{DS}$, $V_{GS}$,$V_{GD}$ versus $C_{ST1}$

In this analysis also, input power level is kept *1 dB* higher than the input compression point ($P_{in}$ = *5 dBm*). The X axis in Figure 4.10 denotes the factor that needs to be multiplied with $C_{GS1}$ to obtain the value of $C_{ST1}$ in *pF*. From Figure 4.10, it is seen that $\eta_D$ and $P_{\text{OUT}}$ increases as $C_{ST1}$ increases similar to the previous case. It is seen that nodal voltages ($V_{DS}$, $V_{GS}$ and $V_{GD}$) doesn't have a larger dependence on $C_{ST1}$. This means there is no added advantage in having $C_{ST1}$ in stacked operation for nodal voltage. This is the reason $C_{ST1}$ is chosen to operate in cascode. Note that during this optimization, value of $C_{ST2}$ is kept as *2.4 pF*.

$$C_{ST1} = 10 * C_{GS1} \approx 5\ pF$$

The biasing point $OS\_V_{B0}$ of the bottom transistor ($M_0$ & $M_3$) can be reduced to get higher $\eta_D$ as the PA moves closer to a switching PA. But, this degrades the linearity. In this case, $OS\_V_{B0}$ was optimized to *0.32 V* such that $\eta_D$ is higher without trading the linearity much.

## 4.3. Comparison of output networks with output stage

In this section, four output network designs are tested with output stage and input transformer. Input transformer converts single-ended input signal to differential signal and provides input matching over the bandwidth of *2.1 - 2.7 GHz*. The biasing voltage for the bottom transistor is fed through the center tap of the input transformer. Input transformer is designed using the concept of double tuned transformer [7] [8]. Error vector magnitude (EVM) is calculated for all four designs using the script[1] provided by *CATENA MICROELECTRONICS B.V.*

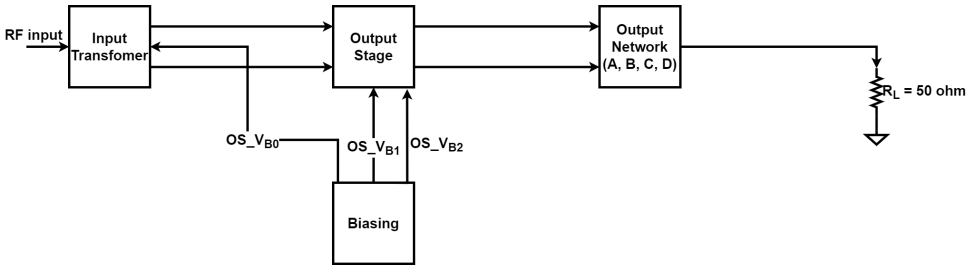



**Figure 4.11:** Block diagram showing the input transformer, output stage and output network

From Table 4.4 shown in the next page, it is seen that there is comparatively a large variation in peak $P_{OUT}$ and output 1dB compression point ($OP1dB$) across bandwidth (*2.1 - 2.7 GHz*) in the case of *Design B* and *D* unlike the Design *A* and *C*. This is due to large variation in the real part of $1^{st}$ harmonic for Design *B* and *D* (refer Figure 3.16a). *Design A* was chosen even though *Design C* performs slightly better. The reason is that RF choke in *Design C* is outside the chip and thus making it vulnerable to the outside factors. It is always easier to replicate the results if the entire design is inside the chip and there is no outside components. This applies when the PA is integrated into the WiFi chip as well.

## 4.4. Influence of $3^{rd}$ harmonic impedance on drain efficiency and output 1 dB compression point

Figure 4.12 shows the influence of $3^{rd}$ harmonic impedance on maximum $\eta_D$ and $OP1dB$ for the frequency *2.4 GHz* with *Design A*[2] output network and output stage. The $3^{rd}$ harmonic impedance in *Design A* can be adjusted by varying $R_{SB}$ which was discussed in the section 3.3 (Figure 3.5b). It is observed that as the $3^{rd}$ harmonic impedance increases, there is negligible effect on maximum $\eta_D$ and $OP1dB$.

[1] Script uses AM (amplitude modulation) - AM and AM - PM (phase modulation) to calculate EVM. Since the script is propriety of CATENA MICROELECTRONICS B.V., it is confidential.

[2] no RF choke and with $L_2C_2$

| Parameters | | Design A (no RF choke & with $L_2C_2$) | | | Design B (no RF choke & no $L_2C_2$) | | | Design C (with RF choke & with $L_2C_2$) | | | Design D (with RF choke & no $L_2C_2$) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Class of Operation | | Class F | CCF | | Class F | CCF | | Class F | CCF | | Class F | CCF | |
| Frequency (*GHz*) | | 2.4 | 2.1 | 2.7 | 2.4 | 2.1 | 2.7 | 2.4 | 2.1 | 2.7 | 2.4 | 2.1 | 2.7 |
| Peak Pout (*dBm*) | | 26.9 | 26.5 | 26.5 | 26.9 | 25.8 | 28 | 27 | 26.4 | 27 | 26.9 | 25.9 | 28 |
| OP1dB (*dBm*) | | 25.6 | 25.5 | 25.4 | 25.6 | 25.2 | 27.6 | 25.7 | 25.4 | 26.1 | 25.7 | 25.3 | 27.7 |
| $\eta_D$ (%) | Maximum | 70.3 | 60.8 | 69.6 | 70.6 | 52.7 | 66.9 | 70 | 61 | 71 | 70.9 | 53.2 | 66.8 |
| | @ P1dB | 61.8 | 59.6 | 64.7 | 62.3 | 51.9 | 65.2 | 61.9 | 59.8 | 66.7 | 62.8 | 52.4 | 65.3 |
| | @ Pout = 18 dBm | 21.6 | 21.3 | 22.1 | 21.6 | 19.3 | 19.3 | 21.4 | 21.4 | 21.4 | 21.6 | 19.3 | 19.2 |
| | @ Pout = 16.5 dBm | 16.4 | 16.2 | 16.7 | 16.4 | 14.9 | 14.9 | 16.3 | 16.3 | 16.3 | 16.4 | 14.8 | 14.8 |
| EVM (*dB*) | @ Pout = 18 dBm | -31.1 | -30.2 | -29.3 | -30.9 | -22.2 | -33.8 | -31.9 | -29.1 | -32.4 | -31.2 | -22.5 | -33.6 |
| | @ Pout = 16.5 dBm | -35 | -34.8 | -34 | -34.7 | -25.7 | -34 | -35.7 | -33.9 | -36.2 | -35 | -26 | -33.8 |
| Voltage Gain (*dB*) | | 22.9 | 22.3 | 23.2 | 22.9 | 21 | 20.9 | 22.7 | 22.4 | 22.6 | 22.9 | 21 | 20.8 |
| IM3 (*dBc*) | @ Pin = -20 dBm | -64.5 | -64.8 | -64.4 | -64.6 | -61.5 | -62.9 | -64.5 | -64.8 | -64 | -64.6 | -61.6 | -62.8 |
| | @ Pin = 5 dBm | -13.2 | -13 | -12.6 | -13.1 | -12.9 | -16.5 | -13.4 | -12.8 | -13.2 | -13.2 | -12.9 | -16.7 |
| OIP3 (*dBm*) | | 34.7 | 34.6 | 35 | 34.8 | 31.2 | 31.7 | 34.5 | 34.8 | 34.2 | 34.7 | 31.3 | 31.6 |

**Table 4.4:** Comparison between four output network designs

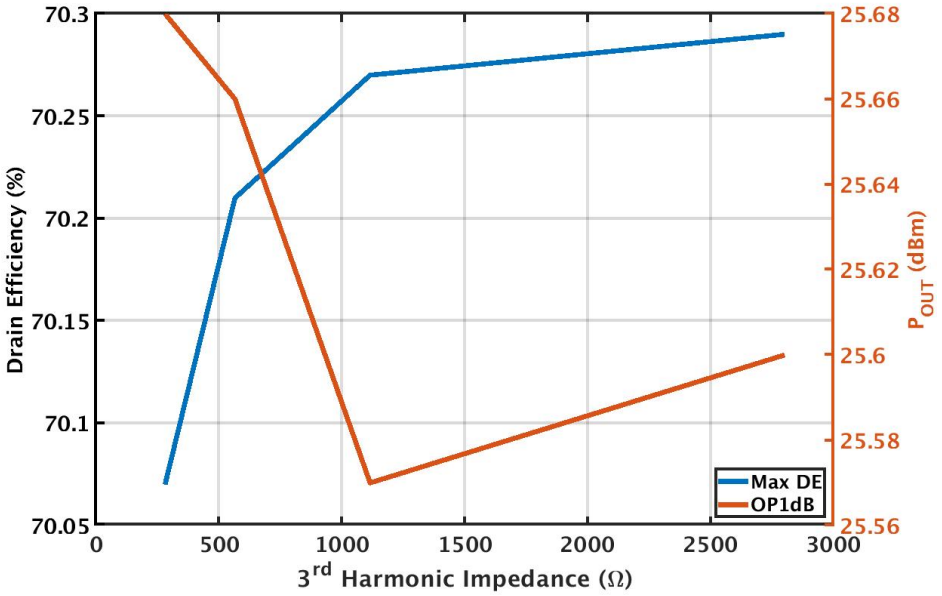



**Figure 4.12:** Drain efficiency ($\eta_D$) and output 1 dB compression point ($OP1dB$) versus $3^{rd}$ harmonic impedance at *2.4 GHz*

From Figure 3.5b, it is evident that the $3^{rd}$ harmonic impedance at *2.1 GHz* and *2.7 GHz* is around *52* $\Omega$ and *74* $\Omega$ respectively. At the same time, Table 4.4 clearly indicates that the maximum $\eta_D$ at *2.1 GHz* and *2.7 GHz* for *Design A* is *60.8%* and *69.6%*. This confirms that there is no need to have a open circuit or high impedance at $3^{rd}$ harmonic as it has very trivial effect on the parameters like $\eta_D$ and $OP1dB$.

## 4.5. Conclusion

This chapter explained the procedure to calculate the biasing voltages and $W/L$ for the stack of three transistors. Further, the four output network designs were compared and *Design A* (no RF choke and $L_2C_2$) was chosen. The chapter also showed that $3^{rd}$ harmonic impedance has insignificant effect on $\eta_D$ and $OP1dB$. The following chapter explains the procedure for the design of driver.

## References

[1] B. Razavi, *Rf microelectronics: pearson new international edition* (Pearson Education Limited, 2013).

[2] T. Sowlati and D. M. W. Leenaerts, *A 2.4-ghz 0.18-µm cmos self-biased cascode power amplifier,* IEEE Journal of Solid-State Circuits **38**, 1318 (2003).

[3] J. Jeong, S. Pornpromlikit, P. M. Asbeck, and D. Kelly, *A 20 dbm linear rf*

*power amplifier using stacked silicon-on-sapphire mosfets,* IEEE Microwave and Wireless Components Letters **16**, 684 (2006).

[4] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, *A watt-level stacked-fet linear power amplifier in silicon-on-insulator cmos,* IEEE Transactions on Microwave Theory and Techniques **58**, 57 (2010).

[5] A. Grebennikov and N. Sokal, *Switchmode RF Power Amplifiers. 1st ed.* (Elsevier Inc., 2007).

[6] H. Le, J. Crossley, S. R. Sanders, and E. Alon, *A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19w/mm2 at 73% efficiency,* in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers* (2013) pp. 372–373.

[7] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, *An ultra-wideband if millimeter-wave receiver with a 20 ghz channel bandwidth using gain-equalized transformers,* IEEE Journal of Solid-State Circuits **51**, 323 (2016).

[8] M. Vigilante and P. Reynaert, *On the design of wideband transformer-based fourth order matching networks for $E$ -band receivers in 28-nm cmos,* IEEE Journal of Solid-State Circuits **52**, 2071 (2017).

# 5

# Design of driver

This chapter explains the procedure to design the driver. The sole reason to add the driver is to increase the voltage gain ($G_V$). This should be done without decreasing the output 1dB compression point ($OP1dB$) and the output third order intercept ($OIP3$).

## 5.1. Driver specification

| | | | |
|---|---|---|---|
| **Output stage** | **IIP3** | 12 | dBm |
| | **Power gain ($G_P$)** | 22.4 | dB |
| | **OIP3** | 34.7 | dBm |
| | **OP1dB** | 25.6 | dBm |

**Table 5.1:** Specifications of the output stage obtained after simulation of the schematics

Table 5.1 shows specifications obtained from the simulation of both output stage and *Design A*[1] output network at *2.4 GHz*.
Assume that the total $OIP3$ should be around *33 dBm* and total power gain ($G_P$) will be around *35 dB*.

$$\Longrightarrow G_{P\_\text{Driver}} = 35 - 22.7 \approx 13\ dB$$

[1] no RF choke with $L_2C_2$

Using the below equation, $IIP3_{\text{Driver}}$ can be calculated.

$$\frac{1}{IIP3_{\text{Total}}} = \frac{1}{IIP3_{\text{Driver}}} + \frac{G_{P\_\text{Driver}}}{IIP3_{\text{OutputStage}}} \tag{5.1}$$

$$\Longrightarrow IIP3_{\text{Driver}} = 5\ dBm$$

$$OIP3_{\text{Driver}} = IIP3_{\text{Driver}} + G_{P\_\text{Driver}} = 18\ dBm \tag{5.2}$$

Theoretically, $OIP3$ is *10 dB* higher than $OP1dB$.

$$OP1dB_{\text{Driver}} = OIP3_{\text{Driver}} - 10 = 8\ dBm \tag{5.3}$$

$$IP1dB_{\text{Driver}} = OP1dB_{\text{Driver}} - G_{P\_\text{Driver}} + 1 = -4\ dBm \tag{5.4}$$

The important specifications $OIP3$ and $OP1dB$ of the driver are calculated above.

## 5.2. Driver design

The driver needs to have decent linearity and voltage gain. Moreover, efficiency of PA is decided primarily by the output stage. So, it is wise to start with Class A driver. Then, later shift the biasing point to get the operation of Class AB such that linearity of the complete PA isn't degraded much.
Peak output power can be assumed as

Differential-ended peak $P_{\text{OUT}} = 9\ dBm$

Single-ended peak $P_{\text{OUT}} = 6\ dBm$

Single-ended peak $P_{\text{OUT}} = 3.98\ mW$

Supply voltage

$$V_{DD} = 2.7\ V$$

Single ended ($SE$) voltage swing

$$V_{FUND}(SE) = V_{DD} = 2.7\ V \tag{5.5}$$

Single ended impedance to be seen at the drains of the driver

$$R_D(SE) = \frac{V_{FUND}^2(SE)}{2P_{\text{OUT}}} = 915.58\ \Omega \tag{5.6}$$

Single ended current swing at the fundamental band

$$I_{FUND}(SE) = \frac{V_{FUND}(SE)}{R_D(SE)} = 2.95\ mA \tag{5.7}$$

Maximum current at the fundamental band

$$I_{FUND\_MAX}(SE) = 2 * I_{FUND}(SE) = 5.90\ mA \tag{5.8}$$

DC current is calculated by [1]

$$I_{DC}(SE) = \frac{I_{FUND\_MAX}(SE)}{2} = 2.95\ mA \tag{5.9}$$

DC power dissipated is given by

$$P_{DC}(SE) = V_{DD} * I_{DC}(SE) = 7.96\ mW$$

Drain efficiency ($\eta_D$) is given by

$$\eta_D = \frac{P_{\text{OUT}}}{P_{DC}(SE)} = 50\ \%$$

Since the peak $P_{OUT}$ is *6 dBm* and is operated as class A, simple cascode structure can be used for driver (shown in Figure 5.1).



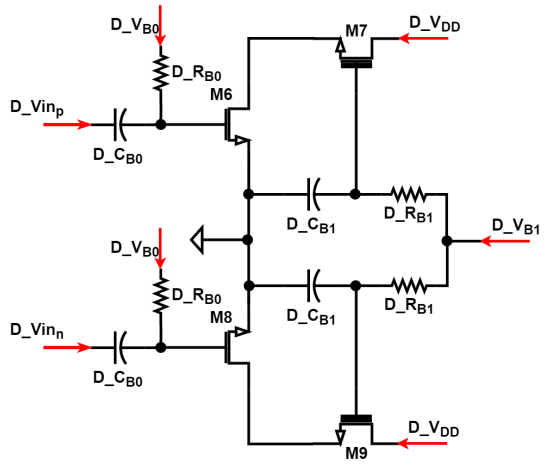



**Figure 5.1:** Schematics of the driver

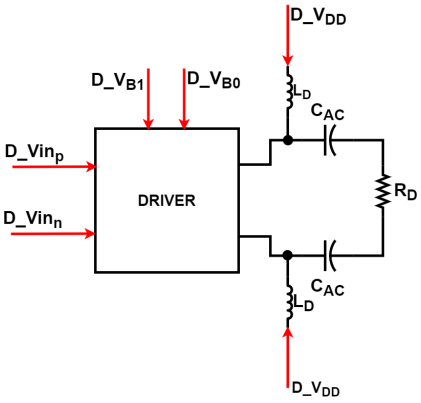



**Figure 5.2:** Schematics of test bench for simulating driver

Figure 5.3 shows $I_D$ versus $V_{DS}$ of the nominal device on left side and $I_D$ versus $V_{DS}$ of thick oxide device on the right side. Load-line is plotted using $V_{FUND}$ and $I_{FUND}$ which is calculated using Equation 5.5 and 5.7. From this, the $W/L$ and biasing voltages of the top and bottom transistors can be calculated.

Figure 5.2 shows test bench used to test the driver cell. $L_D$ is used to feed the $V_{DD}$ and $C_{AC}$ is used to block DC in the $R_D$. $R_D$ isn't a physical component, but it is the impedance seen from the drain of the driver. It is added here solely for simulation purpose . In reality, $V_{DD}$ for the driver is fed through the center tap of the inter-stage transformer.

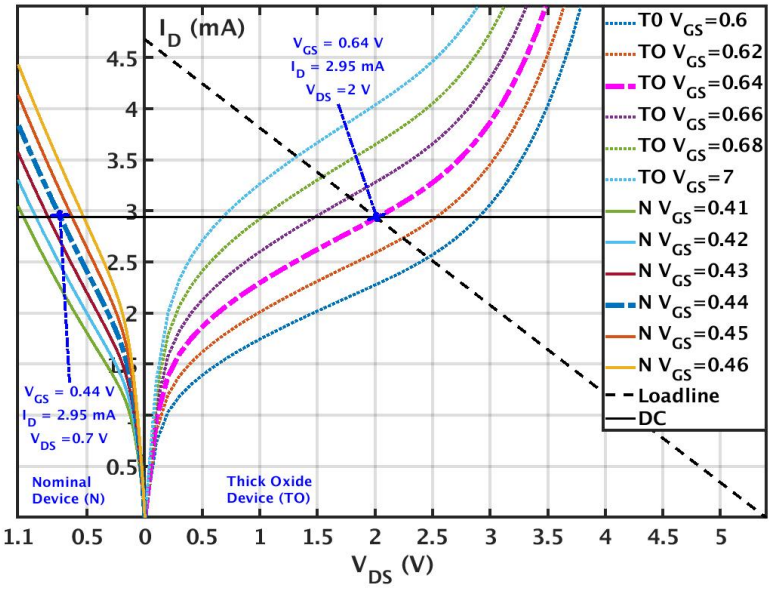



**Figure 5.3:** Load-line for the driver

| Transistors | Top transistor ($M_7$ & $M_9$) Thick oxide | Bottom transistor ($M_6$ & $M_8$) Nominal |
|---|---|---|
| **Finger width ($W$)** | 1 um | 1 um |
| **Fingers ($F$)** | 32 | 32 |
| **Multiplier ($M$)** | 80 | 50 |
| **Total width ($W_T$)** | 2.56 mm | 1.6 mm |

**Table 5.2:** Aspect ratio ($W/L$) of the transistors in the driver

The biasing point and aspect ratio of the transistors in the driver cell was tuned such that the class of operation shifts to AB instead of A as well as meet the $OIP3$ and $OP1dB$ specifications. The optimized biasing point and aspect ratio of the transistors are shown in Table 5.4. $R_D = 200\ \Omega$ needs to be presented to the drain of the driver cell. This value is selected so that the voltage gain ($G_V$) and the linearity requirements of the driver cell are met. The function of capacitor $D\_C_{B1}$ is to make sure that the thick oxide devices ($M_7$ & $M_9$) acts as a cascode. Meanwhile, $D\_C_{B0}$ acts as an AC coupling capacitor and makes sure that only the AC signal reaches the gate of the bottom transistors ($M_6$ & $M_8$).

| | | |
|---|---|---|
| $M_7$ & $M_9$ | Width ($W$) ($um$) | 1 |
| | Fingers ($F$) | 32 |
| | Multiplier ($M$) | 6 |
| $M_6$ & $M_8$ | Width ($W$) ($um$) | 1 |
| | Fingers ($F$) | 32 |
| | Multiplier ($M$) | 2 |
| $D\_V_{B1}$ ($V$) | | 1.35 |
| $D\_V_{B0}$ ($V$) | | 0.38 |
| $D\_C_{B1}$ ($pF$) | | 5 |
| $D\_C_{B0}$ ($pF$) | | 5 |

**Table 5.3:** Component values for the driver schematics



| | | | |
|---|---|---|---|
| **Output stage** (*From simulation of schematics*) | **IIP3** | 12 | dBm |
| | **Power gain** | 22.4 | dB |
| | **OIP3** | 34.7 | dBm |
| | **OP1dB** | 25.6 | dBm |
| **Driver** (*From simulation of schematics*) | **IIP3** | 4.1 | dBm |
| | **Power gain** | 13.9 | dB |
| | **OIP3** | 18.0 | dBm |
| | **OP1dB** | 9.4 | dBm |
| **Total** (*Calculated by using Equation 5.1*) | **OIP3** | 33.4 | dBm |
| | **IIP3** | -2.9 | dBm |

**Table 5.4:** $OIP3$ of the driver, output stage and entire system at *2.4 GHz*

Table 5.4 shows the $OIP3$ and $OP1dB$ of the driver and the output stage individually at *2.4 GHz* which is obtained from the simulation of schematics. By using the Equation 5.1, $OIP3$ and $IIP3$ is computed for both the driver and output stage together and is presented in the last row of the Table 5.4. The performance of the driver at *2.1 GHz* and *2.7 GHz* are identical to that of *2.4 GHz*. But it is important to note that the results tabulated here are at the schematics level and before integrating with the output stage.

## 5.3. Conclusion

This section explained the procedure to calculate biasing point and $W/L$ of the transistors in the driver. The subsequent chapter explains the design of inter-stage between the driver and the output stage.

# References

[1] A. Grebennikov and N. Sokal, *Switchmode RF Power Amplifiers. 1st ed.* (Elsevier Inc., 2007).

# 6

# Design of inter-stage matching

This chapter illustrates the procedure to design the inter-stage matching between the **driver** (designed in chapter 5) and the **output stage** (designed in chapter 4). The main function of inter-stage matching is to present *200* $\Omega$ between the drains of the driver over the bandwidth of *2.1 - 2.7 GHz* so as to meet the requirements of linearity and output 1 dB compression point ($OP1dB$). But the main motivation to use transformer as the inter stage matching compared to other alternatives are:

- It provides isolation between supplies of the driver and the output stage;
- It provides wide band matching over the entire bandwidth (*2.1 - 2.7 GHz*).

The concept of double tuned transformer was used to achieve matching over the entire bandwidth [1] [2]. But the double tuned network needs low transformer coupling ($km$), thus increasing the size of transformer in the layout. Also, inductance of primary and secondary coils is comparatively higher than normal transformer matching (can be seen in the later section). Considering these reason, normal transformer matched at *2.4 GHz* was also considered as a candidate for the inter stage matching.
The following section compares *3* cases:

- Case 1 : Double tuned matching without parallel capacitor ($C_{SEC}$);
- Case 2 : Double tuned matching with parallel capacitor ($C_{SEC}$);
- Case 3 : Normal transformer matching.

## 6.1. Types of inter-stage matching

The input impedance of the output stage was measured by doing S-parameter simulation:

$$Rin_{OS} = 2.11\ k\Omega$$

$$Cin_{OS} = 0.81\ pF$$

The output capacitance of the driver was measured similar to the output stage. The technique is discussed in the Appendix A.

$$C_{DS\_DRIVER} = 99.5\ fF$$

The output resistance of the driver is

$$Rout_{DRIVER} = 15\ k\Omega$$

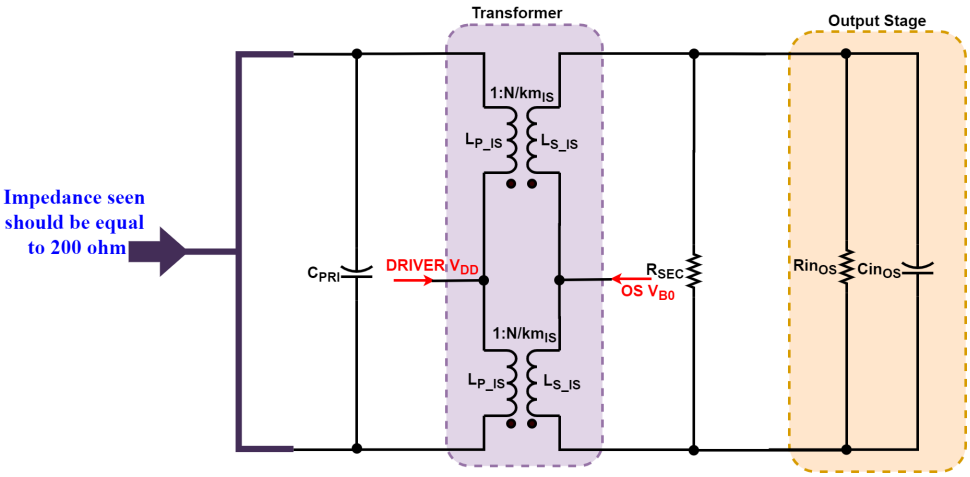



**Figure 6.1:** Schematics of double tuned transformer

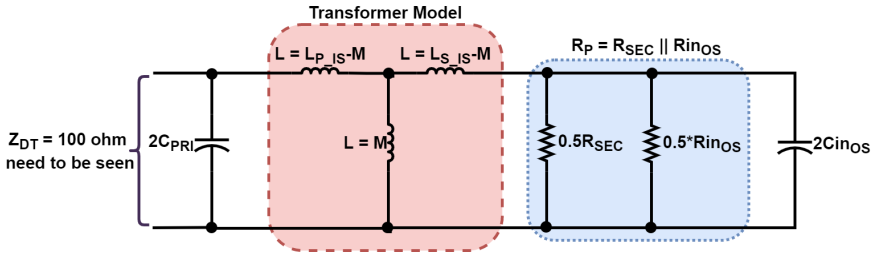



**Figure 6.2:** Differential half circuit of double tuned transformer

The schematics of double tuned transformer is shown in Figure 6.1. In the differential half circuit (Figure 6.2), the transformer is modelled using primary inductance ($L_{P\_IS}$), secondary inductance ($L_{S\_IS}$) and mutual inductance between them ($M$), which is elucidated in [3].

$Z_{DT}$ is calculated as

$$Z_{DT} = \frac{-\omega\left(-Cin_{OS}R_P T\omega^2 + jT\omega - L_{P\_IS}R_P\right)}{\left(jTR_P C_{PRI} Cin_{OS}\omega^4 + C_{PRI}T\omega^3 + j\left(C_{PRI}L_{P\_IS} + Cin_{OS}L_{S\_IS}\right)R_P\omega^2 + L_{S\_IS}\omega - jR_P\right)} \tag{6.1}$$

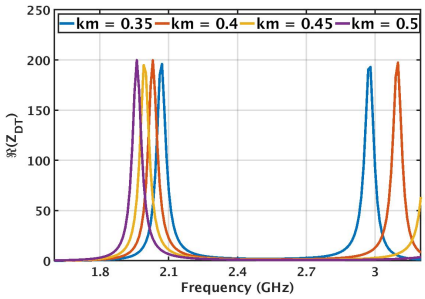
where

$$T = -L_{P\_IS}L_{S\_IS} + M^2$$

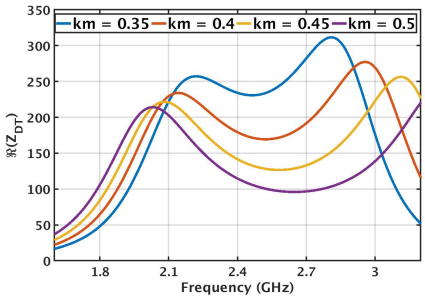
$$km = \frac{M}{\sqrt{L_{P\_IS}L_{S\_IS}}}$$

$$R_P = R_{SEC}||Rin_{OS}$$

The $R_{SEC}$ is added in parallel to $Rin_{OS}$ in order to reduce the input resistance of the output stage. In case $R_{SEC}$ is not added or the value is higher than *200 Ω*, then the input resistance of the output stage is high and there will be a large dip occurring at *2.4 GHz* (Figure 6.3a). Consequently, *200 Ω* won't be seen by the driver at *2.4 GHz*, thus affecting the linearity performance of the PA and voltage gain of the driver at that frequency. This is the reason that the designs with double tuned transformer have $R_{SEC} \approx$ *200 Ω*. In addition, $R_{SEC}$ around *200 Ω* keeps the turn ratio of the inter-stage transformer to be unity. On the contrary, a value lower than *200 Ω* (for eg. *150 Ω*) can reduce voltage gain of the system and also bring two peaks together. Thus, having lower matching at *2.1 GHz* and *2.7 GHz*. From Figure 6.3, it is seen that the spacing between the peaks is primarily determined by transformer coupling ($km_{IS}$) whereas $L_{S\_IS}$ decides at which frequency the peak occurs.



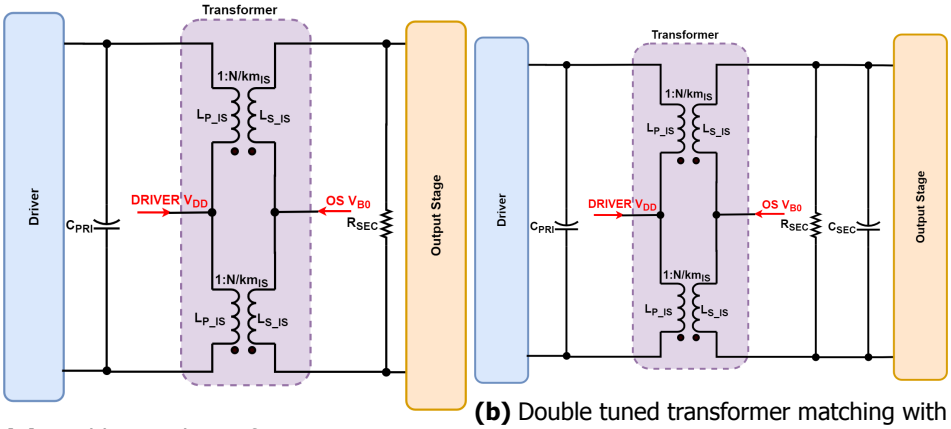

**(a)** Without $R_{SEC}$




**(b)** With $R_{SEC}$ = 200 Ω

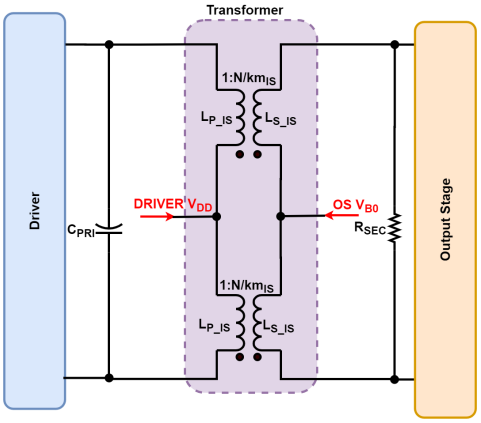
**Figure 6.3:** $\Re(Z_{DT})$ for different values of $km$ and $R_{SEC}$

Figure 6.4a and 6.4b shows the schematics of double tuned transformer with and without $C_{SEC}$. Normal transformer matching schematics (Figure 6.4c) is similar to schematics of double tuned transformer without $C_{SEC}$ (Figure 6.4a) but the value of $L_{P\_IS}$, $L_{S\_IS}$ and $km_{IS}$ is different.




**(a)** Double tuned transformer matching without $C_{SEC}$ (Case 1)

**(b)** Double tuned transformer matching with $C_{SEC}$ (Case 2)




**(c)** Normal transformer matching (Case 3)

**Figure 6.4:** Inter-stage designs

### 6.1.1. Case 1 : Double tuned matching without parallel capacitor ($C_{SEC}$)

The capacitance ($C_{PRI}$) connected to the primary side of transformer (refer Figure 6.5) is calculated as

$$C_{PRI} = Cin_{OS} * N^2 - \frac{C_{DS\_DRIVER}}{2} \tag{6.2}$$

The turn ratio of transformer

$$N = \sqrt{\frac{R_{SEC}}{200}} \tag{6.3}$$

The primary inductance $L_{P\_IS}$ can be calculated as

$$L_{P\_IS} = \frac{L_{S\_IS}}{N^2} \tag{6.4}$$

The variables available for tuning is secondary inductance ($L_{S\_IS}$), resistance added at secondary side ($R_{SEC}$) and transformer coupling ($km_{IS}$). The values of components are shown in Table 6.1.

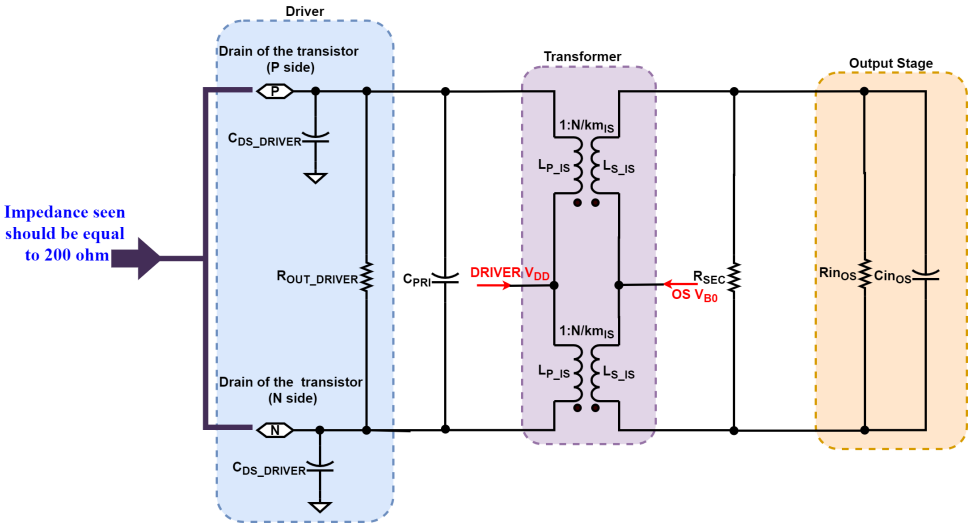



**Figure 6.5:** Schematics of double tuned matching without parallel capacitor ($C_{SEC}$)

### 6.1.2. Case 2 : Double tuned matching with parallel capacitor ($C_{SEC}$)

Compared to the previous design, a capacitance $C_{SEC}$ is added to secondary side. This is done to reduce both $L_{P\_IS}$ and $L_{S\_IS}$.

The capacitance ($C_{PRI}$) connected to the primary side of transformer (refer Figure 6.6) is calculated as

$$C_{PRI} = (Cin_{OS} + C_{SEC}) * N^2 - \frac{C_{DS\_DRIVER}}{2} \tag{6.5}$$

$N$ and $L_{S\_IS}$ can be calculated using the Equation 6.3 and 6.4. Like the previous design, $L_{S\_IS}$, $R_{SEC}$ and $km_{IS}$ are available for tuning. In addition to this, $C_{SEC}$ is also available. The values of components are shown in Table 6.1.

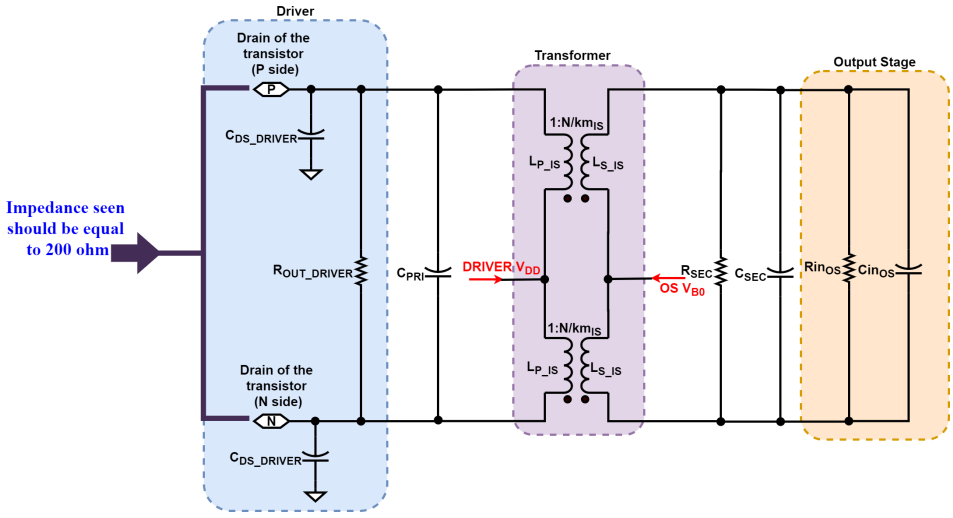



**Figure 6.6:** Schematics of double tuned matching with parallel capacitor $C_{SEC}$

### 6.1.3. Case 3 : Normal transformer matching

In this case, transformer is designed to provide *200* Ω only at *2.4 GHz* and not at other frequencies like *2.1 GHz* and *2.7 GHz*. $R_{SEC}$ is added here so that the turn ratio of the inter-stage transformer is not very large so as to present *200* Ω between the drains of the driver. The main motivation to test this design is that $L_{P\_IS}$ and $L_{S\_IS}$ is lower than previous designs and also $km_{IS}$ is high. The above-mentioned specifications reduces the transformer size in layout significantly. The values of components are shown for normal transformer matching in Table 6.1.

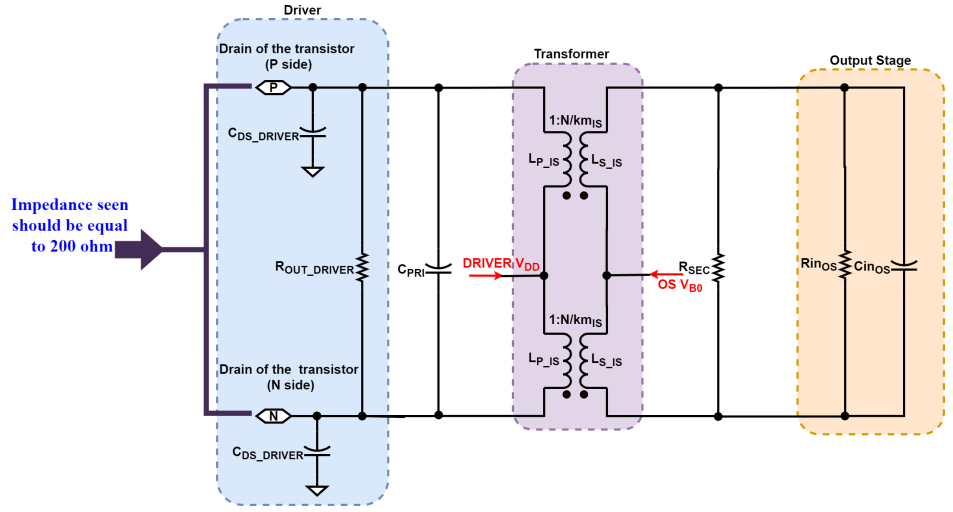



**Figure 6.7:** Schematics of normal transformer matching

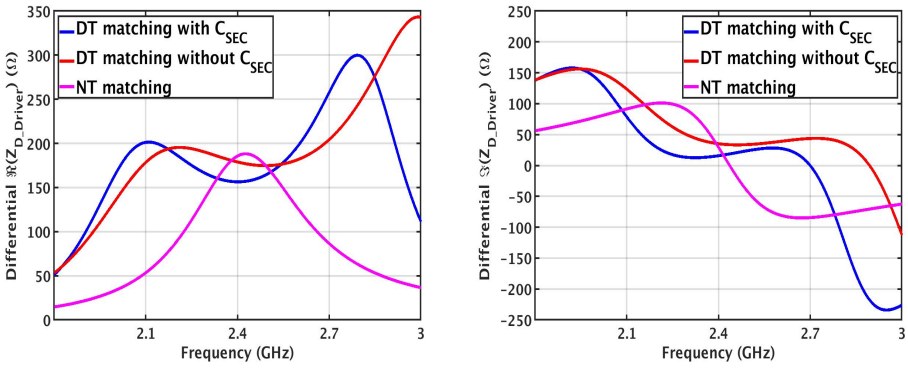
## 6.2. Double tuned transformer vs Normal transformer

This section compares the performance of the PA with the 3 designs of inter-stage.

| | **Case 1 : Double tuned transformer matching without $C_{SEC}$** | **Case 2 : Double tuned transformer matching with $C_{SEC}$** | **Case 3 : Normal transformer matching** |
|---|---|---|---|
| $R_{SEC}$ **(Ω)** | 200 | 160 | 200 |
| $C_{SEC}$ **(*pF*)** | - | 0.5 | - |
| $L_{P\_IS}$ **(*nH*)** | 2.7 | 2.25 | 1.25 |
| $L_{S\_IS}$ **(*nH*)** | 2.7 | 1.8 | 1.25 |
| $km_{IS}$ | 0.4 | 0.35 | 0.85 |
| $C_{PRI}$ **(*pF*)** | 0.7 | 0.95 | 1 |

**Table 6.1:** Component values for the 3 designs of inter-stage matching

The differential impedance (both real and imaginary part) presented to the drains of the driver is shown in Figure 6.8. It is seen that normal transformer matching (case 3) doesn't present *200* Ω at *2.1 GHz* and *2.7 GHz* which is expected as per the design. The other 2 inter-stage designs which uses double tuned network concept present around *200* Ω for the entire bandwidth (*2.1 - 2.7 GHz*).




**(a)** Resistance (real part) **(b)** Reactance (imaginary part)

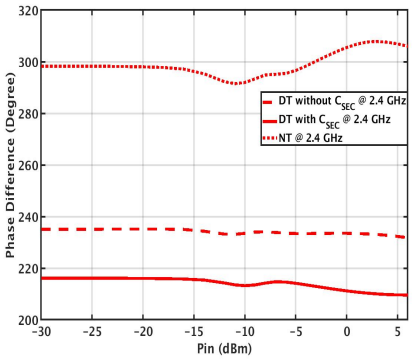
**Figure 6.8:** Impedance presented to the driver for *3* designs of inter-stage matching

From Table 6.2, it is seen that normal transformer matching (*case 3*) has similar performance at *2.1 GHz* and *2.7 GHz* in terms of maximum efficiency even though

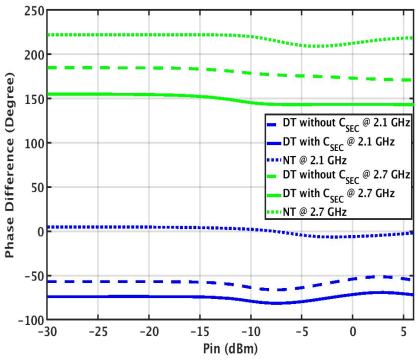
| | | Case 1 : Double tuned Transformer matching without $C_{SEC}$ | | | Case 2 : Double tuned transformer matching with $C_{SEC}$ | | | Case 3 : Normal transformer matching | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Class of Operation** | | **Class F** | **CCF** | | **Class F** | **CCF** | | **Class F** | **CCF** | |
| **Frequency (*GHz*)** | | **2.4** | **2.1** | **2.7** | **2.4** | **2.1** | **2.7** | **2.4** | **2.1** | **2.7** |
| **OP1dB (*dB*)** | | 25.0 | 25.0 | 25.3 | 25.1 | 25.1 | 25.3 | 23.1 | 24.7 | 25.1 |
| **Efficiency ($\eta$)(%)** | **Max** | 67.3 | 62.1 | 67.5 | 67.4 | 60.9 | 70.6 | 69.1 | 61.7 | 68.2 |
| | **@ P1dB** | 56.2 | 56.1 | 61.8 | 56.1 | 57.5 | 62.0 | 48.4 | 55.1 | 61.3 |
| | **@ Pout = 18 dBm** | 20.1 | 19.9 | 20.5 | 20.1 | 20.0 | 20.5 | 20.2 | 19.9 | 20.6 |
| | **@ Pout = 16.5 dBm** | 15.2 | 15.1 | 15.4 | 15.2 | 15.1 | 15.4 | 15.2 | 15.1 | 15.5 |
| **EVM (*dB*)** | **@ Pout = 18 dBm** | -31.4 | -28.5 | -30.3 | -30.9 | -29.7 | -27.6 | -25.3 | -25.8 | -28.4 |
| | **@ Pout = 16.5 dBm** | -36.8 | -34.2 | -34.9 | -35.3 | -35.1 | -31.5 | -29.4 | -29.3 | -34.4 |
| **Voltage Gain (*dB*)** | | 30 | 29.7 | 30.5 | 28.4 | 29.4 | 30.5 | 30.0 | 24.2 | 27.3 |

**Table 6.2:** Performance of PA with *3* inter-stage designs

the driver doesn't see an impedance of *200* $\Omega$. This shows efficiency is dominated by the output stage and not the driver. But in terms of EVM, there is a significant degradation for normal transformer matching (case 3) even at *2.4 GHz* where the impedance is matched to *200* $\Omega$. This can be attributed to the large AM-PM shift for normal transformer matching which is showcased in Figure 6.9a. Figure 6.9b shows that the trend is same for *2.1 GHz* and *2.7 GHz*. Double tuned transformer with $C_{SEC}$ (*case 2*) is selected as it has lower value of $L_{P\_IS}$ and $L_{S\_IS}$ than *case 1* as well as better EVM performance compared to *case 3*.




**(a)** AM-PM for *2.4 GHz*




**(b)** AM-PM for *2.1 GHz* and *2.7 GHz*

**Figure 6.9:** Phase difference between input of the driver and the output of the output stage (AM-PM) for 3 designs of inter-stage matching ($DT$ - double tuned transformer and $NT$ - normal transformer)

## 6.3. Conclusion

This chapter illustrated the procedure to design the inter-stage matching. The inter-stage matching is designed using double tuned transformer with $C_{SEC}$ (*case 2*) as it has lower $L_{P\_IS}$ and $L_{S\_IS}$ and better EVM performance. Upcoming chapter shows the entire circuit of the PA and final results using schematics.

## References

[1] M. Vigilante and P. Reynaert, *On the design of wideband transformer-based fourth order matching networks for $E$ -band receivers in 28-nm cmos,* IEEE Journal of Solid-State Circuits **52**, 2071 (2017).

[2] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, *An ultra-wideband if millimeter-wave receiver with a 20 ghz channel bandwidth using gain-equalized transformers,* IEEE Journal of Solid-State Circuits **51**, 323 (2016).

[3] J. R. Long, *Monolithic transformers for silicon rf ic design,* IEEE Journal of Solid-State Circuits **35**, 1368 (2000).

# 7

# Entire PA (Driver, inter-stage, output stage & output network)

This chapter shows the results of the entire circuit (driver, inter-stage, output stage and output network) schematics at $125^0$ C. It also checks if circuit is layout friendly in terms of the size of the transformer and inductance of primary and secondary coils in the output network.

## 7.1. PA performance based on schematics

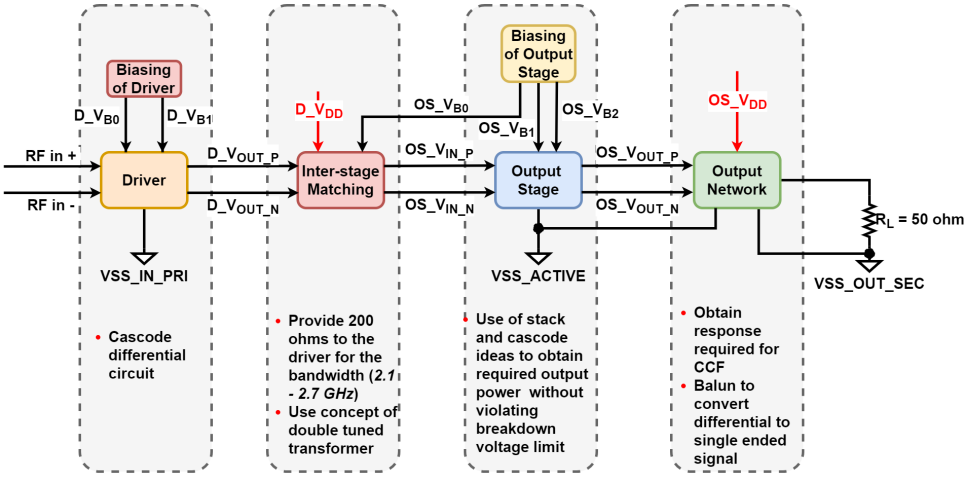



**Figure 7.1:** PA architecture

The chapters 5, 6, 4, and 3 discussed the design of the driver, inter-stage matching, output stage and output network respectively.

From two-tone test, $OIP3$ for the entire system consisting of the driver, inter-stage matching, output stage and output network was simulated to be *32.2 dBm* at *2.4 GHz*. This matches with the value (*33.4 dBm*) calculated in chapter 5. Thus, confirming that linearity is dictated by the output stage and not the driver.

| **Class of Operation** | | **Class F** | **CCF** | |
|---|---|---|---|---|
| **Frequency (*GHz*)** | | **2.4** | **2.1** | **2.7** |
| **OP1dB (*dB*)** | | 25.1 | 25.1 | 25.3 |
| **Efficiency ($\eta$)(*%*)** | **Max** | 67.4 | 60.9 | 70.6 |
| | **@ P1dB** | 56.1 | 57.5 | 62 |
| | **@ Pout = 18 dBm** | 20.1 | 20.0 | 20.5 |
| | **@ Pout = 16.5 dBm** | 15.2 | 15.1 | 15.4 |
| **EVM (*dB*)** | **@ Pout = 18 dBm** | -30.9 | -29.7 | -27.6 |
| | **@ Pout = 16.5 dBm** | -35.3 | -35.1 | -31.5 |
| **Voltage Gain (*dB*)** | | 28.4 | 29.4 | 30.5 |
| **IM3 (*dBc*)** | **@ Pin = -20 dBm** | -40.5 | -46 | -46.3 |
| | **@ Pin = -7 dBm** | -15.1 | -19.9 | -13.1 |
| **OIP3 (*dBm*)** | | 32.2 | 31.5 | 35.9 |

**Table 7.1:** Performance of PA with the driver, inter-stage, output stage and output network

The value of inductance of primary and secondary coils are *2.2 nH* and *3.9 nH*. These values are pretty large and can't be created inside the chip efficiently. In the chapter 3, value of transformer coupling ($km$) is chosen as *0.8* for designing the output network where ever the number of variables is more than the number of equations. Below section discusses the effect of varying transformer coupling ($km$) on component values and performance of the PA.

## 7.2. Influence of transformer coupling ($km$) in the output network on PA performance

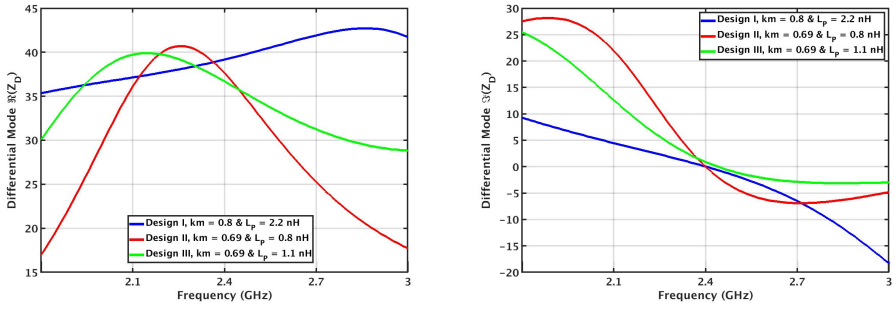
From Table 7.2, it is seen that reducing transformer coupling ($km$) reduces inductance of the primary ($L_P$) and the secondary coil ($L_S$) of the output balun. At the same time, inductance of second harmonic trap ($L_2$) increases with $km$. The *Design*

| Output Network Design | $L_{BND}$ (nH) | $L_P$ (nH) | $N$ | $km$ | $L_S$ (nH) | $C_L$ (pF) | $L_2$ (nH) | $C_2$ (pF) | $C_{DCP}$ (pF) | Selected Designs |
|---|---|---|---|---|---|---|---|---|---|---|
| Design A (no RF Choke & with $L_2C_2$) | 1 | 3 | 1.38 | 0.85 | 5.8 | 0.9 | 0.7 | 1.5 | 100 | |
| | ***1*** | ***2.2*** | ***1.34*** | ***0.8*** | ***3.9*** | ***0.9*** | ***0.7*** | ***1.5*** | ***100*** | **I** |
| | 1 | 1.7 | 1.25 | 0.75 | 2.7 | 1 | 0.8 | 1.4 | 100 | |
| | 1 | 0.7 | 0.94 | 0.7 | 0.7 | 3 | 2.4 | 0.5 | 100 | |
| | 1 | 1.2 | 1.15 | 0.7 | 1.6 | 1.3 | 0.9 | 1.3 | 100 | |
| | ***1*** | ***0.8*** | ***0.99*** | ***0.69*** | ***0.8*** | ***2.4*** | ***1.5*** | ***0.8*** | ***100*** | **II** |
| | ***1*** | ***1.1*** | ***1.11*** | ***0.69*** | ***1.4*** | ***1.5*** | ***0.9*** | ***1.2*** | ***100*** | **III** |
| | **No solution exist for values of $km$ below 0.69** | | | | | | | | | |

**Table 7.2:** Component values in Design A for different transformer coupling $km$

*I* (highlighted in blue in Table 7.2) represents Design A[1] output network with $km$ = *0.8* in the output balun which was previously chosen in chapter 4. The *Design II* (highlighted in red in Table 7.2) and *Design III* (highlighted in green in Table 7.2) denotes variants of Design A output network with $km$ = *0.69* in the output balun. These *2* designs are shortlisted to be compared with *Design I* because they have the least value of $L_P$, $L_S$ and $L_2$ compared to the others in the table. In the following subsection, impedance of *Design II* and *III* will be compared with that of *Design I* at $1^{st}$, $2^{nd}$ and $3^{rd}$ harmonic.

## 7.2.1. Impedance at first harmonic ($\omega_0$)



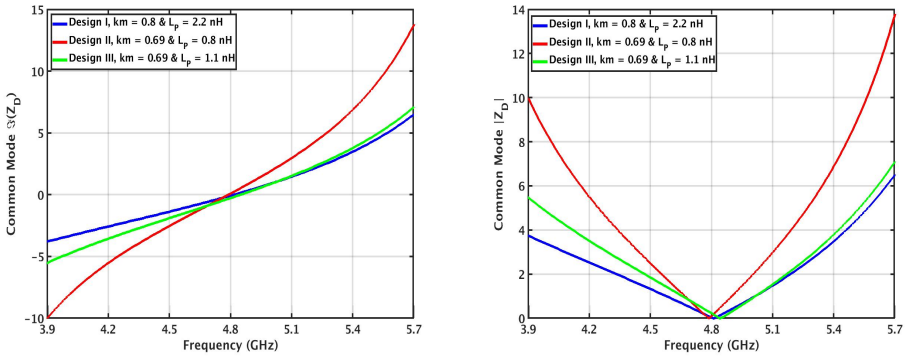

**(a)** Real part of $Z_D$ ($\Re(Z_D)$) **(b)** Reactive part of $Z_D$ ($\Im(Z_D)$)

**Figure 7.2:** Impedance ($Z_D$) at $1^{st}$ harmonic ($\omega_0$) for different values of $km$

From Figure 7.2a, it is seen that real part at $1^{st}$ harmonic is flatter in the bandwidth *2.1 - 2.7 GHz* for *Design I* compared to *Design II* and *III*. Also, reactance is larger in *Design II* and *III* compared to *Design I* which is shown in Figure 7.2b.

[1]no RF choke and with $L_2C_2$

### 7.2.2. Impedance at second harmonic ($2\omega_0$)




**(a)** Reactive part of $Z_D$ ($\Im(Z_D)$) **(b)** Magnitude of $Z_D$ ($|Z_D|$)

**Figure 7.3:** Impedance ($Z_D$) at $2^{nd}$ harmonic ($2\omega_0$) for different values of $km$

From Figure 7.3a and 7.3b, it is seen that *Design II* has larger magnitude at $2^{nd}$ harmonic compared to other designs. Since in CCF, $1^{st}$ harmonic reactance and $2^{nd}$ harmonic reactance should have an inverse relationship. Thus, in *Design II*, reactance is larger at $1^{st}$ and $2^{nd}$ harmonic, therefore keeping the CCF requirements intact.

7

### 7.2.3. Impedance at third harmonic ($3\omega_0$)

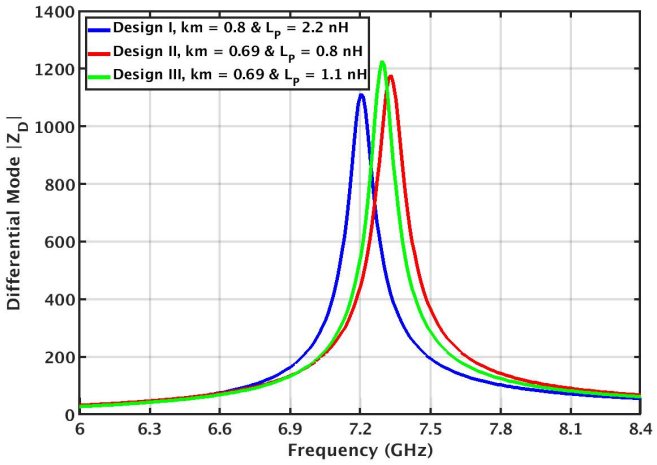



**Figure 7.4:** Magnitude of $Z_D$ ($|Z_D|$) at $3^{rd}$ harmonic ($3\omega_0$) for different values of $km$

As designed, *3* variants of Design A[2] output network have an impedance of *1000* Ω at $3^{rd}$ harmonic. It is also seen that impedance at *2.1 GHz* and *2.7 GHz* is less for all *3* output network designs. From the section 4.4, it is important to note that the $3^{rd}$ harmonic impedance doesn't have significant effect on the PA performance.

### 7.2.4. Performance comparison

| Frequency (*GHz*) | Parameter | I | II | III |
|---|---|---|---|---|
| 2.4 | $\eta$ @ **P1dB** (*%*) | 56.1 | 56.5 | 55.9 |
| | **OP1dB** (*dBm*) | 25.1 | 25.3 | 25.3 |
| | $\eta$ @ **Pout = 18 dBm** (*%*) | 20.1 | 20.0 | 19.9 |
| | $\eta$ @ **Pout = 16.5 dBm** (*%*) | 15.2 | 15.1 | 15.0 |
| | **EVM @ Pout = 18 dBm** (*dB*) | -30.9 | -30.7 | -31.7 |
| | **EVM @ Pout = 16.5 dBm** (*dB*) | -35.3 | -34.4 | -35.8 |
| 2.1 | $\eta$ @ **P1dB** (*%*) | 57.5 | 55.9 | 57.5 |
| | **OP1dB** (*dBm*) | 25.1 | 25.1 | 25.0 |
| | $\eta$ @ **Pout = 18 dBm** (*%*) | 20.0 | 19.4 | 20.0 |
| | $\eta$ @ **Pout = 16.5 dBm** (*%*) | 15.1 | 14.8 | 15.1 |
| | **EVM @ Pout = 18 dBm** (*dB*) | -29.7 | -25.2 | -27.1 |
| | **EVM @ Pout = 16.5 dBm** (*dB*) | -35.1 | -29.6 | -32.1 |
| 2.7 | $\eta$ @ **P1dB** (*%*) | 70.6 | 69.5 | 71.4 |
| | **OP1dB** (*dBm*) | 25.3 | 26.6 | 26.3 |
| | $\eta$ @ **Pout = 18 dBm** (*%*) | 20.5 | 18.6 | 19.4 |
| | $\eta$ @ **Pout = 16.5 dBm** (*%*) | 15.4 | 14.2 | 14.7 |
| | **EVM @ Pout = 18 dBm** (*dB*) | -27.6 | -33.6 | -32.6 |
| | **EVM @ Pout = 16.5 dBm** (*dB*) | -31.5 | -35 | -35.1 |

**Table 7.3:** Efficiency ($\eta$), $OP1dB$ and EVM for *3* variants of Design A output network based on different $km$ values

From Table 7.3, it is seen that all *3* designs have similar performance at *2.4 GHz*. Even though efficiency remains same at *2.1 GHz* and *2.7 GHz*, EVM performance is different in each case. *Design II* is chosen because it has lower inductance for primary and secondary coils for the output balun and the performance of PA isn't

[2]no RF choke and with $L_2C_2$

affected a lot.

The performance of the PA with Design A output network (*Design II*) is tabulated in Table 7.4. The plots showing the voltage and current waveforms at the drain of the top transistor ($M_2$) at *2.1*, *2.4* and *2.7 GHz* are available in Appendix C.

| **Class of Operation** | | **Class F** | **CCF** | |
|---|---|---|---|---|
| **Frequency (*GHz*)** | | **2.4** | **2.1** | **2.7** |
| **OP1dB (*dB*)** | | 25.3 | 25.1 | 26.6 |
| **Efficiency (%)** | **Max** | 68.6 | 59.2 | 69.5 |
| | **@ P1dB** | 56.5 | 55.9 | 60.8 |
| | **@ Pout = 18 dBm** | 20.0 | 19.4 | 18.6 |
| | **@ Pout = 16.5 dBm** | 15.1 | 14.8 | 14.3 |
| **EVM (*dB*)** | **@ Pout = 18 dBm** | -30.7 | -25.2 | -33.6 |
| | **@ Pout = 16.5 dBm** | -34.4 | -29.6 | -35.0 |
| **Voltage Gain (*dB*)** | | 28.3 | 29.3 | 28.6 |
| **IM3 (*dBc*)** | **@ Pin = -20 dBm** | -40.0 | -42.4 | -46.3 |
| | **@ Pin = -7 dBm** | -15.6 | -18.4 | -14.7 |
| **OIP3 (*dBm*)** | | 31.9 | 31.74 | 32.1 |

**Table 7.4:** Performance of the PA with the driver, inter-stage, output stage and Design A output network (*Design II*)

## 7.3. Conclusion

This chapter showed the performance of PA for different variants of Design A based on values of transformer coupling ($km$). In the end, *Design II* (with $km$ = *0.69* and $L_P$ = *0.8 nH*) is chosen because it has smaller inductance for primary and secondary coils. Thus, making it layout friendly. Next chapter describes layout of each component in detail.

# 8

# Layout

This chapter explains the layout of the driver, inter-stage, output stage, and output network (*Design A*[1]) as well as the layout of the entire PA chip. Due to unforeseen circumstances, tape-out in TSMC *22 nm* ULL was canceled by the company *CATENA MICROELECTRONICS B.V.* Later, the entire design was ported to TSMC *40 nm* so that the tape out could happen through TU DELFT in *March 2021*.

## 8.1. Conversion to TSMC 40 nm

Table 8.1 compares the aspect ratio ($W/L$) of the transistors in the driver and output stage, also the values of components in the inter-stage matching and output network between TSMC *22 nm* ULL and TSMC *40 nm*.

The number of multipliers ($M$) for the transistors in the output stage is higher for *40 nm* than *22 nm* due to lower transconductance ($g_m$) of the nominal device in *40 nm*.

By specification, the maximum $V_{DD}$ of the thick oxide is *2.5 V* in *40 nm* compared to that of *1.98 V* in *22 nm*. The value of $C_{ST2}$ is increased from *2.4 pF* to *6 pF* in *40 nm* since the thick oxide device has a higher breakdown voltage in this technology.

But for the driver, the thick oxide has lower $M$ in *40 nm* than *22 nm*. Here, the reason is that *40 nm* has flatter $g_m$, thereby better linearity. So, $M$ of thick oxide device could be reduced in *40 nm*. The nominal device in the driver still has more multipliers in *40 nm* because of lower $g_m$.

The value of components for the inter-stage in *40 nm* were calculated in the same way as shown in the chapter 6. The component values in the output network was kept same for for *22 nm* and *40 nm*. Even though the drain source capacitance ($C_{DS}$) was *1.87 pF* in *22 nm* and *1.7 pF* in *40 nm*. This didn't have any significant effect on the performance of the PA.

[1] no RF choke, with $L_2C_2$ and $km = 0.69$ in the output balun

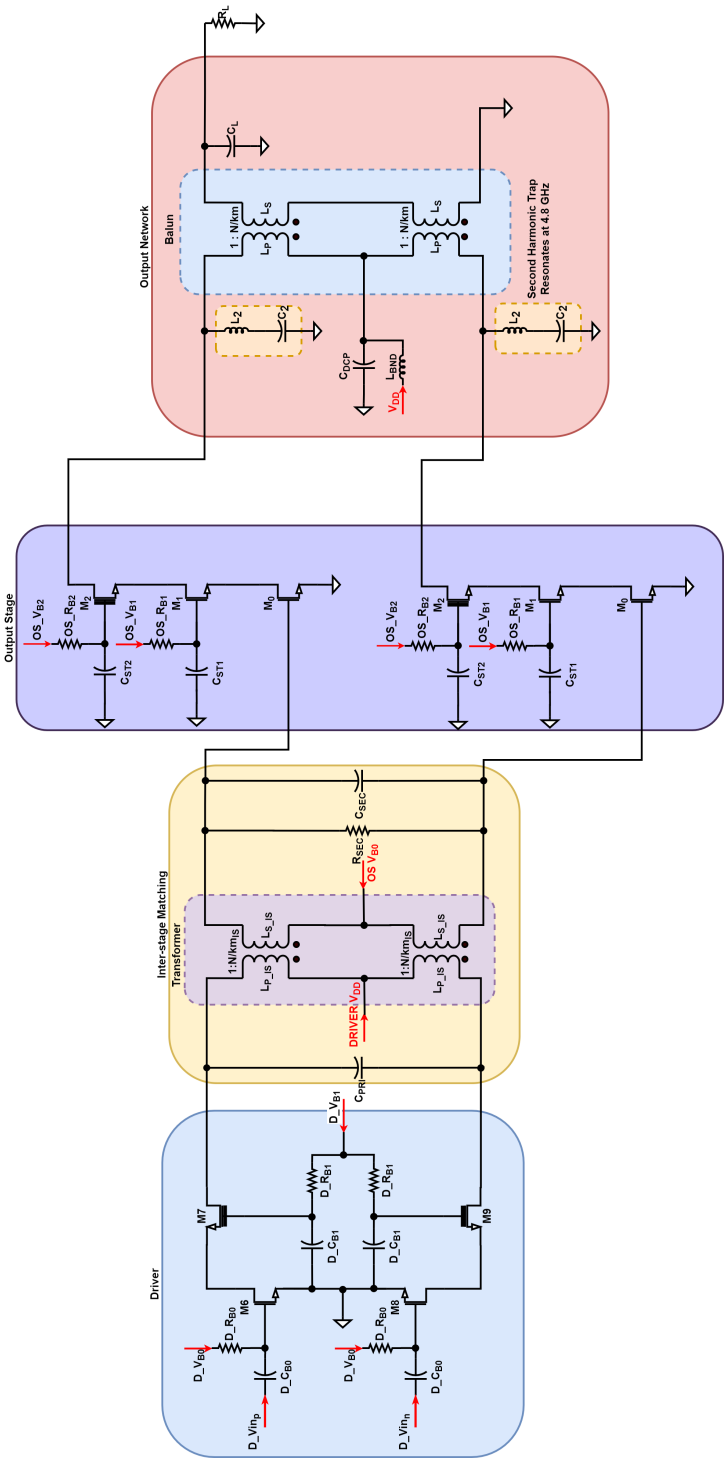



**Figure 8.1:** Entire schematics of the PA consisting of the driver, inter-stage matching, output stage and output network

| Technology | | 22 nm | 40 nm | Unit |
|---|---|---|---|---|
| **Driver** | | | | |
| $M_7$ & $M_9$ | $W*N*M$ | 1*32*6 | 1*32*4 | *um* |
| | $L$ | 30 | 40 | *nm* |
| $M_6$ & $M_8$ | $W*N*M$ | 1*32*2 | 1*32*4 | *um* |
| | $L$ | 30 | 40 | *nm* |
| $D\_V_{B1}$ | | 1.35 | 1.36 | *V* |
| $D\_V_{B0}$ | | 0.38 | 0.46 | *V* |
| $D\_C_{B1}$ | | 5 | 1 | *pF* |
| $D\_C_{B0}$ | | 5 | 1 | *pF* |

| Technology | | 22 nm | 40 nm | Unit |
|---|---|---|---|---|
| **Output stage** | | | | |
| $M_2$ & $M_5$ | $W*N*M$ | 1*32*80 | 1*32*80 | *um* |
| | $L$ | 30 | 40 | *nm* |
| $M_1$ & $M_4$ | $W*N*M$ | 1*32*50 | 1*32*80 | *um* |
| | $L$ | 30 | 40 | *nm* |
| $M_0$ & $M_3$ | $W*N*M$ | 1*32*50 | 1*32*80 | *um* |
| | $L$ | 30 | 40 | *nm* |
| $OS\_V_{B2}$ | | 2.26 | 2.31 | *V* |
| $OS\_V_{B1}$ | | 1.09 | 1.36 | *V* |
| $OS\_V_{B0}$ | | 0.32 | 0.46 | *V* |
| $C_{ST1}$ | | 5 | 5 | *pF* |
| $C_{ST2}$ | | 2.4 | 6 | *pF* |

| Technology | 22 nm | 40 nm | Unit |
|---|---|---|---|
| **Inter-stage matching** | | | |
| $R_{SEC}$ | 160 | 190 | Ω |
| $C_{SEC}$ | 0.5 | 0.11 | *pF* |
| $L_{P\_IS}$ | 2.25 | 2.25 | *nH* |
| $L_{S\_IS}$ | 1.8 | 1.8 | *nH* |
| $km$ | 0.35 | 0.35 | |
| $C_{PRI}$ | 0.95 | 1 | *pF* |

| Technology | 22 nm | 40 nm | Unit |
|---|---|---|---|
| **Output network** | | | |
| $L_P$ | 0.8 | 0.8 | *nH* |
| $L_S$ | 0.8 | 0.8 | *nH* |
| $km$ | 0.69 | 0.69 | |
| $L_2$ | 1.4 | 1.4 | *nH* |
| $C_2$ | 0.8 | 0.8 | *pF* |
| $C_L$ | 2.4 | 2.4 | *pF* |

**Table 8.1:** Component values and aspect ratios of the transistors in TSMC *22 nm* ULL and TSMC *40 nm*



## 8.2. Layout

This section shows the layout of the driver, inter-stage, output stage and output network.

### 8.2.1. Driver

In Figure 8.2, the biasing circuit is highlighted in yellow which is common to both P and N cells. The resistor of 53 Ω is added between each input of the driver and ground (marked with a green rectangle in the right side of Figure 8.2). This is done to obtain 50 Ω matching at inputs of the PA chip to make testing easier.

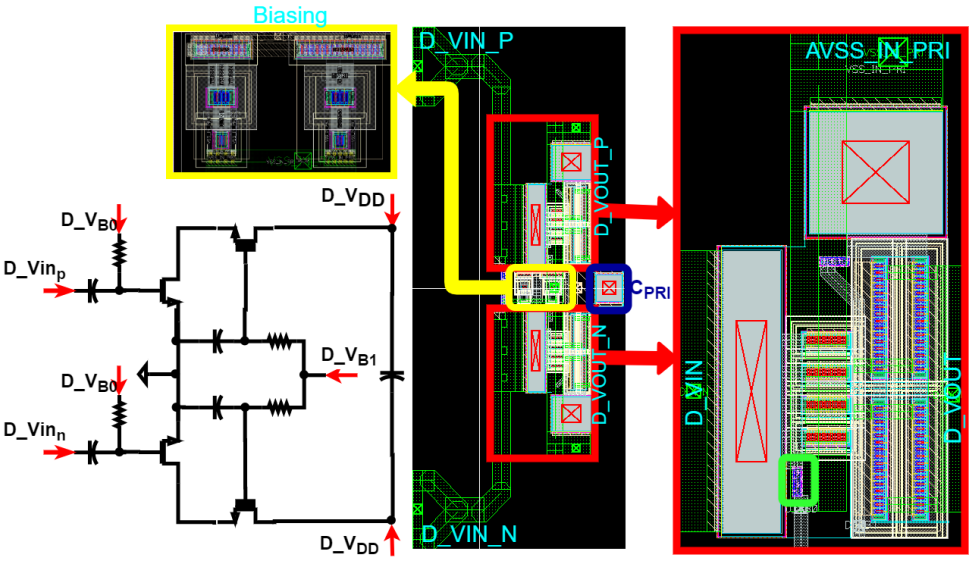



**Figure 8.2:** Layout of the driver

### 8.2.2. Inter-stage matching

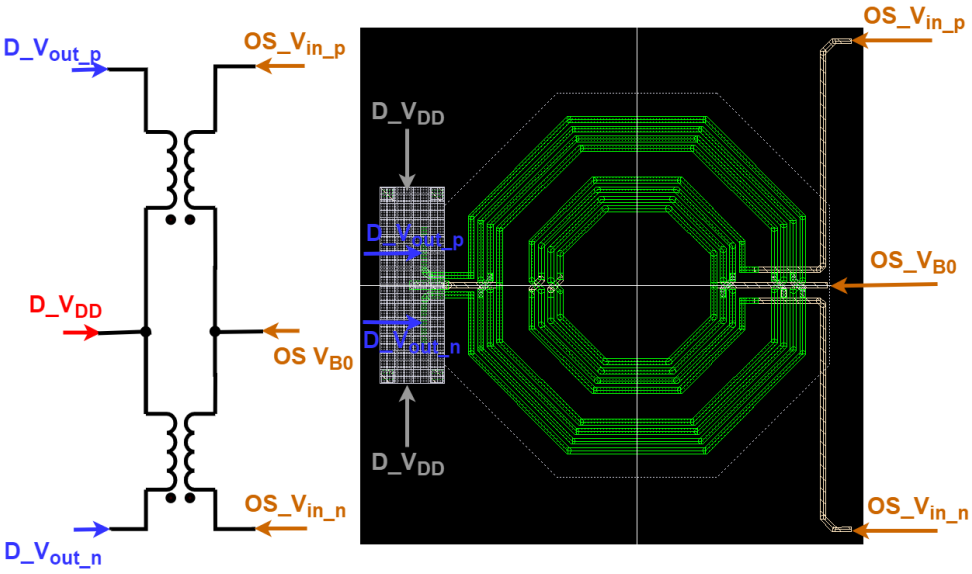



**Figure 8.3:** Layout of inter-stage matching

Due to the parasitic capacitance and resistance in the layout of inter-stage matching (Figure 8.3), $C_{SEC}$ and $R_{SEC}$ are removed. Also, $C_{PRI}$ (marked with a blue rectangle in Figure 8.2) was reduced from *1 pF* to *0.33 pF*. Moreover, $L_{P\_IS}$ and $L_{S\_IS}$ was also reduced to *2.1 nH* and *1.1 nH* respectively to get required matching in the bandwidth *2.1 - 2.7 GHz*[2]. The reason to reduce the inductance is the presence of increased parasitic capacitance due to ultra thick metal layer in *40 nm*. Figure 8.4 shows the differential impedance presented to the drain of the driver for ideal and momentum ($MoM$) simulation case. For this simulation, the outputs of the inter-stage transformer ($OS\_V_{in\_p}$ & $OS\_V_{in\_n}$) are connected to *RC extracted* view of the output stage which is followed by the $MoM$[3] simulation of the output network.

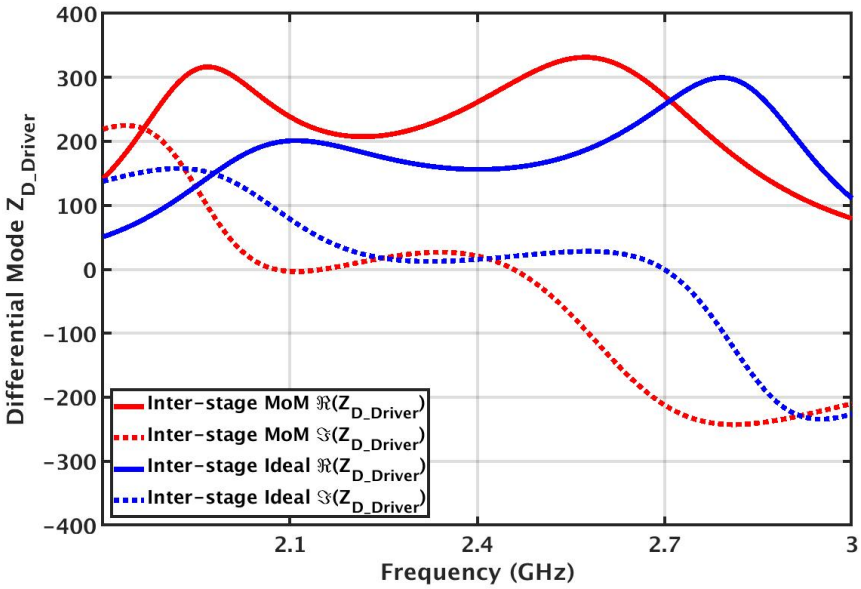



**Figure 8.4:** Differential impedance presented to the drain of the driver ($Z_{D\_Driver}$) for ideal and ($MoM$) simulation case

### 8.2.3. Output stage

In Figure 8.5, P and N cells are marked with a red rectangle. Each cell consist of 4 unit cells which is marked with a blue rectangle in Figure 8.5 and enlarged image is shown in the right side. The biasing voltages $OS\_V_{B2}$, $OS\_V_{B1}$, and $OS\_V_{B0}$ are generated using *3* biasing circuit (highlighted in yellow rectangle in Figure 8.5) which is common to both P and N cells. When individual biasing circuits were provided for each unit cell in the output stage, there wasn't much improvement in the EVM performance. Moreover, there was significant degradation in efficiency

[2]previous value of $L_{P\_IS}$ and $L_{S\_IS}$ was *2.25 nH* and *1.8 nH* which is available in Table 8.1
[3]Momentum file included both inter-stage and output network

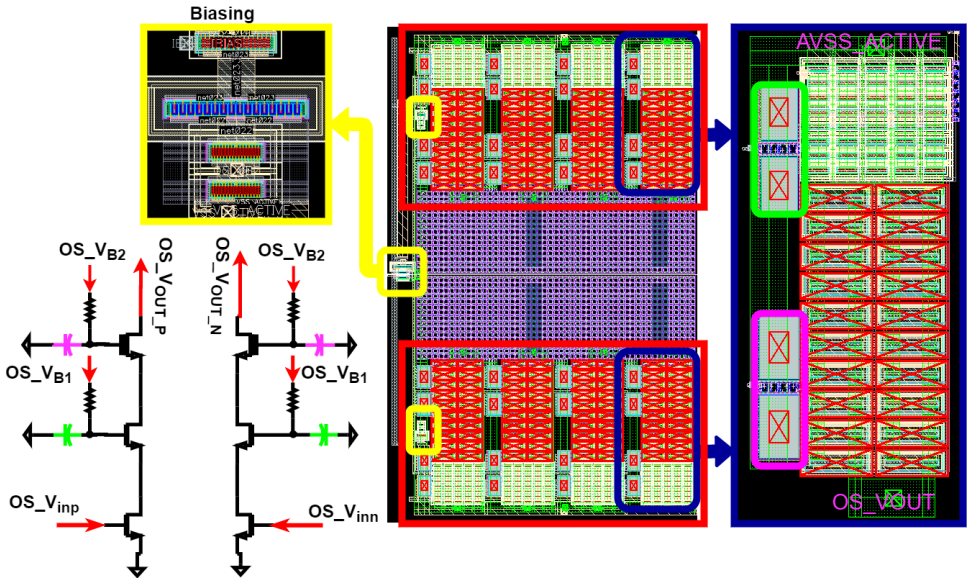



**Figure 8.5:** Layout of output stage

due to increased current consumption in the biasing circuits. Owing to this reason, it was chosen to have global biasing circuits for both P and N cells in the output stage.

### 8.2.4. Output network

The main motivation to have balun with diameter of *600 um* is to have high self resonance frequency (at least above *8.4 GHz*). The designed balun has self resonant frequency of *10 GHz*. The drain of each unit cell in the output stage is connected to output balun at the locations marked with red arrow (P1, P2, P3 and P4) in Figure 8.5. The capacitors $C_2$ and $C_L$ are marked in blue and purple respectively.

The entire output network except the capacitors ($C_2$ and $C_L$) were simulated in the ADS momentum. The $MoM$ simulation of capacitors take a long time due to fringe capacitance and smaller mesh. Instead of $MoM$ simulation, *RC extracted view* can be used to calculate capacitance by performing PEX and both these values matches pretty well.

Figure 8.7 denotes the impedance ($Z_{D\_OS}$) seen from the drains of the output stage for ideal case[4] versus non-ideal case[5]. Ideal case (blue dotted line) is plotted with $C_{DS}$ = *1.7 pF* which is calculated for *40 nm* after the layout of output stage transistors were completed[6]. P1, P2, P3, and P4 (marked with red arrow in Figure 8.6) denotes the points where each unit cell of the output stage is connected to

[4] lossless components
[5] $MoM$ *simulation* for balun and inductor $L_2$ whereas *RC extracted view* for capacitors $C_2$ and $C_L$
[6] Using the technique explained in Appendix A

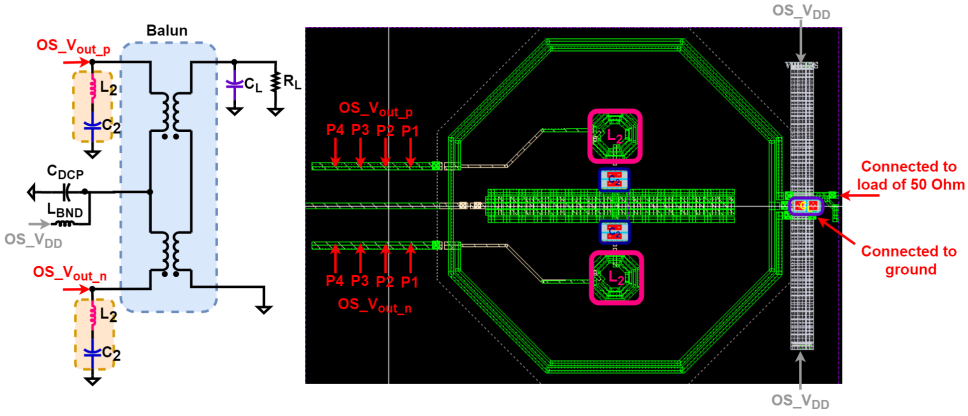
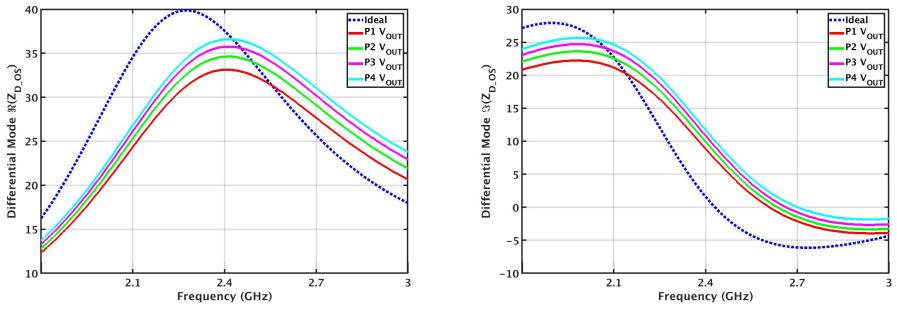



**Figure 8.6:** Layout of output network (balun, second harmonic trap $L_2C_2$, load capacitance $C_L$)

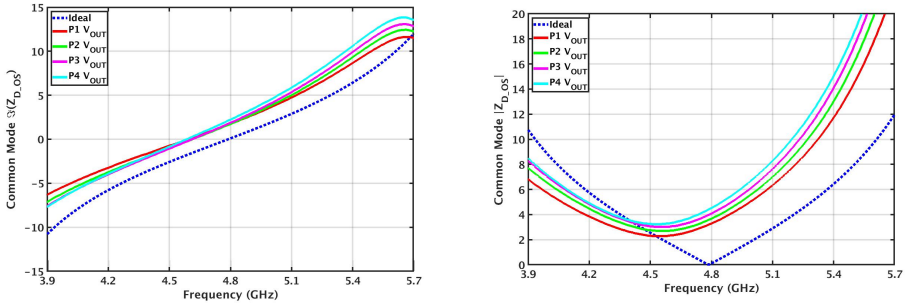
the output balun. This simulation is carried out to estimate the inductance between each unit cell and its effect on output network response.




**(a)** Real part of $Z_{D\_OS}$ ($\Re(Z_{D\_OS})$) **(b)** Reactive part of $Z_{D\_OS}$ ($\Im(Z_{D\_OS})$)

**Figure 8.7:** Impedance ($Z_{D\_OS}$) at $1^{st}$ harmonic ($\omega_0$) for ideal and $MoM$ simulation

Figure 8.8 showcases the reactive part and magnitude of $Z_{D\_OS}$ at $2^{nd}$ harmonic. It is seen that $|Z_{D\_OS}|$ for the non-ideal case doesn't reach *0* because of finite quality factor and attains minimum value of *2.3* Ω at *4.6 GHz*. Another observation made from Figure 8.8a is that zero crossing of $\Im(Z_{D\_OS}(\omega_0))$ has shifted to *4.6 GHz* compared to *4.8 GHz* in the ideal case. But, the requirement for CCF operation is the increasing trend at $\Im(Z_{D\_OS}(2\omega_0))$, so shifting of zero crossing from *4.8 GHz* to *4.6 GHz* doesn't have significant effect on the performance of PA.




**(a)** Reactive part of $Z_{D\_OS}$ ($\Im(Z_{D\_OS})$)

**(b)** Magnitude of $Z_{D\_OS}$ ($|Z_{D\_OS}|$)

**Figure 8.8:** Impedance ($Z_{D\_OS}$) at $2^{nd}$ harmonic ($2\omega_0$) for ideal and $MoM$ simulation

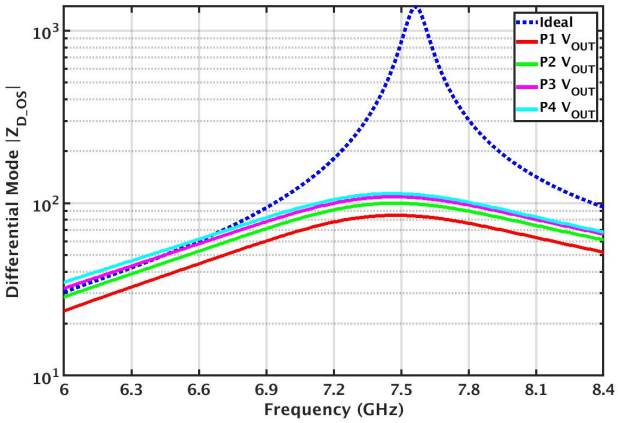



**Figure 8.9:** Magnitude of $Z_{D\_OS}$ at $3^{rd}$ harmonic ($3\omega_0$) for ideal and $MoM$ simulation

Figure 8.9 shows that the peak of $|Z_{D\_OS}(3\omega_0)|$ for the ideal case is shifted slightly from *7.2 GHz* which is due to change in $C_{DS}$ from *1.87 pF* to *1.7 pF*. Similarly, for non-ideal case, $|Z_{D\_OS}(3\omega_0)|$ is lower (around *100* $\Omega$). But, it was explained in section 4.4 that $3^{rd}$ harmonic impedance has trivial effect on PA performance.

## 8.3. Comparison between TSMC 22 nm ULL and TSMC 40 nm

Table 8.2 shows the performance of PA in *22 nm* and *40 nm* with

- *RC extracted view* for the driver, reference generators, output stage and capacitors ($C_2$ & $C_L$) in the output network;

| **Reference Generator** - *RC Extracted* **Driver with biasing** - *RC Extracted* **Output Stage with biasing** - *RC Extracted* **Inter-stage & Output Network** - *MoM* | | **TSMC** ***22 nm* ULL** | | | **TSMC** ***40 nm*** | | |
|---|---|---|---|---|---|---|---|
| **Class of Operation** | | **Class F** | **CCF** | | **Class F** | **CCF** | |
| **Frequency (*GHz*)** | | **2.4** | **2.1** | **2.7** | **2.4** | **2.1** | **2.7** |
| **Output P1dB (*dBm*)** | | 22.6 | 22.4 | 23.9 | 23 | 23 | 22.1 |
| **Efficiency (*%*)** | **Max** | 35.1 | 35.3 | 33.2 | 40.8 | 41.2 | 33.7 |
| | **@ P1dB** | 31.7 | 30.2 | 32.3 | 35.3 | 34.6 | 26.4 |
| | **@ Pout *18 dBm*** | 18.0 | 17.5 | 16.7 | 17.1 | 16.5 | 15.2 |
| | **@ Pout 16.5 *dBm*** | 14.2 | 13.8 | 13.3 | 13.2 | 12.8 | 12.1 |
| **Voltage Gain (*dB*)** | | 26.4 | 28.1 | 24.0 | 24.8 | 26.8 | 20.2 |
| **Output Network Loss (*dB*)** | | -2.1 | -2.1 | -2.2 | -1.2 | -1.2 | -1.4 |
| **OIP3 (*dBm*)** | | 30.7 | 29.1 | 28.0 | 33.8 | 34.9 | 31.5 |
| **IM3 @ Pin = *-20 dBm*** | | -37.6 | -30.9 | -37.8 | -46.3 | -44.4 | -50.9 |
| **IM3 @ Pin = *-7 dBm*** | | -13.0 | -12.0 | -15.1 | -14.9 | -12.5 | -22.8 |

**Table 8.2:** Performance of PA in TSMC *22 nm* ULL and TSMC *40 nm*

- $MoM$ simulation for inter-stage transformer, output balun and $L_2$ of second harmonic trap.

The metal stack in *22 nm* consist of *5* Mx, *2* Mz and AP whereas in *40 nm* consists of *4* Mx, *1* Mz, *1* Ultra and AP. The presence of ultra thick layer has its own merits and demerits. It helps to get higher quality factor in *40 nm* (at least *13* compared to *7* in *22 nm*). But ultra thick metal layer leads to higher capacitance due to increased area. This had significant effect on the design of the output network and inter-stage.

In the case of the output network, the spacing between the drains of output stage (Figure 8.6) were increased to counter increased capacitance. Otherwise, there was peaking in the gain plot which signifies lower phase margin and can lead to instability.

Likewise, in the case of inter-stage matching, $L_{P\_IS}$ and $L_{S\_IS}$ were reduced

to counter increased parasitic capacitance because of ultra thick metal layer and thereby, get required matching in the bandwidth *2.1 - 2.7 GHz*.

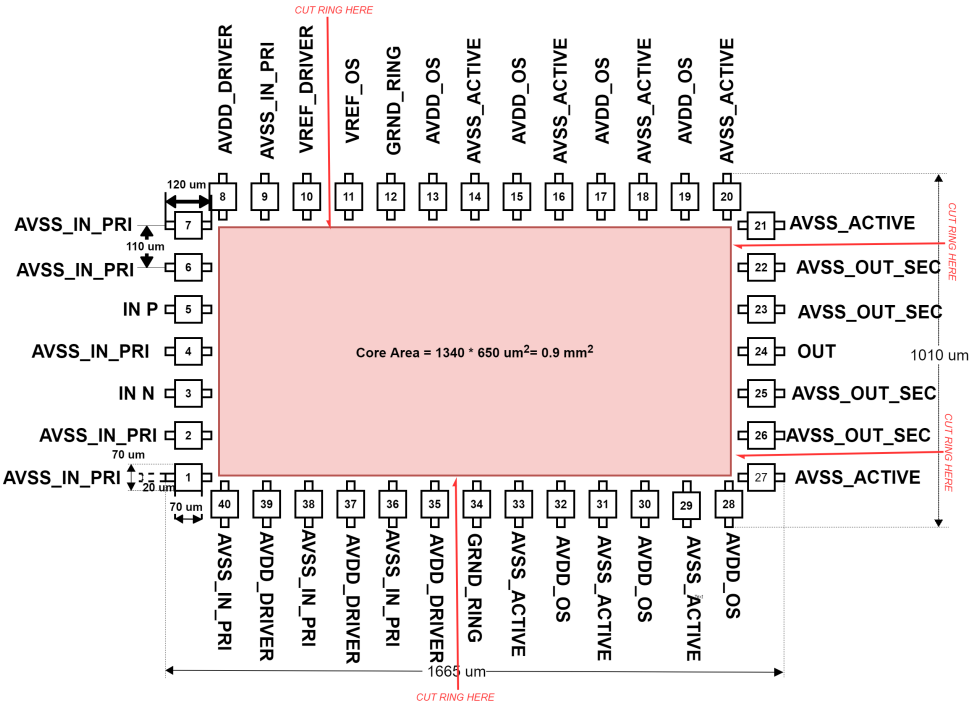



**Figure 8.10:** Pin layout of CCF chip

The pin diagram of the CCF is shown in Figure 8.10. Figure 8.11 portrays the layout of the complete chip including decoupling capacitors[7] and dummy metal fill[8]. The reference generators are marked with a blue rectangle in Figure 8.11. Reference generator circuit takes *1 V* as input and has on chip resistor of *2.35 KΩ* to generate a required current for biasing. Then , this current is copied using current mirrors to the biasing circuit to generate the biasing voltages for the output stage ($OS\_V_{B2}$, $OS\_V_{B1}$ and $OS\_V_{B0}$) and the driver ($D\_V_{B1}$ and $D\_V_{B0}$) (refer Figure B.2 and B.1).

The CCF PA chip has been provided with *3* separate grounds:

- **AVSS_IN_PRI** - connected to the driver;
- **AVSS_ACTIVE** - connected to output stage;
- **AVSS_OUT_SEC** - connected only to output of balun and load capacitance ($C_L$).

[7]Decoupling capacitor consists of a MOM cap, MOS cap and 9 KΩ DQ resistor. The decoupling capacitor was designed by MSc M.R.Beikmirza.

[8]The dummy metal fill was done for passive components like inter-stage transformer and output balun manually such that the performance is not lost.

The motivation to keep grounds of the driver and output stage separate is similar to the reason of having transformer for inter-stage matching, that is, to prevent coupling between them. Since there will be large swing at the output of the balun, it is better to keep different grounds for the output stage and output of the balun. All three grounds are connected together on the printed circuit board (PCB).

## 8.4. Conclusion

This chapter initially explained the conversion of the design[9] to TSMC *40 nm* from TSMC *22 nm* ULL. It also compared the performance of the PA in *22 nm* and *40 nm*. Then, the chapter described the layout of the driver, inter-stage, output stage and output network. The following chapter showcases the post layout results of Continuous Class F power amplifier.



[9] including aspect ratio of transistors, biasing voltage and component values in the output network and inter-stage

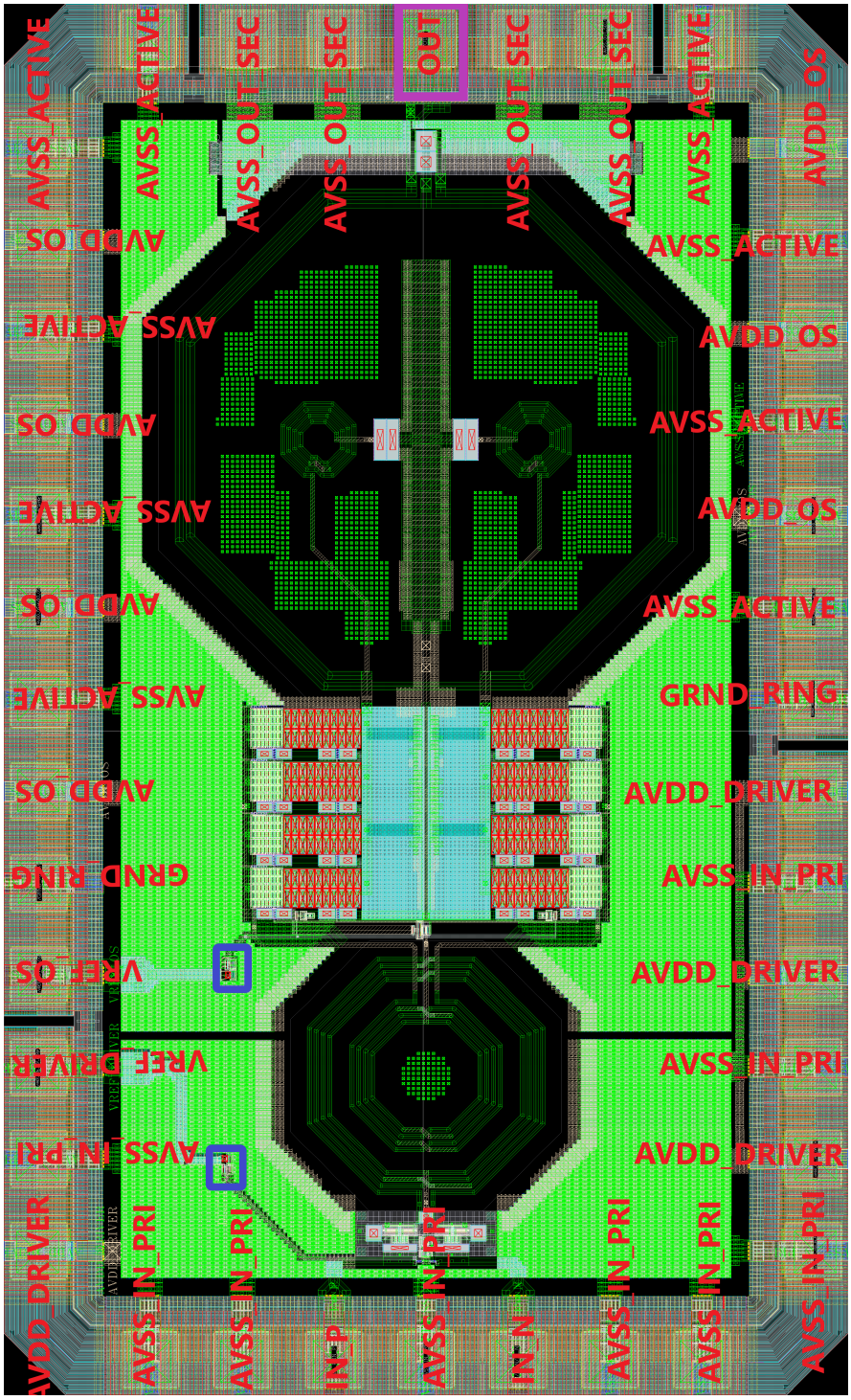



**Figure 8.11:** Chip of Continuous Class F (CCF) power amplifier (PA)

# 9

# Post layout simulation results

The core design which consists of reference current generators, driver, inter-stage matching, output stage and output network is marked with blue rectangle in Figure 9.1. The reference generators, driver, $C_{PRI}$ (part of inter-stage matching), output stage, and $C_2$ and $C_L$ (part of output network) are modeled using *RC extracted view*. The transformer (part of the inter-stage), balun and $L_2$ (part of the output network) are modeled using Momentum ($MoM$) simulation. The inter-stage transformer and output balun with $L_2$ was simulated in a single momentum file. The inputs of the inter-stage ($D\_V_{out\_p}$ and $D\_V_{out\_n}$) were left open and a port was placed between the outputs (between $OS\_V_{in\_p}$ and $OS\_V_{in\_n}$). Similarly, at the inputs of the balun (P1, P2, P3 and P4 of $OS\_V_{out\_p}$ and $OS\_V_{out\_p}$), ports were placed and the outputs were left open. Then, the isolation between the inter-stage transformer and output balun was measured to be *-40 dB*. The ground plane is kept *40 um* away from the transformers so that the parameters of the output network ($L_P$, $L_S$, $km$) and inter-stage transformer ($L_{P\_IS}$, $L_{S\_IS}$, $km_{IS}$) are not varied so much. To further minimize the effect of ground plane, slots are added at the side facing the transformer. This reduces eddy currents as well [1]. The dummy metals were also added to the momentum file for simulation so that the effect of these are also considered [2].

The bondwire inductance ($L_{BND\_VDD}$) for the supply of the driver and output stage ($AVDD\_OS$ and $AVDD\_DRIVER$) is assumed to be *1.5 nH*. Since $AVDD\_OS$ is provided by 9 pins (refer Figure 8.10), the $L_{BND\_VDD}$ is reduced to *1.5 nH/9*[1]. Also, supply and ground are interleaved (refer Figure 8.11) so mutual inductance between the supply $L_{BND}$ can be neglected [3]. Similarly, $L_{BND\_VDD}$ for the supply of the driver is reduced to *1.5 nH/4*. For the 3 grounds, namely $AVSS\_IN\_PRI$, $AVSS\_ACTIVE$ and $AVSS\_OUT\_SEC$, the $L_{BND\_GND}$ is assumed to be *0.5 nH*. Since there are multiple pins connected to ground similar to supply, the approximated bondwire inductance for $AVSS\_IN\_PRI$, $AVSS\_ACTIVE$ and $AVSS\_OUT\_SEC$ becomes *1.5 nH/9*, *1.5 nH/9* and *1.5 nH/4*, respectively.

[1]Since it is parallel connection and assuming all bondwire inductance are equal.

All the pads except $OUT$ pad and $AVSS\_OUT\_SEC$ pads have electrostatic diodes (ESD) and these are taken from ELCA[2] inventory. These pads have a capacitance of $C_{PAD}$ = *0.7 pF*. The electrostatic diodes (ESD) are removed for the $OUT$ pad (highlighted with a purple rectangle in Figure 8.11) since the balun provides isolation to the active devices. Moreover, adding ESD reduces the linearity since it contains a significant amount of nonlinear capacitance. The pad capacitance for $OUT$ was simulated in $MoM$ and the value was calculated to be *0.3 pF*.

Below sections shows the results with schematics portrayed in Figure 9.1 for temperatures $-40°C$, $27°C$, $70°C$ and $125°C$.

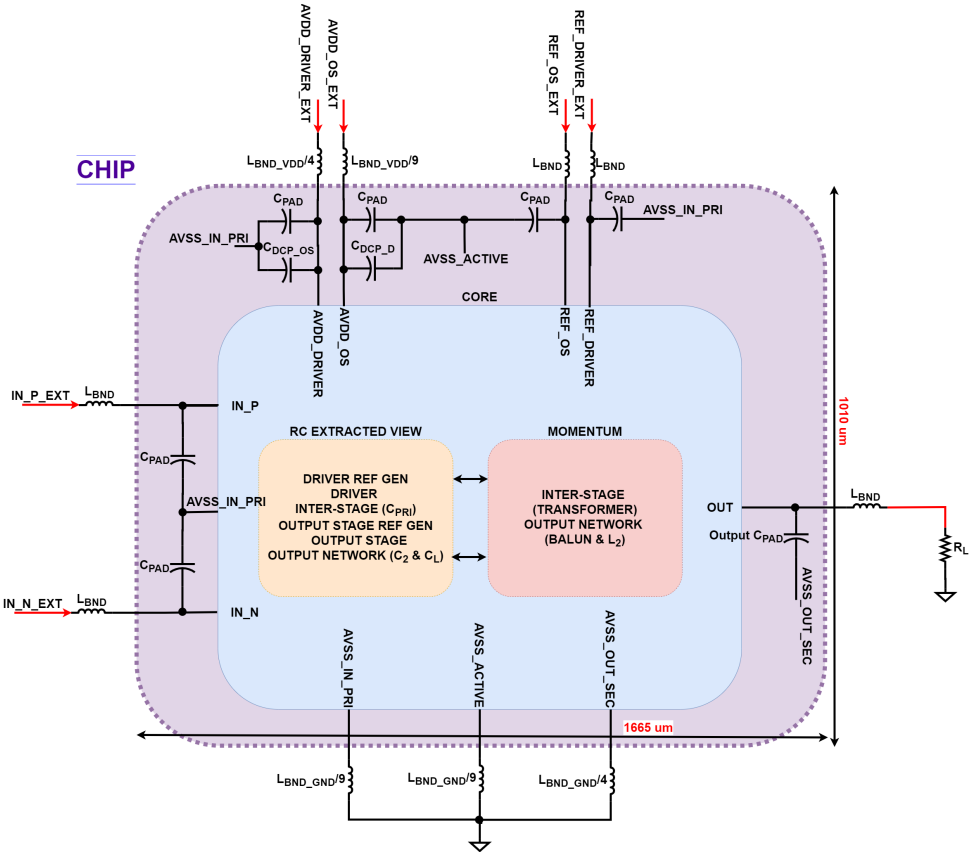



**Figure 9.1:** Schematics consisting of core design, decoupling capacitor ($C_{DCP}$), bondwire inductance ($L_{BND}$) and pad capacitance ($C_{PAD}$) to model the entire chip

[2]Electronic Circuits and Architectures (ELCA), a research group in TU Delft

## 9.1. Peak power and output 1 dB compression point

The input power was swept from *-30 dBm to 2 dBm* in the harmonic balance test (considering *15* harmonics) for different temperatures. From Figure 9.2 and 9.3, it seen that peak $P_{\text{OUT}}$ and $OP1dB$ increases at lower temperature. The reason is that at lower temperature both mobility and threshold voltage decreases with temperature. But decrease in mobility means lesser drain current ($I_D$) and lower power, whereas decrease in threshold voltage signifies increase in $I_D$ and higher power. In this case, threshold voltage dominates the $I_D$ so there is increase in $P_{\text{OUT}}$ and $OP1dB$ at lower temperatures.

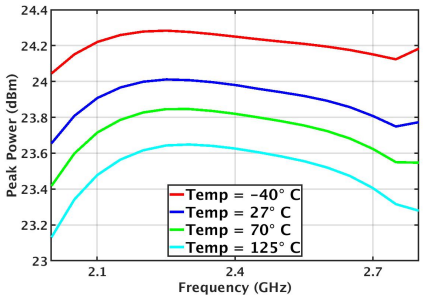



**Figure 9.2:** Peak power ($P_{\text{OUT}}$) across frequency for different temperature

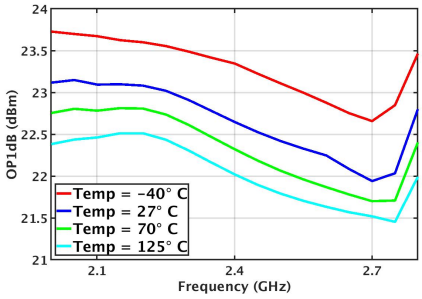



**Figure 9.3:** Output 1 dB compression point ($OP1dB$) across frequency for different temperatures

## 9.2. PA efficiency

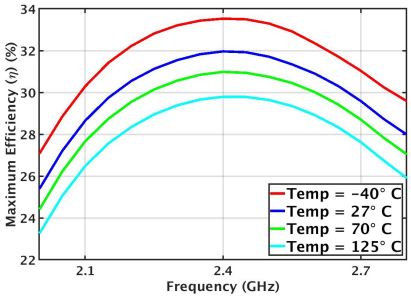



**Figure 9.4:** Maximum efficiency ($\eta$) of the system

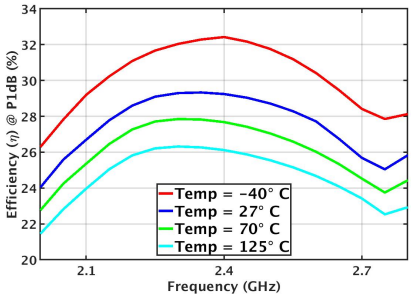



**Figure 9.5:** Efficiency ($\eta$) of the system at P1dB

The system here refers to the entire PA which consists of the driver, inter-stage matching, output stage and output network. Figure 9.4 and 9.5 shows the $\eta$ of the system at maximum and P1dB whereas, $\eta$ at $P_{\text{OUT}}$ = *18 dBm* and *16.5 dBm* is plotted in Figure 9.6 and 9.7 respectively. From the figures, it is seen that $\eta$ increases as the temperature reduces. The reasoning for this is same as the one explained for

the increase in $P_{OUT}$ at lower temperatures.

Across the frequency, $\eta$ is maximum at *2.4 GHz* because the PA operates in Class F condition. Theoretically, CCF has constant $\eta_D$ over the entire bandwidth and is independent of $\gamma$ (refer chapter 2). In reality, change in $V_{DS}$ will have an impact on $I_D$ and also on $\eta_D$. So, in practical scenario, $\eta_D$ reduces with increase in $\gamma$.

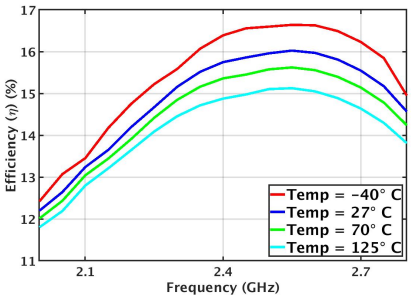



**Figure 9.6:** Efficiency ($\eta$) of the system at $P_{OUT}$ = *18 dBm*

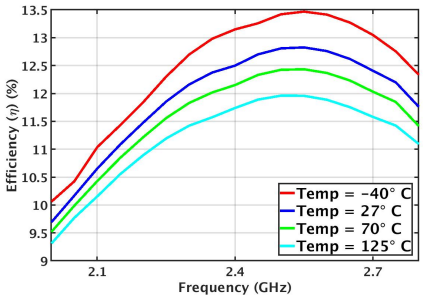



**Figure 9.7:** Efficiency ($\eta$) of the system at $P_{OUT}$ = *16.5 dBm*

## 9.3. Voltage gain

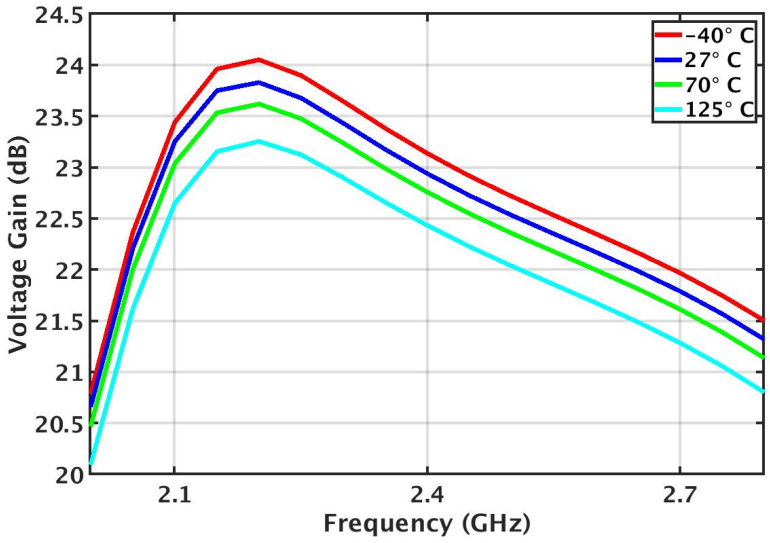



**Figure 9.8:** Voltage gain of the system over frequency for different temperatures

Figure 9.8 shows the voltage gain ($G_V$) of the system across frequency for different temperatures. There is a variation of about *1 dB* in the $G_V$ in the bandwidth *2.1 - 2.7 GHz*. As the temperature reduces, threshold voltage reduces and $P_{OUT}$

increases as explained earlier. Thus, leading to increase in the $G_V$ of the system. At *2.4 GHz*, the driver and output stage has $G_V$ of *11 dB* and *15 dB*, respectively. On the other hand, inter-stage and output network has $G_V$ of *-2.6 dB* and *0.9 dB*, respectively.

## 9.4. Drain efficiency

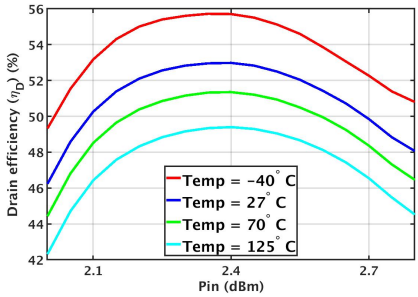



**Figure 9.9:** Maximum drain efficiency ($\eta_D$) of the output stage

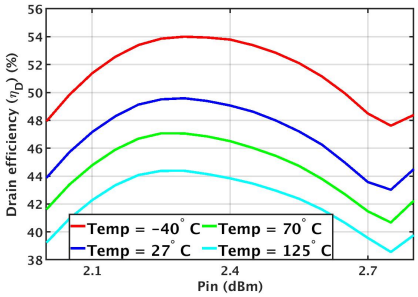



**Figure 9.10:** Drain efficiency ($\eta_D$) of the output stage at P1dB

The drain efficiency ($\eta_D$) of the output stage at peak and P1dB is plotted in Figure 9.9 and 9.10, respectively. It is seen that maximum $\eta_D$ at 125°C is *49%* where as the maximum system $\eta$ at 125°C is only *30%*. This loss can be attributed to the passive efficiency of the output balun.

For the output balun, quality factor of primary ($Q_P$) and secondary ($Q_S$) coils are measured as *12.8* and *11.5* respectively at *2.4 GHz*. The coupling factor ($km$) is designed to be *0.69* in the output balun. Using the following variables, passive efficiency ($\eta_{P\_OS}$) of the output balun at *2.4 GHz* can be computed with equation described in [4].

$$\eta_{P\_OS} = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_P Q_S km^2}\right)\frac{1}{Q_P Q_S km^2} + \frac{2}{Q_P Q_S km^2}}} = 78.5\ \% \qquad (9.1)$$

But, the above equation holds for the following conditions:

- $L_P \cong \frac{L_S}{n^2}$;
- for the optimum value of $C_L$ given by $\frac{1}{\omega C_L} = \omega L_S$;
- for the optimum inductance which is given by $\omega L_P = \frac{R_L}{n^2\sqrt{\frac{1}{Q_S^2} + \frac{Q_P}{Q_S}\cdot km^2}}$ [4].

For $R_L$ = *50* Ω and $\omega$ = *2π*2.4e9*

$$\Longrightarrow L_P = 4.1\ nH$$

The transformer efficiency is reduced when the inductance value is above or below the optimum value determined previously. Since $L_P$ is lower than optimum value, $\eta_{P\_OS}$ is around *60%*.

The quality factor of the primary ($Q_{P\_IS}$) and secondary ($Q_{S\_IS}$) coils in the inter-stage transformer is measured as *6.9* and *5* respectively. By design, transformer coupling $km_{IS}$ of the inter-stage is *0.35* so that matching is achieved across the entire bandwidth (*2.1 - 2.7 GHz*) using double tuned transformer concept. Similarly, passive efficiency ($\eta_{P\_IS}$) of the transformer in the inter-stage is also calculated using the above Equation 9.1.

$$\eta_{P\_IS} = 39\ \%$$

From Equation 9.1, it is seen that low coupling factor ($km$) reduces passive efficiency. But the efficiency of PA is dominated by the output stage. So, loss in the transformer efficiency at the inter-stage matching doesn't matter much.

## 9.5. QAM results

To test linearity and calculate EVM, *64* quadrature amplitude modulation (QAM) and *16* QAM signals with bandwidth of *40 MHz* were created in MATLAB and fed to the circuit (Figure 9.1).

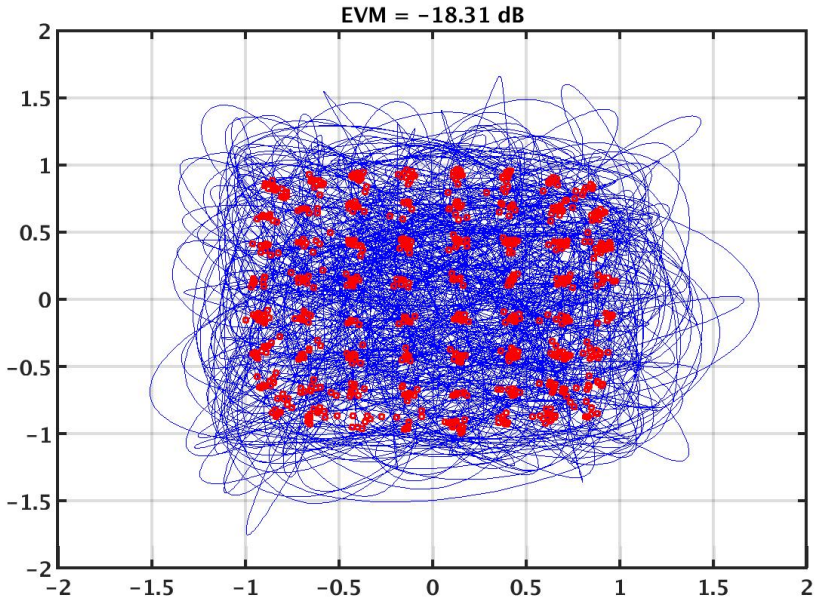



**Figure 9.11:** Constellation diagram for *64* QAM signal with *40 MHz* bandwidth at *2.4 GHz* (maximum power)

The test was conducted at full power, *3 dB* back off and *6 dB* back off for *16*

QAM signal[3] with *40 MHz* bandwidth to calculate the EVM at the same power levels. The constellation diagrams and output spectrum for full power and back off cases at *2.1 GHz* and *2.7 GHz* are available in Appendix D.

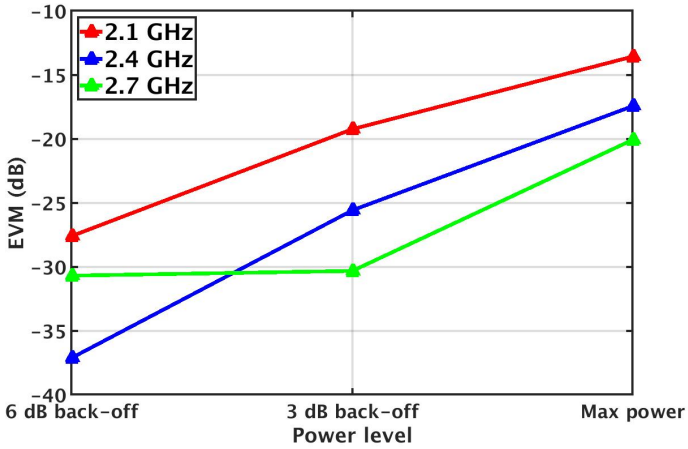



**Figure 9.12:** EVM calculated for *16* QAM signal with *40 MHz* bandwidth at maximum power, *3 dB* back off and *6 dB* back off for *2.1 GHz*, *2.4 GHz* and *2.7 GHz*

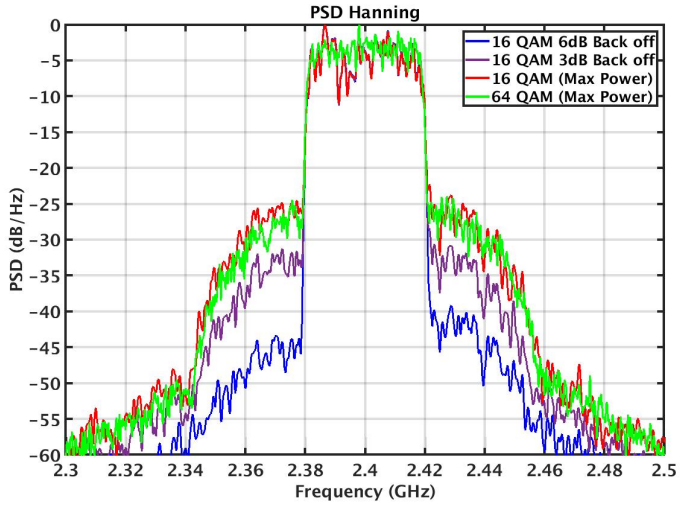


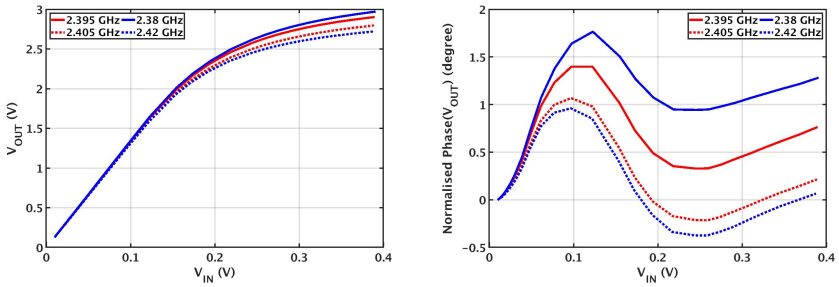

**Figure 9.13:** Output spectrum for *64* QAM signal (maximum power) and *16* QAM signal at *2.4 GHz* (maximum power, *3 dB* back off and *6 dB* back off)

[3] *64* QAM signal simulation takes long duration that's why *16* QAM signals are used for simulating back off cases

As seen in Figure 9.13, at *6 dB* back off, left and right side of the spectrum is not even. This is because memory effect is dominant than non-linearity and it leads to amplitude variation of IM products with frequency. The memory effect is mainly due to the biasing and matching network. It can be prevented by feedback mechanism which is explained in [5], but it is computation intensive. Another technique is to shunt envelope signal which is main contributor for memory effect and linearity [6].

## 9.6. Two-tone test

Two-tones with spacing of *10 MHz* and *40 MHz* at *2.1 GHz*, *2.4 GHz* and *2.7 GHz* were applied to the circuit (refer Figure 9.1). The dotted and solid lines in Figure 9.14 refers to *40 MHz* and *10 MHz* tone spacing respectively. This simulation was carried out to find which contributes significantly to EVM and ACLR degradation. Figure 9.14, Figure D.15, and Figure D.16 showcases AM-AM and AM-PM[4] for *2.4 GHz*, *2.1 GHz* and *2.7 GHz* with input voltage on x axis.




**(a)** AM-AM plot **(b)** AM-PM plot

**Figure 9.14:** AM-AM and AM-PM for *2.4 GHz* with input voltage on x axis

## 9.7. Performance comparison with State-of-the-Art

The performance of the CCF PA is compared with State-of-the-Art PA at 2.4G-Band in Table 9.1. The main highlight of this design is that it maintains the performance (peak power, output P1dB, efficiency and EVM) over a wide bandwidth *2.1 - 2.7 GHz* (*25%*). Compared to the digital PAs, the proposed design doesn't have digital predistortion or integrated T/R switch. Even though, maximum efficiency is not better than the State-of-the-Art, efficiency at $P_{OUT}$ = *18 dBm* and EVM is comparatively good. One of the main drawback of the proposed design is the chip area. Similarly, peak power and OP1dB for the designs in [7] and [8] is higher because the designs have used parallel combined transistors or more than one amplifier.

[4] y axis shows normalised phase that is phase is subtracted from the starting phase so that it starts from *0*.

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[1] D. Mühlhaus, *Effect of ground cutout size on rfic inductor performance,* (Accessed 6 August 2020).

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| Reference | ***This work*[1]** | MTT [7] | ISSCC'16 [9] | ISSCC'16 [10] | CICC'15 [11] | MWCL'15 [8] |
|---|---|---|---|---|---|---|
| Technology | ***40 nm CMOS*** | 40 nm CMOS | 40 nm CMOS | 28 nm CMOS | 55 nm CMOS | 40 nm CMOS |
| Support WiFi standard | ***11n*** | 11abgn/ac | 11 abg/n | 11 abg/n | 11 abgn/ac | 11g |
| Bandwidth | ***2.1 - 2.7 GHz*** | 2.4 - 2.5 / 4.9 - 5.9 GHz | 2.4 / 5.5 GHz | 2.45 / 5.5 GHz | 2.4 / 5 GHz | 2.4 GHz |
| PA Topology | ***Analog PA*** | Analog PA | Digital PA | Digital PA | Analog PA | Analog PA |
| Class of Operation | ***CCF*** | Parallel combined transistors. One of the transistor is biased at A and other at B | NA | NA | Class AB | Main amplifier with class AB bias and an auxiliary amplifier with class C bias |
| Digital pre-distortion | ***No*** | No | Yes | Yes | Yes | No |
| Integrated external PA Driver | ***Yes*** | Yes | No | No | No | Yes |
| Integrated T/R switch | ***No*** | No | Yes | Yes | Yes | No |
| Area | ***1.4*** $mm^2$ | 0.27 $mm^2$ | 0.3 $mm^2$ (TX area) and off chip balun | NA | 2.1 $mm^2$ | 0.54 $mm^2$ |
| Peak Power (dBm) | ***23.5 dBm @ 2.1 GHz*** ***23.6 dBm @ 2.4 GHz*** ***23.4 dBm @ 2.7 GHz*** | 27* | 27* | 27.8* | 23* | NA |
| Output P1dB (dBm) | ***22.5 dBm @ 2.1 GHz*** ***22 dBm @ 2.4 GHz*** ***21.5 dBm @ 2.7 GHz*** | 27* | NA | NA | NA | 24.6 |
| PAE (%) | ***Max Eff at 2.1, 2.4 & 2.7 GHz are 26.5%, 29.82% & 27.9%*** ***Eff @ Pout = 18 dBm at 2.1, 2.4*** & ***2.7 GHz are 12.7%,14.84% & 14.6%*** | Peak PAE - 40% 15% PAE @ EVM = -25 dB for 2.45 GHz 11 ac mcs8* | DPA Efficiency 14.5% @ 8 dB-backoff | Peak PAE - 22% 15% PAE @ EVM = -25 dB for 2.447 GHz 11n40* | 10.5% PAE at 2.45 @ EVM = -32 dB* | Peak drain efficiency - 38% 14% PAE @ EVM = -25 dB for 2.45 GHz with WLAN 802.11g 54 mbps 64-QAM OFDM signal |
| Gain (dB) | ***25.7*** | 25* | NA | NA | NA | 37 |
| EVM | ***-27.6 dB @ 2.1 GHz 6 dB-backoff*** ***-25 dB @ 2.4 GHz 3 dB-backoff*** ***-30.3 dB @ 2.7 GHz 3 dB-backoff*** ***(with 16 QAM 40 MHz signal)*** | -25 dB @ Pout = 22 dBm at 2.45 GHz 20 MHz BW 11n mcs7* | -25 dB @ Pout = 20 dBm at 2.4 Ghz H740 mcs7* | -25 dB @ Pout = 22 dBm at 2.447 GHz 11n40* | -32 dB @ Pout = 17.5 dBm at 2.45 GHz 11n mcs7 20MHz* | -25 dB @ Pout = 18.5 dBm at 2.445 GHz WLAN 802.11g 54 mbps 64-QAM OFDM signal BW = 20 MHz* |

[1] From simulation.
* Graphically estimated.

**Table 9.1:** Performance comparison with State-of-the-Art *2.4*G-Band WLAN CMOS PAs

# 10

# Conclusion

In this thesis, CMOS CCF PA is designed successfully without compromising the linearity and also satisfying the larger bandwidth and efficiency requirements. The PA was developed for **WiFi 802.11n** and LTE, thus making it a multipurpose PA. This PA consist of four basic building blocks: the driver, inter-stage matching, output stage and output network.

The design of the output network was explained in chapter 3 and *Design A* (no RF choke and with $L_2C_2$) was chosen because it had flatter real part at the first harmonic and lower number of components. Even though performance degraded a bit, the coupling factor ($km$) for the output balun was chosen as *0.69* (*Design II*) to reduce $L_P$ and $L_S$ and make it layout friendly.

The output stage consists of *3* transistors (*2* nominal devices and *1* thick oxide device) which uses the concept of stacked transistors to overcome the breakdown voltage issue (refer chapter 4). Further, the driver cell was added to increase the voltage gain of the PA without reducing the linearity. It is a simple cascode structure that operates in Class AB and the design is explained in chapter 5.

Using the double tuned transformer, the inter-stage achieved the required matching over the bandwidth *2.1 - 2.7 GHz* (refer chapter 6). Further, chapter 8 portrayed the layout of the CCF chip and also shed light on the layout techniques used to improve the performance. From the post layout simulation chapter (chapter 9), it is seen that the entire design of PA is very promising. It has wider bandwidth (*25%*) than the State-of-the-Art PAs. It also has an EVM of *-25 dB* for a *16* QAM *40 MHz* signal centered at *2.4 GHz* at *3 dB* back-off which excels most of the State-of-the-Art PAs.

## 10.1. Future work

The tape out of the chip is planned in *March 2021*. So, the next task is to design the PCB board so that the CCF chip can be tested and validated against the simulation results. Finally, this is the first chip that uses the concept of CCF across the

bandwidth *2.1 - 2.7 GHz*.

Few recommendations where the future research can be focused so as to improve the performance of CCF PAs. Firstly, the chip size of $1.4\,mm^2$ is considerably large to be integrated in a WiFi chip. So, if the results for efficiency and linearity are matching with the simulation, then the future work will be primarily focused on reducing the area of output network since it occupies the largest area in the chip. Secondly, power combining techniques such as distributed active transformer could be employed to reach higher power and efficiency. Thirdly, EVM and linearity at lower power is dominated by the memory effect. So to reduce the memory effect, negative feedback or shunting the envelope signal can be employed. Since $C_L$ value is important for the response of the output network, it can be replaced with capacitor banks so that tuning can be done after the chip is fabricated. But the trade off is the losses in the switch and linearity. Finally, the output network is heavily dependent on the notion that the output of PA is always loaded with an ideal and fixed 50 $\Omega$ resistor which resembles the impedance of an ideal antenna. But, this isn't the case in reality. So, to counter this, one method is to have antenna tuning circuitry.

# A

# Calculation of drain source capacitance ($C_{DS}$) of the top transistor

This chapter explains the procedure to calculate $C_{DS}$ of top most transistor (thick oxide device) in a stack. The $C_{DS}$ of the top most transistor in the output stage is used in chapter 3 for designing output networks. Whereas, the $C_{DS}$ of the top most transistor in the driver is utilized in chapter 6 for designing inter-stage matching.

## A.1. $C_{DS}$ of thick oxide device in the output stage

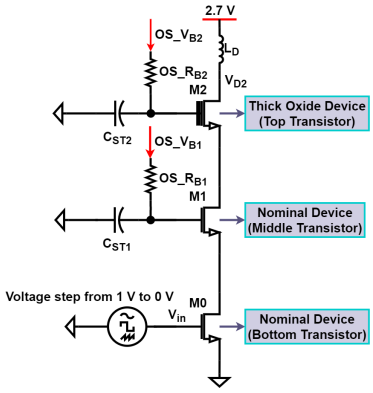



**Figure A.1:** Schematics to calculate $C_{DS}$ of the top most transistor in the output stage

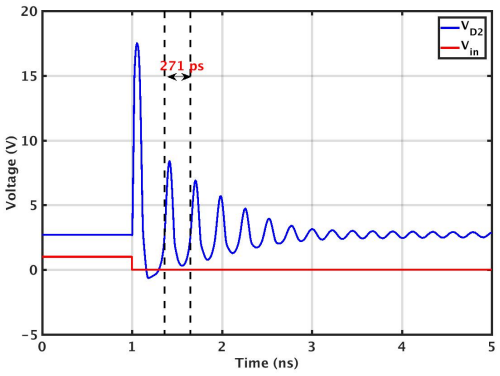



**Figure A.2:** Plot showing step input at the gate of the bottom transistor and oscillation at the drain of top transistor

A

When a pulse is given at the gate of bottom transistor, there will be oscillation at the drain of the top transistor. The frequency of oscillation will be given by the capacitor $C_{DS}$ and inductor $L_D$ (*1 nH*) connected at the drain of the top transistor (See Figure A.1). Also, frequency can be calculated from time period which is marked in Figure A.2.

$$\begin{aligned} T &= 271.4 * 10^{-12} \\ \omega &= \frac{2\pi}{T} = 2.32 * 10^{10} \\ C &= \frac{1}{\omega^2 * 1 * 10^{-9}} = 1.87\ pF \end{aligned} \tag{A.1}$$

On the other hand, $C_{DS}$ value obtained from parameters of the transistor is *0.71 pF*. This value isn't right since it is obtained from only small signal analysis.

## A.2. $C_{DS}$ of thick oxide device in the driver

The $C_{DS}$ of the top most transistor in the driver is calculated identical to that done in the previous section.

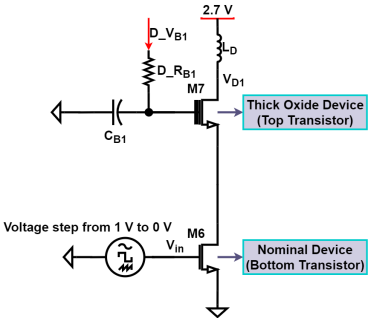



**Figure A.3:** Schematics to calculate $C_{DS}$ of the top most transistor in the driver

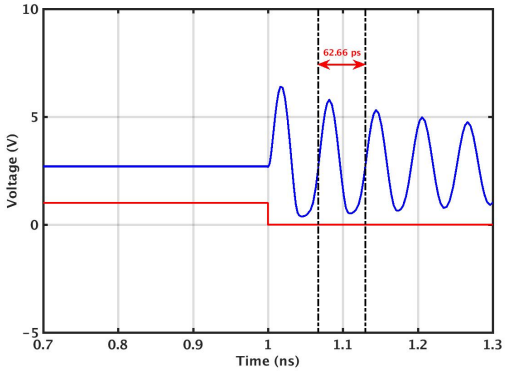



**Figure A.4:** Plot showing step input at the gate of the bottom transistor and oscillation at the drain of top transistor

$$\begin{aligned} T &= 62.66 * 10^{-12} \\ \omega &= \frac{2\pi}{T} = 10 * 10^{10} \\ C &= \frac{1}{\omega^2 * 1 * 10^{-9}} = 99.5\ fF \end{aligned} \tag{A.2}$$

# B

# Biasing for the driver and output stage

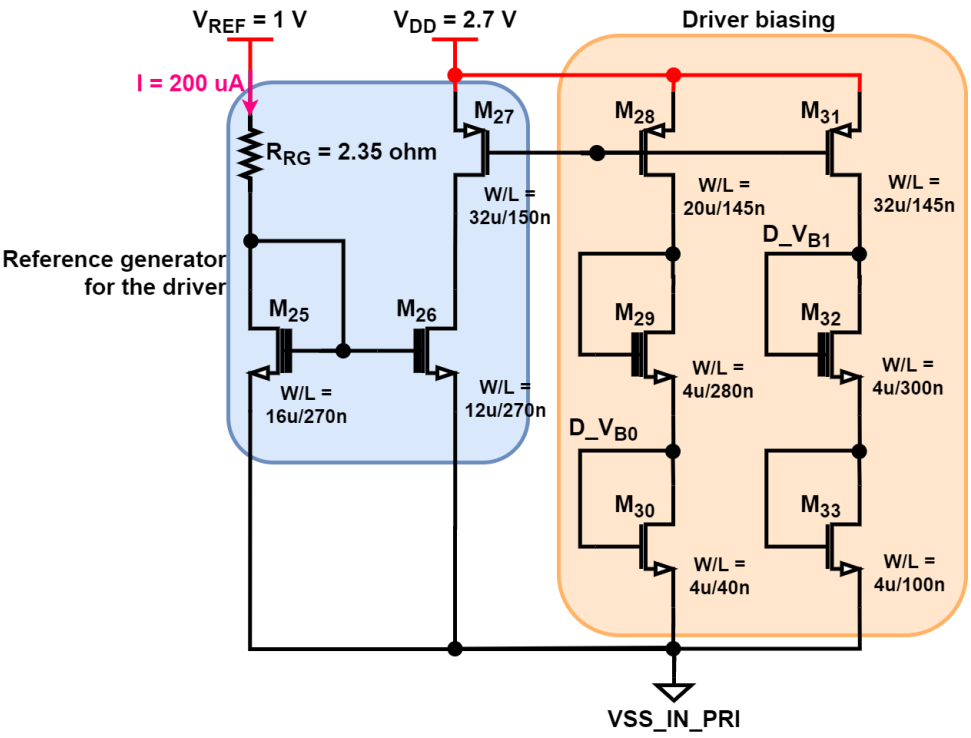



**Figure B.1:** Biasing unit for the driver

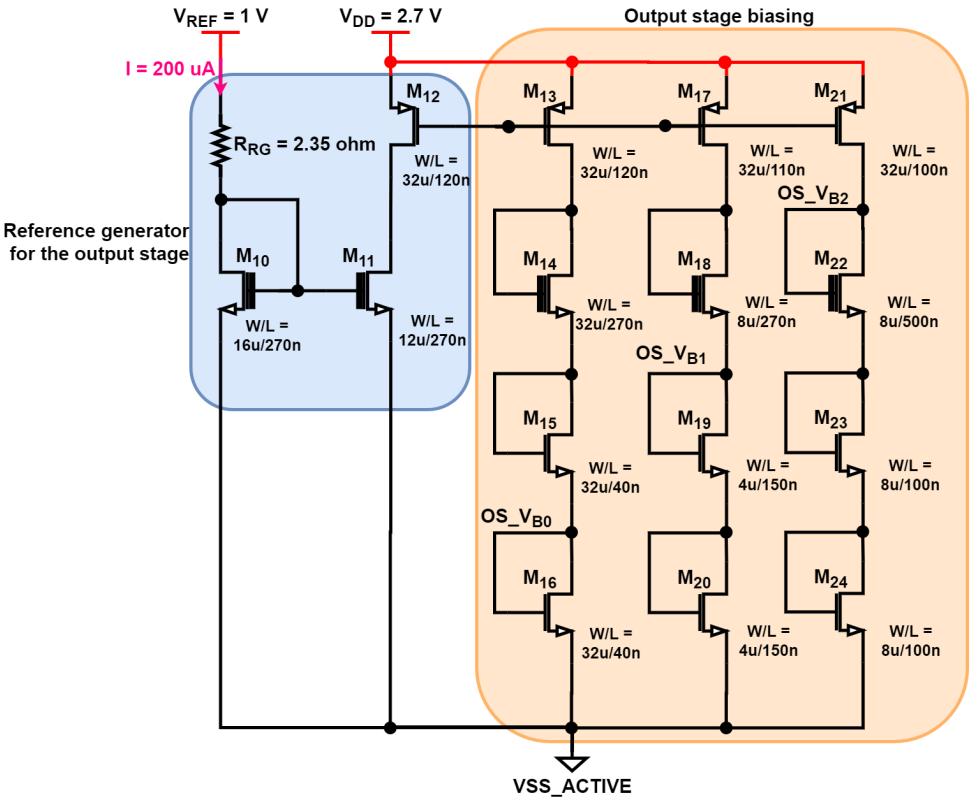



**Figure B.2:** Biasing unit for the output stage

# C

# Schematics results II

## C.1. Efficiency versus $R_{DNW}$

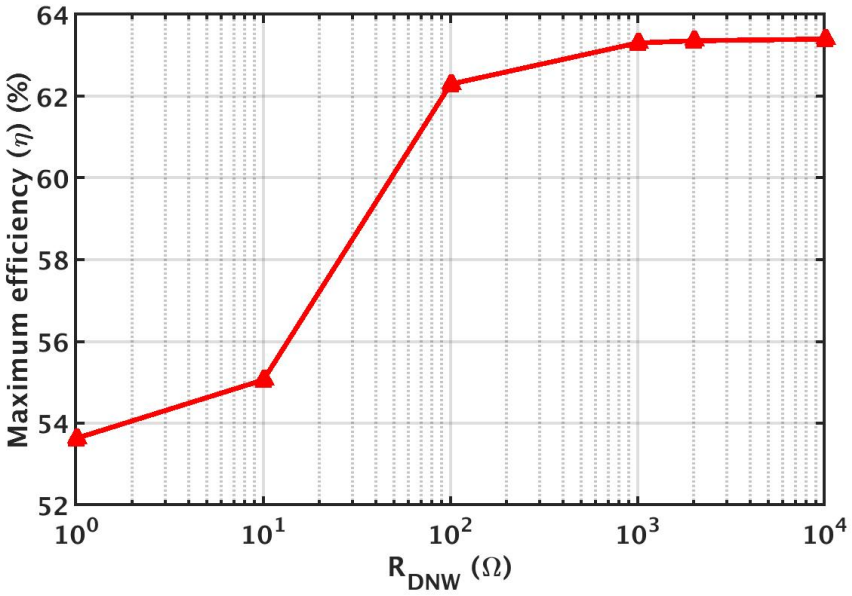



**Figure C.1:** Maximum efficiency of the system versus $R_{DNW}$

## C.2. Voltage and current waveforms at the drain of the top transistor ($M_2$)

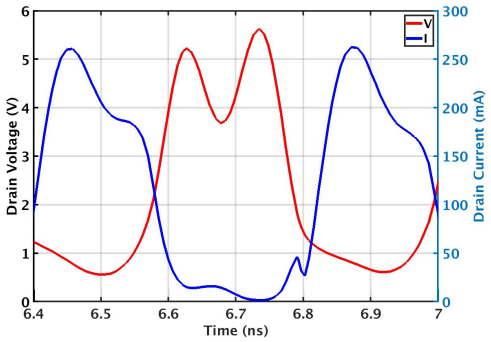



**Figure C.2:** Voltage and current waveforms at the drain of $M_2$ at *2.4 GHz*

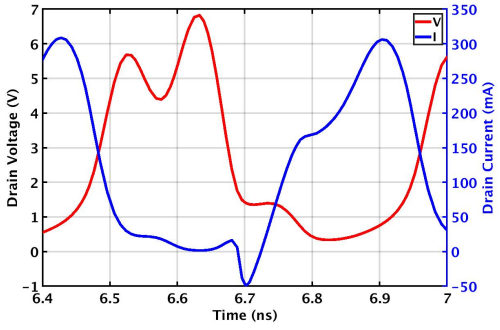



**Figure C.3:** Voltage and current waveforms at the drain of $M_2$ at *2.1 GHz*

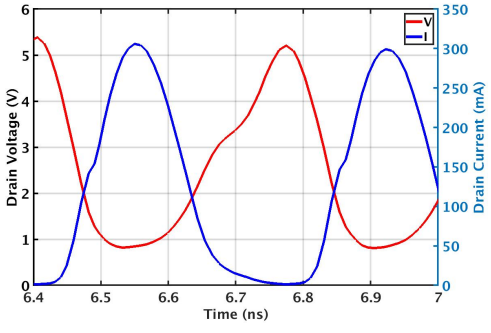



**Figure C.4:** Voltage and current waveforms at the drain of $M_2$ at *2.7 GHz*

# D

# Post layout simulation results II

## D.1. QAM results

### D.1.1. Frequency = 2.4 GHz

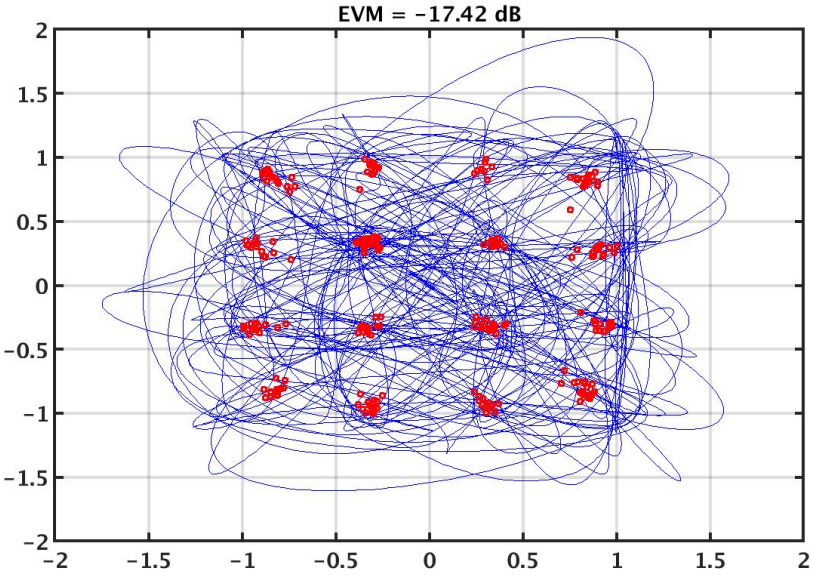



**Figure D.1:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.4 GHz* (maximum power)

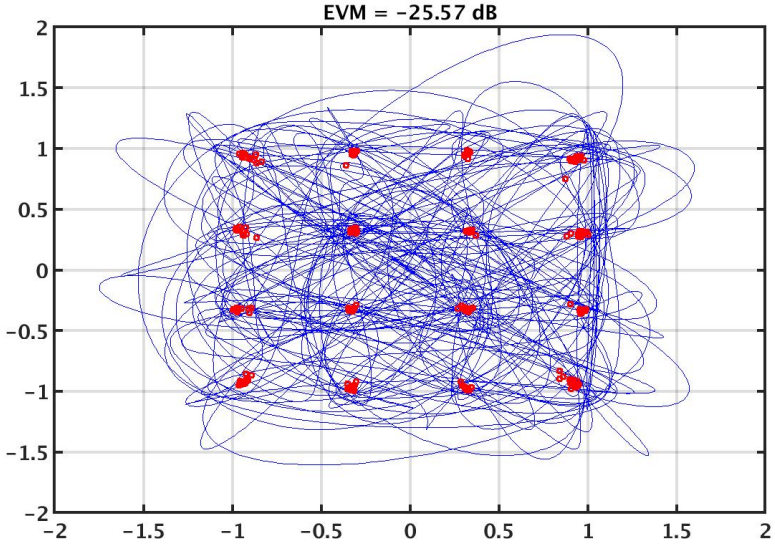



**Figure D.2:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.4 GHz* (*3 dB* backoff)

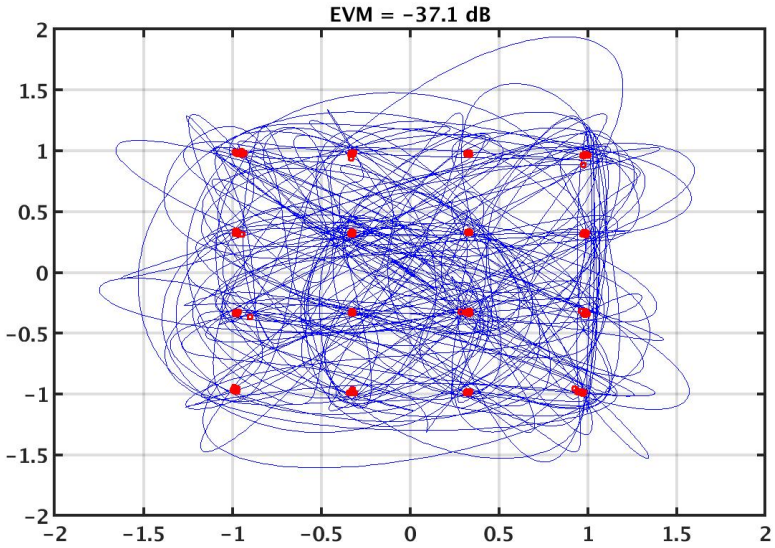



**Figure D.3:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.4 GHz* (*6 dB* back off)

### D.1.2. Frequency = 2.1 GHz

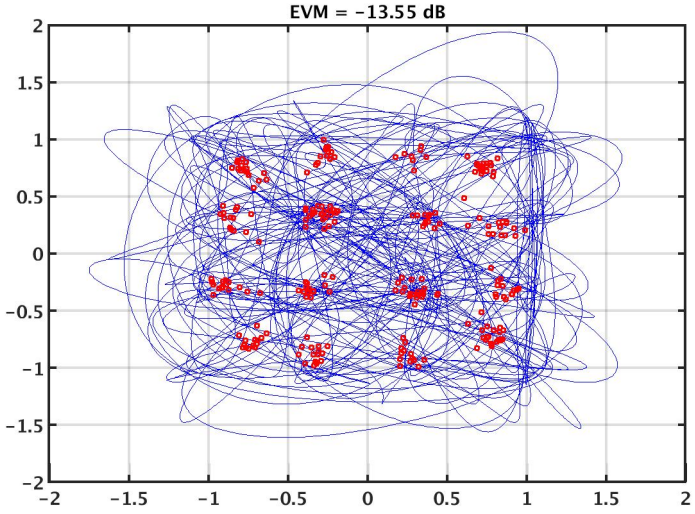



**Figure D.4:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.1 GHz* (maximum power)

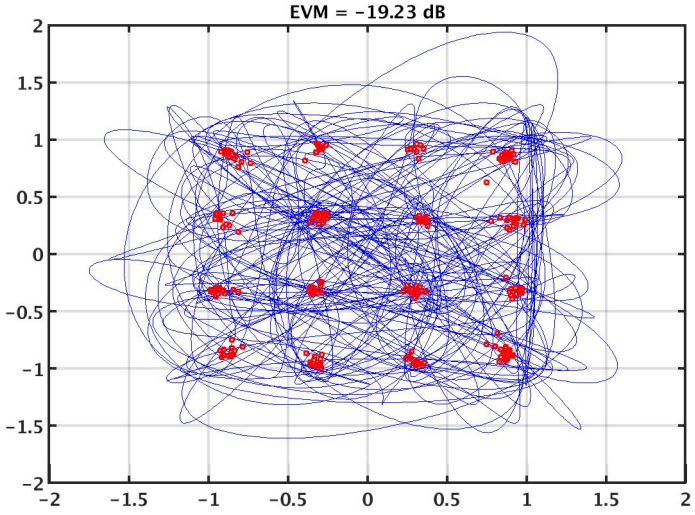



**Figure D.5:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.1 GHz* (*3 dB* backoff)

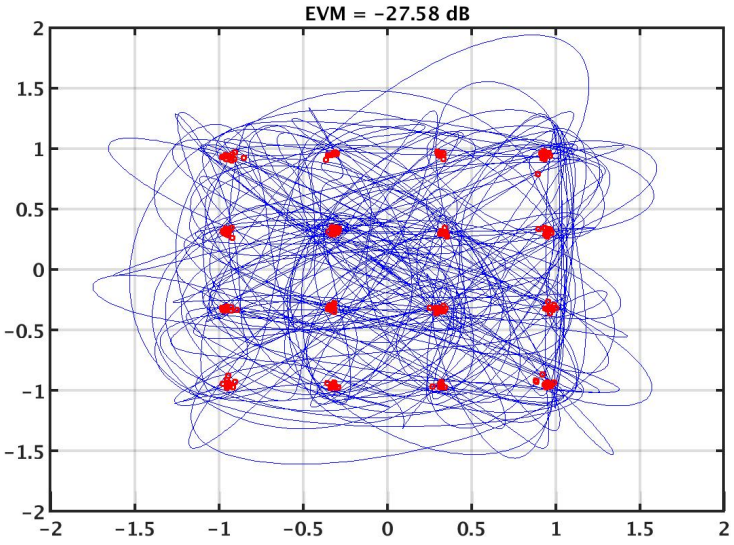



**Figure D.6:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.1 GHz* (*6 dB* back off)

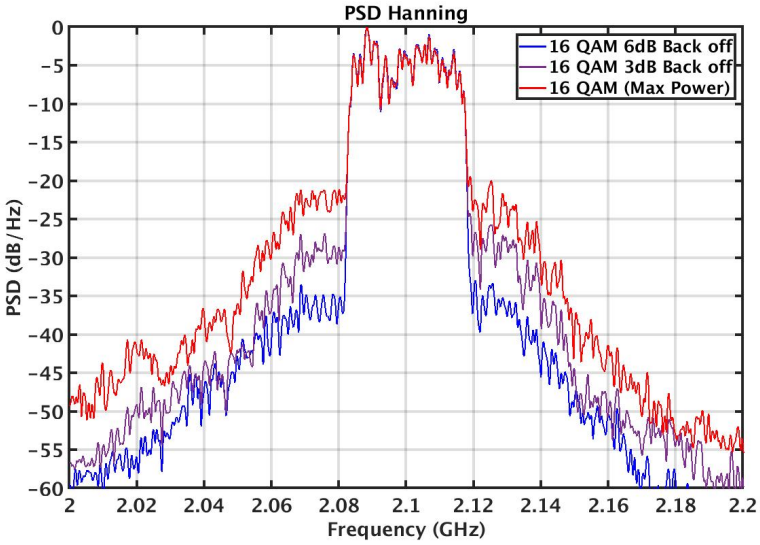



**Figure D.7:** Output spectrum for *16* QAM signal at *2.1 GHz* (maximum power, *3 dB* back off and *6 dB* back off)

### D.1.3. Frequency = 2.7 GHz

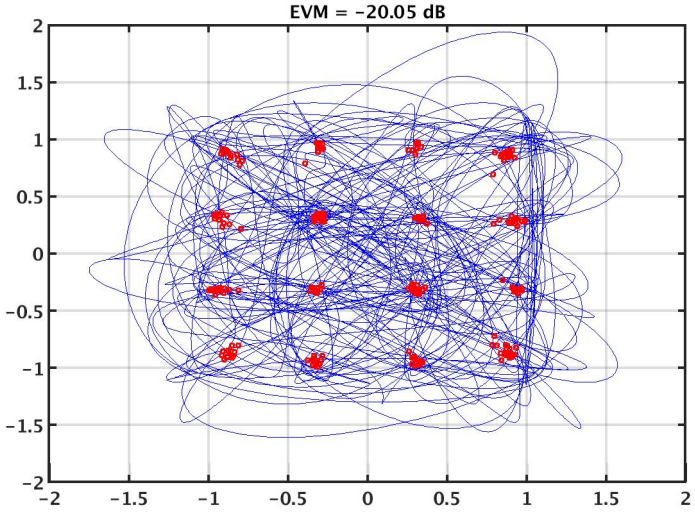



**Figure D.8:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.7 GHz* (maximum power)

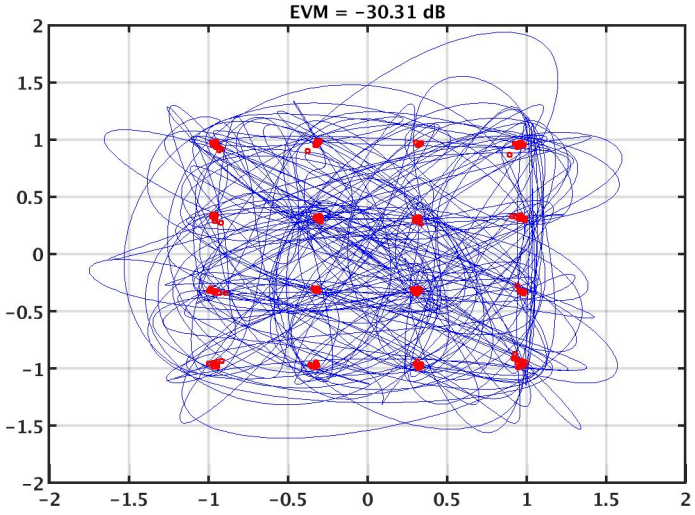



**Figure D.9:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.7 GHz* (*3 dB* backoff)

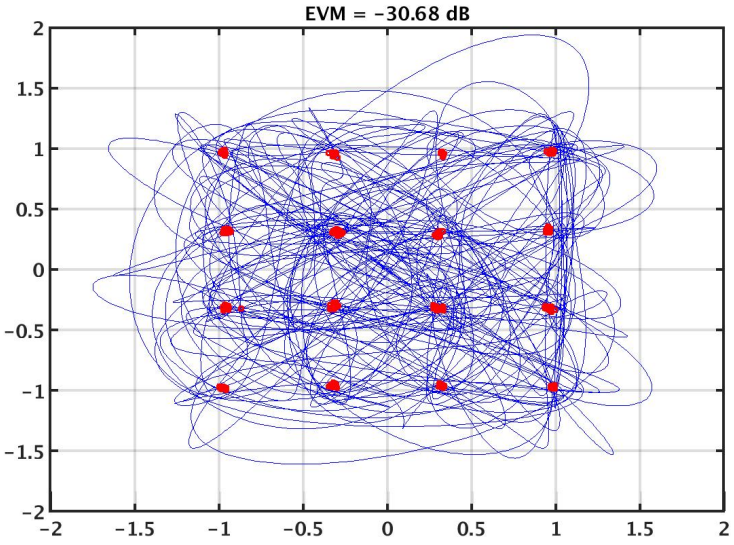



**Figure D.10:** Constellation diagram for *16* QAM signal with *40 MHz* bandwidth at *2.7 GHz* (*6 dB* back off)

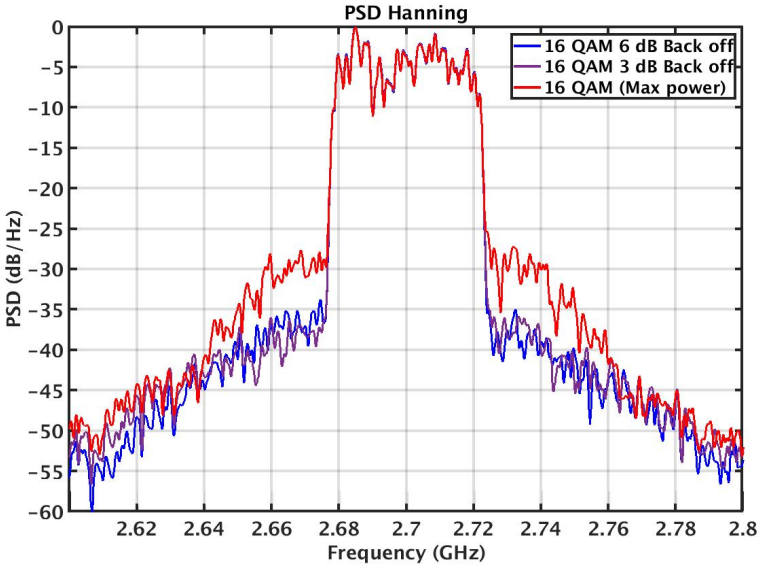
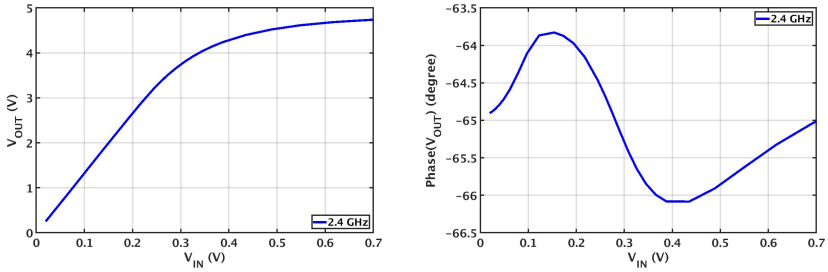



**Figure D.11:** Output spectrum for *16* QAM signal at *2.7 GHz* (maximum power, *3 dB* back off and *6 dB* back off)

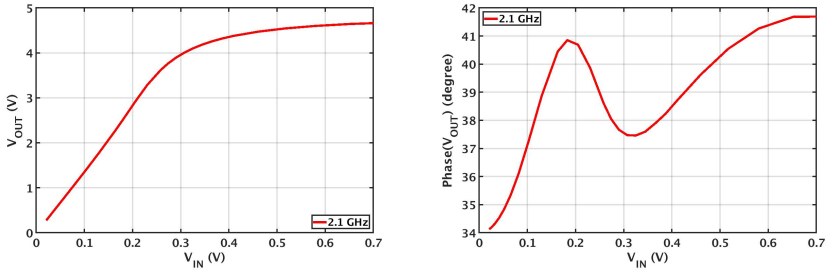
## D.2. Single-tone test

Single tone at *2.1 GHz*, *2.4 GHz* and *2.7 GHz* were fed into circuit (Figure 9.1) and input power was swept from *-30 dBm* to *2 dBm* to plot AM-AM and AM-PM for above-mentioned frequencies.



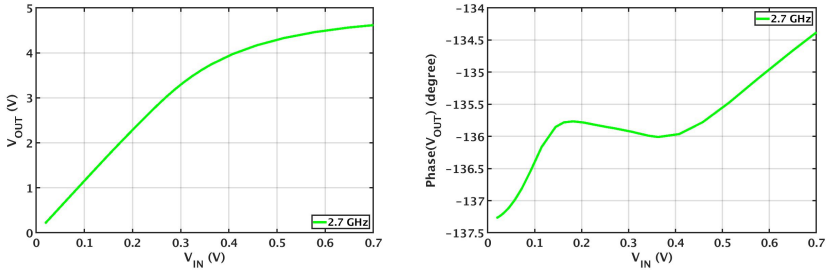

**(a)** AM-AM plot **(b)** AM-PM plot

**Figure D.12:** AM-AM and AM-PM for *2.4 GHz*




**(a)** AM-AM plot **(b)** AM-PM plot

**Figure D.13:** AM-AM and AM-PM for *2.1 GHz*

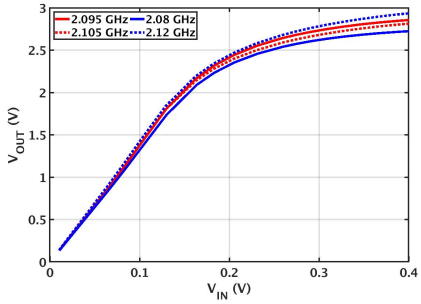



**(a)** AM-AM plot **(b)** AM-PM plot

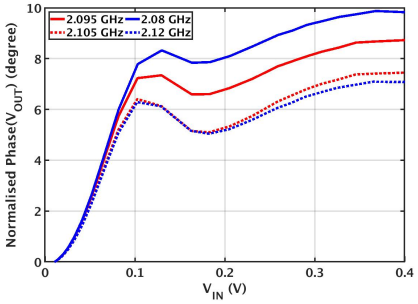
**Figure D.14:** AM-AM and AM-PM for *2.7 GHz*

## D.3. Two-tone test

### D.3.1. Harmonic balance simulation

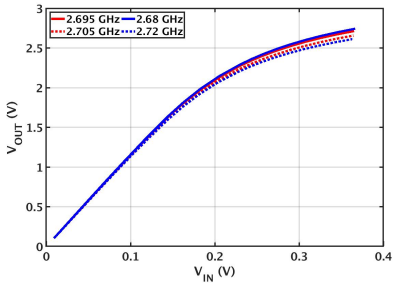



**(a)** AM-AM plot

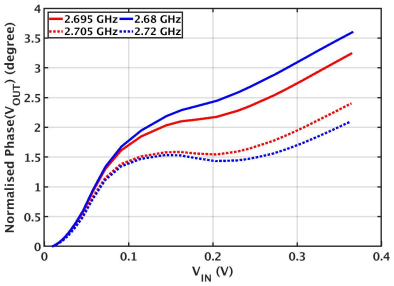



**(b)** AM-PM plot

**Figure D.15:** AM-AM and AM-PM for *2.1 GHz* with input voltage on x axis

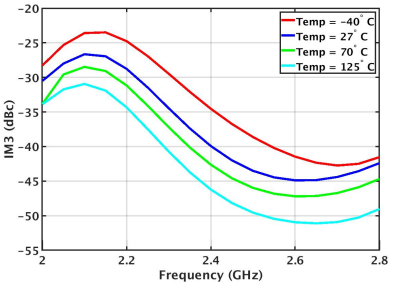



**(a)** AM-AM plot

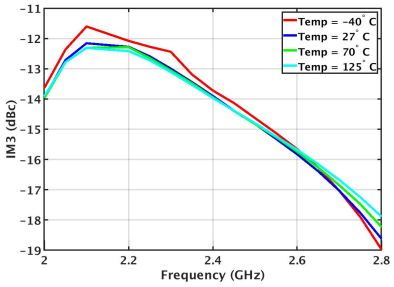



**(b)** AM-PM plot

**Figure D.16:** AM-AM and AM-PM for *2.7 GHz* with input voltage on x axis




**(a)** IM3 for Pin = *-20 dBm*

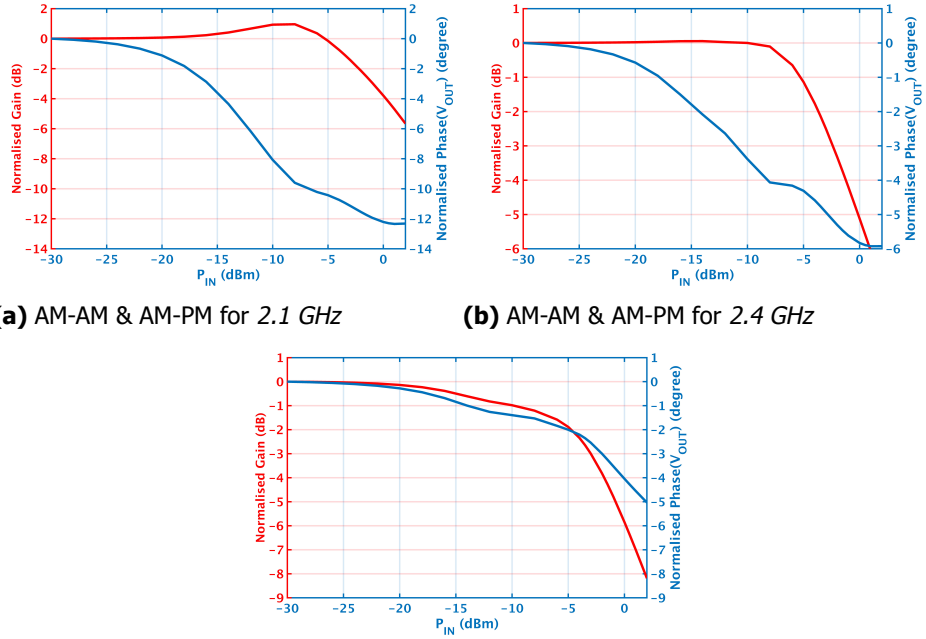



**(b)** IM3 for Pin = *-5 dBm*

**Figure D.17:** IM3 across frequency for different temperatures

### D.3.2. Transient simulation

Two-tones with spacing of *40 MHz* at *2.1 GHz*, *2.4 GHz* and *2.7 GHz* were applied to the circuit (refer Figure 9.1) and transient simulation was conducted to capture AM-AM and AM-PM.




**(a)** AM-AM & AM-PM for *2.1 GHz*

**(b)** AM-AM & AM-PM for *2.4 GHz*

**(c)** AM-AM & AM-PM for *2.7 GHz*

**Figure D.18:** AM-AM and AM-PM plots for *2.1 GHz*, *2.4 GHz*, and *2.7 GHz* with input power on x axis

## D.4. Noise

The noise was simulated using pss and pnoise in cadence with beat frequency of *2.4 GHz*. The main contributors for the integrated noise in the bandwidth *2.38 GHz - 2.42 GHz* is shown in Figure D.20. The main noise contributor is the flicker noise of the thick oxide device used in the reference generators of the driver and output stage for mirroring current. This can be reduced by using PMOS instead of NMOS for current mirroring.

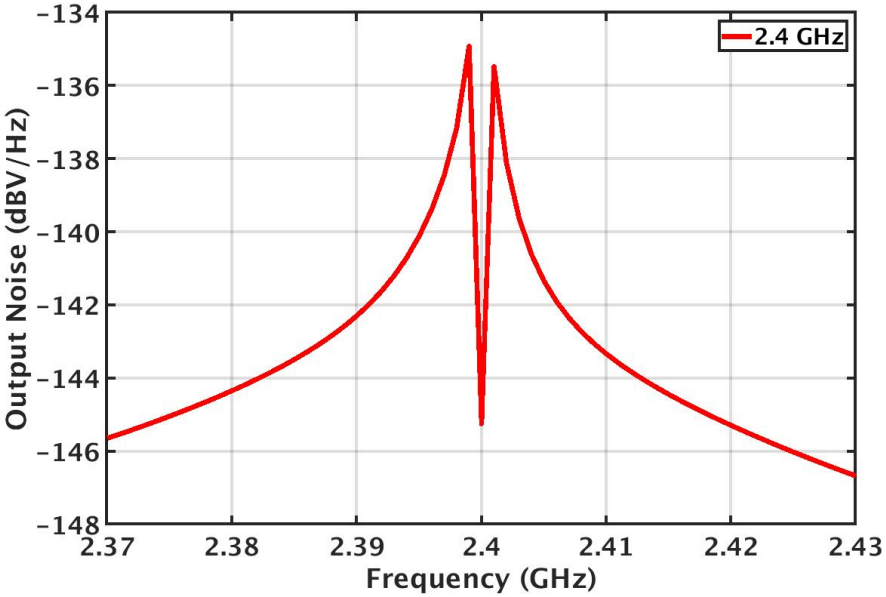



**Figure D.19:** Output noise simulation result

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| /CHIP/CORE/RC/REF_D_M10 | fn | 0.000268693 | 24.01 |
| /CHIP/CORE/RC/Driver_Biasing_M1 | fn | 0.000204873 | 13.96 |
| /CHIP/CORE/RC/REF_OS_M10 | fn | 0.000188129 | 11.77 |
| /CHIP/CORE/RC/REF_D_M9 | fn | 0.000145623 | 7.05 |
| /CHIP/CORE/RC/REF_D_M11 | id | 0.000103877 | 3.59 |
| /CHIP/CORE/RC/REF_D_M10 | id | 0.000102978 | 3.53 |
| /CHIP/CORE/RC/REF_OS_M9 | fn | 0.000101962 | 3.46 |
| /CHIP/CORE/RC/Driver_Biasing_M1 | id | 9.89226e-05 | 3.25 |
| /CHIP/CORE/RC/REF_D_M9 | id | 7.99953e-05 | 2.13 |
| /CHIP/CORE/RC/Driver_Biasing_M3 | id | 7.51799e-05 | 1.88 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000548339
Total Input Referred Noise = 3.30537e-05
The above noise summary info is for pnoise_usb data

**Figure D.20:** Top *10* noise contributors in the bandwidth *2.38 GHz - 2.42 GHz*

# D.5. Nodal voltages

| Freq = 2.4 GHz | | P1dB | P1db + 1dB | Max Power |
|---|---|---|---|---|
| | | Pin = -5 dBm | Pin = -4 dBm | Pin = 2 dBm |
| **Output Stage** | | | | |
| $V_{DS}$ | $M_2$ | 3.5 | 3.7 | 4.1 |
| | $M_1$ | 1.3 | 1.3 | 1.4 |
| | $M_0$ | 1.3 | 1.3 | 1.4 |
| $V_{GS}$ | $M_2$ | 1.5 | 1.5 | 1.6 |
| | $M_1$ | 1.0 | 1.1 | 1.1 |
| | $M_0$ | 1.1 | 1.2 | 1.7 |
| $V_{DG}$ | $M_2$ | 3.1 | 3.2 | 3.6 |
| | $M_1$ | 1.1 | 1.1 | 1.1 |
| | $M_0$ | 1.5 | 1.6 | 2.2 |
| $V_{DB}$ | $M_2$ | 3.5 | 3.7 | 4.1 |
| | $M_1$ | 2.5 | 2.5 | 2.6 |
| | $M_0$ | 1.3 | 1.3 | 1.4 |
| $V_{GB}$ | $M_2$ | 2.9 | 2.9 | 3.0 |
| | $M_1$ | 1.6 | 1.6 | 1.7 |
| | $M_0$ | 1.1 | 1.2 | 1.7 |
| $V_{SB}$ | $M_2$ | 2.5 | 2.5 | 2.6 |
| | $M_1$ | 1.3 | 1.3 | 1.4 |
| | $M_0$ | 0.0 | 0.0 | 0.0 |
| $V_{DPsub}$ | $M_2$ | 6.0 | 6.2 | 6.6 |
| $V_{DNWPsub}$ | | 3.4 | 3.4 | 3.5 |
| $V_{DNWBulk}$ | | 1.8 | 1.8 | 1.9 |
| **Driver** | | | | |
| $V_{DS}$ | $M_7$ | 3.3 | 2.6 | 2.7 |
| | $M_6$ | 1.5 | 1.2 | 1.2 |
| $V_{gs}$ | $M_7$ | 1.4 | 1.1 | 1.2 |
| | $M_6$ | 1.0 | 0.8 | 0.8 |
| $V_{DG}$ | $M_7$ | 2.8 | 1.9 | 2.1 |
| | $M_6$ | 1.0 | 0.6 | 0.7 |

| Freq = 2.1 -2.7 GHz | | P1dB | P1db + 1dB | Max Power |
|---|---|---|---|---|
| | | Pin = -5 dBm | Pin = -4 dBm | Pin = 2 dBm |
| **Output Stage** | | | | |
| $V_{DS}$ | $M_2$ | 4.0 | 4.2 | 4.9 |
| | $M_1$ | 1.4 | 1.4 | 1.5 |
| | $M_0$ | 1.3 | 1.3 | 1.4 |
| $V_{GS}$ | $M_2$ | 1.5 | 1.5 | 1.6 |
| | $M_1$ | 1.0 | 1.1 | 1.1 |
| | $M_0$ | 1.1 | 1.2 | 1.7 |
| $V_{DG}$ | $M_2$ | 3.6 | 3.8 | 4.4 |
| | $M_1$ | 1.1 | 1.1 | 1.1 |
| | $M_0$ | 1.5 | 1.6 | 2.2 |
| $V_{DB}$ | $M_2$ | 4.0 | 4.2 | 4.9 |
| | $M_1$ | 2.5 | 2.5 | 2.6 |
| | $M_0$ | 1.3 | 1.3 | 1.4 |
| $V_{GB}$ | $M_2$ | 2.9 | 2.9 | 3.0 |
| | $M_1$ | 1.6 | 1.7 | 1.7 |
| | $M_0$ | 1.1 | 1.2 | 1.7 |
| $V_{SB}$ | $M_2$ | 2.5 | 2.5 | 2.6 |
| | $M_1$ | 1.3 | 1.3 | 1.4 |
| | $M_0$ | 0.0 | 0.0 | 0.0 |
| $V_{DPsub}$ | $M_2$ | 6.5 | 6.8 | 7.5 |
| $V_{DNWPsub}$ | | 3.4 | 3.4 | 3.5 |
| $V_{DNWBulk}$ | | 1.8 | 1.8 | 1.9 |
| **Driver** | | | | |
| $V_{DS}$ | $M_7$ | 2.7 | 2.8 | 3.5 |
| | $M_6$ | 1.2 | 1.2 | 1.5 |
| $V_{GS}$ | $M_7$ | 1.2 | 1.2 | 1.4 |
| | $M_6$ | 0.8 | 0.9 | 1.1 |
| $V_{DG}$ | $M_7$ | 2.1 | 2.2 | 2.9 |
| | $M_6$ | 0.7 | 0.7 | 1.0 |

**Table D.1:** Nodal voltages in the output stage and driver of the PA in *40 nm*

# List of Figures

# List of Tables

# Abbreviations & Acronyms

**ACLR** adjacent channel leakage ratio. 94

**balun** balanced to unbalanced. 24, 26, 27, 29–34, 38, 70, 71, 73, 75, 80, 81, 83–85, 87, 88, 91, 117–119

**BPF** bandpass filter. 1

**CCF** Continuous Class F. xi, 9, 11, 13–16, 20, 21, 23, 24, 39, 49, 66, 70, 72, 74, 81, 84–86, 90, 94, 96–98, 117, 119

**CM** Current Mode. 3

**CMOS** complementary metal–oxide semiconductor. xi, 2, 6, 11, 41, 96, 97, 122

**DAC** digital to analog converter. 1

**ECCF** Extended Continuous Class F. 15, 16, 20, 21, 117

**ESD** electrostatic diodes. 88

**EVM** Error vector magnitude. xi, 6, 48, 49, 66, 67, 70, 73, 74, 79, 92–94, 96–98, 119, 121

**FET** field-effect transistor. 40, 41, 118

**GaAs** gallium arsenide. 2

**GaN** gallium nitride. 2

**LTE** Long Term Evolution. 6, 97

**MOSFET** metal-oxide semiconductor field-effect transistor. 40

**OFDM** Orthogonal Frequency Division Multiplexing. 96

**PA** power amplifier. xi, 1–9, 11, 13–15, 20, 21, 24, 31, 39–41, 47, 48, 54, 61, 65–67, 70, 73–77, 81–86, 89, 90, 92, 94, 96–98, 115, 117–119, 121, 122

**PCB** printed circuit board. 85, 97

**QAM** quadrature amplitude modulation. 92, 93, 96, 97, 105–110, 119, 120

**RF** radio frequency. 1, 2, 117

**SoC** system on chip. xi, 2

**VM** Voltage Mode. 3

**WiFi** Wireless Fidelity. xi, 1, 2, 6, 7, 11, 21, 31, 48, 97, 98

**WLAN** Wireless Local Area Network. 1, 96, 122

**ZCS** Zero Current Switching. 3, 4

**ZVS** Zero Voltage Switching. 3

# Nomenclature

| | |
|---|---|
| $\eta$ | Efficiency |
| $\eta_D$ | Drain Efficiency |
| $\omega_0$ | Fundamental Frequency Band (2.4 GHz) |
| $C_L$ | Output Load Capacitance |
| $C_{DCP}$ | Decoupling Capacitance |
| $C_{DS}$ | Drain Source Capacitance |
| $C_{GS}$ | Gate Source Capacitance |
| $C_{PRI}$ | Parallel Capacitor added between Primary Terminals of the Inter-Stage Matching |
| $C_{SB}$ | Source Bulk Capacitance |
| $C_{SEC}$ | Parallel Capacitor added between Secondary Terminals of the Inter-Stage Matching |
| $DE$ | Differential Ended |
| $G_P$ | Power Gain |
| $G_V$ | Voltage Gain |
| $I_{DC}(SE)$ | Single Ended DC current |
| $I_D$ | Drain Current |
| $I_{FUND\_MAX}(SE)$ | Single Ended Maximum Current at the fundamental band |
| $I_{FUND}(SE)$ | Single Ended Current Swing at the Fundamental band |
| $IM3$ | Third Order Intermodulation |
| $IP3$ | Third Order Intercept Point |
| $km$ | Coupling Coefficient in the Output Balun |
| $km_{IS}$ | Coupling Coefficient in the Inter-stage Matching |
| $L_2C_2$ | Second Harmonic Trap |

$L_k$ Leakage Inductance in the Transformer

$L_{BND}$ Bondwire Inductance

$L_m$ Magnetizing Inductance in the Transformer

$L_{P\_IS}$ Primary Inductance of the Inter-stage matching

$L_P$ Primary Inductance of the Output Balun

$L_{S\_IS}$ Secondary Inductance of the Inter-stage Matching

$L_S$ Secondary Inductance of the Output Balun

$N$ Turn Ratio in the Transformer

$OIP3$ Output Third Order Intercept

$OP1dB$ Output 1dB Compression Point

$P_{\mathrm{OUT}}$ Output Power

$P_{DC}$ DC Power Consumption

$P_{FUND}$ Power at the fundamental band

$P_{in}$ Input Power

$R_D$ Real part of Drain Impedance

$R_L$ Load Impedance = 50 Ω

$R_D(DE)$ Differential Impedance at the Drain of the Differential Pair

$R_D(SE)$ Single Ended Impedance at the Drain of the Transistor

$R_{SEC}$ Parallel Resistor added between Secondary Terminals of the Inter-Stage Matching

$SE$ Single Ended

$V_{DD}$ Supply Voltage

$V_{DG}$ Drain Gate Voltage

$V_{DS}$ Drain Source Voltage

$V_{FUND}(DE)$ Differential Ended Voltage Swing at Fundamental Band

$V_{FUND}(SE)$ Single Ended Voltage Swing at Fundamental Band

$V_{GS}$ Gate Source Voltage

$W/L$ Aspect Ratio of the Transistor

$X_D$ Reactive part of Drain Impedance

$Z_D$ Drain Impedance

$Z_{1f}$ Load Impedance at Fundamental band

$Z_{2f}$ Load Impedance at Second Harmonic band

$Z_{3f}$ Load Impedance at Third Harmonic band

$Z_{SB}$ Total Impedance of Second Harmonic Trap and Balun