Single-Channel Heterogeneous-Source Energy Harvesting PMIC Design

August 10, 2021

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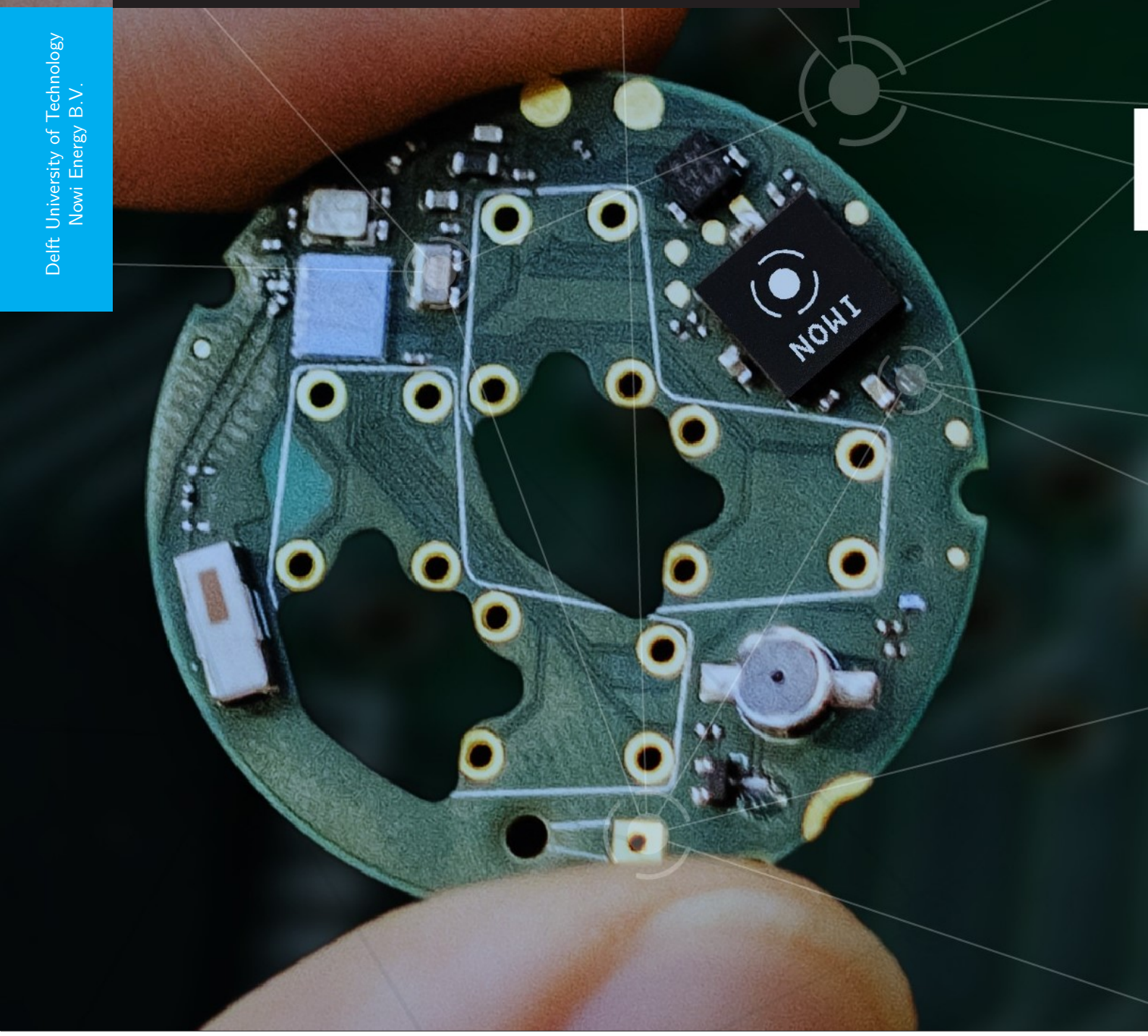

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Challenge the future

Single-Channel Heterogeneous-Source Energy Harvesting PMIC Design

August 10, 2021

by

J.P. van der Velden

in partial fulfillment of the requirements for the degree of

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in Electrical Engineering

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ABSTRACT

This work proposes an energy harvesting platform that is able to convert power from both DC sources (photovoltaic cells and TEGs) as well as piezo element sources. It does so only using a single input channel to which a single harvester can be connected. The proposed system is able to differentiate between the two source types and adjust the power converter configuration accordingly.

For the DC sources, a novel switched-capacitor power converter (SCPC) is proposed, that is able to convert the energy from a harvester that has a maximum power point (MPP) output voltage of $170mV$ to $5V$ and a maximum power point output power of $10\mu W$ to $50mW$. This DC-DC converter offers 119 different positive voltage conversion ratios, with a maximum voltage conversion ratio of 16, using four in-package capacitors. As a result of this high number of conversion ratios, the MPP output voltage of the harvester and the input voltage of the power converter are matched accurately, causing the harvesting efficiency to be very high. A maximum harvesting efficiency of 96.2% is found in simulations.

For the piezo element sources, the concept of a flipping-capacitor rectifier (FCR) has been adjusted to work in harmony with the designed SCPC. In a steady-state condition, the capacitors of the SCPC reach specific voltages, such that they can create evenly spaced voltage steps for the flipping operation. With this technique, a voltage flipping efficiency of 0.9375 and a theoretical maximum output power improvement rate (MOPIR) of 32 can be reached. Due to losses in the system, simulation results show a MOPIR of up to 20.0, which is still significantly higher than the state-of-art. The system is designed to work with harvesters with a piezo capacitance of up to $100nF$, an excitation frequency of $1Hz$ to $200Hz$ and an equivalent FBR maximum power point output power of $1\mu W$ to $50mW$.

An implementation of the proposed system is discussed and simulated. The total active silicon area for the designed system is $2.12mm^2$ in a $0.18\mu m$ TSMC technology.

Keywords: energy harvesting, heterogeneous sources, single-channel, single-input, DC-DC converter, switched-capacitor (SC), charge pump, piezoelectric energy harvesting (PEH), maximum output power improvement rate (MOPIR), flipping-capacitor rectifier (FCR), synchronized switch harvesting on capacitors (SSHC), capacitor re-use, source differentiation, CMOS

PREFACE

The following document contains the thesis work for my Master of Science in Electrical Engineering. It marks the end of my thesis internship at Nowi and educational career at the University of Technology Delft, although I hope to keep learning as much as I did during the last couple of years. I would like to thank Nowi for giving me the opportunity to work with them and for supplying me with the tools and knowledge that come with designing and producing PMICs.

I want to thank the entire IC team for helping me out with designing difficulties and reviewing my work. In particular, many thanks to Gustavo for his excellent supervision during the entirety of this project, helping me acquire new analog IC design skills, helping me out with critical design choices and reviewing my work every step of the way. I would also like to express by gratitude towards Wouter for his encouragements and for challenging me to broaden my view during our meetings.

Finally, I would like to thank my family and friends for their support and interest in my work. Explaining something as extraordinary as energy harvesting has been challenging at times, but has also always encouraged me.

Joram van der Velden
Delft, August 10, 2021

CONTENTS

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INTRODUCTION

1.1. POWERING IOT NODES

While the Internet of Things (IoT) has been around for more than a decade [1], powering IoT nodes has remained a challenge. Traditionally, electronic devices are either powered by connecting them to an electricity grid or to a battery. The first of these methods requires a set of wires to each node, which may be costly and complicated, if not infeasible. Powering an IoT node through a battery is the second method, but this also has its drawbacks. The total amount of energy that can be extracted from a battery is limited, such that battery replacement is inevitable after a certain period of time. This operation does not only bring with it material cost, but also personnel cost, both of which increase with the amount of IoT nodes present in the system.

Fortunately, there is a third option of supplying power to an IoT node, namely through energy harvesting. Energy harvesting does not have the drawbacks of the previously mentioned methods, and therefore enables applications in a much wider range of environments.

1.2. ENERGY HARVESTING

In most of the cases, there is some form of energy around an IoT node, just as there is energy all around us in daily life. As opposed to wireless power transfer, this energy is not present for the sole purpose of supplying energy to some system. Instead, this so-called ambient energy is present because of the structure of nature (e.g. solar energy, kinetic wind energy) or as a by-product of some other action (e.g. vibrational energy, RF energy). In energy harvesting, this ambient energy is gathered and stored, such that it can be used in a different energy domain and/or at a different time. In the context of powering IoT nodes, the energy is converted to electrical energy using a harvester (also referred to as a transducer). Next, the energy is converted in the electrical domain to charge the storage device suitably. This work focusses on this last step of the energy harvesting process.

1.3. MULTI-SOURCE PLATFORMS

Different applications in different environments require energy harvesting from different types of ambient energy sources. Therefore, a device that allows harvesting from multiple types of ambient energy sources has more potential in the field of energy harvesting than a device that supports only one type of ambient energy source. The difficulty in designing a system that allows multiple types of harvesters to be connected, is that different types of harvesters require different harvesting interfaces (circuits that convert the harvested power suitably to charge the storage device).

In the literature, this problem is usually solved by designing a multi-input system [2–7], where each type of harvester is connected to a different input. Sometimes these systems also allow energy harvesting from multiple sources at once. A disadvantage of these types of systems is that additional pins are required as well as additional silicon for the different harvesting interfaces and for switching between the different inputs. As opposed to multi-input systems, a single-input (single-channel) system only requires one set of input pins for connecting harvesters and is thought to increase convenience for implementation. This work focusses

on designing a single-input system that allows (non-simultaneous) harvesting from three types of sources. These were chosen based on the literature study that can be found in Chapter 2.

1.4. THESIS OBJECTIVE

The thesis objective has been defined as follows:

> To design a low-power high efficiency single-channel PMIC that can harvest both DC power from solar and TEG sources and AC power from piezo elements at the maximum power point (MPP).

This work focusses on designing an integrated circuit to reduce the BOM cost and PCB footprint. The type of circuit that is designed is referred to as a power management integrated circuit (PMIC). Several limitations have been set. Firstly, an input power of $10\mu W$ to $50mW$ is expected. A minimum input power is considered, as the harvesting at least has to account for some self-discharging of the battery and power consumption of the control circuitry in the chip. An upper limit of input power is set for the design to limit the expected device current. Secondly, frequencies between $1Hz$ and $200Hz$ can be expected to be harvested from mechanical vibrations, as shown in [8]. Lastly, it is assumed that the power for the circuit will be provided by a battery that has an operating voltage between $3.0V$ and $4.5V$. Although limits are set for the PMIC design, this does not necessarily mean that the design will not work outside these limits, but rather that operations beyond these limits are not considered in the design steps and performance evaluations.

The design of the integrated circuit will be made in a $0.18\mu m$ TSMC technology with devices that can handle a maximum voltage of $5V$.

1.5. THESIS ORGANIZATION

This thesis aims to introduce energy harvesting techniques, present the design choices that have led to the proposed design and discuss the expected performance of the system. This thesis is organized as follows.

Chapter 2 discusses the energy domains in which ambient energy exist, conversion techniques to convert this ambient energy to electrical energy and suitable harvesters to do so. Additionally, it discusses energy harvesting interfaces and power conversion techniques for both piezo element sources as well as DC sources.

Chapter 3 shows an overview of the designed system. It shortly discusses the reasoning for the chosen subsystems and their requirements.

Chapter 4 discusses the design of a novel switched-capacitor power converter (SCPC) — sometimes also referred to as a charge pump — for DC-to-DC voltage conversions. It analyses, models and optimizes the design, shows its expected performance and discusses protection circuitry for the SCPC.

Chapter 5 elaborates on using the designed SCPC to get an increased voltage flipping efficiency for piezo element harvesting. A rectifier is discussed to complete the design of this voltage flipping rectifier. Additionally, protection and control circuits are discussed.

Chapter 6 discusses the combination of the both harvesting methods, such that they can be integrated into a single-channel solution. This includes the design of the controller as well as a debug module.

Chapter 7 shows the simulation results of the designed system in various use cases. It also compares the designed voltage flipping rectifier to the state-of-art.

Chapter 8 contains a discussion of the design, its results and the limitations of the system.

Chapter 9 concludes this work. It shows a thesis overview, highlights the most important contributions to the field of energy harvesting and gives recommendations for future work.

2

Introduction to Energy Harvesting

2.1. Introduction

This chapter introduces techniques involved in energy harvesting. It is the result of the literature study that was conducted for this thesis work. Firstly, energy harvesting sources, conversion phenomena and devices are discussed. This results in the design context that is depicted in the flow chart in Figure 2.17. Secondly, energy harvesting techniques for piezo element sources and DC sources are discussed.

2.2. Energy Harvesting Source Types

In most of the cases, there is be some form of energy around an IoT node, just as there is energy all around us in daily life. This ambient energy can be divided into several categories [9, 10]:

- Solar Energy[1]
- Thermal Energy
- Mechanical/Kinetic Energy
- RF (Radio Frequency) Energy
- Chemical Energy
- Nuclear Energy

Chemical and nuclear energy are not regarded as viable sources of power, as these are generally not be present near IoT nodes. Figure 2.1 shows that the output power of RF (Radio Frequency) energy is much lower than that of the other remaining sources and that its signal frequency range is much higher. Although the high signal frequency can be dealt with by using specific harvesting interfaces, the amount of ambient energy available from RF sources is often considered to be too low for energy harvesting purposes [11]. For this reason, energy harvesting from ambient RF energy is not taken into account in the design and is left for future research.

2.3. Energy Conversion Phenomena

The energy that is available from each of the energy sources, can be converted to electrical energy using several different mechanisms. This section discusses the conversion mechanisms used to convert solar, thermal and mechanical energy to electrical energy.

[1] In this work, solar energy may also refer to energy coming from indoor lighting, instead of the sun. The term electromagnetic energy would also suit this type of energy, however, the use of this term has been limited to avoid confusion with RF energy, which is also a type of electromagnetic energy.

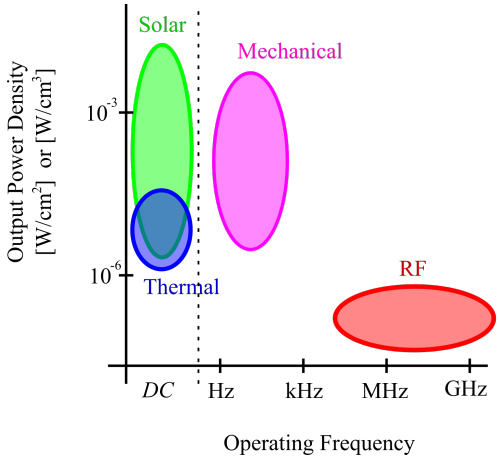


Figure 2.1: Comparison of energy source power and frequency [8, 10, 12–14]

2.3.1. SOLAR ENERGY CONVERSION

Solar energy can be converted to electrical energy through the photovoltaic effect. The energy carried by the photons is transferred to electrons in a PN junction, creating a photo-generated current [15]. Harvesting devices using this effect are called solar or photovoltaic (PV) cells. In this case, the second term is preferred, as energy harvesting using the photovoltaic effect is not limited to light energy from the sun, but is also possible with light originating from indoor lighting.

2.3.2. THERMAL ENERGY CONVERSION

For thermal energy harvesting two physical effects are mainly used: The thermoelectric (Seebeck) effect and the pyroelectric effect. While thermoelectric materials convert energy from a spatial thermal gradient, the pyroelectric materials convert energy from temporal thermal gradients [16]. As temporal thermal gradient around IoT nodes may have a very low frequency and amplitude, the power that can be harvested from this source may be very limited. Therefore, the thermoelectric effect is the preferred conversion phenomena for thermal energy harvesting. A harvester using the thermoelectric effect is often referred to as a thermoelectric generator (TEG).

2.3.3. MECHANICAL ENERGY CONVERSION

For mechanical energy harvesting, multiple conversion phenomena are available: the magnetostatic effect, the electrostatic effect, the triboelectric effect and the piezoelectric effect. [13, 17]

- In magnetostatic energy conversion (also known as electromagnetic induction), the relative position between a coil and a magnetic field causes current flow inside the coil, as a result of an inputted mechanical energy.
- In electrostatic energy conversion, the distance between two conductors separated by a dielectric material, is changed with the help of mechanical energy, creating a change in energy stored in the capacitance between the two conductors. The additional energy can be extracted in the electrical domain.
- In the triboelectric effect, the rubbing of two different materials causes electrons to move between the two materials in a specific direction.
- In the piezoelectric effect a force on a piezoelectric material, directly results in charge accumulation inside the material (see Section 2.4.3).

Several factors contribute to the choice of piezoelectric energy conversion for mechanical energy harvesting. Magnetostatic energy conversion requires larger scale components such as permanent magnets, which is undesirable in small form factor harvesting solutions. Electrostatic conversion requires micro-machined variable capacitors or electrets increasing cost and complexity. The triboelectric effect can only be achieved when there is friction between the two materials, which causes heating and wear, which limits the lifetime of the harvester. Lastly, a significant advantage of using the piezoelectric effect is that many sensing and harvesting elements are commercially available already, easing implementation over a wide range of operating

conditions.

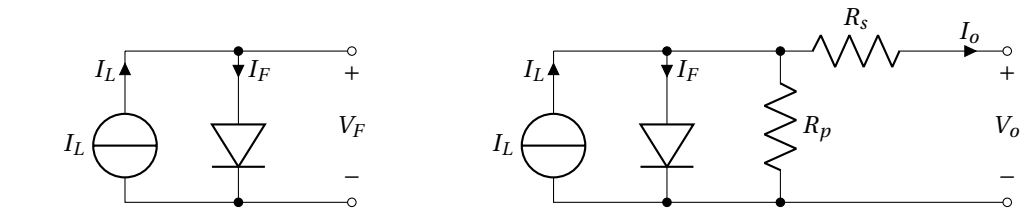
2.4. HARVESTING DEVICES

This section will discuss the various devices that are used in the aforementioned energy conversion phenomena.

2.4.1. PHOTOVOLTAIC CELL

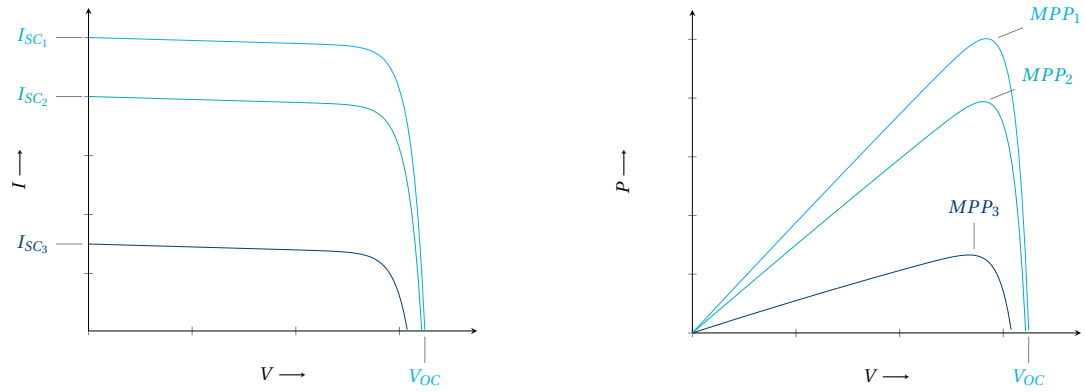
A photovoltaic cell is essentially a PN junction under illumination. The photons that are absorbed in the so-called space charge region of the PN junction, create electron-hole pairs. The holes and electrons are accelerated in opposite directions due to the electric field that is present in the space charge region. The movements of these charge carriers make up the photocurrent I_L. Additionally, a forward-bias current I_F is present in the diode, when a voltage is applied. Equation (2.1) shows the current through the photovoltaic cell [15]. Moreover, we can make an equivalent model of the photovoltaic cell as shown in Figure 2.2. This model is expanded with parallel and series resistances in order to model extrinsic effects like current leaks and material resistances [18].

$$I = I_L - I_F = I_L - I_S \left[exp\left(\frac{eV_F}{kT}\right) - 1 \right] \tag{2.1}$$



(a) (b)

Figure 2.2: Simple (a) and complete (b) equivalent models of a photovoltaic cell



(a) I-V Characteristic (b) P-V Characteristic

Figure 2.3: Characteristics of a PN junction solar cell under different levels of illumination

Figure 2.3a shows the current-to-voltage characteristic of a photovoltaic cell. Figure 2.3b shows the power-to-voltage characteristic of a photovoltaic cell. This depicts one of the main challenges in optimally using photovoltaic cells as harvesting devices: the maximum power point (MPP) may not be easily detectable, due to the non-linearity of the internal diode and changing illumination.

2.4.2. THERMOELECTRIC GENERATOR

A thermoelectric generator (TEG) consists of a number of thermopiles connected in series. In each thermopile, a voltage is induced due to the temperature difference between the two ends, as described by the

Seebeck effect. This is also shown in (2.2) where V is the generated voltage, S is the Seebeck coefficient and ΔT is the temperature difference between the two ends of a thermopile [19].

$$V = S \cdot \Delta T \tag{2.2}$$

The resistance of the series connected thermopiles creates an equivalent source resistance. As the conductivity of a good thermopile is high, one encounters a low source resistance. Furthermore, the number of thermopiles is be limited for a certain TEG size and the temperature difference between the hot and cold side may be low. Therefore, one can expect to encounter very low (maximum power point) voltages from TEG elements. Figure 2.4 shows the equivalent circuit for a TEG element and Figure 2.5 shows the characteristic curves for a TEG element. Equations (2.3) trough (2.6) show that the maximum power point is found for $V_o = V_s/2$.

$$I_o = \frac{V_s - V_o}{R_s} \tag{2.3}$$

$$P_o = V_o \cdot I_o = \frac{V_s}{R_s} \cdot V_o - \frac{1}{R_s} \cdot V_o^2 \tag{2.4}$$

The maximum power point is found when the derivative of the power is zero:

$$\frac{\delta P_o}{\delta V_o} = \frac{V_s}{R_s} - \frac{2}{R_s} \cdot V_o = 0 \tag{2.5}$$

$$V_o = \frac{V_s}{R_s} \cdot \frac{R_s}{2} = \frac{V_s}{2} \tag{2.6}$$

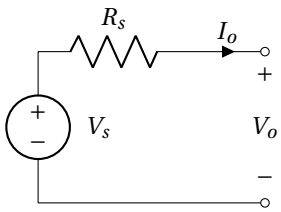
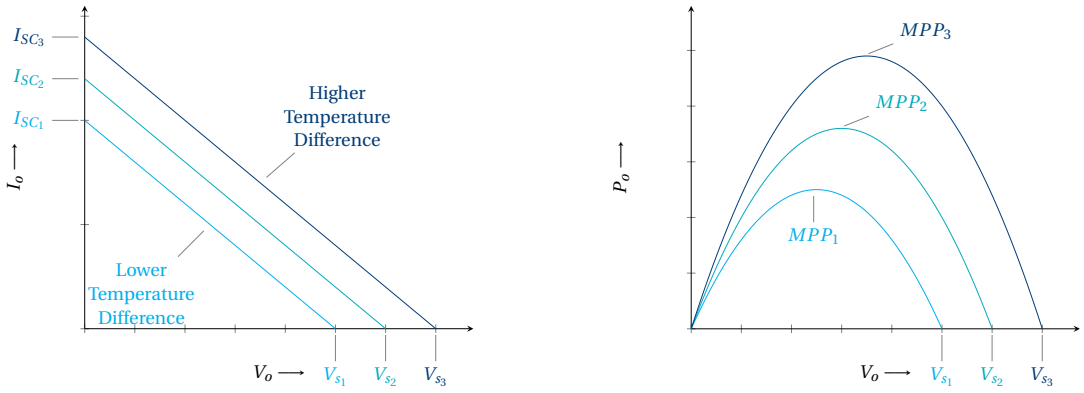


Figure 2.4: Equivalent models of a TEG



(a) I-V Characteristic

(b) P-V Characteristic

Figure 2.5: Characteristics of a TEG for multiple temperatures

2.4.3. PIEZO ELEMENT

This section will elaborate on the behavior of several common piezo elements. The direct and indirect piezoelectric effect are discussed, after which the piezo elements will be discussed.

DIRECT PIEZOELECTRIC EFFECT

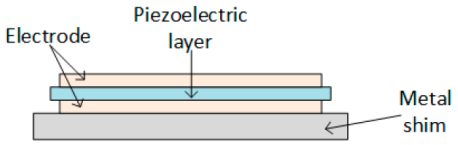


Figure 2.6: The side view of a piezo diaphragm [20]

Firstly, a model for one dimensional charge build-up is be discussed, considering the piezo element as shown in Figure 2.6. From the IEEE Standard on Piezoelectricity one can deduce (2.7), assuming a charge build-up in the z-direction (sometimes referred to as the 3-direction) as a result of stress in the z-direction [21]. The constant in this equation depict the following: D is the electric displacement in the z-direction, d_{33} is a piezo material property and σ is the stress in the z-direction. This is referred to as the piezoelectric effect.

$$D = d_{33} \cdot \sigma \quad \left[C/m^2\right] \tag{2.7}$$

Next, the charge build-up on the electrodes can be expressed as shown in (2.8), where q is the charge on the electrodes and A is the piezo element area.

$$q = A \cdot D = A \cdot d_{33} \cdot \sigma \quad [C] \tag{2.8}$$

The current inside the piezoelectric material can be found to be the derivative of the charge to time, as shown in (2.9).

$$I_p = \frac{\delta q}{\delta t} = A \cdot d_{33} \cdot \frac{\delta \sigma}{\delta t} \quad [A] \tag{2.9}$$

As a piezoelectric material is always dielectric [14], the parasitic capacitance that is created by the electrodes and piezoelectric material is shown by (2.10), where ϵ_0 is the permittivity for air, ϵ_r is the relative permittivity, A is the area of the element and t is the thickness of the piezoelectric layer.

$$C_p = \frac{\epsilon_0 \epsilon_r A}{t} \quad [F] \tag{2.10}$$

Figure 2.7 shows a circuit representation of (2.9) and (2.10).

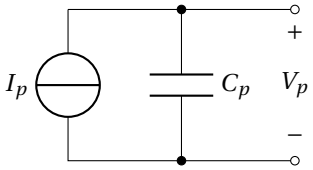


Figure 2.7: Simple equivalent model for the piezoelectric effect

INDIRECT PIEZOELECTRIC EFFECT

Equation (2.8) assumes a direct stress on the piezo material. However, the stress in the material may also be caused by straining the material, as is done in cantilever beams, circular diaphragms and cymbal transducers [20]. The stress and strain inside the material are related with the elastic compliance matrix ($\mathbf{s}^{\mathbf{E}}$) as shown in (2.11) [14].

$$\vec{\epsilon} = \mathbf{s}^{\mathbf{E}} \cdot \vec{\sigma} \tag{2.11}$$

The stress in the z-direction (σ) in the previous equations can be substituted by the third element of the vector created by $\vec{\epsilon}$ / $\mathbf{s}^{\mathbf{E}}$. Whether the charge build-up may be caused directly by a stress or indirectly by a strain, the result in the electrical domain is the same: a charge build-up due to a stress inside the material. Therefore the same equivalent model can be used, except that there is a different definition of the piezo current I_p.

PIEZO ELEMENT RESONANCE

As shown in [22], piezoelectric material may have a resonance frequency of itself. However, as the resonance frequency of the piezoelectric material is in the order of $100s$ of kHz and higher, it is regarded to be out of the frequency range for this design.

Nonetheless, resonance may occur in the structure surrounding the piezo material (e.g. a cantilever beam, circular diaphragm or cymbal transducer). Two approaches can be used to model the resonance of these elements. Firstly, the mechanical resonance could be translated to the electrical domain in an RLC representation, as shown in [22]. Another method is to assume that when used, the element is excited at its mechanical resonance frequency. In this case, the stress inside the material (σ) shows sinusoidal behaviour at the resonance frequency and, following (2.9), so does the current. Therefore, using this second method, the piezo element model is not changed, except for the fact that the current source shows sinusoidal behaviour.

The second approach is used, as it reduces model complexity, and the assumption (excitation at mechanical resonance) is expected to be true.

PARASITIC RESISTANCE

The piezoelectric layer has a finite resistance, which can be modelled by adding a parallel resistance (R_p) to complete the model (shown in Figure 2.8). Adding a finite parasitic parallel resistance increases the accuracy of the model sufficiently for the frequency range of this design [22].

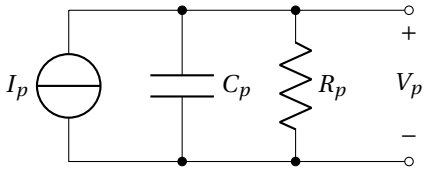


Figure 2.8: Complete equivalent model for the piezoelectric effect

PIEZO ELEMENT BEHAVIOUR

Following the model that has been developed, some remarks can be made about the behaviour of piezo elements.

Firstly, in a realistic scenario, the stress (or strain induced stress) in a material does not constantly increase or decrease, but rather shows change over time. As the current I_p is proportional to the derivative of the stress, there is no DC current from current source I_p. In harvesting situations, the constantly changing stress (or strain induced stress), creates a constantly changing I_p, not only in amplitude but also in polarity. Therefore, a bipolar current and voltage waveforms are present.

Secondly, due to the bipolar waveforms, the parasitic capacitance is constantly charged and discharged. Effort should be put into the recycling of charge present during the cycles to maximize output power. The maximum power point operation is dependent on the chosen converter and is elaborated on in the next chapters.

Lastly, as (random and unpredictable) impulse-based stress or strain inputs may be presented to the piezo element, the to-be harvested current and/or voltage output also has an element of unpredictability.

2.5. ENERGY HARVESTING TECHNIQUES

This section explores several elements of power conversion for energy harvesting PMICs from photovoltaic, TEG and piezoelectric harvesters. Firstly, PMIC designs for multiple sources are discussed. Secondly, MPPT

algorithms are discussed. Next, several piezo element harvesting techniques are discussed. Lastly, several systematic approaches for an integrated DC/DC converter design are discussed.

2.5.1. MULTI SOURCE PMICS

A common reason for PMIC design for multiple heterogeneous sources is that different sources generate different amounts of power, and are, therefore, not always be able to supply power. By using a multi-source solution, the availability and stability of the supplied power is be increased [2].

Several of the multi source PMIC designs simply use a rectifier [2–4] or voltage doubler [5, 6] to handle the AC input power. Other designs feature an inductor that is used for AC to DC conversion as well as maximum power extraction [7]. When using multiple heterogeneous sources at once, the maximum power extraction condition can be complex, as decisions have to be made on which of the sources to use. However, this is not a relevant subject for a single channel PMIC.

2.5.2. MPPT SCHEMES

Maximum power point tracking (MPPT) is essential in most energy harvesting applications, as it ensures that the maximum amount of energy is harvested from the device. One of the more basic methods in this is the FOCV (fractional open circuit voltage), where the energy is harvested at a voltage which is a fraction (0.5 for linear DC sources and 0.6 to 0.8 for PV sources) of the open circuit voltage [3–5, 7]. Additionally, a 'Hill-Climbing' (sometimes referred to as 'Perturb and Observe') algorithm can be used, where PMIC configurations are swept to obtain the optimal configuration and extract the maximum amount of power [6]. Many other MPPT algorithms have also been developed [23, 24]. MPPT for piezo elements is very dependent on the harvesting technique used, as discussed in the next section.

2.5.3. PIEZO ELEMENT HARVESTING TECHNIQUES

This section discusses several methods of increasing the amount of energy harvested from piezo elements. In comparing these methods, the piezo model from Figure 2.7 is used, omitting the parasitic parallel resistance R_p. The simplified model can be used as the dissipation factor of piezoelectric material is generally lower than 2.5% [25], resulting in only insignificant waveform shifts.

FULL BRIDGE RECTIFIER

The methods described in the following sections will be compared to an ideal full bridge rectifier bridge (FBR), sometimes referred to as a full wave rectifier (FWR). This circuit rectifies the AC voltage waveform to a DC harvesting voltage with the value of V_h, as shown in Figure 2.9. Ideal diodes are assumed with a threshold voltage of $0V$.

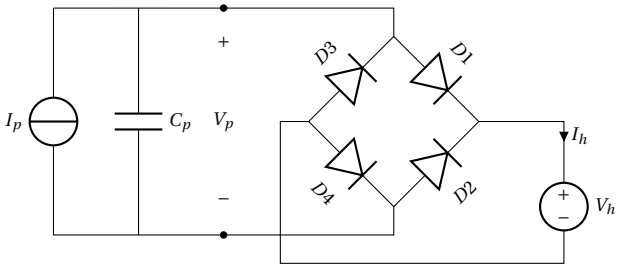
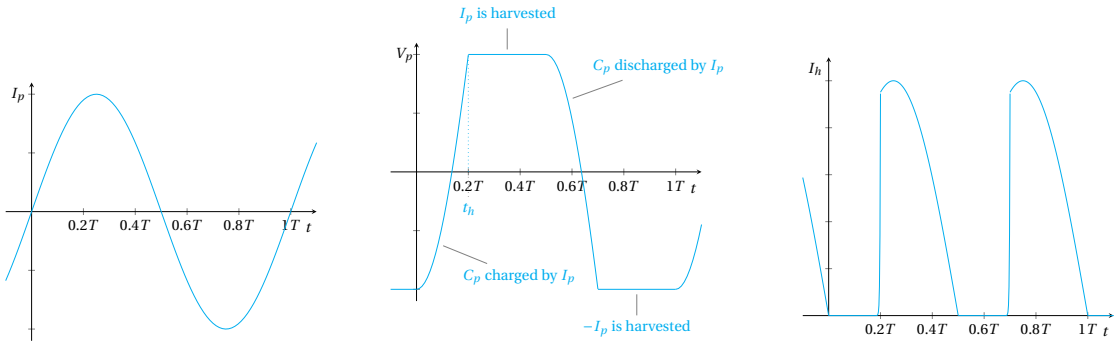


Figure 2.9: Piezo element with a full wave rectifier

The voltage and current waveforms resulting from a sinusoidal current I_p are shown in Figure 2.10, where T is the period of the sinusoidal piezo current and t_h is the time harvesting is started.

- $0 \rightarrow t_h$: The piezo voltage V_p starts at $-V_h$, but due to the *positive* piezo current I_p, no current will flow through the diodes and capacitor C_p starts *charging* up to V_h.
- $t_h \rightarrow 0.5T$: The piezo voltage V_p has reached V_h and diodes $D1$ and $D4$ start conducting, thus $I_h = I_p$.
- $0.5T \rightarrow 0.5T + t_h$: The piezo voltage V_p starts at V_h, but due to the *negative* piezo current I_p, no current will flow through the diodes and capacitor C_p starts *discharging* down to $-V_h$.



(a) Piezo current waveform I_p (b) Piezo voltage waveform V_p (c) Harvesting current waveform I_h

Figure 2.10: Full wave rectifier waveforms

- $0.5T + t_h \rightarrow T$: The piezo voltage V_p has reached $-V_h$ and diodes $D2$ and $D3$ start conducting, thus $I_h = -I_p$.

During the time that the piezo voltage V_p is rebuild ($0 \rightarrow t_h$ and $0.5T \rightarrow 0.5T + t_h$), no current is harvested. The piezo current I_p is 'wasted' on rebuilding V_p. The total charge that the rectifier is not able to harvest for each half-cycle (Q_{loss}) during this rebuilding of the piezo voltage V_p is shown in (2.12).

$$Q_{loss} = C_p \cdot 2V_h \tag{2.12}$$

Several circuit techniques have been developed to increase the amount of charge harvested. These will be discussed next. The first example of this is the switch only rectifier.

SWITCH ONLY RECITIFIER

In the switch-only rectifier (SOR) [26], switch $S1$ is added to the circuit. This switch shortly closes during the zero crossing in piezo current, thus helping the rebuilding of the piezo voltage V_p. The circuit is shown in Figure 2.11 and its waveforms are shown in Figure 2.12.

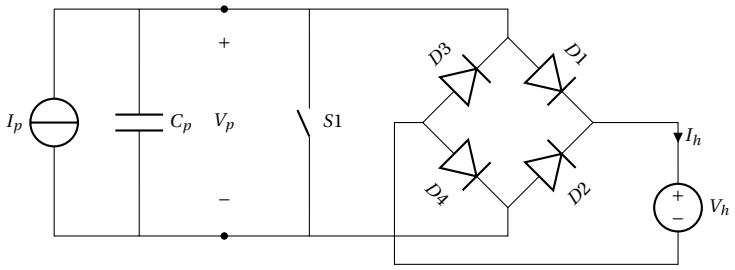
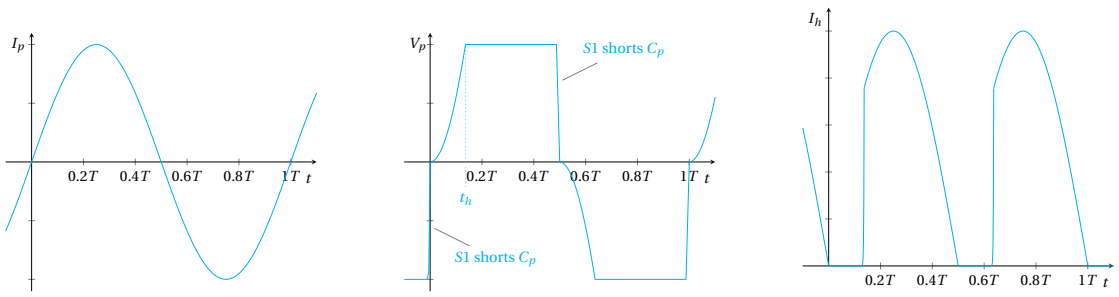


Figure 2.11: Piezo element with a switch only rectifier



(a) Piezo current waveform I_p (b) Piezo voltage waveform V_p (c) Harvesting current waveform I_h

Figure 2.12: Switch only rectifier waveforms

In using this scheme, the time to rebuild the voltage (t_h) is reduced and the charge that cannot be harvested (Q_{loss}) is reduced by four times, as shown in (2.13).

$$Q_{loss} = C_p \cdot V_h \tag{2.13}$$

The lost charge can be reduced further by using a 'Parallel Synchronized Switch Harvesting on Inductor' (P-SSHI) scheme.

PARALLEL SYNCHRONIZED SWITCH HARVESTING ON INDUCTOR

In the P-SSHI circuit [26] (also reffered to as the Bias-Flip Recifier [27]), not only a switch is added to the rectifier, but also an inductor. The LC resonance of the parasitic piezo capacitance and the inductor is used to harvest the energy remaining in the capacitor after one half-cycle, and recycling that energy to the capacitor for the following half-cycle. As is done in the SOR, the switch is only activated shortly during the zero current crossing of the piezo current. The circuit for the P-SSHI is shown in Figure 2.13 and its waveforms are shown in Figure 2.14.

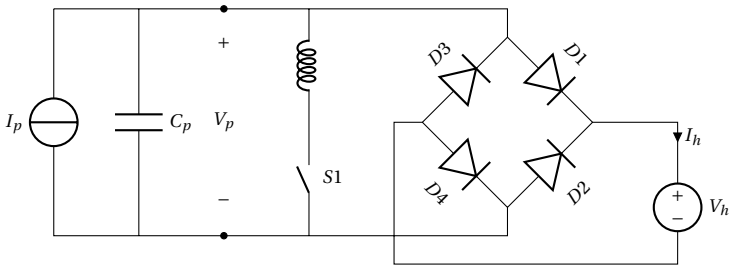
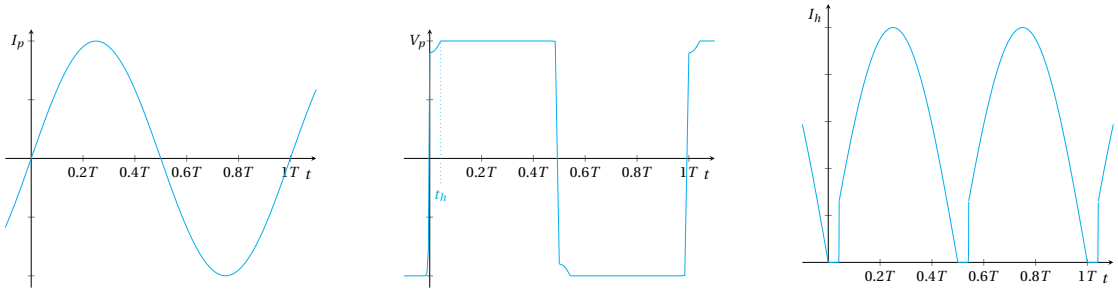


Figure 2.13: Piezo element with an P-SSHI circuit



(a) Piezo current waveform I_p

(b) Piezo voltage waveform V_p

(c) Harvesting current waveform I_h

Figure 2.14: P-SSHI waveforms

As shown in the waveforms, the negative effect of the parasitic capacitance is almost completely nullified. In an ideal case, during a transition, the piezo voltage V_p can be fully restored to its negative equivalent. However, due to the non-zero series resistances of the parasitic capacitance C_p and the inductor and the non-zero resistance of the switch, an equivalent RLC circuit is created during the closing of the switch, which has a certain Q-factor. This Q-factor determines the voltage flipping efficiency (η_{flip}), that is, the fraction of the original voltage (V_h) that the parasitic capacitance C_p is rebuild to (V_r) as shown in (2.14). In the exemplar waveforms above, this is assumed to be 90%. The total amount of charge that is lost is now significantly lower, as shown in (2.15).

$$\eta_{flip} = \frac{V_r}{V_h} \tag{2.14}$$

$$Q_{loss} = C_p \cdot (1 - \eta_{flip}) \cdot V_h \tag{2.15}$$

The disadvantage to using a P-SSHI circuit is that a inductor with a high Q factor is required for an efficient operation. A fully integrated solution is not possible. Therefore, instead of using an inductor to discharge and

recharge the parasitic capacitance C_p, capacitors can be used, as is done in the 'Flipping Capacitor Rectifier' (FCR) circuit.

FLIPPING CAPACITOR RECTIFIER

In the FCR circuit, one or more capacitors are used to discharge and recharge the parasitic capacitance of a piezo element [28]. This is sometimes also referred to as Synchronized Switch Harvesting on Capacitor (SSHC) [29]. As an example, a 7-phase FCR circuit is shown in Figure 2.15 and its waveforms are shown in Figure 2.16, although the circuit can be adapted for a smaller or larger number of capacitors and phases.

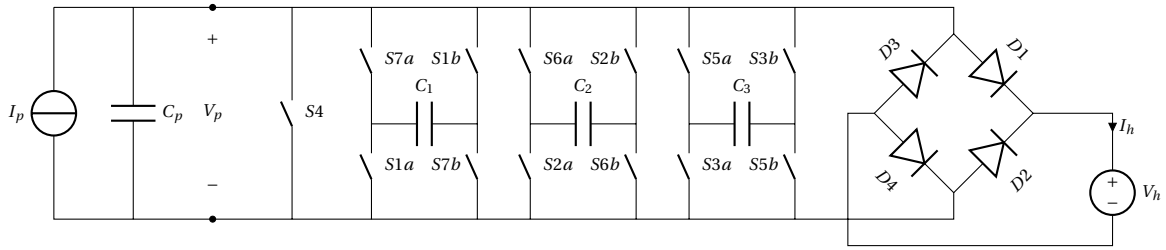
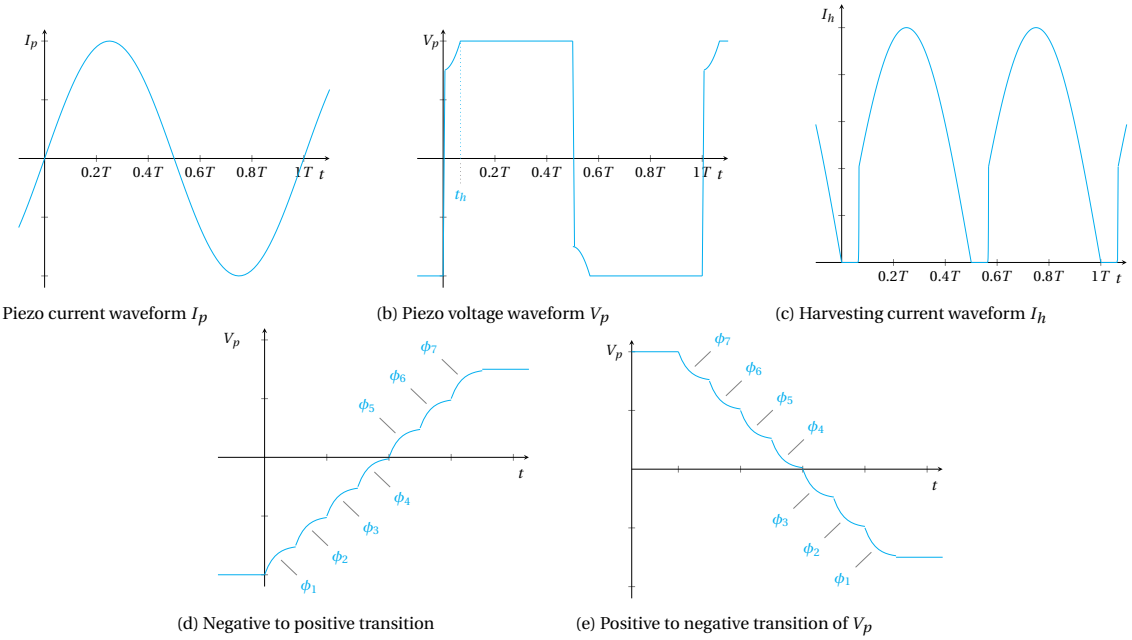


Figure 2.15: Piezo element with an 7-phase FCR circuit



(a) Piezo current waveform I_p

(b) Piezo voltage waveform V_p

(c) Harvesting current waveform I_h

(d) Negative to positive transition

(e) Positive to negative transition of V_p

Figure 2.16: 7-phase FCR waveforms

Figure 2.16d and 2.16e show waveforms zoomed into the transition. These figures show that for a negative to positive transition, the phases ϕ_1 to ϕ_7 are active (where in phase ϕ_N switches SNa and SNb are conducting), and the reverse happens in the positive to negative transition.

The flipping capacitors (C_1, C_2 and C_3) that are required for this operation have certain requirements. Firstly, the capacitance of the flipping capacitors needs to be significantly higher than the parasitic capacitance of the piezo element. This results in a more complete charge transfer from the piezo capacitance to the flipping capacitors. Secondly, the connected flipping capacitors need to be precharged to certain voltage levels. In the example above, it is assumed that C_1 is precharged to $0.75V_h$, C_2 is precharged to $0.5V_h$ and C_3 is precharged to $0.25V_h$.

It should be noted that the flipping capacitors can be realized in different ways, as shown in [30]. One of these is the Split-Phase FCR (SPFCR), where a high number of phases can be realized with a minimal amount of capacitors, by placing capacitors in series, adding more available voltage levels and therefore more phases. This results in a higher voltage flipping efficiency. This can be realized for the example by replacing capacitor C_3 by a series connection of capacitors C_1 and C_2, creating the same flipping voltage of $0.75V_h$.

Equation (2.16) holds for both the charge capturing phases (ϕ_1 to ϕ_3) and the charge releasing phases (ϕ_5 to ϕ_7) since the voltage levels are assumed to be equally spaced by V_{step}. Thus, the charge captured is equal to the charge released from C_n, and assuming that the voltage on C_n remains relatively constant (because $C_n >> C_p$), the energy that is captured by C_n is also equal to the energy released from C_n. Therefore, the energy in the system after the operation, is the same as before the operation (assuming no dynamic losses from driving the switches).

$$\Delta Q_{C_n} = C_p \cdot V_{step} \tag{2.16}$$

From this, it can be concluded that for N charge capturing steps (ϕ_1 to ϕ_4 in Figure 2.16d) and $N-1$ charge releasing steps (ϕ_3 to ϕ_7 in Figure 2.16d), a voltage flipping can be achieved without loss of energy. For this $N-1$ voltage levels are to be created with capacitors. The voltage flipping efficiency is as shown in (2.17).

$$\eta_{flip} = \frac{V_r}{V_h} = \frac{V_h - V_{step}}{V_h} = \frac{V_h - \frac{V_h}{N}}{V_h} = \frac{N-1}{N} \tag{2.17}$$

Assuming that the time taken to flip the voltage is much shorter than the period of the piezo current sinusoid ($t_{flip} \ll T$), the same equation for charge loss can be used as for the P-SSHI circuit (2.15).

HARVESTED POWER

Ideally all of the piezo current is harvested. This theoretically available power is given by (2.18). For each of the converters, in each half-cycle, some of the available current/charge per cycle is not harvested, depicted as Q_{loss}. This results in an amount of power that is not harvested (lost) as shown in (2.19). A general equation for the total harvested power P_h is then found by subtracting P_{loss} from $P_{out,max}$ as shown in (2.20). For the full wave rectifier η_{flip} is equal to -1 (as the voltage is not flipped) and for the switch only rectifier η_{flip} is equal to 0. In these equations, f_{ex} is the excitation frequency of the piezo element. Thus this is also the frequency of the piezo current I_p.

$$P_{out,max} = V_h \cdot I_{avg} = V_h \cdot I_{max} \cdot \frac{2}{\pi} \tag{2.18}$$

$$P_{loss} = 2 f_{ex} \cdot V_h \cdot Q_{loss} = 2 \cdot f_{ex} \cdot V_h \cdot C_p \cdot (1 - \eta_{flip}) \cdot V_h \tag{2.19}$$

$$P_h = P_{out,max} - P_{loss} = V_h \cdot I_{max} \cdot \frac{2}{\pi} - V_h^2 \cdot 2 \cdot f_{ex} \cdot C_p \cdot (1 - \eta_{flip}) \tag{2.20}$$

2.5.4. DC/DC CONVERTERS

As shown in Section 2.4, the output characteristics of DC harvesting sources are such that there is an optimal output voltage (the maximum power point output voltage) at which the maximum available amount of power is outputted. Generally, this is not the same voltage as the storage device. A DC-to-DC voltage conversion is required to ensure that the output voltage of the harvester is at its maximum power point (MPP) output voltage. This section discusses several examples of DC-to-DC power converters found in the literature.

CAPACITIVE AND INDUCTIVE POWER CONVERTERS

In the electrical domain, two types of elements are generally used to store or convert energy: the capacitor and the inductor. Subsequently, in the area of DC-to-DC voltage converters three main methods can be distinguished. Firstly, there are switched-capacitor power converters (SCPCs) — sometimes referred to as charge pumps — that use capacitors to convert power. Secondly, inductive power converters use inductors to convert power. A third method is using a hybrid converter in which capacitors and inductors are combined to convert power.

As off-chip components are to be avoided, on-silicon inductors have to be implemented when opting for an inductive or hybrid power converter. This introduces difficulties in terms of inductance values, series

resistance and parasitic capacitance. This is the reason that SCPCs are more suitable for integrated power conversion in low-power applications ($< 100mW$) [31].

Inductive power converters can achieve any conversion ratio (within the limits, e.g. that of the silicon technology), but this is not the case for SCPCs. For SCPCs, the number of conversion ratios and the maximum and minimum conversion ratio is limited by the amount of capacitors used [32]. Table 2.1 shows these fundamental limitations. This limits its ability to match the maximum power point voltage at the input to the output voltage.

Table 2.1: Maximum voltage conversion ratio (VCR) for given number of phases (N_ϕ) and floating capacitors (N_C) [33]

N_ϕ \ N_C	1	2	3	4
2	2	3	5	8
3	2	4	7	13
4	2	4	8	15
5	2	4	8	16

RECONFIGURABLE SCPC TOPOLOGIES

It is desirable that the maximum power point can be obtained for a wide input voltage range. Therefore, a number of conversion ratios should be achieved. If more conversion ratios are available, the MPP output voltage of the harvester can be matched with more precision, achieving a higher output power for the same input conditions. For an SCPC design with many conversion ratios, it is desired to be able to systematically reconfigure the SCPC, meaning that not individual topologies are combined by reusing switches and capacitors, but rather that individual switched capacitor cells can be configured in different ways to achieve multiple conversion ratios. Several topologies exist that are reconfigurable in this way to achieve multiple conversion ratios.

Recursive Switched Capacitor Converter

[34] presents a step-down (buck) SCPC topology that is reconfigurable to achieve $2^N - 1$ conversion ratios. This so-called 'Recursive Switched-Capacitor' (RSC) converter consist of N 2:1 switched capacitor cells with reconfigurable interconnections each containing one floating capacitor. The range of possible conversion ratios (M) is given in (2.21).

$$M = \frac{n}{2^N} \qquad n = 1,2,3,...,2^N-2,2^N-1 \tag{2.21}$$

The inverse conversion ratios can be achieved easily by substituting the input for the output and vice-versa.

Canonical Switched Capacitor Converter

[32] shows the design of a two-phase buck-boost SCPC topology that is reconfigurable to achieve a large set of conversion ratios. The design is considered to be canonical for which several requirements are given:

- "It is a reconfigurable circuit and can realize all theoretically attainable ratios." The theoretically attainable ratios are given in (2.22), where $P[k]$ and $Q[k]$ can be any number in the Fibonacci series: F_k, where $k \leq N_C + 2$ (the number of capacitor cells used).
- "The said realizations are not necessarily unique."
- "It contains the minimum number of circuit components needed". The design only takes capacitors into account for this criterion.
- "It takes the form of expandable modular blocks."

$$M = \frac{P[k]}{Q[k]} \tag{2.22}$$

This design achieves a larger set of conversion ratios than the RSC converter and the ability to boost the input voltage as well, but it does not reach the minimum and maximum conversion ratios (2^{-N} and 2^{N}). The reason is these conversion ratios can only be reached when the number of phases exceeds the number of floating capacitors (see Table 2.1).

2.6. CONCLUSION

Figure 2.17 visualizes and summarizes the choices made which led to the final design context and its challenges. The previous sections have explained why energy harvesting is a suitable way of powering IoT nodes and why solar, thermal and mechanical energy are most interesting for energy harvesting for IoT nodes. It was also found that the photovoltaic effect, the Seebeck effect and the piezoelectric effect were the most suitable for each of the energy sources. Additionally, the behaviour and challenges related to the generators for each of these effects were discussed. Lastly, power conversion techniques for the different types of harvesters were discussed.

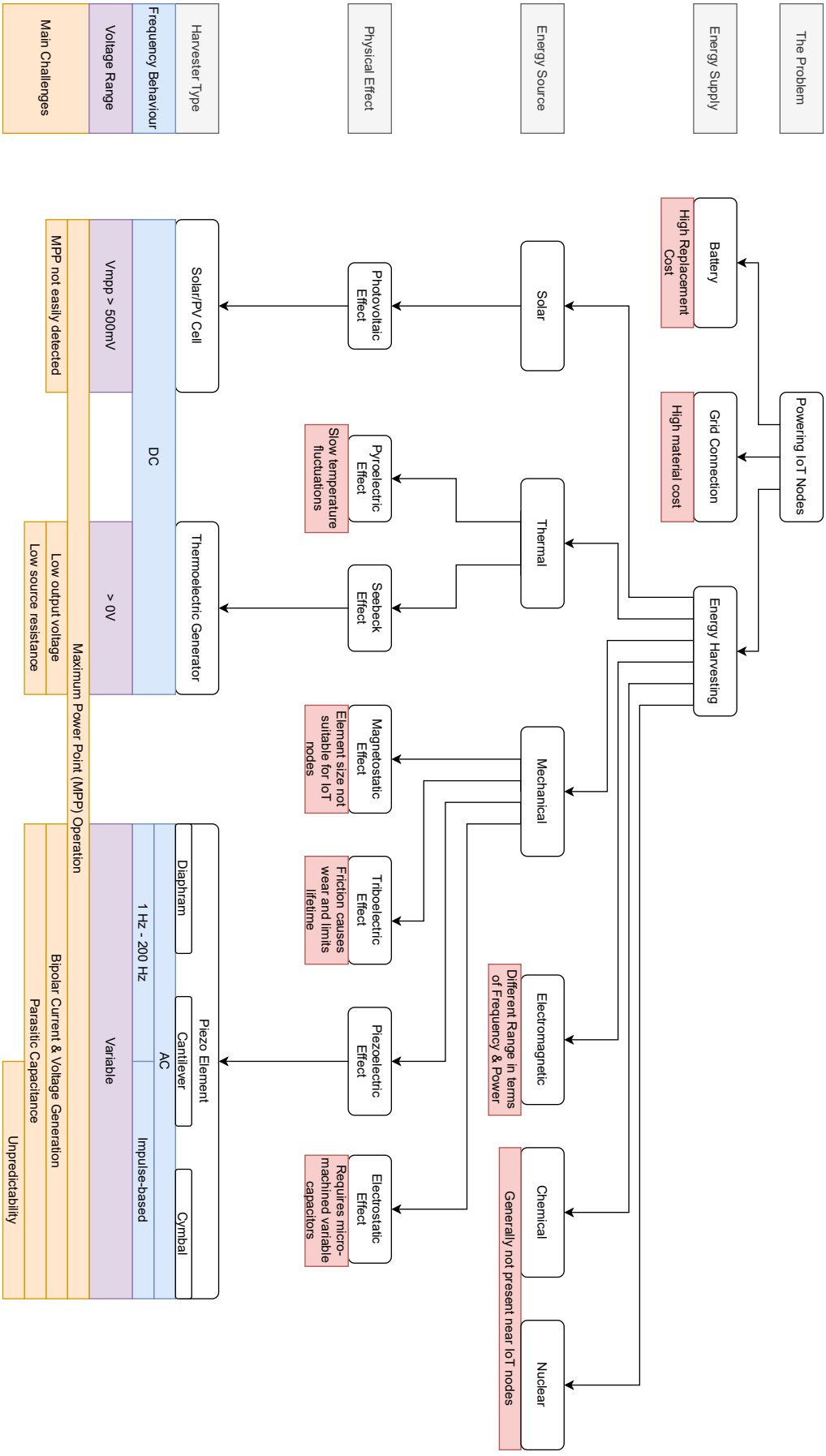


Figure 2.17: The design context flow chart

3

System Outline

3.1. Introduction

Chapter 2 has shown which harvesting sources should be supported by the PMIC, as well as the required harvesting interfaces. This chapter introduces the complete system. It discusses the design features, overview and its modelling. The subsequent chapters will elaborate on the specifics of the subsystems of the design.

3.2. Design Features

This section highlights several of the design features that are to be implemented in the system. Figure 3.1 summarizes the design choices for these features.

Voltage Conversion

A DC-to-DC voltage conversion with a configurable voltage conversion ratio is required to achieve a power conversion as close as possible to the maximum power point. The conversion ratio should be significantly high to convert the low output voltage of TEGs.

As shown in Section 2.5.4, an inductive or hybrid approach is undesirable as both require an inductor. For the capacitors used in the SCPC, three approaches are possible. Firstly, fully integrated (on-silicon) capacitors can be used, but due to their limited capacitance per area, they are unsuitable to convert a large amount of power efficiency. Secondly, off-chip capacitors can be used, but this is undesirable due to the increase in PCB footprint and number of pins. Lastly, in-package capacitors can be used in the form of minimum size SMD capacitors. These offer both a high capacitance, but no increase in PCB footprint. The downside of using these capacitors is that it complicates fabrication.

Rectification

Voltage rectification is required for compatibility with the bipolar voltage and current waveforms of the piezo element. Rectification in the electrical domain can be done using a passive diode rectifier or active bipolar switches, however this introduces a significant voltage drop. Therefore, the voltage rectification needs be done using an active MOS rectifier, which can be designed such that it introduces only a small voltage drop.

Voltage Flipping

The effects of the parasitic capacitance of piezo elements should be limited by implementing a voltage flipping circuit as shown in Section 2.5.3. A capacitor based approach is implemented in this work as the use of inductors is to be avoided. The SPFCR is used as a reference, since it optimizes voltage flipping ability for a limited number of capacitors. External (in-package) capacitors are used to fulfil the requirement that $C_n >> C_p$.

Maximum Power Point Tracking

Due to the capacitive and bipolar behaviour of piezo elements, the harvesting method for piezo elements is different from DC sources and therefore the MPPT algorithm is different from a DC MPPT algorithm[1].

[1] To reduce design complexity it is assumed that an MPPT algorithm for DC sources (PV and TEG) is implemented externally

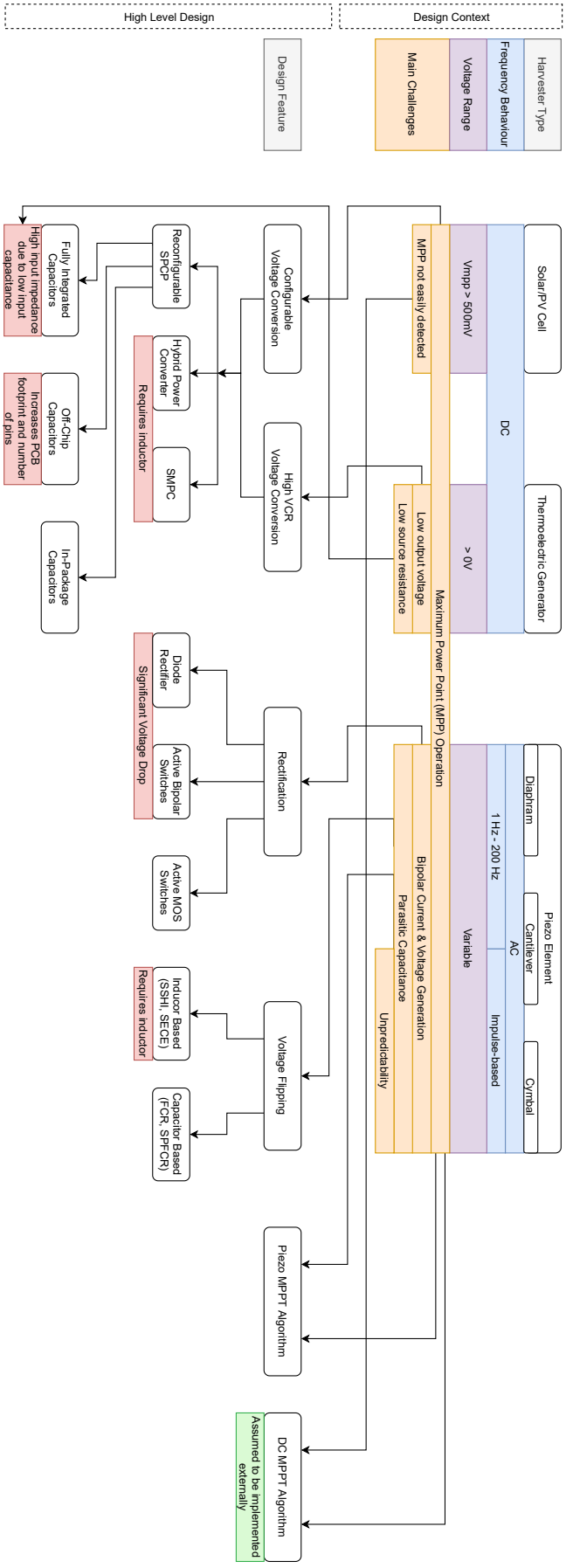


Figure 3.1: Design features flow chart

As such, an algorithm for maximum power point tracking (MPPT) of piezo elements should be developed. This also introduces a need for source differentiation, to determine which MPPT algorithm should have control over the power conversion modules.

3.3. DESIGN OVERVIEW

Figure 3.2 shows the design overview, which consists of seven subsystems. This section discusses these subsystems and their purpose shortly.

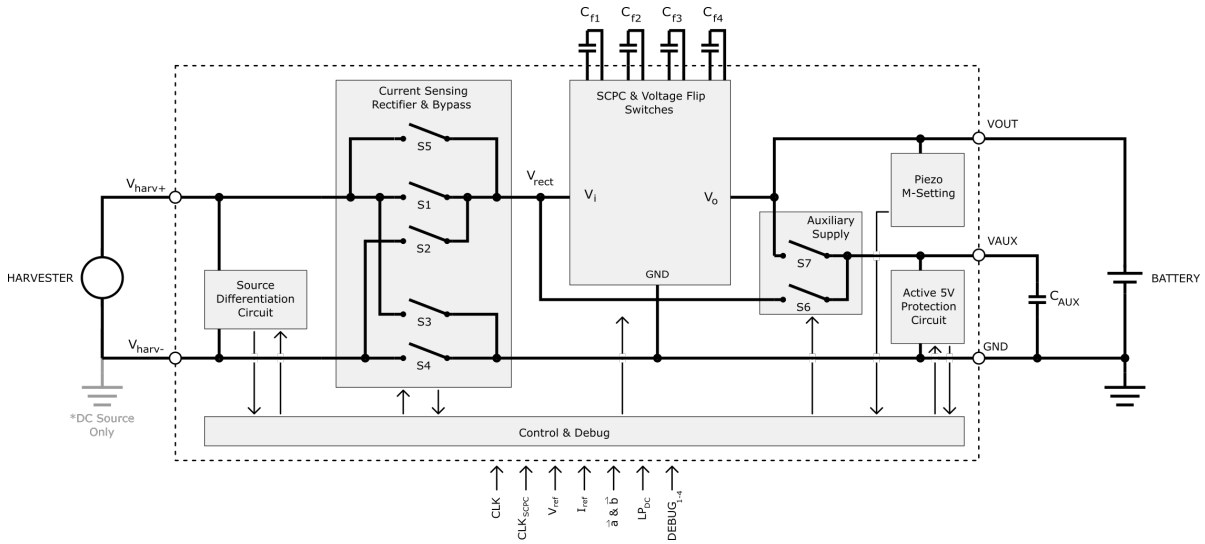


Figure 3.2: Design overview *(not shown: internal current & voltage references and supply & ground connections for subsystems)*

CONTROLLER & DEBUG

A finite state machine and other logic blocks are used to control the subsystems. External inputs for the control are the general clock signal (CLK), the clock and low-power mode enable for SCPC operations in DC source mode, a voltage reference, a current reference and $\vec{a}$ and $\vec{b}$ that are use to set the SCPC conversion ratio when a DC source is connected. Additionally, a debug module enables the user to manipulate the normal operation of the system to improve the testability of the design.

SOURCE DIFFERENTIATION CIRCUIT

The PMIC requires different types of operations for the two different types of sources (piezo element sources and DC sources). For this reason, a source differentiation circuit is required. This subsystem receives an enable from the controller and outputs a signal that denotes whether a DC source of piezo source is connected.

CURRENT SENSING RECTIFIER & BYPASS

Switches $S1$ to $S4$ make up the full bridge rectifier, that rectifies the harvester voltage in case a piezo element is attached. It receives controlling signals from the controller and outputs a signal that specifies the sign of the current through the rectifier, as this is required to detect a zero-current crossing (ZCC), which is required for the voltage flipping operations. Switch $S5$ is used to bypass the rectifier, providing a conduction path with a lower resistance between V_{harv+} and V_{rect} in case a DC source is attached.

SCPC & VOLTAGE FLIP SWITCHES

This subsystem contains the switches that are used in the SCPC and during the voltage flipping operations. The external floating capacitors C_{f1} to C_{f4} and 22 of the 28 switches make up the SCPC and preform the voltage conversion between the (rectified) harvester voltage and the battery voltage. The six additional switches are implemented, such that any series connection of the floating capacitors can be presented at the input terminal, which provides the voltage steps for the voltage flipping operation. A signal for each switch is send by the controller.

AUXILIARY SUPPLY

The auxiliary supply selects either the input or output of the SCPC to be the highest voltage in the circuit. For this, either switch $S6$ or switch $S7$ connects an external capacitor to the proper SCPC terminal, based on a signal from the controller. This circuit is required for ESD protection purposes (see Section 4.5.2) and for presenting an input capacitance to the SCPC when a piezo element source is attached (see Section) 5.8).

ACTIVE 5V PROTECTION

This circuit ensures that the highest voltage in the circuit (the voltage of the auxiliary supply) does not exceed the $5V$ limit, which is imposed by the use of $5V$ tolerant devices. If this voltage is exceeded, it is able to sink current from the auxiliary supply node, such that the voltage drops. The subsystem may receive an input from the controller to disable this feature and outputs a signal which informs the controller when this over-voltage protection mechanism is activated.

PIEZO M-SETTING

This subsystem implements the MPPT algorithm for piezo energy harvesting. It sends the controller the conversion ratio (M) that is required for efficient energy conversion. The optimal conversion ratio is determined by the voltage of the connected battery.

3.4. DESIGN MODELLING

The modelling of the design is an important step in the design procedure. It does not only give an insight in the expected performance of the design, but also enables optimization of circuit parameters and awareness of the trade-offs that come with the design. For this design, equivalent models of subsystems are established and combined to model the complete design.

Figures 3.3a and 3.3b shows the equivalent models for a linear DC source (TEG) and piezo element source respectively. The equivalent circuits for both harvesting elements were used, as found in Section 2.4. The rectifier and bypass are characterized by the on-resistances of the transistors used and Chapter 4 develops a model for the SCPC. Lastly, the current consumption of the logic and other support subsystems is taken from the battery. The developed model is used to optimize the design and estimate its performance, which is compared to simulation results in Chapter 7. MATLAB is used to evaluate these equivalent circuits for a range of operating conditions.

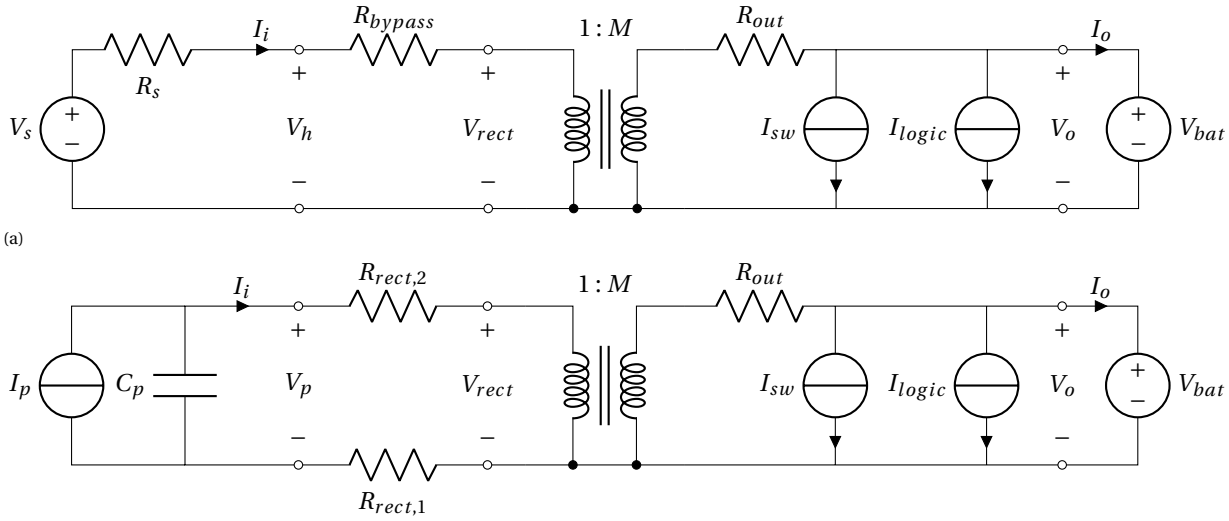


Figure 3.3: Equivalent model for DC source mode (a) and piezo source mode (b)

3.5. LAYOUT

Figure 3.4 shows the layout of the designed integrated circuit. The active die area (chip area excluding the padring) measures $1360\mu m$ by $1560\mu m$ for a total area of $2.12mm^2$. The full chip measures $1600\mu m$ by $1800\mu m$ for a total area of $2.88mm^2$.

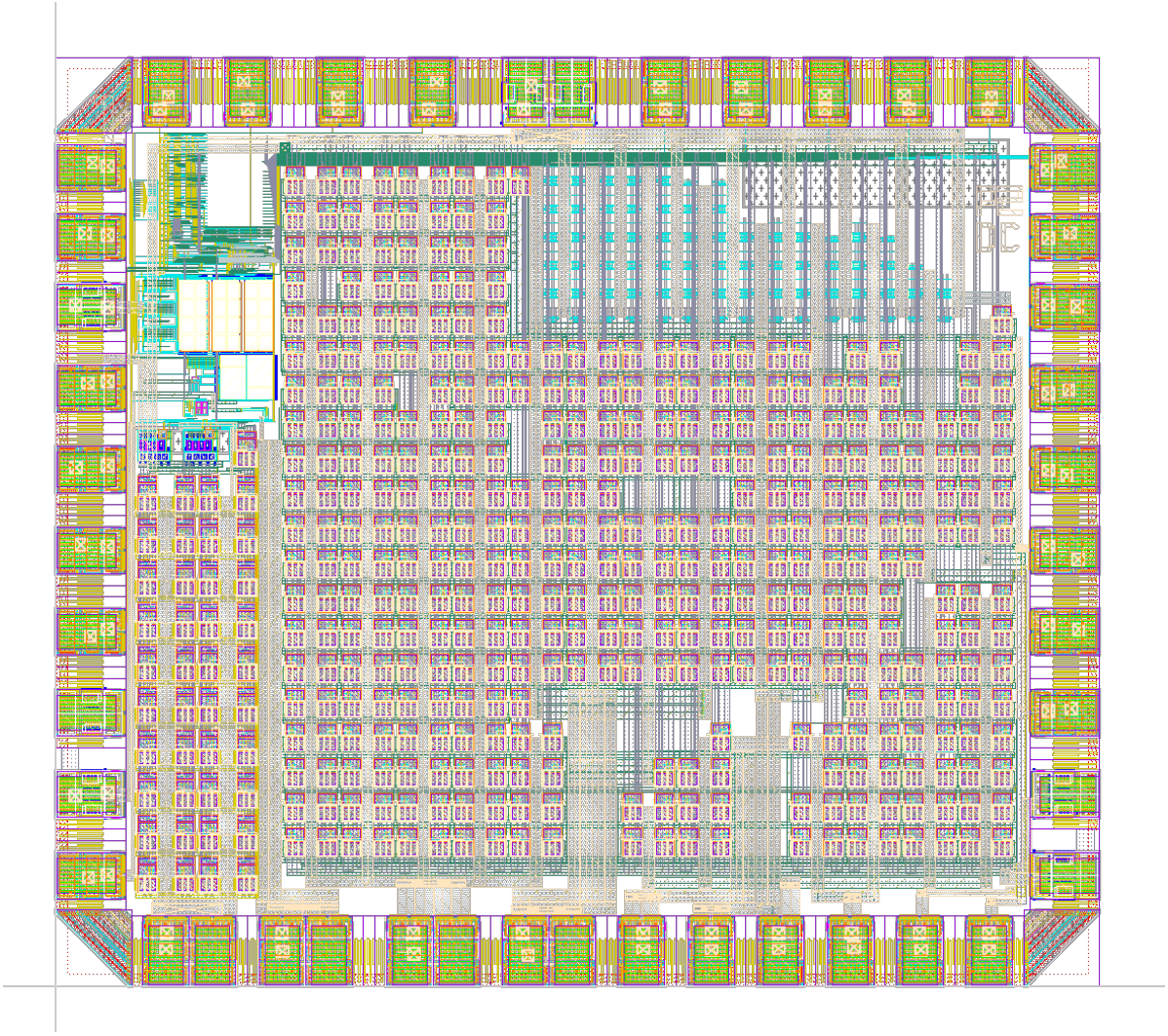


Figure 3.4: Layout of the designed integrated circuit

3.6. CONCLUSION

This concludes the system outline in which the design features and overview of the subsystems were given. Additionally, the importance of modelling the design was highlighted.

The following chapters will describe the design procedure and implementation in detail. Chapter 4 discusses the design and implementation of the SCPC, including the auxiliary supply and over-voltage protection circuits. Chapter 5 shows the combined design and implementation of the rectifier and voltage flipping operation, as well as the conversion ratio setting circuit for piezo element harvesting. Lastly, Chapter 6 discusses the control and debug design, including the source differentiation circuit.

4

SCPC Design

4.1. Introduction

This chapter discussed the design of a novel switched-capacitor power converter (SCPC). Firstly, the SCPC topology and its analysis are discussed. Secondly, the implementation of the design is discussed. Lastly, two protection circuits are added and the chapter is concluded.

Modelling and Optimization

In the design procedure, multiple types of losses are considered to evaluate and optimize the design, such that the output power is maximized. These losses have been visualized in Figure 4.1. The behaviour of the system is analysed with equivalent circuits, which includes these losses:

- The first type of output power reduction is MPP mismatch, in which the power converter is configured such that the less than the MPP power flows into the power converter.
- The second power loss is conduction losses in the SCPC: power loss due to the finite resistance of the switches and the transfer of charge between the capacitors in the SCPC.
- Thirdly, the switches in SCPC (CMOS devices) require power to turn on and off as the gates of the CMOS devices need to be charged and discharged in this process.
- Lastly, losses in the control circuit eat away at the power provided by the source.

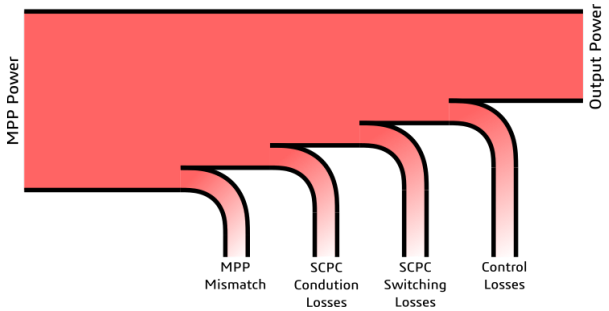


Figure 4.1: Power lost in a harvesting setup with an SCPC

Average Model for SCPCs

In [35] an equivalent model is given that describes the DC behaviour of a switched capacitor power converter, in which M is the voltage gain or conversion ratio and R_{out} is the output resistance that is associated with the voltage drop and some of the energy loss in the converter. The model is shown in Figure 4.2. This model and the equivalent models of the harvesters will be used to evaluate the performance of the SCPC.

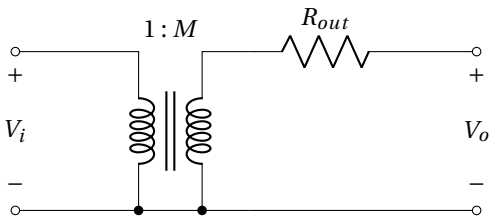


Figure 4.2: SCPC Average Model

4.2. TOPOLOGY AND ANALYSIS

This section discusses the topology and analysis of the novel SCPC.

4.2.1. 5-PHASE SCPC

One of the requirements for the power converter is that a high conversion ratio is achieved (see Section 3.1). It has been shown that a larger number of capacitors will give a higher maximum achievable conversion ratio (Table 2.1). However, design complexity and footprint increases with the number of capacitors. Regarding this trade-off, it is decided that there are four floating capacitors are available for the SCPC. In order to achieve the maximum conversion ratio ($M = 16$) for four floating capacitors, a 5-phase SCPC is required.

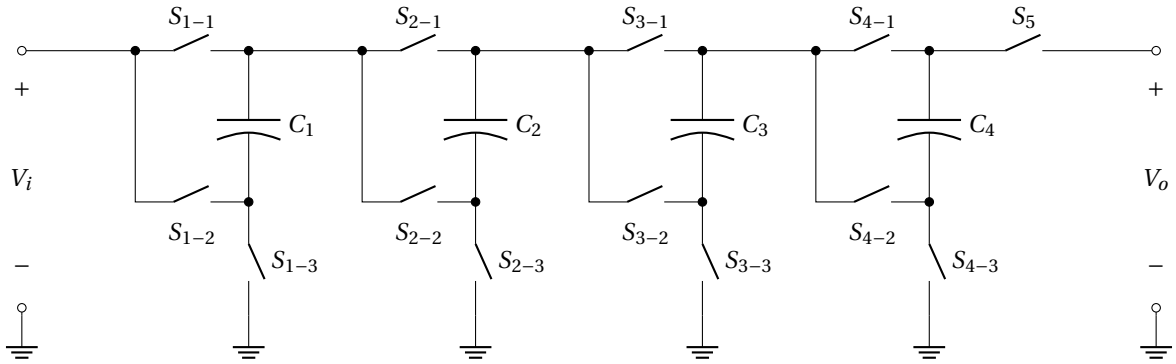


Figure 4.3: SCPC Circuit for $M = 16$

Table 4.1: Switch activation for the 5-phase $M = 16$-SCPC (1 = closed; 0 = open)

SC Cell:	1		3		3		4		
Switch / ϕ	S_{1-1} S_{1-3}	S_{1-2}	S_{2-1} S_{2-3}	S_{2-2}	S_{3-1} S_{3-3}	S_{3-2}	S_{4-1} S_{4-3}	S_{4-2}	S_5
1	1	0	0	0	0	0	0	0	0
2	0	1	1	0	0	0	0	0	0
3	0	1	0	1	1	0	0	0	0
4	0	1	0	1	0	1	1	0	0
5	0	1	0	1	0	1	0	1	1

It is desirable to at least attain the maximum conversion ratio. A converter that achieves this, is given in Figure 4.3. Following the switch activation scheme given in Table 4.1, the charge flows in the SCPC can be defined (also shown in Figure A.4 in Appendix A.3). Assuming a steady state condition, the net charge through a floating capacitor should be zero ($\sum q_{C_i} = 0$). The following charge equalities can be defined:

$$\sum q_{C_4} = q_4 - q_5 = 0 \tag{4.1}$$

$$\sum q_{C_3} = q_3 - q_4 - q_5 = 0 \tag{4.2}$$

$$\sum q_{C_2} = q_2 - q_3 - q_4 - q_5 = 0 \tag{4.3}$$

$$\sum q_{C_1} = q_1 - q_2 - q_3 - q_4 - q_5 = 0 \tag{4.4}$$

From (4.1) to (4.4), it can be concluded that:

$$q_4 = q_5 \tag{4.5}$$

$$q_3 = 2 \cdot q_5 \tag{4.6}$$

$$q_2 = 4 \cdot q_5 \tag{4.7}$$

$$q_1 = 8 \cdot q_5 \tag{4.8}$$

From (4.5) to (4.8), it can be concluded that:

$$q_i = q_1 + q_2 + q_3 + q_4 + q_5 = 16 \cdot q_5 \tag{4.9}$$

$$q_o = q_5 \tag{4.10}$$

Assuming a lossless conversion, where $V_i \cdot q_i = V_o \cdot q_o$, the conversion ratio ($M$ in the average model) can be found:

$$M = \frac{V_o}{V_i} = \frac{q_i}{q_o} = \frac{16 \cdot q_5}{q_5} = 16 \tag{4.11}$$

With this charge flow analysis, it has been proven that a conversion ratio of $M = 16$ is achieved indeed.

4.2.2. INCREASED RECONFIGURABILITY

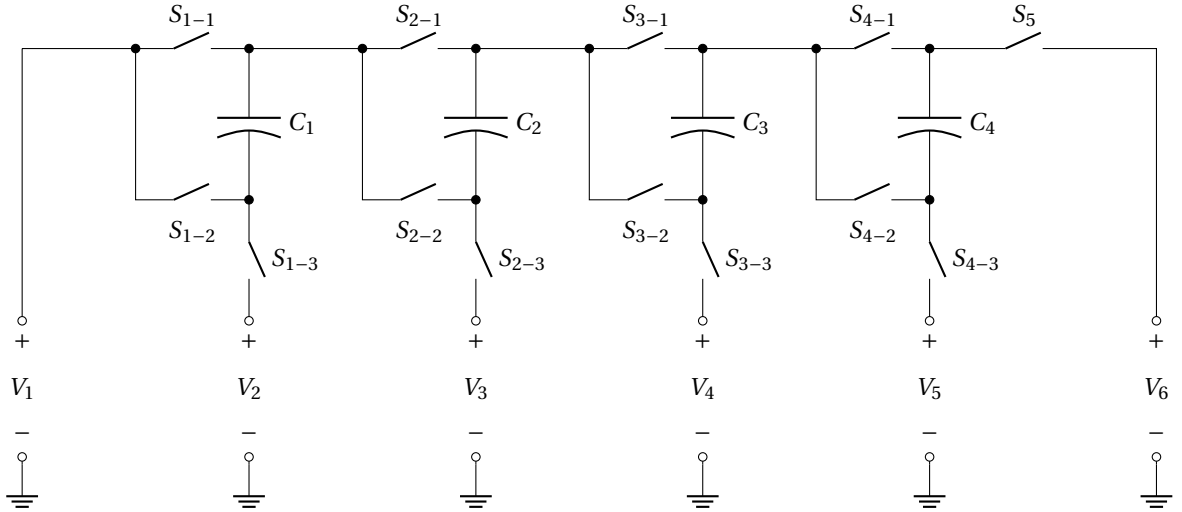


Figure 4.4: Highly configurable SCPC Circuit

Inspired by [32], the SCPC can be made highly configurable by manipulating the available voltage nodes. Figure 4.4 shows the SCPC with manipulative voltage nodes. The same switch activation scheme is applied, therefore the same charge flows are present. Equations (4.12) to (4.17) show the charge flowing *into* the respective nodes.

$$q_{N1} = -16 \cdot q_5 \tag{4.12}$$

$$q_{N2} = 8 \cdot q_5 \tag{4.13}$$

$$q_{N3} = 4 \cdot q_5 \tag{4.14}$$

$$q_{N4} = 2 \cdot q_5 \tag{4.15}$$

$$q_{N5} = q_5 \tag{4.16}$$

$$q_{N6} = q_5 \tag{4.17}$$

The charges that have been found can now be chosen to be part of the input charge, the output charge or ground charge by connecting the respective node to V_i, V_o or ground. Now q_i, q_o and M are as follows:

$$q_i = \vec{a} \bullet [16q_5, -8q_5, -4q_5, -2q_5, -q_5, -q_5] \tag{4.18}$$

$$q_o = \vec{b} \bullet [-16q_5, 8q_5, 4q_5, 2q_5, q_5, q_5] \tag{4.19}$$

$$M = \frac{q_i}{q_o} = \frac{\vec{a} \bullet [16, -8, -4, -2, -1, -1] \cdot q_5}{\vec{b} \bullet [-16, 8, 4, 2, 1, 1] \cdot q_5} = -\frac{\vec{a} \bullet \vec{q}_r}{\vec{b} \bullet \vec{q}_r} \tag{4.20}$$

Vectors $\vec{a}$ and $\vec{b}$ are logical vectors that are made up of logical components $a_1 \rightarrow a_6$ and $b_1 \rightarrow b_6$ respectively. $a_n = 1$ if voltage node V_n is connected to V_i and $a_n = 0$ otherwise. $b_n = 1$ if voltage node V_n is connected to V_o and $b_n = 0$ otherwise. Both values cannot be one, as a voltage node should not be connected to V_i and V_o at the same time. If voltage node V_n is connected to ground, both a_n and b_n are zero. $\vec{q}_r$ is the vector of relative charge flows: $[16, -8, -4, -2, -1, -1]$.

Voltage node V_n can be connected to one of the three possible nodes. This creates (6^3 =) 729 theoretical configurations. An analysis in MATLAB has shown that 178 unique conversion ratio are found, of which 119 give a positive conversion ratio. A complete list of the positive conversion ratios can be found in Table 4.2.

Table 4.2: List of positive conversion ratios for the designed SCPC

$\frac{1}{16}$	$\frac{1}{15}$	$\frac{1}{14}$	$\frac{1}{13}$	$\frac{1}{12}$	$\frac{1}{11}$	$\frac{1}{10}$	$\frac{1}{9}$	$\frac{1}{8}$	$\frac{2}{15}$	$\frac{1}{7}$	$\frac{1}{6}$	$\frac{2}{11}$	$\frac{3}{16}$	$\frac{1}{5}$
$\frac{1}{4}$	$\frac{4}{15}$	$\frac{3}{11}$	$\frac{2}{7}$	$\frac{4}{13}$	$\frac{5}{16}$	$\frac{1}{3}$	$\frac{5}{14}$	$\frac{3}{8}$	$\frac{5}{13}$	$\frac{2}{5}$	$\frac{3}{7}$	$\frac{7}{16}$	$\frac{7}{15}$	$\frac{1}{2}$
$\frac{8}{15}$	$\frac{9}{16}$	$\frac{4}{7}$	$\frac{3}{5}$	$\frac{8}{13}$	$\frac{5}{8}$	$\frac{9}{14}$	$\frac{2}{3}$	$\frac{11}{16}$	$\frac{9}{13}$	$\frac{5}{7}$	$\frac{8}{11}$	$\frac{11}{15}$	$\frac{3}{4}$	$\frac{4}{5}$
$\frac{13}{16}$	$\frac{9}{11}$	$\frac{5}{6}$	$\frac{6}{7}$	$\frac{13}{15}$	$\frac{7}{8}$	$\frac{8}{9}$	$\frac{9}{10}$	$\frac{10}{11}$	$\frac{11}{12}$	$\frac{12}{13}$	$\frac{13}{14}$	$\frac{14}{15}$	$\frac{15}{16}$	$\frac{1}{1}$
$\frac{16}{15}$	$\frac{15}{14}$	$\frac{14}{13}$	$\frac{13}{12}$	$\frac{12}{11}$	$\frac{11}{10}$	$\frac{10}{9}$	$\frac{9}{8}$	$\frac{8}{7}$	$\frac{15}{13}$	$\frac{7}{6}$	$\frac{6}{5}$	$\frac{11}{9}$	$\frac{16}{13}$	$\frac{5}{4}$
$\frac{4}{3}$	$\frac{15}{11}$	$\frac{11}{8}$	$\frac{7}{5}$	$\frac{13}{9}$	$\frac{16}{11}$	$\frac{3}{2}$	$\frac{14}{9}$	$\frac{8}{5}$	$\frac{13}{8}$	$\frac{5}{3}$	$\frac{7}{4}$	$\frac{16}{9}$	$\frac{15}{8}$	$\frac{2}{1}$
$\frac{15}{7}$	$\frac{16}{7}$	$\frac{7}{3}$	$\frac{5}{2}$	$\frac{13}{5}$	$\frac{8}{3}$	$\frac{14}{5}$	$\frac{3}{1}$	$\frac{16}{5}$	$\frac{13}{4}$	$\frac{7}{2}$	$\frac{11}{3}$	$\frac{15}{4}$	$\frac{4}{1}$	$\frac{5}{1}$
$\frac{16}{3}$	$\frac{11}{2}$	$\frac{6}{1}$	$\frac{7}{1}$	$\frac{15}{2}$	$\frac{8}{1}$	$\frac{9}{1}$	$\frac{10}{1}$	$\frac{11}{1}$	$\frac{12}{1}$	$\frac{13}{1}$	$\frac{14}{1}$	$\frac{15}{1}$	$\frac{16}{1}$	

It can be observed that the conversion ratios larger than 1 are the inverse of the conversion ratios smaller than 1. It is also found that the set of the fractions smaller than or equal to 1 is a subset of the Farey sequence of the order 16 (see Table 4.3). Although any denominator or numerator can be made with $\vec{a} \bullet \vec{q}_r$ and $\vec{b} \bullet \vec{q}_r$, the full Farey sequence is not available for this converter. This limitation is caused by the fact that $a_n = 1$ & $b_n = 1$ cannot give a valid configuration. A total of 12 non-zero fraction from the Farey sequence are not part of the list of positive conversion ratios.

Table 4.3: Elements in the Farey Sequence of the order 16

$\frac{0}{1}$	$\frac{1}{16}$	$\frac{1}{15}$	$\frac{1}{14}$	$\frac{1}{13}$	$\frac{1}{12}$	$\frac{1}{11}$	$\frac{1}{10}$	$\frac{1}{9}$	$\frac{1}{8}$	$\frac{2}{15}$	$\frac{1}{7}$	$\frac{2}{13}$	$\frac{1}{6}$	$\frac{2}{11}$
$\frac{3}{16}$	$\frac{1}{5}$	$\frac{3}{14}$	$\frac{2}{9}$	$\frac{3}{13}$	$\frac{1}{4}$	$\frac{4}{15}$	$\frac{3}{11}$	$\frac{2}{7}$	$\frac{3}{10}$	$\frac{4}{13}$	$\frac{5}{16}$	$\frac{1}{3}$	$\frac{5}{14}$	$\frac{4}{11}$
$\frac{3}{8}$	$\frac{5}{13}$	$\frac{2}{5}$	$\frac{5}{12}$	$\frac{3}{7}$	$\frac{7}{16}$	$\frac{4}{9}$	$\frac{5}{11}$	$\frac{6}{13}$	$\frac{7}{15}$	$\frac{1}{2}$	$\frac{8}{15}$	$\frac{7}{13}$	$\frac{6}{11}$	$\frac{5}{9}$
$\frac{9}{16}$	$\frac{4}{7}$	$\frac{7}{12}$	$\frac{3}{5}$	$\frac{8}{13}$	$\frac{5}{8}$	$\frac{7}{11}$	$\frac{9}{14}$	$\frac{2}{3}$	$\frac{11}{16}$	$\frac{9}{13}$	$\frac{7}{10}$	$\frac{5}{7}$	$\frac{8}{11}$	$\frac{11}{15}$
$\frac{3}{4}$	$\frac{10}{13}$	$\frac{7}{9}$	$\frac{11}{14}$	$\frac{4}{5}$	$\frac{13}{16}$	$\frac{9}{11}$	$\frac{5}{6}$	$\frac{11}{13}$	$\frac{6}{7}$	$\frac{13}{15}$	$\frac{7}{8}$	$\frac{8}{9}$	$\frac{9}{10}$	$\frac{10}{11}$
$\frac{11}{12}$	$\frac{12}{13}$	$\frac{13}{14}$	$\frac{14}{15}$	$\frac{15}{16}$	$\frac{1}{1}$									

SWITCH ARRANGEMENT

In the implementation, V_n is connected to V_i, V_o or ground with the help of three separate switches. Figure 4.5 shows the circuit schematic for the SCPC derived from Figure 4.4. Connection from node $N1$ and $N6$ to ground were not required to realise all positive conversion ratios, and were therefore omitted in the implementation.

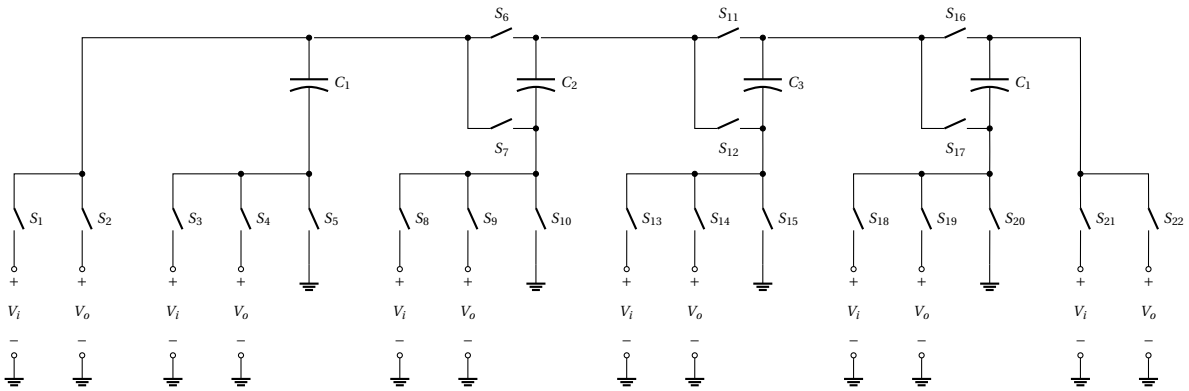


Figure 4.5: Implementation of the highly configurable SCPC Circuit

4.2.3. LOSS ANALYSIS

For this highly configurable SCPC, two types of losses are considered: conduction losses (as shown in the average model) and switching losses.

CONDUCTION LOSSES

The conduction losses in the two types elements (capacitors & switch on-resistances) are considered create two independent types of conduction losses in two limits: The Slow Switching Limit (SSL) and the Fast Switching Limit (FSL) [36].

Slow Switching Limit: R_{SSL}

The SSL losses are characterized by the charging and discharging of the capacitors. The energy lost in charging a capacitor from a different potential (e.g. a voltage source or a second capacitor) is dependent on the charge flow through the capacitor (q) and the capacitance value (C) as shown in (4.21). The losses for each capacitor and each phase are summed to find the total energy loss in one switching cycle in (4.22). The SSL conduction losses are found in (4.23), where T_{sw} is the time taken for one switching cycle and $f_{sw} = T_{sw}^{-1}$.

$$E_{loss_C} = \frac{1}{2} \cdot \frac{q^2}{C} \tag{4.21}$$

$$\begin{aligned} E_{SSL} &= \sum_{i=1}^{N_C} \sum_{\phi=1}^{N_\phi} \left(\frac{1}{2} \cdot \frac{q_{C_i,\phi}^2}{C_i} \right) \\ &= \frac{1}{2} \cdot \left(\frac{\Sigma_{\phi=1}^{5} q_\phi^2}{C_1} + \frac{\Sigma_{\phi=2}^{5} q_\phi^2}{C_2} + \frac{\Sigma_{\phi=3}^{5} q_\phi^2}{C_3} + \frac{\Sigma_{\phi=4}^{5} q_\phi^2}{C_4} + \right) \\ &= \frac{1}{2} \cdot \left(\frac{86 \cdot q_5^2}{C_1} + \frac{22 \cdot q_5^2}{C_2} + \frac{6 \cdot q_5^2}{C_3} + \frac{2 \cdot q_5^2}{C_4} \right) \\ &= q_5^2 \cdot \left(\frac{43}{C_1} + \frac{11}{C_2} + \frac{3}{C_3} + \frac{1}{C_4} \right) \end{aligned} \tag{4.22}$$

$$\begin{aligned} R_{SSL} &= \frac{E_{SSL}}{T_{sw} \cdot I_{out}^2} = \frac{E_{SSL} \cdot T_{sw}}{q_{out}^2} = \frac{E_{SSL}}{f_{sw} \cdot q_{out}^2} \\ &= \frac{q_5^2}{f_{sw} \cdot q_{out}^2} \cdot \left(\frac{43}{C_1} + \frac{11}{C_2} + \frac{3}{C_3} + \frac{1}{C_4} \right) \\ &= \frac{1}{f_{sw} \cdot (\vec{b} \bullet \vec{q}_r)^2} \left(\frac{43}{C_1} + \frac{11}{C_2} + \frac{3}{C_3} + \frac{1}{C_4} \right) \end{aligned} \tag{4.23}$$

Two scenarios are considered for the determination of capacitor sizes: limited total floating capacitance and limited individual floating capacitance.

A limit on the total floating capacitance may be present when on-silicon capacitors are considered, but this is not the case in this design. A limit on total floating capacitance could also be present when a certain SCPC settling time is required, for example, for an MPPT algorithm. Since the DC MPPT algorithm is not considered in this design, it is assumed that there is no limit on the total floating capacitance.

However, a limit on the individual floating capacitance is present in this design. An solution which can be integrated one package is preferred for this design. Therefore, a maximum individual capacitance of $1\mu F$ is assumed, as this allows the option to bond-wire gold-plated SMD capacitor with a size of $1mm$ by $0.5mm$ to the IC inside the package [37]. Equation (4.24) describes the minimal SSL conduction resistance, where C_f is the capacitance of one floating capacitor.

$$R_{SSL} = \frac{58}{C_f \cdot f_{sw}} \cdot \left(\vec{b} \bullet \vec{q}_r\right)^{-2} \tag{4.24}$$

Fast Switching Limit: R_{FSL}

The FSL losses are characterized by the on-resistance of the switches that are used. The FSL losses are dominant over the SSL losses for higher switching frequencies, because the charging and discharging of the capacitors is limited by the on-resistance of the involved switches. The conduction losses occur because of the charge flow through the equivalent on-resistances of the switching devices. Equation 4.25 shows the energy that is lost in one cycle in the fast switching limit. $R_{eq,\phi}$ is the sum of switch resistances that q_ϕ encounters. T_ϕ is the total time of phase ϕ. $r_{T,\phi}$ is the phase time taken for phase ϕ relative to the total time for taken for all 5 phases (T_{sw}). $r_{q,\phi}$ is the charge in phase ϕ relative to q_5: $\vec{r_q} = [8,4,2,1,1]$. R_{eq} is the sum of switch resistances that q_ϕ encounters. This is dependent on the switch configuration ($\vec{a}$ and $\vec{b}$) that is used.

$$E_{FSL} = \sum_{\phi=1}^{N_\phi} \left(R_{eq,\phi} \cdot \frac{q_\phi^2}{T_\phi} \right) = \frac{q_5^2}{T_{sw}} \cdot \sum_{\phi=1}^{N_\phi} \left(R_{eq,\phi} \cdot \frac{r_q^2}{r_{T,\phi}} \right) \tag{4.25}$$

$$R_{FSL} = \frac{E_{FSL}}{T_{sw} \cdot I_{out}^2} = \frac{E_{FSL} \cdot T_{sw}}{q_{out}^2} = \frac{q_5^2}{q_{out}^2} \cdot \sum_{\phi=1}^{N_\phi} \left(R_{eq,\phi} \cdot \frac{r_q^2}{r_{T,\phi}} \right) = \left(-\vec{b} \bullet \vec{q}_r\right)^{-2} \cdot \sum_{\phi=1}^{N_\phi} \left(R_{eq,\phi} \cdot \frac{r_q^2}{r_{T,\phi}} \right) \tag{4.26}$$

The five relative phase times are considered to be equal to each other ($r_{T,i} = 0.2$), such that the FSL resistance is shown by (4.27):

$$R_{FSL} = 5 \cdot \left(\vec{b} \bullet \vec{q}_r\right)^{-2} \cdot \sum_{\phi=1}^{N_\phi} \left(R_{eq,\phi} \cdot r_q^2 \right) \tag{4.27}$$

$\vec{c}$ shows whether node V_i is connected to ground and is mathematically defined as: $\vec{c} = 1 - \vec{a} - \vec{b}$. The components of the sum of equivalent resistances can be written out as follows:

$$R_{eq,1} = R_1 \cdot a_1 + R_2 \cdot b_1 + R_3 \cdot a_2 + R_4 \cdot b_2 + R_5 \cdot c_2 \tag{4.28}$$

$$R_{eq,2} = R_3 \cdot a_1 + R_4 \cdot b_1 + R_6 + R_8 \cdot a_3 + R_9 \cdot b_3 + R_{10} \cdot c_3 \tag{4.29}$$

$$R_{eq,3} = R_3 \cdot a_1 + R_4 \cdot b_1 + R_7 + R_{11} + R_{13} \cdot a_4 + R_{14} \cdot b_4 + R_{15} \cdot c_4 \tag{4.30}$$

$$R_{eq,4} = R_3 \cdot a_1 + R_4 \cdot b_1 + R_7 + R_{12} + R_{16} + R_{18} \cdot a_5 + R_{19} \cdot b_5 + R_{20} \cdot c_5 \tag{4.31}$$

$$R_{eq,5} = R_3 \cdot a_1 + R_4 \cdot b_1 + R_7 + R_{12} + R_{17} + R_{21} \cdot a_6 + R_{22} \cdot b_6 \tag{4.32}$$

Equation (4.27) can be rewritten to include the individual on-resistances of the switches where the on-resistance of switch S_i is noted as R_i:

$$
\begin{aligned}
R_{FSL} &= 5 \cdot \left(\vec{b} \bullet \vec{q}_r\right)^{-2} \cdot (64 \cdot R_{eq,1} + 16 \cdot R_{eq,2} + 4 \cdot R_{eq,3} + R_{eq,4} R_{eq,5}) \\
&= 5 \cdot \left(\vec{b} \bullet \vec{q}_r\right)^{-2} \cdot (\\
&\quad R_1 \cdot 64 \cdot a_1 + R_2 \cdot 64 \cdot b_1 \\
&\quad + R_3 \cdot (22 \cdot a_1 + 64 \cdot a_2) + R_4 (22 \cdot b_1 + 64 \cdot b_2) + R_5 \cdot 64 \cdot c_2 \\
&\quad + R_6 \cdot 16 + R_7 \cdot 6 + R_8 \cdot 16 \cdot a_3 + R_9 \cdot 16 \cdot b_3 + R_{10} \cdot 16 \cdot c_3 \\
&\quad + R_{11} \cdot 4 + R12 \cdot 2 + R_{13} \cdot 2 \cdot a_4 + R_{14} \cdot 2 \cdot b_4 + R_{15} \cdot 2 \cdot c_4 \\
&\quad + R16 + R17 + R_{18} \cdot a_5 + R_{19} \cdot b_5 + R_{20} \cdot c_5 \\
&\quad + R_{21} \cdot a_6 + R_{22} \cdot b_6)
\end{aligned}
\tag{4.33}
$$

The total cumulative switch resistance ($R_{sw,t}$) can be decoupled from the equation by using relative switch sizes instead: x_i is the relative size of switch S_i and (assuming the on-resistance of a switch is inversely proportional to the size of that switch) the on-resistance of switch S_i relative to the total switch resistance $R_{sw,t}$ is x_i^{-1}. The newly defined R_{FSL} is shown in (4.34).

$$
R_{FSL} = R_{sw,t} \cdot 5 \cdot f(\vec{a}, \vec{b}, \vec{x}) \tag{4.34}
$$

$$
\begin{aligned}
f(\vec{a}, \vec{b}, \vec{x}) = \cdot \left(\vec{b} \bullet \vec{q}_r\right)^{-2} \cdot (\quad & \frac{64 \cdot a_1}{x_1} + \frac{64 \cdot b_1}{x_2} \\
& + \frac{22 \cdot a_1 + 64 \cdot a_2}{x_3} + \frac{22 \cdot b_1 + 64 \cdot b_2}{x_4} + \frac{64 \cdot c_2}{x_5} \\
& + \frac{16}{x_6} + \frac{6}{x_7} + \frac{16 \cdot a_3}{x_8} + \frac{16 \cdot b_3}{x_9} + \frac{16 \cdot c_3}{x_{10}} \\
& + \frac{4}{x_{11}} + \frac{2}{x_{12}} + \frac{2 \cdot a_4}{x_{13}} + \frac{2 \cdot b_4}{x_1 4} + \frac{2 \cdot c_4}{x_{15}} \\
& + \frac{1}{x_{16}} + \frac{1}{x_{17}} + \frac{a_5}{x_{18}} + \frac{b_5}{x_{19}} + \frac{c_5}{x_{20}} \\
& + \frac{a_6}{x_{21}} + \frac{b_6}{x_{22}})
\end{aligned}
\tag{4.35}
$$

The FSL resistance can be optimized by minimizing (4.35). This is done by finding the optimal distribution of switch sizes relative to the total cumulative switch size ($\vec{x}$). The dependency on $\vec{a}$ and $\vec{b}$ complicates the optimization of relative switch sizes. In order to incorporate every configuration into the optimization, it was chosen that the sum of $f(\vec{a}, \vec{b}, \vec{x})$ across all 119 conversion ratio settings is minimized, while satisfying the condition that the sum of the area is equal to the total switch area. This minimization is shown in (4.36), where n is the nth conversion ratio setting of the SCPC. The complete list for conversion ratio settings can be found in Appendix A.5. For scenarios where multiple $\vec{a}$ and $\vec{b}$ settings would yield the same conversion ratio, the setting with the highest absolute value for $(\vec{b} \bullet \vec{q}_r)$ was used, such that the lowest R_{FSL} would be achieved.

$$
\min_{\sum_{i=1}^{22} x_i = 1} \left(\sum_{n=1}^{119} f_n \right) \tag{4.36}
$$

$$
\sum_{n=1}^{119} f_n = \sum_{i=1}^{22} \frac{v_i}{x_i} \tag{4.37}
$$

$$
\min_{\sum_{i=1}^{22} x_i = 1} \left(\sum_{i=1}^{22} \frac{v_i}{x_i} \right) \tag{4.38}
$$

Equations (4.37) and (4.38) shows a simplification of the minimization, where the elements v_i represent the constants that are found in the summation of f_n. For example:

$$v_1 = \sum_{n=1}^{119} \left(\left[\vec{b}_n \bullet \vec{q}_r \right]^{-2} \cdot 64 \cdot a_{1,n} \right) \tag{4.39}$$

Using MATLAB, the resulting elements for $\vec{v}$ were found: $\vec{v} = [667.1, 27.20, 236.5, 48.04, 648.5, 173.6, 65.10, 77.81, 12.35, 83.43, 43.40, 21.70, 19.01, 4.653, 19.73, 10.85, 10.85, 4.507, 0.9296, 5.413, 0.9997, 9.849]$.

This minimization has been solved using the Lagrange multiplier and yields the following relative switch sizes: $\vec{x} = [0.1616, 0.0326, 0.0962, 0.0434, 0.1593, 0.0824, 0.0505, 0.0552, 0.0220, 0.0571, 0.0412, 0.0291, 0.0273, 0.0135, 0.0278, 0.0206, 0.0206, 0.0133, 0.0060, 0.0146, 0.0063, 0.0196]$. The derivation can be found in Appendix A.1.

Finally, the SSL and FSL equivalent conduction resistances can be combined [31] and (4.40) is found.

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\frac{58}{C_f \cdot f_{sw}} \right)^2 + \left(R_{sw,t} \cdot 5 \cdot f(\vec{a}, \vec{b}, \vec{x}) \right)^2} \tag{4.40}$$

SWITCHING LOSSES

Switching losses occur due switching CMOS devices used to implement the SCPC switches. The capacitance present at the gate of the switching CMOS device is to be charged and discharged each cycle. Therefore, the switching loss current can be modelled as (4.42) where C_g is the total gate capacitance of the switching devices used for a specific conversion ratio setting and ΔV_g is the voltage swing on the gate.

$$Q_{sw,loss} = \Delta V_g \cdot C_g \tag{4.41}$$

$$I_{sw,loss} = \Delta V_g \cdot C_g \cdot f_{sw} \tag{4.42}$$

Bottom plate losses are normally also considered to be an important factor in SCPC losses, however, due to the use of off-chip capacitors, these losses are not applicable.

The aforementioned conduction and switching losses already show an important trade-off: Increasing switching frequency reduces the SSL component of the output resistance and thus reduces the conduction losses, but this increases the switching losses. The same trade-off can be found for total switch area. Increasing the total switch area reduces the FSL component of the output resistance and thus reduces the conduction losses, but this increases the total gate capacitance and therefore the switching losses. These trade-offs are discussed in Section 4.4.

4.2.4. MODIFICATION FOR VOLTAGE FLIPPING

The SCPC implementation found in Figure 4.5 is adapted, such that the capacitors of the SCPC can used for the voltage flipping operation. For this, it is required that all capacitors can be linked in series between the ground node and the input of the SCPC. Figure 4.6 shows the new implementation where switches S_6, S_7, S_{13}, S_{14}, S_{20} and S_{21} are added.[1]

4.3. IMPLEMENTATION

This section discusses the implementation of the SCPC that was designed in Section 4.2. Firstly, the switch designs for two types of SCPC switches is discussed: a regular NMOS switch and a bootstrapped NMOS switch. Next, an implementation for the dead-time is given, a suitable SCPC area is chosen and the layout is discussed shortly.

[1] Please note that the numbering of the other switches has changed compared to Figure 4.5.

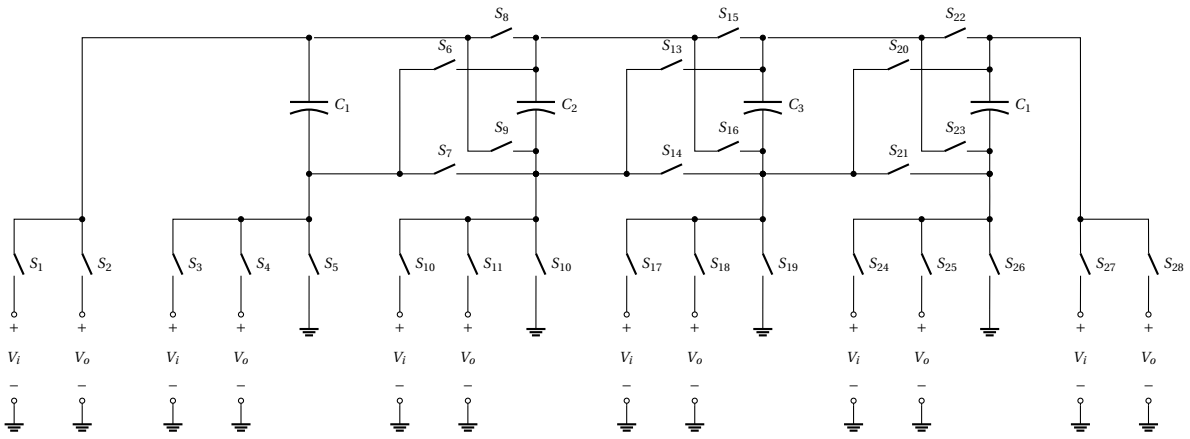


Figure 4.6: Implementation of the highly configurable SCPC Circuit

4.3.1. SWITCH DESIGN

NMOS devices are the preferred transistor type as they offer a lower on-resistance per area than PMOS devices, because the electron mobility is much higher than the hole mobility in silicon. As both devices have the same gate capacitance characteristics, a lower on-resistance is possible for the same switching losses, which is beneficial for the trade-off between conduction and switching losses. Figure 4.6 shows the 28 switches that connect the different nodes of the SCPC. Two types of switch circuits are proposed:

- Switches S_5, S_{12}, S_{19} and S_{26} connect a node to the ground node. These switches can easily be implemented with an NMOS device.
- The other switches do not connect to a ground node. For these switches, a bootstrapped NMOS switch circuit is developed.

Both types of switches are composed of unit size transistors, which are designed to have an on-resistance of roughly 9Ω (see Section 5.3). The switches can operate in two modes:

- In the normal mode, multiple of these unit size transistors are connected in parallel to created the required on-resistance, in accordance with the optimized switch size distribution (see Section 4.2.3 and Table 4.5).
- In the low-power mode, only one of these unit size transistors is activated per switch. This reduces the on-resistance of the switch, but also reduces switching losses (see Section 5.3).

All implemented switches require two enable signals to simplify implementation. One enable is used to switch the specific switch, while the other is used to make sure the additional parallel unit size transistors only turn on when in the normal power mode.

Several performance parameters are important for the switch designs. The first is that the switches can turn on and off quickly, thereby reducing the amount of dead-time required (see Section 4.3.2). Secondly, the trade-off between on-resistance and gate capacitance is important, because both influence the losses in the circuit (see Section 4.2.3).

NMOS SWITCH

Design

The turn-on and turn-off times of the switch should be in the nanosecond range as shown in Section 4.3.2. Figure 4.7 shows the implementation of the NMOS switch. Transistor $M0$ is the NMOS switch that conducts or blocks current between the connected node and the ground node. Transistors $M1$ and $M2$ act as a buffer to increase the turn-on and turn-off speed with a tapering factor ($M0$ gate capacitance versus $M1 + M2$ gate capacitance) of ~ 17. Simulations in this technology have shown that a 3:1 ratio between PMOS and NMOS width results in a inverter threshold voltage of $V_{dd}/2$ and similar turn-on and turn-off speeds. A NAND gate is used to provide the required double enable.

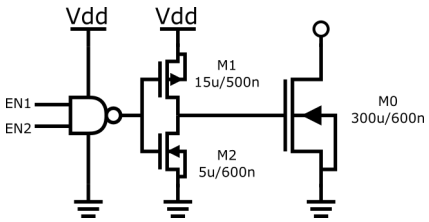


Figure 4.7: NMOS switch implementation

Table 4.4: NMOS switch implementation parameters

V_{dd}	$3.0V$	$4.5V$
R_{on}	8.97Ω	6.70Ω
$R_{on,min,PVT}$	5.68Ω	4.23Ω
$R_{on,max,PVT}$	13.87Ω	9.86Ω
E_{dd}	$4.82pJ$	$11.7pJ$
t_{on}	$2.74ns$	$2.11ns$
t_{off}	$3.66ns$	$3.03ns$
Area	$720um^2$	

Performance

A layout of this circuit was made, and the parasitics were extracted. The simulation of this layout extraction yielded the parameters seen in Table 4.4. Simulations with process variation, different operating temperatures and voltages have been executed, which showed a change in the on-resistance of the NMOS switch, as expected. The minimum and maximum on-resistance are also shown in Table 4.4. The energy from the supply taken for one switch cycle is given by E_{dd}. The turn-on time (defined as the time taken for the switch to reach 90% of its final on-resistance) and turn-off time (defined as the time taken to reach an off-resistance of $100k\Omega$) were also evaluated.

BOOTSTRAPPED NMOS SWITCH

Design

For the switches that are not connected to the ground node with one of their terminals, a bootstrapped NMOS switch circuit is developed, as the source of the NMOS transistor is not connected to ground. Simply driving the gate of a regular NMOS device with the supply voltage will not ensure that the threshold voltage of the transistor is exceeded, and will therefore not ensure that the device turns on. Instead, a bootstrapping circuit is required to switch the NMOS device properly.

The basic working of the bootstrapping circuit is shown in Figure 4.8. In a bootstrapping circuit, a capacitor (the bootstrapping capacitor C_b) is charged up in one phase. The charge on C_b is then used to charge the gate such that the gate-source voltage exceeds the threshold voltage of the transistor. The NMOS switched is turned off by connecting the gate to the source (assuming that the drain voltage is lower than or equal to the source voltage). Using the conservation of charge, the gate-source voltage in the on-phase can be determined, as shown in (4.43) to (4.46). This simplified approach assumes that the gate-source capacitance is the only capacitance in the transistor and is equal to the total gate capacitance.

$$\Delta Q_{Cb} = \Delta V \cdot C_b = (V_{dd} - V_{gs,on}) \cdot C_b \tag{4.43}$$

$$\Delta Q_{Cg} = \Delta V \cdot C_g = V_{gs,on} \cdot C_g \tag{4.44}$$

$$\Delta Q_{Cb} = \Delta Q_{Cg} \quad \rightarrow \quad (V_{dd} - V_{gs,on}) \cdot C_b = C_g = V_{gs,on} \cdot C_g \tag{4.45}$$

$$V_{gs,on} = \frac{V_{dd} \cdot C_b}{C_g + C_b} = \frac{V_{dd} \cdot k_{bg}}{k_{bg} + 1} \tag{4.46}$$

Where k_{bg} is the ratio between C_b and C_g:

$$k_{bg} = \frac{C_b}{C_g} \tag{4.47}$$

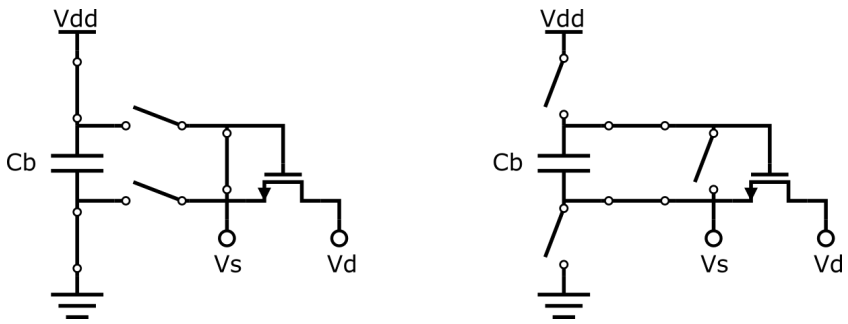


Figure 4.8: The two phases of the bootstrapping operation

Two additional requirements should be taken into account while designing this circuit:

- Due to limits in the technology used, the voltage between any two terminals of any transistor should not exceed $5V$.
- The NMOS switch should be able to conduct or block current between the two nodes, irrespective of the voltages on those nodes. The two nodes are assumed to have different voltages between $0V$ and $5V$.

Figure 4.9 shows the implementation of a bootstrap circuit that satisfies both requirements. The connection of the body of transistor $M0$ to the bottom plate of the bootstrapping capacitor C_b allows this [38]. In the off-state, the body and gate of transistor $M0$ are connected to ground through transistor $M2$ and $M5$. Therefore transistor $M0$ is not conducting current, neither through a created channel (as $V_{gs} \leq 0$ and $V_{gd} \leq 0$) nor through the body diodes (as $V_{bs} \leq 0$ and $V_{bd} \leq 0$). Also, the bootstrapping capacitor C_b is charged trough transistors $M1$ and $M2$. In the on-state, the bootstrapping capacitor C_b supplies a gate-source voltage V_{gs} larger than the threshold voltage through transistors $M3$ and $M4$. Furthermore, the source and body of the transistor $M0$ are connected together with transistor $M3$, such that the body-gate voltage does not exceed the technology voltage limit.

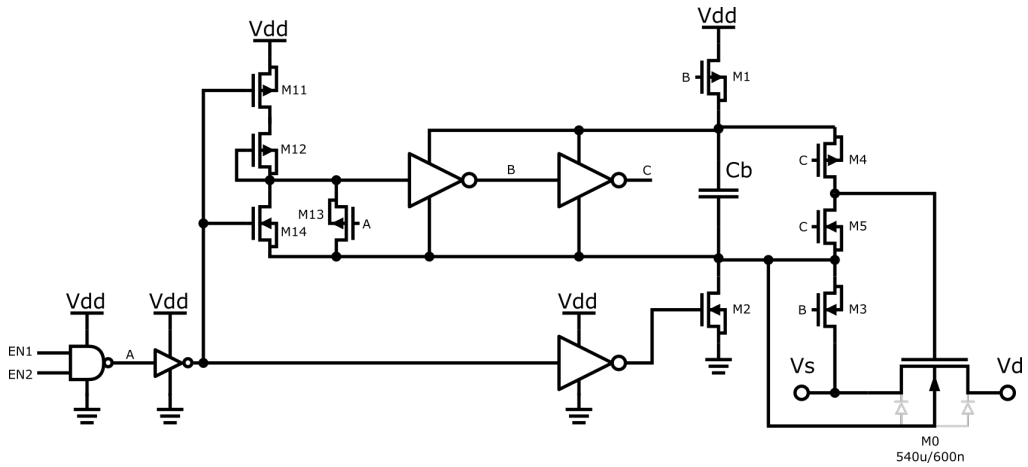


Figure 4.9: Bootstrapped NMOS switch implementation with level shifter

In order to generate the correct driving signals for the transistor in the bootstrapping circuit, a level shifter is added to the circuit. Transistor $M0$ is implemented as a deep-nwell NMOS device, to be able to change the body voltage, as this is not equal to the substrate voltage (ground).

Performance

The performance of the bootstrapping circuit is slightly different than what is expected from (4.46) and (4.42). The reason is that this formula assumes the only capacitance in transistor $M0$ is the gate-source capacitance. However, there are parasitic capacitances between all of the terminals of the transistor. Furthermore, the

gate and source are not connected together in the off-state, as was previously assumed. Instead, the gate is connected to ground, increasing the voltage swing on the gate terminal. Due to the required body connection of $M0$, this node also has a voltage swing in which the parasitic capacitances are charged and discharged. The increased voltage swing on the parasitic capacitances has two effects:

- Charge is taken from the V_s and V_d nodes, increasing dynamic losses.
- Additional charge is required from the bootstrapping capacitor C_b, which decreases the gate-source voltage V_{gs} in the on-state and thus decreases the on-resistance.

To compensate for the second effect, the transistor width is increased compared to that of the regular NMOS switch. For a transistor width of $540\mu m$ and $k_{bg} = 2.14$[2], the expected on-resistance and gate capacitance loss are 7.21Ω and $5.68pJ$ respectively. The aforementioned effects are visualized in Figure 4.10, which shows the simulation results for different source and drain voltages (where $V_{ds} = 100mV$) and a supply voltage V_{dd} of $3.0V$. For $V_s < 700mV$, the gate-source voltage V_{gs} is increased to above the expected value, due to the body diode in transistor $M1$. For larger source voltages, the gate source voltage declines steadily, which increases the on-resistance. The third graph clearly shows the increased switching energy losses due to the increased voltage swings on the parasitic capacitances.

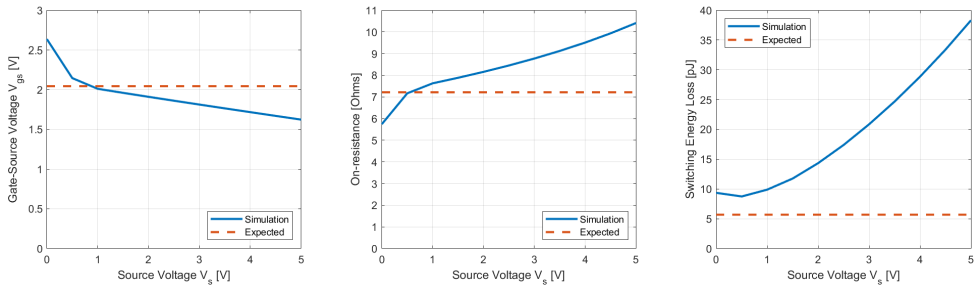


Figure 4.10: Bootstrapped NMOS Switch Performance (level shifters for ϕ and $\bar{\phi}$ signals not shown)

The calculations used in the model for the on-resistance and switching losses of the switches are changed to account for the aforementioned effect. The total area of the bootstrapped NMOS switch amounts to $1680\mu m^2$.

4.3.2. SCPC DEAD-TIME

The implementation of the switches bring with it an inevitable finite switching time. To ensure that a set of switches is actually turned off before the next set of switches turns on, a dead-time is introduced. The dead-time is the time between the falling edge of one signal and the rising edge of the next. This dead-time has an effect on the FSL resistance of the SCPC, as the factor of 5 in (4.34) actually comes from the inverse of the relative phase time $r_{T,\phi}$ which was assumed to be 0.2. The new relative phase time is found in (4.48), where T_{dead} is the newly introduced dead-time. The new FSL resistance and output resistance are respectively found in (4.49) and (4.50).

$$r_{T,\phi} = \frac{T_\phi}{T_{sw}} = \frac{\frac{T_{sw}}{5} - T_{dead}}{T_{sw}} = \frac{1 - 5 \cdot T_{dead} \cdot f_{sw}}{5} \tag{4.48}$$

$$R_{FSL} = R_{sw,t} \cdot f(\vec{a}, \vec{b}, \vec{x}) \cdot \frac{1}{r_{T,\phi}} = \frac{R_{sw,t} \cdot f(\vec{a}, \vec{b}, \vec{x}) \cdot 5}{1 - 5 \cdot T_{dead} \cdot f_{sw}} \tag{4.49}$$

$$R_{out} = \sqrt{\left(\frac{58}{C_f \cdot f_{sw}}\right)^2 + \left(\frac{R_{sw,t} \cdot f(\vec{a}, \vec{b}, \vec{x}) \cdot 5}{1 - 5 \cdot T_{dead} \cdot f_{sw}}\right)^2} \tag{4.50}$$

Figure 4.11 shows the effect of dead-time on the worst case efficiency ($V_{in,mpp} = 170mV$, $P_{in,mpp} = 50mW$). Due to the increase in FSL resistance, as shown in (4.50), the output resistance of the SCPC increases slightly,

[2] This value was chosen, such that the MIM capacitor area was equal to the area of the level shifter, bootstrapping circuit and deep n-well NMOS switch devices in the layout. This way the bootstrapping capacitor does not require extra area, as it can be placed in the metal layers above the devices

which reduces the expected efficiency. However, it can also be seen that for dead-times smaller than $20ns$, the absolute efficiency drop is less than 1%.

The conventional two-phase non overlapping clock generator [39] cannot be used to implement the dead-time, as the designed SCPC uses a 5-phase clock. Instead the dead-time is implemented by generating the signals with a delayed rising edge. Figure 4.12 shows the implementation of the dead-time. Through simulations of the layout cells it was found that a nominal rising edge delay of $11ns$ is enough such that the switches that are turning off already present an resistance of $100k\Omega$ by the time the other switches turn on. This should be more than enough to ensure that only a very limited amount of energy is lost due to unwanted conduction paths, while the dead-time will not have a large influence on the worst case efficiency.

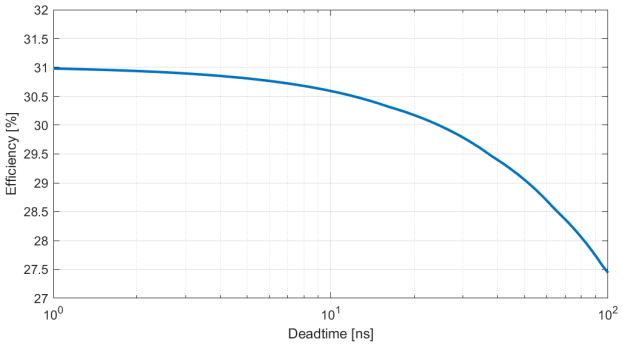


Figure 4.11: Dead-time Effect

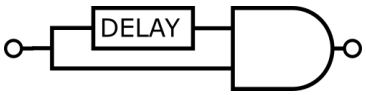


Figure 4.12: Dead-time Implementation

4.3.3. OPTIMIZATION AND TRADE-OFFS

The final step in determining the implementation parameters of the SCPC is the total switch size. This is done using the model that was developed throughout this chapter. To reduce the complexity of the model, it was assumed that all switches were implemented with bootstrapped NMOS switches. The on-resistance and energy losses found for these switches were used to determine the proper area for the SCPC.

The trade-off between area and efficiency is most interesting for the worst case scenario: $V_{in,mpp} = 170mV$, $P_{in,mpp} = 50mW$. For this scenario, the highest currents are expected. The output resistance must be low, because otherwise the the efficiency is decreased drastically due to the conduction losses. As shown in (4.50), the output resistance is decreased by increasing the frequency up to the point where the fast switching limit is dominant. The total switch resistance ($R_{sw,t}$), and therefore the total area, is an important variable for the fast switching limit. Additionally, the high switching frequency results in high switching losses, which are also highly dependent on the area.

Despite the fact that there is no hard constraint on the area that can be taken, a sensible trade-off should be made between area and worst case efficiency. This is shown in Figure 4.13. For this implementation, an SCPC area of $0.84mm^2$ was chosen, such that the minimum expected efficiency is roughly 30%.

Table 4.5: Number of NMOS Switches per SCPC Switch (see Figure 4.5)

SCPC Switch	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Nr. of NMOS Switches in Parallel	76	25	45	30	75*	1	1	40	25	26	13	27*	1	1

SCPC Switch	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Nr. of NMOS Switches in Parallel	20	14	13	7	13*	1	1	10	10	6	3	7*	4	9

*regular NMOS switch instead of bootstrapped NMOS switch

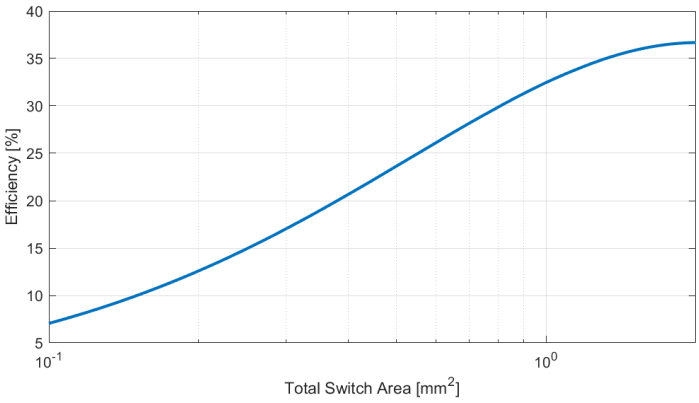


Figure 4.13: SCPC area vs. worst case efficiency

4.3.4. SCPC LAYOUT

Now that the parameters of the SCPC have been discussed, it can be implemented. With a total available area of $0.84mm^2$ for the switches and a switch size of $1680um^2$, the total number of switches that can be used is 500. The optimized switch sizes from Section 4.2.3 are used and the number of parallel 9Ω NMOS switches per SCPC switch can be seen in Table 4.5. The switches that were added for the voltage flipping operation only use a single 9Ω NMOS switch.

A significant portion of the SCPC layout is used for metal interconnects, as these have a maximum current density to limit the effects of electro-migration. The total area of the SCPC including all 500 switches and metal interconnect is $1.6mm^2$. The layout of the SCPC is shown in Figure 4.14. It was designed such that the layout was compact, with large enough metal interconnects to have acceptable current densities and low parasitic resistances.

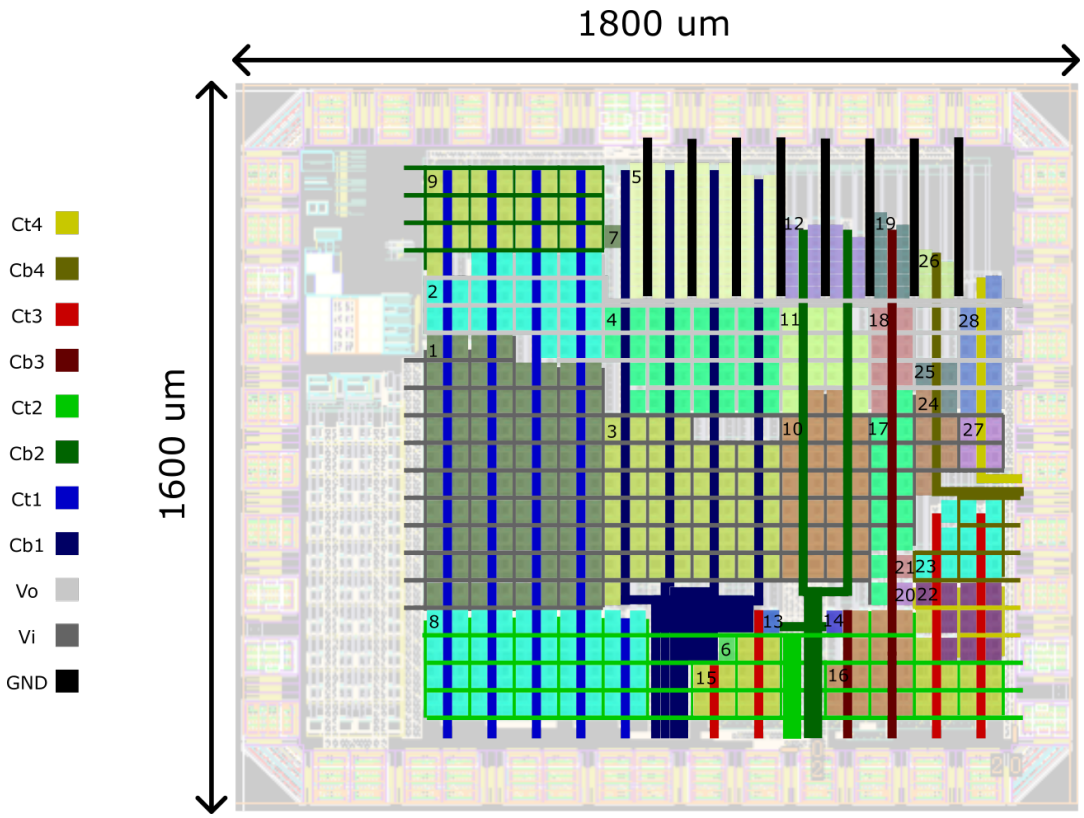


Figure 4.14: SCPC layout in the IC layout

4.4. PERFORMANCE ANALYSIS

Using the average model, the conduction losses, switching losses and device parameters found in the previous sections, the performance of the SCPC can be analysed.

4.4.1. LINEAR SOURCE EXAMPLE

The equivalent model for a linear DC source (like a TEG) and the average model for the SCPC are combined in the circuit in Figure 4.15. The current required for switching is modelled as a current source taking current from the output and a battery at $3V$ is attached. The resulting circuit is shown in Figure 4.15 and incorporates the power losses shown in Section 4.1. The control losses are assumed to be negligibly small for now.

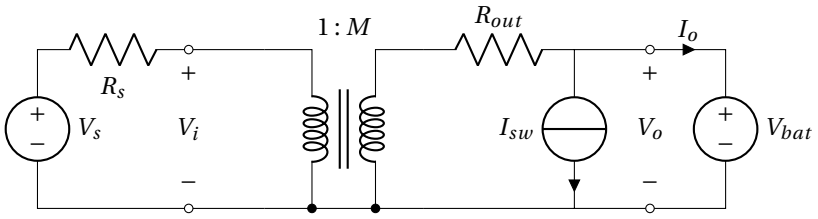


Figure 4.15: Equivalent circuit for harvesting from a linear source

With the help of a circuit analysis in MATLAB, the performance of the equivalent circuit is analysed. Figure 4.16 shows the harvesting efficiency as a function of the switching frequency. The harvesting efficiency is the ratio between the actual output power and the MPP power of the source. To find the optimal efficiency, a trade-off has to be made between switching losses (increase with switching frequency f_{sw}), conduction losses (decrease with switching frequency f_{sw}) and MPP mismatch (dependent on the SCPC conversion ratio and output resistance).

The figure also shows the behaviour of the SCPC output resistance with regards to the switching frequency. It shows that indeed the SSL resistance is dominant for $R_{SSL} > R_{FSL}$ while the FSL resistance is dominant for $R_{SSL} < R_{FSL}$. The FSL resistance also shows a slight increase for higher frequencies due to the chosen deadtime. The switching frequency rises linearly with the switching frequency as expected. It is uncommon for the FSL resistance to be dominant in the optimal configuration, because increasing the frequency far beyond the transition region between the SSL and FSL resistance barely decreases the conduction resistance and only increases conduction losses, which almost guarantees a worse harvesting efficiency.

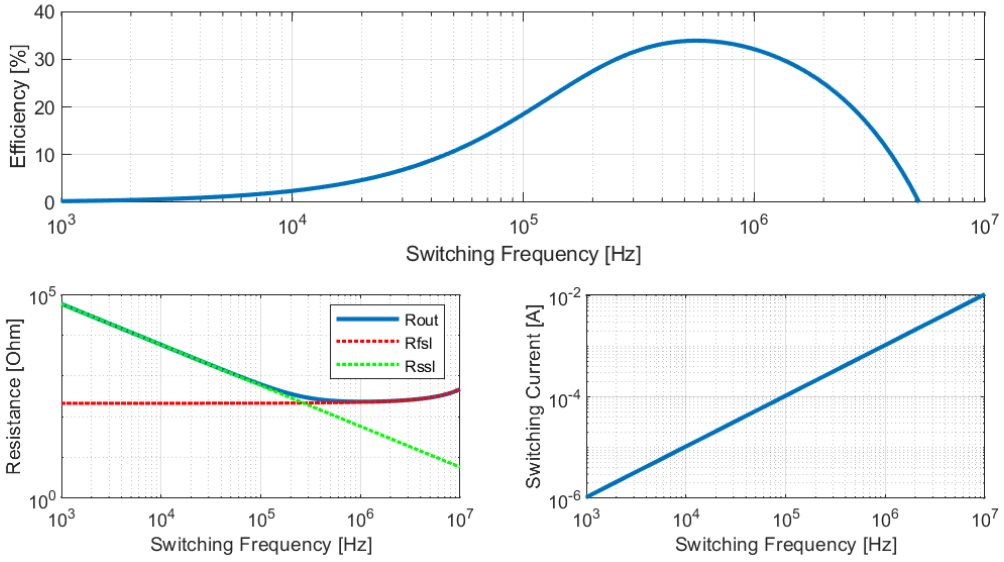


Figure 4.16: Harvesting efficiency for $V_{mpp} = 170mV$, $P_{mpp} = 1mW$ and $M = 16$

4.4.2. PERFORMANCE ACROSS OPERATING REGION

The same analysis was done for the full range of expected MPP input voltages and powers. The same circuit analysis in MATLAB was applied for a range of MPP input voltages ($170mV$ [3] to $5V$) and MPP input powers ($10uW$ to $50mW$). For each operating point, all conversion ratios and a range of switching frequencies ($100Hz$ to $10MHz$) were tested, to find the maximum possible harvesting efficiency. The resulting harvesting efficiencies can be found in Figure 4.17. Several observations about the performance of the SCPC can be made:

- A peak efficiency of 97.6% is found.
- A large part of the operating region ($V_{in,MPP} > 900mV$) shows an efficiency higher than 90%.
- The efficiency drops for lower MPP input voltages. This is caused by the limited maximum conversion ratio of 16 and the subsequent MPP mismatch.
- The efficiency decreases even further for higher input powers. This is due to the effect of the fast switching limit, where the SCPC output resistance cannot be decreased further and the high currents cause a larger voltage drop in the SCPC, limiting its ability to reach the MPP voltage at the input.

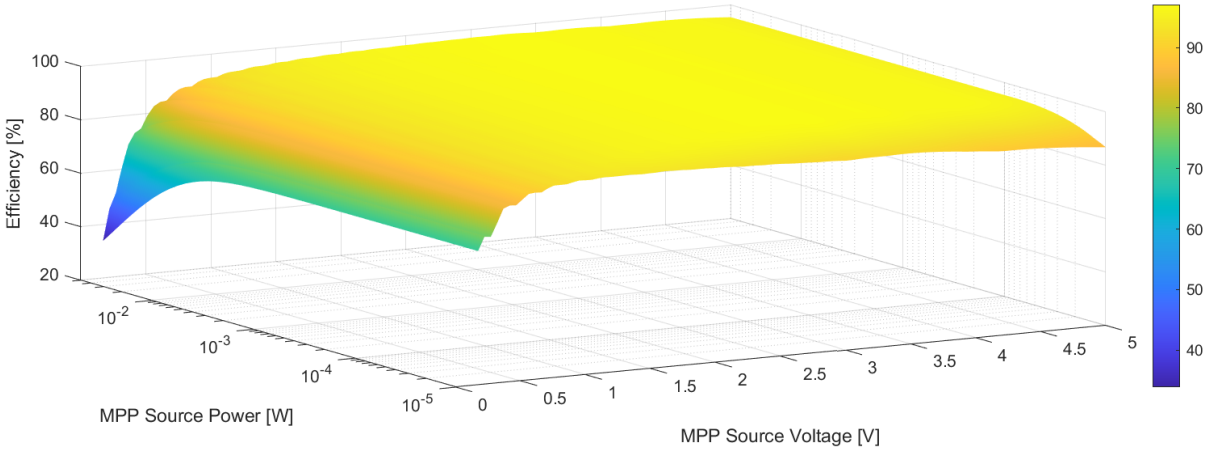


Figure 4.17: Harvesting Efficiency for a range of input voltages and powers

4.5. PROTECTION CIRCUITRY

To ensure reliable operation over the lifetime of the PMIC, the devices have to be protected against high voltages. High voltages can be expected from two sources: an ESD (electro-static discharge) event from the environment or a high voltage from the harvester. These two are discussed separately.

4.5.1. ESD PROTECTION

An ESD event is an incident where a charge is suddenly transferred between two nodes with a different potential. In this scope, an external capacitance (e.g. human body or metal object) has a charge which was accumulated through the triboelectric effect. The voltage potential of these objects can reach up to $35kV$ [40]. If an IC conducts the high current from an ESD effect, devices on that IC may be damaged due to the excessive voltages that occur. For this reason, ESD protection circuits are used, such as the one found in Figure 4.18. In this setup, diode $D1$ ensures that the voltage on the IO pin, and thus the circuitry does not reach voltages higher than the supply voltage V_{dd}, plus the diode voltage (usually around $700mV$). Diode $D2$ ensures that the voltage on the IO pin does not drop below the ground potential, minus the diode voltage.

However, this exact method cannot be use in this design. The reason for this is that the SCPC may be in a step-down configuration ($M < 1$), therefore creating voltages larger than the supply voltage (output voltage) at the input of the SCPC. This way, the harvester inputs V_{harv+} and V_{harv-}, but also the IO pins that connect

[3] The minimum MPP input voltage of $170mV$ was chosen because of the specifications of an envisaged harvester, but the design is compatible with lower input voltages, although a significant drop in efficiency is to be expected.

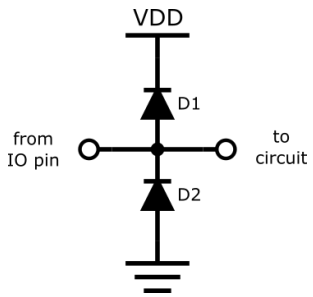


Figure 4.18: Conventional ESD Protection Circuitry

the external floating capacitors C_{f1} to C_{f4} to the IC, are regularly exposed to voltages that exceed the supply voltage.

For this reason, an auxiliary supply is added to the implementation, as shown in Figure 4.19. This auxiliary supply is connected to the SCPC input if it is in step-down mode, and to the SCPC output if it is in step-up mode. This way, the auxiliary supply always has the highest potential of the IC, and it is able to protect against ESD events, without disturbing normal operations. According to the ESD models described in [40], the charge from ESD events do not increase the auxiliary supply voltage significantly, due to its relatively large capacitance of $1\mu F$.

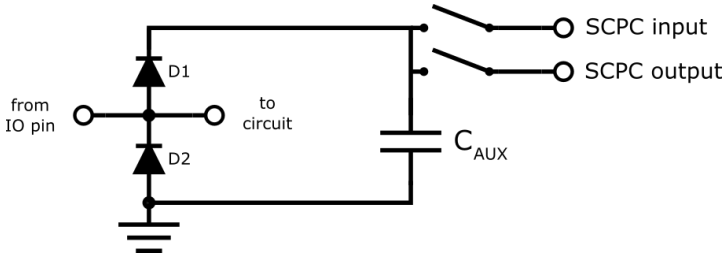


Figure 4.19: ESD protection circuit with auxiliary supply

4.5.2. ACTIVE 5V PROTECTION

An active protection circuitry is used to prevent excessively high voltages from the harvester. Compared to passive protection methods, such as series connected diodes or Zener diodes, this solution allows more precise protection against high voltages. Additionally, the protective measures taken to limit the voltage can act discretely, instead of there being a transition region between fully conducting and not conducting for the (Zener) diode methods. The circuit used for this uses a resistive ladder and comparator as shown in Figure 4.20. A scaled down voltage of the to-be-protected node is compared to the bandgap reference voltage of $1.25V$. If the voltage exceeds the configured protection voltage, the over-voltage protection trigger output signal (OVP) is high. Transistor $M1$ sinks current from the protected node, if this current sinking is enabled. The auxiliary supply node is protected against the high voltages, as has the highest voltage in the PMIC.

Four non-idealities from this circuit should be taken into account: the limited bandwidth of comparator, transistor mismatch in the comparator, the delay in the resistive divider and resistor mismatch. Transistor level simulations were used to find a good trade-off between these limitations, but also voltage headroom, circuit area and power consumption. The nominal trigger voltage is $4.88V$, with a mismatch offset of $6.3mV/\sigma$ and a maximum total delay of $10\mu s$.

As the maximum expected input power from a harvester is $50mW$, the maximum expected input current from a harvester at $5V$ is $10mA$. The maximum voltage slope on the auxiliary supply, to which a $1\mu F$ capacitor is connected, is therefore expected to be $10V/ms$. Combining the nominal trigger voltage of $4.88V$, a 3σ offset voltage of $18.9mV$ and a delay of $10\mu s$, the over-voltage protection is always triggered before the auxiliary supply reaches $5.0V$. Once the over-voltage protection is triggered, the protection is executed differently, dependent on whether a DC source or piezo source is connected.

The actual protection from high voltages, happens through of the sinking of current trough transistor $M1$,

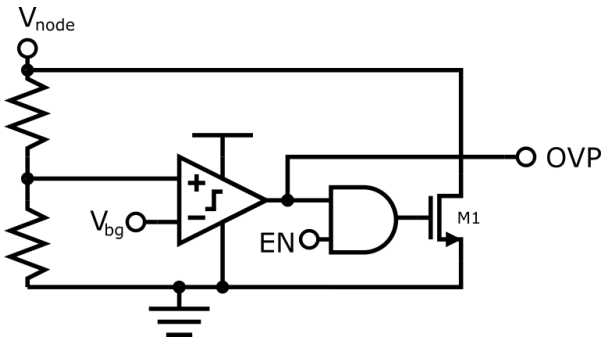


Figure 4.20: Active $5V$ protection circuit

when a DC source is connected. Across the process and temperature variations, this transistor is to sink more than $10mA$, the maximum input current at a $5V$ input. This way, the voltage on the auxiliary supply drops. The over-voltage protection trigger OVP turns off and transistor $M1$ then stops sinking current from the node and the voltage is be able to rise again. This cycle is repeated to ensure the voltage on the auxiliary supply never exceeds $5V$. Some delay is present in the loop due to the resistive ladder and finite comparator bandwidth, which avoids high frequency toggling.

A significant amount of energy is lost in protecting the node this way. Therefore, over-voltage protection triggers should be avoided as much as possible in DC source more by changing the settings of the SCPC such that its input voltage is not too close to $4.88V$.

4.6. CONCLUSION

This chapter has discussed the design, implementation and performance of a novel switched-capacitor power converter (SCPC). The implementation has revealed several drawbacks in this SCPC design. Namely the need for bidirectional NMOS switch designs and the additional of the auxiliary supply, which is required as the SCPC supports both step-up and step-down voltage conversion. However, the resulting the high efficiency over a wide range of input voltages and powers is believed to compensate for these implementation difficulties.

5

VOLTAGE FLIPPING RECTIFIER DESIGN

5.1. INTRODUCTION

This chapter shows the design of the voltage flipping rectifier that is used to convert the energy from a piezo element, using the SCPC designed in Chapter 4. Firstly, the benefits and expected results of using an SCPC for the voltage flipping operation are discussed. Secondly, a low-power mode adaptation of the SCPC is discussed, to increase the performance of the voltage flipping rectifier. The control and protection circuits for the voltage flipping rectifier are discussed, as well as the design of a current sensing rectifier. Lastly, the switching input capacitor that enhances the SCPCs settling behaviour is discussed.

5.2. VOLTAGE FLIPPING OPERATION

5.2.1. VOLTAGE FLIPPING IN SCPCS

In order to do a voltage flipping operation, one or more capacitors at different voltages are required. Coincidently, a switched capacitor power converter also works with one or more capacitors at different voltage levels and as shown in Section 2.5.3, during a voltage flipping operations, the power converter does not need to be active. This brought up the idea to do a voltage flipping operation with capacitors from the SCPC. This sections gives a few examples of the integration of a voltage flipping operation into an SCPC. [1]

EXAMPLE 1: $M = 1/4$

Figure 5.1 shows a 2-phase $M = 1/4$ switched capacitor power converter. For this converter the following capacitor voltages are found: $V_i = 4V_o = 4V_{C_1} = 4V_{C_2} = 4V_{C_3}$. That means that for a voltage flipping operation, the following voltages can be created by placing capacitors in series: $3/4V_i$, $2/4V_i$, $1/4V_i$. Therefore a 7-phase voltage flipping operation is possible by switching the scheme in Table 5.1.

ϕ_{FCR}	1	2	3	4	5	6	7
V_p	$\frac{3}{4}V_i$	$\frac{1}{2}V_i$	$\frac{1}{4}V_i$	0	$-\frac{1}{4}V_i$	$-\frac{1}{2}V_i$	$-\frac{3}{4}V_i$

Table 5.1: 7-phase voltage flipping

[1] Capacitor sharing between an SCPC and voltage flipping rectifier was attempted in [30], however, that work did not take into account that the SCPC could be designed such that different voltage levels were created by the SCPC operation

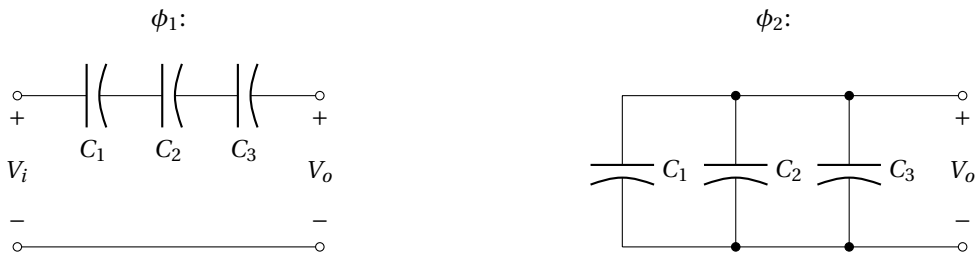


Figure 5.1: 2-phase SCPC Circuit for $M = 1/4$

EXAMPLE 2: $M = 4/5$

Figure 5.1 shows a 2-phase $M = 4/5$ switched capacitor power converter with the following capacitor voltages: $V_{C_1} = 2V_{C_2} = 2V_{C_3} = 4V_o = 5V_i$. Thus, the following voltages can be created: $4/5V_i$, $3/5V_i$, $2/5V_i$, $1/5V_i$. A 9-phase flipping capacitor operation is possible as shown in Table 5.2.

ϕ_{FCR}	1	2	3	4	5	6	7	8	9
V_p	$\frac{4}{5}V_i$	$\frac{3}{5}V_i$	$\frac{2}{5}V_i$	$\frac{1}{5}V_i$	0	$-\frac{1}{5}V_i$	$-\frac{2}{5}V_i$	$-\frac{3}{5}V_i$	$-\frac{4}{5}V_i$

Table 5.2: 9-phase voltage flipping

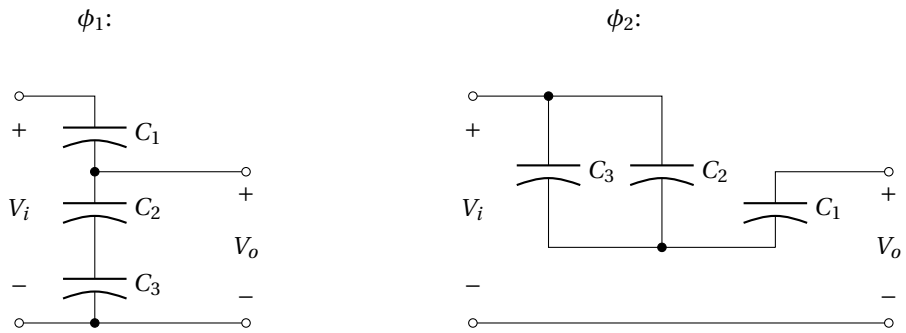


Figure 5.2: 2-phase SCPC Circuit for $M = 4/5$

EXAMPLE 3: $M = 4$

Figure 5.1 shows a 2-phase $M = 4$ switched capacitor power converter with the following voltages: $4V_{C_1} = 4V_{C_2} = 4V_{C_3} = 4V_i = V_o$. As no voltages below V_i can be created with the available capacitors, no voltage flipping operation is possible for this converter.

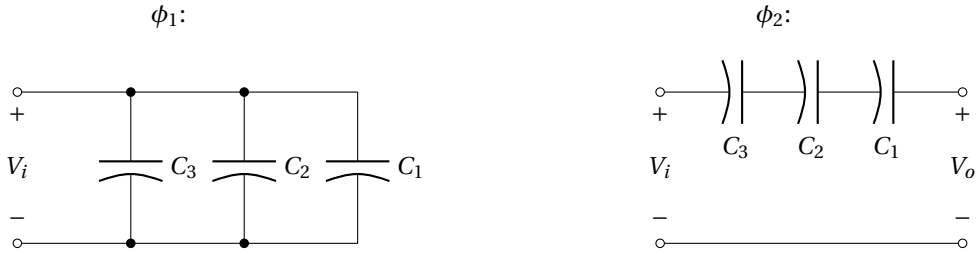


Figure 5.3: 2-phase SCPC Circuit for $M = 4$

These three examples have shown that the voltage flipping ability of a switched capacitor power converter is highly dependent on the chosen topology. From the examples above, the following hypothesis may be found:

> For an SCPC operating with a conversion ratio of $M = \frac{P}{Q}$, $Q-1$ equally spaced intermediate voltage levels between V_i and $0V$ can be made with the floating capacitors.

With the help of an analysis in MATLAB, the hypothesis above was tested and found to be true for all conversion ratios of the newly designed SCPC. Unfortunately, no mathematical evidence was found to accept or refute the hypothesis. Section 4.2.4 shows how the SCPC was modified, such that the floating capacitors can be connected in series between the ground and input of the SCPC to create the different voltage steps.

5.2.2. GENERAL OUTPUT POWER ESTIMATION

Equations (2.20) from Section 2.5.3 is used to find the output power for any voltage flipping rectifier, as shown in (5.1), where V_{OC} is the open circuit voltage of the piezo element, which is found in (5.2).

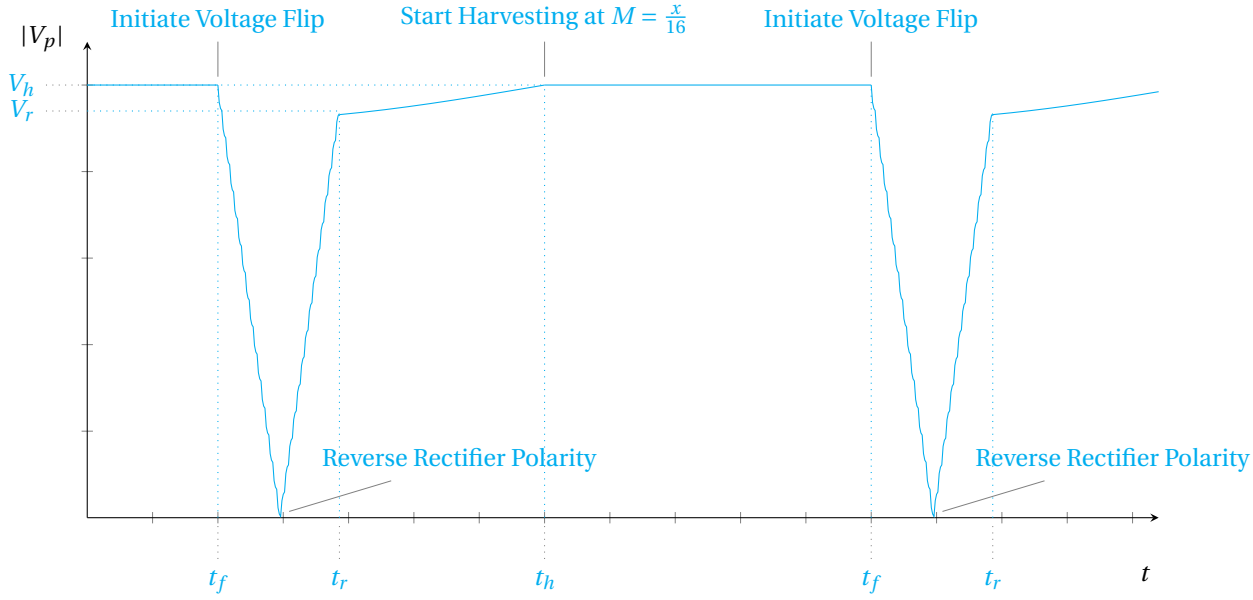
$$P_h(V_h) = V_h \cdot V_{OC} \cdot 4 \cdot f_{ex} \cdot C_p - V_h^2 \cdot 2 \cdot f_{ex} \cdot C_p \cdot (1-\eta_{flip}) = 2 \cdot f_{ex} \cdot C_p \cdot \left(V_h \cdot V_{OC} \cdot 2 - V_h^2 \cdot (1-\eta_{flip})\right) \tag{5.1}$$

$$V_{OC} = \int_0^{\pi/2} \frac{I_p}{C_p}(t)dt = \frac{1}{C_p}\int_0^{\pi/2} I_{max} \cdot sin(2\pi \cdot f_{ex} \cdot t)dt = \frac{I_{max}}{2\pi \cdot f_{ex} \cdot C_p} \tag{5.2}$$

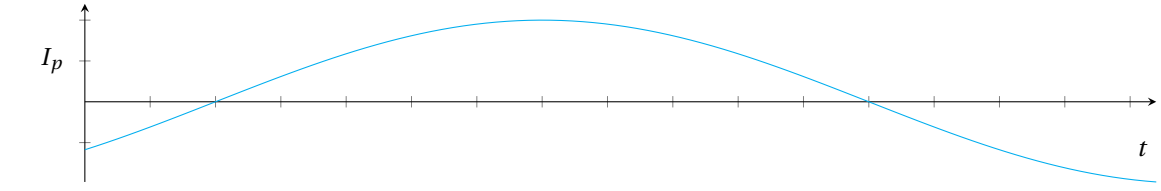
The maximum power point voltage can be found through in (5.4).

$$\frac{\delta P_{mpp}}{\delta V_h} = 4 \cdot f_{ex} \cdot C_p \cdot \left(V_{OC} - V_h \cdot (1-\eta_{flip})\right) = 0 \tag{5.3}$$

$$V_{h,mpp} = \frac{V_{OC}}{1-\eta_{flip}} \tag{5.4}$$



(a) Absolute Piezo Voltage



(b) Piezo current waveform I_p

Figure 5.4: Piezo Harvesting Scheme with exaggerated 31-phase Voltage Flipping Operation

5.2.3. 31-PHASE VOLTAGE FLIPPING OPERATION

Equation (5.1) shows that a higher voltage flipping efficiency η_{flip} results in a higher output power. Equation (2.17) shows that for a higher number of available voltage levels, the voltage flipping efficiency is higher. Therefore, for the designed SCPC, conversion ratios with a denominator of 16 are preferred during the harvesting phase of the piezo harvesting cycle (see Section 2.5.3). This way, 15 intermediate equally spaced voltage levels are available after the harvesting phase, according to the hypothesis from Section 5.2.

This results in a 31-phase voltage flipping operation, where firstly the 15 intermediate voltage level are accessed, then the piezo element in shorted and the rectifier polarity is changed. Next, the 15 intermediate voltage levels are used to rebuild the piezo voltage up to 93.75% (or $\frac{15}{16}$th) of its original value. This cycle is depicted in Figure 5.4. Appendix A.4 shows the switch configurations for the 31 steps of the 31-phase voltage flipping operations. The combination was chosen such that as few floating capacitors as possible had to be switched in series to create the highest equivalent flipping capacitance C_{flip}.

5.2.4. LIMITATIONS FOR C_p

In the aforementioned equations, it is assumed that $C_p << C_{flip}$ (Section 2.5.3). However, as the piezo capacitance C_p increases, the voltage flipping operation becomes less ideal. An example of this is shown in Figure 5.5, which shows an analysis of a flipping operation where $C_p = 200nF$. It is assumed that the settling time is larger than 5τ for each step and that harvesting is possible at $5V$.

As the piezo capacitance is no longer much smaller than the floating capacitors, the charge gathered during the discharging of the piezo capacitance, changes the voltages on the flipping capacitors. This disrupts the voltage flipping operation. The intermediate voltage levels are no longer equally spaced and the voltage flipping efficiency is decreased from 93.75% to 92.4%. Moreover, the voltages on the flipping capacitor do not necessarily return to their original value. This imbalance is restored upon engaging the SCPC, but this does require some charge transfers between the capacitors, which in turn introduces new losses.

In order to keep these effects to a minimum, it is decided that the piezo capacitance C_p should be no larger than $100nF$ assuming that $1\mu F$ floating capacitors are used. Up to this value, the voltage flipping efficiency is very high (see Figure 5.6). This also relaxes the requirements for the implementation regarding the settling of each step of the voltage flipping operation, as the settling constant τ is highly dependent on the piezo capacitance C_p.

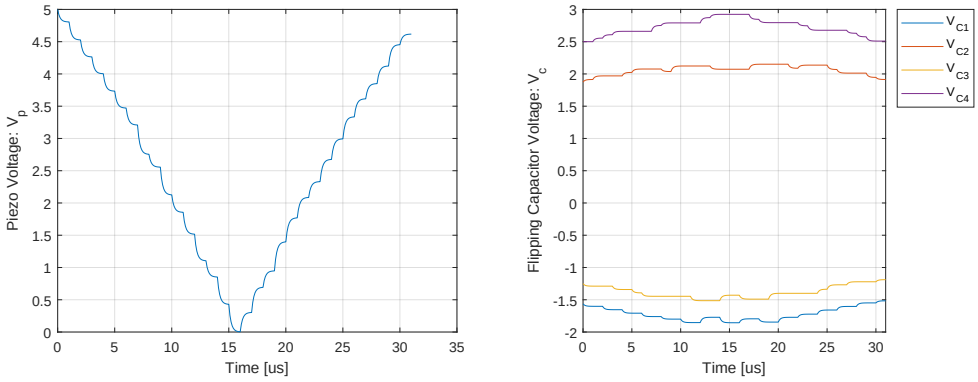


Figure 5.5: Example of how the capacitor voltages and η_{flip} change for large piezo capacitances ($C_p = 200nF$)

5.2.5. MOPIR

A common method for determining the performance of a voltage flipping rectifier is by computing the Maximum Output Power Improvement Rate (MOPIR) [28, 30, 41–43]. This is the ratio between the output power of the proposed voltage flipping rectifier versus the MPP output power of a full bridge rectifier. The literature is not always on the same page on whether to use an ideal or non-ideal full bridge rectifier. This work assumes an ideal full bridge rectifier for comparison, as it decouples the comparison from design choices made in designing a full bridge rectifier (e.g. diode choice or passive versus active implementation). Using (5.4), the MPP harvesting voltage of the ideal full bridge rectifier is found to be $V_{mpp,fbr} = V_{OC}/2$. The MPP harvesting voltage of the 31-phase flipping capacitor rectifier is found to be $V_{mpp,fcr} = V_{OC} \cdot 16$, using (2.17). Next, the

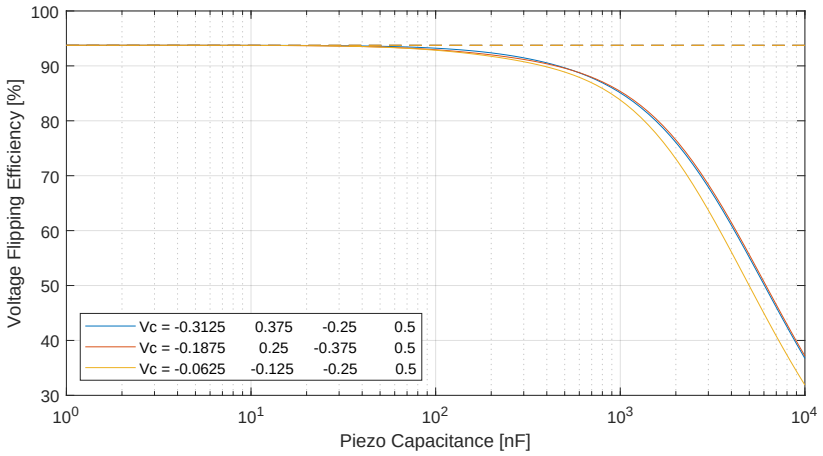


Figure 5.6: Voltage Flipping Efficiency versus Piezo Capacitance C_p

MOPIR is calculated, assuming the voltage flipping rectifier harvests using its MPP harvesting voltage:

$$MOPIR = \frac{P_{fcr}}{P_{fbr}} = \frac{2 \cdot f_{ex} \cdot C_p \cdot \left(V_h \cdot V_{OC} \cdot 2 - V_h^2/16\right)}{2 \cdot f_{ex} \cdot C_p \cdot \left(V_h \cdot V_{OC} \cdot 2 - V_h^2 \cdot 2\right)} = \frac{V_h \cdot V_{OC} \cdot 2 - V_h^2/16}{V_h \cdot V_{OC} \cdot 2 - V_h^2 \cdot 2} \tag{5.5}$$

Using the MPP harvesting voltages $V_{mpp,fbr}$ and $V_{mpp,fcr}$, the theoretically attainable MOPIR for the 31-phase flipping capacitor rectifier is found to be 32:

$$MOPIR_{ideal} = \frac{V_{OC}^2 \cdot 32 - V_{OC}^2 \cdot 16}{V_h \cdot V_{OC} \cdot 2 - V_{OC}^2/2} = 32 \tag{5.6}$$

5.2.6. OUTPUT POWER LIMITATIONS

Several limitations have to be taken into account while evaluating the MOPIR. Firstly, the harvesting voltage V_h is always limited by the technology voltage, which is $5V$ in the technology that is used in this work. Therefore, $V_{mpp,fbr}$ and $V_{mpp,fcr}$ may never exceed this $5V$ limit. Secondly, only certain discrete harvesting voltages can be achieved due to the limited number of conversion ratios. Assuming that the currents are low enough such that the SCPC output resistance introduces a voltage drop that is negligable, the following condition has to be met:

$$V_h = \frac{V_{bat}}{M} \leq 5 \tag{5.7}$$

For battery voltages between $3V$ and $4.5V$, the conversion ratios that have a denominator of 16 are $\frac{11}{16}$, $\frac{13}{16}$ and $\frac{15}{16}$. Figure 5.7 shows the expected MOPIR for these conversion ratios.

5.3. LOW POWER MODE

Determining the total switch size of the SCPC is a matter of balancing the conduction losses and switching losses (see Section 4.2.3). Equation (4.50) shows two variables that can be changed to do so: The switching frequency and the total switch area (effecting the total switch resistance). For the DC source operations, the most straight forward way of balancing both losses was by changing the switching frequency. However, this is not the case for harvesting from piezo element sources. To provide sufficiently low switching losses, the switching frequency would have to be below $1kHz$, for the chosen switch size. This is not feasible for piezo element harvesting, because at least a few SCPC cycles are required to consistently track the current (see Section 5.7). For a maximum excitation frequency of $200Hz$, the minimal switching frequency was found to be $5kHz$.

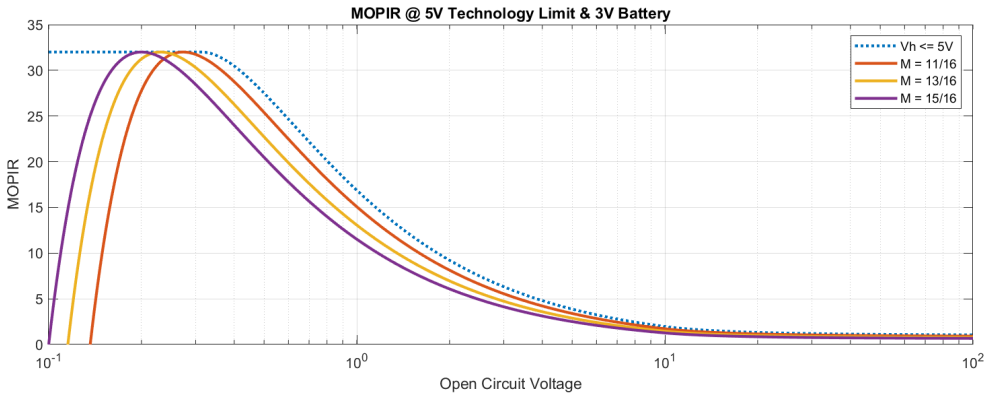


Figure 5.7: MOPIR limit for $V_h < 5V$ and multiple conversion ratios

Instead of lowering the switching frequency to reduce losses, the second approach is used: lowering the switch area. A low-power mode is introduced for which a fraction of the total number of switches is used. This way, low switching losses can still be achieved with a higher switching frequency (such as $5kHz$). To simplify the implementation, all switches have the same size in the low-power mode. However, this switch size does not only effect the conduction and switching losses in the SCPC. The voltage flipping operation also uses these switches. The on-resistance of the switches, together with the piezo and floating capacitances, determine the settling time of each of the 31 phases. Furthermore, switching losses are introduced for switching the switches for each of the 31 phases. Decreasing the switch size can decrease switching losses, but this increases the time required per phase to settle, therefore increasing the total time taken to flip the voltage. This reduces the conduction angle (time between t_r and the end of the half cycle in Figure 5.4), which reduces the amount of energy harvested.

Finding the optimal switch size is complicated due to the many aforementioned dependencies. Therefore it was decided to determine the optimal switch size through simulations of the transistor level implementation. Through these simulations, it was found that a switch on-resistance of 9Ω, a $100kHz$ voltage flipping clock frequency and SCPC switching frequency of $5kHz$ balances SCPC switching losses, voltage flip switching losses and conduction angle losses. This allows each voltage flipping phase to settle up to roughly 95% for the maximum piezo capacitance of $100nF$, while the total time taken for the voltage flip is $310us$, roughly 16% of one half cycle for the maximum excitation frequency of $200Hz$.

As an additional feature of the SCPC, the low-power mode can also be activated by an external signal for DC source operations.

5.4. CONVERSION RATIO SETTING

Figure 5.7 suggests that for the region where the MOPIR is not limited by the harvesting voltage ($V_{OC} < 312.5mV$), different open circuit voltages give a different optimal conversion ratio setting. For this reason, a piezo harvesting specific MPPT algorithm has been developed, which can be found in Appendix A.2.

However, the aforementioned formulas and figures assume a lossless system. Simulation results of the transistor level circuits, which will be elaborated in Chapter 7, have shown a loss of roughly $20uW$ for this design. The effects on these losses can be seen in Figure 5.8. This shows that the V_{OC} based MPPT will not be of much use, and that reaching the maximum MOPIR (and thus maximum power output) is much more dependent on the conversion ratio setting. This must be set to be as low as possible, such that V_h is as high as possible, while not exceeding the technology voltage limit ($5V$). Therefore the conversion ratio must be set as follows (as $V_{rect} = V_h < 5V$ and $V_{rect} \cdot M = V_{bat}$):

- For $V_{bat} < 3.43V$: $M = \frac{11}{16}$
- For $3.43 < V_{bat} < 4.06V$: $M = \frac{13}{16}$
- For $4.06 < V_{bat} < 4.69V$: $M = \frac{15}{16}$

It should be noted that this method does not necessarily ensure the best conversion ratio setting, espe-

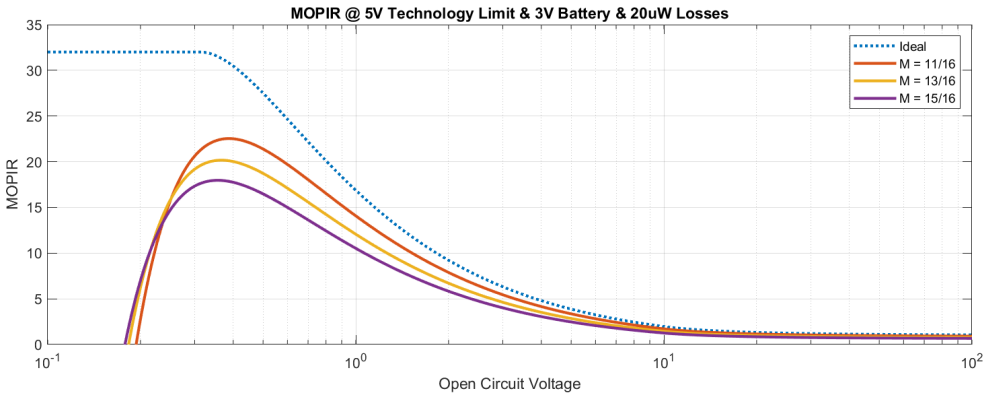


Figure 5.8: MOPIR with $20uW$ of losses for $f_{ex} = 200Hz$ and $C_p = 100nF$

cially because losses can differ between different setting and are not necessarily always $20uW$. However, this method can be implemented relatively easily and robustly, which benefits the design. To truly ensure maximum output power, an output power measurement and feedback elements would have to be added to the design.

IMPLEMENTATION

For the implementation, the respective voltage levels are changed to allow for some current ripple headroom before the over-voltage protection is triggered (see Section 4.5.2):

- Allow $M = 11/16$: $V_{bat} < 3.23V = 4.7V \cdot \frac{11}{16}$
- Allow $M = 13/16$: $V_{bat} < 3.82V = 4.7V \cdot \frac{13}{16}$
- Allow $M = 15/16$: $V_{bat} < 4.5V = 4.8V \cdot \frac{15}{16}$

The last voltage level allows a rectifier voltage of $4.8V$ instead of $4.7V$, such that the battery can still be charged up to $4.5V$. With an over-voltage protection at $4.86V$ at its lowest, there is still enough headroom available for some voltage ripple. These battery voltage dependent triggers are implemented with a resistive ladder and comparators as shown in Figure 5.9.

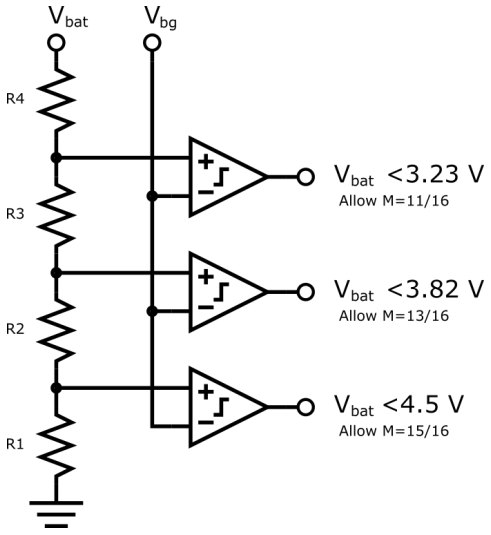


Figure 5.9: Piezo conversion ratio setting implementation

A bandgap voltage reference of $1.25V$ is assumed. The total series resistance of the voltage ladder is $56M\Omega$, such that the current consumption remains low. MIM capacitors are added and connected to the inputs of the comparators to lower the noise contribution and charge injection from the comparators. Figure 5.10 shows

the two stage comparators that are used to compare the voltage from the resistive ladder with the reference voltage. Hysteresis is added to the comparator such that toggling around a threshold is avoided.

Transistors $M5$ to $M9$ make up the two stage comparator with a current mirror using transistors $M1$, $M2$ and $M4$. Transistor $M10$ enables an extra current source from transistor $M3$ when the output (OUT) is high. This makes up a hysteresis of roughly $15mV$. Two inverters are used to add gain and thus ensure sharp transitions for the output signal OUT and its inverted counterpart $\overline{OUT}$. The total area for one comparator is $2814um^2$ and its supply current is $17nA$ at a supply voltage of $3.0V$.

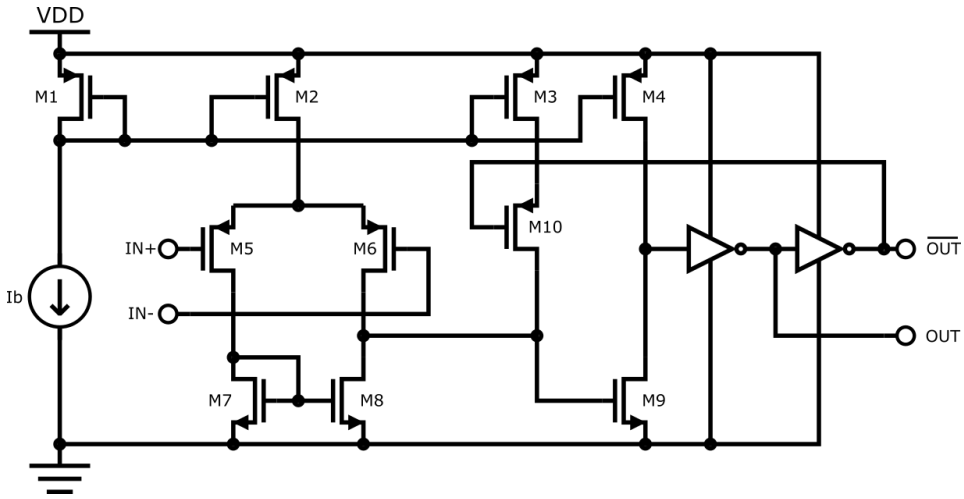


Figure 5.10: Hysteretic comparator implementation

Additionally, logic is added to ensure that the highest allowed conversion ratio is chosen. Lastly, the outputs of this logic are latched, such that changes cannot occur during harvesting, or during the voltage flip, as this would severely impact performance. The latching of these outputs is allowed because the battery voltage is not expected to change rapidly. The complete circuit uses an area of $31800um^2$ and consumes roughly $105nA$ at a battery voltage of $3.0V$.

5.5. OVER-VOLTAGE PROTECTION IN PIEZO SOURCE MODE

Figure 5.11 shows the equivalent circuit when the PMIC is in piezo source mode, omitting switching and control losses for simplicity. Equations (5.1), (5.2) and (5.4) can be combined to find the expected maximum input current, given by (5.8). R_{out} can be calculated from (4.50) and is found to be 56.4Ω for a switching frequency of $5kHz$ and using the low-power mode. The theoretical maximum rectified voltage V_{rect} can be calculated using (5.9) and amounts to $5.18V$, excluding the voltage ripple effects from the SCPC. This would surely trigger the over-voltage protection, which in turn would dissipate a significant amount of power.

$$I_{p,max} = 2\pi \cdot \sqrt{P_{fbr,mpp} \cdot f_{ex} \cdot C_p} = 2\pi \cdot \sqrt{50mW \cdot 200Hz \cdot 100nF} = 6.28mA \tag{5.8}$$

$$V_{rect,max} = \frac{V_{bat}}{M} + I_{o,max} \cdot R_{out} = \frac{V_{bat} + I_{i,max} \cdot R_{out}}{M} \tag{5.9}$$

$$P_{mpp,fbr} = f_{ex} \cdot C_p \cdot V_{OC}^2 = \frac{I_{p,max}^2}{4\pi^2 \cdot f_{ex} \cdot C_p} \tag{5.10}$$

However, just like with the DC source mode, it is possible to change the SCPC parameters to avoid dissipating energy. Decreasing the output resistance reduces its equivalent voltage drop and therefore reduces the rectified voltage. In the implementation, this is done by increasing the switching frequency to $40kHz$ and using all switching elements (like the regular power mode) instead of only a single switching element per SCPC switch (like in the low-power mode). This decreases R_{out} to 5.79Ω and the maximum rectified voltage to $4.84V$, below the over-voltage protection trigger voltage.

This over-voltage protection mode (increased switching frequency and number of parallel switches) is activated once the OVP signal is high and reset upon starting the voltage flipping operation. This way, the over-voltage protection mode is only activated for the harvesting cycles that require it, as the input power may change over time. Simulations have shown that although the increased switching frequency and number of parallel switches increases switching losses, the additional power consumption is relatively small compared to the output power, as the over-voltage protection mode is only required for high power levels.

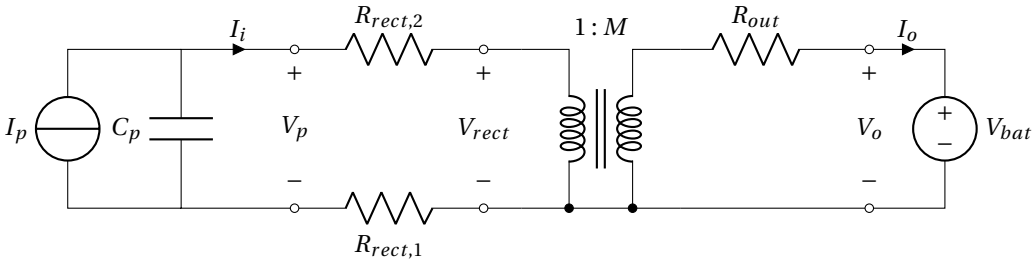


Figure 5.11: Equivalent model for piezo source harvesting mode

5.6. CONTROLLER DESIGN

The scheme shown in Figure 5.4 displays information about the controller design. Three states can be defined:

- Voltage Flip: The voltage on the piezo element is flipped (reversed in polarity) to V_r ($= -\eta_{flip} \cdot V_h$)
- Open Circuit: The piezo current I_p charges the piezo capacitance from V_r to V_h
- Harvesting: The piezo current I_p is harvested at the harvesting voltage V_h ($t = T/2$)

A finite state machine (FSM) is used to implement the piezo harvesting scheme. The 'Voltage Flip' state is split up into two states ('Count Down' and 'Count Up') such that the reversal of the polarity of the rectifier is part of the FSM. Additionally, the amount of states is doubled to seperate the two configurations of the rectifier. As such, a finite state machine with eight states is created. The FSM is shown in Figure 5.12 and more detailed in Table 5.3.

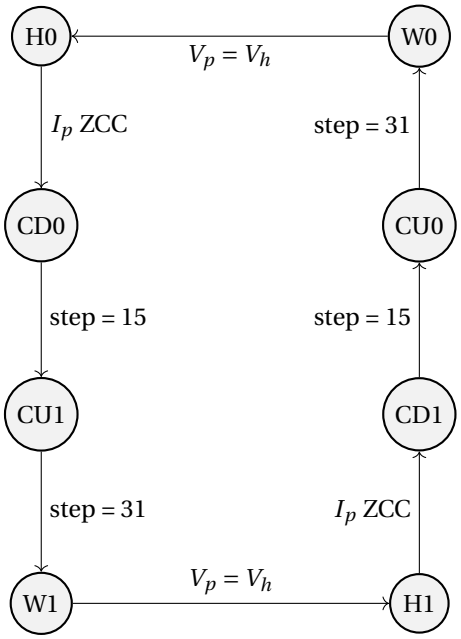


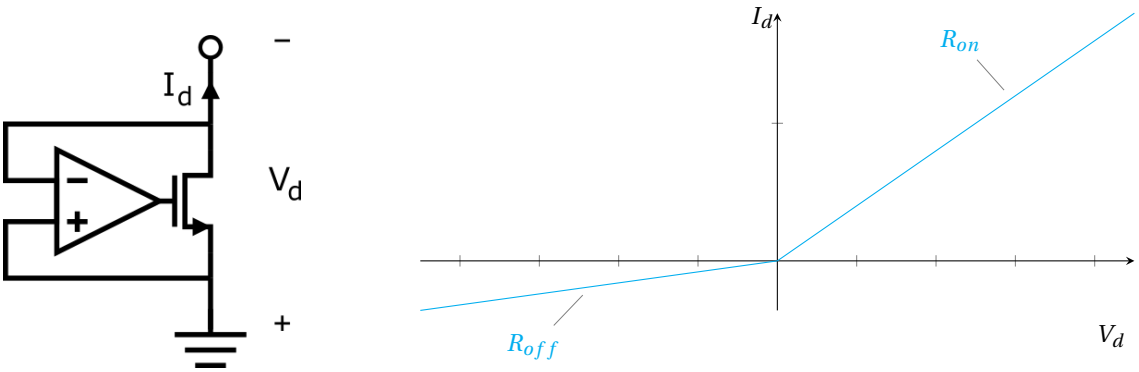
Figure 5.12: Finite state machine (FSM) for piezo harvesting cycles

Table 5.3: FSM state descriptions for piezo harvesting cycle

State		Description	Rectifier Setting	Next State if	Next State
H0	Harvest 0	Harvest I_p with the SCPC at $M = \frac{x}{16}$	A	I_p Zero Current Crossing	SD0
SD0	Step Down 0	Discharge V_p with capacitors	A	Step 15 is reached	SU1
SU1	Step Up 1	Charge V_p with capacitors: rebuild to V_r	B	Step 31 is reached	W1
W1	Wait 1	Open Circuit condition: C_p charged by I_p	B	$V_p = V_h$	H1
H1	Harvest 1	Harvest I_p with the SCPC at $M = \frac{x}{16}$	B	I_p Zero Current Crossing	SD1
SD1	Step Down 1	Discharge V_p with capacitors	B	Step 15 is reached	SU0
SU0	Step Up 0	Charge V_p with capacitors: rebuild to V_r	A	Step 31 is reached	W0
W0	Wait 0	Open Circuit condition: C_p charged by I_p	A	$V_p = V_h$	H0

5.7. CURRENT SENSING RECTIFIER DESIGN

As shown in the previous section, two state changes are initiated by the zero-current crossing (ZCC) of the piezo current I_p. Fortunately, as this piezo current I_p is being harvested by the SCPC, the zero-current crossing can also be detected from the current in the system. Three possible methods are shown. Firstly, a method for doing a zero current crossing detection is by allowing the current to flow trough a shunt resistor and detecting the sign change in the voltage across this resistance. However, a small resistance is preferred for a low voltage drop and low power loss, but this would potentially require a very accurate analog circuit, as the voltage changes over this small shunt resistance would also be very small. This could dissipate a significant amount of power. Secondly, the non-linearity of a diode could be used as a shunt element to require a less accurate read-out of the voltage across the current sensing element. However, this would result in a larger voltage drop due to the forward voltage of the diode, which would result in a significant power loss. Thirdly, an active diode circuit can be used, as seen in [28] and [30].



(a) (b)

Figure 5.13: Active diode circuit (a) and input-output relation (b)

5.7.1. ACTIVE DIODE CIRCUIT

Figure 5.13 shows the active diode circuit and its behaviour. The active diode circuit works as follows:

- For $I_d > 0$, the driver outputs a high signal, ensuring that the resistance of the active diode is the on-resistance of the transistor (R_{on}).[2]
- For $I_d < 0$, the output of the driver is low and the resistance of the active diode is the off-resistance of the transistor (R_{off}).

This circuit does not only reduce the voltage drop between the terminals significant, but also outputs information about the sign of the current, through the output of the driver. Therefore, this would be a suitable solution to measure the zero current crossing.

As [28] and [30] have shown, such a circuit can be integrated into the rectifier by replacing the two switches

[2] The on-resistance and off-resistance are over-simplifications of the actual behaviour of the transistor. In reality, the I-V relationship will be non-linear for both cases.

that connect the inputs to the ground of the system, with active diode circuits. This current sensing rectifier is implemented according to Figure 5.14, where the diodes are realised with active diode circuits. The gate of the transistor in the active diode circuit can also be overwritten with a high signal during the voltage flipping operation (as bi-directional current conduction is required) or with a low signal, depending on the polarity configuration of the rectifier.

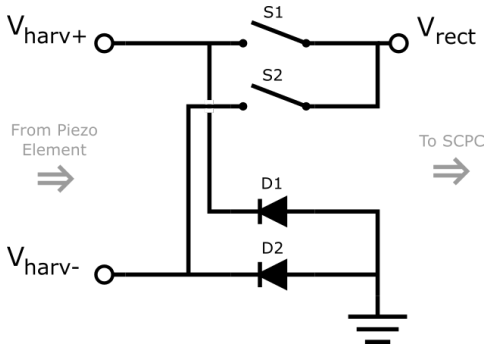
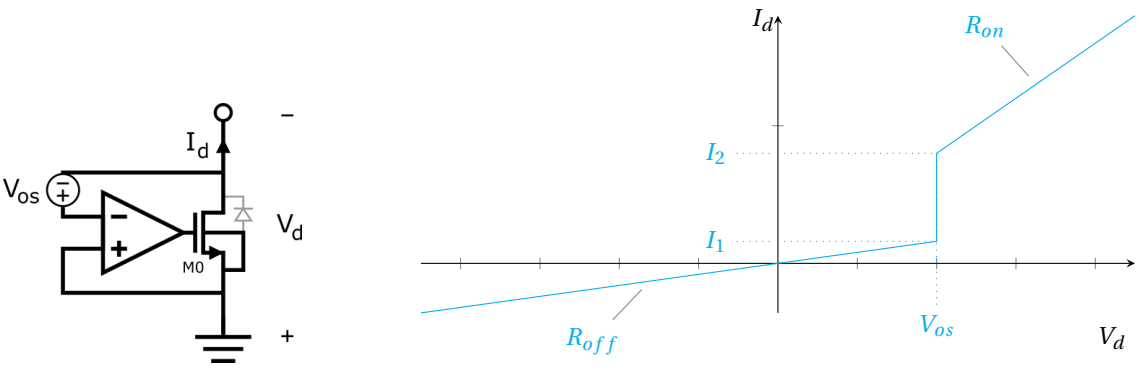


Figure 5.14: Current sensing rectifier

CIRCUIT IMPLEMENTATION

An ideal driver has been assumed, but a real operational amplifier has a limited bandwidth, limited gain and mismatch offset. Especially the last non-ideality is problem. If the mismatch is negative, a negative current of up to $V_{os} \cdot R_{on}$ can be flowing through the transistor, while the driver does not change its output. For this reason, the input referred offset should always be positive as show in Figure 5.15. The gain and bandwidth should be large enough such that the active diode can detect the zero current crossing without too much delay. The active diode circuit then worka as follows:

- For $I_d > I_2$, the voltage drop across the transistor is larger than the offset voltage ($V_d > V_{os}$) and the output of the operational amplifier (V_g) is clipped at V_{dd}. The resistance of the active diode is the on-resistance of the transistor (R_{on}).
- For $I_1 < I_d < I_2$, the operational amplifier behaves as a linear driver for the transistor. The gate voltage is regulated such that $V_d = V_{os}$.
- For $I_d < I_1$, the output of the operational amplifier is $0V$ and the resistance of the active diode is the off-resistance of the transistor (R_{off}).



(a) (b)

Figure 5.15: Active diode circuit (a) and waveform (b)

A two-stage miller compensated operational amplifier circuit is used, such that a rail-to-rail output swing is achieved. The rail-to-rail driving capability allows transistor $M0$ to turn on and off completely. Figure 5.16 shows the implementation of the active diode in transistor level. It operates as follows:

- Transistor $M0$ is a large NMOS device through which the current I_d flows.

Table 5.4: Active diode specifications for $V_{dd} = 3.0V$

V_{os}	$7.48mV$
$V_{os,min,PVT}$	$6.08mV$
$V_{os,mismatch}$	$751uV/\sigma$
R_{on}*	6.8Ω
I_{dd}	$72nA$
Area	$4345um$

* calculated from I_d for $V_{ds} = 100mV$

- Transistors $M4$ to $M8$ and capacitor $C1$ make up the two stage miller compensated operational amplifier and use currents from the current mirror made by transistors $M1$ to $M3$. Transistors $M4$ to $M7$ are sizes such that the mismatch offset meets the requirements. Mirroring transistor $M7$ is 12% smaller than transistor $M6$ such that a positive input referred offset is guaranteed.
- Transistors $M9$ through $M12$ set the correct mode for the active diode circuit. In diode mode, transistors $M9$ and $M10$ (a transmission gate) control the gate of $M0$. In off mode (when the opposite rectifier polarity should be achieved), transistor $M12$ disables transistor $M0$. In switch mode (during the voltage flip), transistor $M0$ is turned on by transistor $M11$ such that it conducts current in both directions. The control signals DIO, SW and OFF originate from the controller (see Section 5.6).
- Transistor $M13$ and $M14$ make signal I_{neg} that outputs information about the current polarity in active diode mode. When the gate voltage of transistor $M0$ is above its threshold, a positive current flows out of its drain, and the I_{neg} output is low.

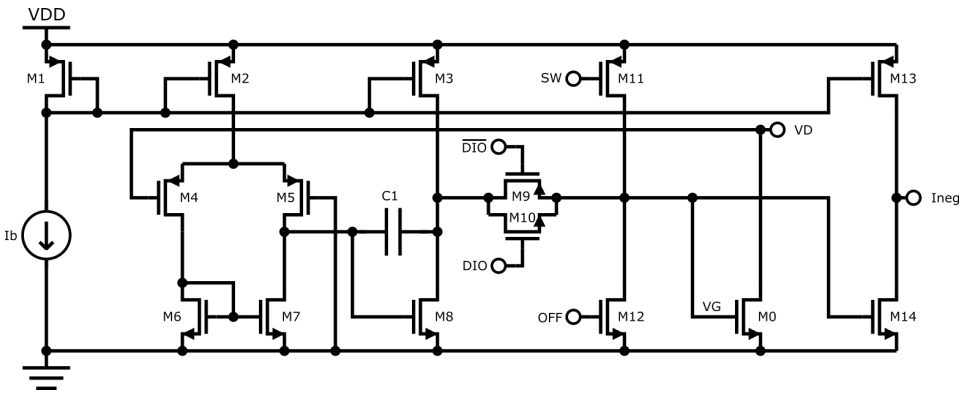


Figure 5.16: Active Diode Implementation

Table 5.4 shows the specifications of the designed active diode circuit for the minimal supply voltage of $3.0V$. The values for offset were chosen such that the minimal input referred offset is positive with a certainty of at least 6σ.

5.7.2. HIGH SIDE & BYPASS SWITCH

Three switches are used in the current sensing rectifier. Two switches are used for the high side switching, connecting either V_{harv-} or V_{harv+} to V_{rect}. The third switch is a larger switch connecting V_{harv+} to V_{rect} in case the rectifier needs to be bypassed.

RECTIFIER BYPASS

In the two different modes of operation (piezo element and DC source harvesting), two different things are expected from the rectifier. For piezo element operations, the rectifier is switching between its two different polarity configurations, which gives dynamic losses, but the on-resistance does not have to be very low, as we expect the piezo element to act as a current source. However, for DC source operations, the rectifier needs to conduct high currents (especially for low voltages and high MPP input powers) and therefore a very low on-resistance is required, but there are no switching losses, as the polarity configuration of the rectifier does not change. Thus it was decided to add a switch that bypasses the rectifier and has a much lower on-resistance

than the switches in the rectifier. For DC source operations, this large bypass switch connects V_{harv+} and V_{rect} together, while the rectifier is inactive.

IMPLEMENTATION

The implementation of the switch is similar to that of the switches in the bootstrapped NMOS switches in the SCPC. However, due to leakage — especially present in certain process and temperature variation corners — the above-threshold gate voltage of the NMOS device may not be sustained, even though it is bootstrapped. The switches in the rectifier need to stay on for longer periods of time: continually for the bypass switch and up to $0.5s$ (half of the period for $1Hz$ excitation) for the high side switches. For this reason, additional circuitry is added to the bootstrapped switch, that continually adds charge to the gate. This circuit is shown in Figure 5.17.

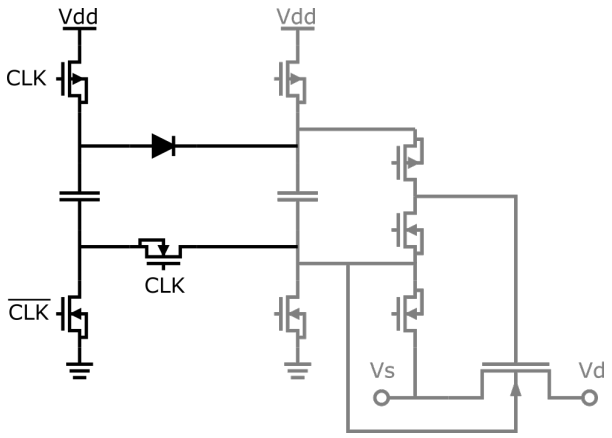


Figure 5.17: Active Diode Implementation *(level shifters for CLK signal not shown)*

To ease implementation, the layout cell of the regular bootstrapped NMOS switch was expanded with the additional circuitry. The charge that is repeatedly added to the gate of the NMOS device increases the gate-source voltage V_{gs} and thus decreases the on-resistance, compared to the regular bootstrapped NMOS switch. The on-resistance of this switch is 5.62Ω with an area of $2275um^2$. A single clocked bootstrapped NMOS transistor was used for the high side switches, as this has a similar on-resistance compared to the switches of the SCPC in low power mode.

The bypass switch needs to be large, as it is required to carry a large amount of current, especially for the worst case scenario. Therefore, multiple of the designed clocked bootstrapped NMOS transistors are placed in parallel to achieve a lower on-resistance. Similar to the SCPC implementation, there is a trade-off between area and worst case efficiency. Figure 5.18 shows this trade-off. It was chosen that $1.76mm^2$ (a 10% increase in area) was a suitable size. For this 39 switch elements are routed in parallel.

5.8. SWITCHING INPUT CAPACITOR

Simulations have shown that for the first cycles after start-up, the SCPC has difficulty reaching its steady state operating point, while reaching that settled operating point is what is needed for the voltage flipping operation to be preformed correctly, as the settling of the SCPC brings the floating capacitors to the correct voltage. The root of the problem is that the input capacitances (piezo capacitances in this case, namely up to $100nF$) is too small in comparison with the floating capacitors ($1uF$).

This issue is solved by adding an large capacitor ($1uF$) into the design that can provide additional input capacitance to the SCPC input. However, the voltage on the input node of the SCPC changes significantly during the voltage flipping operation. As such, the added capacitor is not permanently connected to the SCPC input, but is disconnected during the voltage flipping operation.

An added benefit of this switching input capacitor is that it allows an easy recognition of the $V_h = V_p$ state change trigger of the finite state machine. For the states $W0$ and $W1$, the input capacitor is connected to the input of the SCPC (which is inactive during that period) and thus to the rectified voltage of the rectifier (V_{rect} in Figure 5.14). For $V_p < V_h = V_{C,added}$ the open circuit condition is guaranteed, as the active diodes ($D1$ and

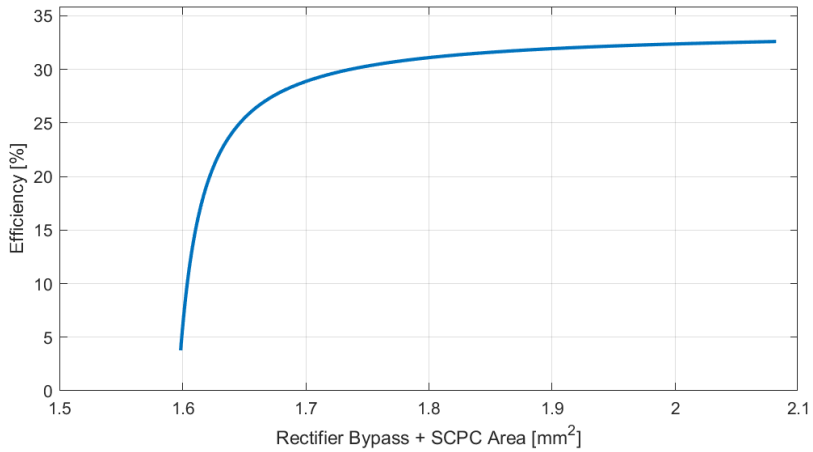


Figure 5.18: Effect of the rectifier bypass area on the worst case efficiency

$D2$) are not conducting. As the piezo voltage V_p reaches V_h, one of the active diode circuits (dependent on the polarity configuration of the rectifier) starts conducting. The output of the driver of this conducting active diode circuit then indicates that $V_p = V_h$ and that the FSM should go to the next state (either $H0$ or $H1$).

IMPLEMENTATION

Capacitor C_{aux} from the auxiliary supply is used to implement this feature, as it is already connected to the input of the SCPC (because the SCPC only uses step-down conversion ratios in piezo source mode). However, it should be disconnected temporarily during the voltage flip. This is not a problem for the ESD protection as the voltage on the auxiliary supply capacitor remains constant during this very short period of time ($310us$).

5.9. CONCLUSION

This chapter has discussed the design of the piezo harvesting interface that yields an increased output power. The SCPC designed in Chapter 4 enabled the voltage flipping rectifier to reach a rebuild voltage of up to 0.9375 times the harvesting voltage, reaching a theoretical maximum output power improvement of 32 times. A low power mode was added to the SCPC to decrease the inevitable circuit losses and the conversion ratio setting circuit that is used during the harvesting was shown. An over-voltage protection scheme was added to reduce additional losses in case the over-voltage protection was triggered. The controller design for the designed interface was discussed as well as the current sensing rectifier that is required for said controller. Lastly, the switching input capacitor was implemented by the auxiliary supply, such that the SCPC would settle correctly during piezo harvesting.

6

CONTROLLER DESIGN

6.1. INTRODUCTION

This chapter discusses the controller design for the created system. Firstly, the differentiation between the two types of sources is discussed. Secondly, the finite state machine design and implementation are shown. Lastly, the debug module design is discussed.

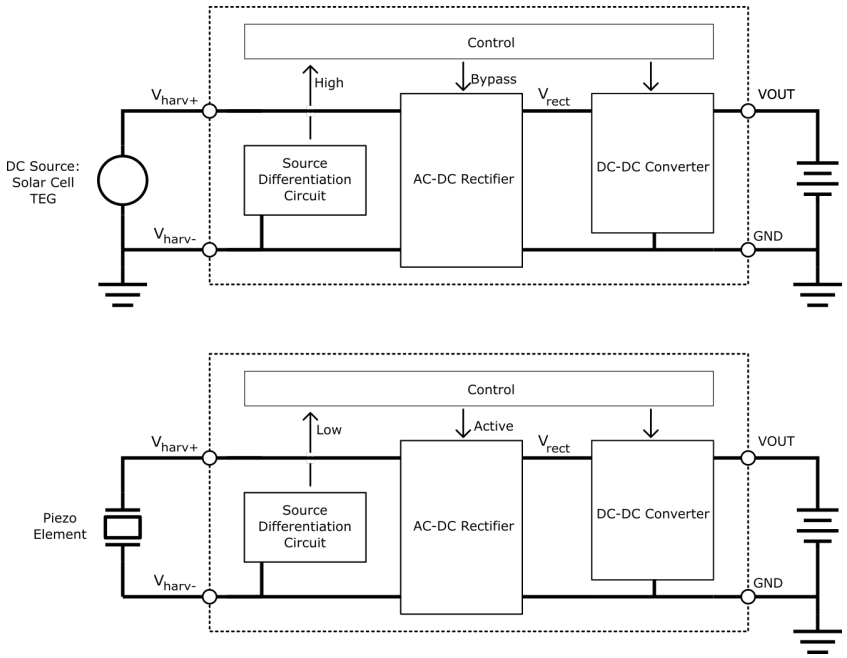


Figure 6.1: Current sensing rectifier

6.2. SOURCE DIFFERENTIATION

A circuit is required that is able to differentiate between piezo-electric harvesting elements and DC harvesting elements (photovoltaic cells and thermo-electric generators), without requiring any other external source of information that would require additional pins. The block diagram in Figure 6.1 shows the difference between connecting the two types of sources to the two input pins: for the DC source, the V_{harv-} node is connected to the ground node of the system, while for piezo sources, this is not the case and the node is floating (assuming the rectifier is inactive). This information is used to differentiate between the two source types:

- When a DC source is connected, the V_{harv-} node is connected to ground. The source differentiation circuit should give a high output signal, notifying the controller that a DC source is connected.

- When a piezo source is connected, the V_{harv+} node is only connected to one of the piezo element ports. The source differentiation circuit should give a low output signal, notifying the controller that a piezo source is connected.

IMPLEMENTATION

The circuit implementation of the source differentiation subsystem is shown in Figure 6.2. Upon enabling the circuit, the V_{harv-} pin is pulled to V_{dd} by transistor $M2$ if possible. In the case that a DC source is connected, V_{harv-} is connected to the ground node externally and the voltage does not rise. Therefore, the output remains high. In the case that a piezo source is connected, V_{harv-} is only connected to the piezo element, and is therefore able to rise to above the threshold voltage of transistor $M5$ and the output is low. The rising of node V_{harv-} causes V_{harv+} to rise as well, because both are connected to the piezo element. Especially in case of an initial voltage on the parasitic capacitance of the piezo element, this voltage may rise above the technology voltage and damage the devices. In order to prevent this, the V_{harv+} node is also pulled to V_{dd}. Diodes $D1$ and $D2$ prevent a conduction path from V_{harv-} or V_{harv+} to V_{dd} when the input voltage is higher than the supply voltage, but the circuit is not enabled.

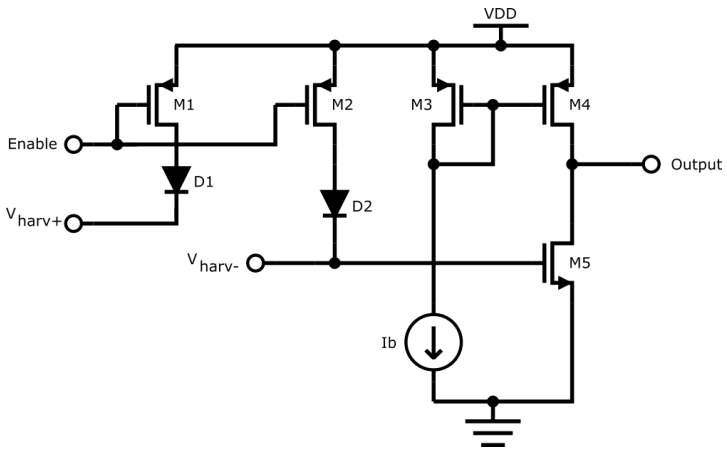


Figure 6.2: Source differentiation circuit

The power consumption of this circuit is relatively high when it is enabled and a DC source is connected, as transistor $M2$ and diode $D2$ connect the supply to the ground node. However, as this operation is only required upon enabling the PMIC and for a short time (during a single clock period). After this, the controller makes the decision to continue to either DC source or piezo source harvesting techniques.

When the circuit is not enabled, a current of only $12nA$ is required to power the output stage. This feature is used in one of the fault detections: in case the controller goes into DC source mode, while a piezo element is connected, the input of the SCPC (V_{rect}) settles to a positive voltage. As V_{rect} and V_{harv+} are connected together by the rectifier bypass, and the voltage over the piezo element will at some point be zero (either due to a zero crossing, or the discharging of the parasitic capacitance due to the finite isolation resistance of the piezo element). Therefore V_{harv-} rises as well and the output of the source differentiation circuit is low. This is can be noticed by the controller and the system can be reset.

6.3. FINITE STATE MACHINE

The finite state machine from Section 5.6 is extended to also include the source differentiation. The FSM is shown in Figure 6.3 and more detailed in Table 6.1. From the 'Reset' state, which is the initial state as the system is enabled, the 'Test Source' state is entered, in which the source differentiation circuit tests which source type is connected. If a DC source is connected, the 'DC Source' state is entered. In this state, the rectifier is bypassed and the SCPC is operated according to the inputs that set the SCPC settings. If a piezo source is connected, the state machine enters the 'Settle' state, in which time is taken to let the SCPC settle. This is vital for the voltage flipping operation, as it will bring the capacitors to the expected voltage levels. After the appropriate number of clock cycles the SCPC is expected to have settled and the piezo harvesting cycle can be started.

Table 6.1: FSM state descriptions (* = except when a time-out is triggered, then enter the Reset state)

State		Description	Rectifier Setting	Next State if	Next State
R	Reset	State entered upon enabling the system	-	-	T
T	Test DC	Use Source Differentiation Circuit to determine the source type	-	DC Source = 0 DC Source = 1	S DC
DC	DC Source	Operate SCPC according to external settings	Bypass	DC Source = 0	R
S	Settle	Let the SCPC settle in several clock cycles	A	'settled' timer finishes	H0
H0	Harvest 0	Harvest I_p with the SCPC at $M = \frac{x}{16}$	A	I_p Positive to negative transition	SD0*
SD0	Step Down 0	Discharge V_p with capacitors	A	Step 15 is reached	SU1
SU1	Step Up 1	Charge V_p with capacitors: rebuild to V_r	B	Step 31 is reached	W1
W1	Wait 1	Open Circuit condition: C_p charged by I_p	B	$V_p = V_h$	H1*
H1	Harvest 1	Harvest I_p with the SCPC at $M = \frac{x}{16}$	B	I_p Positive to negative transition	SD1*
SD1	Step Down 1	Discharge V_p with capacitors	B	Step 15 is reached	SU0
SU0	Step Up 0	Charge V_p with capacitors: rebuild to V_r	A	Step 31 is reached	W0
W0	Wait 0	Open Circuit condition: C_p charged by I_p	A	$V_p = V_h$	H0*

Two types of fault detection are also introduced, to make the design resilient against erroneous signal for the source differentiation circuit:[1]

- For states in the piezo harvesting cycle that are not exited via a timed event ($H0$, $H1$, $W0$ and $W1$) a time-out can trigger a state change to the 'Reset' state. This ensures that if the state changes are not triggered in time (1 second), the system is reset. Normally, this would not occur, as the lowest expected excitation frequency is $1 Hz$ and one half of the piezo harvesting cycle should always be done within 0.5 seconds. This way, the time-out triggers a reset when the source differentiation circuit gives a faulty output and the piezo harvesting cycle is entered while a DC source is connected.
- If the 'DC Source' state is reached, while a piezo element is connected, the source differentiation circuit should eventually notice this and with the corrected output signal, make the state machine return to the 'Reset' state.

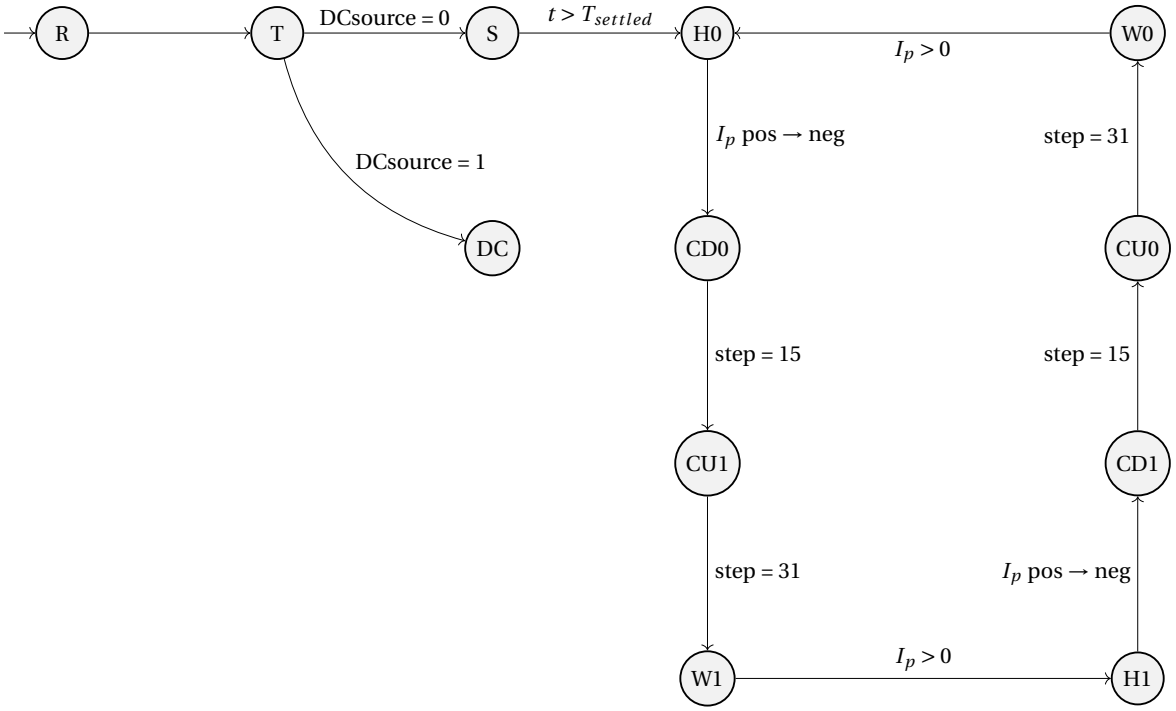


Figure 6.3: Finite state machine (FSM) diagram

[1] Please note that these are not included in the diagram

IMPLEMENTATION

The finite state machine is implemented with a synchronous sequential circuit, using logic gates in the combinatorial logic and D flip-flops as memory elements. The same $100kHz$ signal that is used for the timing of the voltage flip, is used to provide a clock signal for this circuit.

Secondly, the FSM inputs are implemented. The time-dependent (or rather clock cycle number dependent) FSM input signals ($T_{settled}$, $T_{time-out}$, 'step=15' and 'step=31') are constructed using a counter, implemented with a cascade of D flip-flops. The 'DCsource' and '$I_p > 0$' signals originate from the source differential circuit and current sensing rectifier respectively. A separate synchronous sequential circuit is used to detect a positive-to-negative transition for the piezo current I_p, using the signal provided by the current sensing rectifier.

Lastly, the control for the 28 switches in the SCPC is implemented with lookup tables. Inputs for these lookup tables are the FSM state, the conversion ratio setting (for piezo source mode), $\vec{a}$ & $\vec{b}$ (for DC source mode) and the SCPC phase or voltage flipping phase.

6.4. DEBUG MODULE

An important part of the design verification is be testability. Although the subsystems and final design have been simulated extensively in for both nominal conditions and process and temperature variations, circuits may behave differently than expected in a taped-out IC. For this reason a debug module is created, which is able to override the following control signals, in case they do not perform as required:

- 'DCsource' can be overridden to force either the DC source mode or piezo source mode.
- 'OVP' signal can be overridden, such that the over-voltage protection power mode is not activated. Additionally, current sinking in the over-voltage protection subsystem can be disabled.
- The output of the conversion ratio setting circuit can be overridden, to force a certain conversion ratio for the piezo harvesting mode.
- The output of the current sensing rectifier can be overridden, to control the FSM state changes externally.

6.5. CONCLUSION

This chapter has shown the design for the controller and its supporting systems. The design and implementation of the source differentiation circuit was shown, which was designed to generate a signal for the controller such that either of the two operating modes (DC source mode or piezo source mode) can be used. Secondly, the finite state machine was designed and implemented with logic gates to ensure robust control of the system. Lastly, a debug module was designed, such that the system will be testable even if a subcircuit outputs an erroneous signal.

7

RESULTS

7.1. INTRODUCTION

This chapter shows the simulations results of the proposed design. The results are separated into two sections. Firstly, the performance of the design in DC source mode will be discussed. The analytical model is compared for verification. Secondly, the performance of the design in piezo source mode is discussed. These results are also compared to the expected results. Lastly, the effects of process variation and different operating temperatures are discussed.

7.2. DC SOURCE PERFORMANCE

The results for DC sources is split into two parts. Firstly, the performance for TEGs (and other linear sources) is discussed. The simulation results are compared to the analytical model of the system (see Section 3.4), which was used to find the optimal conversion ratio and switching frequency for the different operating conditions. After verification of this model, the performance for non-linear sources (such as solar cells) is discussed.

7.2.1. LINEAR SOURCES

Figure 7.1 shows the power consumption and losses for different use cases. The internal losses of the SCPC include the conduction losses and parasitic losses of the switches (see Section 4.2.3 and 4.3.1). The different operating conditions have been selected to illustrate the effect of different input powers and voltages.

The power losses from MPP mismatch, rectifier losses, internal SCPC losses and switching losses of the SCPC generally have the most significant impact. These losses have been modelled in Chapter 4. Figure 3.3 shows the complete equivalent models for the design. From the simulation results, the power and current consumption of the logic and supporting circuits are estimated to be $2.4uW$ and $800nA$ respectively at a battery voltage of $3.0V$.

CONTROL & SUPPORT CIRCUIT LOSSES

The following power losses are a result of the implementation of control and support circuits. The behaviour of these losses are affected by different parameters.

Delay Element Losses

The losses of the delay elements are highly dependent on the switching frequency, as each switching action requires gate capacitances in the delay elements to be charged and discharged. However, as these losses are insignificant compared to the SCPC losses (more than 100x smaller in general), these do not require to be modelled.

Logic & Debug Losses

The logic and debug subcircuit losses are moderately dependent on the switching frequency. One component of these losses is very dependent on the switching frequency (such as the lookup tables for the switch control)

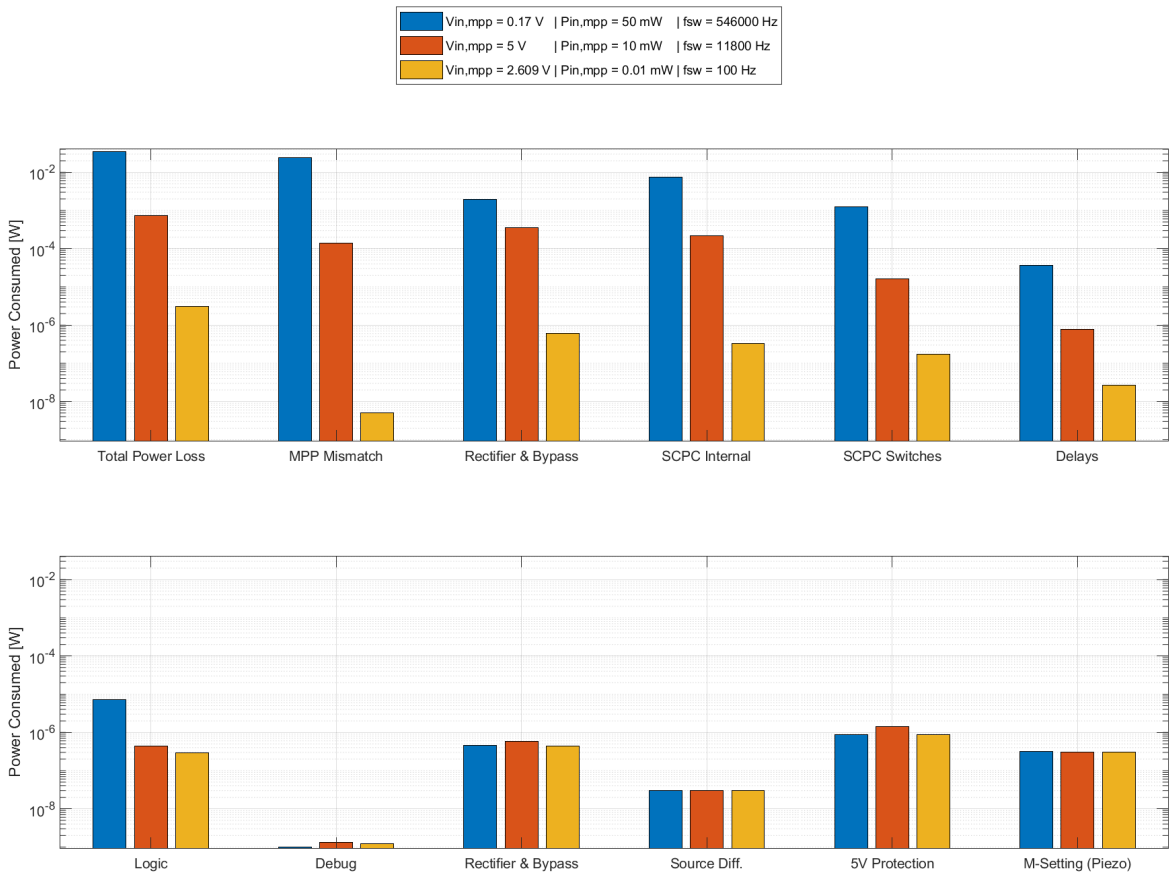


Figure 7.1: Comparison power losses from simulations with $V_{dd} = 3.0V$

while another part is independent of the switching frequency (such as the finite state machine and clock divider for the logic clock). The switching frequency dependent losses are again small relative to the SCPC losses, but this is not necessarily the case for the losses independent on the switching frequency.

Other Losses

The remaining losses (rectifier supply, auxiliary supply, source differentiation circuit, active 5V protection circuit and conversion ratio setting circuit) show very little or no dependency on the switching frequency. No variation in losses is expected from these circuits, except for a slight increase of the protection circuit consumption for input voltages higher than the battery voltage, as the resistive ladder dissipates more power in these cases.

VERIFICATION OF ANALYTICAL MODEL

With the losses for the logic and supporting circuits modelled, the analytical model is complete. The expected performance is shown in Figure 7.2.

To analyse the performance of the implementation of the design, and to verify the analytical model, several simulations have been executed. A total of 30 simulations were run for different MPP input voltages and power levels. The results are shown in Table 7.1. The relative error of the analytical model was computed using (7.1). The relative error is also shown in Figure 7.3.

$$\epsilon = \frac{\eta_{sim} - \eta_{model}}{\eta_{model}} \cdot 100\% \tag{7.1}$$

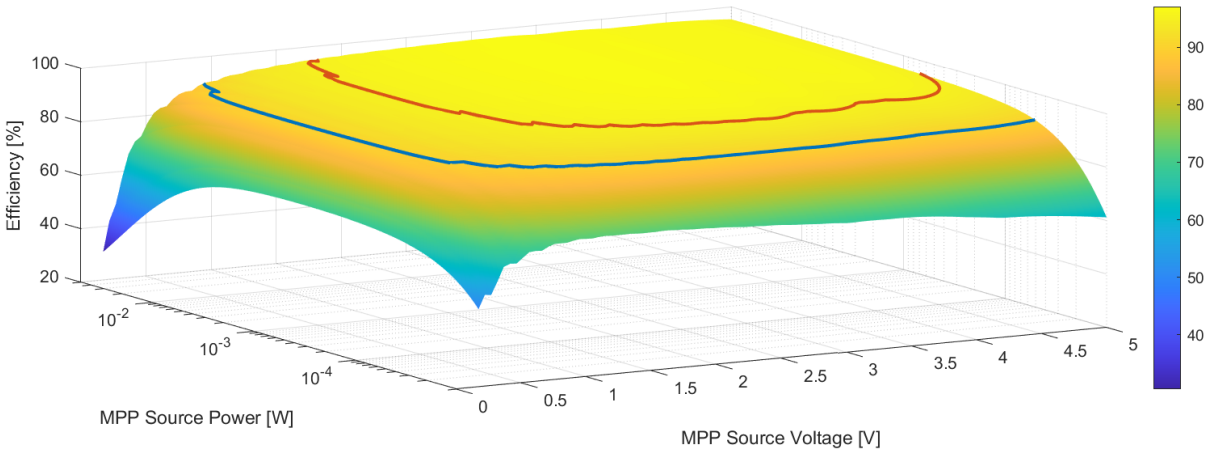


Figure 7.2: Expected performance over the operating range or $V_{bat} = 3.0V$ *(the red and blue lines in the plot represent the* 95% *and* 90% *efficiency boundaries respectively)*

Table 7.1: Efficiency from Analytical Model (A) in %; Efficiency from Simulations (S) in %; Relative Error of Analytical Model (ϵ) in %

$V_{in,mpp} \rightarrow$	$170mV$			$1.39V$			$2.61V$			$3.83V$			$5V$		
$P_{in,mpp} \downarrow$	A	S	ϵ	A	S	ϵ	A	S	ϵ	A	S	ϵ	A	S	ϵ
$10\mu W$	49.1	50.2	2.22	72.1	71.6	-0.66	70.6	69.3	-1.87	69.4	*	*	65.6	*	*
$100\mu W$	68	68.8	1.19	92.6	92.1	-0.541	94.6	92.9	-1.83	94.7	*	*	93.3	*	*
$1mW$	69.4	70.5	1.59	94.5	94	-0.51	96.5	95.4	-1.16	96.6	94.7	-1.98	95.2	92.5	-2.79
$10mW$	59	60.9	3.16	94.6	94.1	-0.478	96.7	95.6	-1.11	96.8	95	-1.85	95.3	92.7	-2.77
$22mW$	46.2	46.8	1.29	94.3	94.2	-0.107	96.6	95.6	-1.06	96.8	95	-1.83	95.3	92.8	-2.65
$50mW$	30.5	30.4	-0.471	93.4	92.9	-0.517	96.4	95.9	-0.524	96.6	95.1	-1.59	95.2	93	-2.36

* The simulation results for these operating conditions were omitted due to some unexpected leakage in the rectifier bypass switches, which degraded the performance significantly

Upon analysing the error in the analytical model, it seems that an increasing voltage leads to a decrease in simulated performance relative to the expected performance. The cause for this is the inaccurate modelling of the switches in the SCPC circuit. Section 4.3.1 has shown that the performance of the bootstrapped switch decreases with increased terminal voltages: the on-resistance and energy consumption per cycle increase. As the input voltage of the SCPC increases, the internal voltages are also likely to increase. Although this has been adjusted for in the model, the dependency has not been removed completely.

Nonetheless, the analytical model can predict the SCPC performance with a maximum error of ~ 3%. This enables a performance analysis of non-linear sources without the need to simulate non-linear sources in a simulator. This is given in Section 7.2.2.

SIMULATION RESULTS FROM PARASITIC EXTRACTION

Table 7.2 shows the results of simulations with parasitics extracted from the layout. Some of the results show a worse performance than what is expected from the model and the transistor level simulations. Two of these occur for low power operations ($P_{in,mpp} = 10\mu w$). It is likely that due to the parasitics, the control and supporting circuits consume slightly more power, which only has a noticeable impact for use cases with low

Table 7.2: Extracted layout simulations results for a linear DC source

$V_{in,mpp}$	$P_{in,mpp}$	η_{model}	η_{sim}	η_{pex}
$170mV$	$50mW$	30.5%	30.4%	26.1%
$170mV$	$1mW$	69.4%	70.5%	69.5%
$170mV$	$10\mu W$	49.1%	50.2%	44.9%
$2.61V$	$1mW$	96.5%	95.4%	96.2%
$2.61V$	$10\mu W$	70.6%	69.3%	65.4%
$5V$	$50mW$	95.2%	93.0%	93.4%

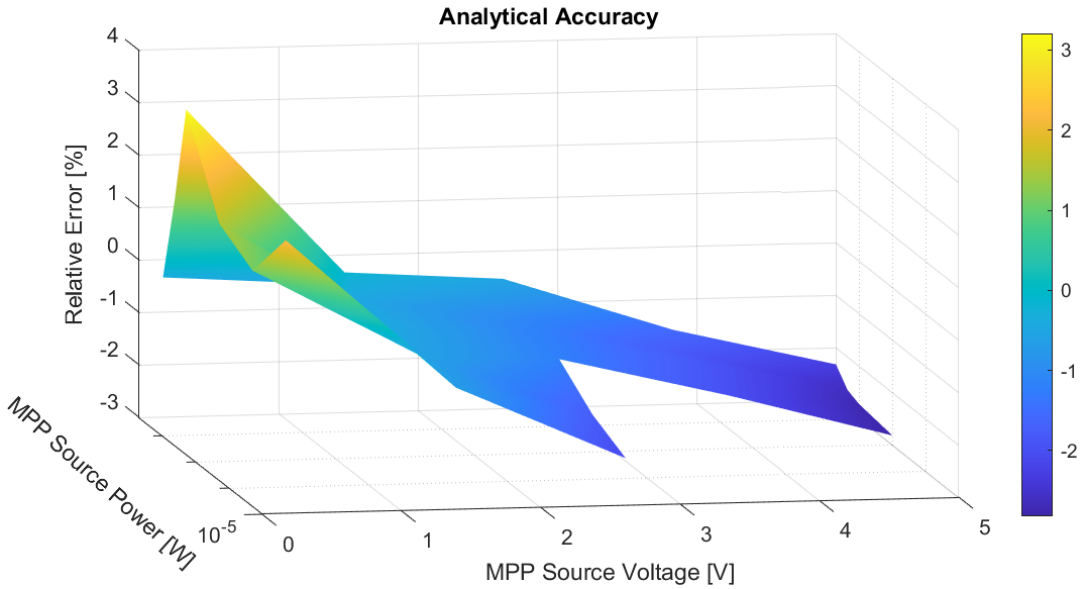


Figure 7.3: Relative error in the analytical model

input powers. The third indiscrepancy occurs for the use case where $V_{in,mpp} = 170mV$ and $P_{in,mpp} = 50mW$. This is likely due to the increase in conduction resistance in the SCPC due to the metal interconnects. The finite resistance of the metal interconnects that connect the switches to the capacitor terminals, input node, output node and ground increases FSL resistance and therefore the conduction resistance. The other use cases show no significant difference between the regular simulations and those with extracted parasitics.

7.2.2. NON-LINEAR SOURCES

Solar cells are the second type of DC sources that the PMIC is designed for. A solar cell can be classified as a non-linear source, as its source resistance changes with the output voltage. Achieving (near) MPP output power is often harder for a non-linear source compared to a linear sources. The reason for this is that the output power around the MPP drops faster for non-linear sources, as shown in Figure 7.4. This figure shows that the narrow P-V curve for the non-linear source with a fill factor of 0.7 (the ratio between the MPP power and the product of the short-circuit current and open circuit voltage). In order to achieve a (near) MPP output power, a more accurate matching of the MPP input voltage is required.

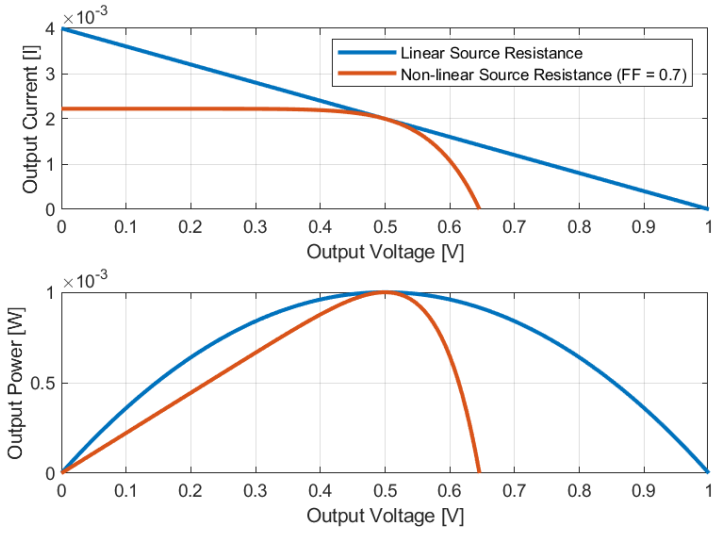


Figure 7.4: I-V and P-V curves of a linear and non-linear source with the same MPP power and voltage

The designed SCPC has a large range of conversion ratios and is therefore able to match a large range of input voltages, with a high accuracy. For this reason, the efficiency for a non-linear DC source is similar to the efficiency of a linear DC source, as shown in Figure 7.5. However, it can be observed that the plot is not as flat as that of the linear DC sources, as a result of the sharper P-V curves.

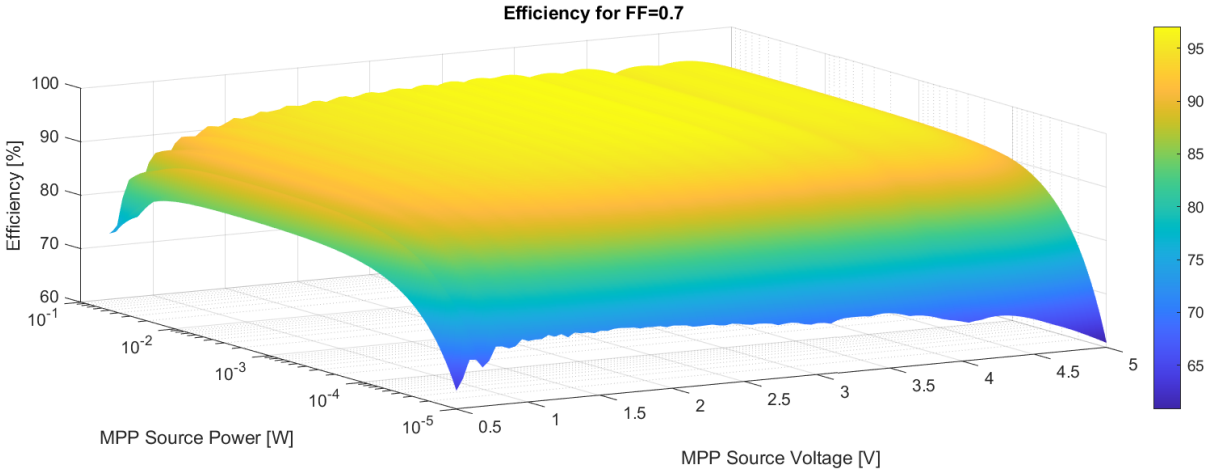


Figure 7.5: Expected performance for a non-linear DC source with a fill factor of 0.7

7.3. PIEZO SOURCE PERFORMANCE

The performance for piezo energy harvesting has also been simulated for a range of input powers ($1\mu W$ to $50mW$) and piezo capacitances ($1nF$ to $100nF$). As several excitation cycles are required to evaluate the performance properly, the performance is evaluated for an excitation frequency f_{ex} of $200Hz$ to reduce simulation time. Several simulations at lower excitation frequencies showed no significant deviations from the expected results.

The key performance parameter is the Maximum Output Power Improvement Rate (MOPIR), which is the ratio between the output power of the system and the output power of an ideal full bridge rectifier at its maximum power point. Equations (5.1) and (5.4) are used to compute the MOPIR for a lossless system in (7.2), and the expected MOPIR for a system with losses in (7.5).

$$MOPIR_{ll} = \frac{P_{out}}{P_{fbr,mpp}} = \frac{2 \cdot f_{ex} \cdot C_p \cdot \left(V_h \cdot V_{OC} \cdot 2 - V_h^2/16\right)}{2 \cdot f_{ex} \cdot C_p \cdot \left(V_{h,fbr} \cdot V_{OC} \cdot 2 - V_{h,fbr}^2 \cdot 2\right)} = \frac{V_h \cdot V_{OC} \cdot 2 - V_h^2/16}{V_{h,fbr} \cdot V_{OC} \cdot 2 - V_{h,fbr}^2 \cdot 2} \tag{7.2}$$

$$V_{h,fbr} = min\left(\frac{V_{OC}}{2}, 5\right) \tag{7.3}$$

$$V_h = \frac{V_{bat}}{M} \tag{7.4}$$

$$MOPIR_{expected} = \frac{P_{out}}{P_{fbr,mpp}} = \frac{2 \cdot f_{ex} \cdot C_p \cdot \left(V_h \cdot V_{OC} \cdot 2 - V_h^2/16\right) - P_{loss}}{2 \cdot f_{ex} \cdot C_p \cdot \left(V_{h,fbr} \cdot V_{OC} \cdot 2 - V_{h,fbr}^2 \cdot 2\right)} \tag{7.5}$$

Table 7.3: Power output in μW and loss results for piezo element harvesting simulation for $f_{ex} = 200Hz$ and $V_{bat} = 3.0V$

$C_p \rightarrow$	$1nF$		$3nF$		$10nF$		$30nF$		$100nF$	
$P_{mpp,fbr} \downarrow$	$P_{out,sim}$	P_{loss}	$P_{out,sim}$	P_{loss}	$P_{out,sim}$	P_{loss}	$P_{out,sim}$	P_{loss}	$P_{out,sim}$	P_{loss}
$1\mu W$	-1.15	8.48	3.78	8.31	11.4	8.52	19	9.47	2.59	27.9
$3.5\mu W$	5.44	8.69	14.9	8.97	31.9	9.52	54	11.7	73.4	25
$10\mu W$	15.2	9.01	31.8	9.53	62.5	10.8	107	13.9	167	32.2
$100\mu W$	66.4	11.2	120	13.8	224	18.1	385	28.3	681	52
$1mW$	228	18	400	26	737	39	1270	68	2270	151
$10mW$	741	39	1290	61	2360	104	4080	181	7250	508
$50mW$	1660	85	2890	132	5230	285	8680	866	16000	1407

Table 7.4: Piezo element MOPIR for lossless system (M_{ll}) and simulated results (M_{sim}) for $f_{ex} = 200Hz$ and $V_{bat} = 3.0V$

$C_p \rightarrow$	$1nF$		$3nF$		$10nF$		$30nF$		$100nF$	
$P_{mpp,fbr} \downarrow$	M_{ll}	M_{sim}	M_{ll}	M_{sim}	M_{ll}	M_{sim}	M_{ll}	M_{sim}	M_{ll}	M_{sim}
$1\mu W$	7.33	-1.15	12.1	3.78	19.9	11.4	28.5	19	30.5	2.59
$3.5\mu W$	4.04	1.55	6.82	4.26	11.8	9.11	18.8	15.4	28.1	21
$10\mu W$	2.42	1.52	4.13	3.18	7.33	6.25	12.1	10.7	19.9	16.7
$100\mu W$	1.12	0.956	1.41	1.26	2.42	2.24	4.13	3.85	7.33	6.81
$1mW$	0.937	0.867	0.991	0.93	1.12	1.06	1.41	1.34	2.42	2.27
$10mW$	0.892	0.847	0.907	0.866	0.937	0.898	0.991	0.949	1.12	1.04
$50mW$	0.881	0.838	0.888	0.849	0.9	0.854	0.922	0.838	0.967	0.889

7.3.1. OUTPUT POWER

The simulation results are shown in Table 7.3 and Figure 7.6. The losses in the system have multiple origins. The control circuits consume a certain amount of power. Just like for the DC source operations, this is roughly $2.4\mu W$. The switching actions (during harvesting and during the voltage flip) also introduce losses. The increase in power loss for larger piezo capacitances and input power has multiple causes.

As the input power and/or piezo capacitance are increased, the voltage rises faster in the open circuit condition ($t_r \rightarrow t_h$), reaches the start of the harvesting period t_h earlier. This therefore increases the time the current is harvested ($t_h \rightarrow t_f$), increasing switching and parasitic losses in the SCPC, as the number of SCPC cycles increases. This is one of the causes the power loss increases when increasing input power and piezo capacitance.

Secondly, the over-voltage protection mode (see Section 4.5.2) is activated for larger current. The total switch size is increased as well as the switching frequency of the SCPC to decrease its output resistance. This increases switching and parasitic losses in the SCPC.

Besides these effects, as shown in Section 5.2.2, the voltage flip performs more poorly for larger piezo capacitance. More of the available current is required to charge the piezo capacitance up to V_h, thus less current is harvested. Moreover, the voltages on the floating capacitors have changed slightly during the flipping operation, which is corrected by the SCPC, but does also require a little bit of extra power.

7.3.2. MOPIR

Table 7.4 and Figure 7.7 show the MOPIR that was deducted from the simulated results. From the simulation results, the losses are estimated and the general trend in relation to the open-circuit voltage V_{OC} is shown for the region where the losses have the highest impact on the MOPIR.

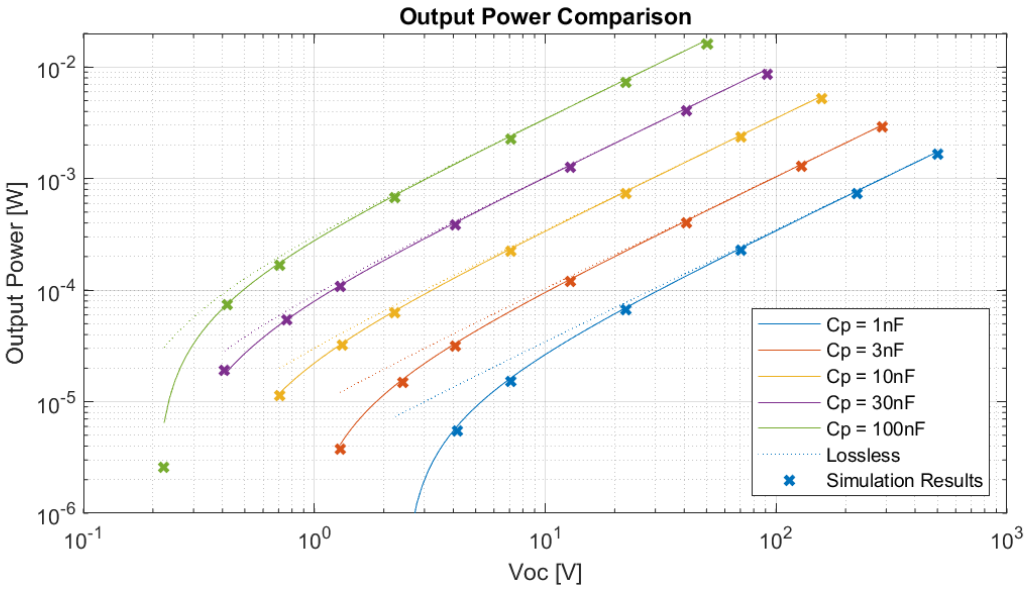


Figure 7.6: Output power across the operating region (for $f_{ex} = 200Hz$ and $V_{bat} = 3.0V$)

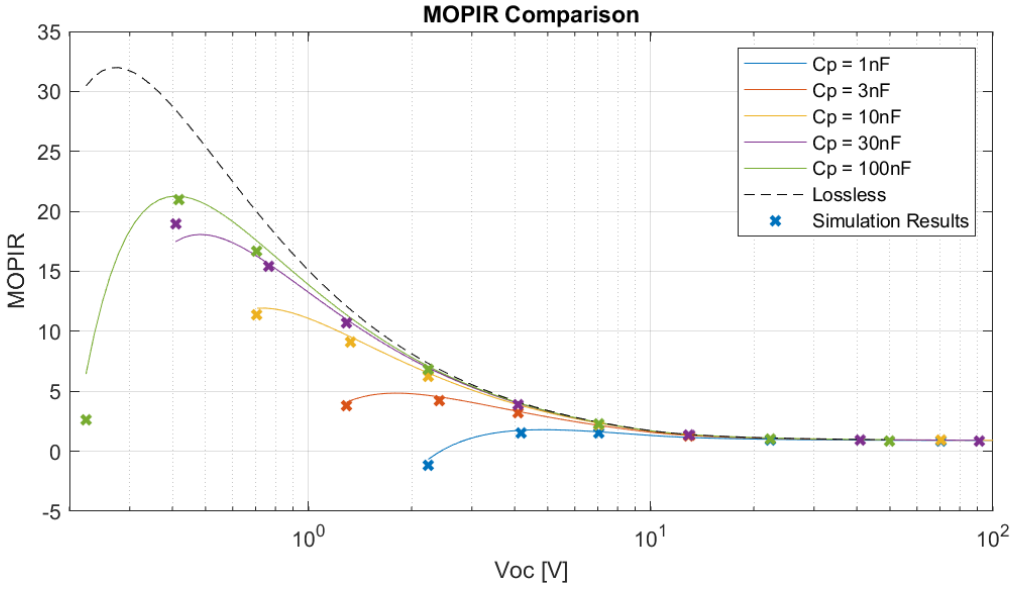


Figure 7.7: MOPIR across the operating region (for $f_{ex} = 200Hz$ and $V_{bat} = 3.0V$)

7.3.3. PARASITIC EXTRACTION RESULTS

Table 7.5 shows the simulations result that were obtained after extracting the parasitics from the layout of the design. It shows that for all cases, the performance is decreased slightly. The probable causes for this are the increased loss from charging parasitic capacitances, as well as a change in the timing of the harvesting cycle due to parasitics in the analog circuits (namely the active diode circuit).

7.3.4. COMPARISON TO STATE-OF-ART

Table 7.6 shows how the proposed design compares to other piezo harvesting interfaces using capacitors for voltage flipping. The increased voltage flipping efficiency yields a significantly higher MOPIR compared to the prior art. The larger external capacitors and the matching of the SCPC and FCR operations are the largest contributors to this increased voltage flipping efficiency. Although the total flipping capacitance is significantly higher that that of the prior art, it should be kept in mind that this system is also able to do DC-

Table 7.5: Extracted layout simulations results for a piezo source (for $f_{ex} = 200Hz$ and $V_{bat} = 3.0V$)

C_p	$P_{fbr,mpp}$	$MOPIR_{lossless}$	$MOPIR_{sim}$	$MOPIR_{pex}$
$100nF$	$3.5\mu W$	27.1	21.0	20.0
$100nF$	$10\mu W$	19.9	16.7	15.4
$10nF$	$10\mu W$	7.33	6.25	5.71
$100nF$	$10mW$	1.12	1.04	0.72

Table 7.6: Comparison to the state-of-art in piezo harvesting

	This Work	JSSC'17 [28]	JSSC'17 [41]
Energy Extration Technique	FCR & SCPC Integration	Flipping Capacitor Rectifier	SSHC
Key Component	Off-chip Capacitors	On-chip MIM Capacitors	Off-chip Capacitors
Total Flipping Capacitance	$4\mu F$	$1.44nF$	$360nF$
Piezo Capacitance	$1-100nF$	$80pF$	$45nF$
Chip Area	$2.1mm^2$	$1.7mm^2$	$2.9mm^2$
Voltage Flipping Efficiency	0.9375	0.85	0.8
MOPIR	$20.0x$	$4.83x$	$9.7x$
Output Power	$10\mu W - 6.2mW$	$50.2\mu W$	$161.8\mu W$
Operating Frequency	$1-200Hz$	$110kHz$	$92Hz$

	JSSC'19 [42]	JSSC'20 [43]	JSSC'20 [30]
Energy Extration Technique	Split Electrode SSHC	Multi-Level SSHC on capacitors	Split Phase FCR
Key Component	Custom MEMS	On-chip MIM Capacitors	Off-chip capacitors
Total Flipping Capacitance	$4nF$	$600pF$	$272nF$
Piezo Capacitance	$1.94nF$	$6nF$	$22nF$
Chip Area	$5.3mm^2$	$1mm^2$	$0.2mm^2$
Voltage Flipping Efficiency	0.71	0.75	0.84
MOPIR	$8.21x$	$7.01x$	$6.2x$
Output Power	$166\mu W$	$1.5-5.3\mu W$	$0.5-64\mu W$
Operating Frequency	$219Hz$	$22Hz$	$200Hz$

DC voltage conversions for DC harvesting sources (TEGs and solar cells). Lastly, it should be noted that the results are obtained from simulations, whereas the prior art uses experimental measurement data. The measurement data for this design are not available at the time of writing and may be different from the simulation results.

7.4. PROCESS AND TEMPERATURE EFFECTS

The aforementioned results from simulations were obtained from nominal conditions: an IC operating at $27°C$ with average process parameters. However, non-average process parameters and other operating temperature will occur in real world conditions. Firstly, the specified operating temperature range for the design is $-40°C$ to $85°C$. Secondly, process variations unavoidably occurs in the fabrication of semiconductors, increasing or decreasing the performance of both N-type and P-type material and the respective devices.

In designing the subcircuits, care was taken to meet its specifications for the different operating temperatures and process variations. As such, there are no significant performance changes compared to the nominal conditions. Furthermore, due to the inherit robustness of the SCPC design (it only requires switches to turn on and turn off properly for operation), only two effect noticeably influence the performance of the system:

- At high operating temperatures, leakage currents increase in the CMOS devices. However, this is only really noticed for low input powers, degrading the performance by up to 30%.

- For different operating temperatures and process variation, the on-resistance of the transistors in the switches change. This effect is only noticed for high frequency operations in DC source mode where the FSL resistance, and thus the on-resistance of the switches, is dominant (e.g. $P_{mpp} = 50mW$ and $V_{mpp} = 170mV$).

7.5. CONCLUSION

This chapter has shown and discussed the simulation results of the implementation of the designed system. It was shown that the efficiency of the system is very high over a large portion of the operating range for DC sources, but also that the edges of the operating range show the limits of the power converter. For low input power levels, the power losses in the supporting circuits cause a drop in the efficiency. For low input voltages, the maximum voltage conversion ratio limits the ability to match the MPP input voltage, limiting output power. The analytical model that was developed throughout Chapter 4 was found to be rather accurate in predicting the performance of the SCPC. For piezo sources, a theoretical MOPIR of 32 could be achieved. However, due to losses and power consumption in the system, a MOPIR of 20.0 was found. Nevertheless, a comparison to the state-of-art shows that the system outperforms existing designs, while also offering the ability to do DC-to-DC voltage conversions to efficiency harvest from DC sources. The effects of process variation and different operating temperatures and voltages has also been studied.

Lastly, it should be noted that measurement results could not be obtained at the time of writing. Simulation results may differ from the performance of the physical IC, even though layout parasitics were taken into account. There are several possible causes of simulation inaccuracy including but not limited to simplified harvester modelling and finite settling time of the system.

8

Discussion

This chapter examines the design and its results. Firstly, some remarks are given regarding design decisions as well as the presented simulation results to emphasize potential weaknesses. Secondly, the expected system behaviour beyond the specifications is shown, to highlight the limits of the design.

8.1. Design and Results

Firstly, the designed SCPC has a high resolution in terms of possible configurations: two power modes, 119 different conversion ratios and a very wide range of switching frequencies. Although this gives it the ability to match a large range of MPP input voltages, it also present a challenge when implementing an MPPT algorithm to work with this SCPC, as it has to consider a large number of options. As such, the number of conversion ratios may need to be reduced to implement an MPPT algorithm sensibly. This can be done with only little effect on the harvesting efficiency by removing closely related conversion ratios (for example 13/16 = 0.813 and 9/11 = 0.818).

Secondly, this thesis work does not include measurement data of the designed system. The most advanced simulation data that is available is that of the layout, from which parasitics were extracted. However, these simulations also have limitations. Firstly, only the parasitics above a certain minimal value are extracted from the layout, to limit the amount of nodes and components to be simulated. Secondly, only a limited number of these simulations have been executed, aiming to get an idea for the differences between the simulations with and without the extracted parasitics from the layout. Simulations of the full system with parasitics extracted from the layout was not possible over the full operating range due to limited time and resources. However, no great differences were found in these simulations, which suggests that this is true across the entire operating range.

Lastly, although the simulations represent the actual behaviour of the system in its taped-out realization, this is not necessarily the case for the equivalent models of the harvesters. Especially the equivalent model of the piezo element harvester that was used, is a simplification of actual piezo elements. Most prominently, excitations in the real world may not be sinusoidal, which changes the waveform of the piezo current compared to the model used. This may impact the amount of energy harvested by the harvesting interface significantly. Measurement data should be obtained to get more accurate values for the performance of this system with actual piezo elements under natural excitation.

8.2. Operating Behaviour Beyond Specifications

This section looks into the behaviour of the system beyond the specified operating conditions. It should be noted that the limitations that are found are partially present because of the specified operating conditions, which lead to certain design choices in terms of the voltage conversion ratio range and power consumption budget of certain supporting circuits.

DC SOURCE LIMITATIONS

For the DC source operations, the input voltage of the power converter is limited to just below $5V$ to protect the devices. Harvesting elements with MPP output voltages larger than $5V$ are supported, but this MPP voltage cannot be matched and a decreased harvesting efficiency should be expected. Energy harvesting for MPP input voltages below the specified range is possible, but only at a very low efficiency as the maximum voltage conversion ratio of 16 limits the minimum input voltage of the system.

In terms of MPP input power, powers much lower than $10\mu W$ will not generate output power due to the static power consumption of the system. Higher output power levels are limited by the maximum current density of the metal interconnects in the IC.

PIEZO ELEMENT SOURCE LIMITATIONS

Limitations exist for the parameters of the piezo harvester and its excitation. For piezo capacitances higher than $100nF$, the voltage flipping efficiency will decrease significantly and the capacitor imbalance after the voltage flip will cause additional power losses. This can be avoided by increasing the size of the floating capacitors, but then they can no longer be implemented as in-package capacitors. There is no lower limit for the piezo capacitance, but the benefit of using this piezo harvesting interface compared to a full bridge rectifier will be lost quickly for piezo capacitances lower than $1nF$.

The minimum acceptable input power is again limited by the power consumption of the system, although a high MOPIR can decrease the minimum FBR MPP input power to below $1uW$. The maximum input power is limited by the over-voltage protection. More specifically, for higher input currents, the voltage drop due to the conduction resistance of the SCPC is higher, and the over-voltage protection will be triggered causing a significant power loss.

The excitation frequency of the piezo element is limited by the design. Due to the build-in time-out of the finite state machine in the controller, the harvesting cycle cannot be completed for excitation frequencies below $0.5Hz$. Frequencies above $200Hz$ will encounter difficulties due to the decreased conduction angle as the voltage flipping operation will always take $310us$. However, as both of these frequency limitations are directly related to the timings from the externally supplied $100kHz$ clock, this frequency can be adjusted to allow lower or higher excitation frequencies.

BATTERY LIMITATIONS

Lastly, the battery voltage limitations are discussed. Battery voltages larger than $4.5V$ are not supported by the system, as the step-down configuration of the SCPC during piezo harvesting mode will create voltages too close to the over-voltage protection trigger voltage. For battery voltages lower than $3.0V$, poorer performance is expected because of the lower gate drive voltage in the SCPC.

9

CONCLUSION

The goal of this thesis work was to design a low-power high efficiency single-channel PMIC that can harvest both DC power from solar and TEG sources and AC power from piezo elements at the maximum power point (MPP). This concluding chapter gives an overview of presented work done to achieve this goal and summarizes the contributions to the field of energy harvesting. It also provides some recommendations towards future research.

9.1. THESIS OVERVIEW

Firstly, a literature study was conducted to determine the requirements for the design of a single-channel heterogeneous-source energy harvesting PMIC for powering IoT nodes. Chemical and nuclear energy were discarded as energy sources as these are generally not available near IoT nodes. RF energy harvesting was also discarded because of its low power levels. Solar, thermal and mechanical energy harvesting were the remaining types of energy and the photovoltaic effect, Seebeck effect and piezoelectric effect were deemed most suitable energy conversion phenomena. The respective energy harvesting devices were discussed and modelled. Moreover, the energy harvesting interfaces for piezo element harvesting and power conversion techniques for DC source harvesting from literature were discussed.

The design was discussed in a top-down approach, starting with a description of the system requirements. A DC-to-DC voltage conversion was required for harvesting from a DC source (TEG or solar cell). The switched capacitor power converter (sometimes referred to as a charge pump) with in-package capacitors was found to give a good trade-off between the physical system size and efficient energy conversion for the given input voltages and powers. Rectification and voltage flipping was required for the energy conversion from the piezo element source type, for which the active MOS rectifier and SPFCR were the preferred existing techniques. Next, the system overview was given, with each subsystem and a brief description of their working. Additionally, the modelling of the design was discussed.

A novel SCPC was designed with a maximum voltage conversion ratio of 16 and 119 different voltage conversion ratios in total. A charge flow analysis was used to model the behaviour of the designed SCPC and was of great use in optimizing the design. It was expected to perform very well in terms of converting the available energy at the source to energy in the battery storage, because of its high resolution in terms of voltage conversion ratios. Furthermore, the protection circuitry was discussed that protects the system from excessively high voltages.

For conversion of energy from piezo element sources, a novel voltage flipping rectifier design was discussed, that integrates SCPC and FCR operations. The two separate actions for the efficient piezo element harvesting interface (harvesting the piezo current and performing the voltage flip) were matched such that these actions complement each other. It was found that if the SCPC would be harvesting with a voltage conversion ratio of $M = n/16$, the external capacitors would be at certain voltage levels, such that 15 equally spaced fractions of the input voltage could be created by connecting these capacitors in series. This greatly increased the voltage flipping efficiency and therefore the theoretical MOPIR to 32. Additionally, circuits for reaching the MPP, over-voltage protection and control were designed.

The system was completed by the integration of both harvesting modes with the novel source differentiation circuit and the corresponding expansion of the finite state machine that controls the system. Moreover, a debug module was added to increase testability of the IC.

The simulation results showed a harvesting efficiency of up to 96.2% for DC source harvesting. Furthermore, it was found that the equivalent circuit can accurately predict the behaviour of the SCPC with linear DC sources (such as TEGs). For this reason, performance of the system with non-linear DC sources (such as solar cells) was not needed to be simulated and only given by the developed system model. Next, the expected and simulated results for piezo harvesting were discussed and a MOPIR of 20.0 was found, a significant improvement over the state-of-art. Finally, the effects of process variation and different operating temperatures were discussed.

Lastly, the design and its results were discussed. A remark was made on the high number of conversion ratios for the SCPC and its impact on designing an MPPT algorithm. Furthermore, comments were made on the accuracy and reliability of the simulation data. The expected operating behaviour beyond the design specifications were also discussed.

Concludingly, the goal of this thesis has been met. Both the areas of DC source harvesting and piezo element source harvesting have been explored and a single-channel PMIC has been designed and implemented. The simulation results show highly efficient energy harvesting across the full operating range.

9.2. CONTRIBUTIONS

This list summarizes the key contributions made to the field of energy harvesting:

- An energy harvesting platform, with only one input channel, able to harvest from different types of harvesters (non-simultaneously).
- A source differentiation circuit that is able to determine whether a DC source or piezo element source is connected.
- A novel SCPC design with a wide range and high resolution of voltage conversion ratios.
- A voltage flipping rectifier design that uses capacitors from specific SCPC configurations to achieve a MOPIR of 20.0.
- An exemplar CMOS implementation of the aforementioned system and subsystems.

9.3. FUTURE WORK

This section shows recommendations towards future research. Next to the measurement and characterization of the designed IC, design improvement and expansion is possible as well as improved system integration. The following tasks could be performed to enhance the design:

- An MPPT algorithm for DC source operation is vital part of completing the energy harvesting platform.
- The single-channel heterogeneous-source principle can be expanded by adding compatibility for RF energy harvesting.
- In its current form, the system will not be able to operate when the energy storage device is fully depleted. This issue can be solved by adding a cold-start circuit to the system.
- Although the SCPC can be configured to have a 1-to-1 voltage conversion, this can be done much more efficiently by bypassing the SCPC as a whole, either by using some existing switches or adding a separate bypass switch.
- Regulation circuitry should be added to ensure that the battery is not charged above its rated voltage.
- One of the limiting factors in reaching a high MOPIR is the technology voltage limit of $5V$. Implementing the design in a high-voltage technology might increase the MOPIR over a larger range of input conditions. However, it should be kept in mind that the characteristics of these CMOS devices differ, such that they may impact other parameters that influence the output power.

- A comparative analysis of the proposed SCPC, other reconfigurable SCPCs and inductor based converters can be conducted to show how they compare and which type is preferred under which conditions.
- The hypothesis that an SCPC operating with a conversion ratio of $M = \frac{P}{Q}$, $Q-1$ equally spaced intermediate voltage levels between V_i and $0V$ can be made with the floating capacitors (see Section 5.2) should be investigated, such that it can be accepted or refuted.

A

APPENDIX

A.1. SWITCH SIZE OPTIMIZATION

$$\min_{\Sigma_{i=1}^{22} x_i = 1} \left(\sum_{i=1}^{22} \frac{v_i}{x_i} \right) \tag{A.1}$$

With $\vec{v} = [667.1, 27.20, 236.5, 48.04, 648.5, 173.6, 65.10, 77.81, 12.35, 83.43, 43.40, 21.70, 19.01, 4.653, 19.73, 10.85, 10.85, 4.507, 0.9296, 5.413, 0.9997, 9.849]$.

The task at hand is to execute the minimization given in (A.1). This minimization can be solved with the help op the Lagrange multiplier:

$$\begin{aligned} \mathscr{L}(\lambda, \vec{x}) &= f(\vec{x}) - \lambda(g(\vec{x}) - 1) \\ f(\vec{x}) &= \sum_{i=1}^{22} \frac{v_i}{x_i} \\ g(\vec{x}) &= \sum_{i=1}^{22} x_i \end{aligned} \tag{A.2}$$

At the global minimum, the derivative of $\mathscr{L}$ to each x_i will be zero:

$$\frac{\delta \mathscr{L}}{\delta x_i} = -\frac{v_i}{x_i^2} - \lambda = 0 \tag{A.3}$$

This can be rewritten to find x_i:

$$x_i = \pm \sqrt{\frac{-v_i}{\lambda}} \tag{A.4}$$

Only the positive values for x_i are taken. Considering the condition that $g(\vec{x}) = 1$, λ can be found:

$$g(\vec{x}) = \sum_{i=1}^{22} (x_i) = \sum_{i=1}^{22} \left(\sqrt{\frac{-v_i}{\lambda}} \right) = 1 \tag{A.5}$$

This can be rewritten to find λ:

$$\sum_{i=1}^{22} \left(\sqrt{-v_i}\right) = \sqrt{\lambda} \tag{A.6}$$

$$\lambda = \left(\sum_{i=1}^{22} \left(\sqrt{-v_i}\right)\right)^2 \tag{A.7}$$

Lastly, the values for x_i are found, using (A.4):

$$x_i = \pm\sqrt{\frac{-v_i}{\left(\sum_{i=1}^{22} \left(\sqrt{-v_i}\right)\right)^2}} \tag{A.8}$$

$\vec{x} = [0.1616, 0.0326, 0.0962, 0.0434, 0.1593, 0.0824, 0.0505, 0.0552, 0.0220, 0.0571, 0.0412, 0.0291, 0.0273, 0.0135, 0.0278, 0.0206, 0.0206, 0.0133, 0.0060, 0.0146, 0.0063, 0.0196]$

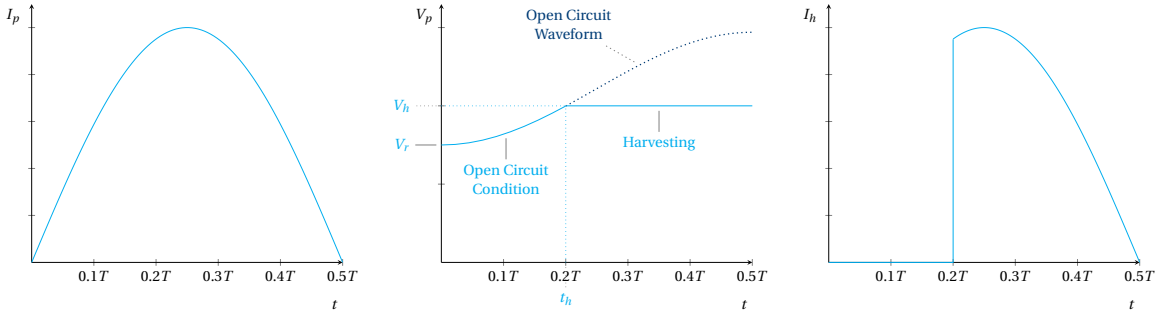
A.2. PIEZO MPPT ALGORITHM

This section explores the design of a dynamic maximum power point tracking (MPPT) for piezo harvesting interfaces.

Equation (2.20) shows a general equation for the power that is harvested from a piezo element connected to a harvesting interface with voltage flipping ability. Due to P_h's dependency on V_h (in the form of $P_h(V_h) = a \cdot V_h^2 - b \cdot V_h$) V_h can be chosen such that a maximum output power is guaranteed. The variables a and b are dependent on the voltage flipping efficiency, the harvester properties and the stress exerted on the harvester. Thus, the optimal V_h (MPP voltage) is also dependent on these parameters. A robust method of finding the MPP voltage is developed, such that any change in parameters will be corrected accordingly.

A.2.1. POSITIVE HALF CYCLE MPP

For the determination of the MPPT a positive half cycle is assumed with a harvesting circuit that has a voltage flipping ability (see Section 2.5.3). The input current has a period of $T = 1/f_{ex}$ where f_{ex} is the excitation frequency. Equations (A.9) and (A.10) are assumed to describe the current and voltage waveforms for such a harvesting circuit. This open circuit condition is present for $V_r < V_p$ (between t_r and t_h) as shown in Figure A.1.



(a) Piezo current waveform I_p (b) Piezo voltage waveform V_p (c) Harvesting current waveform I_h

Figure A.1: Piezo harvesting waveforms

$$I_p(t) = I_{max} \cdot sin(2\pi f_{ex}) \tag{A.9}$$

$$V_p(t) = V_r + \int_0^{t_h} \frac{I_p(t)}{C_p} dt \qquad for \quad 0 < t < t_h \tag{A.10}$$

Combining these V_p can be rewritten as such:

$$V_p(t) = V_h \cdot \eta_{flip} + \frac{I_{max}}{C_p \cdot 2\pi f_{ex}} \cdot (1 - cos(2\pi f_{ex} \cdot t)) \qquad for \quad 0 < t < t_h \tag{A.11}$$

Using $V_p(t_h) = V_h$, V_h is evaluated:

$$V_h = V_h \cdot \eta_{flip} + \frac{I_{max}}{C_p \cdot 2\pi f_{ex}} \cdot (1 - cos(2\pi f_{ex} \cdot t_h)) \tag{A.12}$$

$$V_h(1 - \eta_{flip}) = \frac{I_{max}}{C_p \cdot 2\pi f_{ex}} \cdot (1 - cos(2\pi f_{ex} \cdot t_h)) \tag{A.13}$$

$$V_h = \frac{I_{max}}{C_p \cdot 2\pi f_{ex} \cdot (1 - \eta_{flip})} \cdot (1 - cos(2\pi f_{ex} \cdot t_h)) \tag{A.14}$$

Next, the total amount of *charge* harvested in one half cycle can be found as follows:

$$Q_h = \int_{t_h}^{T/2} I_p(t) dt = \frac{I_{max}}{2\pi f_{ex}} \cdot (cos(2\pi f_{ex} \cdot t_h) + 1) \tag{A.15}$$

Therefore, the total amount of *energy* harvested in one half cycle is as follows:

$$E_h = V_h \cdot Q_h = \frac{1}{(1-\eta_{flip}) \cdot C_p} \left(\frac{I_{max}}{2\pi f_{ex}} \right)^2 \cdot (1 - cos(2\pi f_{ex} \cdot t_h)) \cdot (cos(2\pi f_{ex} \cdot t_h) + 1) \tag{A.16}$$

$$E_h = V_h \cdot Q_h = \frac{1}{(1-\eta_{flip}) \cdot C_p} \left(\frac{I_{max}}{2\pi f_{ex}} \right)^2 \cdot (1 - cos^2(2\pi f_{ex} \cdot t_h)) \tag{A.17}$$

$$E_h = V_h \cdot Q_h = \frac{1}{2 \cdot (1-\eta_{flip}) \cdot C_p} \left(\frac{I_{max}}{2\pi f_{ex}} \right)^2 \cdot (1 - cos(4\pi f_{ex} \cdot t_h)) \tag{A.18}$$

Then, for $0 < t_h < \frac{T}{2}$, the maximum amount of energy is harvested can be found by derivating E_h to t_h:

$$\frac{\delta E_h(t_h)}{\delta t_h} = (-4\pi f_{ex}) \cdot \frac{1}{2 \cdot (1-\eta_{flip}) \cdot C_p} \left(\frac{I_{max}}{2\pi f_{ex}} \right)^2 \cdot sin(4\pi f_{ex} \cdot t_h) = 0 \tag{A.19}$$

Resulting in:

$$t_h = \frac{1}{4 f_{ex}} = \frac{T}{4} \tag{A.20}$$

If the condition above is satisfied, the maximum amount of energy harvested in one positive half cycle is:

$$E_{h,mpp} = \frac{1}{(1-\eta_{flip}) \cdot C_p} \left(\frac{I_{max}}{2\pi f_{ex}} \right)^2 \tag{A.21}$$

As the negative half cycle will shows the same behaviour, expect with voltages and current in opposite polarity, the maximum power point (MPP) power is given by (A.22). The MPP harvesting voltage is given by (A.23).

$$P_{h,mpp} = E_h \cdot 2 f_{ex} = \frac{I_{max}^2}{(1-\eta_{flip}) \cdot C_p \cdot 2\pi^2 \cdot f_{ex}} \tag{A.22}$$

$$V_{h,mpp} = V_p(t_h) = \frac{I_{max}}{C_p \cdot 2\pi f_{ex} \cdot (1-\eta_{flip})} \tag{A.23}$$

A.2.2. STATE DEFINITION AND TRANSITIONS

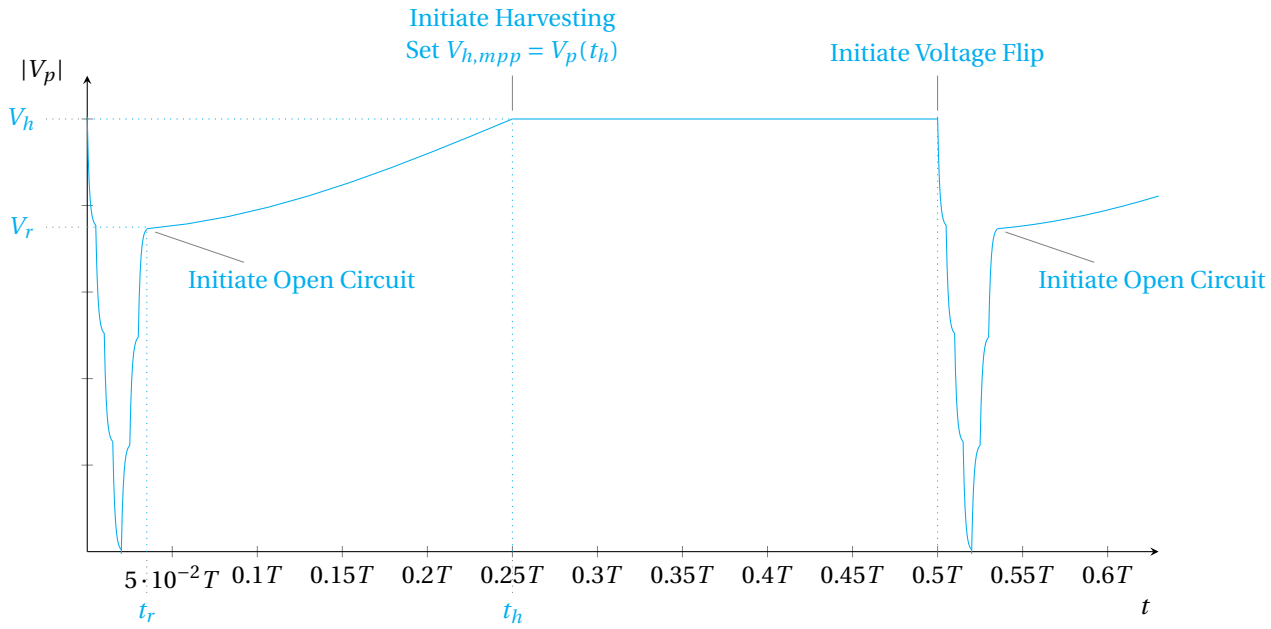
In one piezo harvesting cycle, three different states can be defined (see Figure A.2):

- Voltage Flip: The voltage on the piezo element is flipped (reversed in polarity) to V_r $(= -\eta_{flip} \cdot V_h)$
- Open Circuit: The piezo current I_p charges the piezo capacitance from V_r to V_h
- Harvesting: The piezo current I_p is harvested at the harvesting voltage V_h $(t = T/2)$

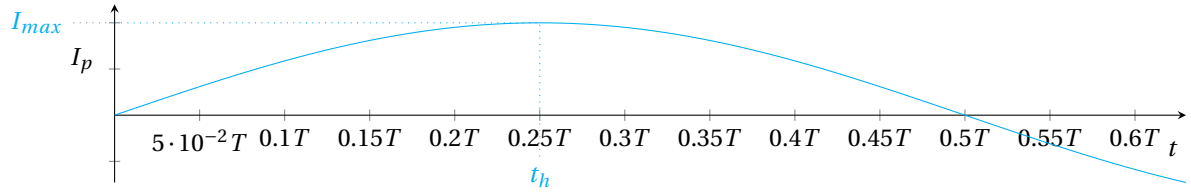
The each state is initiated by a specific trigger. At t_r the voltage flipping operation is finished and the 'Open Circuit' state is initiated. At t_h the MPP voltage is reached and harvesting at this voltage should be started. The voltage flipping operation should be initiated around the transition from one half cycle to the next (indicated by the zero current crossing of I_p).

Considering that $V_p(t_h) = V_{h,mpp}$, the maximum power point voltage can be evaluated for each cycle to achieve a true tracking of the maximum power point when t_h is known. When the input frequency is know, t_h has a fixed value. However, this may not be the case. Therefore, a method must be found to dynamically determine the value of t_h.

As shown by (A.9) and Figure A.2, at t_h the peak piezo current is found $(I_p(t_h) = I_{max})$. Because of the open circuit configuration for $t_r < t < t_h$, the derivative of the piezo voltage V_p is proportional to the piezo current I_p. Thus, t_h is also indicated by a peak in $\delta V_p(t)/\delta t$.



(a) Absolute Piezo Voltage



(b) Piezo current waveform I_p

Figure A.2: The Piezo MPPT Scheme (with an exaggerated 7-phase FCR operation)

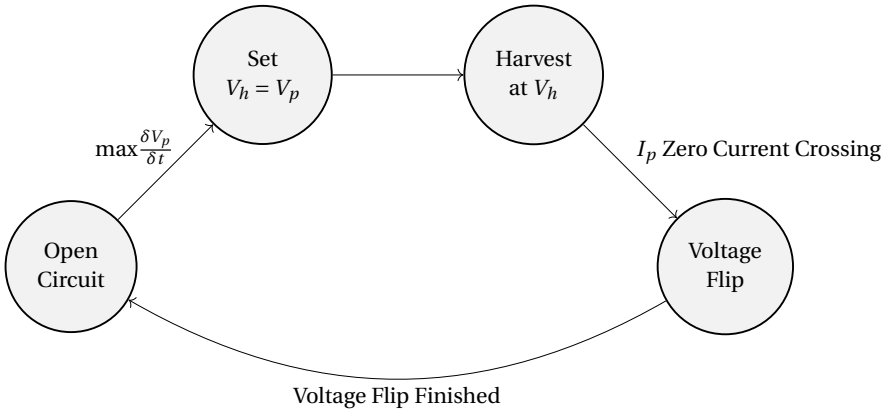


Figure A.3: MPPT FSM Implementation

COMMENTS

The developed piezo MPPT algorithm can be used for multiple types of voltage flipping rectifiers. However, some non-ideal could impact the accuracy of the MPPT severely. Examples of these non-idealities are losses in the system or non-sinusoidal input currents.

A.3. FIGURES

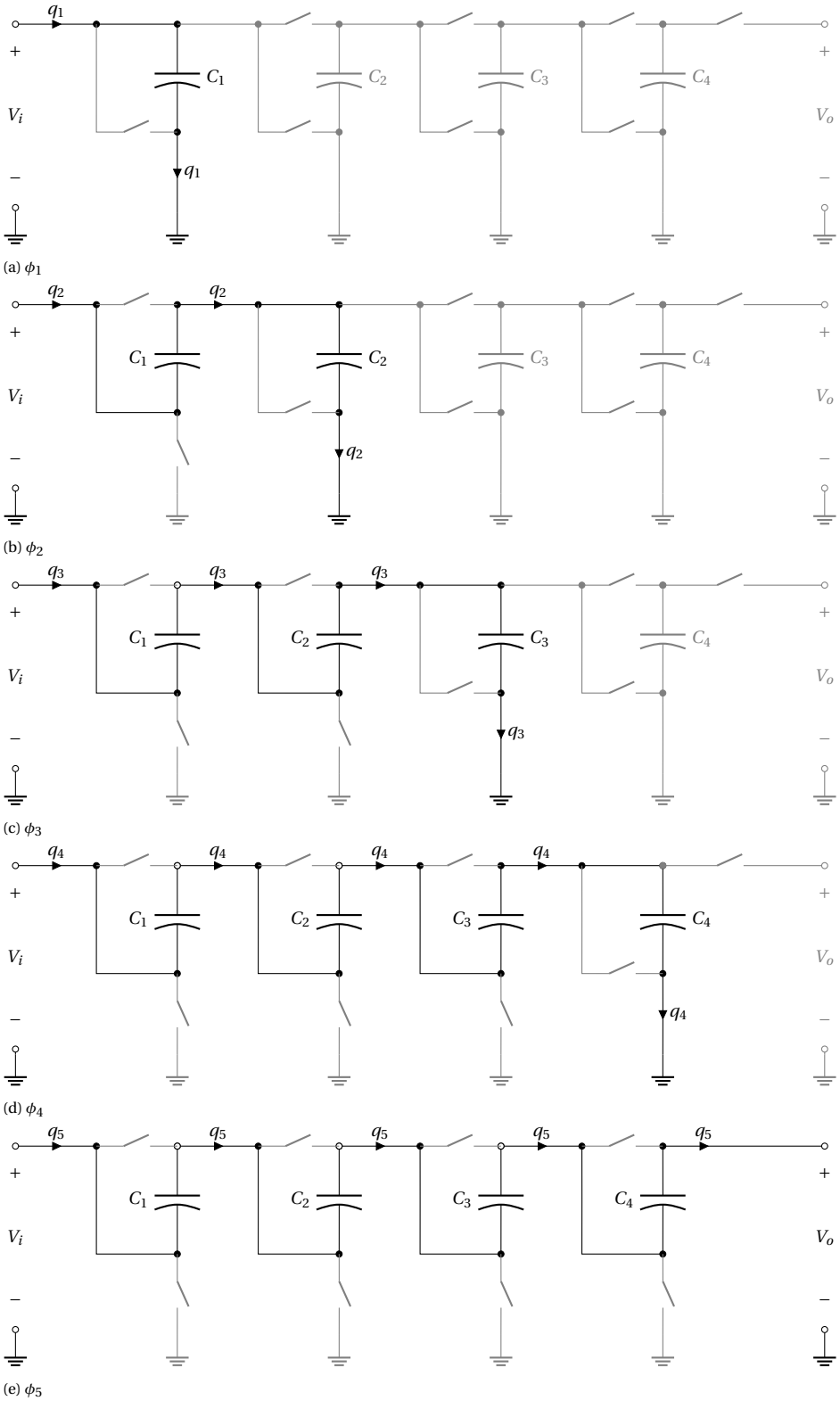


Figure A.4: Charge flows for the SCPC circuit for $M = 16$

A.4. LIST OF SWITCH CONFIGURATIONS FOR VOLTAGE FLIP

Table A.1: Switch configurations for voltage flips for for $M = \frac{11}{16}$: $V_{C1} = \frac{-5}{16} \cdot V_h$, $V_{C2} = \frac{6}{16} \cdot V_h$, $V_{C3} = \frac{-4}{16} \cdot V_h$ and $V_{C4} = \frac{8}{16} \cdot V_h$

Step	$V_{rect} = \lvert V_p \rvert$	Active Switches
1 + 31	$\frac{15}{16} \cdot V_h = -V_{C1} + V_{C2} - V_{C3}$	3, 8, 14, 23, 26
2 + 30	$\frac{14}{16} \cdot V_h = V_{C2} + V_{C4}$	3, 6, 13, 22, 26
3 + 29	$\frac{13}{16} \cdot V_h = -V_{C1} + V_{C4}$	3, 8, 15, 22, 26
4 + 28	$\frac{12}{16} \cdot V_h = -V_{C3} + V_{C4}$	3, 6, 16, 22, 26
5 + 27	$\frac{11}{16} \cdot V_h = -V_{C1} + V_{C2}$	3, 8, 13, 23, 26
6 + 26	$\frac{10}{16} \cdot V_h = V_{C2} - V_{C3}$	3, 6, 14, 23, 26
7 + 25	$\frac{9}{16} \cdot V_h = -V_{C1} - V_{C3}$	3, 9, 14, 23, 26
8 + 24	$\frac{8}{16} \cdot V_h = V_{C4}$	1, 8, 15, 22, 26
9 + 23	$\frac{7}{16} \cdot V_h = -V_{C1} - V_{C2} + V_{C4}$	3, 9, 15, 22, 26
10 + 22	$\frac{6}{16} \cdot V_h = V_{C2}$	1, 8, 13, 23, 26
11 + 21	$\frac{5}{16} \cdot V_h = -V_{C1}$	3, 9, 13, 23, 26
12 + 20	$\frac{4}{16} \cdot V_h = -V_{C3}$	1, 9, 14, 23, 26
13 + 19	$\frac{3}{16} \cdot V_h = V_{C1} + V_{C4}$	1, 6, 15, 22, 26
14 + 18	$\frac{2}{16} \cdot V_h = -V_{C2} + V_{C4}$	1, 9, 15, 22, 26
15 + 17	$\frac{1}{16} \cdot V_h = -V_{C1} + V_{C3}$	1, 6, 13, 23, 26
16	$0V$	24, 26

Table A.2: Switch configurations for voltage flips for for $M = \frac{13}{16}$: $V_{C1} = \frac{-3}{16} \cdot V_h$, $V_{C2} = \frac{-6}{16} \cdot V_h$, $V_{C3} = \frac{4}{16} \cdot V_h$ and $V_{C4} = \frac{8}{16} \cdot V_h$

Step	$V_{rect} = \lvert V_p \rvert$	Active Switches
1 + 31	$\frac{15}{16} \cdot V_h = -V_{C1} + V_{C3} + V_{C4}$	3, 9, 13, 20, 26
2 + 30	$\frac{14}{16} \cdot V_h = -V_{C2} + V_{C4}$	3, 7, 15, 22, 26
3 + 29	$\frac{13}{16} \cdot V_h = -V_{C1} - V_{C2} + V_{C3}$	3, 9, 15, 21, 26
4 + 28	$\frac{12}{16} \cdot V_h = V_{C3} + V_{C4}$	1, 9, 13, 20, 26
5 + 27	$\frac{11}{16} \cdot V_h = -V_{C1} + V_{C4}$	3, 8, 15, 22, 26
6 + 26	$\frac{10}{16} \cdot V_h = -V_{C2} + V_{C3}$	1, 9, 15, 21, 26
7 + 25	$\frac{9}{16} \cdot V_h = -V_{C1} - V_{C2}$	3, 9, 16, 21, 26
8 + 24	$\frac{8}{16} \cdot V_h = V_{C4}$	1, 8, 15, 22, 26
9 + 23	$\frac{7}{16} \cdot V_h = -V_{C1} + V_{C3}$	3, 8, 15, 21, 26
10 + 22	$\frac{6}{16} \cdot V_h = -V_{C2}$	1, 9, 16, 21, 26
11 + 21	$\frac{5}{16} \cdot V_h = V_{C1} + V_{C4}$	1, 6, 15, 22, 26
12 + 20	$\frac{4}{16} \cdot V_h = V_{C3}$	1, 8, 15, 21, 26

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Table A.2 – *Continued from previous page*

Step	$V_{rect} = \lvert V_p \rvert$	Active Switches
13 + 19	$\frac{3}{16} \cdot V_h = -V_{C1}$	3, 8, 16, 21, 26
14 + 18	$\frac{2}{16} \cdot V_h = -V_{C2} - V_{C3}$	1, 8, 14, 20, 26
15 + 17	$\frac{1}{16} \cdot V_h = V_{C1} + V_{C3}$	1, 6, 15, 21, 26
16	$0V$	24, 26

Table A.3: Switch configurations for voltage flips for for $M = \frac{15}{16}$: $V_{C1} = \frac{-1}{16} \cdot V_h$, $V_{C2} = \frac{-2}{16} \cdot V_h$, $V_{C3} = \frac{-4}{16} \cdot V_h$ and $V_{C4} = \frac{8}{16} \cdot V_h$

Step	$V_{rect} = \lvert V_p \rvert$	Active Switches
1 + 31	$\frac{15}{16} \cdot V_h = -V_{C1} - V_{C2} - V_{C3} + V_{C4}$	3, 9, 16, 22, 26
2 + 30	$\frac{14}{16} \cdot V_h = -V_{C2} - V_{C3} + V_{C4}$	1, 9, 16, 22, 26
3 + 29	$\frac{13}{16} \cdot V_h = -V_{C1} - V_{C3} + V_{C4}$	3, 8, 16, 22, 26
4 + 28	$\frac{12}{16} \cdot V_h = -V_{C3} + V_{C4}$	1, 8, 16, 22, 26
5 + 27	$\frac{11}{16} \cdot V_h = -V_{C1} - V_{C2} + V_{C4}$	3, 9, 15, 22, 26
6 + 26	$\frac{10}{16} \cdot V_h = -V_{C2} + V_{C4}$	1, 9, 15, 22, 26
7 + 25	$\frac{9}{16} \cdot V_h = -V_{C1} + V_{C4}$	3, 8, 15, 22, 26
8 + 24	$\frac{8}{16} \cdot V_h = V_{C4}$	1, 8, 15, 22, 26
9 + 23	$\frac{7}{16} \cdot V_h = V_{C1} + V_{C4}$	3, 9, 16, 23, 26
10 + 22	$\frac{6}{16} \cdot V_h = -V_{C2} - V_{C3}$	1, 9, 16, 23, 26
11 + 21	$\frac{5}{16} \cdot V_h = -V_{C1} - V_{C3}$	3, 8, 16, 23, 26
12 + 20	$\frac{4}{16} \cdot V_h = -V_{C3}$	1, 8, 16, 23, 26
13 + 19	$\frac{3}{16} \cdot V_h = -V_{C1} - V_{C2}$	3, 9, 15, 23, 26
14 + 18	$\frac{2}{16} \cdot V_h = -V_{C2}$	1, 9, 15, 23, 26
15 + 17	$\frac{1}{16} \cdot V_h = -V_{C1}$	3, 8, 15, 23, 26
16	$0V$	24, 26

A.5. LIST OF CONVERSION RATIO SETTINGS

Table A.4: List of conversion ratio settings

M (decimal)	M (fraction)	a_1	a_2	a_3	a_4	a_5	a_6	b_1	b_2	b_3	b_4	b_5	b_6
0.0625	$\frac{1}{16}$	0	0	0	0	0	1	1	0	0	0	0	0
0.0667	$\frac{1}{15}$	0	0	0	0	0	1	1	0	0	0	1	0
0.0714	$\frac{1}{14}$	0	0	0	0	0	1	1	0	0	1	0	0
0.0769	$\frac{1}{13}$	0	0	0	0	0	1	1	0	0	1	1	0
0.0833	$\frac{1}{12}$	0	0	0	0	0	1	1	0	1	0	0	0
0.0909	$\frac{1}{11}$	0	0	0	0	0	1	1	0	1	0	1	0
0.1	$\frac{1}{10}$	0	0	0	0	0	1	1	0	1	1	0	0
0.111	$\frac{1}{9}$	0	0	0	0	0	1	1	0	1	1	1	0
0.125	$\frac{1}{8}$	0	0	0	0	1	1	1	0	0	0	0	0
0.133	$\frac{2}{15}$	0	0	0	1	0	0	1	0	0	0	0	1
0.143	$\frac{1}{7}$	0	0	0	0	1	1	1	0	0	1	0	0
0.167	$\frac{1}{6}$	0	0	0	0	1	1	1	0	1	0	0	0
0.182	$\frac{2}{11}$	0	0	0	1	0	0	1	0	1	0	0	1
0.188	$\frac{3}{16}$	0	0	0	1	0	1	1	0	0	0	0	0
0.2	$\frac{1}{5}$	0	0	0	1	0	1	1	0	0	0	1	0
0.25	$\frac{1}{4}$	0	0	0	1	1	1	1	0	0	0	0	0
0.267	$\frac{4}{15}$	0	0	1	0	0	0	1	0	0	0	0	1
0.273	$\frac{3}{11}$	0	0	0	1	0	1	1	0	1	0	1	0
0.286	$\frac{2}{7}$	0	0	1	0	0	0	1	0	0	0	1	1
0.308	$\frac{4}{13}$	0	0	1	0	0	0	1	0	0	1	0	1
0.313	$\frac{5}{16}$	0	0	1	0	0	1	1	0	0	0	0	0
0.333	$\frac{1}{3}$	0	0	1	0	0	1	1	0	0	0	1	0
0.357	$\frac{5}{14}$	0	0	1	0	0	1	1	0	0	1	0	0
0.375	$\frac{3}{8}$	0	0	1	0	1	1	1	0	0	0	0	0
0.385	$\frac{5}{13}$	0	0	1	0	0	1	1	0	0	1	1	0
0.4	$\frac{2}{5}$	0	0	1	1	0	0	1	0	0	0	0	1
0.429	$\frac{3}{7}$	0	0	1	0	1	1	1	0	0	1	0	0
0.438	$\frac{7}{16}$	0	0	1	1	0	1	1	0	0	0	0	0
0.467	$\frac{7}{15}$	0	0	1	1	0	1	1	0	0	0	1	0
0.5	$\frac{1}{2}$	0	0	1	1	1	1	1	0	0	0	0	0
0.533	$\frac{8}{15}$	0	1	0	0	0	0	1	0	0	0	0	1
0.563	$\frac{9}{16}$	0	1	0	0	0	1	1	0	0	0	0	0
0.571	$\frac{4}{7}$	0	1	0	0	0	0	1	0	0	0	1	1
0.6	$\frac{3}{5}$	0	1	0	0	0	1	1	0	0	0	1	0

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Table A.4 – *Continued from previous page*

M (decimal)	M (fraction)	a_1	a_2	a_3	a_4	a_5	a_6	b_1	b_2	b_3	b_4	b_5	b_6
0.615	$\frac{8}{13}$	0	1	0	0	0	0	1	0	0	1	0	1
0.625	$\frac{5}{8}$	0	1	0	0	1	1	1	0	0	0	0	0
0.643	$\frac{9}{14}$	0	1	0	0	0	1	1	0	0	1	0	0
0.667	$\frac{2}{3}$	0	1	0	1	0	0	1	0	0	0	0	1
0.688	$\frac{11}{16}$	0	1	0	1	0	1	1	0	0	0	0	0
0.692	$\frac{9}{13}$	0	1	0	0	0	1	1	0	0	1	1	0
0.714	$\frac{5}{7}$	0	1	0	0	1	1	1	0	0	1	0	0
0.727	$\frac{8}{11}$	0	1	0	0	0	0	1	0	1	0	0	1
0.733	$\frac{11}{15}$	0	1	0	1	0	1	1	0	0	0	1	0
0.75	$\frac{3}{4}$	0	1	0	1	1	1	1	0	0	0	0	0
0.8	$\frac{4}{5}$	0	1	1	0	0	0	1	0	0	0	0	1
0.813	$\frac{13}{16}$	0	1	1	0	0	1	1	0	0	0	0	0
0.818	$\frac{9}{11}$	0	1	0	0	0	1	1	0	1	0	1	0
0.833	$\frac{5}{6}$	0	1	0	0	1	1	1	0	1	0	0	0
0.857	$\frac{6}{7}$	0	1	1	0	0	0	1	0	0	0	1	1
0.867	$\frac{13}{15}$	0	1	1	0	0	1	1	0	0	0	1	0
0.875	$\frac{7}{8}$	0	1	1	0	1	1	1	0	0	0	0	0
0.889	$\frac{8}{9}$	0	1	0	0	0	0	1	0	1	1	0	1
0.9	$\frac{9}{10}$	0	1	0	0	0	1	1	0	1	1	0	0
0.909	$\frac{10}{11}$	0	1	0	1	0	0	1	0	1	0	0	1
0.917	$\frac{11}{12}$	0	1	0	1	0	1	1	0	1	0	0	0
0.923	$\frac{12}{13}$	0	1	1	0	0	0	1	0	0	1	0	1
0.929	$\frac{13}{14}$	0	1	1	0	0	1	1	0	0	1	0	0
0.933	$\frac{14}{15}$	0	1	1	1	0	0	1	0	0	0	0	1
0.938	$\frac{15}{16}$	0	1	1	1	0	1	1	0	0	0	0	0
1	$\frac{1}{1}$	0	1	1	1	1	1	1	0	0	0	0	0
1.07	$\frac{16}{15}$	1	0	0	0	0	0	0	1	1	1	0	1
1.07	$\frac{15}{14}$	1	0	0	0	0	1	0	1	1	1	0	0
1.08	$\frac{14}{13}$	1	0	0	1	0	0	0	1	1	0	0	1
1.08	$\frac{13}{12}$	1	0	0	1	0	1	0	1	1	0	0	0
1.09	$\frac{12}{11}$	1	0	1	0	0	0	0	1	0	1	0	1
1.1	$\frac{11}{10}$	1	0	1	0	0	1	0	1	0	1	0	0
1.11	$\frac{10}{9}$	1	0	1	1	0	0	0	1	0	0	0	1
1.13	$\frac{9}{8}$	1	0	1	1	0	1	0	1	0	0	0	0
1.14	$\frac{8}{7}$	1	1	0	0	0	0	0	0	1	1	0	1
1.15	$\frac{15}{13}$	1	0	0	0	0	1	0	1	1	0	1	0

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Table A.4 – *Continued from previous page*

M (decimal)	M (fraction)	a_1	a_2	a_3	a_4	a_5	a_6	b_1	b_2	b_3	b_4	b_5	b_6
1.17	$\frac{7}{6}$	1	1	0	0	0	1	0	0	1	1	0	0
1.2	$\frac{6}{5}$	1	1	0	1	0	0	0	0	1	0	0	1
1.22	$\frac{11}{9}$	1	0	1	0	0	1	0	1	0	0	1	0
1.23	$\frac{16}{13}$	1	0	0	0	0	0	0	1	1	0	0	1
1.25	$\frac{5}{4}$	1	1	0	1	0	1	0	0	1	0	0	0
1.33	$\frac{4}{3}$	1	1	1	0	0	0	0	0	0	1	0	1
1.36	$\frac{15}{11}$	1	0	0	0	0	1	0	1	0	1	1	0
1.38	$\frac{11}{8}$	1	0	1	0	0	1	0	1	0	0	0	0
1.4	$\frac{7}{5}$	1	1	0	0	0	1	0	0	1	0	1	0
1.44	$\frac{13}{9}$	1	0	0	1	0	1	0	1	0	0	1	0
1.45	$\frac{16}{11}$	1	0	0	0	0	0	0	1	0	1	0	1
1.5	$\frac{3}{2}$	1	1	1	0	0	1	0	0	0	1	0	0
1.56	$\frac{14}{9}$	1	0	0	1	0	0	0	1	0	0	0	1
1.6	$\frac{8}{5}$	1	1	0	0	0	0	0	0	1	0	0	1
1.63	$\frac{13}{8}$	1	0	0	1	0	1	0	1	0	0	0	0
1.67	$\frac{5}{3}$	1	0	0	0	0	1	0	1	0	0	1	0
1.75	$\frac{7}{4}$	1	1	0	0	0	1	0	0	1	0	0	0
1.78	$\frac{16}{9}$	1	0	0	0	0	0	0	1	0	0	0	1
1.88	$\frac{15}{8}$	1	0	0	0	0	1	0	1	0	0	0	0
2	$\frac{2}{1}$	1	1	1	1	0	0	0	0	0	0	0	1
2.14	$\frac{15}{7}$	1	0	0	0	0	1	0	0	1	1	1	0
2.29	$\frac{16}{7}$	1	0	0	0	0	0	0	0	1	1	0	1
2.33	$\frac{7}{3}$	1	1	0	0	0	1	0	0	0	1	1	0
2.5	$\frac{5}{2}$	1	0	0	0	0	1	0	0	1	1	0	0
2.6	$\frac{13}{5}$	1	0	0	1	0	1	0	0	1	0	1	0
2.67	$\frac{8}{3}$	1	1	0	0	0	0	0	0	0	1	0	1
2.8	$\frac{14}{5}$	1	0	0	1	0	0	0	0	1	0	0	1
3	$\frac{3}{1}$	1	1	1	0	0	1	0	0	0	0	1	0
3.2	$\frac{16}{5}$	1	0	0	0	0	0	0	0	1	0	0	1
3.25	$\frac{13}{4}$	1	0	0	1	0	1	0	0	1	0	0	0
3.5	$\frac{7}{2}$	1	1	0	0	0	1	0	0	0	1	0	0
3.67	$\frac{11}{3}$	1	0	1	0	0	1	0	0	0	1	1	0
3.75	$\frac{15}{4}$	1	0	0	0	0	1	0	0	1	0	0	0
4	$\frac{4}{1}$	1	1	1	0	0	0	0	0	0	0	0	1
5	$\frac{5}{1}$	1	1	0	1	0	1	0	0	0	0	1	0
5.33	$\frac{16}{3}$	1	0	0	0	0	0	0	0	0	1	0	1

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Table A.4 – *Continued from previous page*

M (decimal)	M (fraction)	a_1	a_2	a_3	a_4	a_5	a_6	b_1	b_2	b_3	b_4	b_5	b_6
5.5	$\frac{11}{2}$	1	0	1	0	0	1	0	0	0	1	0	0
6	$\frac{6}{1}$	1	1	0	1	0	0	0	0	0	0	0	1
7	$\frac{7}{1}$	1	1	0	0	0	1	0	0	0	0	1	0
7.5	$\frac{15}{2}$	1	0	0	0	0	1	0	0	0	1	0	0
8	$\frac{8}{1}$	1	1	0	0	0	0	0	0	0	0	0	1
9	$\frac{9}{1}$	1	0	1	1	0	1	0	0	0	0	1	0
10	$\frac{10}{1}$	1	0	1	1	0	0	0	0	0	0	0	1
11	$\frac{11}{1}$	1	0	1	0	0	1	0	0	0	0	1	0
12	$\frac{12}{1}$	1	0	1	0	0	0	0	0	0	0	0	1
13	$\frac{13}{1}$	1	0	0	1	0	1	0	0	0	0	1	0
14	$\frac{14}{1}$	1	0	0	1	0	0	0	0	0	0	0	1
15	$\frac{15}{1}$	1	0	0	0	0	1	0	0	0	0	1	0
16	$\frac{16}{1}$	1	0	0	0	0	0	0	0	0	0	0	1

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