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A Frequency-Locked Loop Based on an Oxide Electrothermal Filter in Standard CMOS

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***Abstract*—The thermal diffusivity of silicon D_{Si} has been used to realize fully-CMOS frequency references. However, due to the temperature dependence of D_{Si}, the accuracy of such frequency references is limited to about 1000 ppm (−55 °C to 125 °C, one-point trim) due to the inaccuracy of the on-chip temperature compensation circuitry. As an alternative, we propose a frequency reference based on the thermal diffusivity of silicon dioxide D_{Ox}. Since the temperature dependence of D_{Ox} is much less than that of D_{Si}, the resulting frequency reference will be much more stable over temperature. To investigate this idea, a thermal-diffusivity-based frequency-locked loop (FLL) was realized in 0.18-μm CMOS. With ideal temperature compensation, the proposed frequency reference achieves an inaccuracy of 90 ppm (−45 °C to 85 °C, two-point trim). Even with 0.1 °C inaccuracy, which can be achieved by BJT-based temperature sensors, 200 ppm can still be achieved. This demonstrates the feasibility of high-accuracy oxide-based frequency references in standard CMOS.**

Keywords—frequency reference; oxide; thermal diffusivity; CMOS

I. Introduction

Quartz crystal oscillators are widely used as frequency references for IC's for their high accuracy, but they require separate manufacturing process and packaging, thus increasing system cost and size. Among fully-integrated CMOS alternatives, LC-based frequency references provide good accuracy (100 ppm) at the expense of large power consumption (>10 mW) [1]. On the contrary, RC-based references are characterized by low power (<100 μW) but worse accuracy (>>1000 ppm) [2]. A better tradeoff is offered by frequency references based on the thermal diffusivity (TD) of silicon, which can reach 1000 ppm accuracy, some 10× better than RC references, with a power consumption of only 2 mW.

A TD frequency reference (Fig. 1) consists of an electrothermal frequency-locked loop (FLL) combined with temperature compensation [3]. The FLL locks its frequency to the phase shift of an electrothermal filter (ETF). In a silicon ETF, a diffusion resistor generates heat pulses at frequency f that diffuse through the silicon substrate. At a distance s from the heater, a thermopile senses the heat pulse's phase shift $\phi_{ETF,Si}$, which is a function of s and of the temperature-dependent thermal diffusivity of silicon $D_{Si}(T)$. The frequency

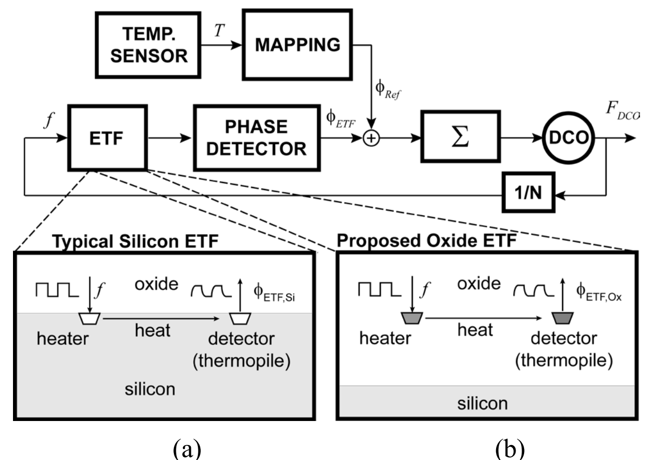

Fig. 1. Block diagram of a thermal-diffusivity-based frequency reference.

accuracy is potentially very high, since the distance s is limited by the nanometer-level lithographic accuracy of modern CMOS processes, and $D_{Si}(T)$ is very well-defined for the high-grade silicon used for IC's [4].

Temperature compensation is achieved by appropriately computing ϕ_{Ref} from the output of an on-chip temperature sensor. The loop then ensures that $\phi_{ETF}(T) = \phi_{Ref}(T)$, so that the output frequency is constant. However, due to the large temperature dependence of silicon thermal diffusivity ($D_{Si} \propto T^{-1.8}$), any temperature sensing error can heavily degrade the frequency reference's accuracy. For instance, the frequency accuracy of a state-of-the-art TD-based references was limited to 1000 ppm (−55°C to 125°C, one-point trim) by the accuracy of its on-chip temperature sensor (0.2 °C) combined with the large temperature coefficient of its silicon ETF's phase shift (~3000 ppm/°C) [3].

To provide greater immunity to temperature sensing errors, an ETF based on the thermal diffusivity $D_{Ox}(T)$ of silicon dioxide (SiO_2) can be employed, since this is less temperature dependent than $D_{Si}(T)$. In an oxide ETF (Fig. 1b), a polysilicon resistor injects heat pulses into the adjacent oxide. The resulting temperature signal is detected by a polysilicon/Al thermopile at a distance g. As the heat now flows through SiO_2, the phase shift now depends on $D_{Ox}(T)$. In a recent 65-nm CMOS implementation [5], the reported temperature

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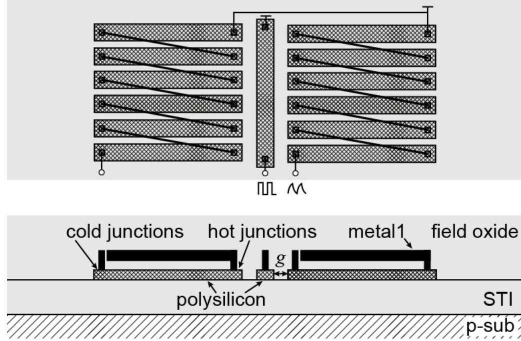

Fig. 2. Top and side view of a CMOS oxide electrothermal filter.

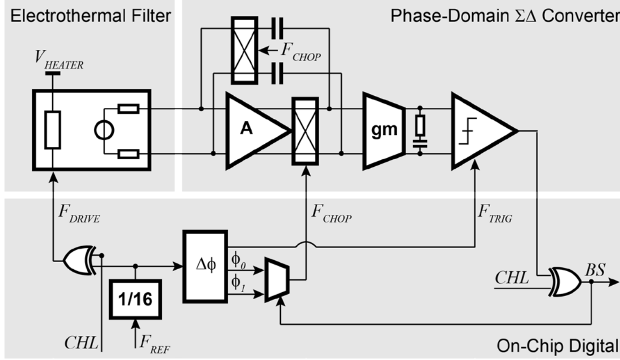

Fig. 3. Block diagram of the on-chip front-end.

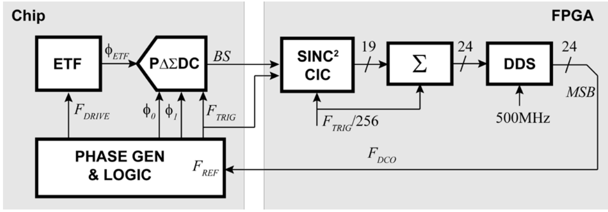

Fig. 4. Block diagram of the frequency-locked loop implemented in this work.

coefficient of the oxide ETF's phase shift $\phi_{ETF,Ox}$ is ~500 ppm/°C, i.e. 6× lower than in a typical silicon ETF. Thus, a TD frequency reference locked to $\phi_{ETF,Ox}$ could provide much better accuracy, mainly limited by the ETF's own spread.

In this paper, we present the first FLL based on an oxide ETF, which exhibits 90-ppm accuracy (−45°C to 85°C, 2-point trim). Thanks to the low temperature coefficient of $D_{Ox}(T)$, it is robust to temperature sensing errors of up to 0.1 °C. This result paves the way to the implementation of CMOS frequency references with better than 100 ppm accuracy.

The paper is organized as follows: Section II and III describe the FLL architecture and the circuit-level design, respectively. Measurement results are shown in Section IV. Conclusions are drawn in Section V.

II. FLL Architecture

Fig. 4 shows the block diagram of the FLL. The oxide ETF is driven by F_{DRIVE} at $f = F_{DCO}/16$, and provides a phase shift

$$\phi_{ETF,Ox} \propto g\sqrt{\pi f / D_{Ox}(T)}, \quad (1)$$

where $D_{Ox}(T)$ is the temperature dependent thermal diffusivity of SiO_2 and g is the oxide gap between the heater and the thermopile. This phase shift is subsequently digitized by an on-chip Phase-Domain ΣΔ Converter (PDΣΔC), whose output bitstream's average is proportional to $\phi_{ETF,Ox}$. A decimation filter removes the out-of-band quantization noise in the bitstream *BS*, and downsamples it by a factor 256. The feedback loop is closed by the loop filter that is implemented by a digital integrator driving the DCO. The loop forces the integrator's input to be zero on average, thus defining the working point to be $\phi_{ETF,Ox} = \phi_{Ref}$, for which:

$$f \propto \left(\phi_{Ref}/g\right)^2 \cdot D_{Ox}(T)/\pi . \quad (2)$$

In the current FLL implementation, ϕ_{Ref} is constant, and not temperature compensated, resulting in a DCO output frequency that follows the temperature dependent thermal diffusivity of the ETF. To convert the FLL into a frequency reference, only temperature compensation must be added by providing a $\phi_{Ref}(T)$ that matches the temperature behavior $D_{Ox}(T)$.

III. Circuit Design

A. Electrothermal Filters

The oxide ETF's top view and cross section are shown in Fig. 2. A 450-Ω p+ silicided polysilicon resistor (heater), sitting on top of a shallow-trench isolation (STI) oxide layer, is pulsed at frequency f, dissipating an average power of 3.6 mW. A series combination of 24 p+ unsilicided polysilicon resistors and aluminum interconnect form an integrated thermopile with Seebeck coefficient $\alpha \sim 24 \times 100\,\mu V/°C$, which converts the temperature difference between its hot and cold junctions into a voltage of a few mV. An oxide gap $g = 450$ nm separates the heater from the thermopile's hot junctions. The cold junctions are located 5.5 μm away, in order to have a large output signal while keeping the thermopile thermal noise at an acceptable value (26 nV/√Hz with a 43-kΩ thermopile resistance). The oxide gap g should ideally dominate the heat path, so that the behavior of the oxide ETF is well described by (1). However, because the STI thickness is in the order of a few hundred of nanometers, and therefore comparable to g, the ETF is not completely isolated from the silicon substrate. As a result, the temperature dependency and accuracy of the resulting ETF will be determined by both the thermal diffusivity of the STI and, to a lesser extent, that of the silicon substrate.

In order to demonstrate that oxide-based FLL's have a lower temperature coefficient than silicon FLL's, a silicon ETF was also implemented, using a 400-Ω n+ diffusion resistor as heater, and, as thermopile, the series combination of 16 p+ unsilicided diffusion resistors in a n-well (to reject the substrate noise). $s = 4.5$ μm has been chosen to replicate the results of the state-of-the-art TD frequency reference in [3], that uses a process node (0.16 μm CMOS) similar to the one adopted in this work (0.18 μm CMOS). For the chosen values of g and s, the two ETF's are expected to exhibit a similar phase shift at room temperature, thus simplifying readout design.

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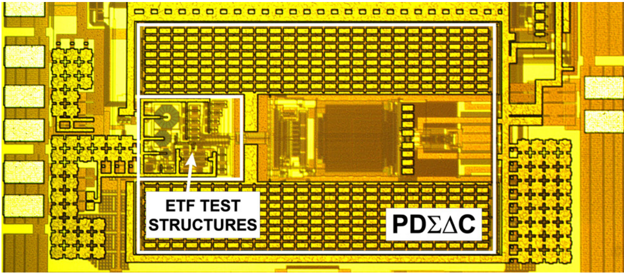
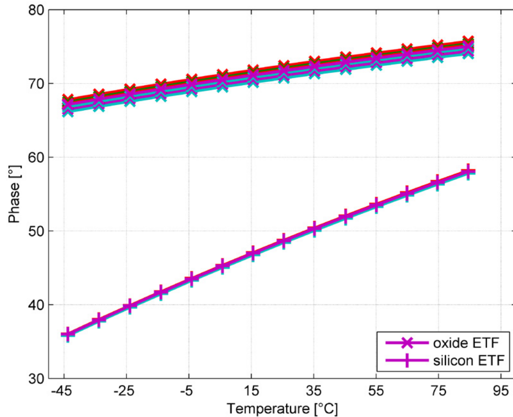
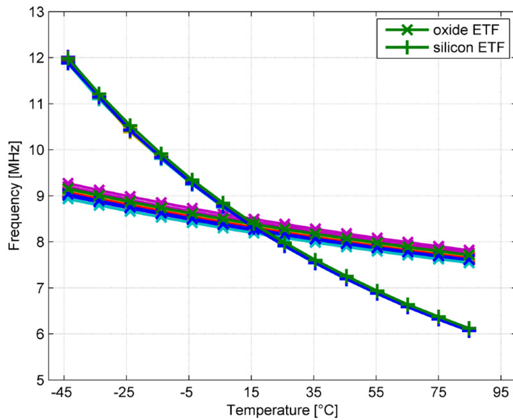


Fig. 6. Chip microphotograph.



(a)



(b)

Fig. 5. (a) Measured oxide and silicon ETF's phase shift over temperature at constant 9 MHz/16 = 562.5 kHz driving frequency; (b) measured oxide and silicon FLL's frequency over temperature.

B. Phase-to-Digital Converter

The ETF's phase is digitized by a Phase-Domain Sigma-Delta Converter (PDΣΔC, Fig. 3) [6]. In order to read the ETF's phase with a 100-ppm resolution, a single-bit 2nd-order topology was chosen. The current through the ETF's thermopile is demodulated by a chopper and integrated on a capacitor. The chopper drive F_{CHOP} is switched between two reference phases ϕ_0 and ϕ_1 (ϕ_0 = 135°, ϕ_1 = 180° for the oxide ETF; ϕ_0 = 90°, ϕ_1 = 180° for the silicon ETF) in a ΣΔ manner, thus forcing F_{CHOP} to be in quadrature with the ETF's phase shift on average. The comparator is sampled by F_{TRIG} at frequency $f = F_{DCO}/16$. As in [6], placing the input at the integrator virtual ground reduces the electrical phase shift that limited the accuracy of previous G_m-C topologies [7], thus allowing for high accuracy phase measurements. The *RC* network at the output of the 2nd integrator implements a loop-filter zero that stabilizes the loop. Although the main chopper suppresses the 1st integrator's noise and offset, system level chopping is added to reduce residual offset contributions, which would corrupt the phase sensing, by digitally reverting the polarity of F_{DRIVE} and *BS* according the two system-level-chopping states, i.e. signal *CHL* in Fig. 4 [7].

C. Digital Decimation, Loop Filter and Oscillator

The digital decimation filter, loop integrator and the digitally controlled oscillator are implemented off-chip, on an Altera Stratix IV GX FPGA, for design flexibility (Fig. 4). The decimation filter, at an input rate defined by F_{TRIG}, removes the out of band quantization noise and downsamples the signal to $F_{TRIG}/256$. The decimation filter is a second-order Cascaded Integrator-Comb (CIC) structure realizing a sinc^2 response, and consists purely of adders and registers to reduce the cost of the digital implementation. The loop filter is a digital integrator, operating at $F_{TRIG}/256$, defining the cut-off frequency of the FLL loop. The output of the integrator drives the DCO. The DCO is implemented utilizing the direct-digital synthesis (DDS) method. It employs a higher reference clock (500 MHz) and a 24-bit phase accumulator to provide an output frequency with a resolution of 30 Hz, i.e. 3 ppm at its 9-MHz free-running frequency.

IV. Experimental Results

The ETFs and the PDΣΔC, its bias circuit and driving logic were fabricated in a 0.18-μm CMOS process (Fig. 5). With a 0.7 mm^2 active area, it consumes 3.6 mW in the oxide ETF, and 0.27 mW in the PDΣΔC from a 1.8 V supply. 16 samples in DIL ceramic package were characterized in a temperature-controlled environment from −45 °C to 85 °C. A Pt100 resistor, read by a precision multimeter, served as temperature reference.

In a first set of measurements, the on-chip blocks (ETF and PDΣΔC) were tested over temperature, to derive the ETF phase shift curves (Fig. 6a). A function generator provided a constant F_{REF} = 9 MHz, therefore the ETFs were driven at 562.5 kHz. The ETF's phase shift was separately measured in the two states of the system level chopping, and then averaged off-chip. As a result, an average temperature coefficient of 750 ppm/°C was measured for the oxide ETF, 5× lower than the silicon ETF's (3700 ppm/°C). The 65-nm-CMOS oxide ETF in [5] has a lower coefficient (510 ppm/°C), and the difference is attributed to the larger oxide gap in this work, which makes the ETF more sensitive to the silicon substrate.

In a second set of measurements, the bitstream output of the PDΣΔC was fed to the FPGA, while the chips were clocked by $F_{REF} = F_{DCO}$, which was measured over temperature (Fig. 6b). The loop sets the ETF phase at the mid value of the converter's phase range, i.e. 67.5° for the oxide and 45° for the silicon ETF. As anticipated in (2), F_{DCO} is proportional to the thermal

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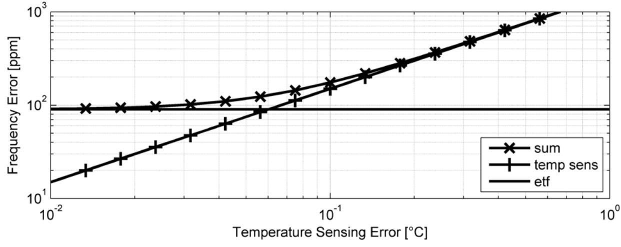

Fig. 7. Estimated accuracy of a frequency reference based on the proposed oxide frequency-locked loop, as a function of the temperature sensing errors.

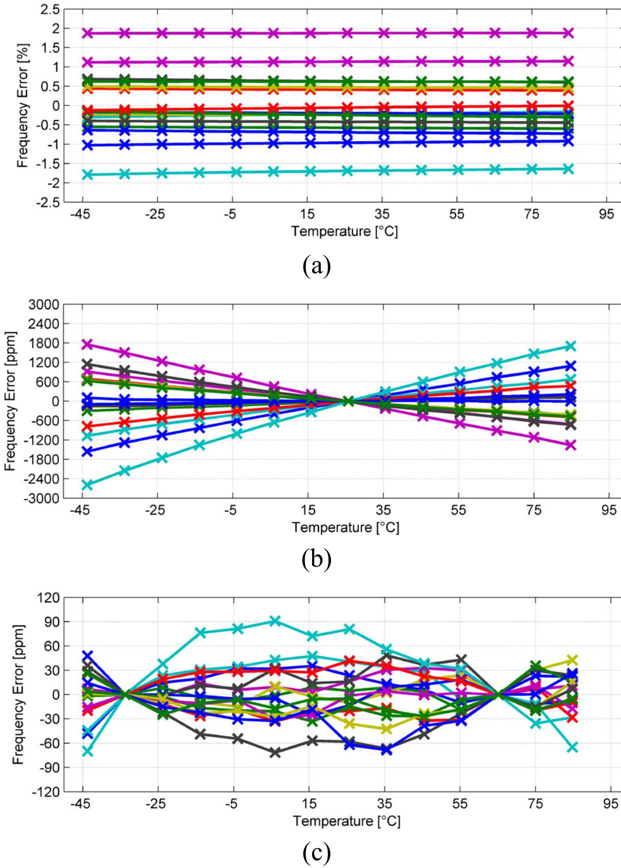

Fig. 8. (a) Measured oxide FLL's frequency error over temperature, 16 samples, untrimmed; (b) with a room-temperature one-point trim; (c) with a two-point trim.

diffusivity of silicon dioxide and silicon, respectively. F_{DCO} was separately measured in the two system-level-chopping states, and then averaged off-chip. While the silicon FLL reflects the $T^{-1.8}$ behavior of D_{Si}, leading to an average temperature coefficient of 5400 ppm/°C, the oxide ETF has a 4.5× lower temperature dependence (1200 ppm/°C). This is consistent with the previous measurements of the ETF's phase in Fig. 6a and Eq. (1).

From the curves in Fig. 6b, the average characteristic over temperature of F_{DCO} was fitted to a polynomial (master curve). The frequency error of the oxide FLL was then evaluated with respect to this master curve. The oxide FLL exhibits an accuracy of 2% ($1\sigma = 0.9\%$, Fig. 8a) without trimming, and 2700 ppm ($1\sigma = 1100$ ppm, Fig. 8b) after a one-point room-temperature trim. This improves to 90 ppm ($1\sigma = 40$ ppm, Fig. 8c) after a two-point trim.

The projected accuracy of the TD frequency reference based on the proposed oxide FLL is evaluated by adding (in the rms sense) the contribution of a compensating temperature sensor (Fig. 7). By differentiating (2), the frequency error due to a temperature sensing error ΔT is computed as $\Delta f \approx \Delta T \times 2 \times 750$ ppm/°C. By using an on-chip temperature sensors with an inaccuracy of 0.1 °C, e.g. [8], the estimated inaccuracy would still be better than 200 ppm.

V. Conclusions

The design and characterization of an FLL based on the thermal diffusivity of SiO_2 in a 0.18-µm CMOS process has been described. The oxide ETF achieves a frequency accuracy of 90 ppm (−45 °C to 85 °C), which is 11× better than that of previous TD-based frequency references, albeit at the expense of an additional trimming point. Thanks to a temperature sensitivity 5× lower than traditional silicon FLL's, its accuracy is not significantly degraded by the inaccuracy of readily realizable CMOS temperature sensors. This result demonstrates that the proposed oxide FLL can be effectively used in high accuracy TD-based frequency references.

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