

A Tiny Quadrature Oscillator Using Low-Q Series LC Tanks

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Abstract—A new quadrature oscillator topology is proposed, which arranges four low-Q series LC tanks in a ring structure driven by inverters operating in class-D. With a very small area of 0.007 mm² that is comparable to conventional ring oscillators, this oscillator has 7–20 dB better phase noise FoM of 177 dB. It is widely tunable for nearly an octave from 2.66 to 4.97 GHz.

Index Terms—Class-D oscillator, LC oscillator, low area, low phase noise, low-Q inductor, nanoscale CMOS, quadrature oscillator, ring oscillator, series LC, wide tuning.

I. INTRODUCTION

OSCILLATORS are essential building blocks in almost every SoC. For low-cost applications with relaxed performance specifications, conventional inverter-based ring oscillator (RO) structures [1]–[5] have traditionally been used. This is thanks to their small silicon area and a wide frequency tuning range (at least an octave). However, the lack of a resonator causes poor phase noise (PN) and high power consumption. On the other hand, LC-tank oscillators are predominant for high-performance applications. Though providing low PN, they normally occupy a large area and have a limited tuning range.

In this letter, we propose a novel *quadrature* oscillator with four *series* LC tanks arranged in a ring structure. By using tiny inductors with a low quality factor (Q), it features excellent PN while occupying as little area as the conventional ROs and providing a very wide tuning range of nearly an octave.

II. QUADRATURE SERIES LC TANK OSCILLATOR

A. Oscillator Core

A series LC tank driven by a voltage source is shown in Fig. 1(a). As per Bode plot in Fig. 1(b), the tank's output voltage is amplified Q_{LC} times and shifted -90° at the resonant frequency f_0 . To work properly, the tank should be driven by a low impedance source and its output should be seen by high impedance. A simple CMOS inverter, as shown in Fig. 1(c), driven by a sufficiently large input signal will provide such low driving impedance while acting as a high-impedance isolator to the preceding stage.

Since the inverter input is sinusoidal, its output jumps rapidly between two supply rail voltages, 0 V and V_{DD} , thus producing

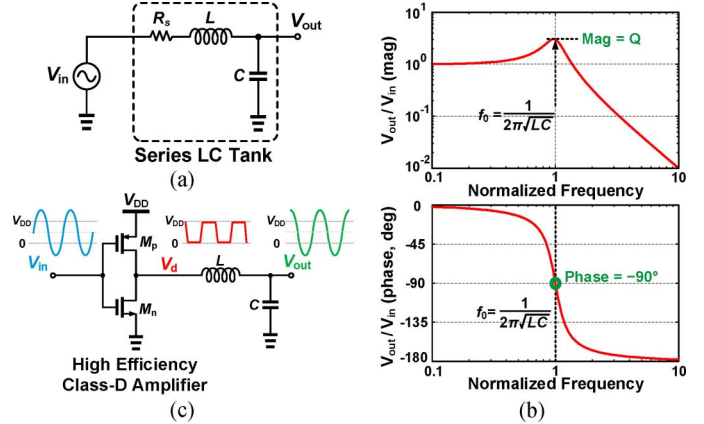


Fig. 1. (a) Series LC tank as a 90° phase shifter with (b) its frequency response. (c) Class-D amplifier as a low output impedance driver.

a near square wave. The 2nd-order low-pass LC tank filters higher harmonics and recreates a sinusoidal with a total phase shift of $+90^\circ$ with respect to the inverter's input. Four of these stages are placed in a loop to make the 360° phase shift around it, thus forming the oscillator's core (see Fig. 2(a) top). By also providing enough gain, Barkhausen criteria of oscillation are met. Therefore, if there happens to be an oscillation in the loop, the oscillator core will maintain it while creating 0° , 90° , 180° , and 270° phase outputs. Fig. 2(b) shows the transient waveforms. Having the inverters sized properly, voltage waveforms are nearly square wave. Each of the transistors conducts only when its drain-source voltage is near zero. This way the inverters are working as high-efficiency class-D amplifiers.

Assuming the inverter delay is negligible compared to the delay of each LC tank, the oscillation frequency turns out to be identical to the tank's resonant frequency

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}. \quad (1)$$

In practice, each inverter contributes a few degrees of phase shift (10 ps in this implementation), slightly lowering f_{osc} .

Superior PN performance of this oscillator topology compared to the conventional ROs is mainly due to its higher total open loop quality factor (Q_{loop}). As calculated in [6], Q_{loop} of a 4-stage inverter RO is ~ 1.4 . Applying the same methodology, Q_{loop} of the proposed oscillator is $4 \times Q_{LC}$. Therefore, a very poor quality LC tank, even as low as 1.5 (due to its tiny size) makes the total $Q_{loop} \sim 6$, thus substantially improving its phase noise. Due to the low quality of LC tanks, PN sensitivity to mismatches is very low. E.g., even a few percent capacitor mismatch does not degrade PN noticeably and only introduces a few degree of I/Q phase error.

In [7], a multiphase ring structure uses *parallel* LC tanks. Consequently it oscillates at a lower frequency than the tank's

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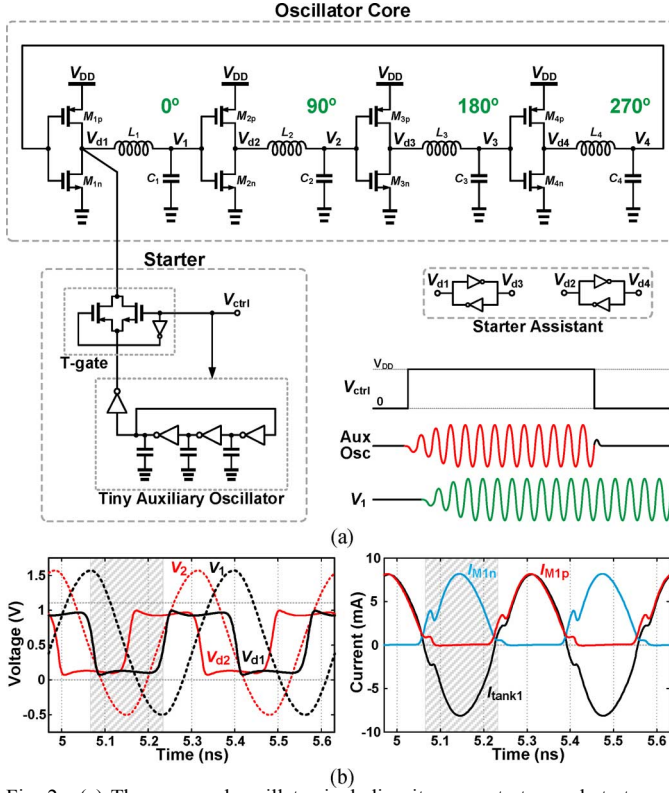


Fig. 2. (a) The proposed oscillator including its core, starter, and starter assistant circuit. (b) Transient voltages and currents of the core at 3 GHz and $V_{DD} = 1.1$ V.

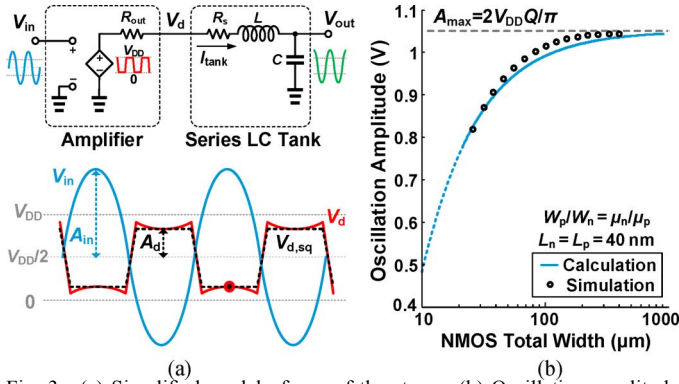


Fig. 3. (a) Simplified model of one of the stages. (b) Oscillation amplitude versus transistor width ($V_{DD} = 1.1$ V, $f_{osc} = 2.8$ GHz, and $Q_{LC} = 1.5$).

resonance with 45° phase shift per LC stage. This reduces Q_{loop} from the maximum possible. A similar structure is also used in [8] with four delay lines in a loop. However, the use of low-efficiency differential amplifiers has resulted in poor PN.

Oscillation amplitude of the proposed oscillator can be calculated based on the simplified model of one of the stages shown in Fig. 3(a). The amplifier is modeled as a voltage-controlled limiting voltage source of output resistance R_{out} switching between the ground (0) and V_{DD} . Signal V_d is then approximated with an ideal square waveform, $V_{d,sq}$, with amplitude A_d . The first harmonic of $V_{d,sq}$ is $4/\pi$ times of A_d and so output voltage amplitude becomes:

$$A_{out} = \frac{4}{\pi} A_d Q_{LC}. \quad (2)$$

From (2), peak current of the tank, that is sinusoidal and out-of-phase with V_{in} , is derived:

$$I_{peak} = \frac{4}{\pi} \frac{A_d}{R_s} = \frac{A_{out}}{Q_{LC} R_s}. \quad (3)$$

At the peak of input voltage, where NMOS is in deep triode, V_d reaches $V_{DD}/2 - A_d$. Using MOS current eq. in triode and (2)

$$I_d = k (V_{gs} - V_{th}) V_{ds} \\ = k \left(A_{in} + \frac{V_{DD}}{2} - V_{th} \right) \times \left(\frac{V_{DD}}{2} - \frac{\pi A_{out}}{4 Q_{LC}} \right) \quad (4)$$

where, k is the transistor strength equal to $\mu_n C_{ox} W/L$. At a steady-state oscillation, A_{in} must be equal to A_{out} . Also, considering that NMOS current in (4) is the same as tank peak current in (3), the oscillation amplitude is found. Fig. 3(b) shows the calculated oscillation amplitude versus transistor size, which shows a good agreement with simulations. The wider the transistor, the lower output resistance of the inverter and consequently the higher amplitude. For weaker transistors, the drain current deviates from (4) towards lower values and the loop might not even have enough gain for oscillation.

B. Startup Circuit

Before the oscillation could begin, the devices would normally be biased at proper dc operating points. Intrinsic device noise may find a small-signal loop gain higher than unity with 360° phase shift at a certain frequency, so that the oscillation could be build up.

Contrarily, in the proposed oscillator core, even though we could find an oscillation amplitude in which the loop has a large signal gain of unity or more, it will never start the oscillation on its own. Since the core contains four inverting amplifiers, there is a strong positive feedback in the loop at dc (with shorted inductors and opened capacitors) that forces the outputs of inverters to get stuck at 0 and V_{DD} (e.g., $V_{d1} = V_{d3} = 0$ and $V_{d2} = V_{d4} = V_{DD}$). At this state, the oscillator core is locked and gain of the inverters is almost zero, thus no oscillation.

Consequently, a starter circuit is added (see bottom left of Fig. 2(a)) to directly put the core in a large-signal mode thus initiating the oscillation. The starter consists of a simple *under-sized* auxiliary ring oscillator, and a T-gate switch that connects it to the core. At first, the auxiliary oscillator is turned on and connected to V_{d1} . It makes periodical perturbations to V_{d1} at close to the f_{osc} rate. Large enough perturbations can pull the second stage out of the dc lock state, which is then propagated to all stages. After the oscillation is established in the main core (in few nano-seconds), the auxiliary oscillator is turned off and disconnected. This operation is similar to starting a car engine using its starter. It could be shown that in the large-signal mode the total loop dc gain drops to less than unity and therefore the oscillator cannot fall back into the lock state.

As shown in Fig. 2(a), adding back-to-back inverters between the complementary outputs (i.e., $V_{d1,3}/V_{d2,4}$) assists with the startup. Three dummy T-gates in “off” state (not shown) connected to outputs of the other core inverters are also used to balance core phases.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

The oscillator is fabricated in TSMC 40-nm CMOS process. To make the total oscillator area as small as the ring oscillators, tiny inductors are used for the oscillator core. Each of them is a 17-turns spiral inductor using two available top thick metals in parallel, all fit in a $34 \mu\text{m} \times 34 \mu\text{m}$ area (Fig. 4). As per EM simulations, inductance value is ~ 5.6 nH with self-resonance of ~ 20 GHz. Tank Q-factor ranges from 2.0 to 3.4, though the effective Q , loaded by the output resistance of the inverters, drops

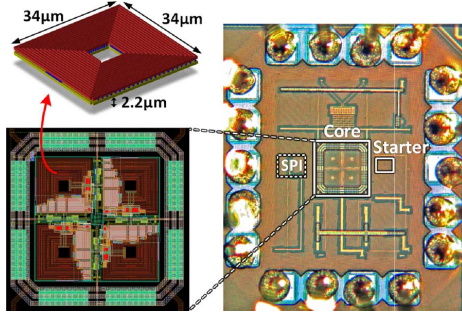


Fig. 4. Chip micrograph of the proposed oscillator with its symmetric layout.

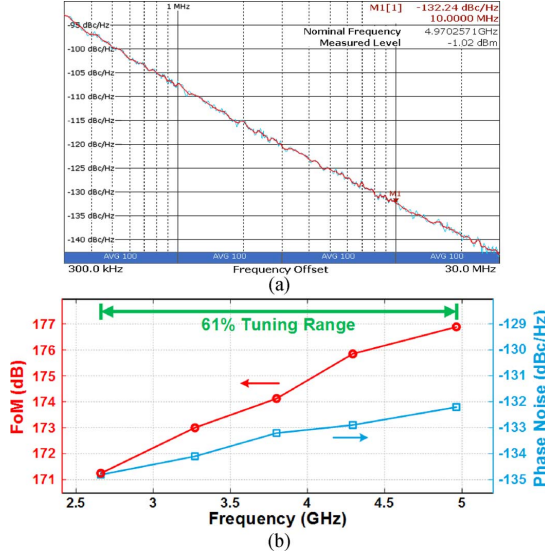


Fig. 5. (a) Measured phase noise spectrum at 4.97 GHz carrier. (b) Measured phase noise and FoM @ 10 MHz offset over tuning range.

to 1.6–2.8 over the tuning range (TR). The frequency tuning capacitors (C_{1-4}) are implemented as 5-bit binary switched-capacitor banks with a maximum value of 500 fF. Each of them is placed underneath its inductor to save area, at a cost of negligible reduction in tuning range.

The total oscillator core occupies $80 \mu\text{m} \times 80 \mu\text{m}$. Although the inductors are closely spaced, each adjacent pair has lower than 4% magnetic coupling. As measured, oscillation frequency covers almost an octave, tunable from 2.66 to 4.97 GHz (61%). Worst-case I/Q inaccuracy for 5 samples is between 35 to 45 dB ($\approx 1^\circ$) over TR.

The starter circuit is placed out of the core area and occupies $16 \mu\text{m} \times 30 \mu\text{m}$. Its frequency is tunable via 5-bit binary-weighted switched capacitors. Its TR is from 2 to 6 GHz, designed to cover more than the whole core tuning range to ensure startup at any condition.

Phase noise is measured using R&S® FSW spectrum analyzer. Fig. 5(a) shows measured PN of -132 dBc/Hz at 10 MHz offset from 4.97 GHz carrier. Fig. 5(b) shows PN and its FoM across the tuning range. At higher frequencies, where the effective Q-factor is higher, the FoM is better. To ensure reliability, V_{DD} is lowered linearly from 1.1 to 0.9 V at higher frequencies. Flicker noise corner is between 600 kHz to 2 MHz over TR.

Table I summarizes the proposed oscillator performance and compares it with state-of-the-art low-area oscillators. Its total area of 0.0069 mm^2 is comparable to a conventional inverter ring oscillator. While maximum phase noise FoM of best ring oscillators ranges 155–170 dB, the proposed oscillator offers

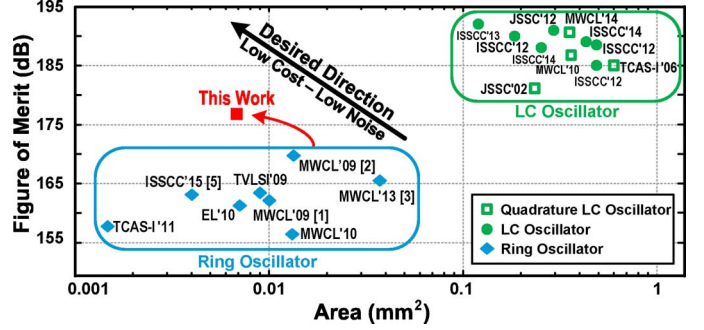


Fig. 6. FoM of state-of-the-art oscillators versus active area.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH
STATE-OF-THE-ART LOW-AREA OSCILLATORS

	This Work	[1]	[2]	[3]	[4]	[5]
Technology	40 nm	180 nm	130 nm	65 nm	45 nm	16 nm FF
Description	Series LC	Inv. Ring	Inv. Ring	Inv. Ring	Inv. Ring	Inv. Ring
Tuning Range (GHz)	2.66 – 4.97	1.7 – 5.5	1.8 – 10.2	2 – 8	2 – 3	0.25 – 4
Supply Voltage (V)	1.1 – 0.9	2.9	1.3	1.2	1.0	0.52 – 0.8
Power (mW)	16 – 8.5	81	5	1.7–6.8	3.1	4.64
Frequency (GHz)	4.97	4.46	5.6	4.2	2.4	3
Phase Noise (dBc/Hz) @ (MHz)	-132.2 @10	-120.2 @4	-121.7 @10	-101 @1	-121 @10	-120.2 @10
FoM* (dB)	171.3 – 176.9	162.2	158.3–169.9	165.4	163.7	163.0
Area (mm²)	0.0063	0.01	0.0144	0.038	NA	~0.004

$$^* \text{FoM} = |\text{PN}| + 20 \log_{10}(f_{\text{osc}}/\Delta f) - 10 \log_{10}(\text{Pdc}/1 \text{ mW})$$

7–20 dB better FoM. In fact, its FoM is the best amongst all other small-size oscillators and almost reaches the FoM of regular large-area LC-tank RF oscillators. Fig. 6 plots FoM of state-of-the-art ring and LC oscillators versus their active area. The proposed oscillator clearly stands out between the two groups: for low-cost (i.e., area) applications, it has a lower PN or power consumption than ring oscillators; for high performance applications, it saves significant area by consuming somewhat higher power compared to normal LC oscillators.

IV. CONCLUSION

A new oscillator topology is proposed that arranges four series LC tanks in a ring structure. By using low-Q inductors it occupies the same chip area as ring oscillators while significantly reducing the phase noise and maintaining wide tuning range.

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