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Analysis of Mismatch Effects in Matrix-Based Systems Using Dynamic Element Matching (Out of the chains and into the matrix?)

Alex Calinescu[1], Traian Antonovici[2], and Marius Enachescu[3]

[1,3]Electronic Devices, Circuits and Architectures , Faculty of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, Bucharest, Romania ,
[2]Electronic Instrumentation Laboratory, Delft University of Technology
Email ids: [1]alex.calinescu@stud.etti.upb.ro, [2]t.antonovici@student.tudelft.com, [3]m.enachescu@upb.ro

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***Abstract*—The Dynamic Element Matching (DEM) technique's role is to mitigate mismatch issues in complex, matrix-based systems. In this paper, we explore the impact of partially applying DEM to the thermometrically encoded 10-bit most significant bits (MSBs) out of a high-resolution segmented 16-bit Digital-to-Analog Converter (DAC) with the least significant 6 bits being binary encoded. Specifically, we design a general purpose scalable digital control circuit able to employ the DEM algorithm, independent of the matrix dimensions. When implementing the proposed controller using a commercial 180 nm CMOS process, tailored to the 10-bit thermometric decoded DAC MSBs, the integral nonlinearity (INL) 12.63 times lower and the differential nonlinearity (DNL) is 5.8 times lower. The silicon area required for the additional circuitry is around 0.12 mm^2, with a power consumption of up to 12.88 mA from a 1.8 V power supply when running at 100 MHz.**

***Index Terms*—Dynamic Element Matching, Digital Controller, INL, DNL, DAC, Mismatch.**

I. Introduction

High resolution DACs are an integral part of a hi-fi audio system. Unfortunately, component mismatch creates nonlinearity, degrading the system's performance. As shown in [1], segmentation is an attractive method to reduce a DAC's differential nonlinearity, at the cost of additional chip area. This method implies splitting the DAC in multiple sections (called segments), coded either binary or thermometric, and using an additional digital decoding step to convert the input data into the required format. Usual designs, such as the one in [2], use a thermometric coded MSB segment and a binary coded LSB one. At the expense of additional area required for the decoder and associated routing, segmented DACs mitigate DNL while maintaining the same integral nonlinearity (INL).

The Dynamic Element Matching (DEM) technique is used to increase the precision of analog and mixed-signal systems. The studies from [2-4] have employed DEM to reduce the gain error in an instrumentation amplifier. Notably, in [2] a digital control circuit that implemented a DEM algorithm was attached to a $16\times$ programmable-gain amplifier (PGA) to reduce the gain error to ppm level. Hence, this paves the way to explore its potential to mitigate mismatch-induced INL errors that occur during the conversion of discrete digital input codes into continuous analog signals.

Alternatively, the DEM technique is used when designing digital to analog converters, but avoid complete thermometric encoding, choosing to employ other techniques such as dithering [5-6]. In [7], each bit controls two identical binary-weighted elements and applies DEM by interchanging between them periodically, not exploiting the entire potential of the dynamic element matching technique.

Starting from [1], this work presents the design of a DEM digital controller for a 16-bit DAC with 10 bits thermometrically encoded. With an area of 126000 μm^2 and a current consumption of up to 12.88 mA at 100 MHz, this digital controller will employ an implementation of the DEM principles by periodically switching between DAC elements when building the analog output to efficiently reduce the INL $12.63\times$ and the DNL $5.79\times$. To achieve the desired performance, the DAC elements are organized in a matrix structure to facilitate the required shuffling method.

The rest of the paper is organized as follows. Section 2 presents the background. Section 3 details the proposed digital controller implementation from a system standpoint. Section 4 presents the system implementation together with a comparative analysis showcassing the DEM techniques advatages. And finally, the paper concludes in Section 5.

II. Backgroud

This section explains the theory behind the Dynamic Element Matching technique and explores how component mismatch affects matrix-based systems. The study specifically looks at a 10-bit thermometric encoded digital-to-analog converter in the matrix system being studied.

A. The Dynamic Element Matching technique

The DEM technique is used to mitigate the effects of mismatches between elements of a system that are intended to be identical [2-4]. An element's mismatch is characterized as the deviation between its actual value and its intended value. This discrepancy is a result of fabrication process variations and can be mathematically represented by Eq. 1.

$$c_{i,j} = c(1 + \epsilon_{i,j}), |\epsilon_{i,j}| < 1 \quad (1)$$

In a system composed of multiple elements, $c_{i,j}$, each element deviates from the ideal expected value, c, due to its individual mismatch $\epsilon_{i,j}$. By toggling between various configurations (activating or deactivating elements), the system produces a different output each time. Averaging these output values yields a value closer to the ideal intended output. Let $b_{i,j}$ represent binary values indicating the activation state of the matrix element (0 for inactive, 1 for active). The output S of the $M \times N$ system is determined by Eq. 2.

$$S = \sum_{i=1}^{M} \sum_{j=1}^{N} b_{i,j} c_{i,j} \tag{2}$$

When switching between active elements, a specific configuration is represented by an $M \times N$ matrix constructed using the $b_{i,j}$ values. For instance, a system with only 2 elements can be denoted by the element matrix $[c_{1,1}\ c_{1,2}]$ and configuration matrices [0 1] and [1 0]. Depending on the configuration, either $c_{1,1}$ or $c_{1,2}$ is generated. Three possible cases can be summarized in Eq. 3: i) when both elements' true values are slightly below the ideal value c, the average output falls between the two real outputs, below the ideal output; ii) similarly, if both possible outputs exceed the ideal value, the average output falls between the two real outputs, above the ideal output, and iii) when one output surpasses the ideal value and the other falls short, the average output tends to be closer to the ideal expected output than either individual output.

$$S_{average} = \frac{S_1 + S_2}{2} = c + \frac{\epsilon_1 + \epsilon_2}{2} \tag{3}$$

Scenarios 1 and 2 yield a gain error which can be corrected in the digital domain. For the third scenario, utilizing the DEM technique mitigates the system's output error, hence aligning with the mean value of the mismatch distribution.

This study will use a thermometric digital-to-analog converter for the 10 most significant bits, serving as a matrix-based system for the application of the DEM technique. This design incorporates 2^n-1 identical 1-bit DACs activated by 2^n-1 bits derived from the binary input code, where n represents the DAC's bit count. The system under examination features a 10-bit DAC with this architecture, capable of generating 1023 distinct non-zero voltage levels [1]. The first step is arranging the 1-bit DAC cells into a 32×32 matrix. The next step is symetrically bordering it with $2r$ additional rows and $2c$ additional columns, establishing the matrix system for DEM implementation. For instance, if both r and c equal 10, the DAC matrix becomes 52×52.

In this scenario, the DEM algorithm will include the core DAC matrix with additional identical cells, forming the "border" around the matrix. Fig. 1 illustrates the generalized schematic of the proposed matrix-based thermometric DAC system. The light orange cells represent the additional DEM cells necessary for the algorithm, while the white cells relate to a standard thermometrically encoded matrix DAC.

III. The DEM Digital Controller

This section describes the design and operation of the proposed digital control circuitry required for a DEM system.

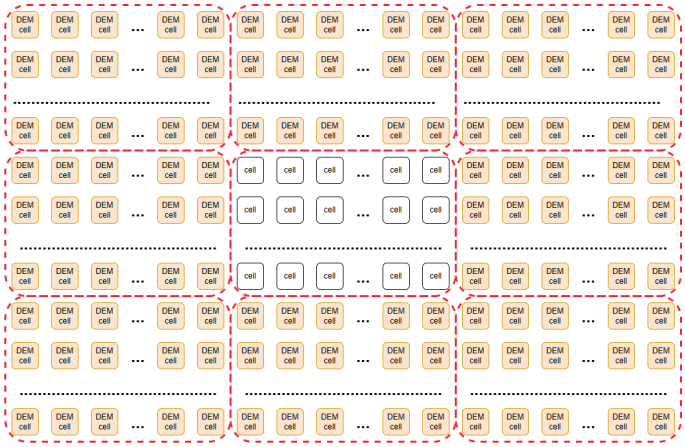

Fig. 1. Generalized Cell Matrix

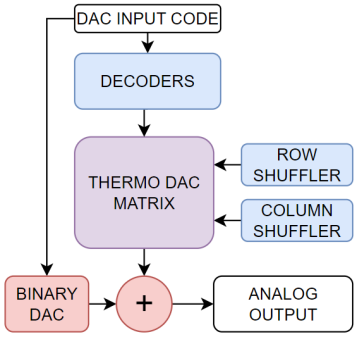

Fig. 2. System-level schematic diagram

The schematic diagram shown in Fig. 2 illustrates the structure of the proposed matrix system. Blue blocks represent digital circuits and signals, while red blocks represent analog components. The digital controller is responsible for controlling the output of the 10-bit thermometric DAC arranged in a matrix configuration. Initially, the controller separates the 10 most significant bits (MSBs) from the 6 least significant bits (LSBs). The LSBs are directed to a 6-bit binary-weighted DAC, while the 10 MSBs are sent to the DEM controller.

The DEM digital controller converts the digital input code into a matrix of cell control signals, establishing an initial configuration for the cell matrix. This conversion involves two decoding stages: first, the 10-bit binary code is transformed into a 1023-bit wide bus, followed by rearranging this bus into a set of data indexed by rows and columns.

The cell matrix shuffling is controlled by two pseudo-random number generators that manage the cell shifting direction. One generator handles column shifting and another manages row shifting. The controller switches between the two shufflers in each clock cycle.

The design is highly flexible and can be easily scaled and customized for different cell matrix sizes, input data sizes, and variations in the number of additional DEM cell rows and columns. This adaptability is enabled by defining a set of design parameters during the circuit generation process using Hardware Description Languages (HDL) like Verilog, SystemVerilog, or VHDL. Table I outlines the key design parameters that form the foundation of the digital controller.

TABLE I
DEM CONTROLLER' MAIN DESIGN PARAMETERS

Design parameter name	Value	Comments
THERMO_BITS	10	Number of DAC bits
MATRIX_ROWS	32	
MATRIX_COLS	32	
DEM_ROWS	10	Additional DEM rows
DEM_COLS	10	Additional DEM columns

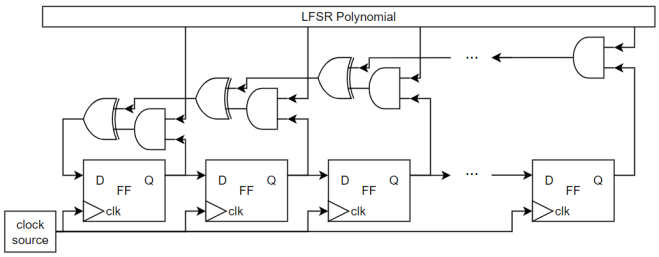

Fig. 3. Row and Column Shuffler

To transform the binary input code into the initial state of the matrix cell system, two decoding circuits are required: a standard thermometric decoder and an additional circuit dedicated to creating the initial configuration for the cell matrix. The matrix generation logic uses the binary-to-thermometric decoder's output to arrange and populate the rows and columns of the matrix. The thermometric encoded bus is segmented into sub-buses, each with a width corresponding to the quantity of rows, resulting in 32 sub-buses of 32 bits each. These sub-buses provide the preliminary configuration data for the cell matrix when the DAC initiates a new conversion.

During each shuffling step, the state of the cell matrix is altered. In every odd clock cycle, the rows are shifted, while in every even clock cycle, the columns are shifted. To ensure equal utilization of each cell, the shifting direction for rows and columns is determined by each bit of a shuffler. A logic 1 indicates a shift to the right or down, while a logic 0 signifies a shift up or to the left. To introduce randomness in the shifting pattern, hardware pseudo-random number generators in the form of linear feedback shift registers are used to generate the shifting direction bits. Fig. 3 illustrates the internal structure of such a circuit, excluding the reset connections. Additionally, Fig. 4 displays the configuration of a single matrix cell control element along with its associated 1-bit DAC element. Digital circuitry components are represented in blue, while analog circuitry components are depicted in red. The configuration data is the initial state of the cell when a new conversion is initiated. When the DEM circuitry is enabled, the DEM cell data input contains the current state of the surrounding matrix cells, and the row and column shuffling circuitry starts its operation.

IV. RESULTS

The following section presents the area and power required by the presented DEM digital controller and simulation results.

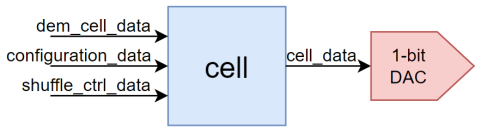

Fig. 4. Cell element structure

A. Implementation results

Following the 180 nm CMOS commercial process implementation step using a automated backend design flow, the proposed digital controller has been evaluated yielding the power and timing reports presented in Table II and Table III. The analysis was perfomed over process variations, temperature (-55^{o}C, 25^{o}C or 125^{o}C) and supply voltage (1.62 V, 1.8 V or 1.98 V). In terms of timing, the longest propagation delay (the time taken for a signal to travel from its source to destination without violating setup or hold times) is under 7.28 ns, corresponding to a maximum system operating frequency exceeding 128 MHz, hence 28% higher than the targeted system clock speed. In terms of power, the proposed controller will drain up to 12.88 mA when operating at 100 MHz.

TABLE II
AREA REPORT

Area report [μm^2]			
Module	Area	Instances	Total
bin2thermo_matrix	33301.184	1	33301.184
matrix_cell	34.006	2704	91952.224
prng	405.6	2	811.2
DEM Digital Controller			126064.608

TABLE III
POWER REPORT

Power report [nW] @100 MHz			
Module	Power	Instances	Total
bin2thermo_matrix	4136692.764	1	4136692.764
matrix_cell	4065.008	2704	10991781.632
prng	4022821.705	2	8055643.411
DEM Digital Controller			23184117.807

B. Simulation Results

This section will detail the performance evaluation of the chosen DEM-based DAC architecture. Note the number of shuffling operations per code (and therefore the number of measurements per code) will be referred to as the oversampling ratio (OSR).

Fig. 5 presents the DAC's INL and DNL results for the DEM digital controller adapted to 10 additional DEM rows and columns and 1024 clock cycles of shuffling for each code. The results show that the highest absolute INL has decreased from 0.821 to 0.065 LSBs, while the highest absolute DNL has decreased from 0.603 to 0.104 LSBs. Fig. 6 presents the full 1024-codes INL curves for OSR values ranging between 1 and 1024, while Fig. 7 highlights how the maximum absolute INL and DNL values decrease from 0.821(INL) and 0.603(DNL) when the OSR is 1(so no shuffling), to 0.065 LSBs(INL) and 0.104 LSBs(DNL) when the OSR reaches 1024. Hence, running multiple shuffling steps for each input code allows the average output value to match the ideal desired output.

Fig. 8 represents the power spectral density comparison between the DAC with and without the DEM algorithm when synthesizing a full-scale sinewave with 5% element mismatch. The DEM scheme renders the HD2 and HD3 components non-distinguishable against the noise floor, as expected. Compared to the non-DEM DAC, the SFDR is increased by 18dB, making the DEM-based DAC a good candidate for hi-fi audio.

Fig. 9 presents the grayscale histograms for multiple OSR values. The data indicates that by using the proposed shuffling

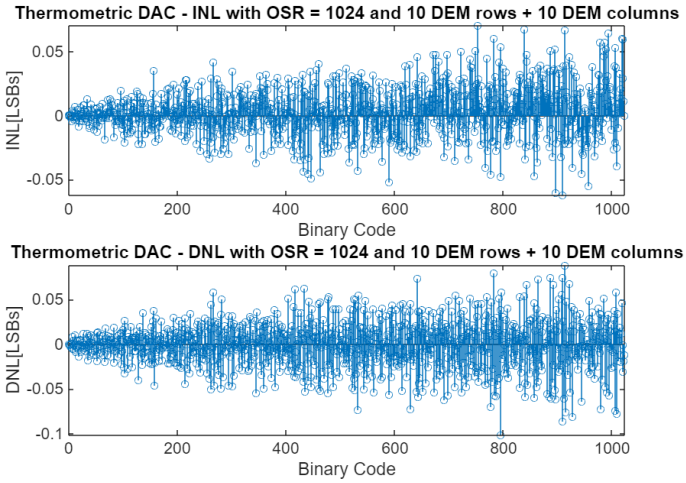

Fig. 5. INL and DNL measurements for a DEM DAC with 10 DEM rows, 10 DEM columns and an oversampling ratio of 1024.

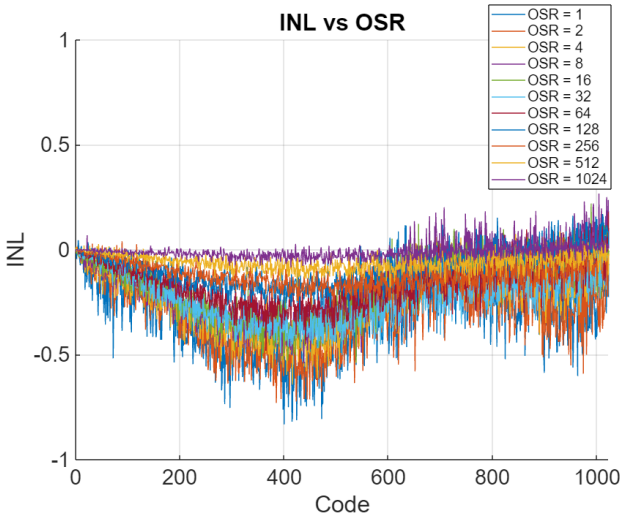

Fig. 6. INL evolution of the DEM DAC for different OSR values.

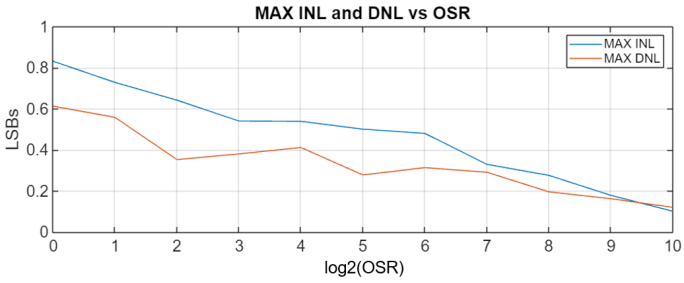

Fig. 7. Max INL and DNL values for different OSR values.

algorithm with additional cells for a matrix-based system results in a 12.63 times smaller INL and a 5.8 times smaller DNL. With a system clock of 100 MHz and an OSR of 2048, the effective sampling rate of the converter is 48.828 kHz, highlighting the tradeoff between speed and precision. Nonetheless, this sampling rate remains suitable for low-speed audio applications.

V. Conclusions

The proposed digital controller, implemented in a commercial 180 nm CMOS process, occupies 126000 μm^2 and consumes up to 12.88 mA from a 1.8 V power supply at 100 MHz.

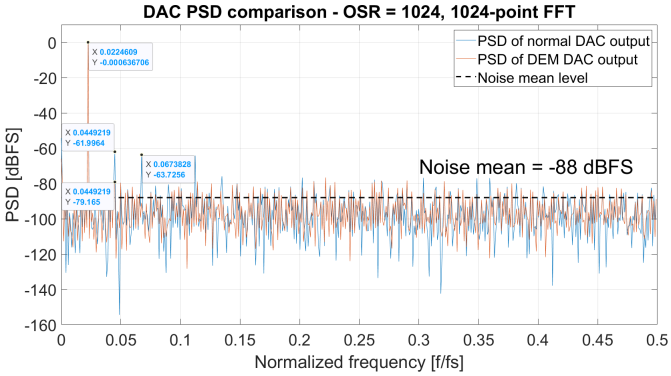

Fig. 8. PSD of DEM-DAC and non-DEM DAC outputs.

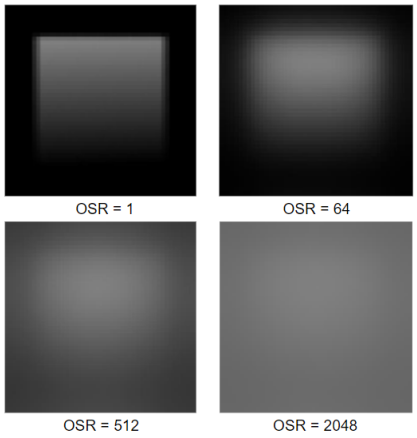

Fig. 9. Grayscale histograms of different OSR values for the same matrix.

Utilizing the DEM technique to address element mismatch, the controller is evaluated on 10-bit thermometrically encoded section of a 16-bit DAC. The DEM algorithm improved the INL 12.63 times, the DNL 5.8 times and achieved uniform cell usage distribution.

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