Design and Simulation of CMOS-compatible Micro-structured Ge-on-Si Wideband Image Sensor

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TU Delft

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by

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There is always more than what meets the eye...

... for the eye cannot see wavelengths beyond 750 nm.

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Abstract

The bandgap limitation of silicon (Si) limits the imaging capabilities of conventional Si CMOS Image Sensors to wavelengths below 1100 nm and thus are inadequate for near-infrared (NIR) / short-wave infrared (SWIR) imaging applications such as metrology, medical imaging and computer vision. Current SWIR image sensors, while capable of detecting wavelengths up to 2000 nm, suffer from several critical drawbacks: they are incompatible with CMOS technology, lack the scalability inherent to CMOS processes, and are prohibitively expensive.

This thesis presents the design and simulation of a CMOS-compatible microstructured germanium-on-silicon (Ge-on-Si) visible and SWIR wideband image sensor. The proposed design uses light-trapping microstructures on the sensor's surface to help enhance the optical efficiency of the infrared-sensitive germanium layer while maintaining compatibility with standard CMOS fabrication techniques. The proposed design is highly scalable, with diffusion-drift and finite-difference time-domain (FDTD) simulations of pixels with 5 um, 15 um and 55 um pitches demonstrating a quantum efficiency of 28% at 1000 nm and 2% at 1300 nm using only a 100 nm Ge layer while also being compatible with the 4T-pixel active pixel sensor (APS) architecture. With future developments using 1 µm Ge layer potentially allowing for QE over 40% across the entire visible+NIR/SWIR spectrum, such a design will enable integrated wideband integrated imaging applications that can utilize the developments of existing CMOS image sensors.

Keywords - CMOS-compatible, Wideband, Short-Wave Infrared, Ge-on-Si, Image Sensor

Contents

List of Figures

List of Tables

Nomenclature

Abbreviations

Abbreviation	Definition
APS	Active Pixel Sensor
BEOL	Back End of Line
CMOS	Complementary Metal-Oxide-Semiconductor
FDTD	Finite Difference Time Domain
FEOL	Front End of Line
MP	Megapixel
NIR	Near Infrared
QE	Quantum Efficiency
RoHS	Restriction of Hazardous Substances Directive
ROIC	Read-Out Integrated Circuit
SR	Spectral Response
SRH	Shockley-Read-Hall
SWIR	Short-wave Infrared

Symbols

Symbol	Definition	Unit
α_{abs}	Absorption Coefficient	[cm^{-1}]
A	Area	[μm^2]
n	Refractive Index	[-]
k	Extinction Coefficient	[-]
λ	Wavelength	[nm]
$\mu_{n,p}$	Charge carrier mobility	[cm$^2 s^{-1} V^{-1}$]
t	Time	[s]
ε_r	Relative permittivity	[-]
E_g	Energy band gap	[eV]
E_C	Conduction band energy	[eV]
E_V	Valence band energy	[eV]
E_{Fn}	Fermi energy level	[eV]
FF	Fill Factor	[%]
$\mathbf{J_{e,h}}$	Current density of charge carriers	[A/cm^2]
$N_{A,D}$	Dopant density	[cm^{-3}]
τ	RC Time constant	[s]

Physical Constants

Symbol	Definition	Value
c	Speed of light	3×10^8 m/s
q	Electron charge	1.602×10^{-19} C
ε_0	Permittivity of free space	8.854×10^{-14} F cm^{-1}
h	Planck's constant	6.626×10^8 m/s

Symbol	Definition	Value
k_B	Boltzmann's constant	$1.381 \times 10^{-23} JK^{-1}$
m_0	Free electron mass	9.1×10^{-31}
T_0	Reference temperature	293 K

1

Introduction

The human eye, a marvel of evolution, through which all visual information over the history of humanity has been processed with remarkable efficiency, is fundamentally limited to only a narrow band of the electromagnetic (EM) spectrum, referred to as visible light, spanning from approximately 400 nm to 700 nm (Fig. 1.1(a)) [1]. The visible light spectrum, from violet to red, corresponds to the peak of solar radiation that reaches the earth's surface, with earth's atmosphere filtering out much of the ultraviolet and infrared radiation [2]. Thus the human vision has evolved to maximize the use of available light in our environment. Interestingly, silicon, the material that forms the backbone of modern electronics and image sensing technologies, exhibits a spectral response that closely mirrors human vision. Silicon-based photodetectors are typically sensitive to wavelengths up to about 1100 nm, just slightly beyond the visible spectrum [3]. This alignment between human vision and silicon's photoelectric properties has been instrumental for the development of digital imaging technologies, as it has allowed for the creation of cameras that capture images in a way that closely approximates human visual perception.

While the visible spectrum has served human needs admirably throughout our evolutionary history and continues to be crucial for our day-to-day experiences, there are significant advantages to expanding our sensing capabilities beyond this limited range. The near-infrared (NIR) and short-wave infrared (SWIR) regions of the spectrum, which lie just beyond visible light, offer unique properties that can greatly enhance the capabilities of current digital imaging applications.

NIR typically refers to wavelengths from about 750 nm to 1000 nm, while SWIR extends from about 1000 nm to 3000 nm [4]. This region of the EM spectrum has a distinctive characteristic that makes it particularly useful for imaging applications: the low photon energy of the NIR/SWIR spectrum allows for the selective penetration of materials that are opaque to visible light, as well as not being scattered in poor-visibility atmospheric conditions. Thus development of a visible + NIR/SWIR wideband sensor can have far-reaching implications across numerous fields:

- Consumer electronics: Smartphones and other portable devices could incorporate NIR/SWIR imaging capabilities, enabling improved low-light imaging capabilities, biometric authentication, and environmental sensing [5, 6].
- Environmental Imaging: Wideband sensors could improve our ability to detect and measure various environmental parameters from crop health in agriculture to pollution levels in urban areas, as well as image through smoke and haze during disasters such as fire or earthquakes (Fig. 1.1(b) [7]) [8, 9].
- Metrology: NIR/SWIR radiation can pass silicon but is opaque to other materials such as metal interconnects on an integrated circuit, thus allowing for through-silicon metrology for the inspection of buried layers (Fig. 1.1(c) [10]) [11].
- Automotive safety: A visible + NIR/SWIR wideband sensor can be integrated into automobiles, improving visibility through smoke, haze, and poor lighting conditions and enhancing overall safety in autonomous and assisted driving systems (Fig. 1.1 (d) [12]).

- Medical Imaging: Non-invasive diagnostic tools could be developed using visible + NIR/SWIR imaging, potentially allowing for earlier detection of certain diseases or more accurate monitoring of physiological processes (Fig. 1.1 (e) [6]) [13, 14]
- Industrial automation: Low-cost, compact NIR/SWIR sensors could enhance quality control processes, material sorting, and machine vision systems in manufacturing environments [15].
- Security and surveillance: Enhanced night vision capabilities and the ability to see through obscurants could significantly improve security systems and law enforcement tools [16].

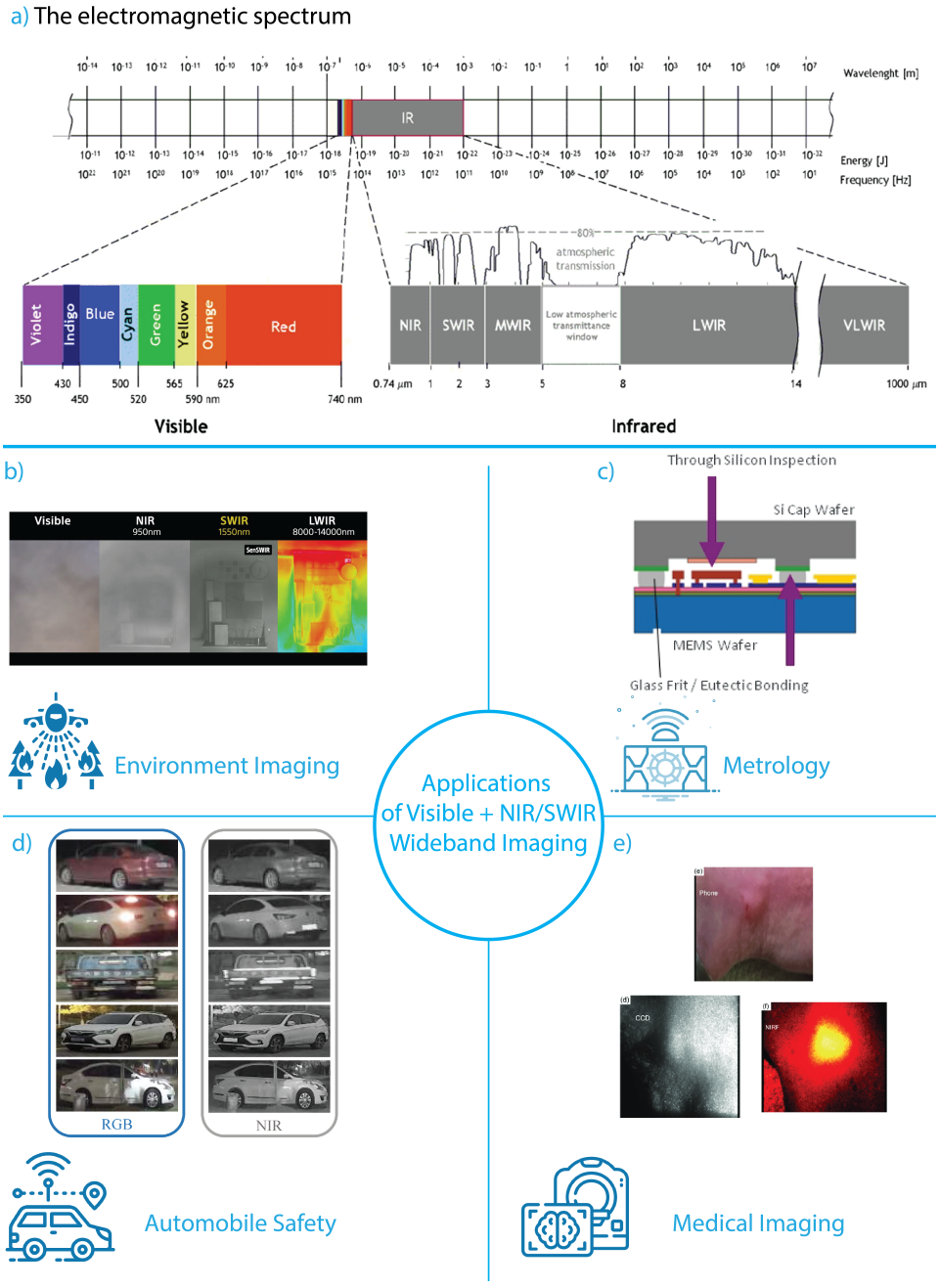


Figure 1.1: a) The electromagnetic spectrum, highlighting the visible and Infrared spectra. (b-e) Applications of visible + NIR/SWIR imaging.

The potential applications of visible + NIR/SWIR imaging are vast and diverse, underscoring the importance of overcoming the current limitations of visible and NIR/SWIR imaging technology. By developing CMOS-compatible wideband image sensors, we can bridge the gap between the specialized, high-cost

NIR/SWIR image sensors currently available and the widespread, low-cost, visible-spectrum CMOS image sensors needed to unlock the full potential of wideband imaging across various industries and applications.

1.1. Research Statement and Auxillary Questions

The development of a CMOS-compatible wideband image sensor capable of detecting both visible and NIR/SWIR radiation presents a formidable challenge at the intersection of materials science, semiconductor physics, and electronic engineering. This challenge is compounded by the stringent requirements of CMOS compatibility and the unique properties of NIR/SWIR radiation. The overwhelming majority of image sensors currently used are silicon-based CMOS and CCD sensors - leveraging the scalability and precision of integrated-circuit (IC) fabrication processes has resulted in low-cost, high-speed, high-resolution and low-noise image sensors that can be integrated with other electronics onto an IC [17]. However, due to the inherent bandgap limitation of silicon, with sensitivity only up to wavelengths of 1100 nm [18], CMOS image sensors are incapable of NIR/SWIR imaging. Although extensive research has been carried out into developing highly efficient NIR/SWIR image sensors using technologies such as Indium-Gallium-Arsenide (InGaAs) [19] and quantum dots [20], these technologies are incompatible with the CMOS-fabrication processes and thus cannot be integrated into the standard CMOS IC flow. As these NIR/SWIR image sensors have to be fabricated separately, they then need to be connected to read-out circuits using highly complex 3D integration processes [21, 22]. This results in complexity in design, larger dies, lower reliability, slower readout speeds and poor scalability [23, 24].

For any NIR/SWIR image sensor to be CMOS-compatible, this work envisions several critical constraints that the development process must adhere to:

- Low-temperature fabrication processes: CMOS compatibility demands that all additional processing steps required for NIR/SWIR sensitivity must be carried out at temperatures compatible with existing CMOS structures. Typically, this means keeping process temperatures below 300°C, known as the thermal budget, to prevent degradation of metal interconnects and dopant profiles in the underlying CMOS circuitry.[25].
- RoHS compliance: The sensor must adhere to the Restriction of Hazardous Substances (RoHS) directive, which restricts the use of certain hazardous materials in electrical and electronic equipment. This requirement excludes the use of many traditional infrared-sensitive materials, such as lead-based compounds, which have been commonly used in IR detectors [26].
- Back-End-Of-Line (BEOL) integration: All SWIR-enhancing processes must be implemented in the Back-End-Of-Line stages of fabrication to maintain compatibility with standard CMOS front-end processes foundaries. This constraint means that any additional layers or structures for NIR/SWIR detection must be added after the formation of transistors and initial metal interconnect layers.

Given these constraints and the potential benefits of such a sensor, the main research statement of this thesis can be articulated as follows:

”Can a CMOS-compatible image sensor be designed and fabricated for visible + SWIR wideband imaging applications, while adhering to low-temperature processing, RoHS compliance, and BEOL integration requirements?”

This overarching question encompasses a wide range of technical challenges and considerations. To systematically address this question and guide the reader through the fundamental concepts, design considerations, simulation results, and final conclusions, the following auxiliary questions have been formulated:

- What are the current state-of-the-art SWIR image sensors, and what key factors make these image sensors CMOS incompatible?
- What are the different potential CMOS-compatible processes that can be used to expand the spectrum of an image sensor into the SWIR spectrum?

- How can an image sensor be designed to incorporate the shortlisted CMOS-compatible processes?
- What is the expected performance of an image sensor designed using these processes?
- What limitations can be identified in such an image sensor?

By addressing these questions in sequence, this report aims to provide a comprehensive exploration of the challenges and potential solutions in developing a CMOS-compatible wideband image sensor.

1.2. Report Structure

This report is structured into five chapters. Chapter 1 presents the baseline of the project, as well as the research statement and auxiliary questions addressed in this thesis. Chapter 2 provides a brief background and introduction to the development of CMOS image sensors. Chapter 3 comprises of the complete theory required during the design and performance characterization of a CMOS Image Sensor, as well as the CMOS fabrication steps. Chapter 4 discusses the different technologies currently used to build NIR/SWIR image sensors, providing their respective advantages and drawbacks. Chapter 5 presents the two CMOS-compatible processes identified as part of this project that can potentially enhance the SWIR sensitivity of a CMOS image sensor. The design and simulation of the proposed image sensor that incorporates the processes identified is presented in chapter 6, detailing the device-physics and optical simulation results. The final chapter 7 presents the main conclusion and recommendations of this research. The Appendix includes all additional figures not included in the main text, such as the mask-layout designed for fabrication.

2

Background - CMOS Image Sensors

In this chapter, the background of development that lead to the CMOS image sensors, as well as different NIR/SWIR Image sensors is discussed to provide an understanding of the interest and potential of the image sensing market. This chapter provides elaboration on the motivation of this project that has been previously discussed.

2.1. Developments leading up to the CMOS Image Sensor

The history of modern digital image sensors is deeply rooted in the evolution of photography and imaging technology, dating all the way back to the 4th century BCE Chinese text describing the the camera obscura - darkened room with a small hole that projected an image on the opposite wall. However, interest in the development of a practical image sensor began with the discovery of phenomenon of silver salt darkening upon exposure to sunlight by Johann Heinrich Schulze in the early 18th century. Schulze's work laid the groundwork for the development of the pin-hole camera, a simple yet revolutionary device that captured images through a small aperture, projecting them onto a darkened interior surface [27].

The invention of the daguerreotype in 1839 by Louis Daguerre marked a significant leap forward. Using a silver iodide (AgI) plate, the daguerreotype process produced detailed and stable images. This method dominated early photography until the introduction of glass plate negatives in the 1850s, which used a wet-collodion process developed by Frederick Scott Archer. These glass negatives were more versatile and provided higher quality images than their predecessors [28].

The late 19th and early 20th centuries saw further advancements with the introduction of film development. George Eastman's development of roll film in 1884 and the Kodak camera in 1888 democratized photography, making it accessible to the masses [29]. Motion cameras, introduced by Thomas Edison and the Lumière brothers, brought about the era of cinematography, capturing moving images on film.

Single-lens reflex (SLR) cameras emerged in the mid-20th century, offering photographers greater control over composition and exposure. These cameras used a mirror and prism system to allow the photographer to see exactly what would be captured on film. The advent of color film further enhanced the capabilities of photographic technology.

The transition from analog to digital imaging began with the invention of the charge-coupled device (CCD) in 1969 by Willard Boyle and George E. Smith. CCDs offered high-quality imaging and were initially used in astronomy and scientific applications - primarily due to its independence of performance from the lithographic process used, which allowed for the development of application specific architectures [30]. However, they were limited by very high power consumption and complex fabrication processes - restricting widespread consumer adoption [31].

Complementary metal-oxide-semiconductor (CMOS) image sensors (CIS), developed in the late 20th century by Eric Fossum [32], addressed many of the limitations of CCDs. CMOS sensors integrated

the image sensor and signal processing on a single chip, reducing power consumption and manufacturing costs. Early CMOS sensors faced challenges in image quality and noise, but advancements in technology have significantly improved their performance, nearly matching CCDs in most applications [33]. With the advantages of low-cost and high scalability of CMOS image sensors with advancements in the fabrication processes, CMOS Active Pixel Sensors (APS) overtook CCDs in market share of consumer image sensors, with the current market size of $ 22.85 Billion and is expected to grow to $32.22 Billion in the next 5 years [34]. Fig. 2.1(b) shows the commercial shipments of CIS and CCD image sensors for different applications over the years [35].

The rapid advancement of CMOS technology enabled the development of high-resolution sensors. In 2016 Phase One introduced the world's first 100 megapixel (MP) medium format CMOS sensor only to surpass it in 2 years with the introduction of a 150MP medium format CMOS sensor [36, 37], showcasing the technology's scalability and capability to produce extremely detailed images. Fig. 2.1(c) shows the shrinking of the pixel pitch sizes of CIS and CCD sensors over the years [35].

The introduction of stacked CMOS sensor technology marked another significant advancement. By separating the photodiode layer from the readout circuitry, stacked sensors achieve higher performance in a more compact form factor. Sony's introduction of stacked CMOS sensors in 2021 revolutionized smartphone camera capabilities [38]. This technology has since become a standard in high-performance imaging devices, enabling remarkable improvements in speed, dynamic range, and low-light performance. Fig. 2.1 (a) shows the timeline of developments in image sensing technologies.

Thus, as CMOS image sensors continue to evolve, it is of great interest to expand the sensing capabilities into the NIR/SWIR spectrum while retaining the technological advantages of CMOS image sensors, which is the focus of this project.

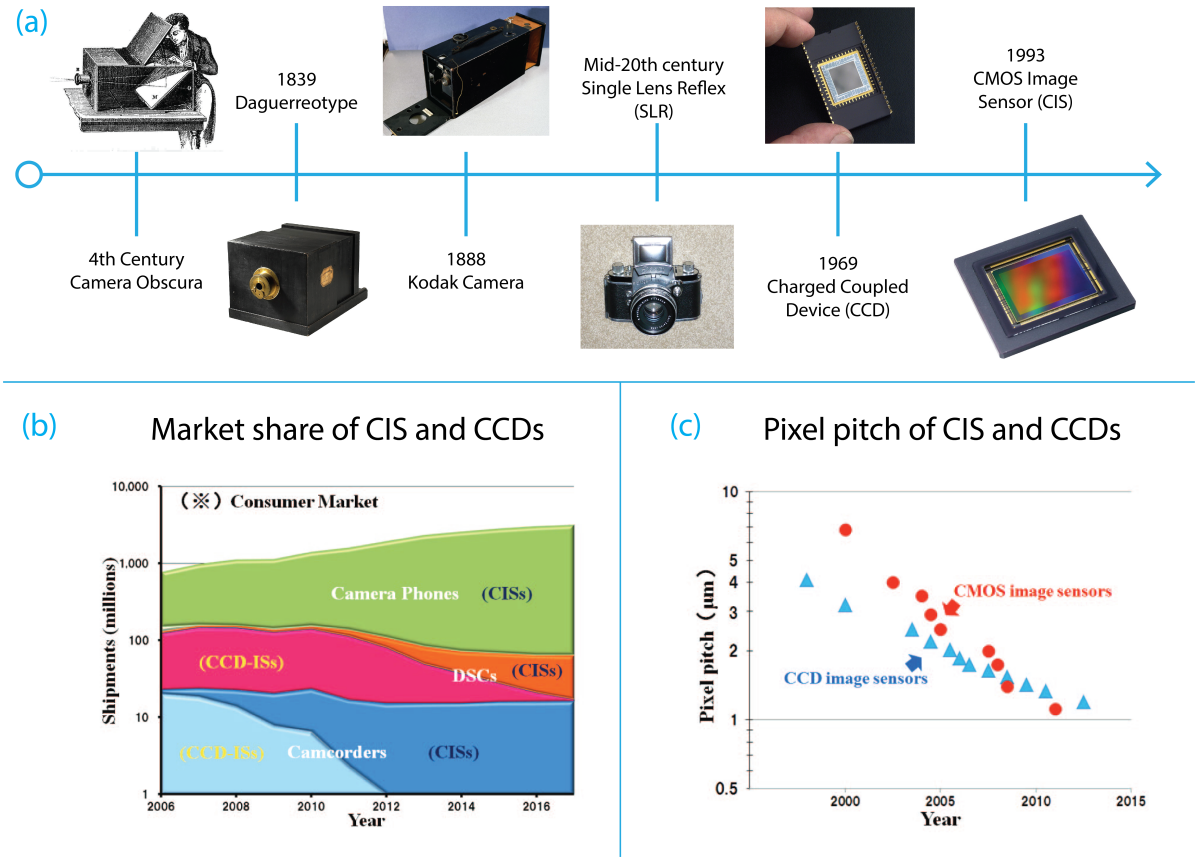


Figure 2.1: (a) Timeline of developments in image sensing technologies - Camera Obscura [39], Daguerreotype [40], Kodak Camera [41], Single Lens Reflex (SLR) [42], Charged Coupled Device (CCD) [43] and the CMOS Image Sensor (CIS) [44]. (b) Market share as CIS and CCDs for different commercial applications by shipment. [35] (c) Scaling of CIS and CCDs by pixel pitch. [35]

2.2. The CMOS Active Pixel Sensor

CMOS Active Pixel Sensors (APS) have revolutionized digital imaging with their ability to integrate light-sensing elements and signal processing circuitry on a single chip. This integrated operation has allowed for a wide-range of applications - smartphone cameras, computer vision in autonomous vehicles, astrophotography, medical imaging, etc. Before delving into the theoretical models and performance parameters required to evaluate a CMOS APS, discussed in the next chapter, it is important to explore the key components of CMOS image sensors and the advancements that have propelled their widespread adoption.

At the heart of every CMOS image sensor is the ”pixel array”, composed of millions of individual ”pixels”. Each pixel consists of a photodiode, which converts incoming light into electrical charges, and several transistors that control charge accumulation, reset, and readout operations required to obtain the signal. CMOS APS architectures are of two architectures - the 3T (three-transistor) and the more recent 4T (four-transistor) design. The 3T architecture includes a reset transistor, source follower, and row select transistor in the readout circuit, while the 4T architecture includes an additional transfer gate [45]. Differences between the 3T and 4T architecture will be discussed in the next chapter. Fig. 2.2 shows the schematic of a standard CMOS image sensor floorplan as well as a picture of a commercial CMOS sensor (the SONY IMX675) [46].

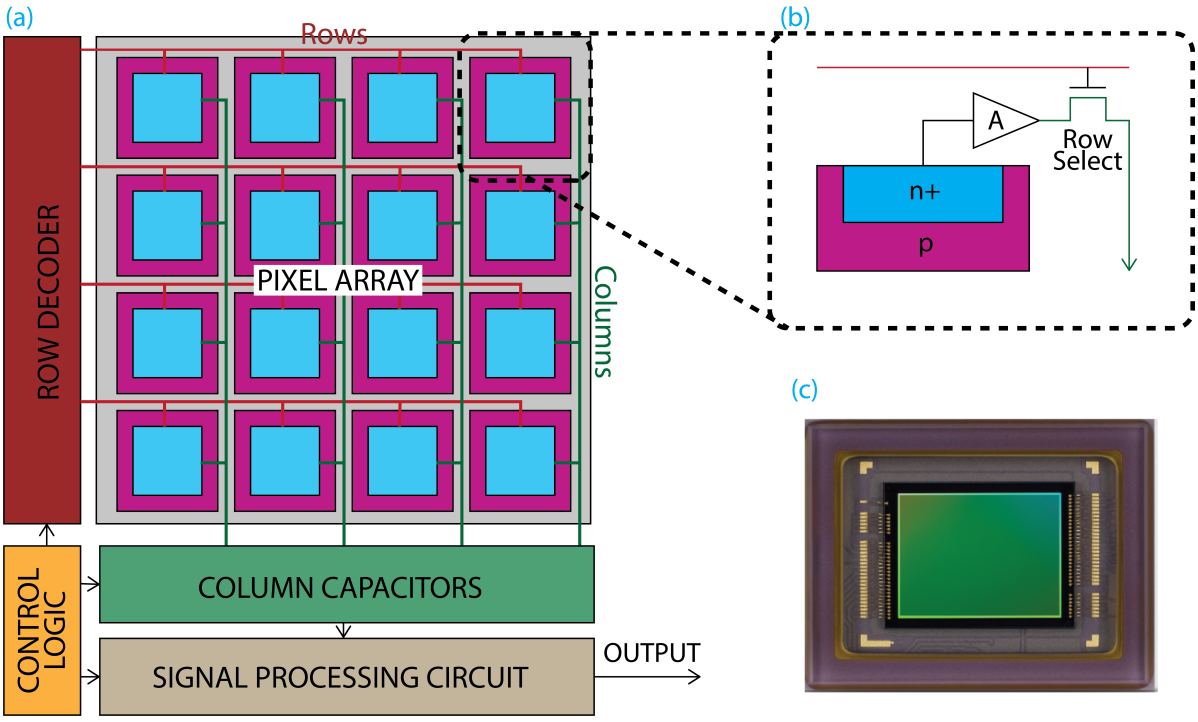


Figure 2.2: (a) The typical CMOS Active Pixel Sensor. (b) The single CMOS Active Pixel with the photodiode, source follower and row select transistor. (c) The Sony IMX 675 [46]

The photodiode is typically made of silicon and is responsible for the photon-to-electron conversion process. When photons strike the photodiode, they generate electron-hole pairs. The electrons are collected in a potential well, while the holes are swept away to the substrate. The number of electrons collected is proportional to the intensity of the incident light, forming the basis of the image signal.

The biggest advantage of CMOS Image sensors has been the ability to integrate the readout electronics and the light-sensitive pixel array onto a single die on an IC. Surrounding the pixel array are various supporting circuits that enable the sensor to function. These include:

1. Row and column decoders: Used to select specific rows and columns of pixels for readout.

2. Analog-to-Digital Converters (ADCs): Convert the analog signal from each pixel into a digital value. Modern CMOS sensors often employ column-parallel ADCs for faster readout speeds. [47]
3. Timing and control circuits: These manage the sequence of operations within the sensor, including exposure timing, readout, and reset cycles.
4. Signal processing circuits: These manage On-chip processing, including functions such as noise reduction, colour interpolation, and basic image enhancement.
5. Interface circuits: These manage communication between the sensor and the host device. They may not be present on the same die.

The integration of on-chip image signal processors (ISPs) has been another significant advancement. These processors can perform complex operations such as multi-frame noise reduction, high dynamic range (HDR) processing, and advanced colour correction, all within the sensor package. This integration has enabled improvements in image quality while reducing the processing load on the host device [48].

Colour imaging in CMOS sensors typically employs a colour filter array (CFA) placed over the pixel array. The most common arrangement is the Bayer pattern, which uses a repeating 2x2 grid of red, green, and blue filters. However, recent developments have explored alternative CFA patterns and the use of additional color filters to improve color accuracy and light sensitivity [49].

Another significant advancement in CMOS sensor technology has been the development of backside-illuminated (BSI) sensors, first introduced by Sony in 2009 [50]. In traditional front-side illuminated sensors, light must pass through the metal wiring layers before reaching the photodiode. BSI sensors flip this arrangement, allowing light to strike the photodiode directly without obstruction. This results in improved light sensitivity and reduced noise, particularly in low-light conditions [51]. Fig. 2.3(a-b) shows the schematics of a front-side and back-side illuminated sensor.

A recent innovation has been the introduction of stacked sensor designs. In these sensors, the photodiode layer is separated from the readout circuitry, with the two layers connected by through-silicon vias (TSVs). This architecture allows for more complex circuitry without compromising the light-gathering area of the pixels. It has enabled features such as high-speed readout, on-chip memory, and advanced noise-reduction techniques [52]. Fig. 2.3(c) shows the schematics of a 2-layer-stacked BSI sensor.

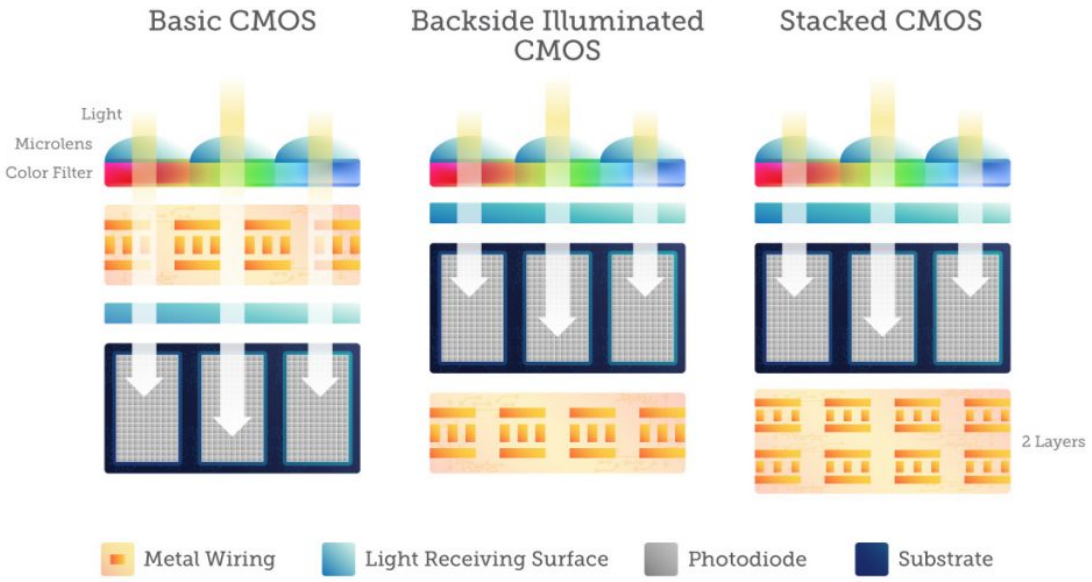


Figure 2.3: Schematic of (a) Front-side illuminated, (b) Back-side illuminated, and (c) stacked image sensors [53].

The pixel size in CMOS sensors has steadily decreased over the years, driven by the demand for higher resolution in compact devices. However, this miniaturization presents challenges in terms of light sensitivity and noise performance. To address these issues, manufacturers have developed various light-concentrating structures, such as micro-lenses and light guides, to improve the light collection efficiency of small pixels [54].

As CMOS sensor technology continues to advance, we are seeing the emergence of new capabilities such as global shutter operation, which eliminates rolling shutter artifacts, and time-of-flight sensors for 3D imaging. Currently, there is great research interest in extending the spectral sensitivity of CMOS sensors beyond the visible range into the near-infrared and even the short-wave infrared regions [55, 56, 57], however integrated visible+NIR/SWIR CMOS Image sensors has remained a challenge.

3

Fundamental Theory

In the previous chapter, the history and structure of a CMOS image sensor were briefly introduced to provide an understanding of the most widespread image-sensing technology currently used, which is also the basis of this project. As this project aims to develop a CMOS-compatible Visible+NIR/SWIR wideband image sensor, it would be interesting to get an insight into the state-of-the-art NIR / SWIR Image sensor developments, their specific CMOS-integration incapabilities as well as the techniques to develop a CMOS-compatible wideband image sensor. However, it is important to have a firm understanding of the fundamental theory involved in creating an image sensor, which would later simplify the discussions of the state-of-the-art NIR/SWIR technologies.

3.1. Introduction to Semiconductors

Image sensors and photovoltaic cells are similar in the way that both produce electric current due to the photovoltaic effect. Edmond Becquerel, a french scientist discovered the effect in 1839 where a voltage or electric current was observed when certain materials were exposed to light or radiant energy. These certain materials, now called *semiconductors*, form the backbone of all electronics and sensing applications in the modern world. A CMOS Image Sensor detects incident light by generating free charges as the photon energy excites electrons to higher energy states, after which the resultant current is current is measured. Thus, the operation of CMOS image sensors depends on the electrical properties, such as the bandgap and conductivity, of these semiconductors for the generation and transportation of free charges. The *bandgap* is an intrinsic property of a semiconductor, while the conductivity of a semiconductor can be manipulated by the process of introducing impurities into the crystal lattice, called *doping*.

3.1.1. Introduction to semiconductors and bandgap

In any bulk substance, only discrete values for electron energies are allowed due to the Pauli exclusion principle. However, these discrete quantized energy levels split into two discrete energy levels due to the interaction and perturbation of atoms in close proximity to each other, a process known as *Band-splitting* (Fig. 3.1(a). The two energy levels are called the *valence band* (lower energy band where all the electrons are bound), and the *conduction band* (higher energy band where electrons can freely move) while the forbidden gap is known as the *bandgap* - E_G expressed as:

$$E_G = E_C - E_V \tag{3.1}$$

where E_G is the bandgap energy, E_C is the energy at the bottom of the conduction band, and E_V is the energy at the top of the valence band (expressed in eV)

The average energy of electrons in a material E_f, known as the *fermi-energy* or *fermi-level*, is determined by the Fermi-dirac distribution and is expressed for intrinsic semiconductors as:

$$E_f = \frac{E_C + E_V}{2} \tag{3.2}$$

where E_f is the fermi energy (expressed in eV).

At absolute zero temperature, semiconductors behave like insulators, with all electrons in the valence band and an empty conduction band. However, as the temperature increases, some electrons gain enough energy to jump across the bandgap from the valence band to the conduction band. Once in the conduction band, these electrons can move freely and contribute to electrical conduction. This jump can also take place by the photovoltaic effect, when an incident photon provides sufficient energy to an electron to move to the conduction band. The excited electron then leaves behind an empty *hole*, which behaves like the positive charged equivalent of an electron - thus the absorption of incident photon generates *hole-electron pairs* in the semiconductor. Fig. 3.1(b) shows the generation of hole-electron pairs due to the photovoltaic effect. This is not possible for insulators with too large bandgaps or conductors, where most charges are mobile without the need of incident light (Fig. 3.1(c)).

The photon energy required to generate hole-electron pairs in a semiconductor is expressed as:

$$E_{photon} = \frac{hc}{\lambda} > E_G \tag{3.3}$$

where E_{photon} is the photon energy (expressed in eV), and λ is the wavelength of light.

The bandgap of silicon is 1.12 eV, capable of detecting wavelengths up to 1100 nm [58]. As photovoltaic effect is fundamentally related to the bandgap of the semiconductor, a material property, detecting of longer wavelengths - particularly in NIR/SWIR requires the selection of materials with smaller bandgaps.

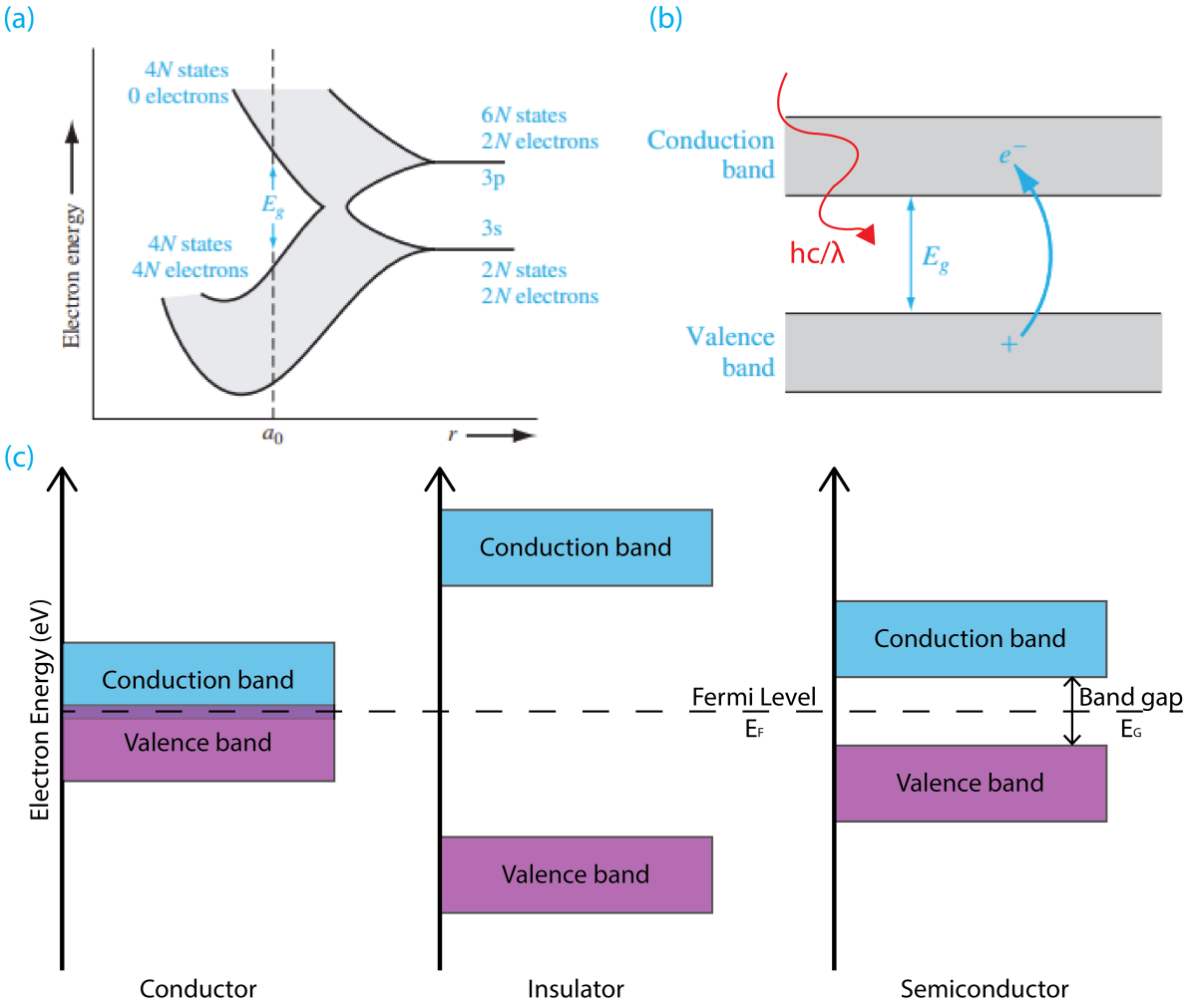


Figure 3.1: (a) Band-splitting in silicon [58], (b) Generation of hole-electron pair by absorption of incident photon, (c) Band diagrams of conductors, insulators and semiconductors

3.1.2. Direct-Indirect Semiconductors

In the previous section, the relation between the wavelength of the incident light and the bandgap of the semiconductor was introduced. However, this relation holds only for materials in which the momentum of electron (given by *k-values*) is the same in both the valence and conduction band, known as direct bandgap semiconductors. This is not the case for indirect bandgap materials, where for an electron to move from the valence band to the conduction band requires the assistance of a *phonon* - quanta of lattice vibration to conserve momentum. Fig. 3.2 shows the E-k diagrams of direct and indirect semiconductors.

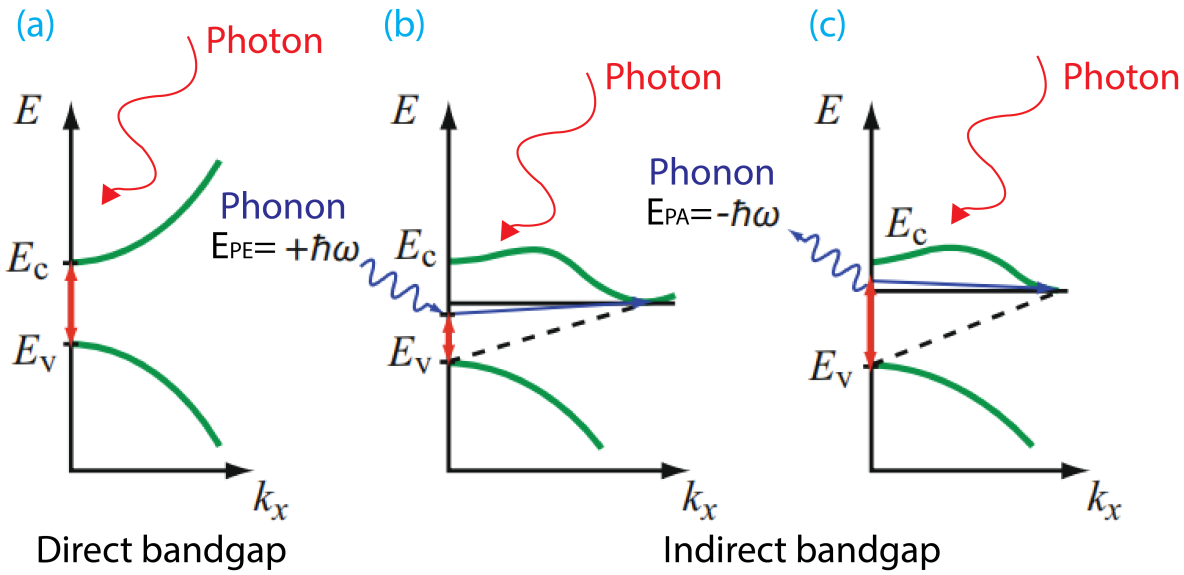


Figure 3.2: E-k diagrams [59] of (a) Direct bandgap semiconductor, (b) Indirect bandgap semiconductor with phonon absorption (c) Indirect bandgap semiconductor with phonon emission

While the details of phonon mechanics is not of importance in this project (for full details, refer Böer [59]), a key takeaway from this is that indirect bandgap semiconductors require more energy for electron-hole pair generation as compared to direct bandgap semiconductors - thus results in significantly larger wafer thickness requirements for indirect bandgap semiconductors while direct bandgap materials can be only a few micron thick. On the other hand, direct bandgap materials are challenging to integrate in CMOS electronics due to lattice mismatch, thermal expansion coefficient differences leading to stresses and polarity issues [60, 61]. This particular result will play an important role in this project in the performance analysis of NIR/SWIR layers.

Material	Direct/ Indirect Bandgap	Bandgap (eV)	Cutoff-Wavelength (nm)
Silicon	Indirect	1.12	1100
Germanium	Indirect	0.6	1840
Gallium Phosphide	Indirect	2.24	551
Gallium-Arsenide	Direct	1.42	
Indium-Phosphide	Direct	1.35	915
Lead-Selenide	Direct	0.27	4570
Aluminium-nitride	Direct	6	205
Indium-Gallium-Arsenide	Direct	0.75	1650
Mercury-Cadmium-Telleride [1]	Direct	0.09-1.6	800-1400
Lead-sulphide [2]	Direct/ Indirect	0.42 (bulk) / 0.37-2.5 (QD)	
Cadmium-Telluride	Direct	1.49	832
Indium-Antimonide	Direct	0.225	5500

Table 3.1: Bandgap and cut-off wavelengths for common direct and indirect semiconductors used in image sensors and photovoltaic cells

[1] $Hg_xCd_{1-x}Te$ bandgap depends on Hg-Cd ratio

[2] Bulk PbS is a direct bandgap material but nanoparticle PbS used in Quantum-Dot (QD) Image sensors behaves as an indirect bandgap material with a dependence on the size of the quantum-dot

3.1.3. Absorption Coefficient

While the bandgap of a material determines the cut-off wavelength of light beyond which no electron-hole pairs are generated in the substrate, this relation does not provide complete information on the thickness of the material required to completely absorb wavelengths shorter than the cut-off wavelength. To obtain this information, a term known as *absorption coefficient* of a material - α is first introduced, quantifying how much light is absorbed per unit distance as it travels through the material. The absorption coefficient is a function of the wavelength of incident light and the refractive index of the material (which is dependent on the direct or indirect bandgap of the material).

The absorption coefficient is given by the following equation [62]:

$$\alpha_{abs} = \frac{4\pi k}{\lambda} \tag{3.4}$$

where α_{abs} is the absorption coefficient (in cm^{-1}), k is the extinction coefficient (complex part of the complex refraction index of the material). Fig. 3.3 provides the graph of absorption coefficients of different semiconductors.

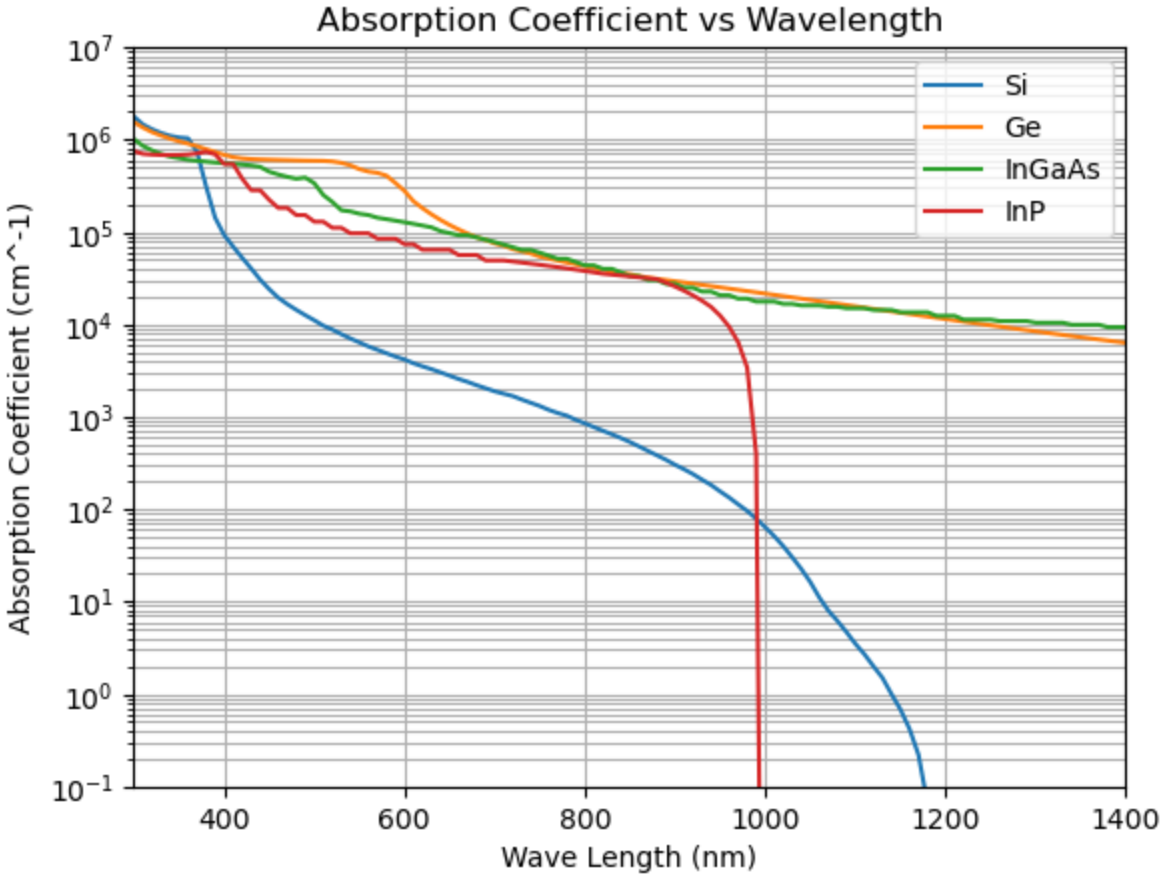


Figure 3.3: Absorption coefficients of Si, Ge, InGaAs and InP calculated from the refractive indexes [63, 64]

3.1.4. Beer-Lambert Law

Using the absorption coefficient of the material, it is now possible to calculate the attenuation of light as it passes through an absorbing medium using the Beer-Lambert Law, which in turn provides information on the thickness of the semiconductor substrates required while designing the image sensor to detect the desired wavelength of light.

The Beer-Lambert Law is mathematically expressed as [62]:

$$F(x) = F_0 e^{-\alpha_{abs} x} \tag{3.5}$$

where $F(x)$ is the photon-flux at a distance x from the surface of the semiconductor in (photons/(cm^2·s)), F_0 is the incident photon flux (photons/(cm^2·s)), α_{abs} is the absorption coefficient of the material (cm^{-1}) and x is the distance from the surface of the material (cm).

From equation 3.5 it can be observed that the photon flux intensity decreases exponentially with the thickness of the material. For silicon with an absorption coefficient of 1000 cm^{-1} for wavelengths of 780 nm and 50 cm^{-1} for wavelengths of 1000 nm, the thickness of the silicon epitaxial layer required to absorb 63% of the incident photons is 10 μm for 780 nm and 200 μm at 1000 nm (Fig. 3.4.

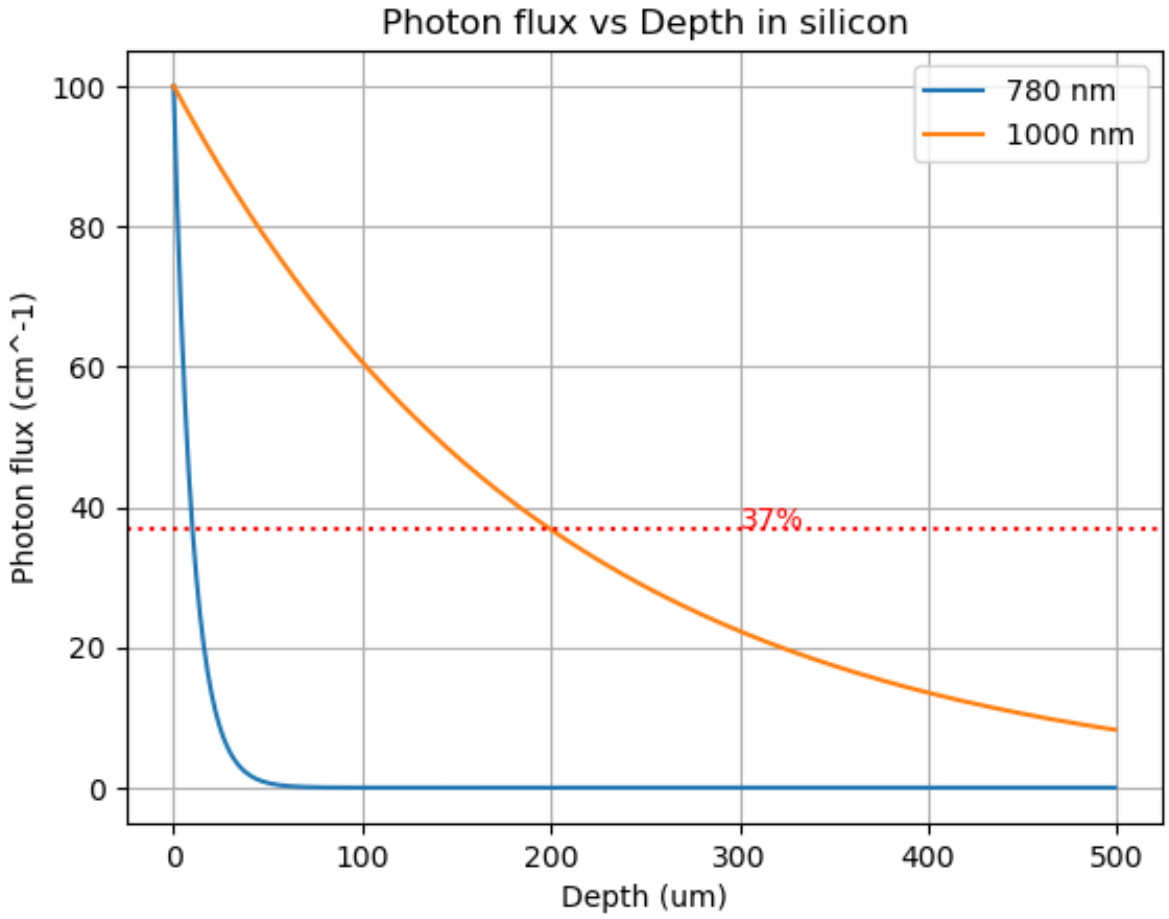


Figure 3.4: Photon flux vs depth in silicon substrate for 780 nm and 1000 nm wavelength light

3.1.5. Doping concentration and the PN junction diode

In the previous sections, the effect of the bandgap of the semiconductor on the absorption of light at different wavelengths and the subsequent generation of electron-hole pairs was seen. While this is one important factor in the design of an image sensor, it is equally important to transport these charges through a circuit either through a charge concentration gradient or under the influence of an electric field. Without this, the generated electron-hole pairs will recombine, and no signal is obtained while also contributing to noise in the form of dark current.

The electrical properties of an intrinsic (pure) semiconductor are altered by the process of introducing impurities in the crystal lattice, called *doping*. All semiconductors belong to Group-IV of the periodic table with 4 valence electrons; thus, replacing some semiconductor atoms with Group-III (3 valence electrons) or Group-V elements (5 valence electrons) makes the semiconductor p- or n-type with excess holes or electrons respectively. These excess holes or electrons can freely move through the p- or

n-doped semiconductor, respectively, and are called *majority carriers*. In a p- or n-doped substrate, electrons and holes then become the *minority carriers* respectively, resulting in a minority current flowing through the substrate.

The concentration of dopants introduced is known as the *doping concentration*. The doping concentration for n-type (N_D) and p-type (N_P) are then used to calculate the following electrical properties of the semiconductor:

Charge Concentration

1. Electron concentration in n-type: $n \approx N_D$ (expressed in cm^{-3})
2. Hole concentration in p-type: $p \approx N_A$ (expressed in cm^{-3})

For an intrinsic semiconductor, the concentration of electrons in the conduction band is equal to the concentration of holes in the valence band, i.e., $n_i = p_i$. As the terms are equal, only n_i is referred to as intrinsic carrier concentration. For silicon, the intrinsic carrier concentration n_i at room temperature is 1.5 $\times 10^{10}$.

For a doped semiconductor, the concentration of carriers is given by the Mass-Action law:

$$n \cdot p = n_i^2 \tag{3.6}$$

PN Junction

Just a single type of doped semiconductor is insufficient for image-sensing applications. The fundamental building block of an image sensor is the *pn-junction*. A pn-junction is formed at the interface of the p-typed doped region and a n-type doped region. At this interface, the excess electrons from the n-doped region diffuse into the p-type region, while the holes from the p-doped region diffuse into the n-doped region. These diffused charges then recombine with the present majority charges in the region, resulting in no more free carriers at the interface. Thus a *depletion region* is formed.

Doped semiconductors are neutral in the absence of any external influence. However, the diffusion of charges at the interface leaves behind fixed charges with give rise to an electric field. The diffusion of charges continues, and the depletion region widens until the electric field inside the depletion region is sufficiently large to block any further diffusion of charges, and thus an equilibrium is formed. The region outside the depletion region remains neutrally charged, and no electric field is present in this region, thus the region is called *quasi-neutral region* (the neutrality assumption can only be made at bulk scale in thermal equilibrium) [65] (Fig. 3.5(a)).

Fig. 3.5(b) shows the band diagram of the pn-junction. In the absence of externally applied voltage or induced current, the Fermi level across the junction is constant. The depletion region is completely devoid of any mobile charges, and the presence of the electric field serves as a barrier to any movement of charges across the pn junction. This barrier, in the form of a *Built-in potential*, occurs only at the pn-junction interface and cannot be measured using a voltmeter.

The built-in voltage (V_{bi}) of a pn-junction is given by:

$$V_{bi} = \frac{k_B T}{q} ln(\frac{N_a N_d}{n_i^2}) \tag{3.7}$$

where V_{bi} is the built-in voltage (expressed in V), and N_a and N_d are the doping concentrations of the p-type and n-type regions of the junction.

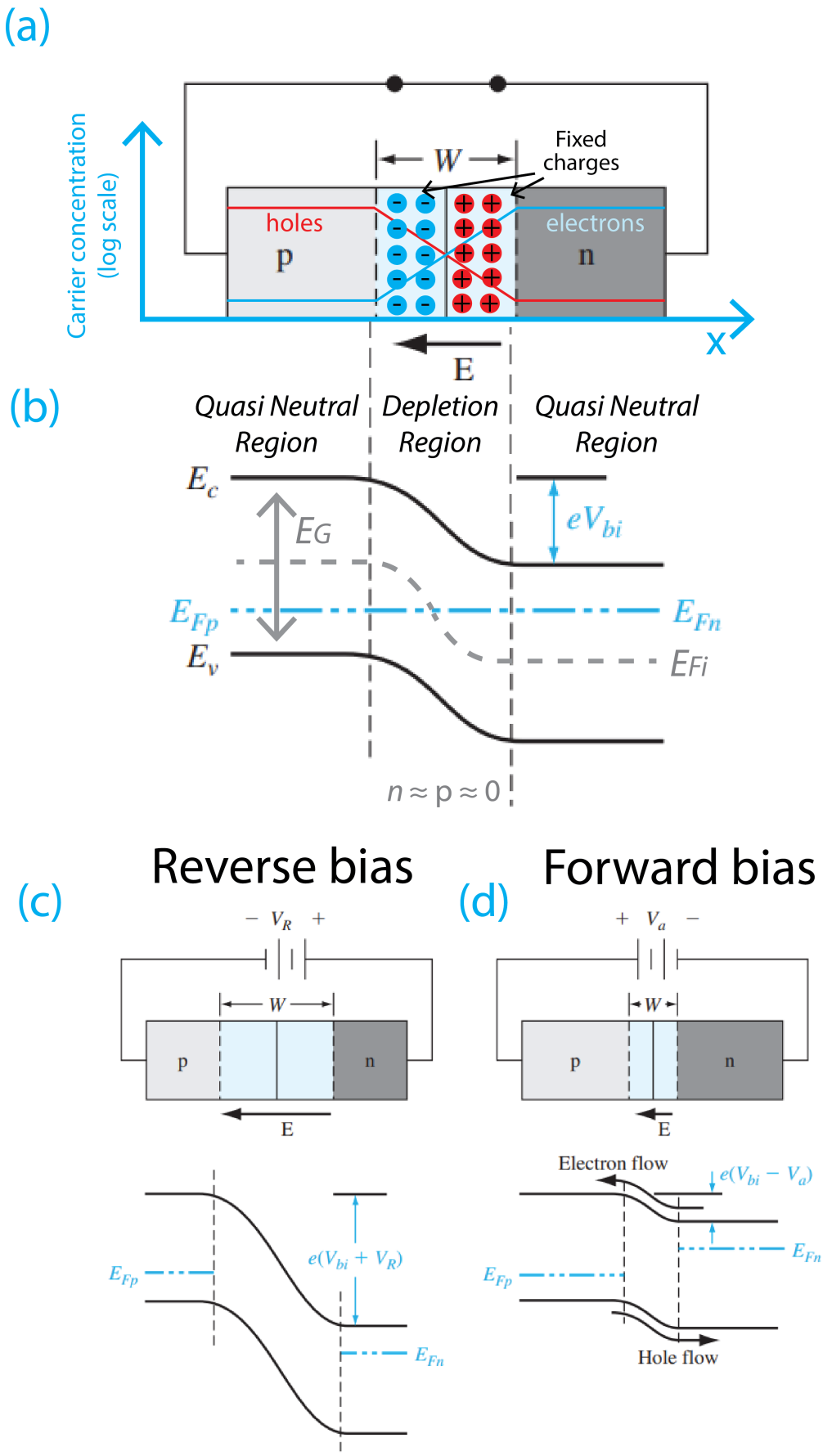


Figure 3.5: (a) The pn-junction in the absence of external bias (b) Band diagram of pn-junction in the absence of external bias (c) Reverse biased pn-junction and its band diagram, (d) Forward biased pn-junction and its band diagram [58].

Biasing, Width of Depletion Region and Junction Capacitance

When an external voltage is applied to the pn-junction, the pn junction is *biased*. The pn-junction is *forward biased* when the positive voltage is applied to the p-doped material and the negative voltage to the n-doped material. Similarly, the pn junction is *reverse biased* when the negative voltage is applied to the p-doped material and the positive voltage is applied to the n-doped material. When the pn-junction is biased, the Fermi level is no longer equal in the p-doped and n-doped regions. Fig 3.5 (c-d) shows the pn-junction in reverse and forward-biased conditions.

In the forward-biased condition, the electric field inside the depletion region is opposite to the external electric field. This results in the shrinking of the depletion region. At sufficiently large applied voltage, charged carriers can move across the depletion region, and a forward current is set up.

The situation is reversed for the reverse-biased condition. The depletion region electric field is in the same direction as the applied electric field, and the depletion region width increases. No charges can move across the depletion in this condition, and no current is set up. When the reverse bias voltage is sufficiently high, the electric field inside the junction is so high that an avalanche of charges is triggered, which causes the junction to break down. As the pn-junction allows for the current to pass through only in one direction, it also also referred to as a *diode*. pn-junction diodes specifically made sensitive for photon detection are referred to as *photodiodes*.

The depletion region width in the n-type of a homogeneously doped pn-junction is given by:

$$x_n = \sqrt{\frac{2\varepsilon_0\varepsilon_r(V_{bi} - V_a)}{q}\frac{N_a}{N_d}\frac{1}{N_a + N_d}} \tag{3.8}$$

where x_n is the depletion region width in n-type, V_a is the external applied voltage, V_{bi} is the built-in voltage, ε_r is the relative permittivity and N_a and N_d are the doping concentrations.

Similarly, the depletion region width in the p-type of a homogeneously doped pn-junction is given by:

$$x_p = \sqrt{\frac{2\varepsilon_0\varepsilon_r(V_{bi} - V_a)}{q}\frac{N_d}{N_a}\frac{1}{N_a + N_d}} \tag{3.9}$$

where x_p is the depletion region width in p-type, V_a is the external applied voltage, V_{bi} is the built-in voltage, ε_r is the relative permittivity and N_a and N_d are the doping concentrations

Combining equation 3.8 and 3.9, the total width of the depletion region in a pn-junction is calculated as:

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_0\varepsilon_r(V_{bi} - V_a)}{q}\frac{N_d + N_a}{N_a N_d}} \tag{3.10}$$

where W is the total width of the depletion region, V_a is the external applied voltage, V_{bi} is the built-in voltage, ε_r is the relative permittivity and N_a and N_d are the doping concentrations

The depletion region behaves as a capacitor in that the depletion regions (also referred to as *space-charge regions* at the p-doped and n-doped regions behave as two oppositely charged plates through which no free charges can cross. The junction capacitance of a homogeneously doped pn-junction is given by:

$$C' = \sqrt{\frac{q\varepsilon_0\varepsilon_r N_a N_d}{2(V_{bi} - V_a)(N_a + N_d)}} \tag{3.11}$$

where C' is the junction capacitance, V_a is the external applied voltage, V_{bi} is the built-in voltage, ε_r is the relative permittivity and N_a and N_d are the doping concentrations.

The detailed derivation of all the pn-junction equations can be found in Neamen [58].

3.1.6. Poisson Equation, Electric Field and Potential across the pn junction

In the previous section, it was mentioned that an electric field is formed across the depletion region due to the diffusion of majority charges. to calculate the electric field in the the depletion region, the Poisson's equation is used.

The term $\varepsilon_0\varepsilon_r$ can be expressed as a single term, defined as the permittivity of the semiconductor ε_s

$$\varepsilon_s = \varepsilon_0\varepsilon_r \tag{3.12}$$

The Poisson's equation for one-dimensional analysis is given by:

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{dE(x)}{dx} = -\frac{\rho(x)}{\varepsilon_s} \tag{3.13}$$

where $\Phi(x)$ is the electric potential, $E(x)$ is the electric field, $\rho(x)$ is the volume charge density, ε_s is the permittivity of the semiconductor and x is the distance from the interface at the pn junction

Integrating equation 3.13, and setting the boundary condition $E = 0$ in the quasi-neutral regions, the electric field in the depletion region is:

$$E = \begin{cases} \frac{-qN_a}{\varepsilon_s}(x + x_p), & -x_p \leq x \leq 0 \\ \frac{-qN_d}{\varepsilon_s}(x_n - x) & 0 \leq x \leq x_n \end{cases} \tag{3.14}$$

where E is the electric field, ε_s is the permittivity of the semiconductor, and x_n, x_p are the thickness of the depletion region in the n- and p-doped regions of the pn junction, respectively.

The electric field in the depletion region is continuous, i.e., at x=0. Substituting in equation 3.14 gives:

$$N_a x_p = N_d x_n \tag{3.15}$$

Similarly, the potential can be found by integrating substituting equation 3.14 and setting the boundary condition as zero potential at $x = -x_p$ and taking the potential as a continuous function:

$$\Phi(x) = \frac{qN_d}{\varepsilon_s}(x_n \cdot -\frac{x^2}{2} + \frac{qN_a}{\varepsilon_s}x_p^2, (0 \leq x \leq x_n) \tag{3.16}$$

From equation 3.16, we can then express the built-in potential as:

$$V_{bi} = |\Phi(x = x_n)| = \frac{q}{2\varepsilon_s}(N_d x_n^2 + N_a x_p^2) \tag{3.17}$$

Fig. 3.6 shows the volume charge density, electric field and potential across a pn-junction diode.

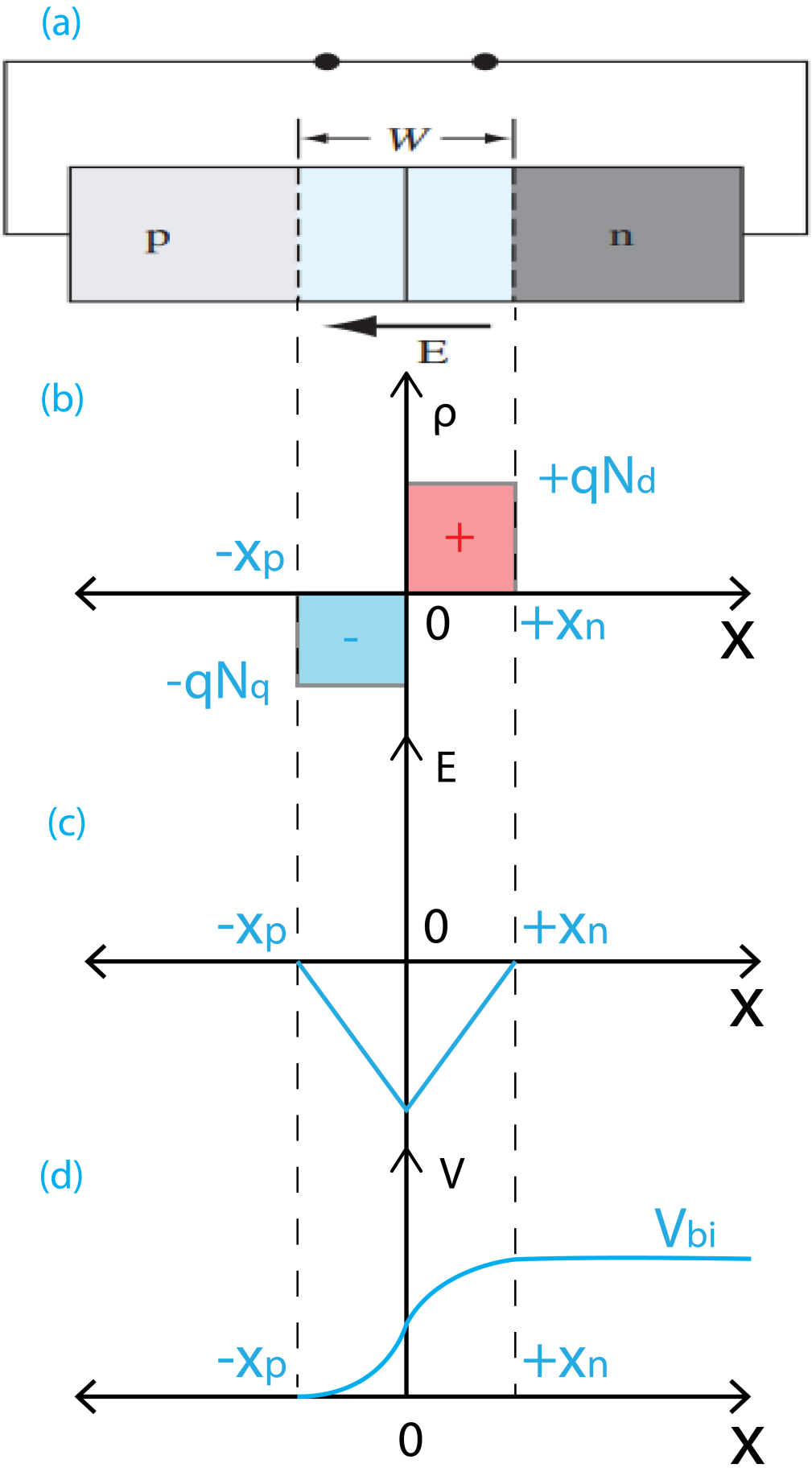


Figure 3.6: (a) The pn-junction in the absence of external bias (b) Volume Charge Density (c) Electric Field, (d) Potential [58].

3.1.7. Diffusion and Drift

The previous section discussed the pn-junction diode at the static condition without any external influence. In an image sensor, the charges generated by the incident light, i.e., by photogeneration, have to be efficiently transported to the contacts of the image sensor while avoiding recombination to reduce signal loss.

There are two primary mechanisms that govern the movement of charge carriers in semiconductors: diffusion and drift (Fig. 3.7).

1. Diffusion: This process occurs due to the concentration gradient of charge carriers. Electrons and holes move from regions of high concentration to regions of low concentration. In a pn-junction, a gradient of the minority carriers exists in the quasi-neutral region as the minority carriers generated close to the depletion are swept by the electric field. This results in the diffusion of minority carriers towards the depletion region.

   The electron and hole diffusion current is given by:

   $$J_{n-diff} = qD_n \frac{dn}{dx} \tag{3.18}$$

   $$J_{p-diff} = -qD_n \frac{dp}{dx} \tag{3.19}$$

   where J_{n-diff} and J_{p-diff} are the electron and hole current densities, D_n and D_p are the diffusion constants of electrons and holes respectively, n and p is the electron and hole densities (cm^{-3})

2. Drift: This process occurs due to the electric field present in the depletion region. Charge carriers move in response to this electric field: electrons are pulled towards the positive potential, and holes are pulled towards the negative potential.

   The drift velocity of the holes and electrons under the influence of an external electric field is:

   $$v_{drift} = \frac{q\tau_m E}{m} = \mu E \tag{3.20}$$

   where v_{drift} is the charge drift velocity, τ_m is the mean free time between collisions (also referred to relaxation time), E is the applied electric field, m is the effective mass of the carrier and μ is knows as the mobility.

   The effective electron and hole mass in silicon m_n and m_p are 0.26 m_0 and 0.39 m_0 respectively.

   Using equation 3.20, the drift current can be found:

   $$J_{n-drift} = -qnv_{drift} = qn\mu_n E \tag{3.21}$$

   $$J_{p-drift} = qpv_{drift} = qp\mu_p E \tag{3.22}$$

   $$\tag{3.23}$$

   where $J_{n-drift}$ and $J_{p-drift}$ are the electron and hole drift current densities, μ_n and μ_p are the electron and hole mobilities.

   The relation between the rate of diffusion and charge mobility is given by the *Einstein relationship*:

   $$\frac{D_{n,p}}{\mu_{n,p}} = \frac{k_B T}{q} \tag{3.24}$$

   The diffusion length $L_{n,p}$ is related to the carrier lifetimes $\tau_{n,p}$ as:

   $$L_{n,p} = \sqrt{D_{n,p}\tau_{n,p}} \tag{3.25}$$

   where $L_{n,p}$ is the diffusion length, $D_{n,p}$ arethe diffusion coefficients, $\tau_{n,p}$ is the charge carrier lifetime

   Because of the larger effective mass of the holes and shorter relaxation time leading to increased recombination, both the diffusion and drift current of holes is lower than electrons for equally doped p- and n-doped semiconductors. Thus an important design consideration in image sensors is the minimization of reduction in the path length of holes.

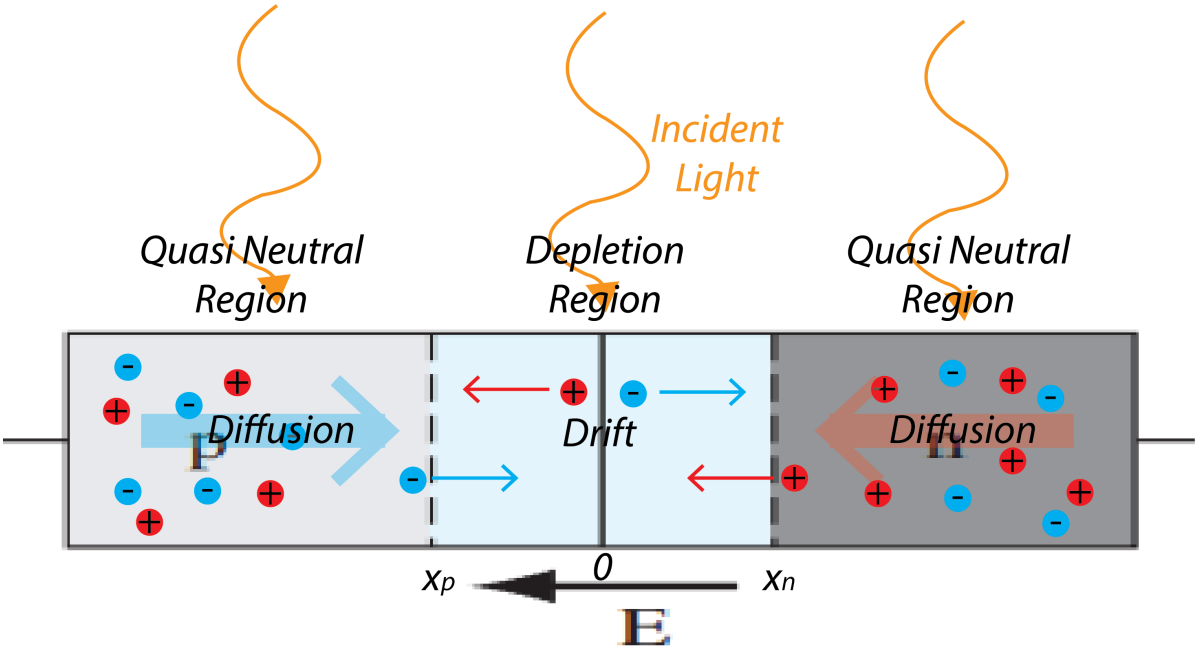


Figure 3.7: The diffusion and drift currents of photogenerated electrons and holes in a pn-junction

3.2. Generation and Recombination

The total diffusion and drift current in an image sensor is the sum of charge carriers generated through photon absorption as well as the charge carriers lost due to the recombination of an electron-hole pair.

Generation

Charge carriers can be generated through two processes: optical generation and thermal generation

1. Optical Generation: As discussed in Section 3.1.1, pptical generation occurs when photons with energy greater than or equal to the bandgap energy E_G of the semiconductor are absorbed, exciting electrons from the valence band to the conduction band and creating electron-hole pairs.

   The rate of optical generation depends on the intensity and wavelength of the incident light, as well as the absorption coefficient α_{abs} of the semiconductor material. Using the beer-lambert law (equation 3.5), the generation rate of hole-electron pairs in the semiconductor layer can then be calculated as:

   $$G(x) = -\frac{dF(x)}{dx} = \alpha_{abs} F_0 e^{-\alpha_{abs} x} \tag{3.26}$$

   where $G(x)$ is the generation rate of electron-hole pairs (photons/(cm^3·s)), F_0 is the incident photon flux, and x is the depth of the semiconductor material.

2. Thermal generation: This process occurs due to thermal energy that excites electrons from the valence band to the conduction band, creating electron-hole pairs. This process is temperature-dependent, with higher temperatures increasing the rate of thermal generation. As this generation generates a current in the absence of light - known as *dark current*, thermal generation is a source of noise and must be minimized to obtain high signal-to-noise ratios (SNR) in the image sensor. Thus high sensitivity image sensors, such as single photon detector are hence operated at cryogenic temperatures [66, 67]

Recombination

Recombination is the process by which electrons and holes recombine, annihilating each other and releasing energy. Recombination can occur through several mechanisms: radiative recombination, non-radiative recombination, and Auger recombination.

1. Radiative Recombination: Radiative recombination occurs when an electron recombines with a hole, and the energy released is emitted as a photon. This process is significant in direct bandgap semiconductors like gallium arsenide (GaAs), where the momentum of the electrons and holes is conserved. Radiative recombination is the basis for light emission in LEDs and laser diodes. However, in indirect bandgap semiconductors like silicon, radiative recombination is less efficient and less significant.
2. Non-Radiative Recombination: Non-radiative recombination occurs when the energy released during recombination is transferred to other carriers or lattice vibrations (phonons) instead of being emitted as light. The primary non-radiative recombination mechanisms are Shockley-Read-Hall (SRH) recombination, surface recombination and Augur recombination.
   (a) Shockley-Read-Hall (SRH) Recombination: SRH recombination mechanism involves recombination through energy states between the conduction and valence band, known as *traps*, where electrons and holes can be captured and later re-emitted. These traps are formed due to imperfections in the semiconductor crystal lattice or impurity atoms. These traps can either be *shallow*, being a few k_BT from band edges or *deep*, being close to the mid bandgap. These traps can also either be *acceptor-type*, that are positively charged in the absence of electrons, or *donor-type*, that are negatively charged when occupied by electrons. Fig. 3.8(a) shows the SRH recombination mechanism.

      The SRH recombination rate (U) is given by [58]:

$$U = \frac{pn - n_i^2}{\tau_n(p + n_i e^{\frac{E_i - E_t}{k_B T}}) + \tau_p(n + n_i e^{\frac{E_t - E_i}{k_B T}})} \tag{3.27}$$

      where U is the SRH recombination rate, n and p are the charge carrier densities of holes and electrons (cm^{-3}), τ_e and τ_p are the minority carrier lifetime of electrons and holes, n_i is the intrinsic carrier concentration of the semiconductor, E_t is the trap energy (eV) and E_i is the intrinsic fermi energy. Derivation of the SRH recombination rate can be found in Neuman [58].
   (b) Surface Recombination: This process occurs at the surface of the semiconductor where the crystal lattice is interrupted, creating a high density of recombination centers. The effect of surface recombination is amplified when the depletion region of the pn-junction is at the surface boundary. This is one of the major source of dark current in the 3T architecture of CMOS image sensors, later resolved in the 4T architecture.
   (c) Auger Recombination: Auger recombination involves a three-charge-carrier interaction where the energy released during electron-hole recombination is transferred to a third carrier (another electron or hole), which is then excited to a higher energy state. This process is significant in heavily doped semiconductors and at high carrier injection levels [68].

      The Auger recombination rate for holes and electrons is given as [58]:

$$R_n = C_n n^2 p \tag{3.28}$$

$$R_p = C_p p^2 n \tag{3.29}$$

$$R_{Auger} = C_n n^2 p + C_p p^2 n \tag{3.30}$$

      where R_{Auger} is the net Auger recombination rate, R_n and R_p are the Auger recombination rates for electrons and holes, C_n and C_p are the Auger coefficient for electrons and holes, n and p are the charge carrier densities of holes and electrons (cm^{-3}). Fig. 3.8(b) shows the Auger recombination mechanism.

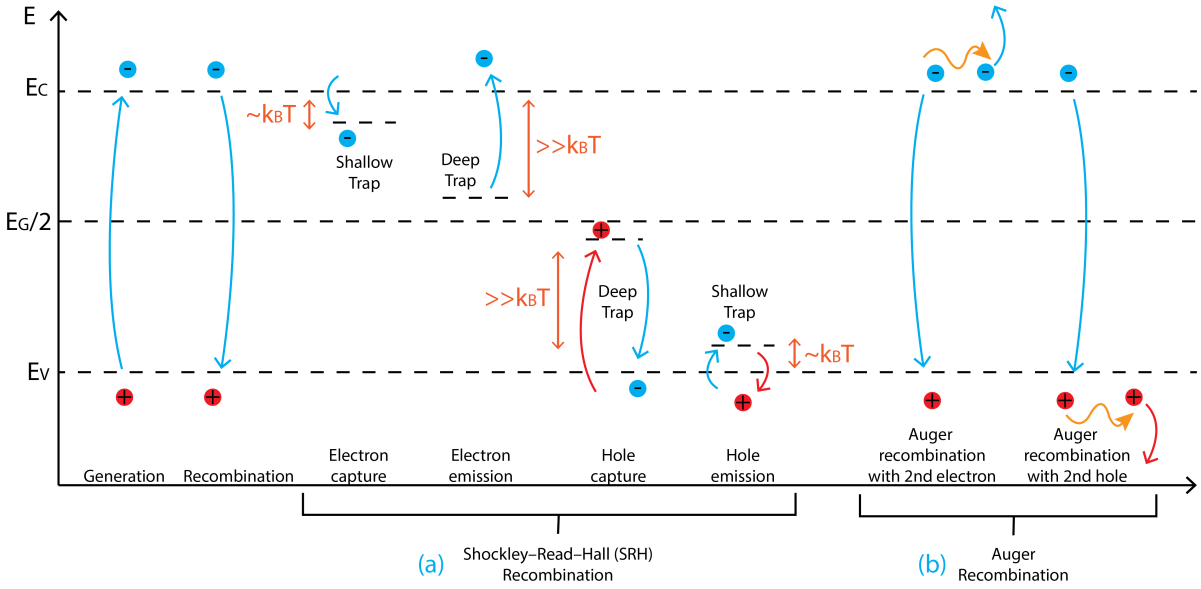


Figure 3.8: (a) The Shockley-Read-Hall (SRH) Recombination mechanism with shallow and deep traps, (b) The Auger recombination [58]

3.3. The Ambipolar Transport Equation / Continuity Equation

By combining the generation and recombination rates in a pn-junction with the diffusion and drift currents, the complete *Ambipolar Transport Equation* (also known as the continuity equation) of the pn-junction is obtained.

The Ambipolar Transport Equation for holes and electrons in a pn-junction is given by:

$$\frac{\partial n(x)}{\partial t} = n(x)\mu_n \frac{\partial E(x)}{\partial x} + E(x)\mu_n \frac{\partial n(x)}{\partial x} + D_n \frac{\partial^2 n(x)}{\partial x^2} + (G_n(x) - R_n(x)) \tag{3.31}$$

$$\frac{\partial p(x)}{\partial t} = p(x)\mu_p \frac{\partial E(x)}{\partial x} + E(x)\mu_p \frac{\partial p(x)}{\partial x} + D_p \frac{\partial^2 p(x)}{\partial x^2} + (G_p(x) - R_p(x)) \tag{3.32}$$

Where E is the electric field, $D_{n,p}$ are the diffusion coefficients, $\mu_{n,p}$ is the carrier mobility, $G_{n,p}$ is the net generation rate, $R_{n,p}$ is the net recombination rate, and t is time.

3.4. Spectral Response and Quantum Efficiency

In the design and optimization of image sensors, particularly when extending capabilities into the NIR and SWIR regions, three parameters stand out as critically important: spectral response, quantum efficiency, and dark current. These parameters will be used as the figure of merit (FoM) for evaluating image sensor designs.

3.4.1. Spectral Response

Spectral response is a fundamental characteristic of image sensors that describes how the sensor's output signal varies with the wavelength of incident light. It is a comprehensive measure that reflects the sensor's ability to detect light across different parts of the electromagnetic spectrum and is the key specification impacting colour reproduction accuracy, low-light performance, and the sensor's suitability for specific applications.

Spectral response is quantified as the ratio of the sensor's electrical output to the optical input power at each wavelength. It is expressed in units of A/W (amperes per watt) or V/J (volts per joule), depending on whether the sensor's output is measured as a current or a voltage.

The mathematical expression for spectral response can be derived using the ambipolar transport equation (equation 3.31) and solving for diffusion and drift currents using different boundary conditions. The typical pn-junction photodiode structure used to derive the spectral response is shown in Fig. 3.9

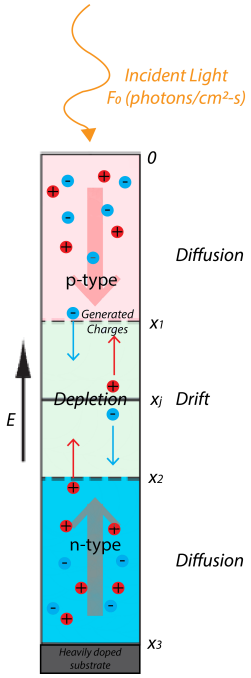


Figure 3.9: Typical vertically-oriented photodiode

As seen in Fig. 3.9, the typical pn-junction photodiode is vertically oriented. PN-junction photodiode are fabricated using thin and high-purity epitaxial layers to two reasons: (a) As seen in section 3.1.4, the percentage of photon flux absorbed by the photodiode depends on the depth of semiconductor layers, thus photodiodes are required to be fabricated very deep for the detection of longer wavelengths of light, and (b) from section 3.2, the recombination rate increases with defect density, thus in order to reduce the recombination rate, high-purity layers are fabricated sequentially. The substrate of a photodiode is generally a heavily doped wafer that acts as a carrier sink.

From equation 3.26, the current density in the depletion region is

$$J_{dep} = qF_0(e^{-\alpha_{abs}x_1} - e^{-\alpha_{abs}x_2})[\mathrm{A\,cm^{-2}}] \tag{3.33}$$

and using equation 3.18 and the ambipolar equation 3.31, current densities in the upper p-type and lower n-type quasi-neutral regions are:

$$J_{n,p-type}(x = x_1) = -q\frac{F_0}{\alpha_{abs}x_1}[1 - (1 + \alpha_{abs}x_1)e^{-\alpha_{abs}x_1}][\mathrm{A\,cm^{-2}}] \tag{3.34}$$

$$J_{p,n-type}(x = x_2) = \frac{qF_0(e^{-\alpha_{abs}x_3} - e^{-\alpha_{abs}x2} + \alpha_{abs}e^{-\alpha_{abs}x2}(x_3 - x_2))}{\alpha_{abs}(x_3 - x_2)}[\mathrm{A\,cm^{-2}}] \tag{3.35}$$

Combining equations 3.33, 3.34 and 3.35, we get the total current density, i.e. the *spectral resposne* of the photodiode $J_{ph_totaal} = J_{dep} + J_{n,p-type} + J_{p,n-type}$ as:

$$J_{ph_totaal} = \frac{qF_0(e^{-\alpha_{abs}x_1}(x_3 - x_2) + x_1e^{-\alpha_{abs}x_2} - x_1e^{-\alpha_{abs}x_3} + x_2 - x_3}{x_1\alpha_{abs}(x_2 - x_3)}[\mathrm{A\,cm^{-2}}] \tag{3.36}$$

It can be seen through equations 3.33, 3.34, 3.35 that the diffusion current is approximately a factor α_{abs} greater than the depletion current. Thus, in order to maximize the spectral response of the image sensor, the depletion region has to be maximized. However, this comes with a trade-off of increased noise, which will be discussed in section 3.5.

3.4.2. Quantum Efficiency

Quantum Efficiency (QE) is a pivotal parameter in image sensor performance, directly quantifying the sensor's ability to convert incident photons into collected electrons. It is a more fundamental measure than spectral response, as it describes the sensor's effectiveness in terms of photon-to-electron conversion, independent of the energy of the incident photons.

It is defined as the ratio of the number of charge carriers generated to the number of incident photons at a specific wavelength:

$$QE = \frac{\text{Number of electrons generated}}{\text{Number of incident photons}} \tag{3.37}$$

$$QE = \frac{J_{ph-total}}{qF_0} \text{electrons/photons} \tag{3.38}$$

QE is critical in determining the sensor's sensitivity, especially in low-light conditions, and plays a significant role in determining the signal-to-noise ratio. In the pursuit of extending sensor capabilities into NIR and SWIR regions, maximizing quantum efficiency across a broad spectrum becomes a central challenge. QE calculations take into consideration all image sensor parameters, such as material properties such as bandgap and absorption coefficient, surface passivation to reduce recombination, anti-reflective-coatings to reduce reflections and photodiode physical structure determining how much light is incident on the light-sensitive area.

QE calculations can be of two types:

1. Internal QE: Charge generation and recombinations within the substrate are considered but surface reflection and absorptions are excluded. Internal QE can be 100%.
2. External QE: Takes into consideration all reflection and absorption losses. External QE is always lower than 100%.

Fig. 3.10 shows a schematic of factors affecting the internal and external QE of an image sensor.

Fill factor

For the calculation of the external QE, one of the important parameters to be considered is the *fill factor*, which is defined as the ratio of light-sensitive pixel area to the total area of the image sensor.

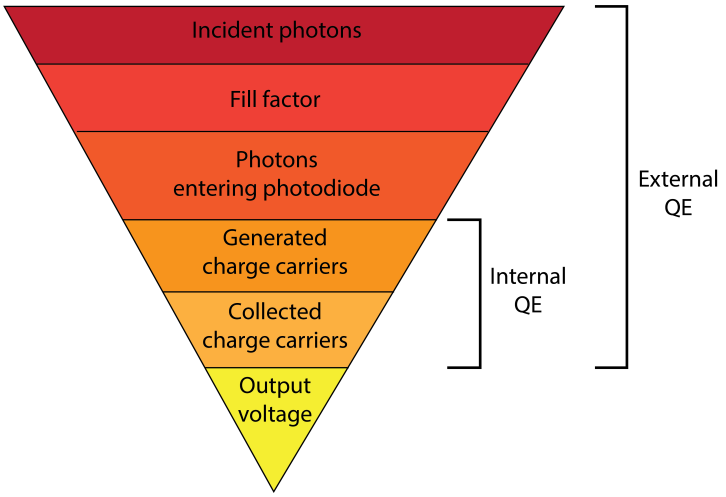


Figure 3.10: Factors affecting the internal and external QE of an image sensor

3.5. Dark Current

The third important parameter to taken into consideration during the design of an image sensor is the *Dark Current*. While the spectral response and QE provide vital information of the sensor's sensitivity,

the dark current sets the lower limit of the sensor's detectable signal and significantly impacts the sensor's dynamic range, especially in low-light imaging conditions.

Dark current is defined as either the current density measured at the output in the absence of light. It represents the rate at which electrons are thermally generated, the capture and emissions occurring at the crystal defects and the noise in the sensor's readout circuitry. As discussed in section 3.2, the main causes of dark current are the thermal generation in depletion regions, surface generation, diffusion in the quasi-neutral regions after the light is turned off, trap-assisted tunneling and impact ionization.

The thermally generated dark current for the photodiode shown in Fig. 3.9 can be calculated from the ambipolar equation 3.31 by setting the generation rate equal to 0 in the quasi neutral region and from the SRH equation 3.27 for the depletion region:

Dark current in the depletion region is:

$$J_{dark(depletion} = \frac{n_i}{2\tau_0}(x_2 - x_1)[\mathrm{A\,cm^{-2}}] \tag{3.39}$$

$$\tag{3.40}$$

while the dark current in the quasi neutral region are:

$$J_{n,dark(p-type)} = qD_n \frac{n_i^2}{x_1 N_A}[\mathrm{A\,cm^{-2}}] \tag{3.41}$$

$$J_{p,dark(n-type)} = qB_p \frac{n_i^2}{(x_3 - x_2)N_D}[\mathrm{A\,cm^{-2}}] \tag{3.42}$$

$$\tag{3.43}$$

where $D_{n,p}$ are the diffusion constants, n_i is the intrinsic carrier concentration, τ_0 is the minority carrier lifetime (assuming $\tau_n = \tau_p = \tau_0$ in the SRH equation), and $N_{A,D}$ are the doping concentrations.

The total dark current is the sum: $J_{dark(depletion} + J_{n,dark(p-type)} + J_{p,dark(n-type)}$

$$J_{dark-current} = \frac{n_i}{2\tau_0}(x_2 - x_1) + qD_n \frac{n_i^2}{x_1 N_A} + qB_p \frac{n_i^2}{(x_3 - x_2)N_D}[\mathrm{A\,cm^{-2}}] \tag{3.44}$$

It can be seen through equations 3.39 and 3.41 that the dark current in the depletion region scales by a factor of n_i and by a factor of n_i^2 in the quasi-neutral region. As n_i (of order 10^{10} in silicon) is significantly smaller than N_A/N_D (of order > 10^{14}), the dark current contribution by the depletion region is several orders of magnitude greater than the quasi-neutral region. As both the spectral response as well as the dark current increase with an increase in depletion width, a trade-off must be made on the size of the depletion depending on the application.

The impact of dark current on the image sensor performance are:

1. Noise: Dark current contributes to shot noise (discussed in the next section), which follows a Poisson distribution.
2. Dynamic Range: Dark current sets the lower limit of detectable signal, effectively reducing the sensor's dynamic range, especially for long exposure times.
3. Fixed Pattern Noise: Non-uniformity in dark current across the pixel array contributes to fixed pattern noise, which can be particularly noticeable in low-light images.
4. Hot pixels: Pixels with abnormally high dark current, often due to defects, appear as bright spots in dark images.
5. Dark Signal Non-Uniformity (DSNU): Variations in dark current across the sensor array, contributing to spatial noise in images.

The following steps can be taken to reduce the dark current:

1. Cooling: As seen in section 3.2, thermal generation is temperature dependent, thus high-performance scientific image sensors are operated at cryogenic temperatures [66, 67].

2. Optimized doping profiles: From the dark-current equation 3.44, the depletion region is the largest contributor to the dark current. Thus, carefully designed doping profiles can minimize depletion region volume while maintaining good quantum efficiency.
3. Surface passivation: Deposition of high-quality dielectric layers over the surface and greatly reduce surface generations.
4. Buried photodiode structures: Preventing surface contact of the depletion region also reduces the impact of surface generation. This design consideration is the key feature of the 4T pixel architecture over the older 3T pixel (detailed explanation provided in later sections).
5. High-purity of epitaxial layers: As dark current is caused by the presence of crystal defects, the high purity of semiconductors and ensuring proper lattice match between the layers reduces the dark current. This is one of the major challenges in the design of NIR/SWIR sensors [19, 69].
6. Correlated Double Sampling (CDS) The effect of dark current on image quality can be mitigated by subtracting the image signal from a reference signal for each pixel when the noise is the *correlated* for both signals. This has been one of the major advancements in CMOS image sensor architectures (the 4T pixel architecture, discussed in Section 3.7).
7. Dark current compensation: Dark current can be compensated in the analog read-out circuits depending on the characterized behaviour of the image sensor.

Dark current in the NIR/SWIR sensors becomes additionally challenging to resolve due to the following factors:

1. Narrower bandgap materials: Materials like germanium or III-V semiconductors used for SWIR detection have higher intrinsic carrier concentrations, leading to increased thermal generation [70].
2. Thicker depletion regions: As discussed by the Beer-Lambert law (section 3.1.4), NIR/SWIR photons require thicker substrates to be efficiently absorbed, which increase the volume of thermal generation.
3. New defect types: Alternative materials may introduce additional defects or generation centers not typically seen in silicon.
4. Heterojunction structures: The interfaces in heterostructure devices - consisting of multiple layers of different materials (e.g., InGaAs/InP sensors) can introduce additional generation sites at the interface.
5. Strain effects: Strain introduced to modify bandgap properties can also affect dark current characteristics [20, 71].

3.6. Noise in Image Sensors

While spectral response and quantum efficiency are important parameters that provide information on the sensitivity of the image sensor, the noise in the image sensor must be taken into consideration to design high performance image sensors. Noise in image sensors refers to unwanted variations in the output signal that are not related to the actual light intensity being measured. Noise affects the sensor's dynamic range, signal-to-noise ratio (SNR), and ultimately determines the lowest light levels that can be accurately detected, thus understanding and minimizing noise is critical for achieving high image quality, particularly in the longer wavelength spectrum.

The types of noises present in an image sensor are:

1. Shot Noise: Also known as Poisson noise, it the the noise that originates at random arrival of discrete particles, either photons or electrons. The shot noise follows a poison distribution and the standard deviation of shot noise is given by:

$$\sigma_N = \sqrt{N} \implies \text{Signal-to-Noise ratio (SNR)} = \frac{N}{\sqrt{N}} = \sqrt{N} \tag{3.45}$$

where N is the number of photons or electrons.

2. Thermal Noise: Thermal noise is caused by the random thermal motion of charge carriers in resistive components of the sensor, in particular, the transistors used for the read-out circuit. The thermal noise is represented by:
$$\sigma_{thermal} = k_B T R \Delta f \tag{3.46}$$
where T is the absolute temperature, R is the resistance, and Δf is the bandwidth
3. Flicker noise: Flicker noise is associated with traps in the semiconductor material and interfaces. It is inversely proportional to frequency, being prominent in lower frequencies and thus is also called "1/f noise". The flicker noise varies with device geometry and fabrication process and can only be reduced in the analog readout circuit.
4. Fixed Pattern Noise: Fixed pattern noise is a spatial variation in pixel outputs under uniform illumination conditions. There are two types of Fixed Pattern noise:
   (a) Dark Signal Non-Uniformity (DSNU): Variation in dark current from pixel to pixel
   (b) Photo Response Non-Uniformity (PRNU): Variation in pixel responsivity to light

   While the fixed pattern noise is constant for a given sensor (with some temperature dependence), they are more noticeable at high signal levels (for PRNU).
5. Random Telegraph Signal (RTS) Noise: RTS noise is characterized by discrete fluctuations in pixel output between two or more distinct levels. It is caused by the trapping and de-trapping of charges due to the tunneling effect between the oxide layer to the substrate. While RTS noise has a $1/f^2$ dependence, multiple RTS noises have a combined effect similar to 1/f.

3.7. Pixel Architectures - 3T and 4T pixels

The final discussion on the background of image sensors is the read-out architecture used in CMOS image sensors. While this project does not include the read-circuit of the image sensor, it is important to understand the different architectures - their features, advantages and disadvantages as well as the sensor design requirements to ensure the proposed design can efficiently utilize the developments made in the CMOS image sensor architectures.

3.7.1. 3T Pixel architecture

The 3T (three-transistor) pixel architecture is one of the simplest and earliest designs in CMOS image sensors. It consists of three main transistors: a reset transistor, a source follower transistor, and a row-select transistor (Fig. 3.11(a)). The basic components and their functions are as follows:

1. Photodiode: The light-sensitive photodiode in the 3T architecture is a simple 2-layer pn-junction in which the generated charges are stored in the photodiode built-in capacitance.
2. Reset Transistor M_{RST}: This transistor is used to reset the photodiode to a known voltage level, typically the supply voltage (V_{DD}), before each integration period. The reset transistor ensures that the photodiode is cleared of any residual charge from the previous exposure.
3. Source Follower Transistor M_{SF}: This transistor buffers the voltage on the photodiode and provides a low-impedance output. It acts as a voltage follower, replicating the photodiode voltage at its source terminal.
4. Row Select Transistor M_{RS}: This transistor is used to connect the pixel output to the column readout line. It allows the selection of a specific row of pixels for readout during image acquisition.

Operation of the 3T Pixel

The operation of the 3T pixel can be divided into three phases: reset, integration, and readout, during which the signal and reference voltage are stored in two capacitors C_{SHS} and C_{SHR} respectively.

1. Reset Phase: During this phase, the reset transistor (M1) is turned on, connecting the photodiode to V_{DD}. This action resets the photodiode to a known voltage level. The reset transistor is then turned off, isolating the photodiode from the supply voltage. During this time, the reset voltage level is stored in C_{SHR}. This reset operation, however, introduces a thermal noise (KTC noise) known as "reset noise" into the photodiode, and the reset voltage fluctuates between multiple

frames. The reset noise introduced by the reset transistor in the photodiode can be calculated from the thermal noise equation 3.46 and is expressed as:

$$\sigma_{thermal}^2 = \frac{k_B T}{C} \tag{3.47}$$

where $\sigma_{thermal}$ is the thermal noise (in V), T is the absolute temperature and C is the photodiode capacitance.

2. Integration Phase: During the integration phase, the photodiode is exposed to light, and incident photons generate electron-hole pairs. The electrons are collected in the photodiode, causing its voltage to drop proportionally to the amount of light received. The integration time is the duration for which the photodiode collects charge.
3. Readout Phase: During the readout phase, the row select transistor (M_{RS}) is turned on, connecting the source follower transistor (M_{SF}) to the column readout line. The source follower transistor buffers the photodiode voltage and the output voltage is stored in the capacitor C_{SHS}.

In the readout circuitry, the difference between the values stored in C_{SHS} and C_{SHR}, initially an analog signal is converted to a digital value. However, an important detail to be noted is that the signal value is stored first, followed by the reset value. This means that the signal value stored in C_{SHS} and the reset value stored in C_{SHR} are of two different frames, resulting in the thermal noise captured in C_{SHS} and C_{SHR} are NOT of the same frame and this operation is not correlated double sampling (CDS). This leads to the *addition of noise* as the KTC noise in the output signal increases by a factor of $\sqrt{2}$ along with the presence of fixed pattern noise. This can be seen in Fig. 3.11(c).

While the 3T pixel is simple with low fabrication costs and small pixel sizes, it has two major disadvantages: (a) high reset noise and fixed pattern noise (FPN) due to the lack of correlated double sampling, and (b) the need for the metal contacts to be present on the light-sensitive region itself, lowering the fill factor of the pixel. This resulted in the architecture falling out of favour in CMOS image sensors. Thus, this architecture must be avoided in the design of the NIR/SWIR-enhanced CMOS image sensor.

3.7.2. 4T Pixel architecture

The 4T (four-transistor) pixel architecture is an enhancement over the 3T design, aimed at improving image quality and reducing noise. It includes an additional transistor, the transfer gate, (Fig. 3.11(b)), which provides several benefits. The main components of the 4T pixel architecture are:

1. Pinned-Photodiode (PPD): In the 4T architecture, the light-sensitive component is the PPD, which of a pn-junction along with a highly doped narrow epitaxy layer above the pn-junction. This layer provides three major benefits:
   (a) This epitaxy buries the depletion region and prevents it from being exposed to surface defects - leading to significantly lower dark current (Section 3.5).
   (b) Two pn-junctions are formed - one between the epitaxy and the buried layer and the other between the buried layer and the substrate. With the appropriate doping and applied bias voltage (pinning voltage), the two depletion regions can join and the buried layer is completely depleted (pinned). This allows for higher device sensitivity at shorter pixel depth.
   (c) The PPD does not participate in the signal readout, thus not requiring metal contacts to be present on the light-sensitive surface and allowing for very high fill-factors.
2. Floating Diffusion (FD): The FD collects charges from the PPD and is connected to the readout circuit to participate in the signal readout.
3. Transfer Gate M_{TX}: This additional transistor controls the transfer of charge from the photodiode to the floating diffusion node. It isolates the photodiode from the rest of the readout circuitry during integration.
4. Reset Transistor M_{RST}: Similar to the 3T pixel, this transistor resets the floating diffusion node to a known voltage level before charge transfer.
5. Source Follower Transistor M_{SF}: Again similar to the 3T pixel, this transistor buffers the voltage at the floating diffusion node.

6. Row Select Transistor M_{RS}: This transistor connects the pixel output to the column readout line during the readout phase.

Operation of the 3T Pixel

The operation of the 4T pixel architecture involves four phases: reset, integration, transfer, and readout.

1. Reset Phase: The reset transistor (M_{RST}) is turned on, resetting the floating diffusion (FD) node to a known voltage level. The photodiode is also reset to V_{DD} through the transfer gate (M_{TX}), which is initially on and then turned off to start the integration phase. Meanwhile, the reset value of the FD is stored in C_{SHR}.
2. Integration Phase: During this phase, the photodiode collects charge generated by incident photons. The transfer gate (M_{TX}) remains off, isolating the photodiode from the floating diffusion (FD) node.
3. Transfer Phase: After the integration period, the transfer gate (M_{TX}) is turned on, allowing the accumulated charge in the photodiode to transfer to the floating diffusion (FD) node. This transfer minimizes the thermal noise and dark current associated with the photodiode.
4. Readout Phase: The row select transistor (M4) is turned on, connecting the source follower transistor (M3) to the column readout line. The source follower buffers the voltage at the floating diffusion node and output is stored in C_{SHS}.

Identical to the 3T pixel, the readout circuitry, finds the difference between the values stored in C_{SHS} and C_{SHR} and converts it to a digital value. However, the storage of the signal value and reset value in C_{SHS} and C_{SHR} is reserved, with the reset value being read out first. The thermal noise captured in C_{SHS} and C_{SHR} is now the same and is subtracted away during readout. This operation is correlated double sampling (CDS), and this leads to a significant reduction in thermal and FPN noise reduction. This can be seen in Fig. 3.11(d).

Thus, most of the modern CMOS image sensors use the 4T pixel architecture, with the advantages of low thermal and FPN, low dark current, and very high fill factors. For any NIR/SWIR wideband CMOS image sensors designed must thus include a buried epitaxy layer to allow the use of 4T pixel architectures.

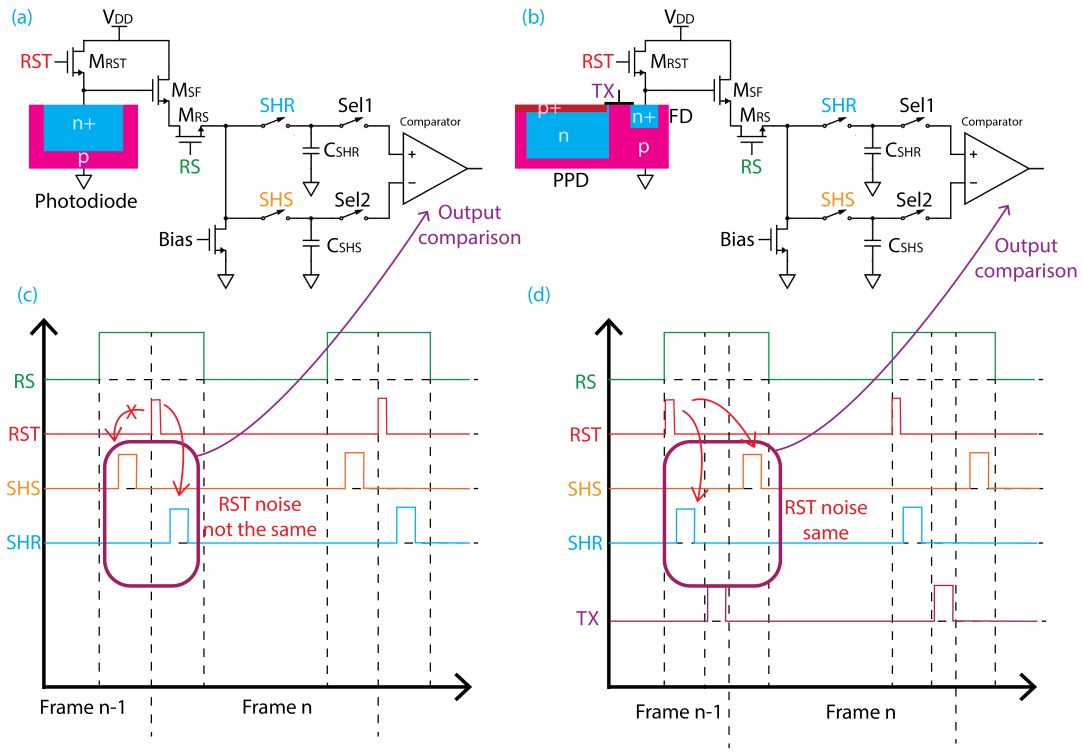


Figure 3.11: (a-b) Schematic of the (a) 3T pixel, (b) 4T pixel. (c-d) Timing diagram of (c) 3T pixel, (d) 4T pixel.

3.8. CMOS Fabrication Processes

This section outlines the key steps in CMOS fabrication, which are crucial in the process of designing a CMOS-compatible NIR/SWIR wideband image sensor. Fig. 3.12 and the list below give an overview of how one integrated circuit layer is created [72]. These steps are used for both the sensor and other integrated circuit components, like readout circuits. Therefore, any technique to enhance the sensor's spectrum must not disrupt these processes. Also, altering semiconductor fabrication flows at fabs for the NIR/SWIR sensor would require complex changes, leading to higher costs and lower reliability, making it economically impractical.

1. **Cleaning**: The wafer is first cleaned with nitric acid and demineralized water to remove any organic matter or dust, ensuring a clean surface for further processing.
2. **Primer treatment**: After cleaning, the wafer surface is hydrophilic. To improve the adhesion of the hydrophobic photoresist, the wafer is treated with HMDS, which increases its hydrophobicity.
3. **Photoresist coating**: Liquid photoresist is applied to the center of the wafer, which is then spun at high speeds (3500 to 9000 RPM) to spread the photoresist evenly. The coating thickness can range from 30 nm to 3 µm.
4. **Pre-exposure Soft-bake**: The wafer undergoes a soft-bake to evaporate the solvent from the photoresist. This step solidifies the photoresist layer, making it ready for the lithographic process.
5. **Alignment and exposure**: In this lithographic step, a mask or reticle is used to imprint a pattern onto the photoresist using light (photolithography). The resolution of the pattern depends on the wavelength of the light, as described by the Rayleigh criterion.
6. **Post-bake**: Following exposure, the wafer is baked again to harden the exposed parts of the photoresist. This improves adhesion to the wafer and prepares it for development.
7. **Development**: The wafer is placed in a developer solution that dissolves the unhardened photoresist. The remaining photoresist acts as a protective mask, defining the areas of the wafer to be etched.
8. **Etching**: The unprotected silicon oxide areas are etched away, exposing the underlying layers. Etching can be performed using either wet chemicals or dry plasma processes.
9. **Ion-implantation**: This step bombards the wafer with ions to dope the substrate, changing the electrical properties of specific areas and forming the IC's components. It is typically done at the deepest layer to create transistors and photodiodes.
10. **Photoresist removal**: Any remaining photoresist is dissolved and removed using a developer solution, leaving the etched pattern on the wafer.
11. **Metal deposition**: Metal is deposited to create electrical contacts, with aluminium used for low-layer contacts, tungsten for vias, and copper for interconnects. This step fills the etched silicon oxide pattern with the appropriate metal.
12. **Polishing**: The wafer surface is flattened using chemical-mechanical polishing (CMP) to ensure it is smooth and prepare it for the next layer of processing.

Wafer inspection and measurement are done at each step to ensure precision and functionality of the final semiconductor devices. As mentioned in Chapter 1, visible + NIR/SWIR wideband image sensors are ideal for this because they can easily distinguish between silicon and materials like metal interconnects in the SWIR spectrum.

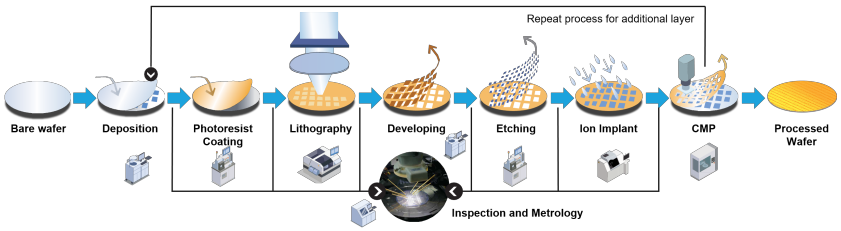


Figure 3.12: Fabrication process of the lowest layer in an integrated circuit. [73]

4

Review of current NIR/SWIR image sensors

With a complete understanding of the fundamental theory of image sensors in Chapter 3, this chapter introduces the different technologies currently used in a wide range of NIR/SWIR applications such as medical diagnostics, industrial process monitoring and surveillience. In section 3.1.2, it was seen that the primary limitation of silicon, used for CMOS image sensors, has been its large bandgap of 1.12 eV, and thus is unable to detect wavelengths beyond 1100 nm. For detection of longer wavelengths, materials with smaller bandgaps (listed in table 3.1) must be used. Fig. 4.1 shows graphically the different NIR/SWIR image sensing technologies and their respective wavelengths:

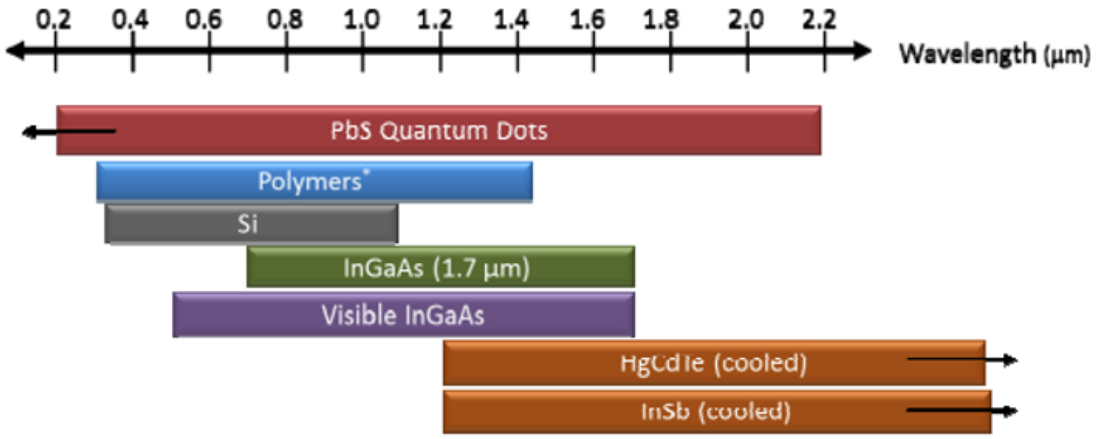


Figure 4.1: Wavelength range of different commonly used materials for NIR/SWIR imaging applications [74]

In visible+SWIR spectrum (up to 1400 nm), Indium-Gallium-Arsenide (InGaAs) have seen the most wide-spread applications, while interest in commercial applications PbS Colloidal Quantum Dot (CQD) image sensors has been on the rise - and thus will be discussed in this chapter. Additionally, despite the current lack of commercial applications, research on Ge-on-Si sensors will also be discussed in this chapter, as it is the backbone technology being explored as part of this project.

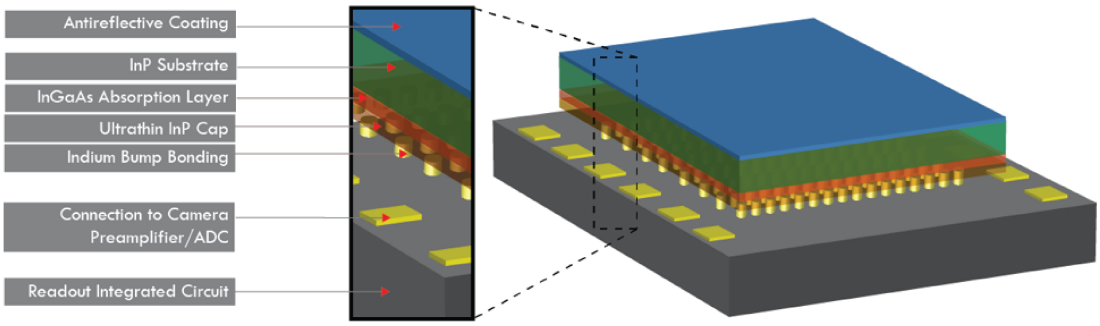
4.1. Indium-Gallium-Arsenide (InGaAs) Image sensors

Indium-Gallium-Arsenide (InGaAs) sensors are the type of image sensors with most commercial products available, such as Sony SenSWIR IMX990/991 [75], Teledyne DALSA's Linea SWIR [76], Xenics XSW cooled InGaAs sensor [77], Hamamatsu Photonics G1656X [78] as well as high-performance

scientific sensors such as the Teledyne FLIR A6260 [79].

These sensors utilize the unique properties of ternary alloy semiconductors where the bandgap of $In_xGa_{1-x}As$, formed by combining indium arsenide (InAs) and gallium arsenide (GaAs), can be tuned from 1.42 eV (x = 0, pure GaAs) up to 0.36 eV (x = 1, pure InAs) [80] - this allows for high efficiency detection from wavelengths from 900 nm up to 1700 nm, far beyond the capabilities of CMOS image sensors. Additionally, cooling InGaAs image sensors shifts the long-wavelength cutoff by 8 nm for every 10 °C, further allowing end-user tunability [81]. Most commercial used composition in InGaAs sensors is $In_{0.53}Ga_{0.47}As$ (bandgap of 0.75 eV, cut-off wavelength 1700 nm), as it is lattice matched with the Indium-Phosphide substrate and greatly reduces dark current.

(a)



(b)

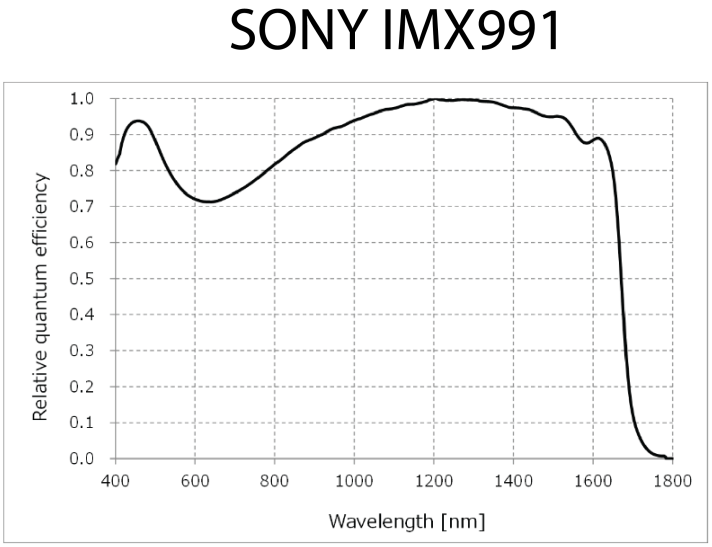


Figure 4.2: (a) Structure of a typical InGaAs sensor [82], (b) Quantum Efficiency of the Sony IMX991 [75] sensor in the visible+NIR/SWIR spectrum

The physical structure of InGaAs sensors, as seen in Fig. 4.2, comprises of:

- Substrate: The substrate, usually InP, provides the mechanical support for the sensor. InP is chosen because it has a lattice constant closely matched to InGaAs, reducing strain and defects during epitaxial growth.
- Buffer layer: A buffer layer is often grown on the substrate to smooth out any imperfections and provide a good surface for the subsequent layer

- InGaAs Absorption Layer: This is the active layer where photons are absorbed, generating electron-hole pairs. The composition of the InGaAs layer (the ratio of indium to gallium) determines the bandgap and thus the spectral sensitivity of the sensor.
- Cap Layer: A cap layer is grown on top of the InGaAs layer to protect it and to form the electrical contacts.
- 3D hydridization: InGaAs sensors are connected to the readout integrated circuit (ROIC) using 3D hybridization techniques such as 3D flip-chip indium bump bonding [83, 84]. Research is being carried out for the use of Cu-Cu hybridization bonding, such as in the Sony IMX991 [85].

InGaAs sensors have a number of advantages: (a) as evidenced by Fig. 4.2(b), InGaAs sensors have excellent performance in NIR/SWIR range, far exceeding any other comparable technology. (b) Additionally, while InGaAs sensors are generally cryogenically operated, they can also be operated at room temperatures significantly reducing system costs, and (c) InGaAs sensors have lower noise levels as compared to HgCdTe sensors [86].

However, InGaAs sensors can only be developed on InP substrates due to lattice-match constraints and thus require Indium or Copper bumps to attach to the silicon. This makes InGaAs sensors fundamentally incompatible with CMOS-technology, and the complex fabrication process of creating and aligning indium/copper bumps introduces several disadvantages that are challenging to resolve [24]:

1. Poor scalability: As InGaAs sensors cannot utilize the excellent scalability of CMOS processes, InGaAs sensors are very low resolutions as compared to CMOS image sensors (The Sony IMX991 has a resolution of 0.3 MP (megapixels) [75] as compared to commercially available phone image sensors exceeding resolutions of 200 MP)
2. Reliability Issues: 3D hybridization, such as the use of indium bumps or Cu-Cu bonding, can introduce mechanical stress during the bonding process. There is also often a mismatch in the thermal expansion coefficients between the indium bumps and the materials they connect. This mismatch can lead to further mechanical strain and potential failure of the sensor during temperature cycling.

   These mechanical and thermal stresses associated with 3D hybridization affect the long-term reliability of the sensor, particularly in harsh operating environments where temperature fluctuations and mechanical vibrations are common.
3. Complexity in ROIC design: Most modern circuit design tools are not equipped to design 3D integrated structures with multiple different substances, and thus ROIC design requires the development of new mathematical models - increasing development time and reducing reliability.
4. High Costs: As InGaAs sensors require specialized processes involving complex epitaxial growth techniques and expensive materials, the production of InGaAs sensors is prohibitively expensive. Additionally, the fabrication facilities can only be used for building InGaAs sensors, thus the very high initial setup costs further compounds the problem.

Due to these fundamental problems with InGaAs sensors, it is extremely challenging to use this technology to develop CMOS-compatible visible+NIR/SWIR image sensors.

4.2. Lead-sulphide (PbS) Colloidal Quantum Dot (QD) Image sensors

While InGaAs sensors currently continue to dominatee the NIR/SWIR imaging market, there is growing interest in an emerging technology of Lead sulfide (PbS) quantum dot (QD) based image sensors for NIR applications [20, 74, 87], with several start-ups developing commerical products such the STMicroelectronics [88], SWIR Vision Systems Acuros CQD [89], Quantum Solutions Q.Eye [90] and Emberion VS20 [91].

Quantum dots are semiconductor nanocrystals that exhibit size-tunable optical properties - with strong absorption occuring at certain photon energies, at the expense of reduced absorption at other energies [92]. This size-tunable optical properties works on the principle of quantum confinement - when the nanocrystal radius is much smaller than the Bohr radius of the exciton (a hole-electron within the crystal lattice) in the bulk material, the normally continuous energy bands (as seen in section 3.1.1 become

discrete, changing the bandgap of the material [92] (Fig. 4.3(a)). The Bohr Raddi of excitons in different semiconductors is listed in table 4.1.

Material	Exciton Bohr radius (nm)
CuCl	1
CdSe	6
PbS	20
InAs	34
PbSe	46
InSb	54

Table 4.1: The Bohr Raddi of excitons in different semiconductors

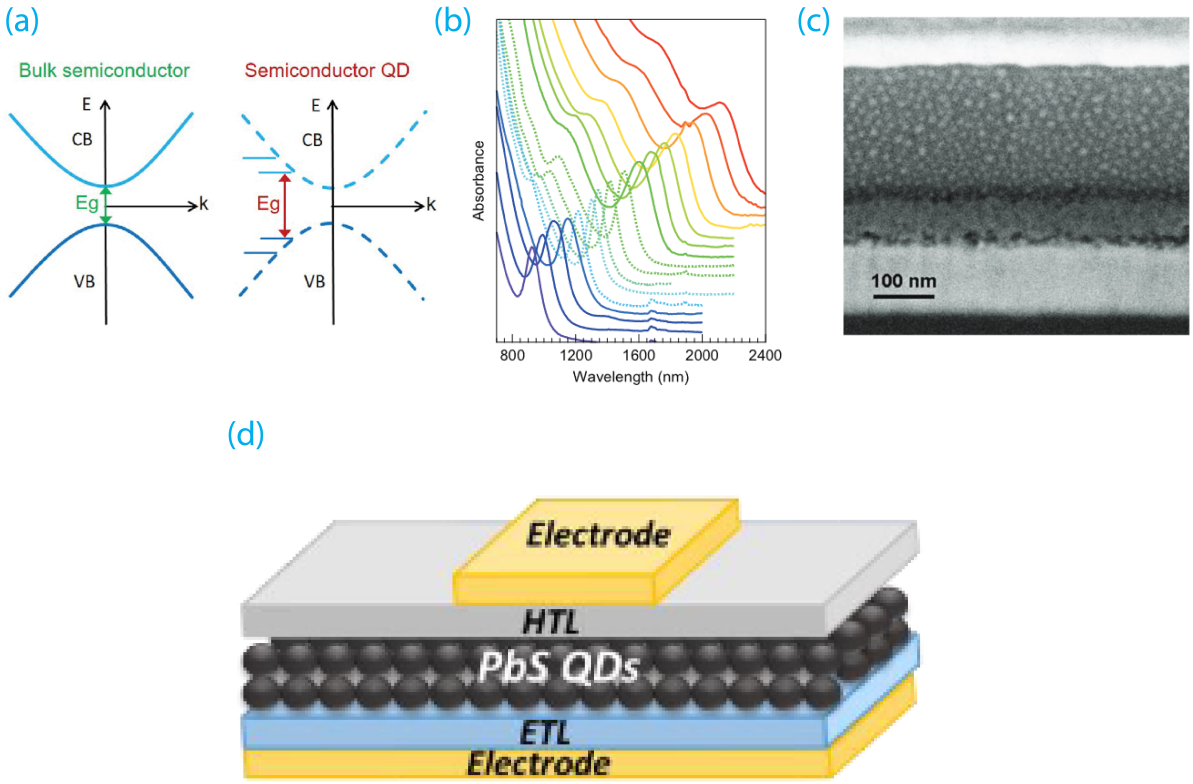


Figure 4.3: (a) Quantum Confinement effect of the bandgap of quantum dot nanocrystals [93], (b) Absorption spectra peaks of PbS CQD for different sizes [94], (c) Photograph of PbS CQDs [95], (d) Typical structure of a PbS CQD NIR image sensor [90]

PbS is a direct bandgap semiconductor with bulk bandgap of 0.41 eV, however, quantum dot PbS crystals with a size range of 2.6-7.2 nm behaves as an indirect bandgap semiconductor with corresponding aborption peaks of 825-1750 nm as shown in Fig. 4.3(b) [94].

The preparation of PbS CQD involves several solution-based colloidal chemistry methods, the details of which can be found in Agarwal [96]. Fig. 4.3(c) shows the picture of PbS CQDs used in NIR image sensors. The typical structure of a PbS CQD NIR sensor, as shown in Fig. 4.3(d) consists of:

- Substrate: The foundation of the PbS CQD image sensor is the substrate, which provides mechanical support and stability for the subsequent layers - it can be either glass or silicon.
- Bottom Electrode: On top of the substrate, a bottom electrode is deposited. This electrode serves as the anode for the device and is typically made of a transparent conductive oxide (TCO) to allow

light to pass through.

- Hole Transport Layer (HTL): The hole transport layer is deposited on top of the bottom electrode. This layer facilitates the movement of holes from the active layer to the anode and also helps to block electrons, reducing recombination losses.
- PbS Quantum Dot Layer: The PbS CQD layer is the active layer where light absorption and photogeneration of charge carriers occur. This layer consists of colloidal PbS quantum dots, which are typically deposited using solution-based techniques such as spin-coating or inkjet printing. The thickness of this layer is optimized to balance light absorption and charge transport.
- Electron Transport Layer (ETL): The electron transport layer is deposited on top of the PbS CQD layer. This layer facilitates the movement of electrons from the active layer to the cathode while blocking holes.
- Top Electrode: On top of the ETL, a bottom electrode is deposited. This electrode serves as the cathode for the device and is typically made of metal for good electrical conductivity.
- Encapsulation Layer: To protect the device from environmental degradation (e.g., moisture, oxygen), an encapsulation layer is often applied. This layer is generally made of polymer coatings.

PbS CQDs aim to solve the cost and the complexity issues that affect InGaAs sensors. As PbS CQDs are solution based with relatively inexpensive materials, the synthesis is low cost and can easily be scaled to large scale commercial production. Additionally the size-tunable bandgap of PbS CQDs is easier to control as compared to InGaAs sensors, while also being easily integratable with the ROIC using silicon substrates as compared to the 3D integration of InGaAs.

However, PbS CQDs also face some fundamental problems that make it CMOS-incompatible which cannot be resolved. Some of these problems include:

1. RoHS Non-Compliance: Lead is a toxic heavy metal, and the use of PbS in quantum dot sensors raises major environmental and health concerns. Safe handling and disposal of lead-containing materials are essential, and Pb cannot be introduced into the CMOS fabrication plants [97].
2. Stability Issues: PbS quantum dots are prone to degradation when exposed to air, moisture, and light. This degradation affects the performance and longevity of the sensors. Encapsulation techniques can mitigate these issues, but they add complexity and cost to the fabrication process.
3. Non-Uniform absorption coefficient: While the size-tunable bandgap of PbS provides high absorptions at specific wavelengths, the compromise at other wavelengths makes the device behaviour highly irregular, making the design of wideband sensors challenging.
4. Integration with ROIC: While PbS are easier to integrate with ROIC than InGaAs, integration of solution-based CQDs is still a novel domain with the need to develop more advanced hybrid integration techniques [21].
5. Incapability of 4T Pixel architecture: Due to the physical structures of PbS CQD sensors, these sensors can only be built using the 3T pixel architecture and thus cannot utilize any of the advancements made in CMOS image sensors.

Thus, PbS CQDs too cannot be used for the design of CMOS-compatible Visible+NIR/SWIR wideband image sensors.

4.3. Germanium-on-Silicon NIR Image sensors

As compared to InGaAs sensors and PbS CQD sensors, Germanium-on-Silicon image Sensors are structurally simple - utilizing the simple pn-junction structure shown in Fig. 3.9, with one layer as germanium and the other as silicon. The bandgap of germanium (0.66 eV) allows for the absorption of light in the NIR/SWIR range (700-1700 nm), while the underlying silicon in theory in theory allows for integrated operation capabilities. However, despite extensive research on Ge-on-Si sensors [98, 69, 99, 100, 101, 102] , there are no commercially available Ge-on-Si wideband image sensor to date. This is primarily due to the poor performance on these sensors as compared to InGaAs sensors and PbS CQD sensors, combined with the CMOS incompatibility of the fabrication processes used - making Ge-on-Si not viable for practical applications [103].

The simplest technique to build an integrated Visible+NIR/SWIR wideband image sensor would be to build the existing CMOS image sensor designs - from the image sensor, the ROIC, as well as all the other signal processing components - on a germanium wafer in place of silicon. Devices made out of germanium have operating principles similar to silicon - as a matter of fact, the world's first transistor was made of germanium instead of silicon [104]. However, the transition to silicon based electronics with optimization of all fabrication processes geared for silicon has rendered the design and fabrication of germanium-based ROIC and signal processing analog circuits infeasible.

Thus, most of the current research for Germanium-based image sensors have focused on the fabrication of Germanium-Silicon heterojunction diodes. Most Ge-on-Si sensors are fabricated using either chemical vapor deposition (CVD) [102, 105, 57] or molecular beam epitaxy (MBE) [98, 69, 106] - these processes require very high temperatures, well beyond the 300 °C BEOL thermal budget of the ROIC and other electronics in an integrated circuit [107], and thus are CMOS incompatible. Additionally, these processes introduce very high strain and defects in the germanium lattice while the lattice mismatch between Ge and Si through these processes is high - leading to poor device performance. While other promising fabrication techniques such as low-temperature wafer-bonding are being investigated [108, 109], this process is not currently not scalable for the use in large pixel arrays and can only utilize the 3T pixel architecture.

Fig. 4.4 shows some of different Ge-on-Si image sensors designs using CVD, MBE and wafer-bonding processes.

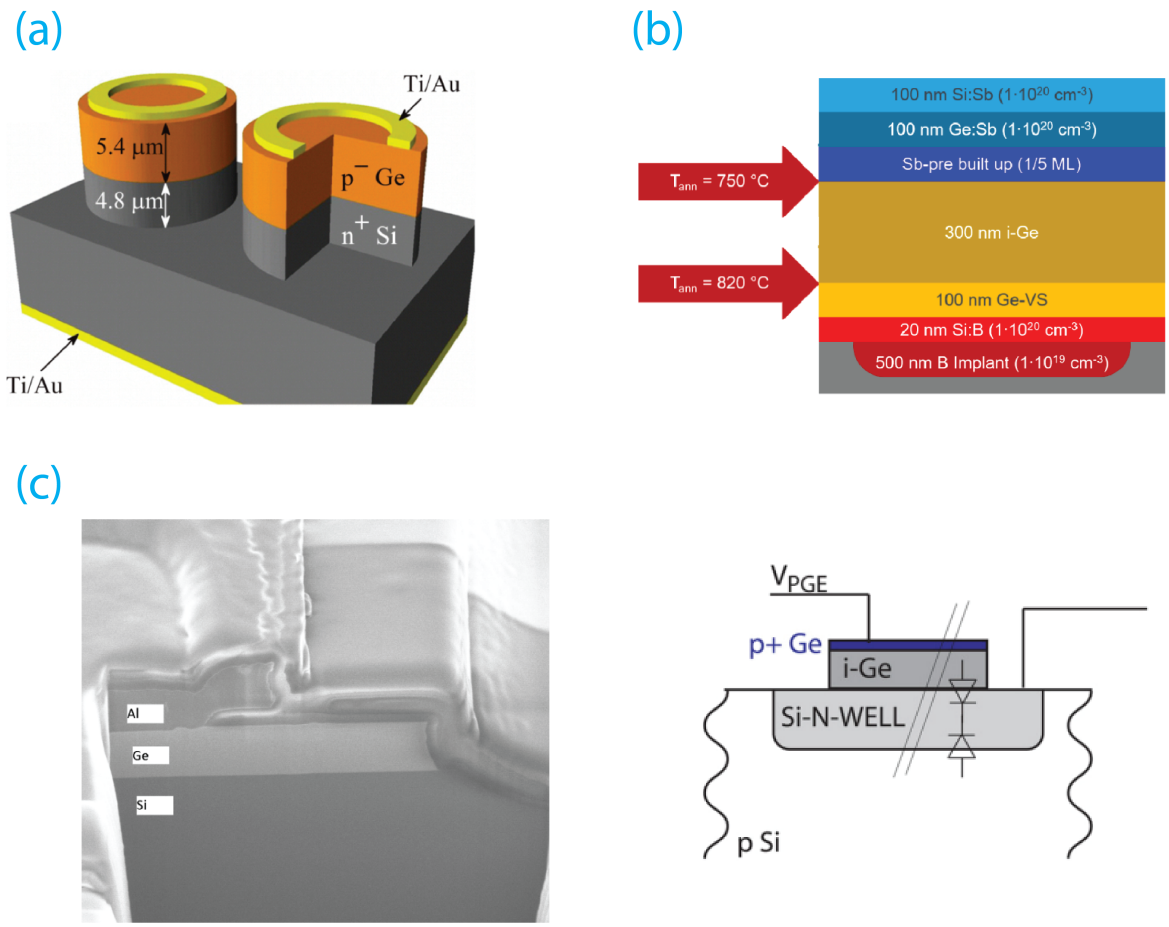


Figure 4.4: Design of Ge-on-Si NIR image sensors fabricated using (a) wafer-bonding [108], (b) MBE [98], and (c) CVD (specifically LEPECVD) [102] (Right) SEM cross-section of the Ge-Si diode.

The structure and operation of the current Ge-on-Si image sensors is identical to the 3T architecture Si-CMOS image sensor and thus will not be discussed here.

The advantages of Ge-on-Si image sensors include:

1. CMOS Compatibility: Ge-on-Si image sensors are inherently compatible with CMOS-technology, with the current incompatibility only stemming from the high-temperatures of fabrication processes used, which can potentially be resolved.
2. Visible + NIR/SWIR Wideband sensitivity: Germanium's low bandgap makes it highly sensitive to NIR wavelengths, enabling the detection of a broader spectrum without compromising on the visible light spectrum
3. High-Speed Performance: Ge-on-Si sensors can potentially operate at high speeds due to the high carrier mobility in germanium, making them suitable for applications requiring fast image capture.

The disadvantages of Ge-on-Si include:

1. Lattice mismatch: Any significant lattice mismatch between Ge and Si during the fabrication process will introduce defects and dislocations in the Ge layer, which can severely degrade the sensor's performance and reliability.
2. Thermal Expansion Coefficient Mismatch: The mismatch in thermal expansion coefficients between Ge and Si can lead to thermal stress, especially during high-temperature processing, affecting the sensor's structural integrity. This can potentially be avoided using low temperature fabrication processes
3. Maturity of technology: Currently, there is a lack of mature and scalable processes for the large-scale production of Ge-on-Si NIR sensors. Other NIR sensing technologies, such as InGaAs (Indium Gallium Arsenide) sensors, are already well-established in the market, resulting in low interest in research in further development.

4.4. Conclusion

Despite the limitations of current Ge-on-Si image sensors, this technology does not have the same fundamental limitations towards CMOS compatibility like InGaAs and PbS CQDs. Any low-temperature deposition process of crystalline Ge would allow for the development of BEOL NIR/SWIR enhancement of CMOS image sensors, while retaining all the advantages of scalability and maturity of current CMOS sensor. One such technique is metal-induced layer exchange of group-IV materials [110], which has to potential to deposit crystalline germanium thin-films. This technology can potentially resolve the current CMOS-compatiblity issues of Ge-on-Si sensors while allowing for more advanced image sensor designs, thus will be the basis of this project.

5

Proposed CMOS-compatible NIR/SWIR enhancement techniques for CMOS Image sensors

With Chapter 4 discussing three different technologies currently used for NIR/SWIR image sensors, this chapter shall present two different CMOS-compatible NIR/SWIR enhancement techniques, which adhere to the three main requirements laid down in section 1.1, allowing for the realization of the project goal of CMOS-compatible wideband image sensor.

5.1. Depostion of Germanium through low-temperature processes

In section 4.3, it was seen that the bandgap limitation of CMOS image sensors can be overcome using a pn-heterojunction of low-bandgap materials with silicon, such as the Ge-on-Si image sensor. However, CMOS-incompatibility and performance limitations of CVD, MBE and wafer-bonding fabrication processes of low-bandgap materials have limited the applications of such sensors. It can be seen that the limitation of Ge-on-Si is fabrication process dependent, and this has resulted in a lack of research into the design of CMOS image sensors that use BEOL low-bandgap material deposition. As part of this project, the Image Sensor Group at Delft University of Technology is currently carrying out extensive research into the formation of polycrystalline thin films of low-bandgap materials through the deposition of amorphous layers. The thickness of these thin films is in the order of 100 nm and can potentially allow for the design of advanced CMOS-compatible wideband Ge-on-Si image sensors. This project is focused on exploring the design feasibility of BEOL-deposited Ge thin films over CMOS sensors (as shown in Fig. 5.1), and due to intellectual property restrictions, the details of the low-temperature Ge deposition process used will not be discussed here.

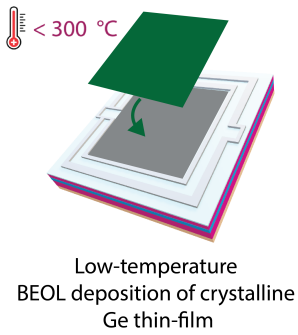


Figure 5.1: Schematic of the BEOL deposition of Ge thin-films to build Ge-on-Si image sensor

5.2. Micro-structured surface for NIR/SWIR enhancement

The second proposed is through the micro-structuring of the image sensor surface with inverted-pyramidal cavities of similar dimension to the desired wavelength, i.e., ~1 µm, through anisotropic wet-etching of the silicon substrate as shown in Fig. 5.2. While this process does not solve the bandgap limitations of silicon, it can potentially greatly enhance the performance of the Ge-thin film deposited using the low-temperature process, as proposed in the previous section.

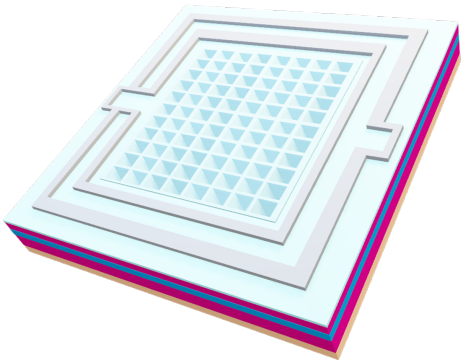


Figure 5.2: Schematic of the proposed use of pyramidal micro-structures for the NIR/SWIR enhancement of the Ge-on-Si image sensor

Micro-structured surfaces have been used extensively to enhance the performance of solar cells in the form of ”moth-eye anti-reflective (AR) coating” [111, 112, 113], and has recently seen a growing interest for use in image sensors [55, 114, 115, 116]. These micro-structures behave as an anti-reflective coating, providing spectral response enhancement up to 70%. However, the extremely low spectral response of CMOS image sensors at wavelengths above 850 nm combined with its near 100% QE in the visible spectrum meant that micro-structuring the surface as an individual process did not provide practically sufficient enhancement to justify its use.

On the other hand, surface micro-structuring with inverted pyramids followed by the low-temperature deposition of germanium can greatly enhance the performance of the Ge-thin film in the following ways:

1. Absorption Enhancement through scattering: Scattering on two dimensional structures of dimensions slightly smaller than the wavelength of light leads to formation of localized surface plasmons, which enhances the absorption of thin films while also resulting in surface lower recombination rates [117].
2. Absorption Enhancement through increased path length: The angled surface of Ge thin-film within the cavities as well as the repeated reflections in a pyramidal cavity increases the effective distance the light has to travel across in Ge, increasing the photon flux absorbed (guided by the Beer Lambert equation 3.5).
3. Anti-Reflections through photon-trapping: The difference in refractive index of the germanium thin-film and the upper native oxide naturally formed prevents reflections on the surface of the pixel due to refraction and total internal reflections [55]. This behaviour is similar to the moth-eye AR coating in solar cells.

Thus, the two techniques: low-temperature-deposition of Ge-thin-film as well as surface micro-structuring through anisotropic wet etching, will be used in conjunction in this project for the design of CMOS-compatible visible+NIR/SWIR image sensor and the performance of this design will be evaluated using device-physics and optics simulations.

6

Complete Design and Simulation Results

With the two different CMOS-compatible NIR/SWIR enhancement techniques: (a) Layer exchange deposited germanium on silicon, and (b) microstructured surface for performance enhancement of the deposited Ge layer, proposed in Chapter 5, this chapter presents a novel design which incorporates both these techniques into a single sensor. Several key performance parameters of the image sensor must be considered in such a design, including:

1. Effect of Ge-Si hetero-junction and doping concentrations on the transport efficiency of generated charge carriers.
2. Charge carrier Generation rate of low-temperature-deposited Ge thin-film for the currently reported thicknesses - with and without microstructures.
3. Effect of microstructures on transport efficiency of generated charge carriers.
4. Response time of the image sensor.

To perform the analysis of the above-mentioned parameters for the proposed design, three simulators, (a) AFORS-HET for hetero-junction simulations, (b) SPECTRA for diffusion-drift simulations, and (c) TOCCATA for FDTD simulations, are used and the results presented in this chapter.

6.1. Complete Design

Figure 6.1(a-b) shows the complete proposed CMOS-compatible Ge-on-Si visible+SWIR wideband image sensor design. The image sensor is a front-side illuminated sensor with 3 epitaxial silicon layers grown over a highly doped p-type silicon wafer. The surface is microstructured with inverted pyramids of 1 μm of size and depth, with a 1 μm spacing between adjacent pyramids. A Ge thin film is deposited on this microstructured surface, which is taken as 100 nm for this project (the maximum thickness currently being researched by the Image Sensor group at TU Delft). The area of the photosensitive region is highly scalable, with pixel pitches ranging from 300 μm up to 1 mm currently being fabricated by the Image Sensor Group. However, the interest of this project lies only in the internal QE calculations- which are independent of the area of the photosensitive region, and thus all simulations have been carried out using only 10 μm and 55 μm pixels to reduce simulation time (The layout for these two pixels can be found in Appendix A).

As discussed in section 3.4.1, the spectral response of an image sensor can be maximized by expanding the depletion region. The depletion regions in the proposed design are formed between the buried n-doped epitaxial layer (buried n-epitaxy) and the two p-doped epitaxies. The buried n-epitaxy is highly doped (1e16), while the top p-doped epitaxial layer (top p-epitaxy) is lowly doped (1e14). This ensures that the depletion expands into the top p-epitaxy, and the depletion width (2.8μm) is greater than the combined width of the top p-epitaxy and buried n-epitaxy (2.5 μ). Thus, the top p-epitaxy is fully de-

pleted without the requirement of any externally applied voltage. The buried p-doped epitaxial layer (buried p-epitaxy) is highly doped (1e16) to prevent the depletion from reaching the substrate, thereby reducing the dark current (Section 3.5). By applying a sufficiently high bias voltage (*pinning voltage*), the buried n-epitaxy is also completely depleted, similar to a pinned-photodiode (PPD) in the 4T pixel architecture (Section 3.7).

The buried n-epitaxy serves as the *cathode* and is connected to the positive terminal of the device through the DN implantation. The negative terminal, i.e. the *anode*, is connected to the top p-epitaxy and the Ge thin-film through the $p+$ implantation. The generated electrons move towards the buried n-epitaxy under the influence of the electric field in the depletion region and then move towards the cathode, while the generated holes diffuse towards the anode (Fig. 6.1(c)). The DP implantation is a barrier to the mobile electrons between adjacent pixels and is used to prevent cross-talk.

The simulations of the proposed image sensor as part of this project use a design compatible with the 3T pixel architecture (Section 3.7). However, this device can be used in a 4T pixel architecture with the use of an additional transfer gate in place of the cathode contact - thus, allowing for the use of advanced CMOS readout circuits in partial implementations of this image sensor.

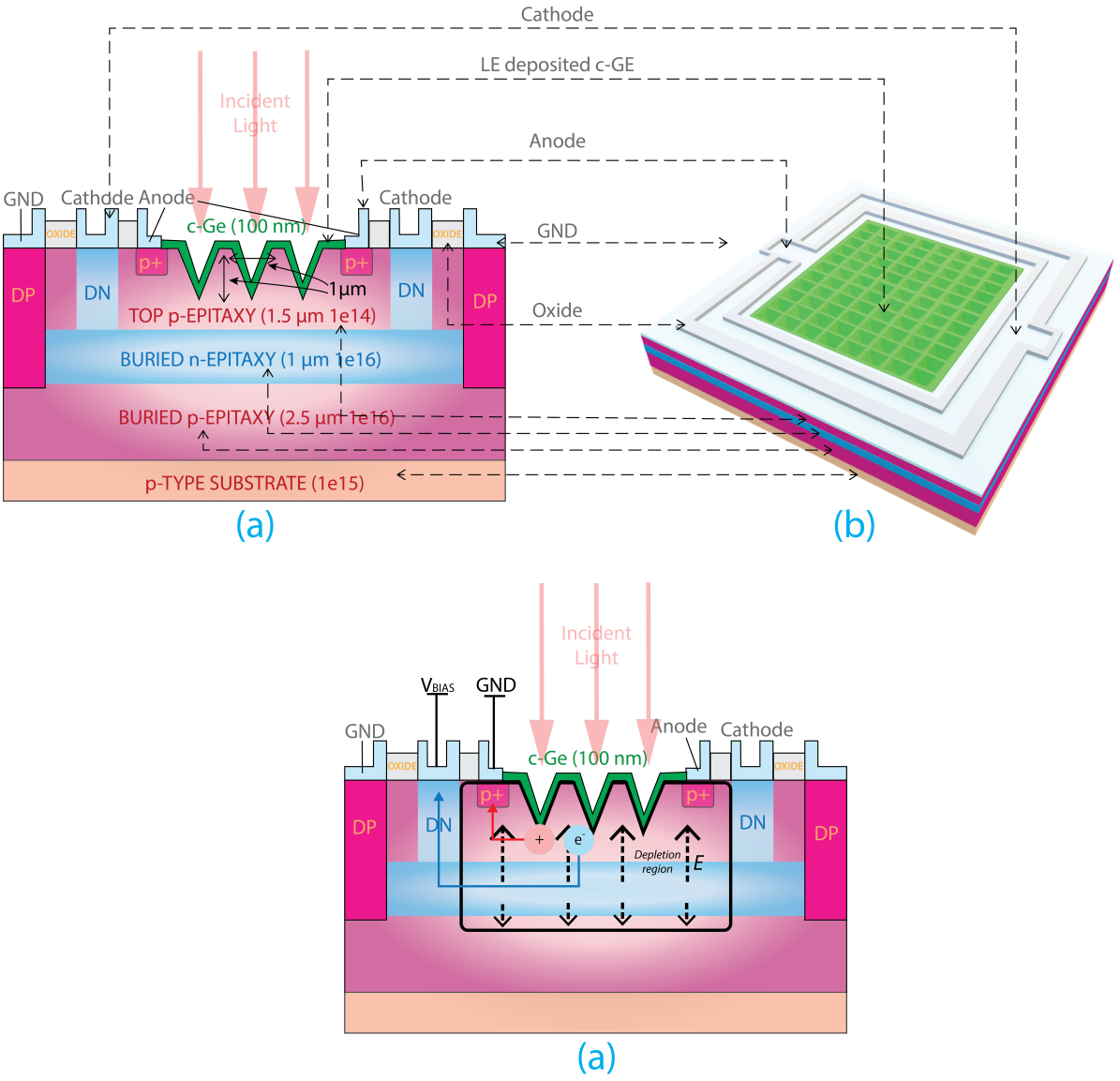


Figure 6.1: (a-b) Schematic of the proposed image sensor. (c) Biasing on the image sensor and transport of the generated charge carriers.

6.2. About the simulators: AFORS-HET, SPECTRA and TOCCATA

About the simulators Before presenting the different performance results and analysis of the proposed image sensor, it is important to first understand the simulators used as part of this project and their respective theoretical models. These simulation results are important in making feasibility studies of the proposed image sensor design while also providing an estimation of the performance of the fabricated device. Additionally, any deviation between the simulated results and the fabricated device characterization can prove useful in understanding the limitations of current theoretical models and serve as a baseline for improved future simulations.

This project uses three key simulators:

- AFORS-HET simulator: The AFORS-HET (automat for simulation of hetero-structures) simulator, developed by the Helmholtz-Zentrum Berlin (HZB) [118], is used to model and analyze the semiconductor heterojunction in solar cells. In the context of this project, AFORS-HET is used to obtain the band diagrams of the Ge-Si interface, taking into account different phenomena such as valence band offsets, band bending, doping concentration and applied potential.
- SPECTRA: SPECTRA, developed by Link Corporation [119], is a 3-D two-carrier semiconductor device physics modelling program that simulates the readout characteristics of an image sensor by using the diffusion-drift model (Section 3.1.7). This project uses this simulator to calculate the spectral response and quantum efficiency of the proposed image sensor for different parameters. However, this simulator does not take into account the optical effects of microstructures on the surface of the sensor.
- TOCCATA: TOCCATA, also developed by Link Corporation [119], is an optics simulator capable of simulating the absorption profiles of semiconductor layers. This simulator can take into account the surface reflections and refractions using the ray-tracing method, or additionally the diffraction and interference using FDTD (Finite Difference Time Domain) method. This project uses the FDTD method, which solves the four Maxwell equations:

$$\nabla \times \mathbf{E} = -\mu \frac{\partial \mathbf{H}}{\partial t} \tag{6.1}$$

$$\nabla \times \mathbf{H} = \epsilon \frac{\partial \mathbf{E}}{\partial t} + \mathbf{J} \tag{6.2}$$

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\epsilon} \tag{6.3}$$

$$\nabla \cdot \mathbf{H} = 0 \tag{6.4}$$

$$\tag{6.5}$$

  (where μ, ϵ, and ρ are the permiability, permitivity, and conductivity) on loop at every time step, to observe the spectral response enhancement obtained using the microstructures on the surface of the image sensor.

6.3. The Ge-Si Heterojunction and Band diagram of the proposed design using AFORS-HET

The primary design consideration to be made for the proposed Ge-on-Si wideband image sensor is the doping type and concentration of both the low-temperature-deposited Ge-thin film as well as the different Si epitaxial layers. The movement of generated holes and electrons across the different layers is determined by the charge concentrations, potential barriers as well as the electric field across the regions. These parameters can be obtained through the observation of the band diagrams of the different semiconductor layers, and this section presents the AFORS-HET band-diagram simulations of the proposed image sensor and the reasoning behind the selection of the doping type and concentrations.

The interface between Ge and Si forms a *heterojunction*. Heterojunctions formed between substances of different bandgaps result in band alignment through band bending and band offset. Fig. 6.2 shows the band diagram of a 2 mm thick Ge-Si heterojunction. Although both Ge and Si have identically doping (p-type 1e14), the difference in Ge-Si band gap leads to the formation valence band offset while the conduction band remains continuous. This results in the selective movement of charge carriers - where

only electrons can freely move across the junction, any hole at the interface is obstructed and leads to recombination and reduction in the spectral response.

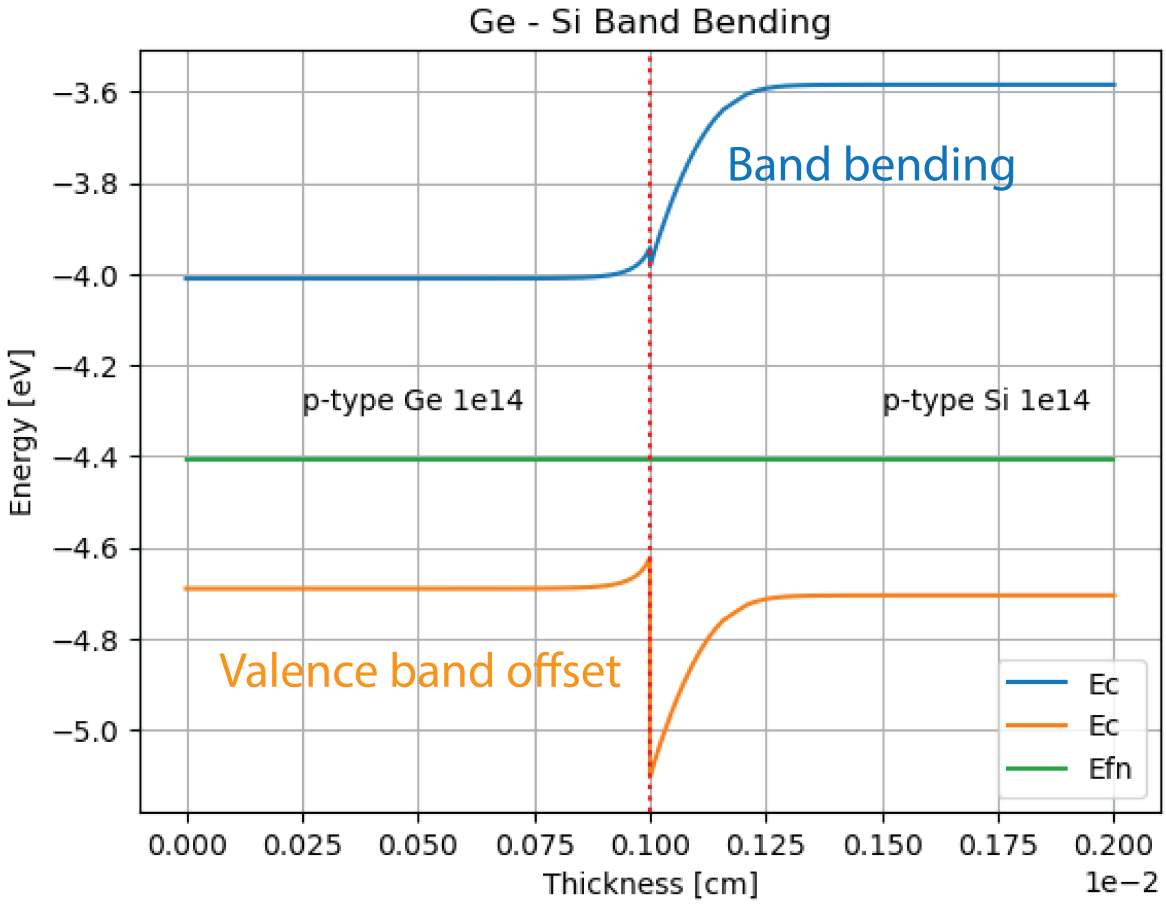


Figure 6.2: AFORS-HET simulation of a 2 mm Ge-Si heterojunction showing the band-bending and valence band offset

To account for the selective permeability of charge carriers across the heterojunction, the lowly doped top epitaxial layer in contact with the Ge layer is chosen to be p-type doped, while the highly doped buried epitaxial layer is n-type doped - this ensures only the transport of electrons across the Ge-Si interface while the holes can be collected directly from the Ge layer through diffusion to anode.

However, it is also important to take the doping of the Ge layer itself into consideration. The doping type and concentration of the Ge-layer causes a shift in the band diagrams and electric field across the depletion region in the Si layers. p-doped Ge layer favours the transport of electrons across the heterojunction and towards the buried n-epitaxy through the depletion region (Fig 6.3(a)) and results in an increase in the electric field. (Fig 6.3(c)), while an n-doped Ge layer results in the formation of a Ge-Si heterojunction depletion - hindering the transport of electrons (Fig 6.3(a)) as well as a reduction in the electric field (Fig 6.3(c)). The electrons and holes accumulate at the Ge-Si interface resulting in a decrease in the spectral response of the image sensor. The impact of Ge-doping on the spectral response of the device is presented in Section 6.5.

After the low-temperature Ge deposition process currently being investigated by the Image Sensor Group, the crystalline Ge layer is reported to be highly doped. By having a high-doped p-type Ge layer, the transport of charge carriers is favoured with an improvement in the spectral response. Thus, the doping type and concentration of the Ge layer are selected to be p-type 1e18.

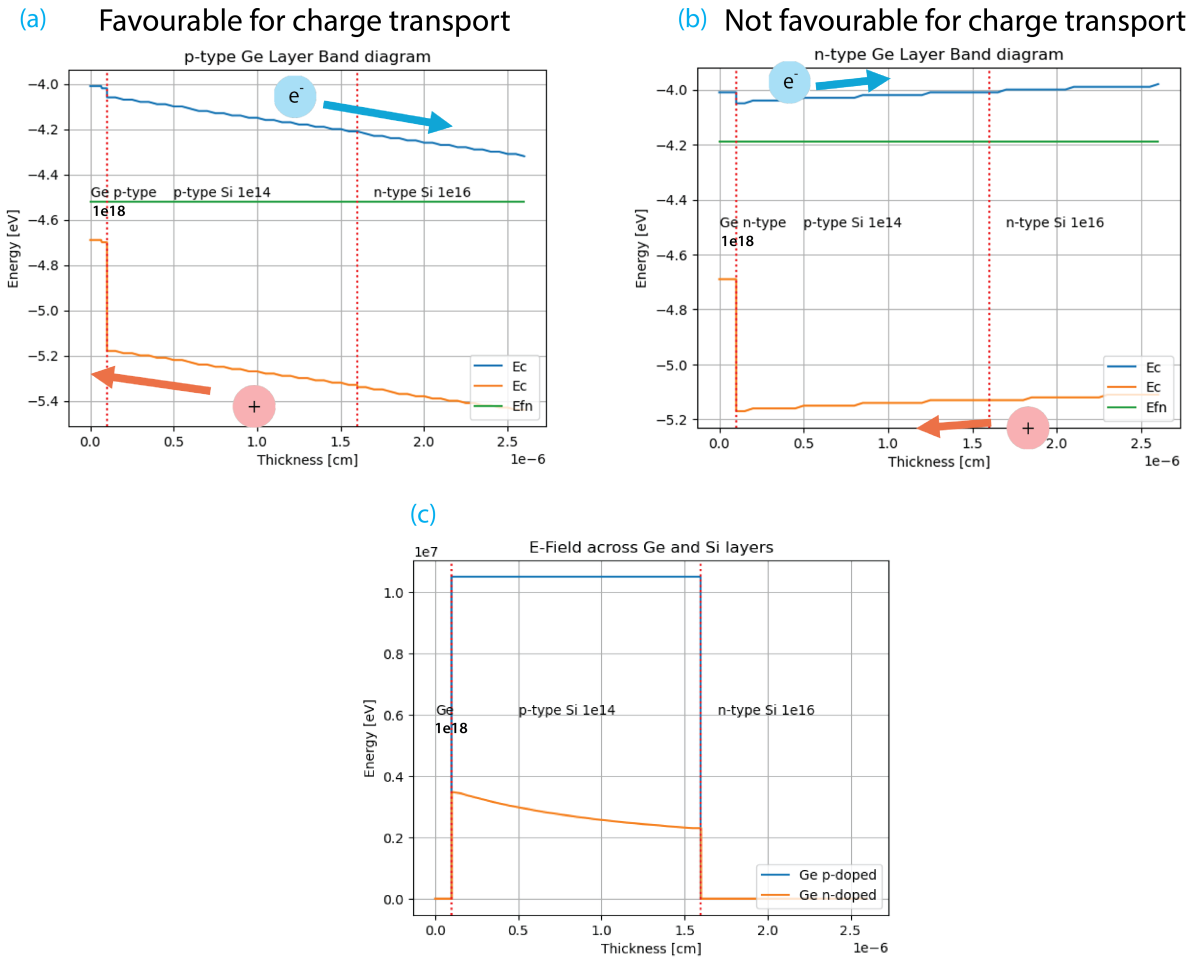


Figure 6.3: AFORS-HET simulations of (a-b) Band diagram of the Ge and Si epitaxial layers of the proposed image sensor for different Ge doping types: (a) 1e18 p-doped Ge layer, (b) 1e18 n-doped Ge layer, (c) E-field across the photodiode. The p-type doping is favourable over the n-type doping of the Ge layer in the facilitation of charge transport across the Ge-Si heterojunction.

6.4. SPECTRA simulation of NIR/SWIR Enhancement through low-temperature-deposited Ge

With the doping type and concentration of the Ge and Si epitaxial layers selected through the AFORS-HET simulations, the complete device without microstructures (as shown in Fig 6.4(a)) can now be simulated in SPECTRA to obtain the currents at the cathode and anode (Fig 6.4(b)). This can then be used to obtain the *spectral response (SR)* of the device (Section 3.4), defined as the response obtained per unit incident power, and is calculated as:

$$\text{Spectral response SR (A/W)} = \frac{\text{Current obtained at electrodes (A)}}{\text{Incident light power (W)}} \tag{6.6}$$

From the spectral response, the quantum efficiency of the image sensor is then obtained as:

$$\text{QE (\%)} = \frac{\text{SR}}{\lambda}\frac{hc}{q} \tag{6.7}$$

where, λ is the wavelength of the incident light.

The simulation parameters used for the proposed image sensor are:

Device Parameter	Value
Incident power per unit area (W')	10^{-2} W/cm^2
Width of the photosensitive area (d)	55 μm
Thickness of Ge	100 nm

Table 6.1: Device simulation parameters

Fig. 6.4(c) shows the QE comparison for the image sensor with and without the low-temperature-deposited GE layer (without the use of microstructures). It can be seen that the low-temperature-deposited Ge not only improves the QE in the visible spectrum, the bandwidth of the image sensor is also expanded into the NIR/SWIR region with a QE of 14% at 1000 nm and 1.4% at 1300 nm using only a 100 nm thick Ge layer - demonstrating the technical feasibility of the proposed design.

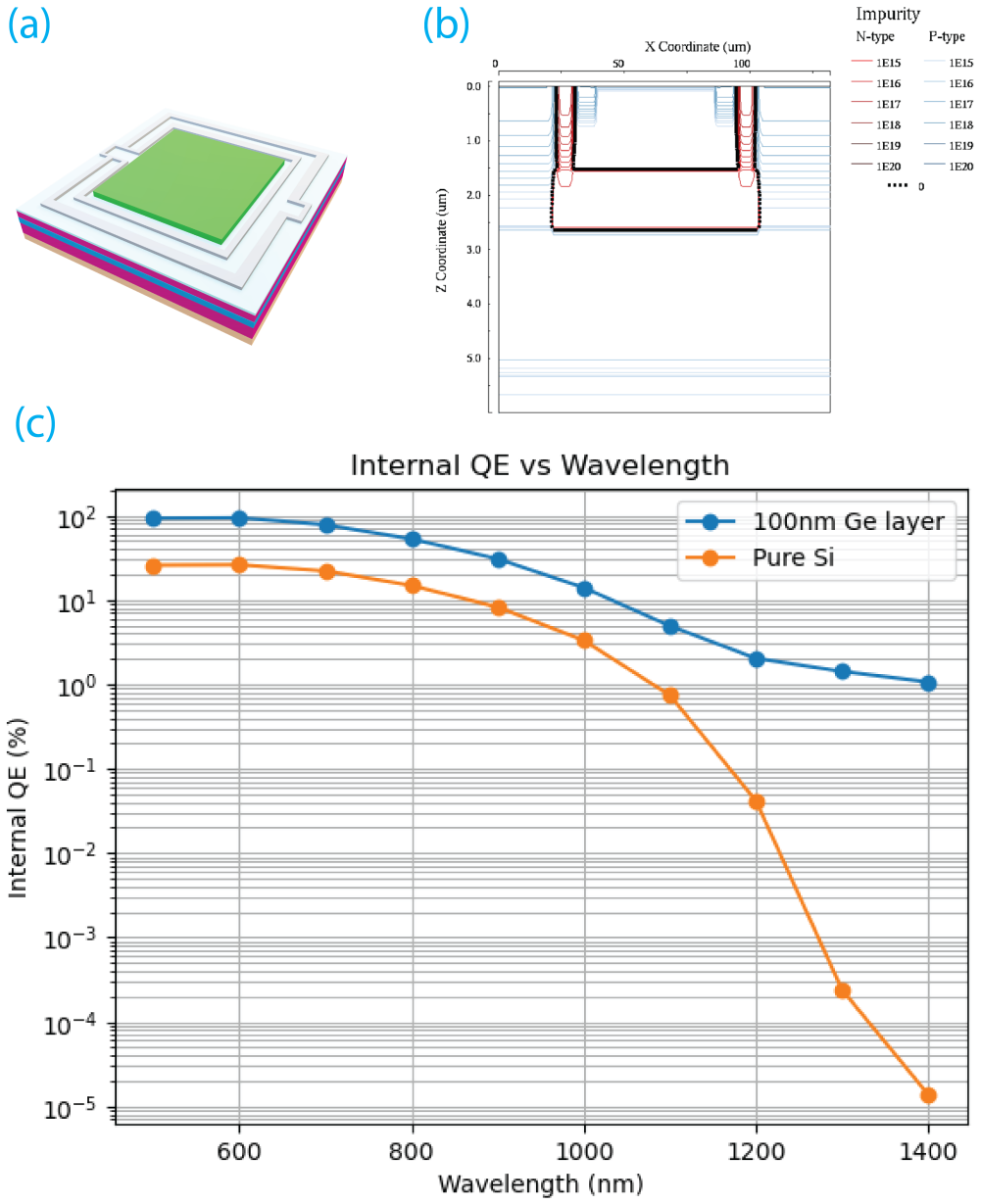


Figure 6.4: (a) Simulated image sensor design with Ge-layer (without microstructures) (b) SPECTRA simulation of the image sensor, showing the impurity concentrations (b) Internal QE comparison of the image sensor using SPECTRA with and without 100 nm Ge-layer

6.5. Effect of Ge-layer doping on QE

The effect of doping of the Le-deposited Ge layer on the energy bands and the electric field across the epitaxial layers of the image sensor - with p-type doped Ge layer facilitating the movement of electrons across the heterojuncion and increases the electric field in the depletion, while n-type doping hinders the charge transport. This is also reflected in the QE simulation results of the image sensor. Fig. 6.5 shows the effect of n-type doping concentration on the QE of the image sensor across the visible and NIR/SWIR bandwidth, and it can be observed that at very doping concentrations, the QE reaches 0 at longer wavelengths indicating a complete blockage of all generated electrons across the Ge-Si heterojunction.

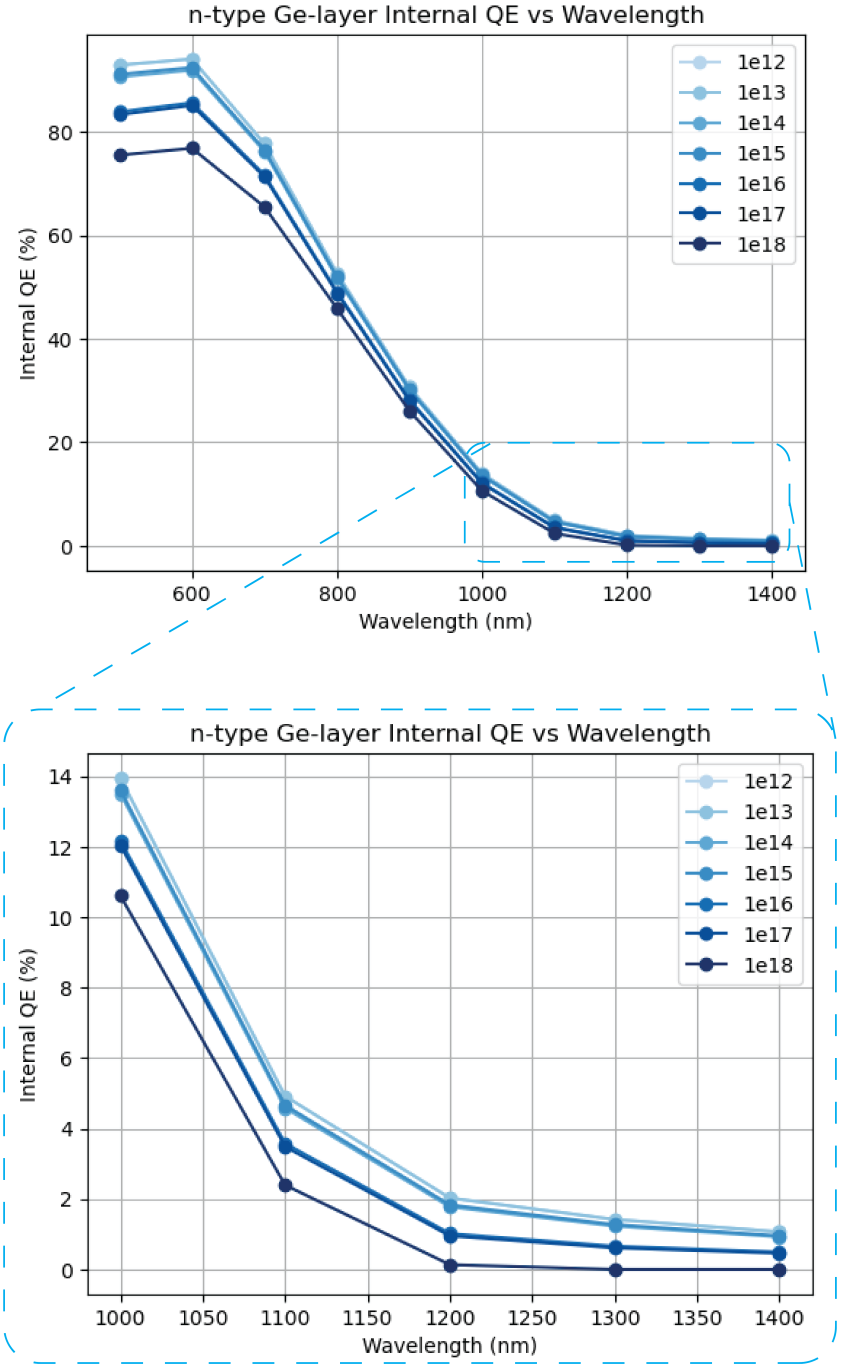


Figure 6.5: QE vs Wavelength for n-type doped Ge layer at different doping concentrations

On the contrary, p-type doping favours the transport of electrons from the Ge layer into the Si epitaxy. Fig 6.6 shows the QE vs wavelength for different p-type doping concentrations of the Ge layer. It is interesting note that while the QE obtained using p-type doping is higher than the QE with n-type doping (Fig. 6.5), no change in the QE is observed with an increase in doping concentration. This indicates that the simulator SPECTRA is simulating an *ideal* Ge-Si heterojunction.

In the simulation of the image sensor with the p-type doped Ge layer, no electrons are lost at across the Ge-Si heterojunction and the charge transfer is 100% efficient, thus there is no effect of change in doping concentration. However, realistically the lattice mismatch between the Ge and Si layers leads to recombination losses at the interface, and higher doping concentrations increases strain and worsens the lattice mismatch [120, 121]. This increase in lattice mismatch should correspond to a decrease in the QE obtained at higher doping concentrations. However, the defect density at the Ge-Si heterojunction formed using low-temperature deposition process must be investigated, which is further complicated by the inherent high doping concentrations of the Ge layer after low-temperature deposition. This can prove to be an area of interest for future research on this project.

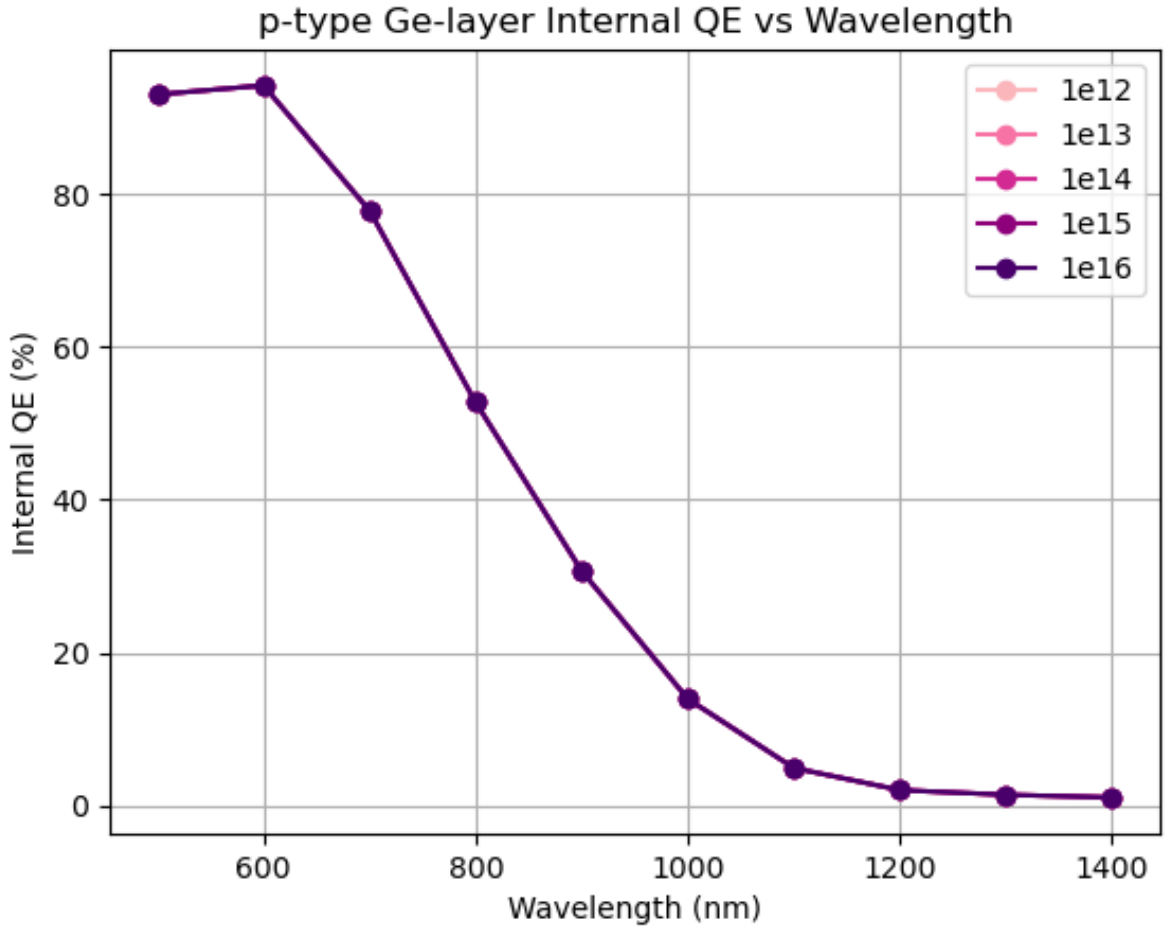


Figure 6.6: QE vs Wavelength for p-type doped Ge layer at different doping concentrations

6.6. Effect of Ge layer thickness

The 100 nm Ge layer used in the simulations presented in the prior sections was selected to account for the current maximum layer thickness achieved through the low-temperature deposition process of deposition. As seen in section 6.4, which this layer significantly improves the CMOS image sensor's performance across the visible as well as the NIR/SWIR spectrum, the QE is very low at wavelengths beyond 1000 nm. Pratical applications of this image sensor for visible + NIR/SWIR image would require for QE exceeding 40% across the spectrum. One way to improve the SWIR performance of this image

sensor is through the use thicker Ge layers, deposited through the multiple low-temperature deposition processes. The maximum achievable QE at different Ge layer thicknesses can be calculated through the Beer Lambert Law (Section 3.1.4), which accounts only for the absorption while neglecting all losses. Fig. 6.7 shows the solution of equation 3.5 for the image sensor using different Ge thicknesses.

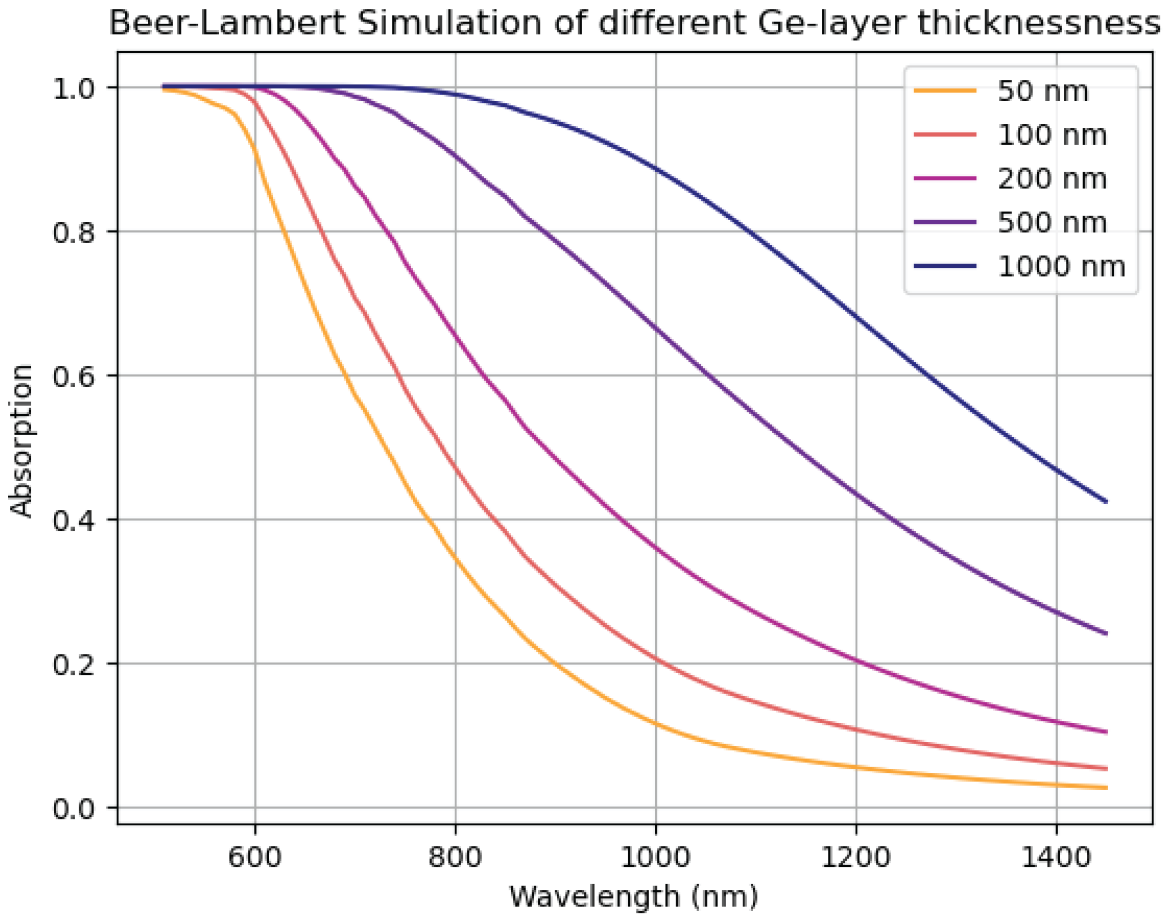


Figure 6.7: Beer Lambert Simulation of the image sensor for different Ge layer thicknesses. The absorption corresponds to the ideal QE neglecting all losses

Fig. 6.8 shows the QE obtained through SPECTRA simulation of the image sensor for different Ge layer thicknesses. The QE obtained through simulations is much lower than the Beer-Lambert calculations in the NIR/SWIR region, with the difference in QE increasing with an increase in Ge layer thickness. This indicates the presence of significant losses in the Ge layers and can potentially be attributed to the recombination losses of charged carriers. As seen in Fig. 6.3(c), due to the high doping concentration of the Ge layer, the depletion region does not extend deeply from the Ge-Si heterojunction boundary. Thus, all electrons generated in the Ge layer have to reach the heterojunction through diffusion only, which leads to significant recombination losses as compared to the depletion region (Section 3.1.7). These recombination losses increase with the increase in diffusion length across thicker layers, potentially leading to larger differences in ideal and simulated QE as observed. However, this does not rule out the possibility of other sources of blockades to the electrons across the Ge-Si heterojunction.

To reduce the diffusion losses in thicker Ge layers, the diffusion rate across the Ge layer must be increased. One possible solution to this is through gradient doping, with higher p-type doping concentrations closer to the image sensor surface and lower doping concentrations nearer to the Ge-Si heterojunction. This difference in doping concentrations sets up an electric field inside the Ge layer which can reduce recombination losses. Exploration of the fabrication processes required for a doping gradient in the Ge layer is another area of interest for future research.

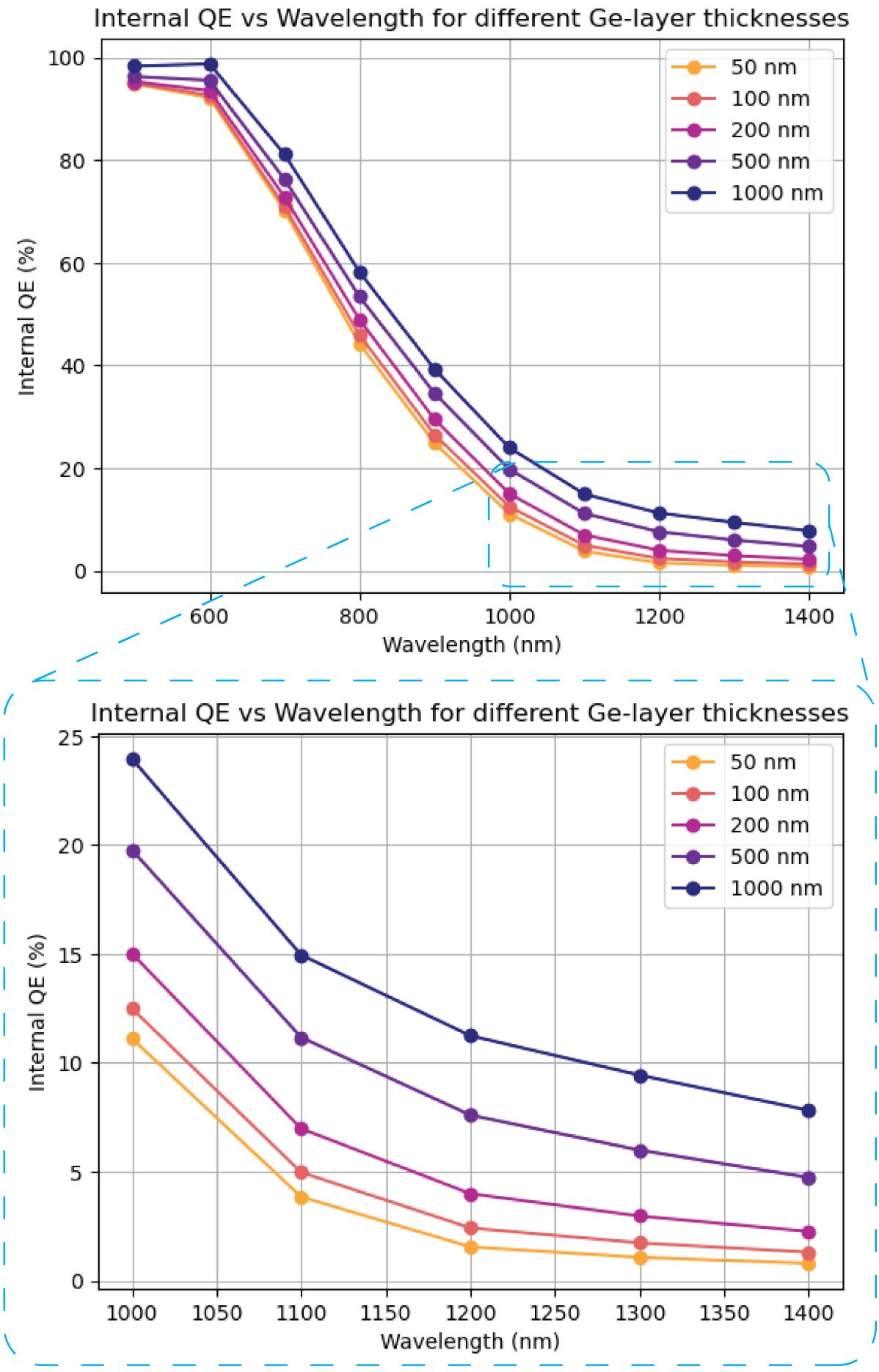


Figure 6.8: Internal QE vs Wavelength for different Ge layer thickness, obtained through SPECTRA simulations

6.7. FDTD Simulation of pyramidal microstructures

The previous sections showcased the first proposed method of achieving NIR/SWIR enhancement through the use of low-temperature-deposited Ge-layer (Section 5.1). In this section, simulation results of the second proposed method, through microstructuring of the image sensor, is presented. A small part of the image sensor comprising of a single 1 µm pyramidal microstructure (as seen in Fig. 6.9, is used for FDTD simulations through the TOCCATA simulator (Fig. 6.9(b)). This is in account for the very large computational power required for FDTD simulations. The FDTD simulations provide the current *generated* in the Ge and Si epitaxial layers, taking in account optical effects such as reflections and scattering. The improvement of the generation current corresponds to an equivalent scaling in spectral response and QE obtained through SPECTRA simulations, as the diffusion-drift current scales linearly with the generation current (Ambipolar equation 3.31).

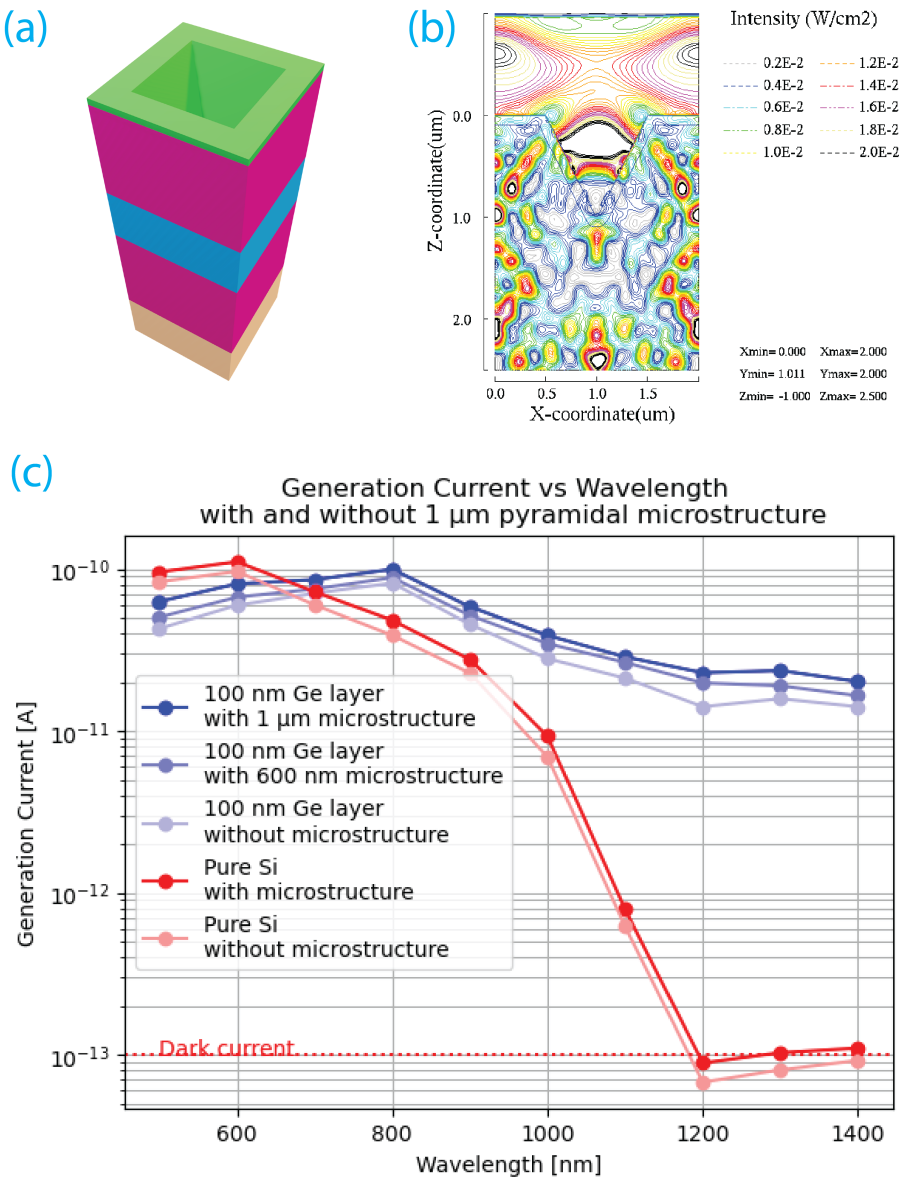


Figure 6.9: (a) Section of the image sensor with single 1 µm pyramidal microstructure used for FDTD simulations. (b) TOCCATA FDTD simulation showing light intensity at different regions of the microstructure. (c) The plot of generation current obtained with and without 1 µm pyramidal microstructure (with and without the low-temperature-deposited Ge-layer). The incident light power is 10^{-2} W/cm^2 over a photosensitive region of width 2 µm, and light propagation time of 5×10^{-13} s

In Fig. 6.9(c), it can be seen that the use of the microstructure provides an improvement in the generation current across the spectrum, both for structures with and without the low-temperature-deposited Ge layer. As reflected by the poor performance of the pure Si structures, the improvement in the QE obtained using the pyramidal microstructure is only a multiple of the QE obtained using for a flat surface, thus, this NIR/SWIR enhancement method cannot be used independently of the low-temperature-deposited Ge layer.

The percentage improvement in internal QE obtained by the pyramidal microstructure is not uniform across the spectrum and depends on both the size of the microstructure as well as the material used (Fig. 6.10). This is due to the differences in refractive indexes of the surface mattering, the effective increase in path length of light through the Ge layer and the scattering of different wavelengths of light on the surface (Section 5.2). With a 600 nm microstructure, it can be seen that the improvement in internal QE is negative at 600 nm. This is due to recombination losses due to increased path length to the contacts, outweighing the enhancement in generation rate due to optical effects at 600 nm wavelength. The cumulative effect of the microstructure provides a maximum improvement of 60% with a pyramidal microstructure.

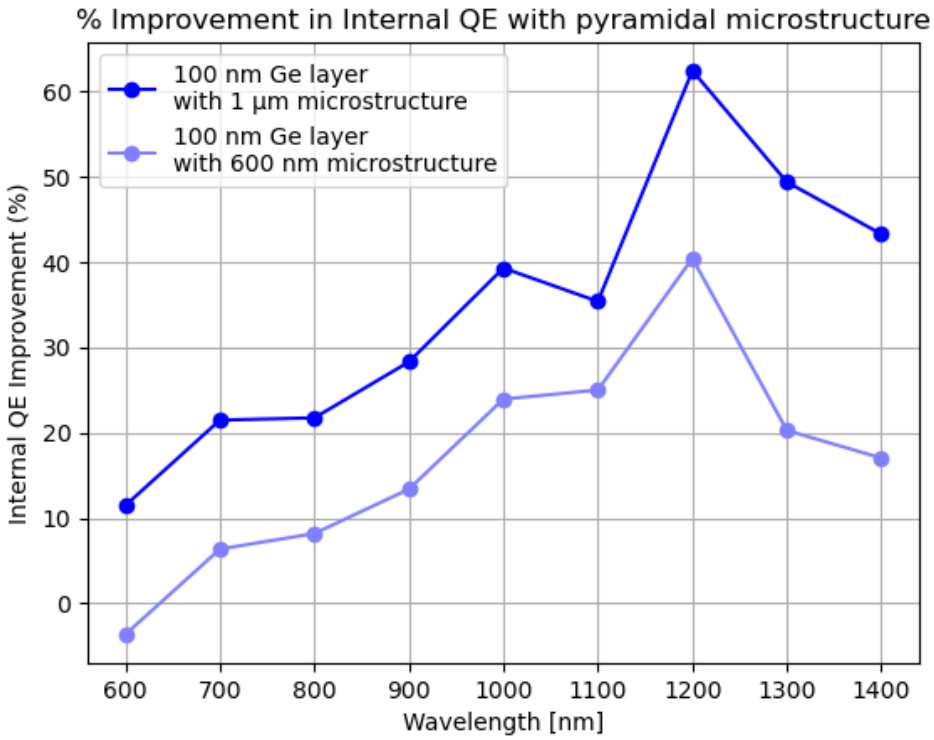


Figure 6.10: Percentage improvement in internal QE obtained through the use of pyramidal microstructures

Different microstructure shapes potentially result in better QE improvement in the NIR/SWIR spectrum. The use of cylindrical holes has better performance as compared with a pyramidal microstructure as seen in Table 6.2. However, it is technologically challenging to develop masks with circular holes and etch the substrate anisotropically to obtain a cylindrical microstructure, thus making its practical implementation infeasible.

1 µm pyramidal microstructure	1 µm cylindrical microstructure
62.41 %	97.45 %

Table 6.2: % Improvement in QE at 1200 nm with pyramidal and cylindrical holes

6.8. QE of complete proposed image sensor design

Combining the 100 nm low-temperature-deposited Ge layer with the 1 µm pyramidal microstructures, the QE of the complete device (as seen in Fig 6.1) is presented in Fig. 6.11 - with an internal QE of 100 % at 600 nm, 20 % at 1000 nm and 2 % at 1300 nm.

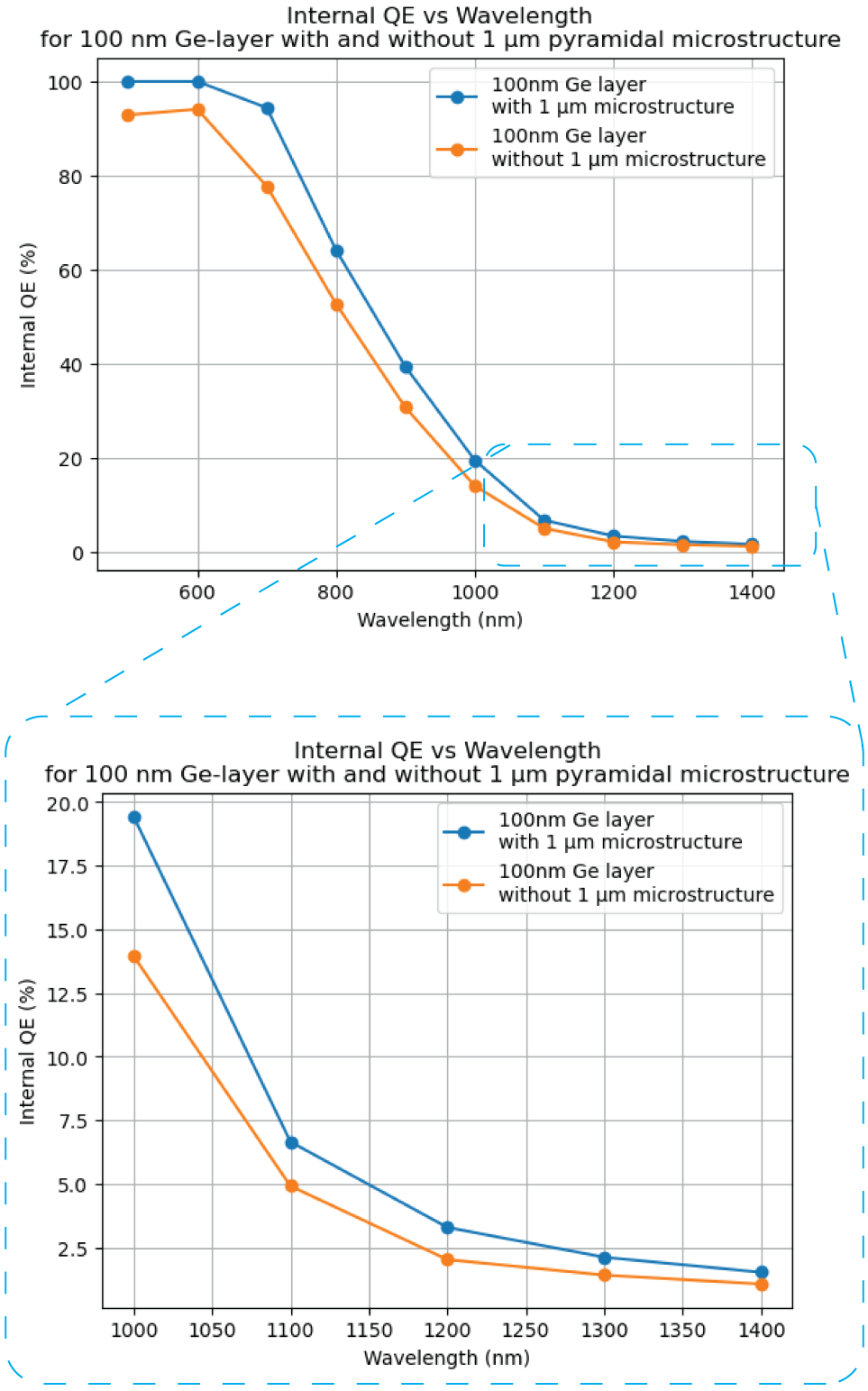


Figure 6.11: QE of complete proposed design with and without 1 µm pyramidal microstructures

6.9. Temporal Simulation and Time Constant

This section presents the temporal simulation of the proposed image sensor design. This determines the response speed of the image sensor, and is an important parameter for high-speed imaging applications. Fig. 6.12 shows a rise time of 10 ns and a fall time of 61.20 ns using light at a wavelength of 1000 nm. Thus, the RC time constant (τ) of the image sensor is 61.20 ns.

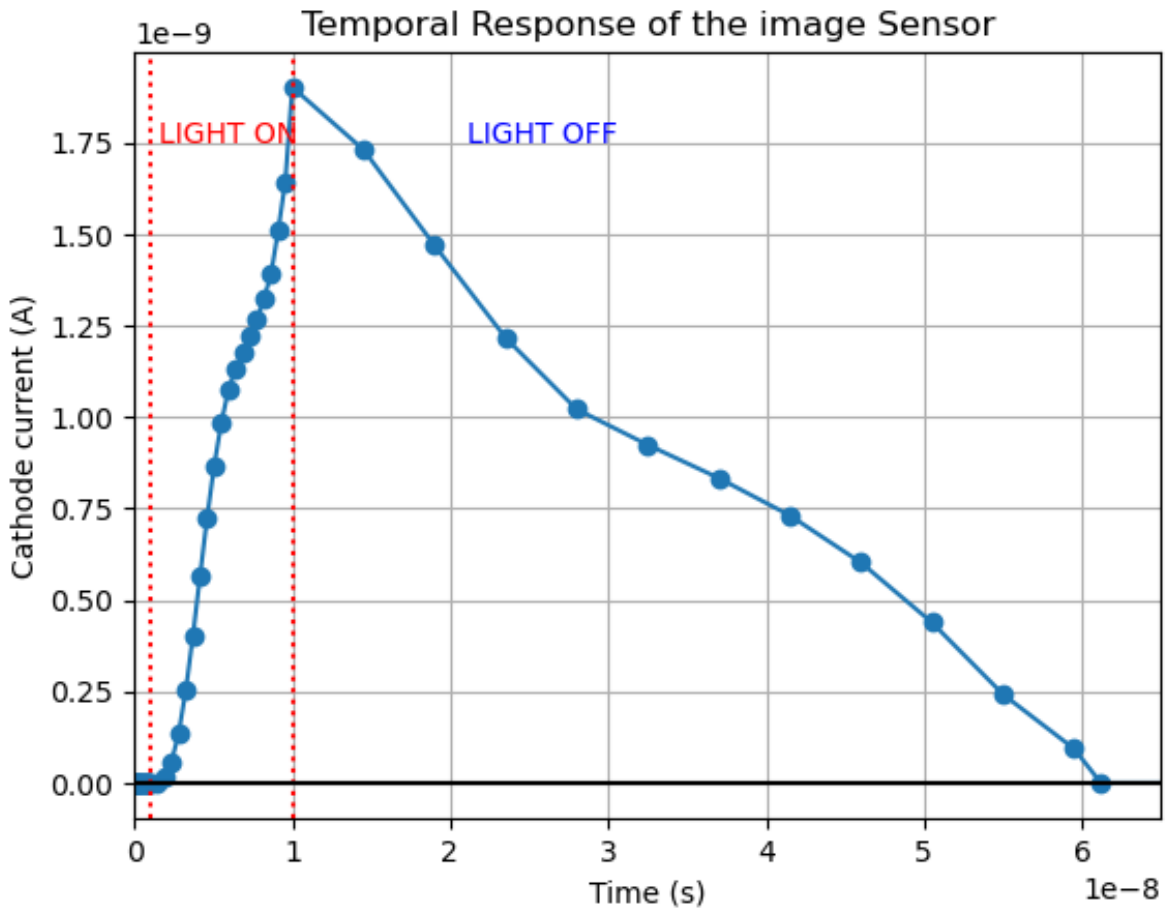


Figure 6.12: Temporal response of the image sensor at light wavelength of 1000 nm

7

Conclusion and Future Recommendations

7.1. Conclusion

The thesis has successfully explored the potential of enhancing CMOS image sensors for NIR/SWIR applications through innovative techniques that bridge the gap between performance and CMOS compatibility. The research began with an extensive literature review, closely examining the fundamental operations, technological advancements, and design considerations that have led to the widespread adoption of CMOS image sensors despite the bandgap limitation of silicon. The literature review and analysis included factors such as bandgap, absorption coefficient, and carrier transport mechanisms, combined with performance parameters such as spectral response and quantum efficiency required for sensor performance evaluations.

A key component of the research was the comparative study of various current NIR/SWIR image sensing technologies. Specialized sensors such as InGaAs and PbS quantum-dot sensors were examined, detailing their respective performance, advantages and limitations. This analysis revealed that despite the excellent NIR/SWIR sensitivity, the fundamental limitations of CMOS incompatibility, complex manufacturing and integration challenges with CMOS read-out integrated circuits made them unsuitable for this widespread wideband imaging applications. Ge-on-Si sensors, on the other hand, showed promise of CMOS-compatibility by addressing current design and fabrication limitations.

Motivated by these findings, this research focused on developing CMOS-compatible wideband solutions with a basis on Ge-on-Si sensors. Two CMOS-compatible NIr/SWIR enhancement techniques were proposed - low-temperature deposition of germanium thin films and light-trapping surface microstructures. The low-temperature deposition allows for the integration of crystalline germanium layers with silicon substrates, crucial for maintaining CMOS compatibility while improving NIR/SWIR sensitivity. The surface microstructuring technique, involving the creation of pyramidal structures, aims to enhance their performance of the low-temperature deposited Ge layer through light absorption and trapping, particularly for longer wavelengths.

Building on these two innovative techniques, a sensor design incorporating a 100 nm thick low-temperature deposited Ge layer combined with 1 µm pyramidal microstructures on the sensor surface was developed. This design aims to enhance NIR/SWIR absorption while maintaining full compatibility with standard CMOS processes and 4T pixel architectures.

Diffusion-Drift and FDTD simulations demonstrated promising results, with QE of 100% at 600 nm, 20% at 1000 nm, and 2% at 1300 nm, along with a time constant of 61.2 ns. While these results show excellent performance in the visible range and significant extension into the NIR region, the QE at longer wavelengths (>1000 nm) requires further improvement before commercial applications are possible. The causes of the performance limitations were identified, and several enhancements were proposed, such as an increase in Ge layer thickness and doping concentration optimisation, as well

as improvement to the microstructure performance through the use of anti-reflective coatings. These advancements highlight the potential for achieving quantum efficiencies over 40% across the spectrum.

Overall, this research represents a critical step towards realising cost-effective, high-performance, wideband CMOS-compatible image sensors. These sensors have the potential to transform various fields requiring advanced imaging capabilities. By overcoming the traditional limitations of silicon-based CMOS sensors, this work opens new possibilities for consumer and industrial applications, including environment imaging, metrology, medical imaging, and beyond, pushing the boundaries of what is achievable in wideband imaging technology. The advancements proposed here are not just incremental improvements but foundational innovations that could redefine the future of image sensing, offering unprecedented capabilities for both current and emerging applications - far beyond the limitations of the human eye.

7.2. Future works and Recommendations

As this report presents an innovative approach to the development of CMOS-compatible wideband sensors using innovative technologies such low-temperature deposition of low-bandgap material and surface micro-structuring, several avenues for future investigation and optimizations have been identified in Chapter 6 to improve the efficiency of the proposed image sensor design:

1. Comparison for post-device characterization and simulation results: As seen in Section 6.5, simulators utilize ideal theoretical models, neglecting several recombination losses which can be measured only through real-world testing. Post-fabrication characterization of the proposed image sensor design was planned as part of this project, with the mask design being completed and fabrication at advanced stages. However, the limited project time did not allow for characterization. Thus, the analysis of theoretical model limitations, particularly for previously unused technologies such as the low-temperature deposition process, through comparison with device characterization results is an area of future research.
2. Optimization of Ge-layer doping profile: The significant deviation between the Beer-Lambert calculations and the SPECTRA simulation results presented in Section 6.6 can potentially be attributed to recombination losses during diffusion through uniformly doped thick Ge layer. A gradient doping profile, with lower doping concentrations near the Ge-Si interface and higher doping concentrations near the sensor surface, would create an electric field pointing towards the sensor's surface, which can stimulate the movement of electrons towards the depletion region and reduce recombination losses. However, losses at the interfaces between Ge regions of different concentrations can lead to recombination losses, which increase with the number of interfaces. Additionally, challenges in the fabrication processes, such as maintaining uniform lateral doping concentrations during low-temperature deposition, must be considered. Thus, research must be performed for doping profile engineering of the Ge layer.
3. Optimization of microstructures: While the current pyramidal microstructures show promise, there is room for further optimization, such as the optimal size for SWIR enhancement beyond wavelengths of 1500 nm. Additionally, the change in optical effects for photodiodes using Ge layers thicker than 1 µm must be investigated. Complex geometries, such as multi-scale structures and embedded nanoscale structures, along with necessary fabrication process optimization allowing large-volume production can also be explored.
4. Integration of Anti-Reflective Coatings: While the surface microstructuring functions as an anti-reflective coating, the use of an anti-reflective material can further improve the absorption in the Ge layer [122]. Fig. 7.1 shows the absorption through 100nm of Ge layer using different thickness of SiO_2 coatings, simulated using the OpenFilters simulation software [123].

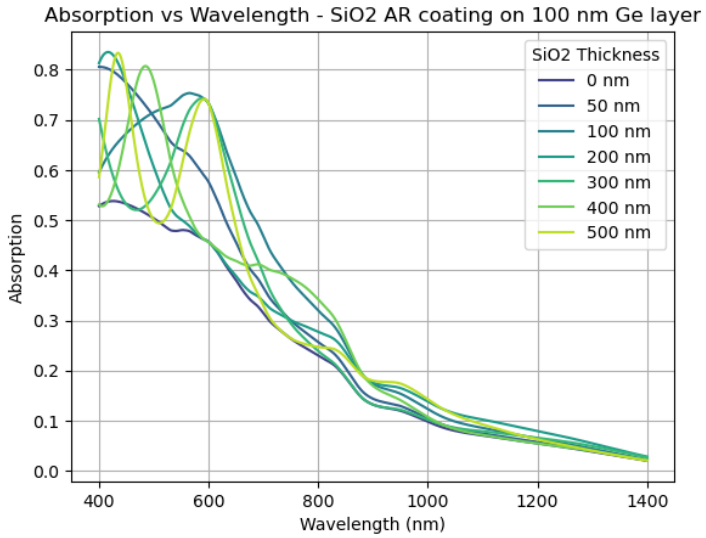


Figure 7.1: OpenFilter simulation of absorption in 100 nm Ge layer with different SiO_2 AR coating thicknesses

Anti-reflective coatings are specific to certain wavelengths and extensive research is required for the design of a visible+NIR/SWIR anti-reflective coating. The use of anti-reflective coatings have a greater impact when used along with a thicker Ge layer, as shows in Fig. 7.2.

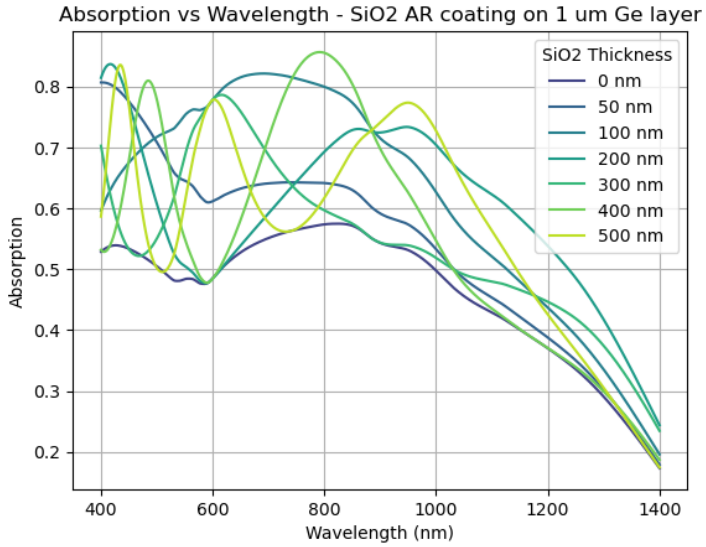


Figure 7.2: OpenFilter simulation of absorption in 1 µm Ge layer with different SiO_2 AR coating thicknesses

5. 4T Pixel Architecture Operation: While the current proposed design is 4T pixel compatible, all simulations performed utilized the 3T pixel architecture. Future works using the proposed NIR/SWIR enhancement techniques can expand the design to include a transfer gate and floating diffusion, thus allowing for 4T pixel operations.

By pursuing these research directions, the field of CMOS-compatible wideband imaging can continue to advance with innovative commercial applications that can bridge the gap between traditional silicon imaging and specialized infrared sensing,

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A

Appendix: Layout

Fig. A.1 shows the layout of the 10 µm and 55 µm pixels used for simulations. 10 µm and 55 µm refers to the dimension of the light-sensitive region of the pixel exposed to light, and used for the calculations of the internal QE of the proposed image sensor design

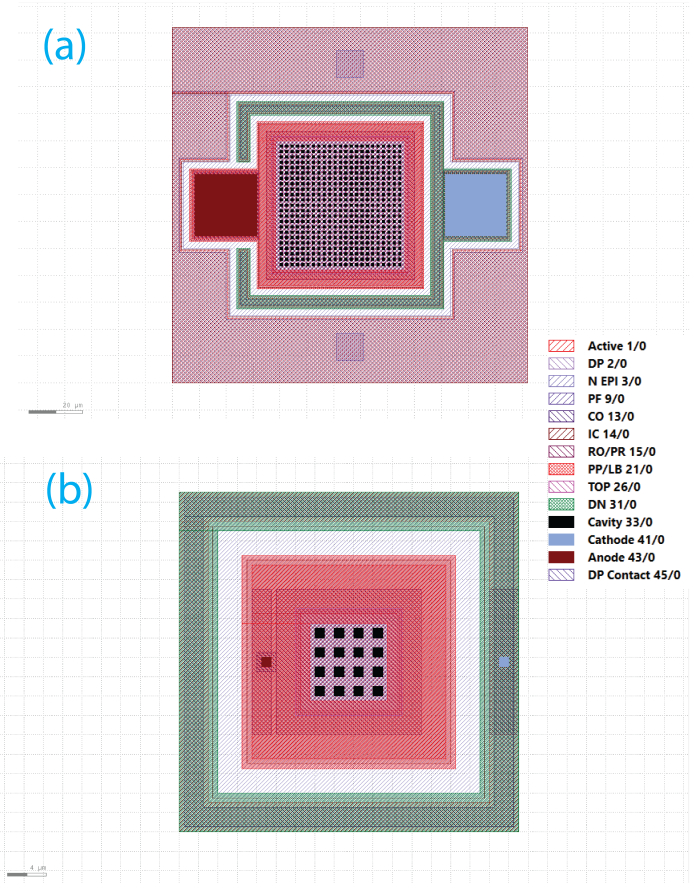

Figure A.1: Layout of the (a) 55 µm and (b) 10 µm pixel. The 55 µm is the true pixel layout consisting of the cathode and anode contact pads and DP boundary barrier. The 10 µm pixel does not contain contact pads or the DP boundary barrier, and instead uses reflective boundary properties within the simulator to mimic the boundary barrier behaviour.