Converter Concepts to Increase the Integration Level

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***Abstract*—In the previous work, a way to improve packaging of power electronic converters by increasing integration level and using multifunctional construction parts is presented. The quantities intended to evaluate integration level and volumetric utilization in power converters are introduced. Based on these values, a number of methods to increase the integration level are presented. A design process in the form of a flow chart that implements these methods in concrete design problems is presented.**

In this paper, the design process is applied to a dc/dc 42/14-V converter for automotive applications. Utilizing commercially available technologies that lend themselves to mass production this design process results in three packaging concepts, namely lead frame converter, printed circuit board embedded converter, and heat conductor converter. These concepts are then compared to a benchmark converter implemented in the conventional, discrete packaging technology. It is shown that by smart use of parts in the converter construction, the high values of integration level and high power densities can be achieved.

***Index Terms*—Heat conductor converter, lead frame converter, power electronic converters, printed circuit board (PCB).**

I. Introduction

THE necessity of changing the present practice of packaging in power electronic converters is widely recognized and reported [1]–[4]. The current practice of dealing with discrete components and assembling them into power electronic circuits has come to the point where it struggles to fulfil the requirements imposed by the higher level system.

At the same time, the demands for power electronics constantly increase [5]–[7]. Due to new electrical features and electrification of mechanical functions the automotive market provides an opportunity for a high volume application of power electronics [8], [9]. However, the requirements on power electronics in automotive applications are very stringent. The automotive market is highly cost-driven which sets boundaries on technologies that can be used for implementation of power electronics. On the other side, the operating environment sets rigorous temperature and size restrictions. In order to meet these rather opposite requirements it is necessary to introduce a new philosophy of constructing power electronic converters.

II. Design Process for High Integration Level

In the previous work [4], a new approach based on looking deeper than the components that we usually assemble with, is introduced. The packaging terminology based on construction parts of power converters is presented. Furthermore, three quantities that describe integration level (K_I, K_P) and volumetric utilization (η_V) in power electronic converters are introduced. A number of techniques to improve packaging and achieve higher integration levels in power electronic converters are presented. Finally, the design process in the form of a flow chart that implements these techniques in concrete designs is given. The reader is referred to this source for in depth explanations. For the sake of clarity the design process flowchart is repeated here in Fig. 1.

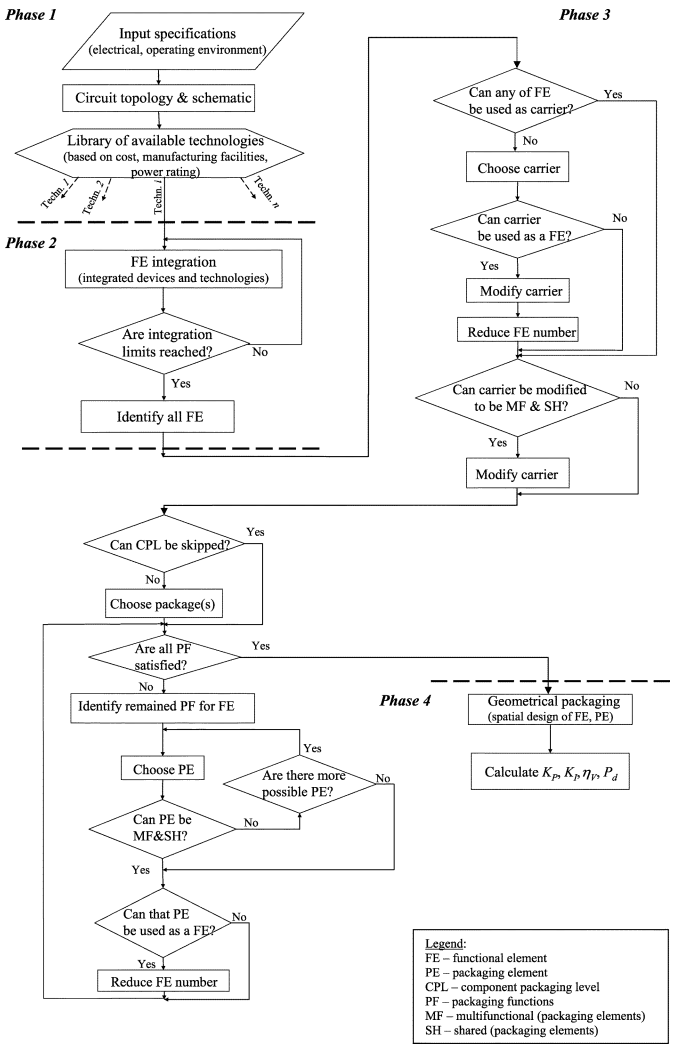

Fig. 1. Design process for improving packaging.

The design process consists of four phases. In the first phase, technologies suitable for the particular application are chosen based on the input specifications (electrical, thermal, volumetric etc.). The second phase deals with integration of functional elements (FEs) (integration technologies and integrated devices) to the point where integration reaches its limits (electromagnetic, manufacturing, economic etc.) for that particular application.

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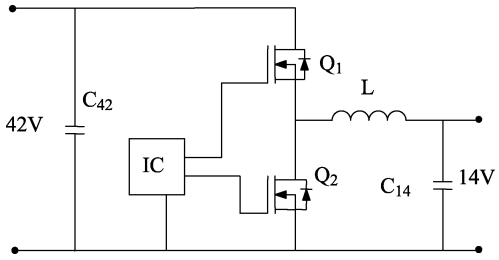

Fig. 2. Converter circuit schematic.

In the third phase, the techniques for packaging elements (PEs) integration are implemented. Finally in the fourth phase, all the designs (coming from different technologies chosen in the first phase) are evaluated and their integration levels and volumetric packaging efficiency are calculated. They are compared to each other and the optimal design is chosen. When evaluating and comparing a number of packaging solutions, a number of different criteria are important. In the previous work a packaging figure-of-merit tree with the root in the ultimate cost-performance criteria is presented [10]. Cost is often the determining criteria in choosing the packaging technology for the particular application. As cost is generally an intangible and complex criteria for a power electronic engineer, the choice is not always optimal. For example, the carrier technology is mostly evaluated by the Euro/cm^2-criteria inherited from the printed circuit board (PCB) market. However, some of the advanced substrate technologies allow for 3-D integration of FEs and can be multifunctional. Therefore, the initial substrate cost might be higher but the component and assembly cost might justify the use of these technologies. Reference [11] gives a comparison of a number of technologies from the cost viewpoint.

The second ultimate criteria, performance, is also influenced by increasing the level of integration. Integration reduces the number of connections which increases the converter reliability. Due to integrating a number of FEs or PEs into one it also brings size reduction and higher power densities as well as reduction of parasitic elements.

III. Novel Concepts

Let us show how the presented design process is implemented in a concrete example. The electrical specifications are dc/dc converter 42/14 V at 15 A for automotive applications. The circuit topology chosen is the synchronous buck topology due to its low number of FEs. Fig. 2 shows the circuit schematic.

The packaging and integration characteristics of new packaging concepts obtained through the design process will be compared to the benchmark converter realized with discrete conventional packaging techniques, namely, discrete through-hole components populated on a double-sided PCB, conventional wire-wound inductor and discrete heat sinking, as shown in Fig. 3. The total number of FEs is nine (as designated in Fig. 3). Each FE performs only one function in the circuit schematic, i.e., $N_{\mathrm{FEv}} = N_{\mathrm{FE}}$ which results in [4]

$$K_I = \frac{\sum_{i=1}^{N_{\mathrm{FE}}} N_{\mathrm{FEv_i}}}{N_{\mathrm{FE}}} = \frac{9}{9} = 1. \tag{1}$$

The total number of PEs is $N_{\mathrm{PE}} = 29$ and they perform following functions.

1) PCB dielectric provides mechanical support and insulation, hence the number of virtual PEs that it represents is $N_{\mathrm{PEv1}} = 2$.
2) PCB copper, conductive vias and input and output connectors provide electrical interconnections $\rightarrow$ $N_{\mathrm{PEv2,3,4,5}} = 1$.
3) MOSFETs and IC wirebonds provide electrical interconnection $\rightarrow$ $N_{\mathrm{PEv6,7,8}} = 1$.
4) MOSFETs leadframes provide electrical interconnection, mechanical support and thermal function $\rightarrow$ $N_{\mathrm{PEv9,10}} = 3$.
5) IC leadframes provide electrical interconnection and mechanical support $N_{\mathrm{PEv11}} = 2$.
6) Bobbin pins and capacitor leads provide mechanical support and electrical interconnection $\rightarrow$ $N_{\mathrm{PEv12}} = 2$ and $N_{\mathrm{PEv13,14,15,16}} = 2$.
7) Bobbin mechanically supports the core $\rightarrow$ $N_{\mathrm{PEv17}} = 1$.
8) MOSFETs and IC cases provide protection $\rightarrow$ $N_{\mathrm{PEv18,19,20}} = 1$.
9) Insulation for inductor wire $\rightarrow$ $N_{\mathrm{PEv21}} = 1$.
10) Capacitor cases provide protection $\rightarrow$ $N_{\mathrm{PEv22,23,24,25}} = 1$ and the insulating paper in electrolytic capacitors provides insulation $\rightarrow$ $N_{\mathrm{PEv26,27,28,29}} = 1$.

From [4] follows (2) shown at the bottom of the page. The integration level, both FEs and PEs, is rather low in this case,

$$\begin{aligned} K_P &= \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} \\ &= \frac{N_{\mathrm{PE_{V1}}}\langle \text{PCBdiel.}\rangle + N_{\mathrm{PE_{V2}}}\langle \text{ PCB copper}\rangle + N_{\mathrm{PE_{V3}}}\langle \text{vias}\rangle + N_{\mathrm{PE_{V4,5}}}\langle \text{ connectors}\rangle + N_{\mathrm{PE_{V6,7,8}}}\langle \text{ wirebonds}\rangle}{N_{\mathrm{PE}}} \\ &\quad + \frac{N_{\mathrm{PE_{V9,10,11}}}\langle \text{leadframes}\rangle + N_{\mathrm{PE_{V12,13}}}\langle \text{ slugs}\rangle + N_{\mathrm{PE_{V14,15,16,17,18}}}\langle \text{ pins, leads}\rangle + N_{\mathrm{PE_{V19}}}\langle \text{bobbin}\rangle + N_{\mathrm{PE_{V20,21,22}}}\langle \text{cases}\rangle}{N_{\mathrm{PE}}} \\ &\quad + \frac{N_{\mathrm{PE_{V23}}}\langle \text{wire insul.}\rangle + N_{\mathrm{PE_{V24,25,26,27}}}\langle \text{ pins, leads}\rangle + N_{\mathrm{PE_{V28,29,30,31}}}\langle \text{pins, leads}\rangle}{N_{\mathrm{PE}}} \\ &= \frac{40}{29} \\ &= 1.38. \end{aligned} \tag{2}$$

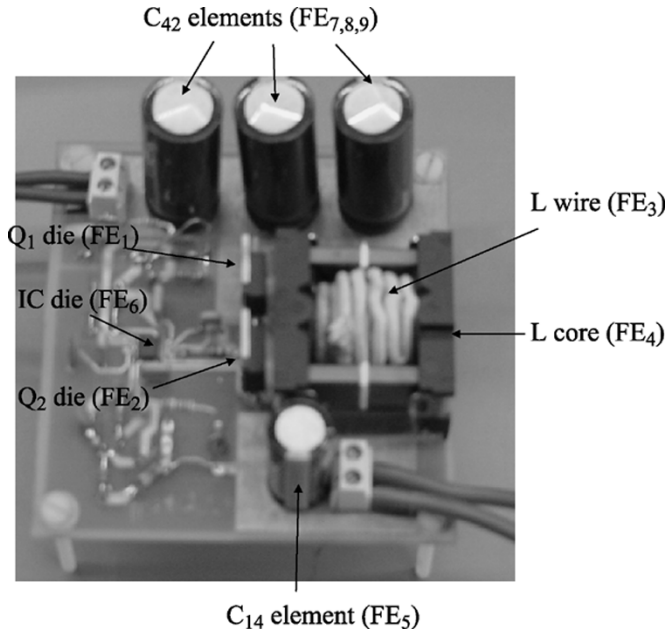

Fig. 3. Discrete benchmark converter.

due to a large number of construction parts in the discrete components. Let us go through the proposed design process in order to come up with designs with higher level of FEs and PEs integration.

As indicated in Fig. 1, the first phase consists of making a library of technologies suitable for this application. Taking into account the discussion on the requirements in automotive applications, the commercially available technologies that lend themselves to mass production are chosen. To illustrate the process, we have chosen three technologies: moulded interconnect technology, multilayer PCB technology, and copper-on-ceramic technology together with their characteristics such as possible interconnect techniques, manufacturing processes etc. By going through the design process for each of these technologies we will end up with three packaging solutions that will be evaluated and compared to each other.

Beside the three chosen, there are a number of other technologies that allow for higher integration level. A large number of parts in discrete heat sinking can be reduced by using insulated metal substrates (IMS) [12]. This substrate also allows for bare die attachment of power semiconductors further reducing a number of total PEs. Due to its cost lead over ceramic substrates and mechanical ruggedness it allows for using a single substrate for both power and control circuitry. On the other side, the ceramic based technologies, such as thick film and low temperature co-fired ceramic (LTCC) [13] allow for integration of passives increasing level of FEs integration. Furthermore, the thermal management can be integrated in the FE such as micro heat pipes on silicon [14], again reducing number of PEs. Advanced planar interconnection technologies, such as embedded power, flip-chip on flex, dimple array [15] allow for double sided cooling, three-dimensional (3–D) spatial integration and higher power densities.

A. Lead Frame Converter

1) Design and Technologies: The moulded interconnect technology does not lend itself to integration technologies of FEs. Looking at the circuit schematic, due to the topology simplicity the possibility for integrated devices can only be realized through the output LC filter. We assume that integration of power semiconductors and control integrated circuit is not viable in this case due to the cost issue of different manufacturing technologies. That means that we have come to the point where the integration limits are reached. Identified FEs at this stage are: two power semiconductor dies, IC chip, capacitive elements for C_{42} and C_{14}, an inductor wire and a FE for magnetic field shaping for L.

A stamped net of electrical conductors referred to as lead frame is chosen to be a carrier. Lead frame, a thin layer of metal that connects the wiring from tiny electrical terminals on the semiconductor surface to the large-scale circuitry is extensively used in semiconductor packages. It has also been used as a base substrate for commercial power modules in low power range incorporating power semiconductors and part of the control circuitry in the same package [16]. Here, we take the concept further and exploit the lead frame functionality even more. Now the whole converter, including the passive components can be populated on a lead frame. In this manner, a simple and effective construction with few parts and manufacturing steps can be achieved. This carrier can be utilized to implement one FE, namely inductor windings so they are manufactured in one process and the number of FEs is reduced. The lead frame can be used for mechanical support as well as electrical interconnections, provided that its thickness is sufficient to carry the current and support the circuitry. It can also be used to conduct the heat from the MOSFETs. The component packaging level could be skipped since both MOSFETs and IC can be mounted in bare die form. Also, unleaded bare metallized film capacitors [17] can be used as capacitive FEs for C_{14} and C_{42}. At this point not all the packaging functions are satisfied, namely thermal packaging function for the MOSFETs, electrical connections of the MOSFET's pads to the rest of the circuitry, mechanical support to hold the assembly together, protection of the MOSFET's bare dies and the whole circuitry. Going through the loop in the flow chart, the remaining packaging functions are implemented. For the electrical connections of the MOSFETs the wire bonding process is chosen. For the heat removal from the MOSFETs an aluminum block is placed underneath both MOSFETs. For the protection and mechanical support, the whole assembly can be encapsulated by a moulding process. This moulding part can provide magnetic field shaper in the form of the commercially available ferrite polymer composite (FPC) material [18]. The number of FEs is once again reduced. As the inductance can be realized with no extra FEs (the winding is part of the lead frame and the magnetic field shaper is part of the moulding process) the option of integrating of the output filter is discarded. Again, checking if all the functions are satisfied, it can be seen that if the aluminum block is directly connected to the lead frame underneath the MOSFETs, the MOSFETs are not insulated from the heat sink. To make this layer thermally conductive, a thermally conductive electrically insulating material such as Kapton [19] is chosen.

In phase 4, the spatial layout and component design is performed. The desired inductance value determines the spatial design of the lead frame. The space underneath the lead frame can be used to place low profile metallized film capacitors. The design concept is shown in Figs. 4–6.

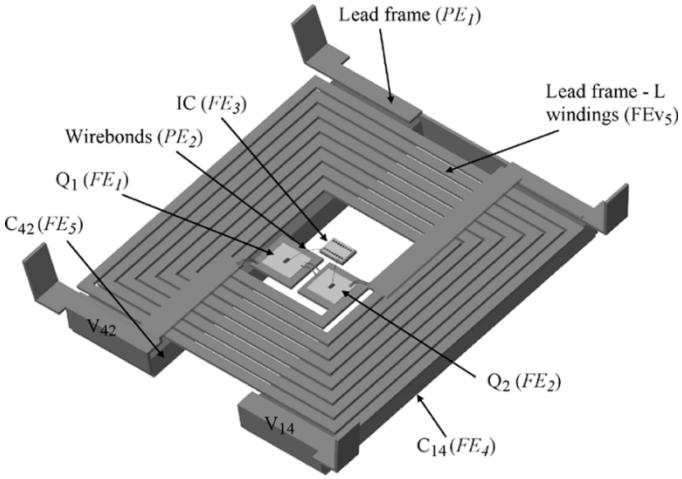

Fig. 4. Multifunctional lead frame populated with components.

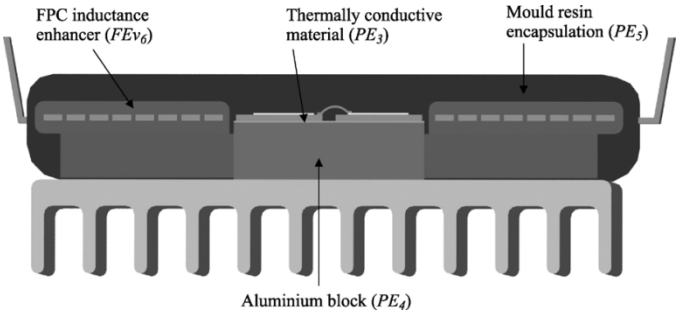

Fig. 5. Converter's vertical cross section.

A few issues regarding the performance of this converter design are to be noted. The interconnections are done by means of wire bonding, which brings up the reliability matter. Furthermore, due to the inductor design and the low magnetic permeability of the FPC material ($\sim$17) a part of the magnetic field will pass in the area where the sensitive control circuitry is placed, which might cause problems in the functioning of the control and gate drive IC. This is still to be investigated.

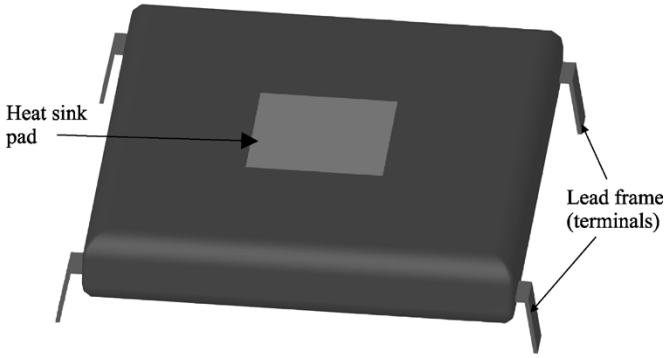

Fig. 6. Moulded encapsulation for protection and mechanical support.

2) Integration Level: The functional and PEs are identified in Fig. 4. The total number of FEs is $N_{\mathrm{FE}} = 5$. Each of them participates in only one function in the circuit schematic which contributes with five virtual FEs. In addition, there are two PEs that serve as FEs—lead frame as inductor winding and FPC mould as the magnetic field shaper (this is an example of functional and PEs duality), which gives the total number of virtual FEs $N_{\mathrm{FEv}} = 7$. From [4] follows (3) shown at the bottom of the page. As for K_P, the PEs are identified in Fig. 4 and Fig. 5. The total number of PEs is $N_{\mathrm{PE}} = 5$. The lead frame performs three functions: electrical interconnection, mechanical support and thermal, therefore $N_{\mathrm{PEv1}} = 3$; the wirebonds perform only electrical function therefore $N_{\mathrm{PEv2}} = 1$; the thermally conductive layer provides insulation and thermal function, $N_{\mathrm{PEv3}} = 2$; the aluminum block performs the thermal conduction function and mechanical support, $N_{\mathrm{PEv4}} = 2$ and finally, the encapsulation mould provides mechanical support and protection, $N_{\mathrm{PEv5}} = 2$. From [4] one can obtain (4) shown at the bottom of the page.

B. PCB Embedded Converter

1) Design and Technologies: Concerning FEs integration, similar reasoning to the previous case can be applied here. The output LC filter can be integrated into one device. By modifying

$$\begin{aligned} K_I &= \frac{\sum N_{\mathrm{FE_{vi}}}}{N_{\mathrm{FE}}} \\ &= \frac{N_{\mathrm{FE_{V_1}}}\langle \mathrm{Q_1}\rangle + N_{\mathrm{FE_{V_2}}}\langle \mathrm{Q_2}\rangle + N_{\mathrm{FE_{V_3}}}\langle \mathrm{IC}\rangle + N_{\mathrm{FE_{V_4}}}\langle \mathrm{C_{14}}\rangle + N_{\mathrm{FE_{V_5}}}\langle \mathrm{C_{42}}\rangle + N_{\mathrm{FE_{V_6}}}\langle \text{leadframe L}\rangle + N_{\mathrm{FE_{V_7}}}\langle \text{FPC mould}\rangle}{N_{\mathrm{FE}}} \\ &= \frac{7}{5} \\ &= 1.4 \end{aligned} \tag{3}$$

$$\begin{aligned} K_P &= \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} \\ &= \frac{N_{\mathrm{PE_{V1}}}\langle \text{leadframe}\rangle + N_{\mathrm{PE_{V2}}}\langle \text{wirebonds}\rangle + N_{\mathrm{PE_{V3}}}\langle \text{thermalepoxy}\rangle + N_{\mathrm{PE_{V4}}}\langle \text{al. block}\rangle + N_{\mathrm{PE_{V5}}}\langle \text{encaps.}\rangle}{N_{\mathrm{PE}}} \\ &= \frac{10}{5} \\ &= 2 \end{aligned} \tag{4}$$

certain properties of the carrier which is a multilayer PCB in this case, it can be used as one or more FEs, i.e., by enhancing dielectric constant of a number of layers, those layers can be used as capacitive dielectric [20] elements and layers with high magnetic permeability layers can be used as magnetic FEs [21]. PCB tracks can be used as the conductors for the integrated LC filter. A layer of PCB compatible material with enhanced magnetic permeability—MagLam [22] can be used to close the magnetic field on the bottom side of the PCB. This reduces the number of FEs. Electromagnetically integrated passive components, such as output filter in this case, are well documented in the literature, the design methods are available and their electrical performance is favorable or comparable to their discrete equivalents [23]–[25].

The PCB carrier is multifunctional, performs mechanical support and electrical interconnection but can be used for thermal function as well, i.e., the copper conductors underneath the MOSFETs can be used for heat spreading. Components packaging level can not be skipped, i.e., the power MOSFETs can not be used in bare die form, due to the mechanical and thermal characteristics of the standard PCB. Both the power MOSFETs and control IC can be used in SMD or Through-hole form, it is yet to be determined. As for the input capacitive element, either an electrolytic or metal film capacitor can be used, which will also be determined later on. All the packaging functions are not satisfied at this point, namely the thermal conduction function and the electrical interconnection to the outside. One solution would be to have discrete heat sinks for MOSFETs. Another PE that can be shared between all FEs is using thermal vias to conduct the heat from the top surface of the PCB to the heat sink on the bottom side. The total thermal resistance through the PCB is equivalent to the thermal resistance of the PCB in parallel with the thermal resistance of the vias [26]. In this case, 16 solder filled vias underneath the MOSFET will reduce the thermal resistance through the PCB more than six times [27]. Finally, the electrical interconnections to the outside are performed by two connectors.

Now we come to the geometrical packaging step. For the semiconductors, SMD packages are chosen in order to keep the bottom side of the PCB flat, and due to their smaller size. For the input capacitive FE, we choose an electrolytic capacitor that can be mounted flat beside the PCB.

2) Integration Level: Let us calculate the K_I and K_P values. The FEs are identified in Fig. 7. The total number of FEs is $N_{\mathrm{FE}} = 5$. Each of them participates in only one function in the circuit schematic which contributes with five virtual FEs. In addition, the capacitive laminate layers serve as dielectric in the output LC filter, $N_{\mathrm{FEv6}} = 1$; copper tracks serve as inductor windings and capacitive electrodes in LC filter, $N_{\mathrm{FEv7}} = 2$;

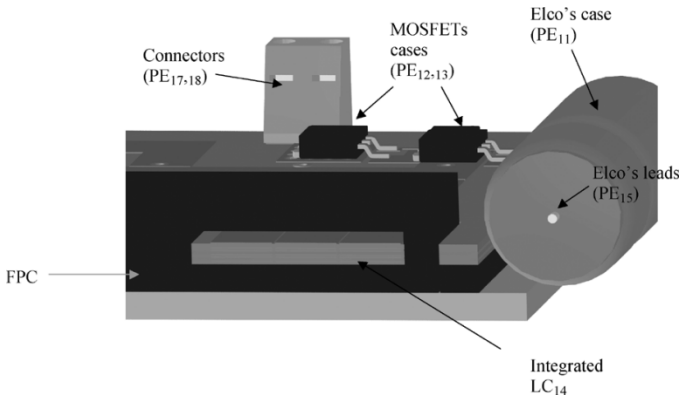

Fig. 7. Embedded capacitors and integrated LC filter.

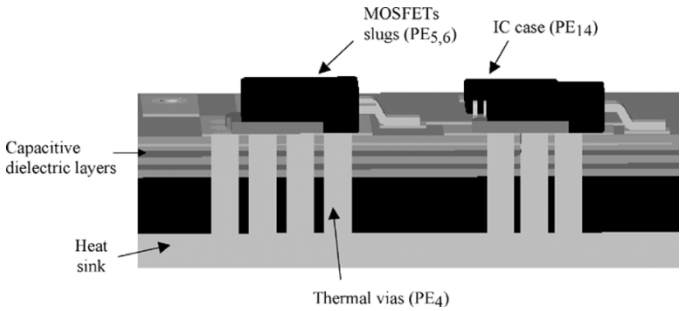

Fig. 8. Built-in heat sink.

and FPC material serves as magnetic field shaper, $N_{\mathrm{FEv8}} = 1$, which gives the total number of virtual FEs of $N_{\mathrm{FEv}} = 9$. From [4] follows (5) as shown at the bottom of the page. The total number of PEs is $N_{\mathrm{PE}} = 18$. The PCB dielectric performs mechanical support, thermal and insulation function, $N_{\mathrm{PEv1}} = 3$; the PCB copper performs electrical interconnection and thermal function, $N_{\mathrm{PEv2}} = 2$; conductive vias perform electrical interconnection, $N_{\mathrm{PEv3}} = 1$; thermal vias perform thermal packaging function, $N_{\mathrm{PEv4}} = 1$; the MOSFETs and IC leadframes provide electrical interconnection, heat removal and mechanical support, $N_{\mathrm{PEv5,6,7}} = 3$; the MOSFETs and IC wirebonds provide electrical interconnection $N_{\mathrm{PEv8,9,10}} = 1$; C_{42} capacitor, MOSFETs and ICs cases provide protection $N_{\mathrm{PEv11,12,13,14}} = 1$; C_{42} leads provide electrical interconnection and mechanical support, $N_{\mathrm{PEv15}} = 2$; the separating paper in C_{42} has insulating function, $N_{\mathrm{PEv16}} = 1$ and finally the input and output connectors provide electrical interconnection function, $N_{\mathrm{PEv17,18}} = 1$ (see Fig. 8). The total number of

$$
\begin{aligned}
K_I &= \frac{N_{\mathrm{FE_{V_1}}}\langle \mathrm{Q_1\ die}\rangle + N_{\mathrm{FE_{V_2}}}\langle \mathrm{Q_2\ die}\rangle + N_{\mathrm{FE_{V_3}}}\langle \mathrm{IC\ \ die}\rangle + N_{\mathrm{FE_{V_4}}}\langle \mathrm{C_{42}}\rangle + N_{\mathrm{FE_{V_5}}}\langle \text{ core}\rangle + N_{\mathrm{FE_{V_5}}}\langle \text{ cap. lam.}\rangle}{N_{\mathrm{FE}}} \\
&\quad + \frac{N_{\mathrm{FE_{V_6}}}\langle \mathrm{FPC\ \ lam.}\rangle + N_{\mathrm{FE_{V_7}}}\langle \text{ PCB copper}\rangle}{N_{\mathrm{FE}}} \\
&= \frac{9}{5} \\
&= 1.8
\end{aligned}
\tag{5}
$$

virtual PEs is then $N_{\mathrm{PEv}} = \sum N_{\mathrm{PEvi}} = 32$ and shown as (6) at the bottom of the page.

C. Heat Conductor Converter

1) Design and Technologies: The copper-on-ceramic is the base technology for this design. There are no integration technologies compatible with this base technology. The FEs at this point in the process are: two power semiconductor dies, IC chip, capacitive elements for C_{42} and C_{14}, an inductor wire and a FE for magnetic field shaping for L. The ceramic is used as the carrier. It is multifunctional, provides mechanical support, electrical interconnection and heat conduction. The component packaging level could be skipped or the semiconductor devices can be used in SMD form. Not all the packaging functions are satisfied at this point, namely heat conduction, mechanical support for the ceramic and electrical interconnections to the outside. A thick conductor busbar can be used to take the heat from all the FEs and deliver it to the heat sink and mechanically support the ceramic substrate. It can also be used as the 14-V electrical interconnection and one turn of the inductor winding. For the other two outside power connections, copper busbars can be used. The remained packaging function is the insulation from the electro-thermal busbar to the heat sink and can be performed by a layer of thermally insulating material.

A low profile planar E–I core is used for the magnetic FE. Low profile metallized capacitors can be used for input and output filtering and be placed underneath the substrate as shown in Fig. 9 for high volumetric efficiency and power density.

This converter design allows for using one carrier for both the control and power circuitry. The sensitive nodes of the control circuitry are in the vicinity of the power tracks which might cause problems in functioning of the control circuitry. Furthermore, the two parts of the inductor winding separated by the ceramic carrier will introduce an interwinding capacitance. The common mode capacitance between the drain of the low side MOSFET and the heat sink will affect the EMI performance of the converter. These issues are to be looked at.

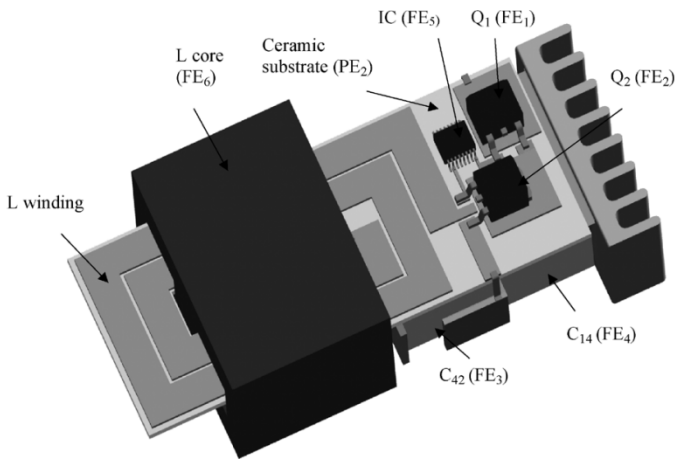

Fig. 9. Converter on ceramic substrate—top view.

2) Integration Level: The FEs are identified in Fig. 9. The total number of FEs is $N_{\mathrm{FE}} = 6$. Each of them participates in only one function in the circuit schematic which contributes with six virtual FEs $N_{\mathrm{FEvi(i=1..6)}} = 1$. In addition, the copper tracks on ceramic serve as the inductor winding which gives the total number of virtual FEs $N_{\mathrm{FEv}} = 7$. From [4] follows (7) as shown at the bottom of the page. Most of the PEs are identified in Figs. 9 and 10. The MOSFETs and IC PEs are not marked for clarity reasons. The total number of PEs is $N_{\mathrm{PE}} = 15$. The copper bus bars provide three functions: mechanical support and thermal function (electro-thermal bus bar) and electrical interconnection (all the busbars), hence, $N_{\mathrm{PEv1}} = 3$, the ceramic substrate provides mechanical support, thermal and insulating function, $N_{\mathrm{PEv2}} = 3$, the copper-on-ceramic provides

$$
\begin{aligned}
K_P &= \frac{\sum N_{\mathrm{PE_{vj}}}}{N_{\mathrm{PE}}} \\
&= \frac{N_{\mathrm{PEv_1}}\langle \text{ PCB diel.}\rangle + N_{\mathrm{PEv_2}}\langle \text{ PCB copper}\rangle + N_{\mathrm{PEv_3}}\langle \text{cond.vias}\rangle + N_{\mathrm{PEv_4}}\langle \text{ therm.vias}\rangle + N_{\mathrm{PEv_{5,6,7}}}\langle \text{leadframe}\rangle}{N_{\mathrm{PE}}} \\
&\quad + \frac{N_{\mathrm{PEv_{8,9,10}}}\langle \text{wirebonds}\rangle + N_{\mathrm{PEv_{11,12}}}\langle \text{slugs}\rangle + N_{\mathrm{PEv_{13,14,15,16}}}\langle \text{ case}\rangle + N_{\mathrm{PEv_{17}}}\langle \text{leads}\rangle + N_{\mathrm{PEv_{18}}}\langle \text{ paper}\rangle}{N_{\mathrm{PE}}} \\
&\quad + \frac{N_{\mathrm{PEv_{19,20}}}\langle \text{conn.}\rangle}{N_{\mathrm{PE}}} \\
&= \frac{28}{18} \\
&= 1.56
\end{aligned} \tag{6}
$$

$$
\begin{aligned}
K_I &= \frac{\sum N_{\mathrm{FEv_i}}}{N_{\mathrm{FE}}} \\
&= \frac{N_{\mathrm{FEv_1}}\langle \mathrm{Q_1} \text{ die}\rangle + N_{\mathrm{FEv_2}}\langle \mathrm{Q_2} \text{ die}\rangle + N_{\mathrm{FEv_3}}\langle \mathrm{C_{42}}\rangle + N_{\mathrm{FEv_4}}\langle \mathrm{C_{14}}\rangle + N_{\mathrm{FEv_5}}\langle \text{ IC die}\rangle}{N_{\mathrm{FE}}} \\
&\quad + \frac{N_{\mathrm{FEv_6}}\langle \text{core}\rangle + N_{\mathrm{FEv_7}}\langle \text{L wind.}\rangle}{N_{\mathrm{FE}}} \\
&= \frac{7}{6} \\
&= 1.17
\end{aligned} \tag{7}
$$

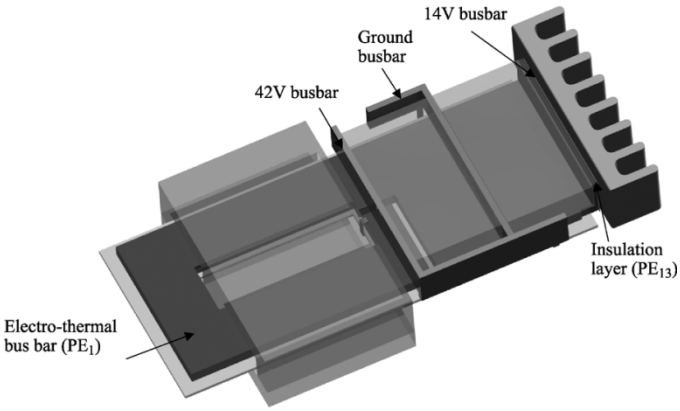

Fig. 10. Electro-thermal bus bar.

TABLE I
PACKAGING AND INTEGRATION CHARACTERISTICS OF THE PROPOSED CONCEPTS

Parameter	Description	Benchmark	Proposed designs		
		Discrete converter	Lead frame converter	PCB converter	Heat conductor converter
N_{FE}	Total number of functional elements in a converter	9	5	5	6
N_{FEv}	Virtual number of functional elements	9	7	9	7
N_{PE}	Total number of packaging elements in a converter	29	5	18	15
N_{PEv}	Virtual number of packaging elements	40	10	28	27
K_I	Functional elements integration level	1	1.4	1.8	1.17
K_P	Packaging elements integration level	1.38	2	1.56	1.8
η_v (%)	Volumetric packaging efficiency	16.4	44.2	43.2	47
Pd (W/in3)	Power density	13.9	53.1	41.8	113.9

electrical interconnection and thermal function, $N_{\mathrm{PEv3}} = 2$, the MOSFETs and IC leadframes provide electrical interconnection, mechanical support and thermal function, $N_{\mathrm{PEv4,5,6}} = 3$, the MOSFETs and IC wirebonds provide electrical interconnection $N_{\mathrm{PEv7,8,9}} = 1$; the MOSFETs and ICs cases provide protection $N_{\mathrm{PEv10,11,12}} = 1$; the thermally conductive insulation layer provides thermal and insulating function $N_{\mathrm{PEv13}} = 2$, the electrically conductive glue between the ceramic and the thermal busbar performs mechanical connection $N_{\mathrm{PEv14}} = 1$ and the metal tabs provide electrical interconnection between the conductor-on-ceramic and busbars $N_{\mathrm{PEv15}} = 1$. Therefore, the level of PEs integration is shown as (8) at the bottom of the page.

D. Packaging Evaluation of Proposed Concepts

Table I shows the values of functional and PEs integration level, volumetric packaging efficiency of the proposed designs, and the benchmark discrete converter. The estimated values of power density are also shown. It can be noticed that regarding FEs integration, the PCB converter achieves the highest level of the four converters, due to its integrated LC filter and embedded capacitance. As for the PEs integration level , the lead frame converter is by far superior due to the multifunctionality of the lead frame.

The PEs integration level of the PCB converter is close to the benchmark version due to the fact that packaged components are used. The heat conductor converter has the highest value of volumetric packaging efficiency which indicates that the converter volume is used more efficiently than in the other concepts. This is mainly due to the electro-thermal bus bar. Furthermore, this concept exhibits by far the highest power density. One reason for this is the good thermal management that the common heat conductor ensures. Another reason is the way that the magnetic component is realized in the different converters. In the Lead frame converter, the required number of turns for an enhanced air core inductor results in a somewhat larger volume. A similar situation can be found in the PCB converter due to the low permeability of the FPC magnetic material.

It is important to note that the evaluation of packaging and integration characteristics of the novel concepts does not include the passive control components. The reason for this is that the primary intention was to investigate the packaging characteristics of the power part of the circuitry. Furthermore, it is possible to implement these small control passives in literally any technology without significantly influencing the volume or manufacturing complexity. Thus, in the PCB embedded converter they can be embedded in the PCB or mounted in SMD form. In the Heat conductor converter the SMD form is the most feasible choice. In the Lead frame converter, these components can be integrated on a separate substrate in different integration technologies (thick film, LTCC) thus increasing the overall integration level.

IV. CONCLUSION

In this paper, the design process for improved packaging of power electronic converters is performed on a dc–dc 42/14-V converter for dual automotive powernet applications. It results in three packaging concepts that come from the technologies chosen as suitable for this application. As shown in the paper, these concepts exhibit higher level of packaging and functional integration compared to the discrete benchmark due to the multifunctional use of PEs and integration of FEs. They also exhibit increased volumetric packaging efficiency due to the improved geometrical packaging and fewer PEs. At the same time they use commercially available technologies that lend themselves to

$$
\begin{aligned}
K_P &= \frac{\sum N_{\mathrm{PEv_j}}}{N_{\mathrm{PE}}} \\
&= \frac{N_{\mathrm{PEv_1}}\langle \mathrm{busbar}\rangle + N_{\mathrm{PEv_2}}\langle \mathrm{cer.subst.}\rangle + N_{\mathrm{PEv_3}}\langle \mathrm{copper}\rangle + N_{\mathrm{PEv_{4,5,6}}}\langle \mathrm{leadframes}\rangle + N_{\mathrm{PEv_{7,8,9}}}\langle \mathrm{wirebonds}\rangle}{N_{\mathrm{PE}}} \\
&\quad + \frac{N_{\mathrm{PEv_{10,11}}}\langle \mathrm{slugs}\rangle + N_{\mathrm{PEv_{12,13,14}}}\langle \mathrm{cases}\rangle + N_{\mathrm{PEv_{15}}}\langle \mathrm{insul.layer}\rangle}{N_{\mathrm{PE}}} \\
&= \frac{27}{15} \\
&= 1.8
\end{aligned} \tag{8}
$$

mass production. Since they employ technology platforms used in the lower power range, a number of these modules can be connected in parallel in order to achieve the desired power rating. The design process illustrated in the paper can be applied to any application, regardless of the specific nature and requirements.

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