A Low Input-Current Chopper Amplifier

By

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A thesis submitted in partial fulfillment for the

Degree of Master of Science

In

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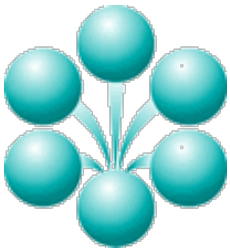

March 2012

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Abstract

Faculty of Electrical Engineering, Mathematics and Computer Science
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This thesis describes the implementation of a low input-current chopper amplifier. Chopper amplifiers are attractive in applications where high DC precision is required, due to their low offset, drift & *1/f* noise. They are generally used in the analog signal chain to boost weak sensor signals and buffer them to an analog-to-digital converter. Till recent years, research related to chopper amplifiers has focused on techniques to reduce their low frequency voltage errors and exploring effective techniques to suppress chopper-ripple. A superior performance on both these fronts has been achieved. However, at the cost of significantly large input currents (>100pA) and input current noise (>100fA/$\sqrt{Hz}$), thus limiting their usage to sensors with low source impedance (<10kΩ).

In this work, a novel input-chopper architecture is proposed, implemented and measured. It achieves a 2.5X improvement in input-current compared to the state-of-the-art in chopper amplifiers with a single-point trim. The proposed technique also reduces the common mode variation of the input current to 4.5pA/V, which is an indication of a high common mode rejection ratio in a high source impedance (>1MΩ) application.

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1 Introduction

This thesis describes the theory, design and realization of a technique for reducing the input current of a chopper op-amp, so as to achieve higher DC precision in the current domain.

In this chapter, an introduction to precision CMOS amplifier techniques like auto zeroing and chopping is given followed by a description of motivation and objectives for this work.

Further, a description of current domain errors in a chopper amplifier is provided. The state-of-the-art in chopper op-amps is then discussed, which leads to target specifications for this work.

1.1 Precision CMOS amplifier techniques

Standard CMOS amplifiers suffer from low frequency errors such as 1/*f* noise, drift and DC offset [1.1]. The low frequency behavior of a typical CMOS amplifier is shown in Figure 1.

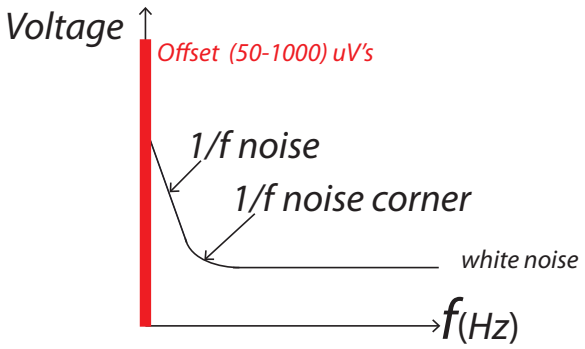

Figure 1. Low frequency behavior of a CMOS amplifier.

The offset in CMOS amplifiers is a DC error due to lithographic errors and variation in doping concentrations [1.2], while *1/f* noise is a type of noise, whose energy is concentrated at low frequencies (<10kHz). Its energy content at any given frequency is inversely proportional to the frequency up until a certain *1/f* noise corner (up to 10 kHz in CMOS amplifiers). The origin of this noise is due to charge trapping in the gate oxide of MOS transistors. There are two commonly used techniques for reducing 1/*f* noise and DC offset in a CMOS amplifier: (a) chopping, and (b) auto zeroing. The underlying principles of these so called dynamic offset cancellation techniques will be briefly reviewed along with the pros and cons of each approach.

1.1.1 Auto-zero amplifiers

The auto-zeroing technique is based on sampling the offset and then subtracting it from the main amplifier(G_1), thereby cancelling the offset, as shown in Figure 2. The low frequency 1/*f* noise and drift are also cancelled in the same way as offset.

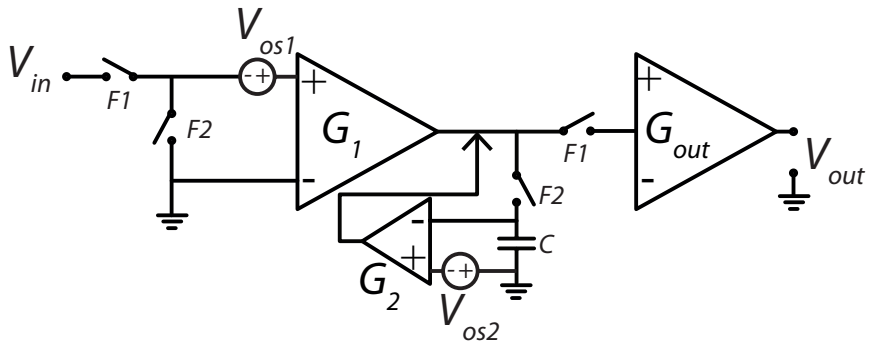

Figure 2. An auto zero amplifier

It works in two phases: the sampling phase and the gain phase. The amplifier's offset (V_{os1}) is sampled on the capacitor (C) during the sampling phase, and during this time, the amplifier cannot be used. In the gain phase, the signal is amplified and offset is subtracted at the output of the amplifier (G_1). Therefore, it is not possible to use an auto-zero amplifier in a continuous time application. However, a Ping-Pong topology where one amplifier is amplifying while the other amplifier is sampling the offset can be used to achieve quasi-continuous operation, but this leads to additional power consumption and chip area [1.3].

The main drawbacks of auto zeroing are that:

- It is not possible to use an auto-zero amplifier in a continuous time application without additional power penalty involved in using a Ping-Pong topology.
- Due to the sampling, some of the amplifier's thermal noise is folded back into the signal band. This causes an increase in the thermal noise floor of an auto-zeroed amplifier (Figure 4).

Therefore, auto-zeroing is not a power efficient technique when very low noise is desired by the application.

1.1.2 Chopper amplifiers

Chopping is a dynamic technique that works by modulating the offset and 1/*f* noise to a chopping frequency (f_{ch}) outside the band of interest. The chopper at the input (CH_1) of the amplifier modulates the signal to the chopping frequency (Figure 3(a)). The chopping frequency (f_{ch}) is usually chosen to be greater than the 1/*f* corner frequency of the amplifier to remove *1/f* noise from signal band. The input

referred offset and the 1/*f* noise of the amplifier add to the modulated input signal and are amplified. The chopper (CH_2) at the output node then demodulates the input signal back to the baseband frequency while the offset and 1/*f* are modulated to the chopping frequency and filtered out by a low pass filter. The output spectrum of a chopper amplifier is shown in Figure 3(b).

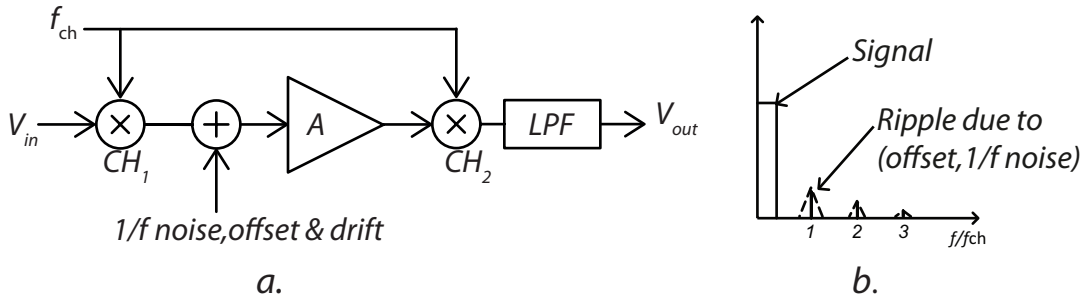

Figure 3. (a) A simple chopper amplifier. (b). The principle of chopping in frequency domain.

Although low offset and 1/f noise can be achieved by chopping, there are several disadvantages such as:

- Switching non-idealities in the choppers CH_1 and CH_2 generate residual errors in both voltage and current domain.
- There is chopping ripple at the amplifier's output due to the amplifiers up modulated *1/f* noise and offset.
- A low pass filter is needed in the signal path to filter out the ripple due to chopping. The presence of a low pass filter poses a bandwidth limitation.

The bandwidth limitation of a simple chopper amplifier can be solved with the aid of a technique called chopper stabilization [1.4]. Recent papers have described how chopper ripple can be suppressed by an offset-reduction loop [1.5] & [1.6]. As a summary of the two techniques, the low frequency noise spectrum of a chopper amplifier and that of an auto-zero amplifier are shown in Figure 4.

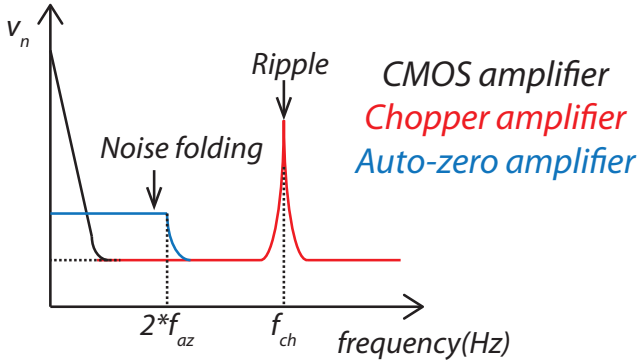

Figure 4. Frequency behavior of an auto zero and a chopper amplifier.

The power efficiency of a chopper amplifier is higher than that of an auto-zero amplifier due to the lack of sampled noise and continuous time operation of the amplifier. The high power efficiency and low noise make chopper amplifiers a better choice for low frequency applications. This work, therefore, is focused towards chopper amplifier. A chopper (Figure 5) performs the task of modulation of signals in a chopper amplifier. It is a four switch passive mixer as shown in Figure 5. The input and output of a chopper are the drain and source terminals of a MOS switch, while the gates of the switches are controlled by complementary clock signal (Figure 5). A MOS switch is a fundamental building block of a chopper. Therefore, non-idealities in a MOS switch are responsible for the residual errors in a chopper amplifier, i.e. input current and input current noise and residual offset. The mechanisms of charge injection and clock feed through in a chopper are explained in the later sections of this chapter.

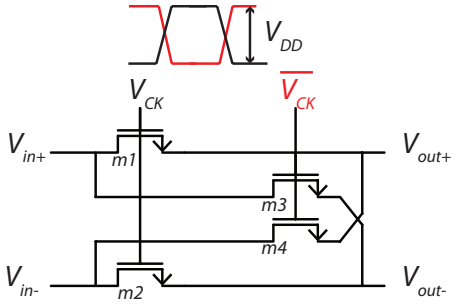

Figure 5. A chopper implemented with NMOS switches.

1.2 Motivation

Op-amps are used to boost the level of weak sensor signals so that they can be handled by an Analog *to Digital Converter* (ADC). A typical example of such a system is shown in Figure 6. The op-amp's specifications are governed by the sensor's characteristics such as its signal amplitude, bandwidth & source impedance (R_s). In the case of sensors with small signal amplitudes (<100mV) and with low bandwidths (<100Hz), e.g. thermocouples and hall sensors, which convert the signals from the thermal and magnetic domains respectively to electrical domain.

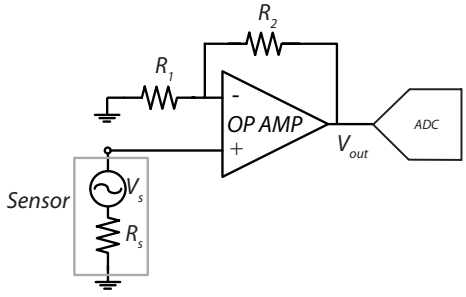

Figure 6. A typical chopper amplifier readout.

Therefore, the low frequency (<100Hz) requirements (offset and *1/f* noise) on the op-amp are more stringent. Thus CMOS op-amps that make use of dynamic offset cancellation (DOC) techniques (section 1.1) are the preferred choice for such applications because of their superior DC performance, i.e. lower *1/f* noise, drift and offset (V_{os}). By using such techniques, amplifiers with µV offset and milli-Hz *1/f* noise corners have been realized [1.7], [1.8]&[1.9].

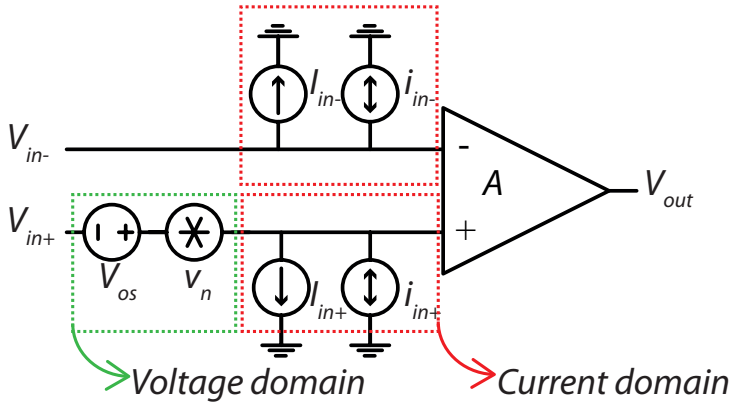

Figure 7. Input errors in an amplifier in the voltage and current domain.

Besides errors in the voltage domain, i.e. voltage offset (V_{os}) and input voltage noise density (v_n); current domain errors, i.e. input current (I_{in}) and input current noise density (i_n); are also important sources of error, especially for high source impedances (>100kΩ). Such current domain error sources can be added to the model of a precision CMOS op-amp as shown in Figure 7. For sensors with small source impedances, voltage domain errors dominate; while for higher source impedance, current domain errors dominate. It is hard to find op-amps, which can be used across a wide range of source impedances, e.g. (10Ω-1MΩ), and still achieve DC precision. A comparison of the state-of-the-art DC specifications of bipolar, trimmed, CMOS & precision chopper op-amps is given in Table 1. If these three op-amps are used in the application as shown in (Figure 6) to interface a sensor with certain source impedance R_s, the resulting offset is given by,

$$V_{OS,total} = V_{OS} + I_{in+}R_S \qquad \textit{Equation 1}$$

Although the offset performance of a chopper op-amp is better than the rest of the competition across a wide range of impedances (Figure 8), it can be seen that its offset performance starts to degrade rapidly when the source impedance R_s exceeds a threshold given by,

$$R_S > \frac{V_{OS}}{I_{in+}} \qquad \textit{Equation 2}$$

Table 1. DC errors in different generations of amplifiers

	I_{in+} (pA)	V_{os} (µV)	i_{in+} (fA/√Hz)	v_n (nV/√Hz)
BJT [1.10]	300000	600	400	10
CMOS [1.11]	2	1000	0.2	22
Trimmed CMOS [1.12]	Negligible	45	Negligible	9.1
Precision CMOS [1.13]	200	0.300	500	5.9

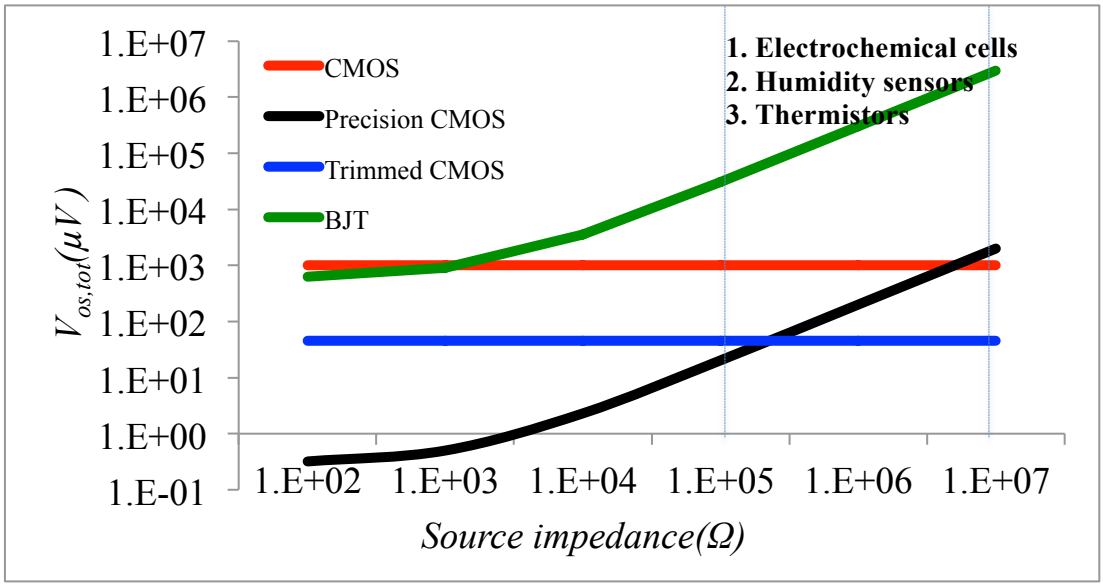

Figure 8. Residual offset as a function of source impedance in BJT, CMOS and precision CMOS amplifiers.

It is also desirable that the noise contribution of the op-amp (v_{ntot}) be smaller than the thermal noise of the source impedance over a wide range of values for source impedances (10kΩ-1MΩ), i.e.,

$$v_n^2 + i_n^2 R_S^2 \ll 4KTR_S \qquad \textit{Equation 3}$$

The equivalent input noise as a function of source impedance across generations of op-amps is illustrated in Figure 9. Given the huge market for high source impedance sensors (Figure 8), it is important to investigate and improve the current domain accuracy of chopper op-amps, which will be the main goal of this thesis.

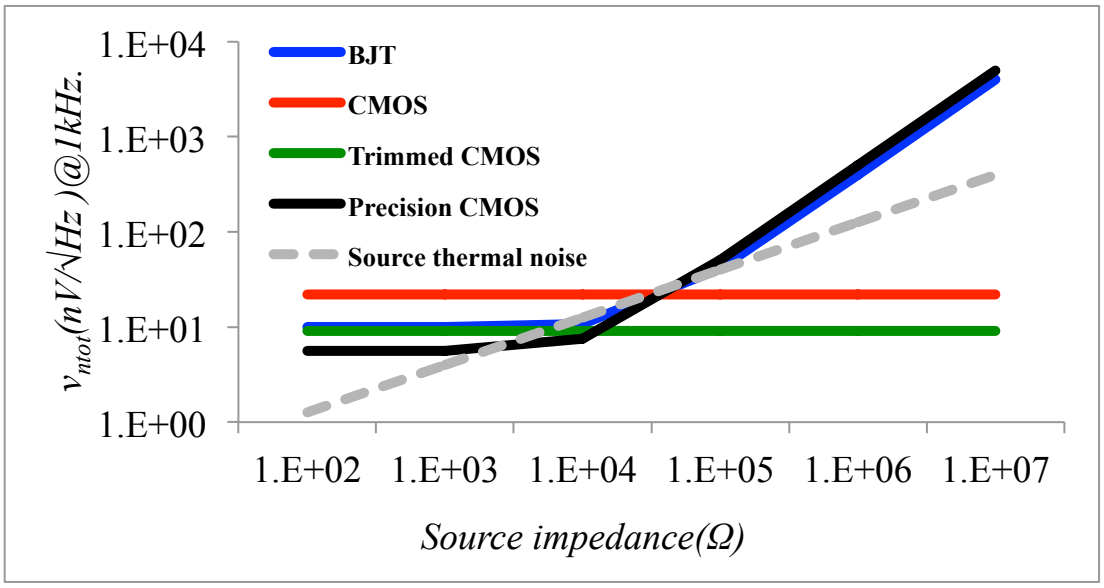

Figure 9. Equivalent input voltage noise density as a function of source impedance.

1.3 Current domain accuracy of a chopper op-amp

The voltage domain accuracy of a chopper stabilized operational amplifier has been extensively studied in [1.7], [1.8] & [1.9]. In this section, the current domain accuracy of a chopper stabilized operational amplifier will be discussed.

1.3.1 Channel Charge injection in a chopper

When a MOS switch is on, a channel is created under the gate of the device (Figure 10).

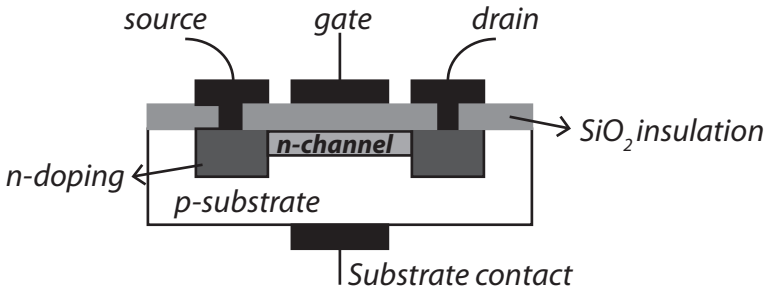

Figure 10. A MOS switch in ON state.

The total charge in the channel of an NMOS switch is given by,

$$q = WLC_{ox}(V_{DD} - V_{in} - V_{th}) \qquad \text{Equation 4}$$

Where, 'W' and 'L' are the width and length of the NMOS switch; 'C_{ox}' is the oxide capacitance per unit area, 'V_{DD}' is the amplitude of the clock, 'V_{in}' is the input common mode voltage and 'V_{th}' is the threshold

voltage of the MOS transistor. A chopper loaded equally on both the inputs (Figure 11 (a)) can be represented as a half circuit towards each of its inputs as illustrated in Figure 11(b). At each clock transition, one of the two switches (m_2) is turning on injecting a certain charge (q_2) and the other (m_4) turns off partially absorbing a part of this charge (q_4). Therefore, a residual charge ($\Delta q = q_2 - q_4$) flows through the input at each of the clock transitions and can be given by,

$$\Delta q = q_2 - q_4 = K \cdot WLC_{ox}(V_{DD} - V_{in} - V_{th}) \qquad \textit{Equation 5}$$

Where, 'K' is a constant < 1 because the residual charge is smaller than the charge injected by a single MOS switch. Since this charge is injected twice every clock cycle, a net DC current flows through each of the input terminals of a chopper and is given by,

$$I_{inj} = 2 \cdot f_{ch} \cdot K \cdot WLC_{ox}(V_{DD} - V_{in} - V_{th}) \qquad \textit{Equation 6}$$

Where, 'f_{ch}' is the chopping frequency. The charge injection current through each input will be slightly different depending on the mismatch in charge injection current and can be given by,

$$\Delta I_{inj} = I_{inj1} - I_{inj2} \qquad \textit{Equation 7}$$

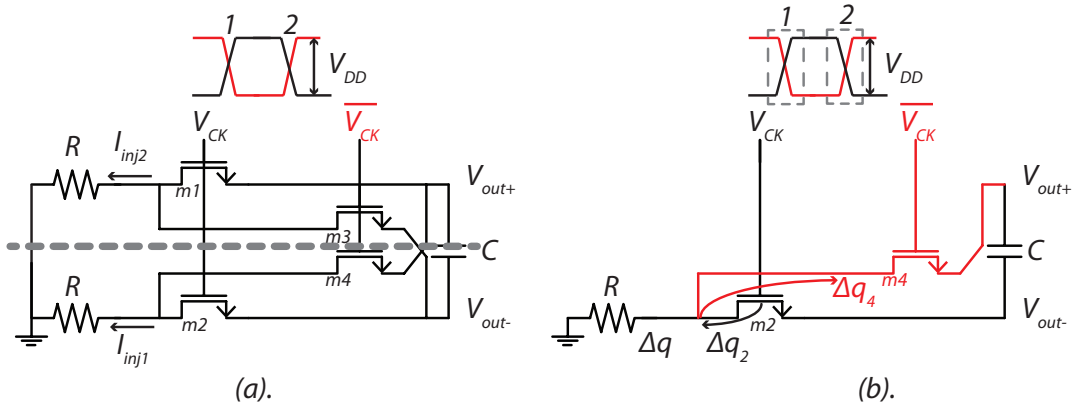

Figure 11. Charge injection in a chopper (a). A chopper (b). Half circuit of a chopper.

1.3.2 Clock feed-through in a chopper

In an ideal chopper, all the MOS switches are perfectly matched. However, in reality, a mismatch is present within the switches and can be represented by a clock feed-through mismatch capacitance 'ΔC' (Figure 12(a)) The clock transitions couple through this capacitance and hence, appear as an AC spikes at the output of the chopper as shown in Figure 12(b) .The offset current can be given by,

$$I_{OS} = 2f_{ch}\Delta C V_{DD} \qquad \text{Equation 8}$$

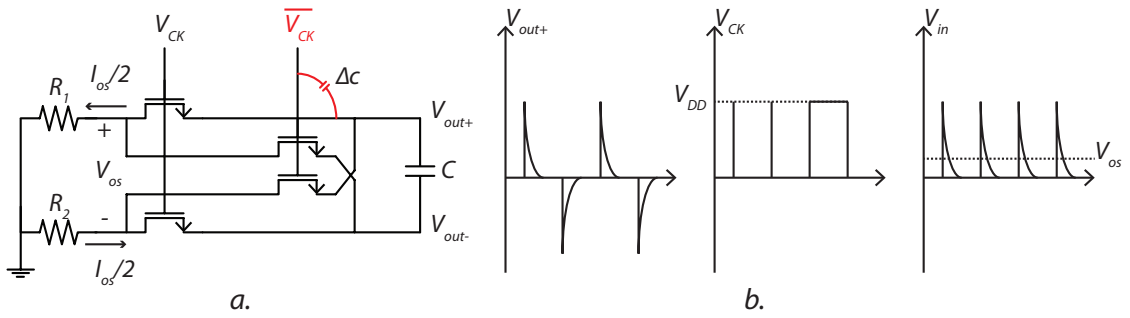

Figure 12. (a) Clock feed-through in a chopper. (b). Clock feed through spikes in time domain.

1.3.3 Input currents in a chopper

The continuous time operation of a chopper will introduce currents that flow through its input pins. The net DC current through each of the input pins is a sum of charge injection component (Equation 6) & offset component (Equation 8). Mathematically this current can be represented by,

$$I_{in\pm} = I_{inj1,2} \pm \frac{I_{OS}}{2} \qquad \text{Equation 9}$$

1.3.4 Common mode variation of input current in a chopper

The input currents in a CMOS chopper depend on the input common mode voltage V_{in}. This is due to variation in channel charge (Equation 6) with input common mode voltage, e.g. when an NMOS chopper is used (as in [1.10]), the measured input current is maximum when the input common mode voltage is close to ground and drops linearly till the switch turns off (Figure 13). In addition to the above effect, the threshold voltage (V_{th}) of a MOS transistor varies with input voltage due to body-effect in a MOS switch and can be given by,

$$V_{th} = V_{t0} + \gamma \cdot (\sqrt{2\phi_F + (V_{in} - V_B)} - \sqrt{2\phi_F}) \qquad \text{Equation 10}$$

Where, 'γ' is the body effect parameter, 'ϕ_F' is the surface potential, 'V_B' is the body bias potential and 'V_{t0}' is the threshold voltage at a zero body bias voltage.

The variation of input current with input voltage is observed in most chopper amplifiers [1.14] & [1.15] and limits their common mode rejection ratio (*CMRR*) when used for readout of high impedance sensors. Therefore, it is important that the input currents remain constant across input common mode voltage. Techniques to tackle this issue will be discussed in chapter 2.

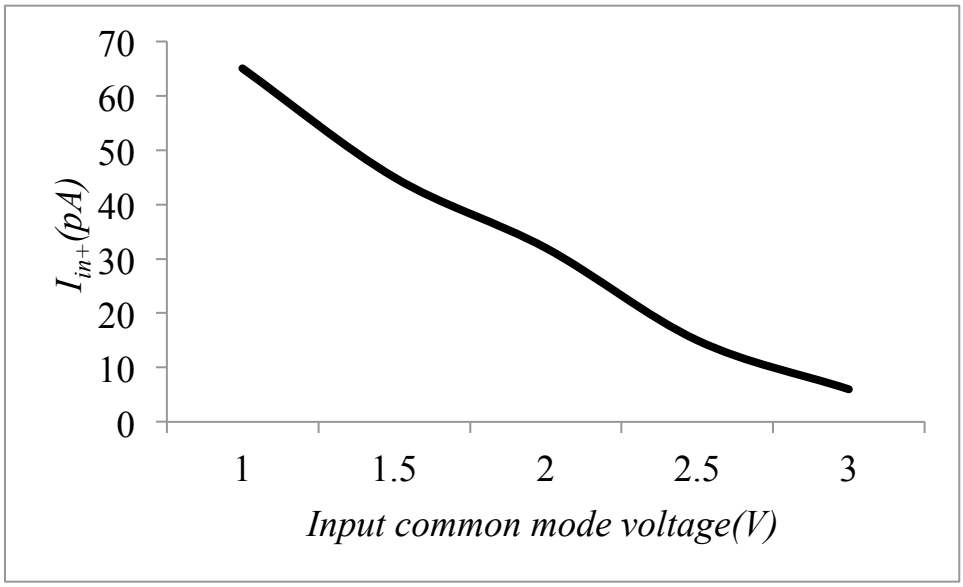

Figure 13. Input current vs. input common mode voltage.

1.3.5 Current noise in a chopper

In addition to a DC current at the input of the chopper, a current noise is present. The DC current in time domain is a continuous flow of discrete charges (electrons). Any fluctuations in the flow of these electrons will result in a fluctuation in the DC current. This fluctuation is defined as "Shot noise" or "current noise" and can be given by,

$$i_n = \sqrt{2qIB} \qquad \textit{Equation 11}$$

Where, 'q' is the charge of an electron in coulombs; 'I' is the net DC current flowing through a conductor and 'B' is the bandwidth under consideration. A standard CMOS amplifier has almost negligible current noise (<5fA/$\sqrt{Hz}$), due to its low input bias currents. However, a chopper amplifier implemented in CMOS process has a higher current noise (>500fA/$\sqrt{Hz}$)[1.13], due to its higher input current as explained earlier. The current noise in a chopper can be expressed by,

$$i_{n\pm} = \sqrt{2q\frac{Q}{t}B} \qquad \textit{Equation 12}$$

Where, 'Q' is the total charge circulating in the chopper in one clock cycle of 't' seconds.

In a chopper amplifier, the Equation 11 doesn't accurately predict current noise because only a part of the total charge (Q) contributes to the DC input current. The parameters input current ($I_{in\pm}$) and input current noise (i_{in}) of a chopper, determine the current domain accuracy of a chopper amplifier and can be modeled as shown in Figure 14(a, b).

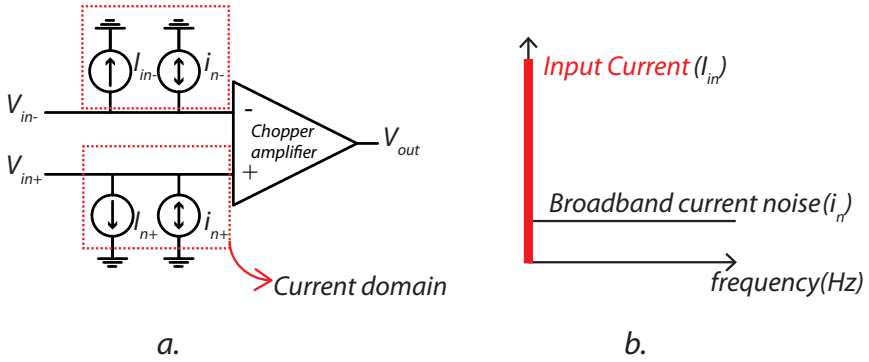

Figure 14. Input errors in the current domain in (a). Chopper amplifier. (b) Current domain errors in frequency domain.

1.4 The state-of-the-art in chopper op-amp

Many precision chopper op-amps have been designed, which use the chopping technique discussed above to achieve a low offset and low noise performance. Table 2 lists the specifications of present state-of-the-art precision chopper op-amp designs. In two of these designs [1.14] and [1.13], the input current and current noise is very large (>90pA) while meeting a state-of-the-art voltage noise specification. The state-of-the-art value for input current has been achieved by [1.16], however, at the cost of degraded input noise voltage.

Table 2.The State-of–the-art in chopper amplifiers.

	ADA4528 [1.13]	ADA4051 [1.16]	ISL28233 [1.15]	OPA333 [1.17]	Q.Fan [1.14]
Input Offset (uV)	0.300	2	2	2	1
Input current *(pA)*	200	50	180	140	70
Input noise voltage *($nV/\sqrt{Hz}$)*	5.9	95	65	55	10.5
Current noise *($fA/\sqrt{Hz}$)*	500	100	72	100	--
f_{ch} *(kHz)*	200	50	5	125	30

1.5 Target Specification

Using chopping technique, the designs mentioned in Table 2 achieve a low voltage offset and low voltage noise. This work targets to improve the current domain accuracy performance in a chopper op-amp while maintaining the state-of-the-art offset and noise performance. The target specifications for this work are listed in Table 3.

Table 3. Target specifications for this work.

Parameter	Target Specification
Offset	<5μV
Voltage Noise	<11nV/√Hz
Input current	<20pA
Input Common mode range	(0-5) V
Input current noise	<100fA/√Hz
Chopping frequency	(30-100) kHz
Process	0.7μm

1.6 Overview of thesis

This thesis describes the design and implementation of a chopper op-amp with low input current. The remainder of this thesis is organized as follows: Chapter 2 discusses existing techniques to suppress the residual errors in chopper amplifiers. A comparison of these techniques and their applicability to this work is also discussed. Chapter 3 describes the design strategy for low input current chopper operational amplifier based on insights obtained from measurements on existing chopper amplifiers. Finally, the measurement results of the prototype chip are presented in Chapter 4.

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2 Advanced Chopper amplifiers

In the previous chapter, the origin of input current noise (i_n) and input current (I_{in}) in a chopper amplifier are explained. The charge injection and clock feed-through mechanisms in a MOS switch are the primary causes of these errors.

Therefore, in this chapter, a few techniques to suppress charge injection and clock feed-through effects in MOS switches are described in Section 2.1. In Section 2.2, a few advanced techniques that focus on reducing charge injection and clock feed-through errors in a chopper amplifier are presented. Section 2.3 compares and identifies the best approach to solve the problem of input current and current noise in a chopper amplifier. Section 2.4, summarizes this chapter with the conclusions drawn from the discussions in Section 2.3.

2.1 Charge injection suppression techniques in a MOS switch

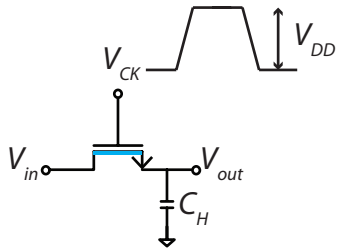

Figure 15. Channel charge in a MOS switch in ON state.

The charge stored in the channel of a NMOS switch (Figure 15) can be given by,

$$q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{th}) \qquad \textit{Equation 13}$$

When this switch turns off, this charge is injected into the drain and the source terminals respectively. The amount of charge flowing into the drain and the source terminals depends on the impedance levels at their terminals.

From Equation 13, it is clear that, in order to reduce charge injection, the area of the switch has to be minimized. However, the above approach is acceptable when the on-resistance (R_{on}) of the switch is not a critical specification. In the case of a chopper amplifier, the R_{on} of a switch becomes critical when an amplifier with low voltage noise is desired. For example, if an input noise specification of 12nV/$\sqrt{Hz}$ is to be achieved, the thermal noise of the switches may become critical. Consider a steady state of a chopper

amplifier as shown in Figure 16, to estimate the thermal noise contribution of the input switches. The total input voltage noise including the thermal noise of input switches can be given by,

$$v_{ntot} = \sqrt{v_n{}^2 + 8KTR_{on}} \qquad \textit{Equation 14}$$

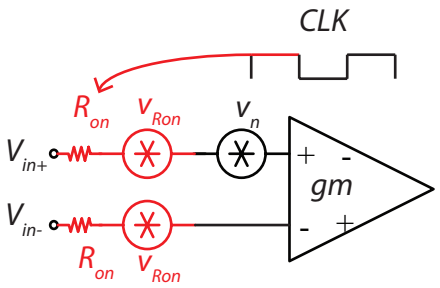

Figure 16. A steady state of a chopper amplifier.

It is desirable that most significant contribution to input noise originates from the input transconductor rather than the input switches, i.e.,

$$v_n{}^2 \gg 8KTR_{on} \qquad \textit{Equation 15}$$

This condition ensures a high figure of merit ($v_{ntot}{}^2$*I), which is an indication of the power efficiency in a low noise amplifier [2.1]. Therefore, the method discussed above is valuable if the noise specification of the amplifier is more relaxed (>80nV/$\sqrt{Hz}$). The above technique has been employed in [2.2] to achieve state-of-the-art performance in terms of current domain accuracy.

2.1.1 Dummy switches

Charge injection can be partially compensated for by adding dummy switches that are driven by a complementary clock signal (Figure 17) and which inject an amount of charge that partially compensates for the charge injected by the main switch [2.3].

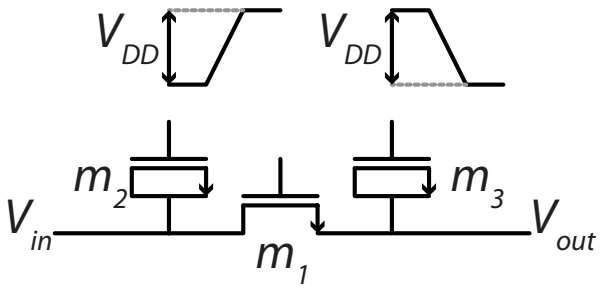

Figure 17. A MOS switch with Dummy transistors for cancelling charge injection.

However, the assumption that the main switches' charge splits equally between the source and drain is generally invalid, making this approach less attractive. Also, dummy switches in a chopper are not attractive as they increase its layout area [2.3].

2.1.2 Complementary switches

Another approach to reduce the charge injection is to use transmission gate switches (Figure 18), which are made from both PMOS and NMOS devices, such that the opposite charge packets injected by the two transistors partially cancel each other. However, this cancellation is only effective for a limited range of the input signal around half of the supply voltage given by,

$$V_{in} = \frac{V_{DD} - V_{th,n} - V_{th,p}}{2} \qquad \textit{Equation 16}$$

Where, '$V_{th,\,n}$' and 'V_{thp}' are the threshold voltages of NMOS and PMOS transistors respectively.

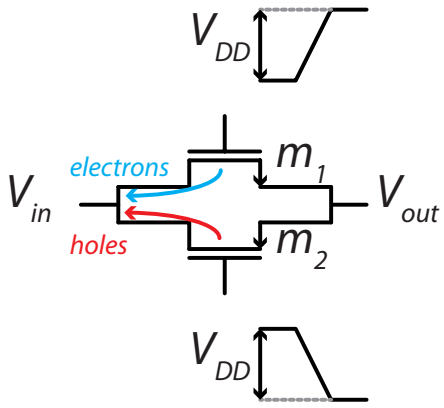

Figure 18. A CMOS switch.

2.2 Clock bootstrapping

The dependency of input current on input common mode voltage was explained in section 1.3.4. This dependency is not desirable in many high precision applications. In order to mitigate this problem, the clock signal can be made to track the input signal (Figure 19). Hence, the channel charge will be made independent of the input signal, which is given by,

$$q_{ch} = WLC_{ox}(\Delta V - V_{th}) \qquad \textit{Equation 17}$$

Where, $'\Delta V'$ is the clock amplitude.

Also, the body of the MOS switch can be connected to the input common mode voltage (Figure 20) to avoid threshold voltage modification due to body effect [2.7]. When a lower charge injection is desired, $\Delta V < V_{DD}$, a technique which is used in [2.2]&[2.4].

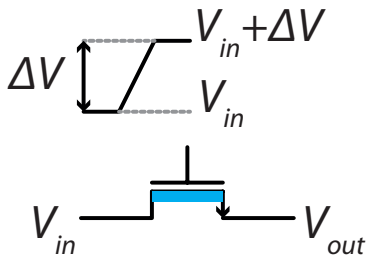

Figure 19. The principle of a bootstrapped switch.

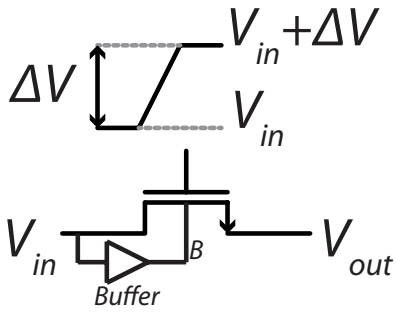

Figure 20. Body biasing in a MOS switch.

2.3 Advanced chopper amplifier techniques

In this section, three advanced chopper amplifier techniques intended to suppress input currents are outlined. Since the final goal of this work is a precision amplifier with low input current, the suitability of these techniques for use in a chopper-stabilized amplifier will be discussed.

2.3.1 Nested chopping

In order to suppress the residual errors in a chopper amplifier, the chopper amplifier is further chopped at a much lower chopping frequency 'f_{CL}' as illustrated in Figure 21(a). The presence of a clock feed-through capacitance(C) in CH_1 injects charge packets (q_b) at the amplifier's input (node 'b'), which will cause net DC charge spikes at node 'a' as illustrated in Figure 21(b). The chopper CH_3 converts the net DC spikes into an AC ripple at 'f_{CL}' at the input (V_{in}). This technique also removes any DC current at the amplifier's input due to clock feed-through in CH_1. However, the input current due to charge injection in CH_1 remains unchecked and appears as a net DC current at the input given by,

$$I_{in} = I_{inj1} \qquad \textit{Equation 18}$$

The errors due to charge injection and clock feed-through in choppers CH_3 and CH_4 will be negligible if the condition ($f_{CL} << f_{CH}$) is satisfied. When extended to a chopper-stabilized amplifier shown in Figure 22.The net input current of the amplifier can be expressed by, Equation 18.

Although, nested chopping is effective in suppressing the offset component of the input current, the presence of a low frequency ripple discourages its usage in commercial amplifiers [2.5].

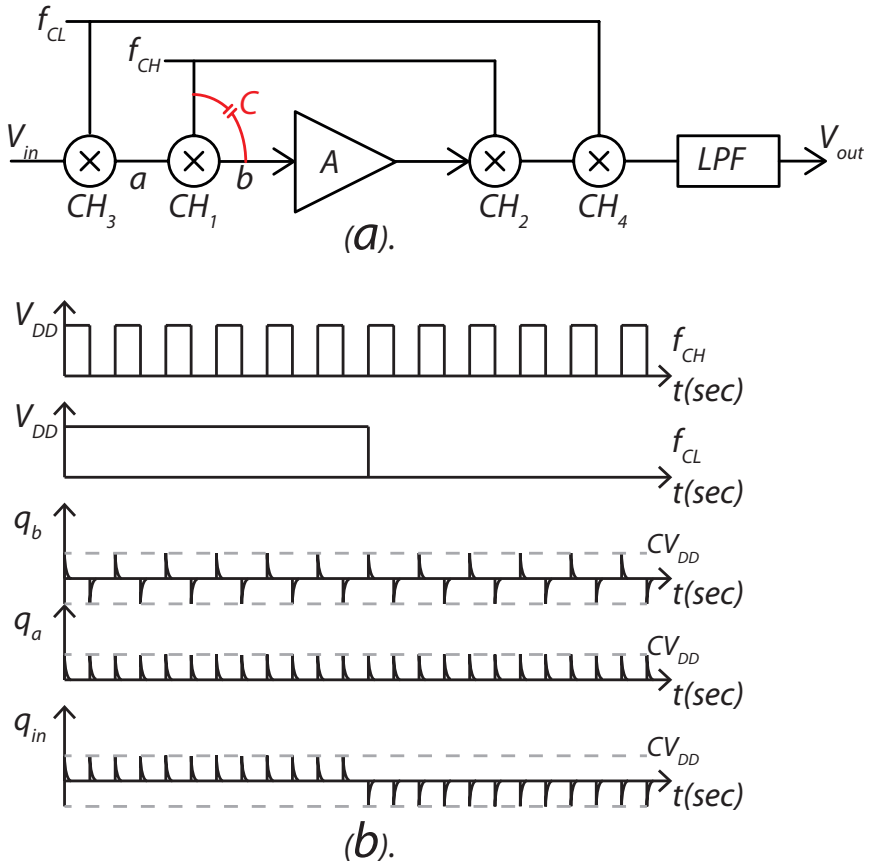

Figure 21. (a). A nested chopper amplifier (b). The principle of nested chopping in the charge-time domain.

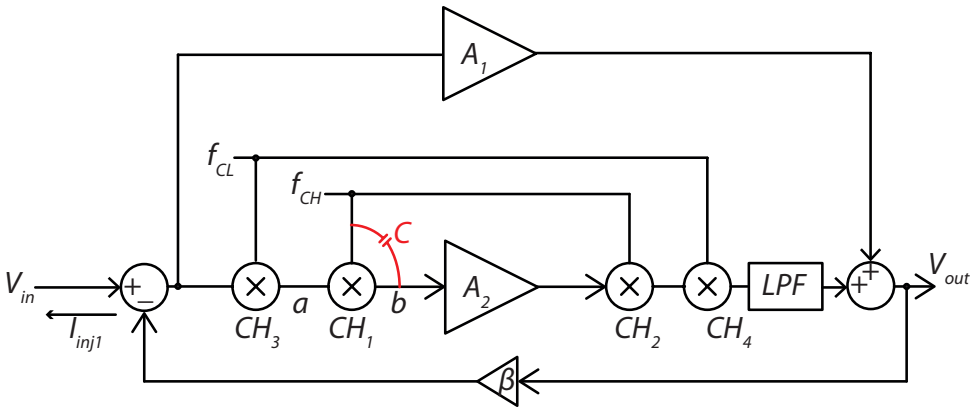

Figure 22. The concept of nested chopping extended to a chopper-stabilized amplifier.

2.3.2 Chopping with guard band

Another method of reducing residual offset in a chopper amplifier is to introduce a small guard time between the clocks driving the choppers CH_1 and CH_2, as illustrated in Figure 23(a), this prevents the spikes caused by charge injection and clock feed-through in CH_1 from being demodulated, as shown in Figure 23(b). This technique has been used in [2.6] for custom sensor interfaces and an average offset of 200nV has been achieved. The guard time delay is determined by the time constant of the voltage spikes, which depends on the source impedance (R_s) and the input capacitance (C_{in}) of the amplifier [2.6].

As most of the DC component of input current is concentrated in the form of voltage spikes (due to interaction between source impedance and current spikes)[2.8] generated by CH_1, the guard band prevents the propagation of these spikes towards the output. Hence, an indirect improvement in current domain accuracy can be obtained. However, the output signal is no longer continuous-time due to the gap due to the guard time in CH_2, thus incurring loss of gain and noise aliasing. Moreover, this technique is not applicable to a chopper-stabilized amplifier because the high frequency path, as shown in Figure 24. Would process the input voltage spikes resulting in DC errors.

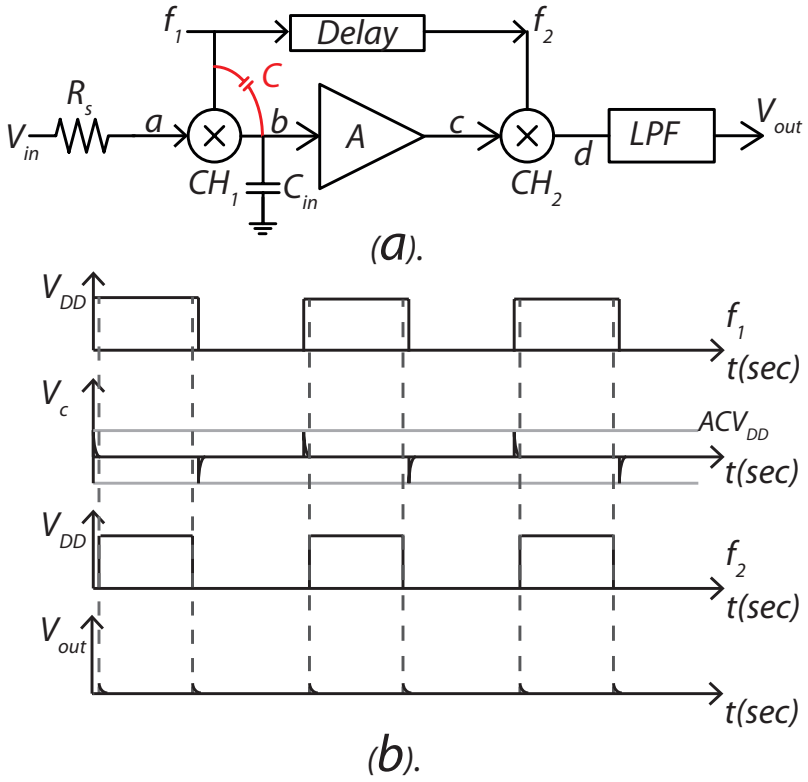

Figure 23. Guard band chopping (a). An amplifier with delayed clock signals. (b). The principle of operation.

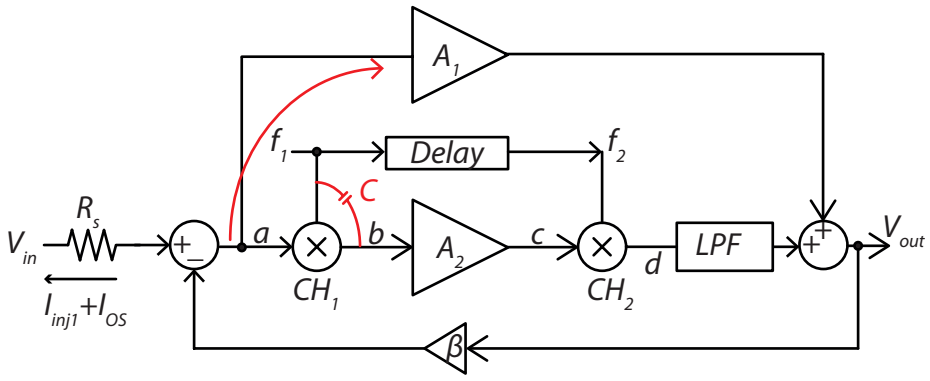

Figure 24. Guard band chopping in a chopper-stabilized amplifier.

2.3.3 Charge injection suppression techniques in chopper amplifiers

Nested chopping (2.3.1) improves DC performance by suppressing the errors due to clock feed-through, while the use of a guard band in a chopper amplifier (2.3.2) indirectly improves the current domain accuracy by cutting-off voltage spikes due to charge injection and clock feed-through further in the signal chain. Recent work has focused on suppressing DC errors due to charge injection [2.7]. The dominant source of charge injection arises from the MOS switches in the chopper connected towards the signal source and varies as a function of input common mode voltage as discussed in section 1.3.4. Therefore, the amplitude of clock signal driving these switches is limited (amplitude<V_{DD}), in order to reduce charge injection and is bootstrapped. In order to prevent variation of threshold voltage with input common mode voltage in the NMOS switches, the bulk of the switches is tied to input common mode voltage through a common mode buffer (Figure 25). The clocking scheme in the front-end chopper is shown in Figure 25. Using this technique, offset current and charge injection current are only suppressed partially. However, they are made independent of input common mode voltage [2.7].

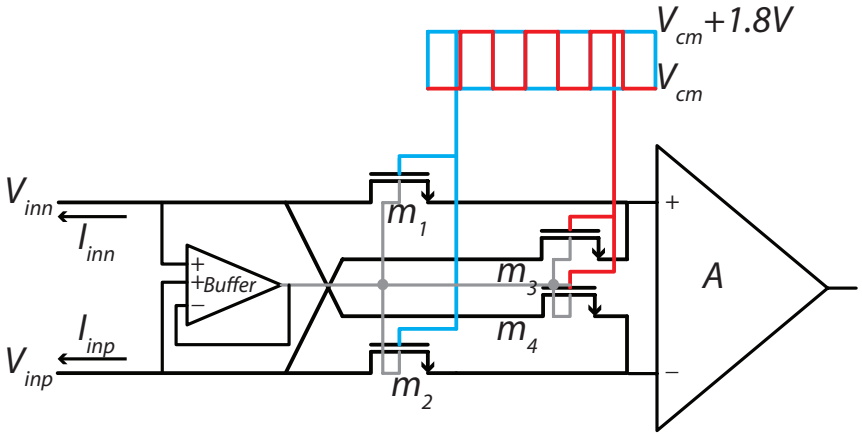

Figure 25. A modified front-end chopper, KUSUDA ISSCC2011.

2.4 Comparison of various techniques

The use of bootstrapped switches is essential for maintaining input current constant across input common mode voltage as discussed in section 2.2 while, the magnitude of the input current can be suppressed by utilizing the techniques proposed in sections 2.1 & 2.3. The techniques discussed in section 2.3 are summarized in Table 4. The presence of a low frequency ripple due to nested chopping discourages its usage in this work. The technique of guard banding (Section 2.3.2) is not applicable to this work, as the final goal is a chopper-stabilized amplifier. Modifying the front-end chopper as suggested in [2.7] reduces input current due to charge injection and clock feed-through (only to a limited extant). Therefore, a modified front-end chopper and its clocking scheme will be presented in the next section.

Table 4. Summary of Advanced techniques in a chopper amplifier.

	Nested chopping *[2.5]*	*Chopper amplifier with a guard band.* *[2.6]*	*Modified front-end chopper* *[2.7]*
Charge injection component (I_{inj})	--	-- *(Indirect)*	+
Clock feed-through current (I_{os})	++	-- *(Indirect)*	+
Suitable in a Chopper-stabilized amplifier.	✓	*X*	✓
(+) Positive effect. (-) Negative effect.			

2.5 Proposed solution

To completely remove charge injection in the front-end chopper, the following conclusions can be drawn from the discussion in sections 2.1, 2.2 & 2.3. Firstly, every switch in the front-end chopper has to be made free (ideally) from charge injection. An efficient way to achieve this is through the use of a complementary switch (section 2.1.2).

Secondly, clock bootstrapping has to be used to ensure that the charge injection and hence, input current is made independent of input common mode voltage (V_{in}). The bulk of the switches have to be connected to

the input common mode voltage (section 2.2), if permitted by the process. Also, layout of the front-end chopper has to be made symmetrical as suggested in [2.3]. This prevents any systematic offset current due to clock feed-through.

Finally, the resistance (R_{on}) of the switch has to be minimized if a low input noise voltage is desired. The proposed front-end chopper and its clocking scheme are illustrated in Figure 26.

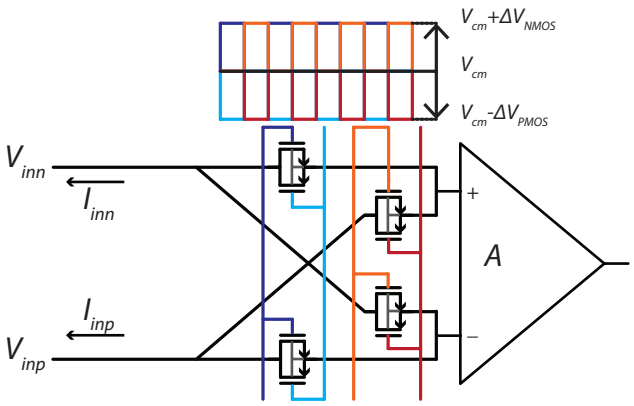

Figure 26. Proposed front-end chopper.

2.6 Summary

In this chapter various techniques to suppress charge injection and clock feed through errors in a chopper amplifier were described along with their pros and cons. A solution is proposed Section 2.5. Design and implementation of a low input current chopper amplifier will be presented in the next chapter.

2.7 References

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3 Design of a low input current chopper amplifier

In this chapter, the design and implementation of a low input current chopper amplifier is presented. The amplifier proposed in [3.1] is a good starting point, since it achieves state-of-the-art performance in terms of offset. In section 3.1, a brief description of this amplifier is given. As the input chopper determines the input current [3.2], the design of a novel input chopper is described in Section 3.2. Details of the test chip are given in Section 3.4. Finally, the simulation results are presented in Section 3.6.

3.1 A State-of-the-art chopper stabilized amplifier

The architecture of the amplifier proposed in [3.1] will be briefly reviewed in this section, as this will be used as a platform for this work. The amplifier, in its possible configurations is illustrated in Figures 27-28. The amplifier is a multi-path precision current feedback instrumentation amplifier (CFIA), when the negative feedback point is current summing node. It can also be used as a general-purpose op-amp depending on the configuration of its transconductors [3.1].

A multipath approach: One high frequency path (HFP), which determines the bandwidth of the amplifier, and a chopped low frequency path (LFP), which ensures good DC performance is used to realize the transconductors. A ripple-reduction loop (RRL) [3.2] is used to suppress the chopping ripple due to offset of gm_{21} and gm_{22}. The frequency compensation network formed by capacitors (Cm_1, Cm_2 and Cm_3) [3.3] merges the signals from these paths to provide a smooth frequency response.

CFIA

The simplified block diagram of the precision CFIA is illustrated in Figure 27 .The amplifier has an input transconductor (gm_{11}, gm_{21}) and a feedback transconductor (gm_{12}, gm_{22}). The chopper (CH_1) of the input transconductor, which is directly connected to the signal source, determines the CFIA's input current. The characteristics of input current in a CFIA are presented in [3.1].

Op-amp

In an op-amp configuration (Figure 28), the input and the feedback transconductors are shorted, and hence the choppers (CH_1, CH_2), which are directly connected towards the input source, determine the op-amp's input current. The measured performance of the op-amp is presented in Table 5 along with the target specifications of this work. The amplifier described above is optimized for f_{ch} =30kHz. The measured input current (I_{in+}) as a function of input common mode voltage is shown in Figure 29. As described in section 1.3.4, the use of simple NMOS switches in the input gives rise to a significant dependency on the

input common mode voltage. The input current (I_{in+}) linearly varies with chopping frequency as shown in Figure 30. The magnitude of the input current and its common mode variation has to be suppressed to meet the target specification < 20pA at f_{ch}=100kHz (Table 5). Therefore, a redesign of the front-end choppers (CH_1 *and* CH_2) is necessary, this will be discussed in the next section.

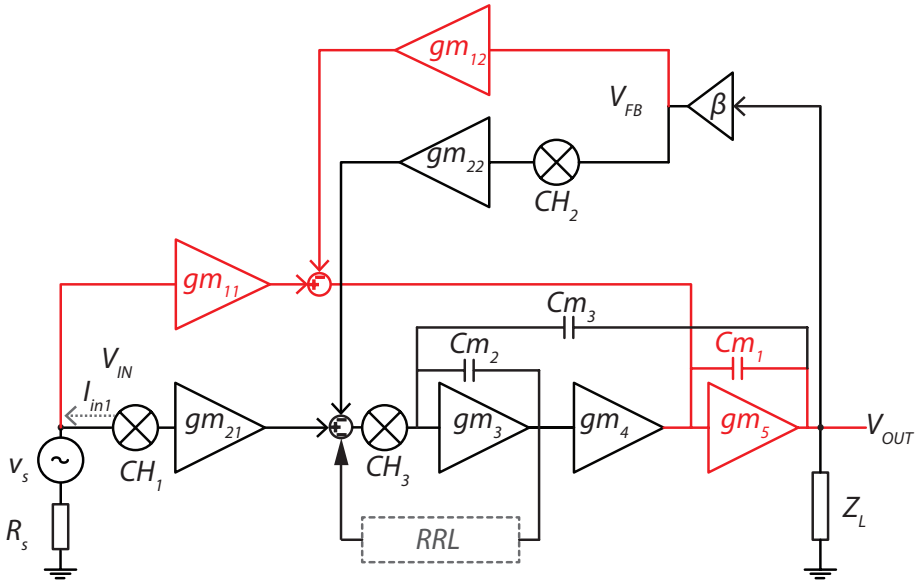


Figure 27. Amplifier configured as a CFIA.

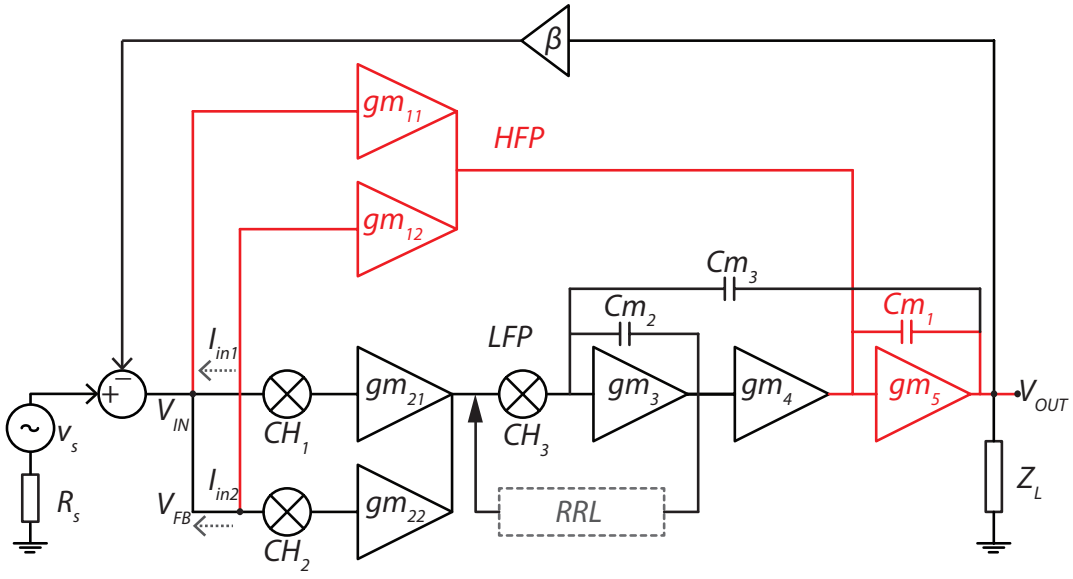


Figure 28. Amplifier configured as an op-amp.

Table 5.Specification of the amplifier.

Parameter	**Q.Fan [3.1]**	**Target specification**
Input Offset (uV)	1	5
Input current *(pA)*	70	±20
Input noise voltage *(nV/√Hz)*	10.5	<12
Current noise (*fA/√Hz*)	---	100
f_{ch} (*kHz*)	30	100
GBW (*kHz*)	1800	1800

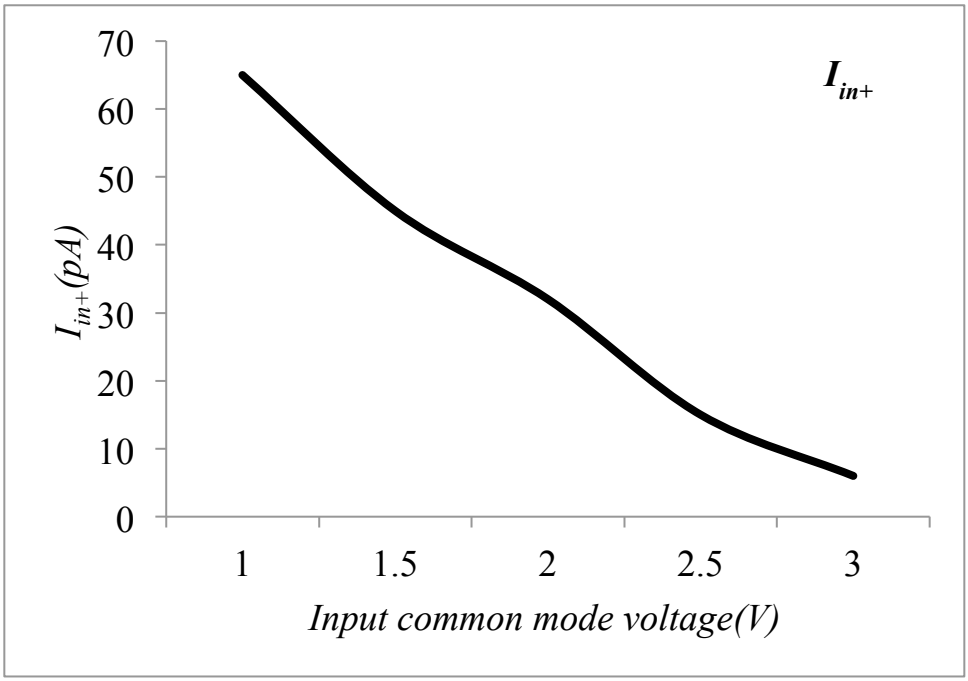


Figure 29. Measured input current vs. input common mode voltage. f_{ch}=30kHz.

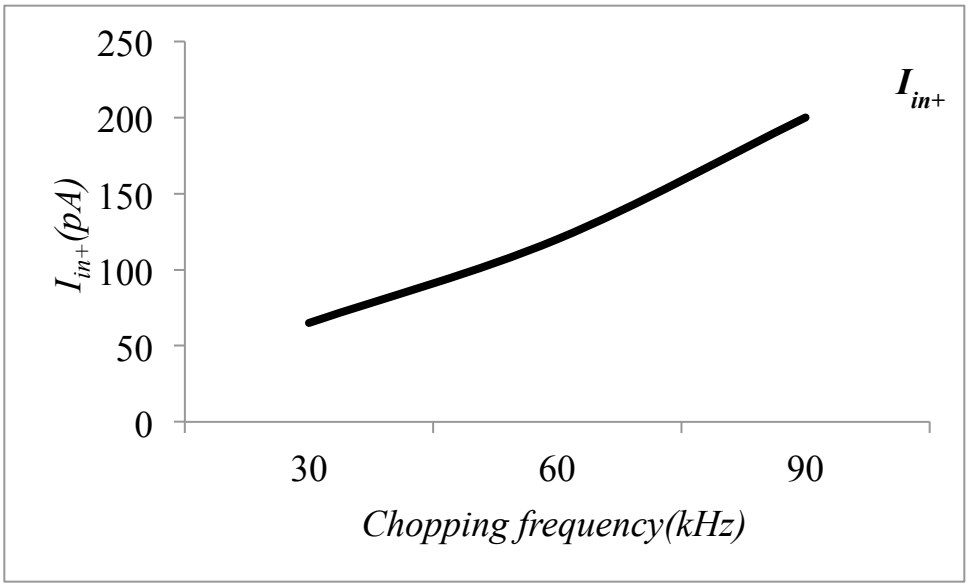


Figure 30. Measured input current vs. f_{ch}. V_{in}=1V.

3.2 A front-end chopper with improved current domain accuracy

The use of a CMOS bootstrapped switch in order to suppress charge injection has been suggested in the previous chapter. In order to bootstrap the switches, a novel technique proposed in [3.4] is preferred due to its simplicity as compared to the more traditional approach used in [3.5] & [3.6]. The design details of the chopper are presented in this section.

3.2.1 Switch on-resistance (R_{on})

The on resistance of the switch (R_{on}) is determined by the input noise voltage specification of the amplifier. The noise contribution of R_{on} to the total input noise of the amplifier can be calculated by,

$$v_{ntot} = \sqrt{{v_n}^2 + 8KTR_{on}} \qquad \text{Equation 19}$$

The input referred voltage noise (v_n) of the amplifier proposed in [3.1] is 10.5nV/$\sqrt{Hz}$. For a total input noise specification of (<12nV/$\sqrt{Hz}$), the maximum allowable R_{on} is 1kΩ.

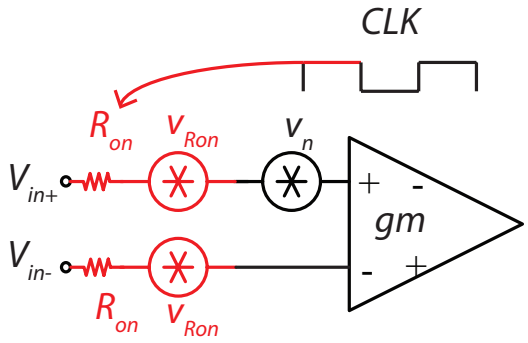


Figure 31.Steady state of a chopper amplifier.

3.2.2 Capacitively-coupled chopper

The Capacitively coupled choppers used in this design are shown in Figure 32(a, b). The capacitors (C) couple the clock signals to the gates of the MOS switches (*m1, m2, m3* and *m4*). The transistors (*m5, m6*) and the resistor (R_{sense}) together define the DC level at the gates of *m1, m2, m3* and *m4*. In this design, the back gates of NMOS and PMOS transistors are connected to ground and supply voltages respectively due to the lack of a bulk connection for the NMOS devices in the 0.7um process by *Euro practice*. The clocking scheme generated by the capacitive coupled choppers is shown in Figure 33. The generated clock signals are referenced to input voltage (V_{in}) instead of ground and their amplitude depends on the capacitive divider formed between the coupling capacitor (C) and the gate capacitance (C_{gg}) of a MOS switch. The gate capacitance of transistors *m5* & *m6* contributes an additional parasitic capacitance and hence their dimensions are made comparatively smaller than the MOS switches. Varying the power supplies (V_{DDNMOS} &V_{DDPMOS}) of the buffers driving NMOS and PMOS choppers respectively enables trimming of any residual charge. The amplitude of the clock signals at the gates of switches (*m1, m2, m3* and *m4*) is determined by,

$$\Delta V_{NMOS} = \frac{C}{C + 2C_{gg}} \cdot V_{DDNMOS}$$

$$\Delta V_{PMOS} = \frac{C}{C + 2C_{gg}} \cdot V_{DDPMOS} \qquad \textit{Equation 20}$$

In a 5V supply, V_{DDPMOS}=V_{DDNMOS}=$5V$.

A common mode voltage sense resistor (R_{sense}) is tied to the inverting input of the amplifier as this node is insensitive to input current. An optimum value for R_{sense} is chosen to suppress leakage current (I_{leak}), flowing into transistors (m_5 and m_6). In order to effectively suppress this leakage current, in this design R_{sense}=$1M\Omega$ (Figure 34). The details of this design are summarized in Table 6.

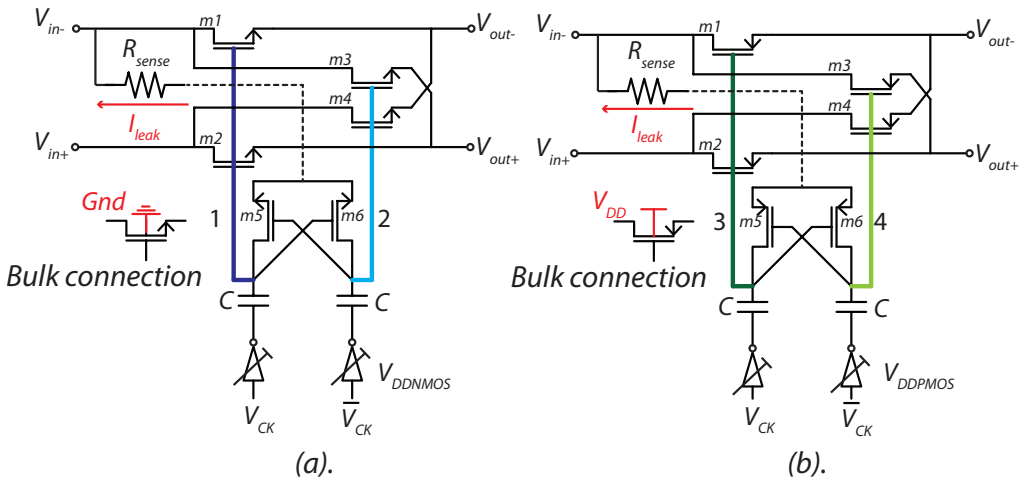


Figure 32. Capacitively-coupled choppers (a) NMOS (b) PMOS.

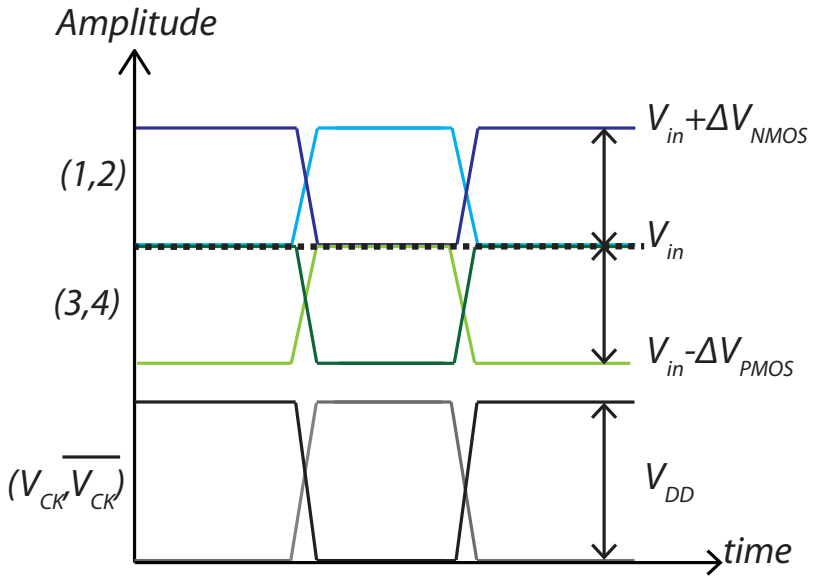


Figure 33. Clocking scheme of capacitive coupled choppers.

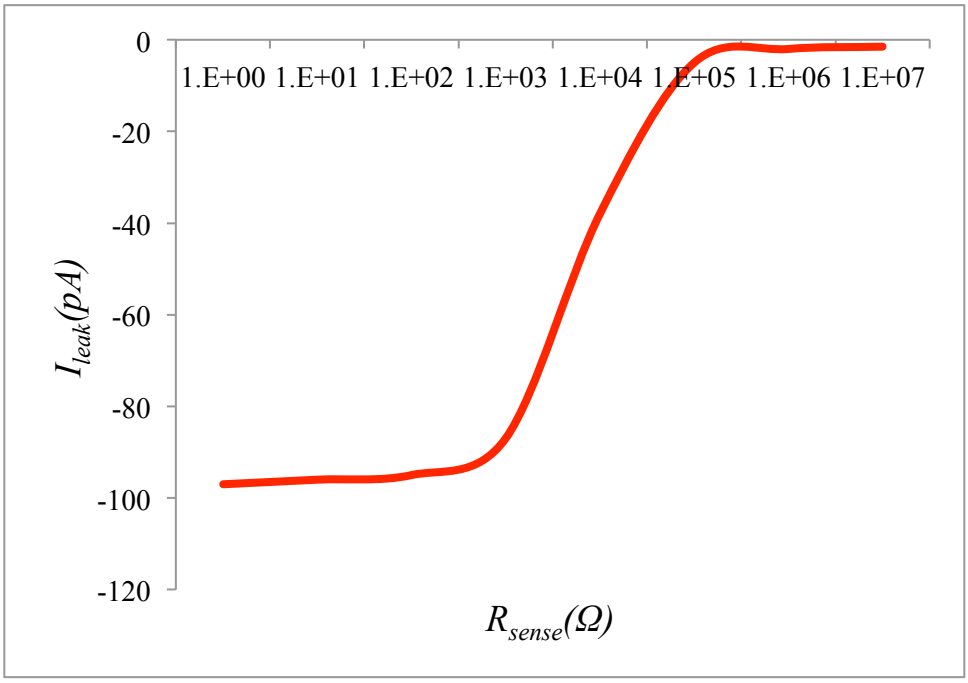


Figure 34. I_{leak} vs.R_{sense}. f_{ch}=30kHz.

Table 6. Design parameters of the proposed choppers.

Parameter	NMOS (Figure 32(a))	PMOS (Figure 32(b))	Original chopper (Simple NMOS)
m1, m2, m3 and m4 (W/L)µm	11/0.7	11/0.7	22/0.7
m5 and m6 (W/L)µm	1.8/0.7	1.8/0.7	---
R_{sense} (MΩ)	1	1	---
C (fF)	150	150	---
ΔV (V)	2.5	2.5	5V
R (Ω)	Figure 35	Figure 35	200
R_{ON} (Ω) [CMOS switch]	Figure 35		

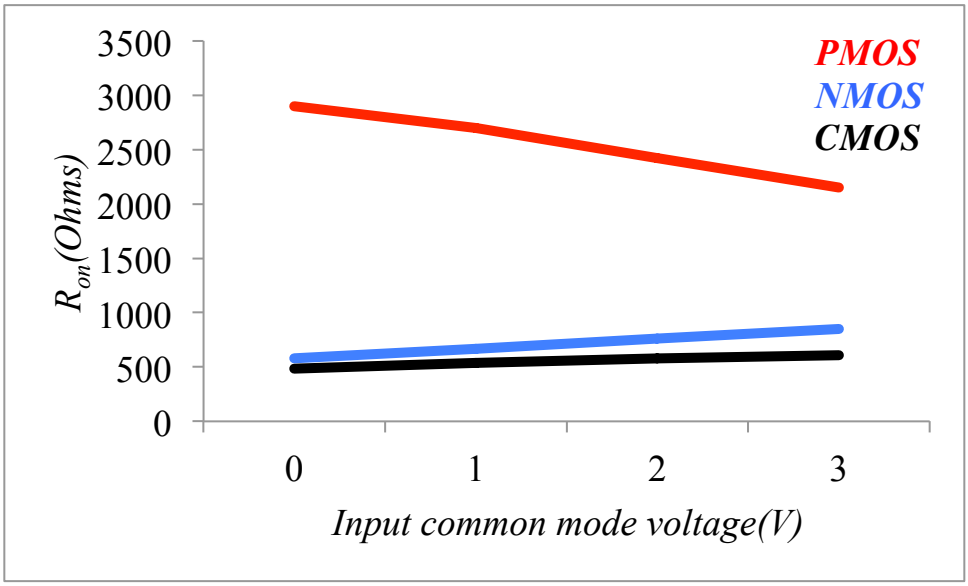


Figure 35. On-resistance modulation due to body effect in the Capacitively- coupled choppers.

3.3 Layout of the proposed choppers

A symmetric layout of the chopper (Figure 36) is crucial to minimizing systematic errors, which otherwise will lead to a large input offset current by introducing unwanted clock feed-through capacitance (section 1.3.2). The layout of the chopper proposed in [3.7] is used in this work. The PMOS chopper switches are placed inside an n-well, which isolates it from the p-substrate. The NMOS chopper switches are placed directly on the p-substrate.

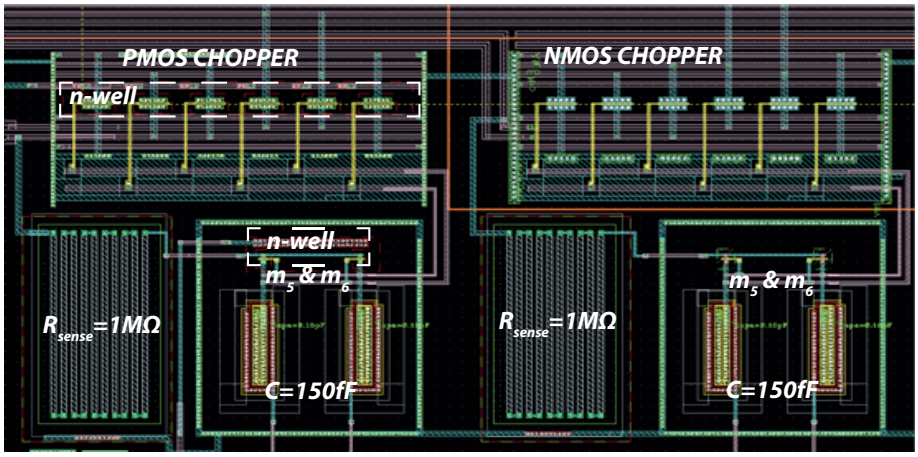


Figure 36.Layout of the front-end chopper.

3.4 Test Chip

The proposed chopper is incorporated into the amplifier described in Section 3.1. The choppers CH_1 and CH_2 are replaced by the capacitively-coupled choppers CH_{PMOS} and CH_{NMOS} (Figure 37). Therefore, when configured as an op-amp, the input current is determined by the combination of choppers CH_{PMOS} and CH_{NMOS}. The CH_{PMOS} determines the input current when the amplifier is configured as a CFIA.

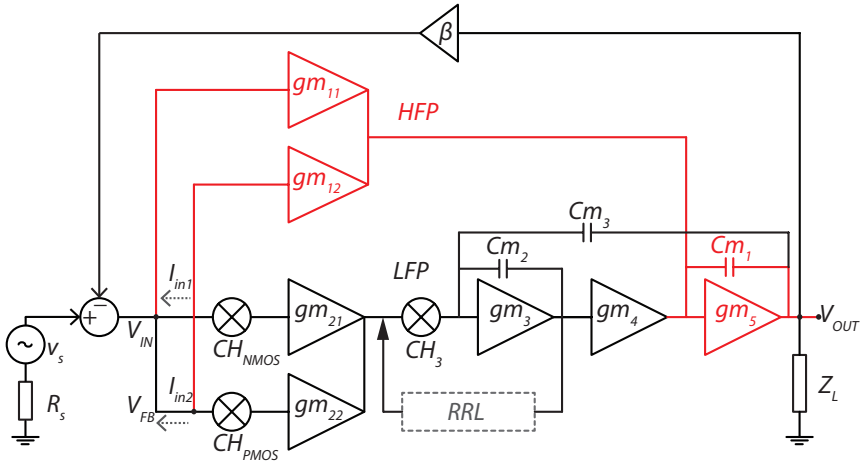


Figure 37. Test chip for this work.

3.5 Simulation setup

In a real life application with high source impedance, the inputs of the amplifier are unequally loaded as shown in Figure 38. Therefore, the input currents are estimated in the simulation in a similar manner by placing a resistor of *1MΩ* in series with each of the inputs.

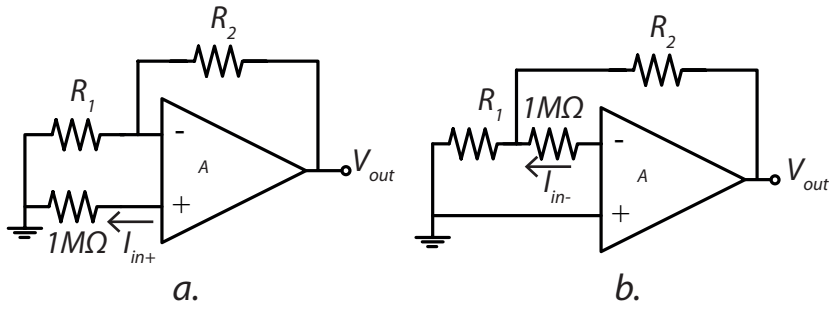


Figure 38. Simulation Setup for estimation of (a) Iin+(b) Iin-

The amplifier amplifies the voltage drop across the series resistor by a closed loop gain defined by R_1 and R_2. The resulting input currents are calculated by,

$$I_{in+} = \left[\frac{V_{out}}{1+\frac{R_2}{R_1}} - V_{os}\right] \cdot \frac{1}{1M\Omega}$$

$$I_{in-} = \frac{-V_{out}}{1M\Omega \cdot \left(1+\frac{R_2}{R_1}\right) - R_2} - \frac{V_{os}}{1M\Omega} \qquad \textit{Equation 21}$$

Where, $'V_{os}'$ is the residual offset of the chopper amplifier.

3.6 Post layout simulation results (op-amp)

Careful layout of the chopper is required to avoid any systematic offset current. Therefore, a post layout simulation is essential to ensure that the chopper layout is symmetrical. The input currents are estimated as a function of input common mode voltage and chopping frequency.

3.6.1 Input current vs. Input common mode voltage (op-amp)

The input currents of the amplifier are estimated as a function of input voltage (V_{in}). The simulation setup shown in Figure 38(a, b) is used to estimate the input currents. The simulation results of the original op-amp [3.1] are presented in Figure 39. As described in section 1.3.4, the use of simple NMOS switches in the input gives rise to a significant dependency on the input common mode voltage. The simulated input currents after the use of the modified capacitively-coupled choppers are presented in Figure 40. This current is mostly due to the charge injection component because the layout of the chopper is symmetrical

and no mismatch is present within the chopper switches. A significant improvement in input currents compared to a simple chopper (Figure 39) is observed in simulations. However, a slight variation of input current is still observed due to bulk-effect (1.3.4).

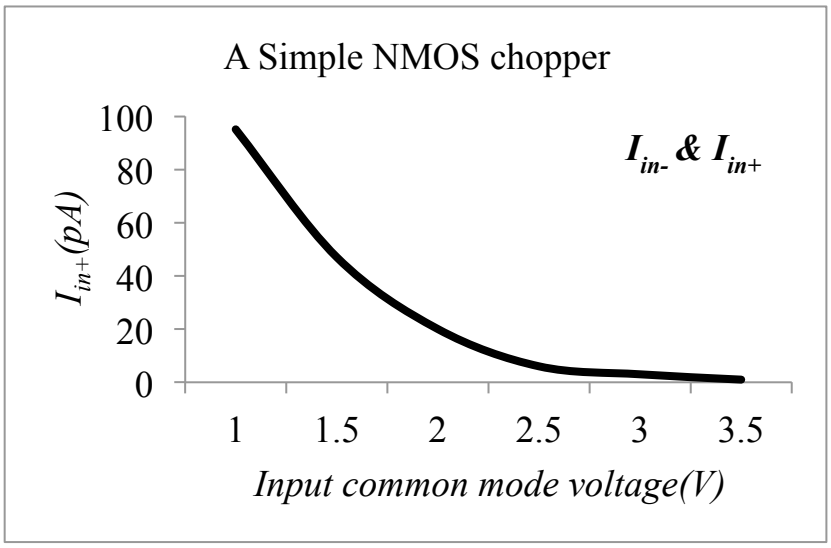


Figure 39. Input current vs. V_{in}. f_{ch}=30kHz.

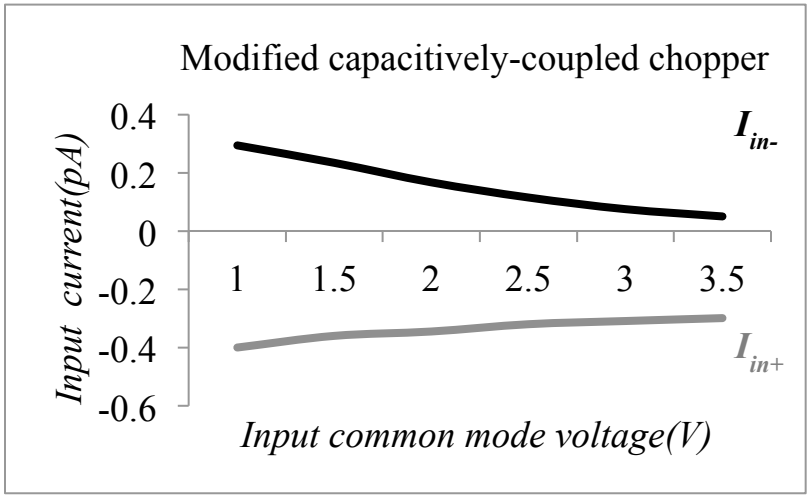


Figure 40.Input current vs. V_{in}. f_{ch}=30kHz. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V

3.6.2 Input current vs. chopping frequency (op-amp)

The variation of input current with chopping frequency of the original op-amp is presented in Figure 41. The input current increases linearly with chopping frequency. The behavior of input current after the use of the modified capacitively-coupled choppers is presented in Figure 42. Compared to the original op-amp (Figure 41), a significant improvement in input current even at higher chopping frequencies is observed.

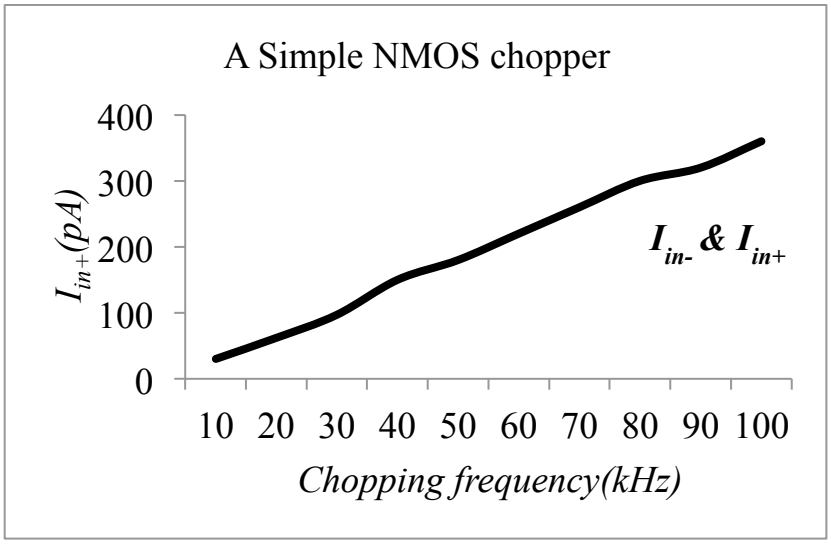


Figure 41. Input current vs. f_{ch}. V_{in}=1V.

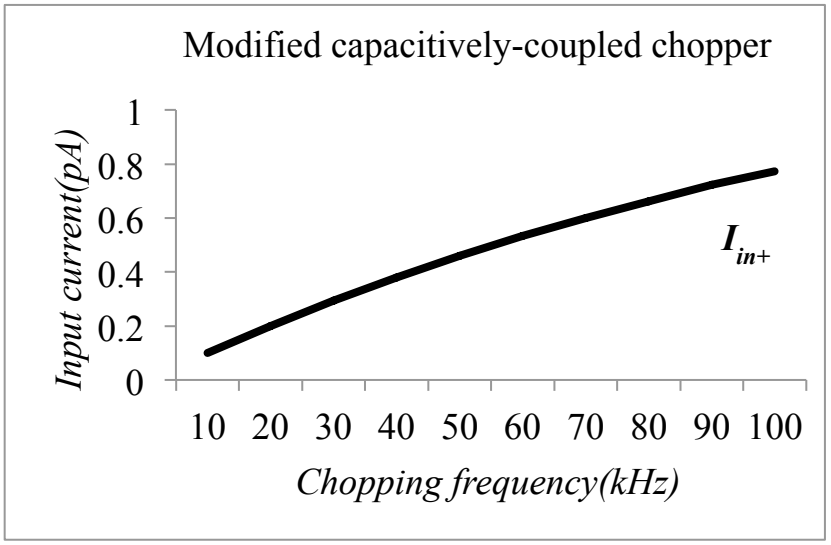


Figure 42. Input current vs. f_{ch}. V_{in}=1V. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V

3.6.3 Monte Carlo simulations (op-amp)

The simulation results presented in sections 3.6.1 & 3.6.2 predict the charge injection component of input current. However, the random mismatch within the input switches is a cause of additional input current due to mismatch within the chopper switches, as discussed in Section 1.3.2. A Monte Carlo simulation is performed on the op-amp with the capacitively-coupled choppers to estimate the component of input current due to random mismatch in input switches. The simulation results are presented in Figures 43-44. A maximum input current of ±20pA is estimated at an f_{ch}=100kHz as shown in Figures 45-46.

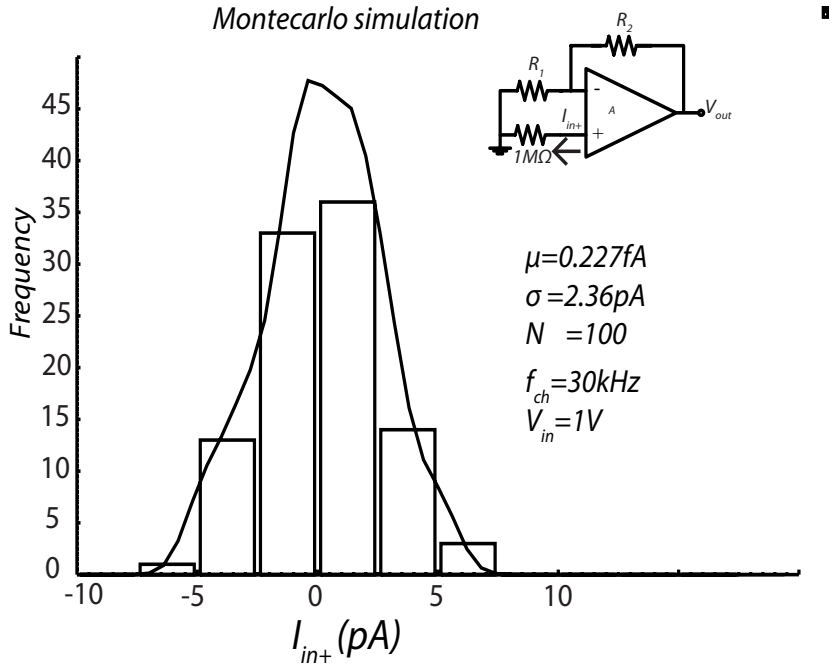


Figure 43. Monte Carlo simulation@ f_{ch}=30kHz,V_{in}=1V. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V.

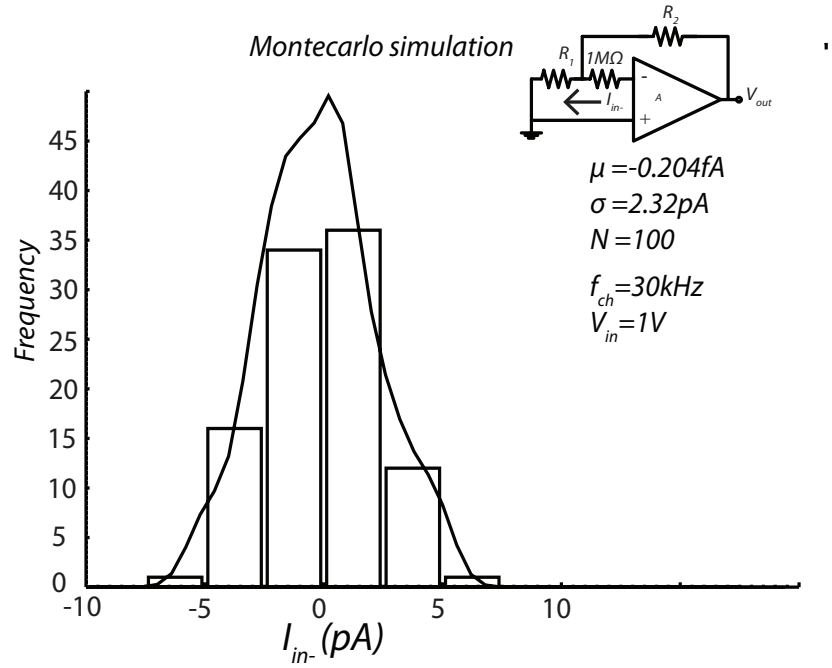


Figure 44. Monte Carlo simulation@ f_{ch}=30kHz,V_{in}=1V. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V.

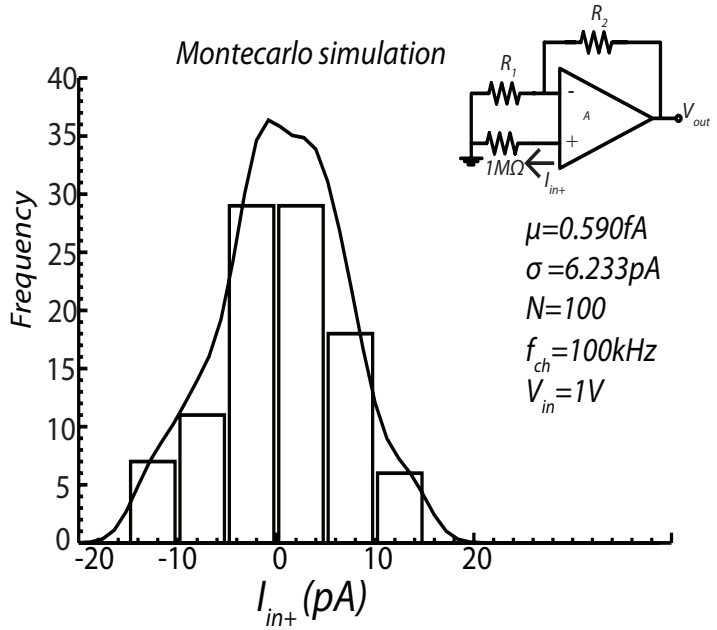


Figure 45. Monte Carlo simulation@ f_{ch}=100kHz, V_{in}=1V. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V.

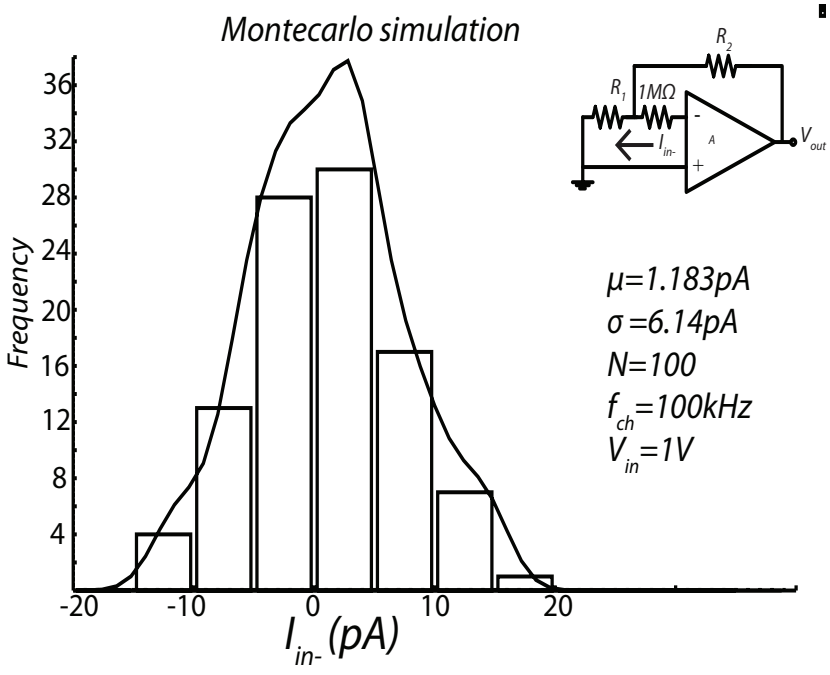


Figure 46. Monte Carlo simulation@ f_{ch}=100kHz, V_{in}=1V. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V.

3.6.4 Noise simulation

The thermal noise floor of the amplifier is predicted to be 10.8nV/$\sqrt{Hz}$ by a PSS/PNOISE simulation. The slight increase of thermal used to noise floor is due to the additional resistance in the signal path. The low frequency noise is shown in Figure 47.

3.7 Summary

In this chapter, a chopping technique to suppress input current is proposed and implemented. Simulation results presented in Section 3.6. A test chip has been implemented to verify the effectiveness of this technique. The Measurement results are given in the next chapter.

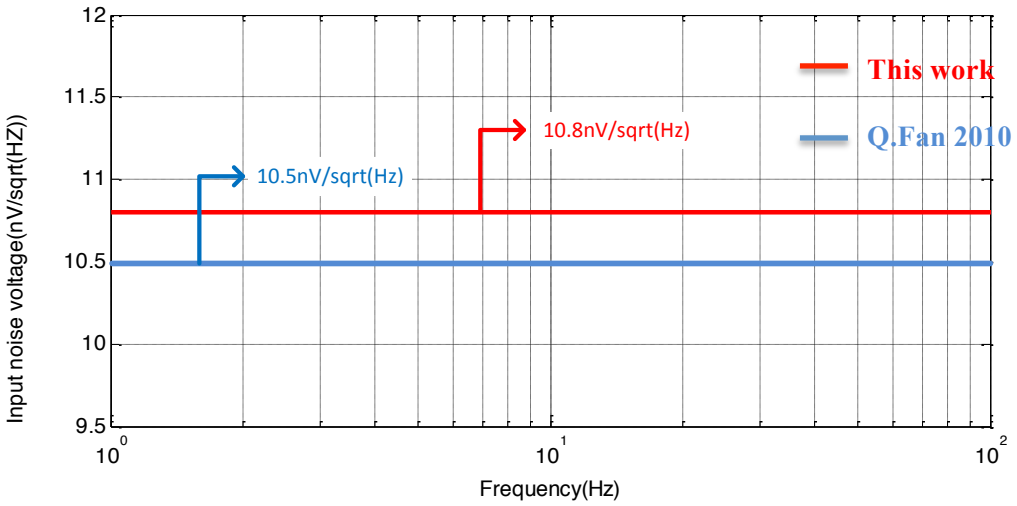


Figure 47. Input noise voltage density @ fch=30kHz. ΔV_{PMOS}=2.5V. ΔV_{NMOS}=2.5V.

3.8 References

[3.1] Qinwen Fan; Huijsing, J.H.; Makinwa, K.A.A.; "A 21 nV/$\sqrt{Hz}$ Chopper-Stabilized Multi-Path Current-Feedback Instrumentation Amplifier With 2 μV Offset," *Solid-State Circuits, IEEE Journal of*, vol.47, no.2, pp.464-475, Feb. 2012.

[3.2] Rong Wu; Makinwa, K.A.A.; Huijsing, J.H.;, "A chopper current-feedback instrumentation amplifier with a 1mHz $1/f$ noise corner and an AC-coupled ripple-reduction loop," *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, vol., no., pp.322-323, 323a, 8-12 Feb. 2009.

[3.3] R. Eschauzier, R. Hogervorst, and J. Huijsing, “A programmable 1.5 V CMOS Class-AB operational amplifier with hybrid nested miller compensation for 120 dB Gain and 6 MHz UGF,” *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1497–1504, Dec. 1994.

[3.4] Qinwen Fan, Johan Huijsing, and Kofi Makinwa, “A Capacitively Coupled Chopper Instrumentation Amplifier with a ±30V Common-Mode Range, 160dB CMRR and 5μV Offset”, *ISSCC2012.*

[3.5] Abo, A.M.; Gray, P.R.; "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” Solid-*State Circuits, IEEE Journal of*, vol.34, no.5, pp.599-606, May 1999.

[3.6] Y. Kusuda, “A 5.9nV/√Hz Chopper Operational Amplifier with 0.78μV Maximum Offset and 28.3nV/°C Offset Drift”, *ISSCC Dig. Tech. Papers*, pp. 242-243, 2011.

[3.7] F. Witte, PhD thesis, 2008.

4 Measurement results

In the previous chapter, the implementation of a low-input-current chopper amplifier was discussed. This chapter presents the results of measurements on the fabricated chips and is organized as follows: Section 4.1 describes the fabricated devices and briefly discusses the test setup. Section 4.2 describes the measurement procedure. Sections 4.3 and 4.5 discusses the DC and AC measurement results respectively. The measurement results are summarized in Section 4.6.

4.1 Fabricated devices and test setup

The test chip was implemented in Euro-practice's *CMOS 0.7um* process. This is a CMOS process with a minimum feature size of 0.7*um*. Figure 48 shows the chip micrograph. A DIP-24 package is used for packaging the samples. A total of 10 devices were measured.

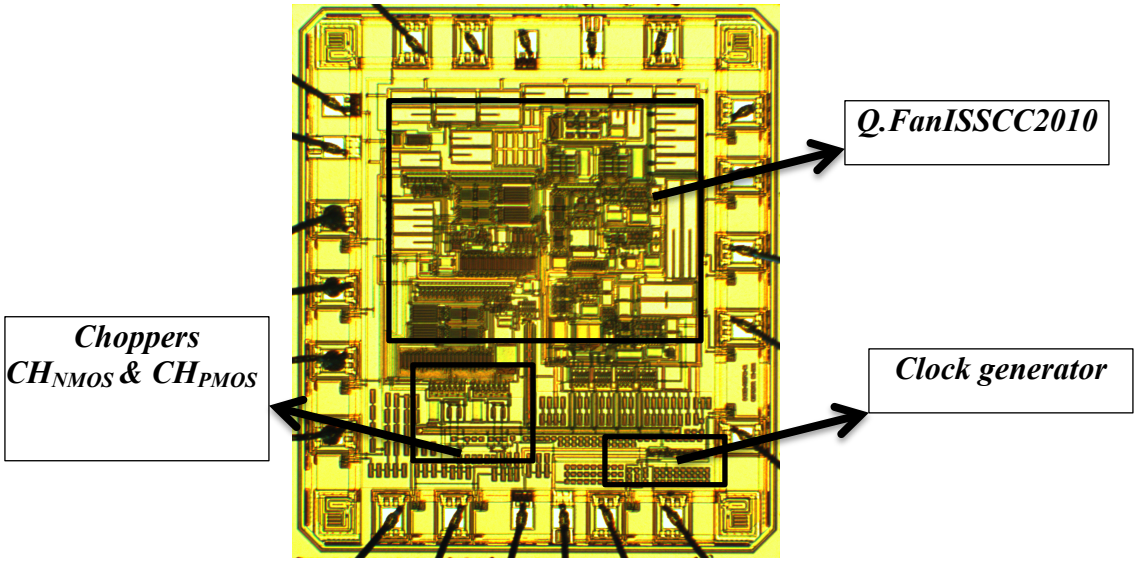


Figure 48. Chip micrograph.

A test PCB was designed to evaluate the performance of the test chip. Figure 48 shows the block diagram of the test setup. The amplifier is configured as an op-amp by shorting the input and feedback transconductors as described in (section 3.1). In order to measure input current (<100pA), resistors of 1MΩ are inserted in series with each of the input and the voltage source (Figure 41). A closed loop gain of 1000 is employed to amplify the voltage drop introduced by the input currents. The pins 'V_{DDPMOS}' and 'V_{DDNMOS}' are used for controlling the amplitude of the clock signals applied to NMOS and PMOS

choppers and thereby varying their input currents contributions respectively. A 'KEITHLEY 2002 DMM' measures the output, 'V_{out}' of the op-amp. Appropriately choosing configurations for the jumpers performs a set of four DC measurements as given in Table 7.

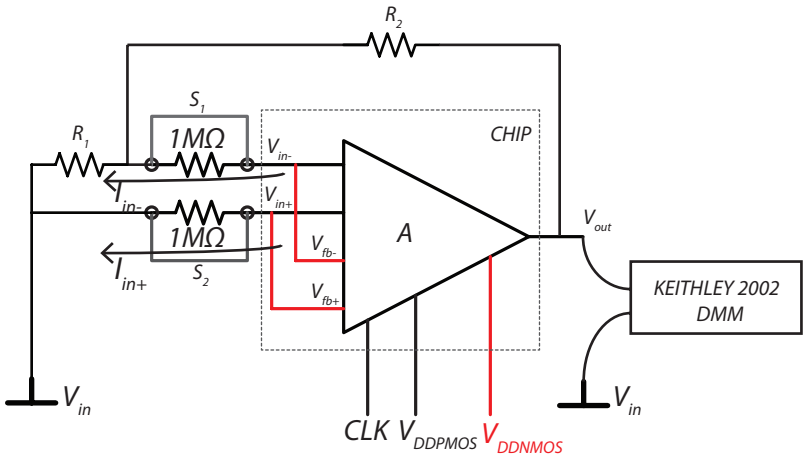


Figure 49. Measurement setup for DC measurements.

Table 7.Configuration for DC measurement.

Step Number	Configuration (S_1, S_2)	DC Measurement performed
1.	ON, ON.	Vos
2.	OFF, ON.	Vos - I_{in-}*1MΩ
3.	ON, OFF.	Vos + I_{in+}*1MΩ
4.	OFF, OFF.	Vos + I_{os}*1MΩ

4.2 Measurement procedure

The four DC measurements, which can be performed by the measurement setup, are given in Table 7. A few calculations are needed to arrive at Input currents. Firstly, the step1 is performed to measure offset voltage. Later, this offset voltage is subtracted from the measurements in Steps 2,3&4 to extract the contribution of input currents. For example, if the current, 'I_{in+}', has to be estimated, the following calculation has to be performed after Steps 1 and 3.

$$I_{in+} = [\frac{V_{out}}{1+\frac{R_2}{R_1}} - V_{os}] \cdot \frac{1}{1M\Omega} \qquad \textit{Equation 22}$$

The influence of input common mode voltage and chopping frequency on input current is measured. The input currents 'I_{in+}' and 'I_{in-}' are presented; a higher emphasis is laid on the current through the non-inverting input, which is of greater concern to this work.

4.3 DC Measurement Results (op-amp)

This section presents the measurement results of offset and input current. To measure the DC value accurately, Keithley 2002 multimeter was used.

4.3.1 Residual offset

To determine the offset of the op-amp, the input terminals of the amplifier were shorted to a DC common mode voltage V_{in} ($1V$). The feedback network was set such that the amplifiers closed loop gain is 1000. A high gain setting is used such that the resulting output offset is at mV levels (for offsets at the μV level) and can be precisely measured. The DC value at the output, when divided by 1000 gives the input referred offset. The offset measurements are performed at 30 kHz. Figure 50 shows the histogram of the input referred offset voltage for the measured devices with a CMOS chopper. From the histogram, the worst-case offset value is $2\mu V$.The residual offset distribution in the case of a PMOS and NMOS choppers are presented in Figures 51-52. An increase in residual offset compared to a CMOS chopper is observed in both the cases.

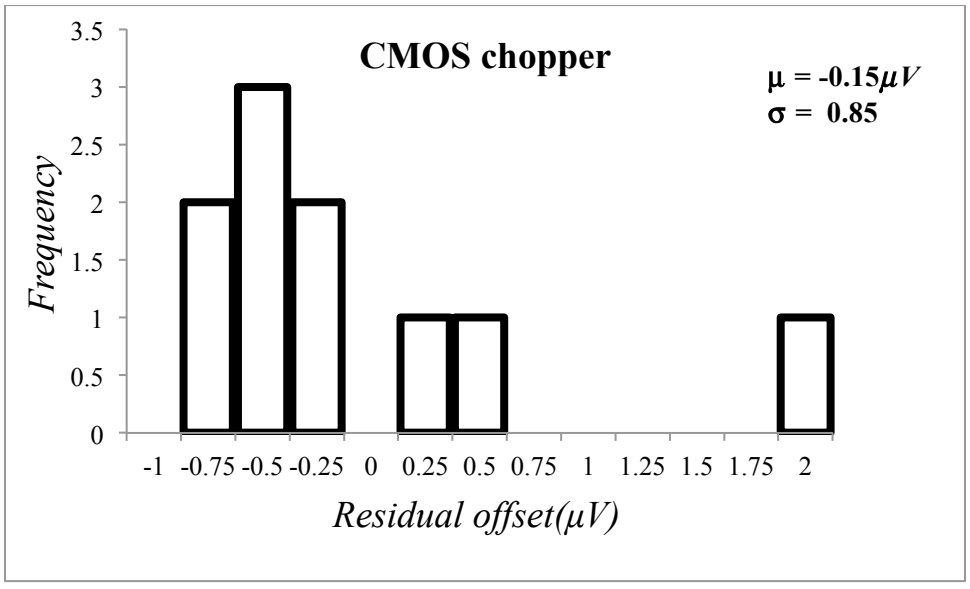


Figure 50. Histogram of residual offset for the op-amp. f_{ch}=30kHz,Vin=1V.CMOS chopper.

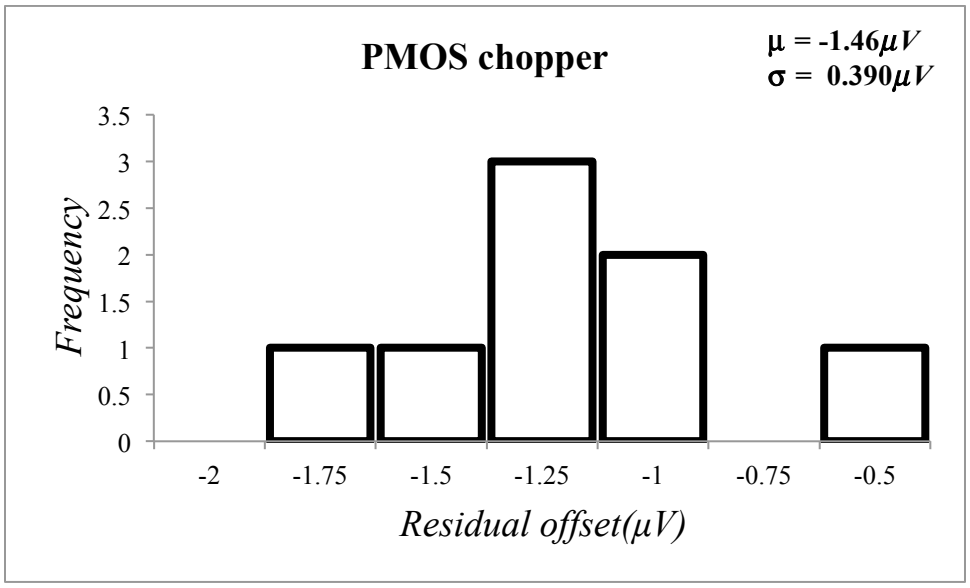


Figure 51. Histogram of residual offset for the op-amp. f_{ch}=30kHz,Vin=1V.PMOS chopper.

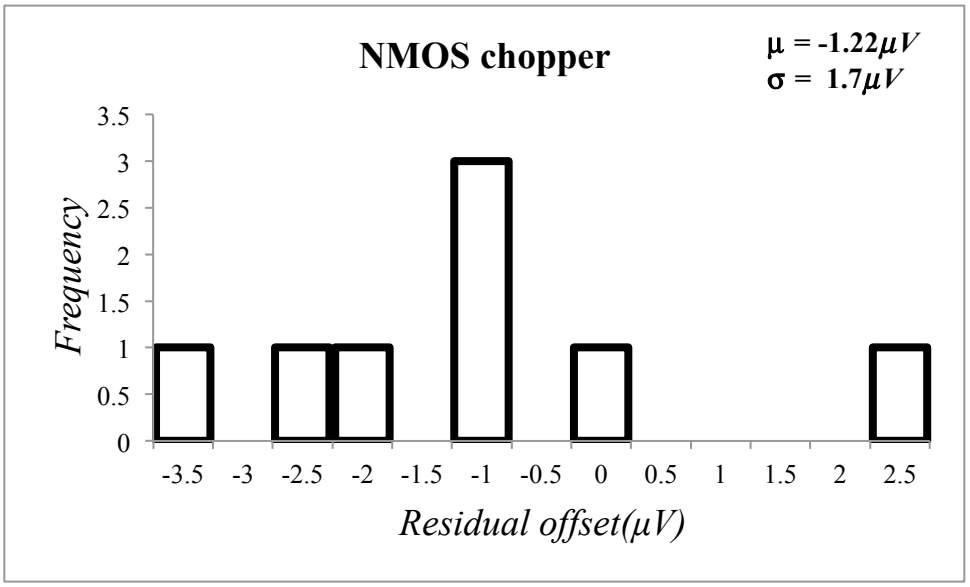


Figure 52. Histogram of residual offset for the op-amp. f_{ch}=30kHz,Vin=1V.NMOS chopper.

Remarks

A higher residual offset voltage is observed when a PMOS or an NMOS chopper is used instead of a CMOS chopper. The following phenomenon could have resulted in an increased offset:

- As compared to a CMOS switch, the PMOS and the NMOS switches have a higher on-resistance.
- In the low frequency path (LFP) (Section 3.1), the effective transconductance is halved.

4.3.2 Input currents in CMOS chopper (Untrimmed)

To measure the input currents of the op-amp, the procedure described in Section 4.2 is followed. The magnitude of the input current and its variation with input voltage (V_{in}) is measured. In the initial measurement, both NMOS and PMOS choppers are operated with equal clock amplitudes (ΔV_{NMOS} & $\Delta V_{PMOS}=2.5V$). The measured values of input currents are reported in Figure 53. The measured offset current is reported in Figure 54. The magnitude and the common mode variation of the input current, I_{in+} is approximately (50pA/V max) and is significantly larger than predicted by the simulations (section 3.6.3). The thick dotted lines represent the mean input current of the devices.

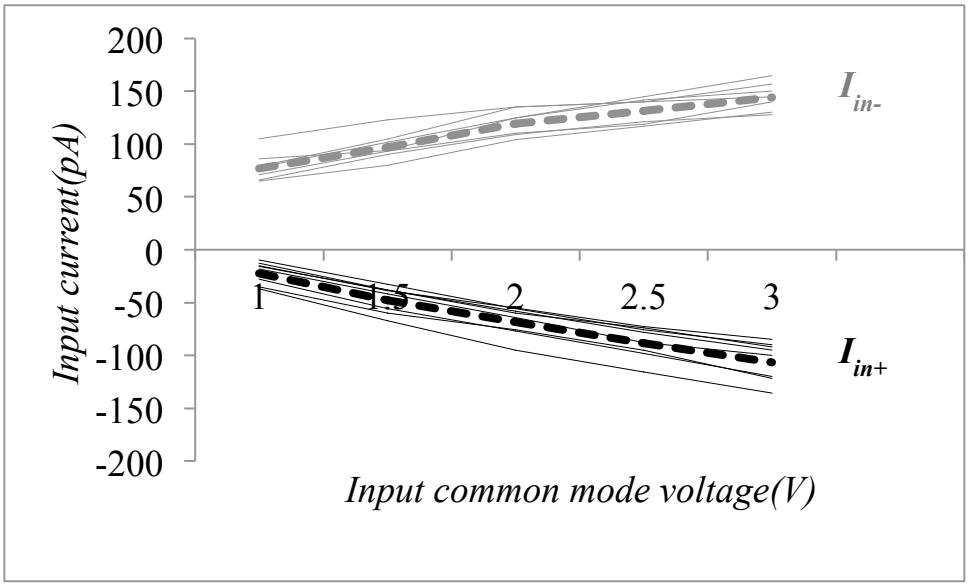


Figure 53. Input current vs. input voltage. f_{ch}=30kHz.

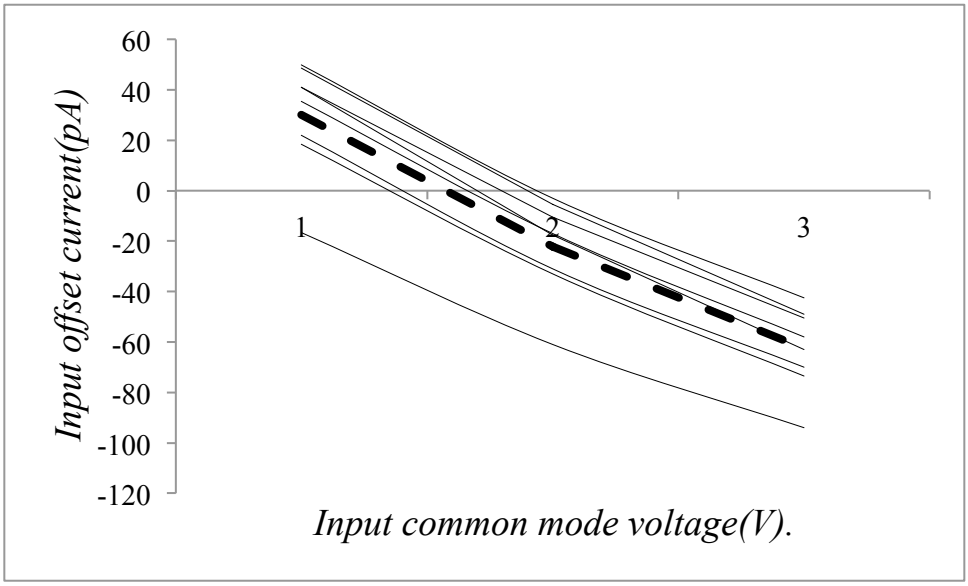


Figure 54. Input offset current vs. input voltage. f_{ch}=30kHz.

4.3.3 Input currents in PMOS chopper (Untrimmed)

The performance of the PMOS chopper is tested by adjusting the ($\Delta V_{PMOS}=2.5V, \Delta V_{NMOS}=0V$). In this scenario, the NMOS chopper is switched off and the input of one of the transconductors is floating. The measured values of the input currents are presented in Figure 55. The input current, I_{in+} is more stable (7pA/V), which is at least 7X better than a CMOS chopper. In Figure 56, offset current in the PMOS chopper is presented. The thick dotted lines represent the mean input current of the devices.

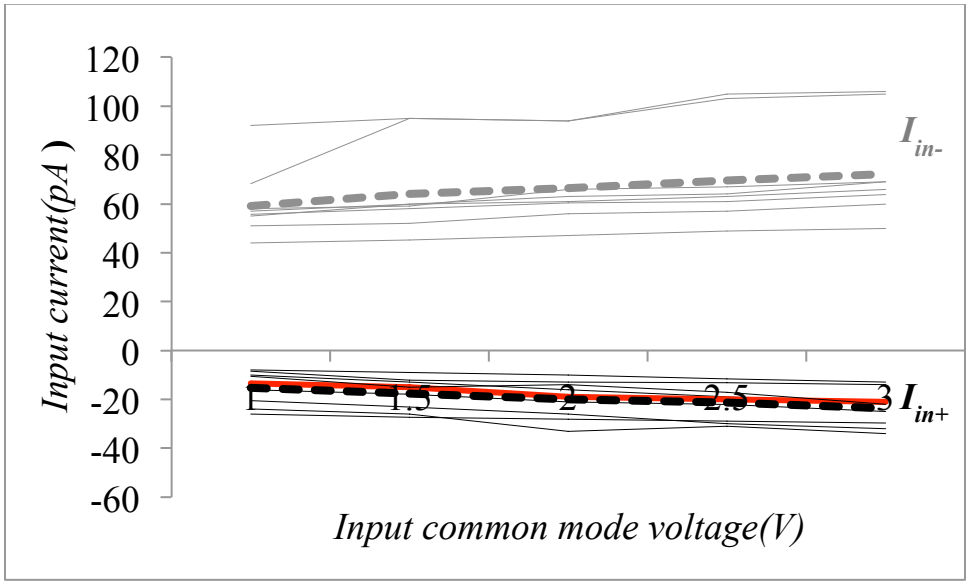


Figure 55. Input current vs. input voltage. f_{ch}=30kHz.

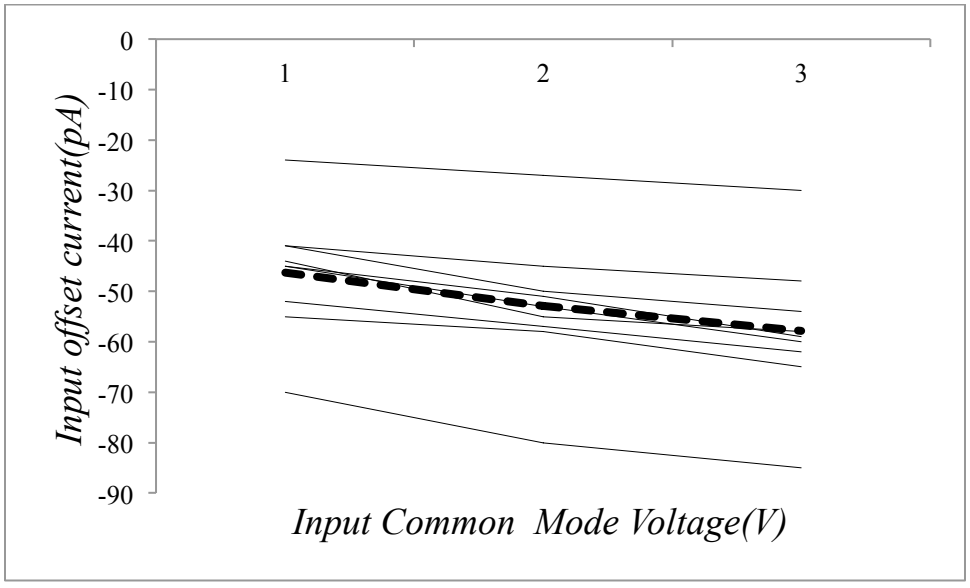


Figure 56. Input offset current v. input voltage. f_{ch}=30kHz.

4.3.4 Input currents in NMOS chopper (Untrimmed)

The input currents introduced by an NMOS chopper are shown in Figure 57. The magnitude and also the variation of input current, I_{in+} with input common mode voltage is 4X larger (25pA/V) than in the case of input current in a PMOS chopper. The common mode behavior of the input currents of a CMOS chopper are mainly determined by input currents of its NMOS chopper (section 4.3.4). The thick dotted lines represent the mean input current of the devices. In the next section, the frequency behavior of input currents will be presented.

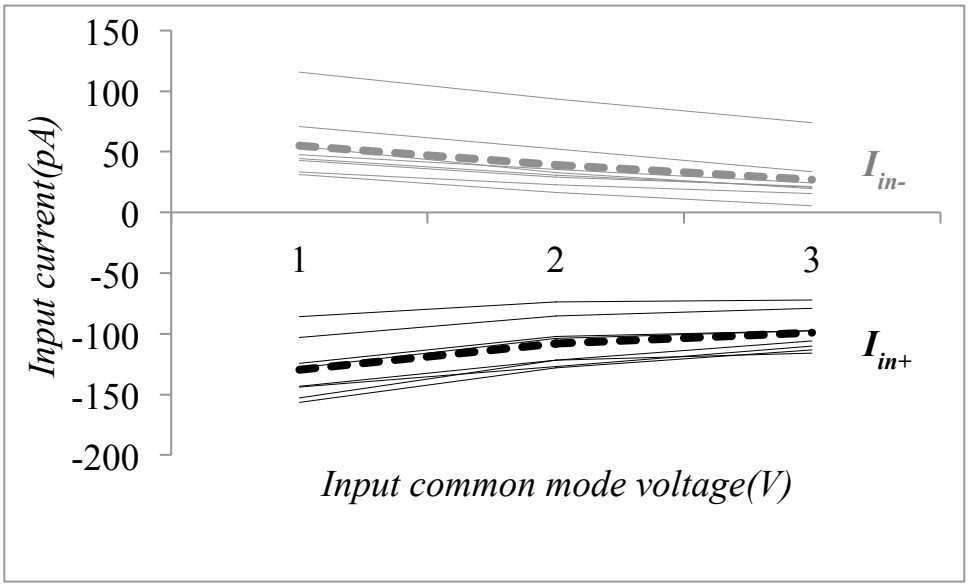


Figure 57. Input current vs. input voltage. f_{ch}=30kHz.

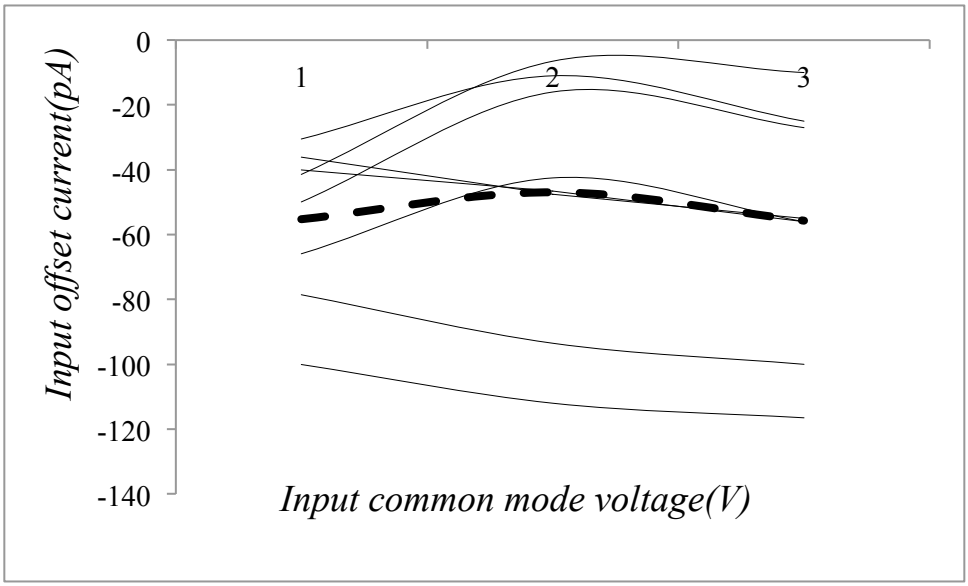


Figure 58. Input offset current vs. input voltage. f_{ch}=30kHz.

4.3.5 Frequency behavior of input current

In Figure 59, the input current through the non-inverting input (I_{in+}) of the amplifier is presented. The input current in the chopping frequency range of interest (30kHz - 100kHz) is minimal in the case of a PMOS chopper. In addition to lower magnitude, the variation of input current with input common mode voltage is significantly smaller compared to NMOS and CMOS choppers, as explained in the previous discussion. The goal of this work is to maintain a stable input current (<20pA) with input common mode voltage unto an $f_{ch}=100kHz$. Therefore, in this design, a stable input current is only possible by the use of a PMOS chopper (section 4.3.3). Hence, Trimming the clock amplitude (ΔV_{PMOS}), as described in section 3.2.2 is employed to suppress the input current further. The trimming procedure and the results are presented in the next section.

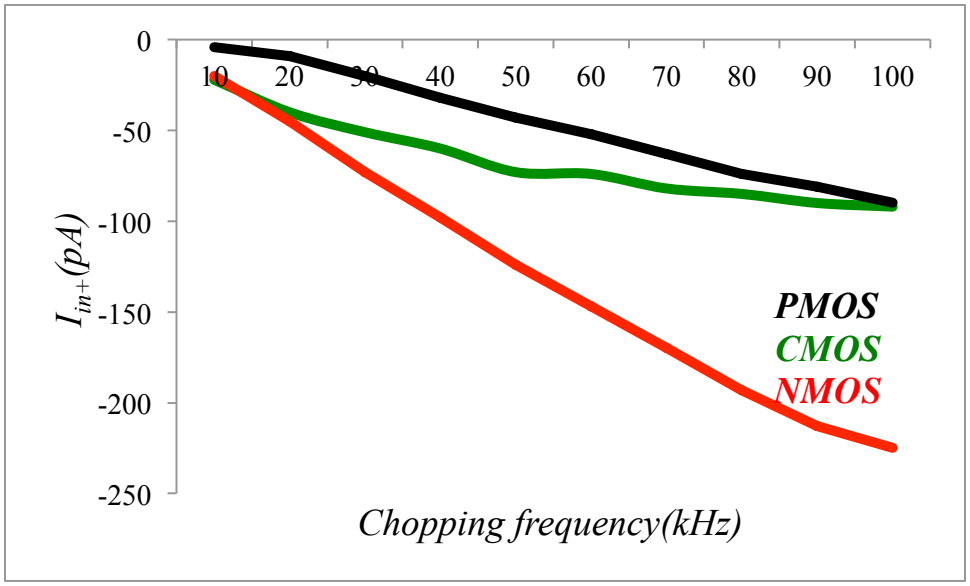


Figure 59. Input current vs. f_{ch}. $V_{in}=2V$

4.3.6 Input currents in a PMOS chopper (Trimmed)

To perform the trimming, a device closer to the mean (shown red in Figure 55) is taken and the input current (I_{in+}) as a function of clock amplitude (ΔV_{PMOS}) is studied, as illustrated in Figure 60. In a 5V supply, the trim is performed at an input common mode voltage ($V_{in}=2.5V$). Measurement suggests that clock amplitude of ($\Delta V_{PMOS}=2V$) yields a negligible input current. The trimmed input current of 10 devices is presented in Figure 61. The target specification of +/-20pA has been achieved after performing the trim. After the trim, the input current, I_{in+} varies with a slope of 4.5pA/V with the input common mode voltage even at an f_{ch}=100kHz.The spread within the devices is due to the random mismatch within the switches in the chopper. The frequency behavior of a trimmed device is shown in Figure 62.

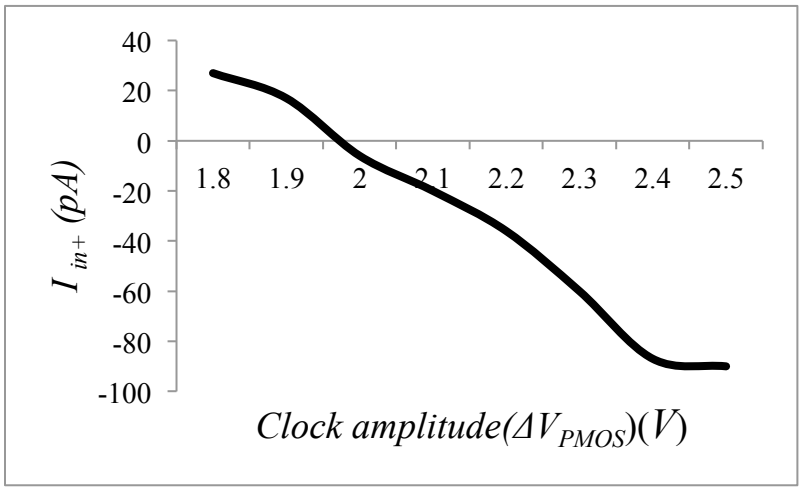


Figure 60. Clock amplitude trimming in a typical device. V_{in}=2.5V

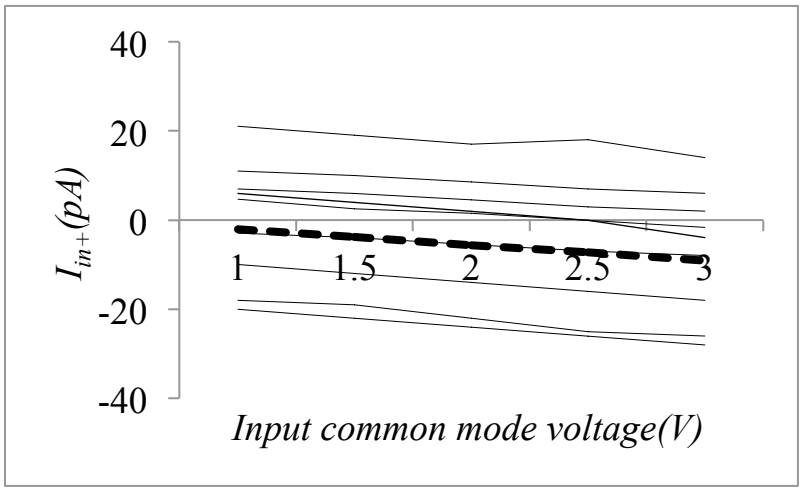


Figure 61. Trimmed input current (I_{in+}) vs. V_{in}. @ f_{ch}=100kHz. ΔV_{PMOS}=2V. ΔV_{NMOS}=0V.

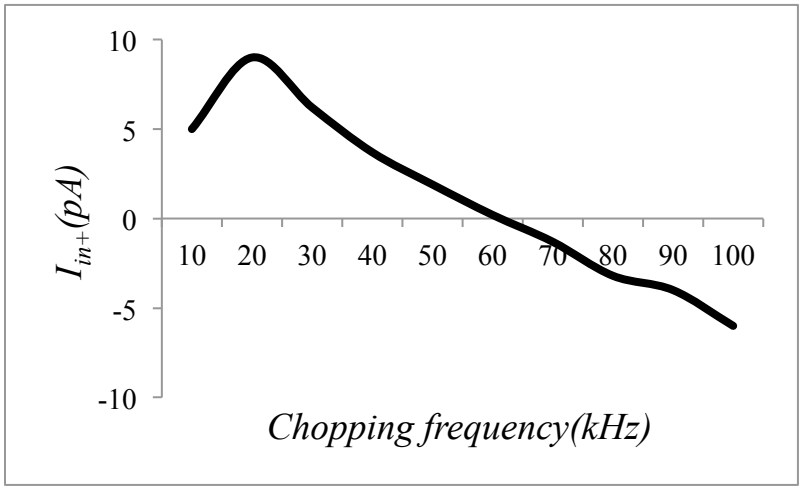


Figure 62. Input current vs. chopping frequency.

4.4 DC Measurement Results (CFIA)

Next, the amplifier is configured as a CFIA (Figure 63). The PMOS chopper determines the input current in a CFIA (section 3.4). The residual offset and input currents of the CFIA are presented next.

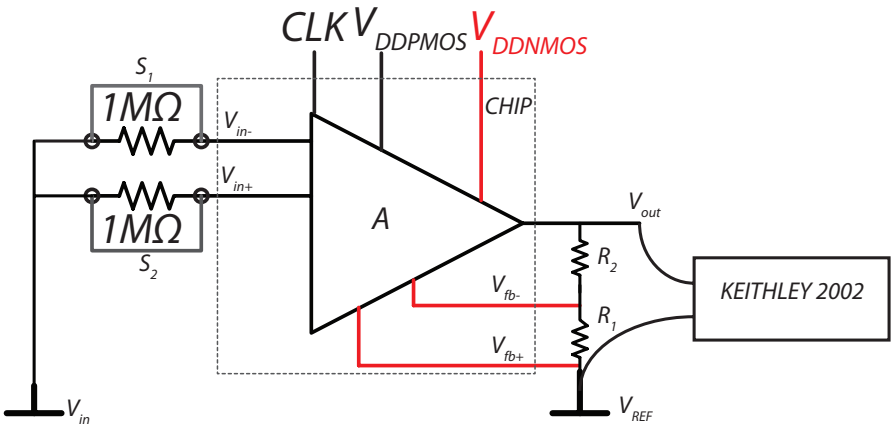


Figure 63. Test setup for DC measurements (CFIA)

4.4.1 Residual offset (PMOS chopper)

To estimate the residual offset in a CFIA, the procedure explained in section 4.3.1 is followed. The result is presented in Figure 64.

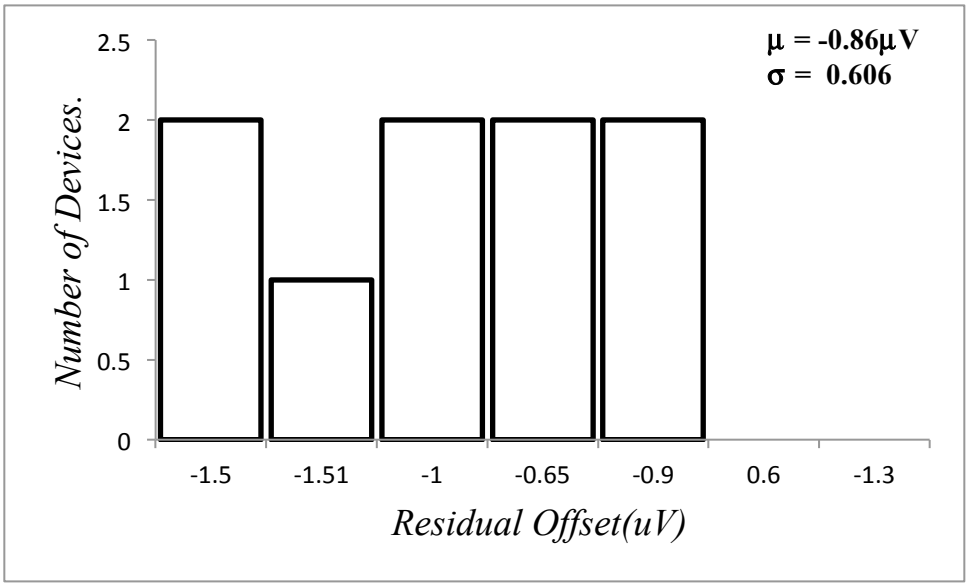


Figure 64. Histogram of residual offset in CFIA. @f_{ch}=30kHz.

4.4.2 Input currents (PMOS chopper)

The PMOS chopper determines the input current in the CFIA (Section 3.4), the magnitude and common mode variation of the input current(Figure 65) is comparable to the case of an op-amp, when only the PMOS chopper is functional (Figure 55). The thick dotted lines represent the mean input current of the devices.

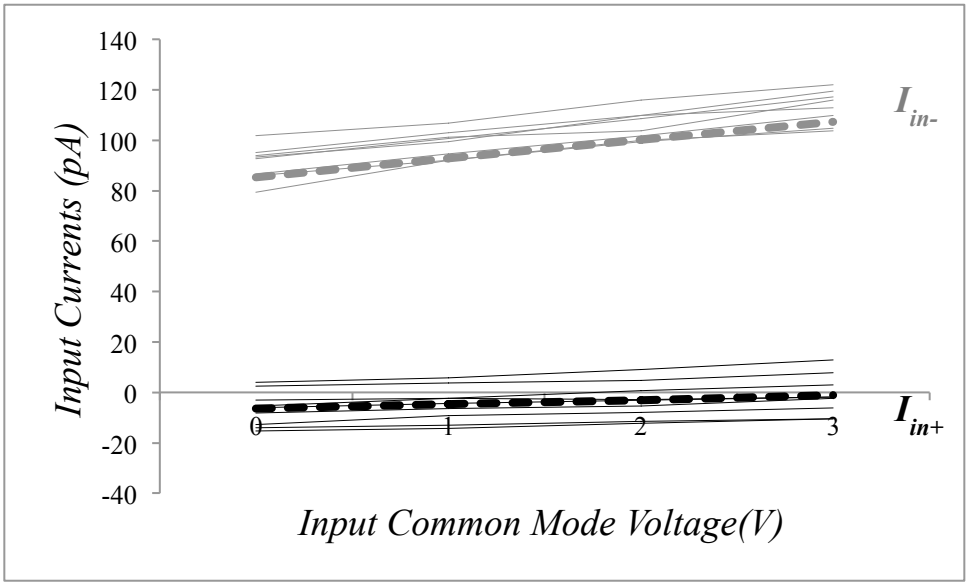


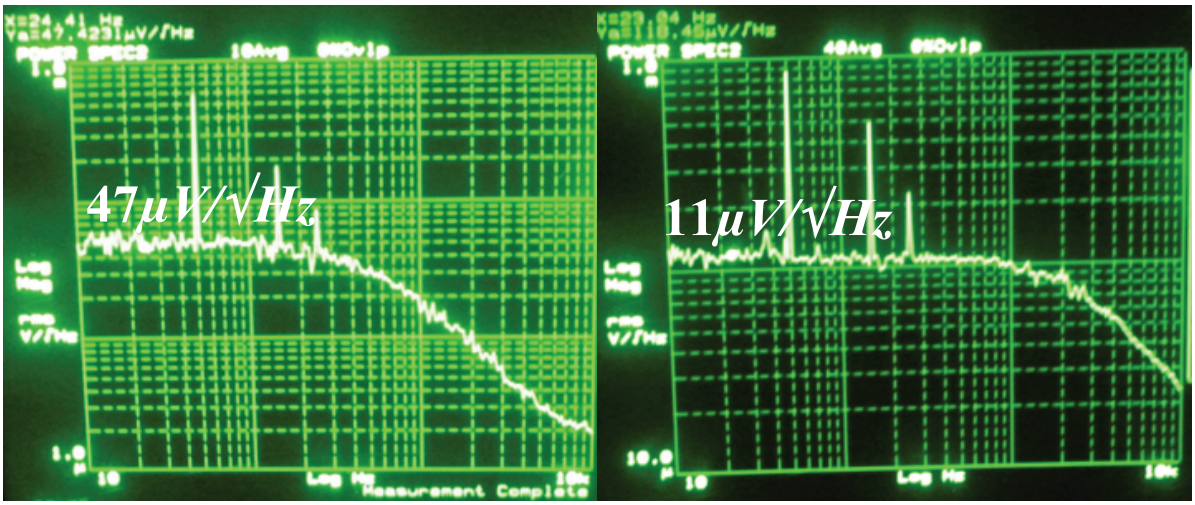
Figure 65. Input currents vs. V_{in} in a CFIA. @ f_{ch}=30kHz. ΔV_{PMOS}=2.5V.

4.5 Noise measurement results

This section is dedicated to the measurements of AC performance of the amplifier. It presents two AC measurements, i.e., Voltage noise (v_n) and current noise (i_n). The voltage noise of this amplifier is measured at a chopping frequency (f_{ch})=*30kHz* and $\Delta V_{NMOS,\ PMOS}$=*2.5V*.The current noise is measured at two different chopping frequencies (f_{ch}=*30kHz & 100kHz*).

4.5.1 Voltage noise (v_n)

To perform the noise measurement, the input of the amplifier was shorted and the amplifier was set to a gain of 1000X. Figure 66 shows the plot of the output noise with chopping in a CFIA (2000X gain) and op-amp (1000X gain). At low frequencies, the input referred noise can be evaluated by dividing the output noise by closed loop gain. The input referred voltage noise floor after chopping is found to be 11 *nV/√Hz* in the case of op-amp and 23.5 *nV/√Hz* in the case of CFIA, which agrees with the analysis in the previous chapter.



a. *b.*

Figure 66. Output noise of (a). CFIA (b). Op-amp.

4.5.2 Current noise (i_n)

The current noise measurement is an indirect measurement, where a *1MΩ* resistor is connected in series with the source (Figure 67) in order to convert the current noise into a voltage noise, which can be sensed by the amplifier. The value of the resistance should satisfy the following condition,

$$i_n{}^2 R_S{}^2 \gg 4KTR_S \qquad \textit{Equation 23}$$

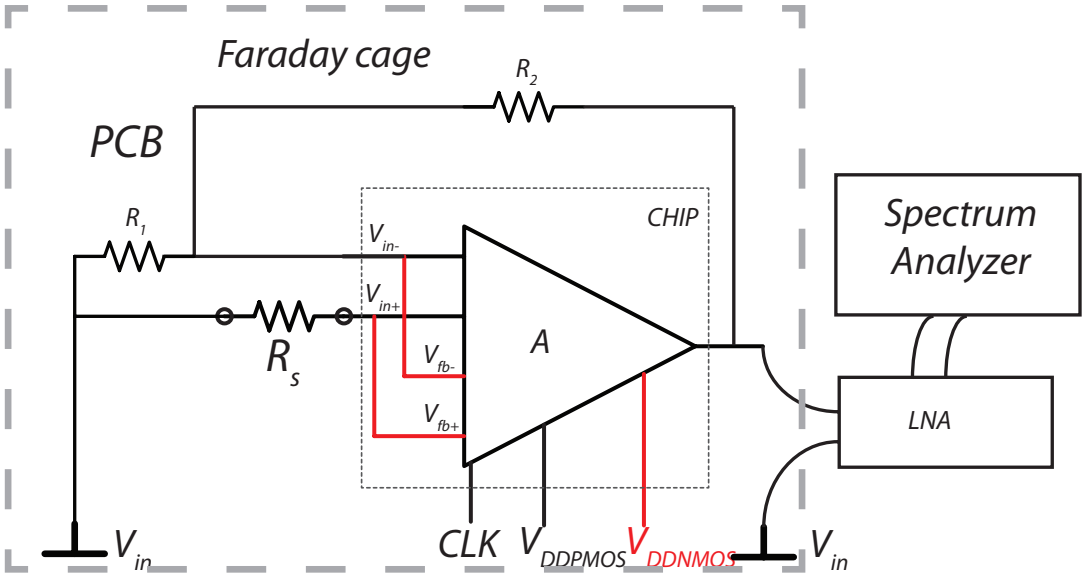


Figure 67.Measurement setup for current noise.

In this design, R_S=1MΩ in order to accurately measure i_n. A faraday cage is used to prevent any environmental noise from interfering with the source impedance.

The following steps are needed before computing (i_n).

- Measure voltage noise (v_n).
- Measure total noise due to v_n, i_n and thermal noise contribution of R_S (v_{tot}).
- Subtract the contribution of voltage noise and thermal noise of the resistor.

The current noise in can be given by,

$$i_n = \frac{\sqrt{{v_{tot}}^2 - {v_n}^2 - 4KTR_S}}{R_S} \qquad \textit{Equation 24}$$

The measured current noise at two different chopping frequencies is presented in Table 8. The input current noise is approximately $\sqrt{3}$X smaller in the PMOS chopper due to its lower channel mobility (μ), as $i_n \propto \sqrt{\mu}$. The current noise also scales with the square root of the chopping frequency, i.e., $i_n \propto \sqrt{f_{ch}}$ and agrees with the discussion in section 1.3.5. The current noise measurement may not be yielding accurate results due to the presence of the common mode sensing resistor.

Table 8. Measured current noise at two different chopping frequencies.

	Current noise ($fA/\sqrt{Hz}$)	
Type of chopper	**@ 30*kHz***	**@ 100*kHz***
PMOS	182	300
NMOS	331	510
CMOS	500	750

4.6 Summary

The performance of the amplifier with each of the chopper configurations is summarized in Table 9. The total residual offset as a function of source impedance in a CMOS, PMOS and NMOS choppers is illustrated in Figure 68. The common mode variation of the input current (I_{in+}) and also its magnitude are significantly smaller in the case of a PMOS chopper compared to an NMOS and a CMOS chopper. The possible reasons for the better performance of the PMOS chopper are:

- The charge injection compensation mechanism in a PMOS chopper might be better than in an NMOS chopper.
- The PMOS chopper is placed in an n-well, which is completely isolated from the noisy p-substrate.

Table 9. Comparison of CMOS, NMOS and PMOS choppers.

	V_{os} (uV)	I_{in+}(pA) @ 100kHz	i_{in}($fA/\sqrt{Hz}$)	v_n($nV/\sqrt{Hz}$)	Input current variation (pA/V)
CMOS Chopper (Untrimmed)	2	-90	750	11	50
NMOS Chopper (Untrimmed)	-3.5	-225	510	---	25
PMOS Chopper	-1.7	-23 (Single trim) (Worst case)	300	---	4.5

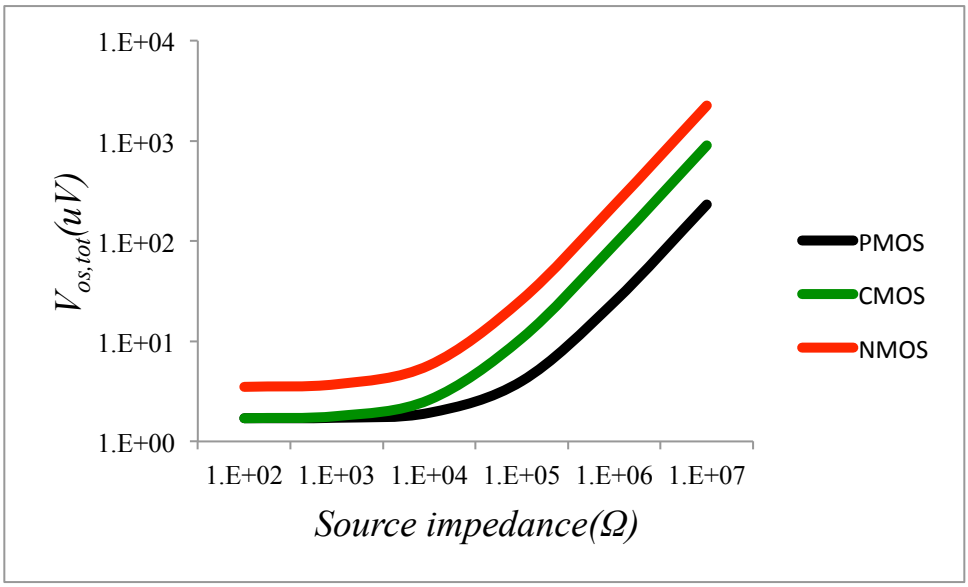


Figure 68. Residual offset as a function of source impedance with CMOS, NMOS and PMOS choppers. @ fch=100kHz.

4.7 References

[4.1] Qinwen Fan; Huijsing, J.H.; Makinwa, K.A.A.; "A 21 nV/$\sqrt{Hz}$ Chopper-Stabilized Multi-Path Current-Feedback Instrumentation Amplifier With 2 μV Offset," *Solid-State Circuits, IEEE Journal of*, vol.47, no.2, pp.464-475, Feb. 2012.

[4.2] Rong Wu; Makinwa, K.A.A.; Huijsing, J.H.; "A chopper current-feedback instrumentation amplifier with a 1mHz $1/f$ noise corner and an AC-coupled ripple-reduction loop," *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, vol., no., pp.322-323, 323a, 8-12 Feb. 2009.

[4.7] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset", *IEEE J. Solid-State Circuit*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000

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5 Conclusions and future work

In the previous chapter, the measurement results of the low-input current chopper amplifier are presented. The performance of the three different chopper configurations is studied. Through trimming, the target specification for input current(I_{in+}) in this work is achieved. In this chapter, the conclusions are drawn from the measurement results and this work is compared to the state-of-the-art. Based on the insight gained through the measurement results, recommendations for future work are given.

5.1 Comparison of this work (with a PMOS chopper) with the state-of-the-art

This design is compared to the state-of-the art chopper amplifiers. As seen from Table 10, the offset voltage work is in line with the current State-of -the-art. An improvement of 2.5X in input currents has been achieved compared to [5.1]. Compared to the original amplifier [5.3], a 3X improvement is achieved. The input referred noise voltage is degraded compared to [5.3], when only PMOS chopper is made functional. This is because; the effective input transconductance in the low frequency path is halved. Therefore, the noise measurement with a single chopper does not meet the expected performance.

Table 10. The state-of-the-art table.

	ADA4528 [5.1]	ADA4051 [5.2]	Q.Fan [5.3]	This work With a PMOS chopper
Input Offset (uV)	0.300	2	1	-1.7
Input current *(pA)*	200	50	70	23
Input noise voltage *(nV/√Hz)*	5.9	95	10.5	18
Current noise (*fA/√Hz*) @1kHz	500	100	--	300
f_{ch} (*kHz*)	200	50	30	100

5.2 Conclusions and Future work

This thesis has presented the design, implementation and measurements of a chopper amplifier with low input currents. This design advances the state-of-the-art in chopper amplifiers by achieving a 2.5X improvement in input current compared to the state-of-the-art [5.2].

The front-end-chopper designed for this work is optimized for low input current. The PMOS chopper meets the specifications for this work. However, in the NMOS chopper, the magnitude and variation of input current with input common mode voltage is much higher and not desired. The PMOS chopper is placed in an n-well, which isolates it from the p-substrate. This could be a possible reason for the superior performance of the PMOS chopper. It is worthwhile to investigate the performance of an NMOS chopper in a p-well.

To further reduce the variation of input current with input common mode voltage, the bulk of the switches should be tied to the input common mode voltage, so as to follow the input common mode voltage.

The input common mode voltage in this design is sensed with a sense resistor (R_s)(section 3.2.2). This resistor is a source of impedance mismatch at the amplifier's input and may introduce additional leakage current. Therefore, in the future design a common mode buffer has to be used to truly isolate the input from the clock generation circuitry. In order to reduce the input current spread (device to device), which is observed in this work, nested chopping [5.4] should be used.

5.3 References:

[5.1]. ADA4528 datasheet:
http://www.analog.com/static/imported-files/data_sheets/ADA4528-1.pdf.

[5.2]. ADA4051 datasheet:
http://www.analog.com/static/imported-files/data_sheets/ADA4051-1_4051-2.pdf.

[5.3]. Qinwen Fan; Huijsing, J.H.; Makinwa, K.A.A.; "A 21 nV/$\sqrt{Hz}$ Chopper-Stabilized Multi-Path Current-Feedback Instrumentation Amplifier With 2 μV Offset," *Solid-State Circuits, IEEE Journal of*, vol.47, no.2, pp.464-475, Feb. 2012.

[5.4] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset", *IEEE J. Solid-State Circuit*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.