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Device-Aware Test for Ion Depletion Defects in RRAMs

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***Abstract*—Many companies are heavily investing in the commercialization of Resistive Random Access Memories (RRAMs). This calls for a comprehensive understanding of manufacturing defects to develop efficient and high-quality test and diagnosis solutions to push high-volume production. This paper identifies and characterizes a new defect based on silicon measurements; the defect is called Ion Depletion (ID). In our case study, $45\,\%$ cycles suffered from an intermittent reduction in high resistance state and did not impact low resistance state. The paper shows that the traditional fault modeling based on linear resistors as a defect model is not accurate. To address this challenge, the Device-Aware (DA) defect modeling method is applied; an RRAM model of the defective device is developed and calibrated using measurements to accurately describe the impact of the defect on the electrical behavior of the memory device. Afterward, fault analysis is performed based on the DA defect model, and appropriate fault models are introduced; they show that the ID defect may sensitize undefined state faults. Finally, dedicated test and diagnosis solutions for the ID defect are proposed.**

***Index Terms*—RRAM test, linear resistors, device-aware defect model, fault modeling, Design-for-Testability (DfT)**

I. Introduction

Resistive Random Access Memory (RRAM) is a promising technology for the next generation of non-volatile memories offering advantages such as high integration density, 3D stackability, high cycle endurance, and low access latency [1, 2]. Although they have many benefits, the mass production of RRAM currently faces significant challenges due to the immaturity of the fabrication process, especially as devices scale down [3–5]. It is widely recognized that defects and variations in device characteristics during the manufacturing process, as well as their effect on the outgoing product quality, present serious obstacles [3, 5–8]. The RRAM manufacturing consists of two steps: Front-End-Of-Line (FEOL) and Back-End-Of-Line (BEOL), both of which may result in fabrication defects [9–11]. Furthermore, RRAM manufacturing involves additional steps and the use of new materials, which may result in new failure mechanisms [9–11]. These RRAM-related defects are often complicated and not guaranteed to be detected directly by conventional tests for existing mainstream memory technologies [8, 11]. Therefore, comprehension of the unique RRAM defects and modeling them accurately for high-quality test solutions is of great importance.

Many works have investigated defect modeling and test generation for RRAMs. In 2009, Ginez *et al.* studied coupling faults by modeling bridge defects [12]. In 2012, Haron *et al.* proposed a special Design-for-Testability (DfT) to detect undefined state faults [13]. In 2013, sneak-path testing for RRAMs was presented to reduce the test time [14]. In 2015, Chen *et al.* reported a dynamic write disturbance fault, and a March test to cover it [15]. In 2021, Liu *et al.* developed DfT scheme for 3D hybrid RRAM array [4]. Nevertheless, all these works employ an *linear resistor* to model defects. Although this model may be good enough for interconnects and contacts, it is certainly not accurate enough to describe unique defects in the RRAM device itself, as the device is *non-linear* by nature. To address the limitations of the conventional RRAM test method, the 'Device-Aware Test (DAT)' approach was proposed [8, 16, 17]. The DAT method properly models physical defects, enabling the exploration of realistic fault models and the development of high-quality test solutions. This has been shown to be very powerful for RRAM unique defects such as Intermittent Undefined State Fault (IUSF) [18]. Moreover, as RRAM is an immature technology, more unique defects induced by device miniaturization or new materials, are still to be discovered, understood, and modeled in order to develop optimal test solutions.

This paper investigates and characterizes (based on silicon measurements) a new unique RRAM defect, referred to as an Ion Depletion (ID) defect. An ID defect occurs when insufficient oxygen ions stored near the capping layer/oxide interface can be released during the RESET process, which affects the on/off resistance ratio and leads to undefined state faults. The DAT approach is applied to accurately model the ID defect, derive realistic fault models, and thereafter develop test solutions. The main contributions of this paper are as follows:

- Identify the ID defect based on silicon measurements.
- Present electrical characterization of RRAM devices with the ID defect and analyze the physics causing it.
- Develop the DA defect model for the ID defect and calibrate it with measured electrical characterization.
- Apply the DA defect model to develop appropriate fault models and subsequently optimal test solutions.

The remainder of this paper is organized as follows. Section II establishes the background on RRAM technology. Section III provides characterization of the ID defect. Section IV illustrates the limitations of the conventional defect models and proposes the appropriate DA defect model for the ID defect. Section V applies this model to perform fault modeling and analysis. Section VI develops the test solutions for the ID defect. Finally, Section VII discusses and concludes the paper.

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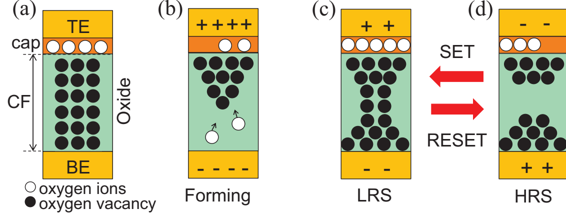

Fig. 1. Evolution of the conductive filament. (a) RRAM stack, (b) Forming, (c) SET, (d) RESET.

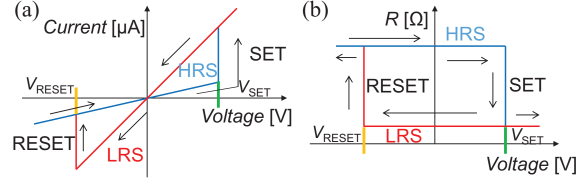

Fig. 2. RRAM electrical switching. (a) Simplified BS switching I-V curve, (b) Simplified BS switching R-V curve.

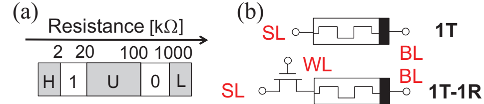

Fig. 3. RRAM technology. (a) RRAM resistance states, (b) 1R, 1T-1R cells.

II. Background

The RRAM device is a Metal-Insulator-Metal (MIM) construction, as schematically shown in Fig. 1a [1, 9]. In its stack organization, a middle metallic oxide (commonly TiO_x, HfO_x) is constructed with an additional capping (cap) layer (commonly Hf, Ti, Ta), between two metal electrodes: the Top Electrode (TE), and the Bottom Electrode (BE) [2, 19]. Typically, RRAM devices require a forming process, in which a high positive voltage (V_{forming}) is applied between the TE and BE to dissociate a portion of the metal-oxygen ionic bonds [1]. Negatively charged oxygen ions (O^{2-}) are pulled out of the lattice towards the positive anode and accumulate at the cap/oxide interface. As shown in Fig. 1b, a chain of positive charged oxygen vacancies (Vo) known as *Conductive Filament (CF)* is created in the insulator between two electrodes as a result of this localized deficiency.

The Bipolar Switching (BS) mechanism depends on the production and dissolution of the CF due to *oxygen ion* migration [1, 2]. The switching direction depends on both the amplitude and the polarity of the applied voltage (V_{SET} and V_{RESET}) [1]. By applying specific programming voltages to an RRAM device, its resistance can be switched between different states. The CF length will increase with a positive voltage from TE to BE (V_{TE}) larger than the specified threshold ($V_{\text{TE}} \geq V_{\text{SET}}$), due to the generation of more Vo, as shown in Fig. 1c [20, 21]. This process is called a SET operation. The value of the resistance in SET is R_{SET}. Oppositely, when there is a negative voltage from TE to BE lower than the reset threshold ($V_{\text{TE}} \leq V_{\text{RESET}}$), some O^{2-} drift from the interface back into the bulk oxide to rupture the CF, as shown in Fig. 1d [20, 21], which is called a RESET operation. The value of the resistance in RESET is R_{RESET}. Fig. 2a shows the simplified current-voltage (I_{TE}-V_{TE}) curve during the switching process. Fig. 2b shows the corresponding resistance-voltage (R-V) curve. Thus, SET and RESET switching occurs when the polarities are reversed. The length of CF in the insulator between two electrodes affects the resistance states. The (binary) RRAM is divided into up 5 states as the resistance increases (in Fig. 3a) [11, 22, 23]. For instance, a longer and a shorter CF corresponds to the Low-Resistive State (LRS) (logic '1') and High-Resistive State (HRS) (logic '0'), respectively. State 'U' in RRAM represents the undefined faulty state, which is commonly defined as the intermediate range between the LRS and HRS [22]. Besides, 'L' (the extremely low faulty conductance state) and 'H' (the extremely high conductance faulty state) stand for resistance values of the RRAM device higher than an HRS and lower than an LRS, respectively.

The most two popular RRAM cell designs are One-Resistor (1R) or One-Transistor-One-Resistor (1T-1R), shown in Fig. 3b. They can both be applied to build a memory crossbar array. In the figure, BL, WL, and SL refer to the bit line, word line, and select line. There is a WL to control the turn-on of the transistor to make the data stored in desired cells accessible. The BL and SL are set to appropriate voltages for write operations. A sense amplifier (SA) senses the current through the RRAM device as a consequence of providing a read voltage to the cell being read out.

III. Defect characterizations of ID

In this section, the characterization of both defect-free and defective RRAM devices is presented based on silicon measurements. A small fraction of devices has been observed failing to achieve the expected HRS during the RESET process while having the normal switching behavior during the SET process. In this paper, we identify the ID defect as the primary contributor to a decrease in HRS. Next, we will present the silicon measurements of a representative ID-defective device as well as a defect-free device for the purpose of comparison. Thereafter, a brief overview of the ID defect and its potential underlying physical explanation is given.

A. Characterization

On a single wafer, we measured the electrical characteristics of a 7×7 1T-1R array (49 BS RRAM devices) during 936 RESET-SET cycles [18]. The RRAM devices are manufactured at ST Microelectronics $130\,\text{nm}$ technology. The stack of the bipolar device is (BE/oxide/cap/TE) = (TiN/$10\,\text{nm}$ HfO_2/$10\,\text{nm}$ Ti/TiN). One ST Microelectronics in $130\,\text{nm}$ technology NMOS high-voltage thick oxide transistor (W = $0.8\,\mu\text{m}$ and L = $0.5\,\mu\text{m}$) is connected in series to regulate the current through the device. The measured 1T-1R device is embedded in an 8-inch wafer, and a probe card connects it to the Keysight B1500 semiconductor parameter analyzer. For the measurement setup, a $1\,\text{ms}$ DC staircase voltage sweep with a $20\,\text{mV}$ step is applied across two nodes of the measured device and the current flowing through the

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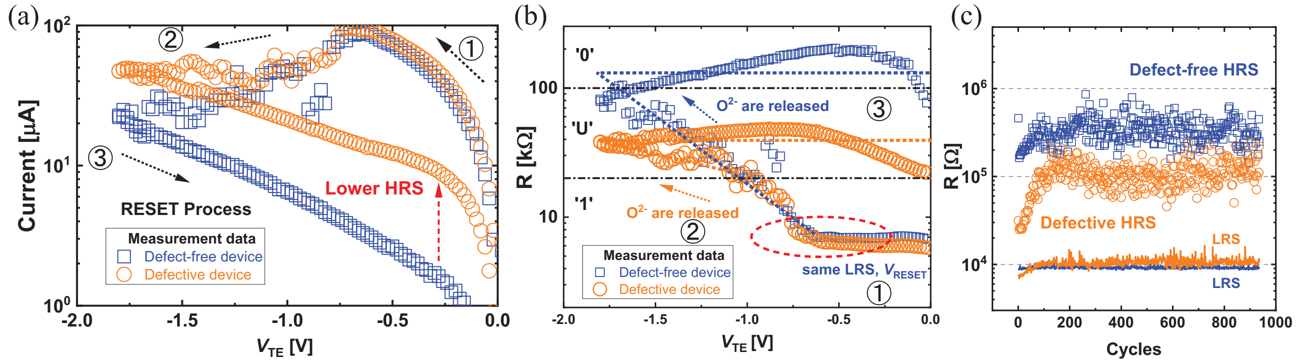

Fig. 4. Comparing defect-free and defective devices. (a) Measured I-V curve in the logarithmic y-axis, (b) Measured R-V curve in the logarithmic y-axis, (c) Measured R_{RESET} and R_{SET} in multiple (936) cycles.

device is measured. Four critical electrical parameters, which illustrate the device's switching performance, are considered: V_{SET}, V_{RESET}, R_{SET}, and R_{RESET}. The switching in a nominally defect-free device is bipolar. Logic '1' is represented by the LRS with $2\,\text{k}\Omega < R_{\text{SET}} < 20\,\text{k}\Omega$, and logic '0' by the HRS with $100\,\text{k}\Omega < R_{\text{RESET}} < 1\,\text{M}\Omega$. The remaining range $[20\,\text{k}\Omega, 100\,\text{k}\Omega]$ is referred to an undefined state ('U').

While analyzing the measurement data, we notice that some of the devices have faulty RESET processes, i.e., their resistance states are stuck at an intermediate resistance state ('U') no matter how large the RESET voltage amplitude is. Fig. 4a and Fig. 4b compare defect-free and defective devices by showing their typical measured 1T-1R $\log(\text{I})$-V and $\log(\text{R})$-V curves in RESET process to characterize the ID defect. The applied V_{TE} is swept from $0\,\text{V}$ to $-1.8\,\text{V}$ (①, ②), and back to $0\,\text{V}$ (③). For the defect-free device, the RESET transition starts from $-0.7\,\text{V}$ with a constant LRS and ends at a very low current (around $20\,\mu\text{A}$). In the case of a defective device RESET switching, an apparent transition is also observed from $-0.7\,\text{V}$. However, this transition fails at ② and gets stuck in the intermediate state. As the RESET voltage decreases even further, the current through the device slowly decreases but is still larger than the normal RESET current (around $50\,\mu\text{A}$). When the applied negative voltage increases back to $0\,\text{V}$, the HRS of the two devices are nearly constant (③). The subsequent SET process follows the normal behavior for both defect-free and defective devices. Fig. 4c presents the on/off resistance window as a function of cycles for defect-free and defective devices. 936 cycles per device have been collected. During the initial ≈ 50 cycles, devices exhibit erratic resistance states, which is also reported in [24]. After the initial few cycles, the variability of resistance values is low. In our case study, the HRS degradation occurs in multiple (around $45\,\%$) cycles. Hence, the faulty behavior is *intermittent*, and it is a serious concern for RRAM devices. It is also noted that measured ID-defective devices exhibit similar normal SET processes (e.g., R_{SET}).

B. Related Work and Potential Physical Explanation

In 2011, the word 'ion depletion' was put forward by Chen *et al.* to describe the RRAM endurance degradation phenomenon with HRS reduction [25]. The physical mechanism of this RESET failure was attributed to the irrecoverable switching behavior after 10^5 cycles. In 2012, Chen *et al.* investigated the influence of SET/RESET pulse on device reliability [26]. It was claimed that an excessive amount of Vo is induced at the interface by using too strong SET pulses, which causes HRS failure (after 10^6 cycles). Afterward, the two aforementioned works proved that the voltage amplitude rather than stress time has a significant effect on O^{2-} drift. In 2015, Schönhals *et al.* argued that the thin oxygen scavenging metal layer fails to form Ohmic contact, in which the capping layer cannot release a sufficient number of O^{2-} to recombine the Vo in RESET process [27]. In 2017, Wang *et al.* experimentally verified the HRS drop and related it to rougher and thicker CFs created after 10^4 switching cycles [28]. However, they all failed to notice the HRS reduction induced by device defects during the first hundreds of cycles, which led to their limited experimental results related only to endurance failures. Furthermore, they did not develop a circuit-level defect model to describe the HRS degradation behavior.

In Section II, the BS mechanism is explained as the movement of O^{2-} to form and rupture the CF composed of Vo, which is a *stochastic* process [20, 21]. In the SET, O^{2-} drifts to the capping layer (Ti) and is stored at the interface between the capping layer and the HfO_2, while Vo is generated [20, 21]. Under a reverse bias, the rupture of CFs near the interface is caused by O^{2-} migration from Ti back to the bulk oxide and recombining with Vo [20, 21]. The nearly constant LRS of defect-free and defective devices (see Fig. 4b, ①) indicates that the same amount of O^{2-} is generated during the SET process. During the RESET process, recombining Vo requires the O^{2-} stored in the capping layer [20]. The O^{2-} are depleted in the oxygen reservoir of defective devices. Only insufficient O^{2-} can be released back to recombine the Vo, which results in the insufficient RESET, and hence the reduced HRS as well as the smaller resistance window. In Fig. 4b, it is worth noting that at low voltages (less than $-1.5\,\text{V}$), defect-free devices exhibit a little drop in resistance, which can be explained by the effect of tunneling leakage currents [21], while defective devices still release a small fraction of insufficient O^{2-} at high voltages to recombine the CF.

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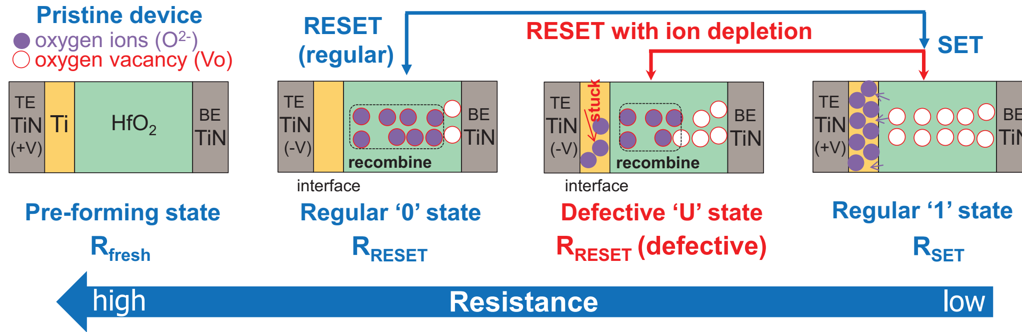

Fig. 5. The schematic view of ion depletion mechanism during RESET process.

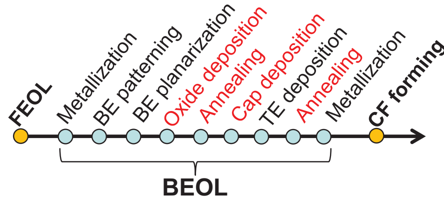

Fig. 6. Flow of RRAM manufacturing process [9, 30–32].

Based on the measurement data presented previously, the faulty RESET switching can be attributed to the ion depletion defect. A probable cause of the defect is related to interface physical imperfections, which involve an increased oxygen trap of the defective device, leading to a lower recombination rate between insufficient O^{2-} and Vo [25, 26, 28, 29]. Hence, the reduced recovery of Vo with insufficient non-lattice O^{2-} stored in the capping layer induces lower HRS. Fig. 5 schematically illustrates the HRS degradation mechanism and four possible resistance states of the device during forming, SET, and RESET processes: 1) before forming, pristine RRAM devices with minimal Vo have an extremely high initial resistance state (R_{fresh}) [9], 2) in SET or forming process, O^{2-} and Vo are generated (R_{SET}), 3) in RESET of defect-free devices, regular recombination between O^{2-} and Vo results in the nominal HRS (R_{RESET}), and 4) in RESET of defective devices, less recombination of Vo due to physical imperfections ($R_{\text{RESET}}(\text{defective})$). Therefore, these resistance values are: $R_{\text{fresh}} > R_{\text{RESET}} > R_{\text{RESET}}(\text{defective}) > R_{\text{SET}}$.

C. Related Fabrication Processes

The defects of RRAM are related to its manufacturing steps, and different stages of manufacturing introduce different defects corresponding to them. The general manufacturing process is shown in Fig. 6 [9, 30–32]. Transistors are first constructed on the wafer in the FEOL, which is identical to a standard CMOS technology. Then, the metal layers are deposited in the BEOL. Finally, the CF is formed by applying a high forming voltage.

In this paper, we consider that the following imperfect fabrication processes (red font in Fig. 6) are related to the characterized ID defect, which may affect the interface imperfections and thus the depletion of generated O^{2-}.

1) Thickness variations of deposition: The capping layer is deposited with different thicknesses. The thicker capping layer favors stable BS because of its decreasing work function and increasing oxygen affinity [27, 29]. Instead, a thin capping layer traps a large number of O^{2-}, difficult to fill the CF, which refers to an interface-formed blocking contact [27]. The proper barrier height formation at the cap/oxide interface is also related to the oxide layer [20]. The improved stability of RESET could be observed in thicker oxide [20, 33].

2) Annealing process: The proper annealing treatment can promote the improvement of crystalline quality of the oxide bulk and increase oxygen content in the capping layer [30, 34]. RRAM switching performance is shown to be related to variations in the hydroxyl group concentration [35]. It has been reported that significant dependence on annealing temperature is apparent at HRS [35]. The annealing temperature also plays a role in the roughness of the surface [35–37]. Hence, nonuniform or inappropriate annealing temperatures can affect the interface activity and thus lead to HRS degradation.

Due to the variation of the manufacturing process [38] and the random nature of CF dissolution, the ID defect does not occur on every device and only around $45\,\%$ of cycles.

IV. Device-Aware Defect Modeling of ID

The structural RRAM test development approach consists of three steps: defect modeling, fault modeling, and test development [8, 18, 39]. Traditionally, RRAM defects are modeled as linear resistors, connected in parallel or series with the device [12, 14, 15, 40]. Next, we will first demonstrate the failure of linear resistors to model the ID defect. Afterward, we apply the device-aware defect modeling for the characterized ID defect discussed in the previous section and develop an accurate defect model able to describe its behavior.

A. Conventional Resistor Defect Models

The linear resistors are used for RRAM defect modeling by connecting them in parallel or series with the device, see Fig. 7. In each of these linear models, varying resistance values are utilized to represent the size and strength of the physical defect. Higher series ohmic resistance or lower parallel ohmic resistance indicates a stronger defect strength as well as a more serious faulty behavior. Fig. 7a and Fig. 7b illustrate how the defective device behaves with varying defect strengths (i.e., the resistance of resistors), and the measurement of ID-defective device (red line). It is evident that with various resistive

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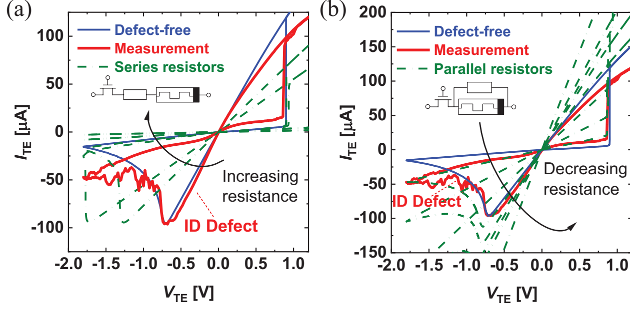

Fig. 7. Linear resistor defect models. (a) Series resistors, (b) Parallel resistors.

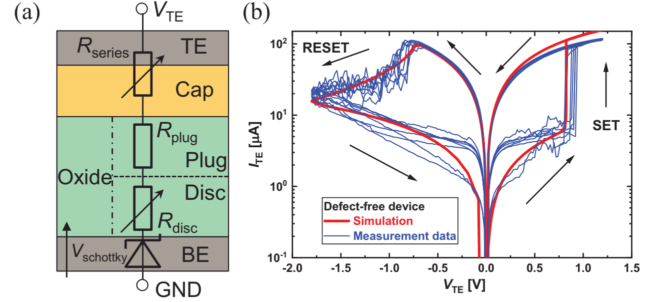

Fig. 8. The Verilog-A compact model diagram and defect-free device simulation model. (a) Equivalent circuit diagram of the JART VCM v1b model [41], (b) Defect-free device fitting in the logarithmic y-axis.

defect strengths, electrical parameters of the defective RRAM device including R_{SET}, R_{RESET}, V_{SET}, and V_{RESET} are all affected. Note that the parallel resistor may also cause the same R_{RESET} with the ID-defective device (see the green dotted line in Fig. 7b). However, it fails to be fitted with other electrical parameters (e.g., V_{RESET}, R_{SET}); hence cannot model the ID defect. When the resistor defect has a strong impact, the device even fails to switch between HRS and LRS. Clearly, none of these two defect models can describe the ID properly. To capture the state transition in the RRAM RESET properties, a more sophisticated defect modeling approach is required.

B. Device-Aware Defect Modeling

To accurately model the unique ion depletion, we will apply a systematic device-aware approach in the remainder of this paper [8]. The device-aware approach appropriately models the physical defect by incorporating the influence of the technological parameters (e.g., the CF length and oxide thickness) of the afflicted devices on the electrical behavior of defective devices [8]. The inputs of the DAT approach are a physics-based device model and silicon data of defective devices. The output is a modified (parameterized) model of a defective device. The systematic device-aware defect modeling approach includes the following three steps: 1) physical defect analysis and modeling, 2) electrical modeling of the defective device, and 3) fitting and model optimization. Next, we will apply the DAT approach to develop a physics-based model for the ID defect. For this purpose, our first step is to model how the presence of ID defects affects the concentration of O^{2-} in defective devices. Thereafter, its impact is mapped to the RRAM's electrical parameters, e.g., V_{RESET}, R_{RESET}. Finally, the ID-defective RRAM compact model is calibrated using the measurements.

1) Physical Defect Analysis and Modeling: The ID defect must be investigated to comprehend its mechanism and determine its impact on one or more technology parameters of the device. In Section III, we characterized and analyzed that the ID defect is caused by the insufficient O^{2-} that can recombine Vo in the bulk oxide. Therefore, one or more technology parameters, which affect the concentration of the inadequate O^{2-} for the Vo recombination during the RESET process, need to be modified from their defect-free values to include/describe the defect behavior. The resistance state of the RRAM device is directly related to the concentration of Vo in the oxide bulk. To accurately model this defect, we apply the physics-based HfO_2 RRAM model, JART VCM v1b, from [41]. The compact model is designed for BS in a Valence Change Mechanism (VCM)-based device as the change of Vo in the oxide. The equivalent circuit diagram of the compact RRAM model is illustrated in Fig. 8a, which consists of a series resistance (R_{series}), two filament resistances (R_{plug}, R_{disc}), and a Schottky-like contact (V_{schottky}) [41]. There are two split regions of the HfO_2 (oxide) layer in this model: the disc region and the plug region. For simulation purposes, the switching occurs in the disc region, whereas the plug region is conductive and serves as an infinite supply of vacancies. Both the SET and RESET processes during switching can be described as the ionic migration of Vo, which influences the Schottky barrier and, subsequently, the electrical conductivity of the VCM device [41]. N_{disc} is the parameter used in the model simulation to calculate the Vo concentration in the disc region. The value of N_{disc} changes to represent the switching behavior and affect the resistance state in the RRAM model. $N_{\mathrm{disc,min}}$ and $N_{\mathrm{disc,max}}$ are limiting parameters to keep N_{disc} between $N_{\mathrm{disc,min}}$ and $N_{\mathrm{disc,max}}$ in RESET and SET processes. Therefore, we are able to include the undesirable ID depletion by modifying: the minimum oxygen vacancy concentration in the disc (parameter $N_{\mathrm{disc,min}}$). Since only insufficient O^{2-} can recombine with the oxygen vacancies due to the ID defect, a higher concentration of oxygen vacancies will remain after RESET switching for the defective device. $N_{\mathrm{disc,min}}$ determines the remaining number of Vo in the disc when the maximum number of Vo is recombined. Lower negative RESET voltages can generate more O^{2-} to recover the HRS and favor the migration of O^{2-} back to the oxide. Hence, the effective values of $N_{\mathrm{disc,min}}$ for the parameter have to be directly determined under the impact of the RESET voltage. Besides, the ionic current into and from the disc region is based on a field-accelerated ionic hopping and Trap-Assisted-Tunneling (TAT) mechanism, which provides an exponential relationship [21, 41]. For numerical estimates, we use the same exponential relation function to define $N_{\mathrm{disc,min}}$ under the RESET process. The equation for the physical defect modeling stage is:

$$N_{\mathrm{disc,min}} = exp\left[-\left(-V_{\mathrm{TE}}/p_1\right)^{p_2}\right]\left(V_{\mathrm{TE}} < -1\,\mathrm{V}\right). \quad (1)$$

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TABLE I
MODEL PARAMETERS FOR JART VCM V1B [41].

Symbol	Value	Symbol	Value
T_0	$0.293\,\mathrm{K}$	ν_0	$2\cdot10^{13}\,\mathrm{Hz}$
ϵ_s	11	ΔW_A	$1.35\,\mathrm{eV}$
$\epsilon_{\phi_{Bn0}}$	2.5	R_{th0}	$15.72\cdot10^6\,\mathrm{K\cdot W^{-1}}$
ϕ_{Bn0}	$0.18\,\mathrm{eV}$	r_{det}	$45\,\mathrm{nm}$
ϕ_n	$0.1\,\mathrm{eV}$	l_{cell}	$3\,\mathrm{nm}$
μ_{n0}	$4\cdot10^{-6}\,\mathrm{m^2/(Vs)}$	l_{det}	$0.45\,\mathrm{nm}$
$N_{disc,max}$	$6.5\cdot10^{25}\,\mathrm{m^{-3}}$	$R_{theff,scaling}$	0.31
$N_{disc,min}$	$5\cdot10^{23}\,\mathrm{m^{-3}}$	$R_{series,ICL}$	$650\,\Omega$
N_{init}	$5\cdot10^{23}\,\mathrm{m^{-3}}$	R_0	$750\,\Omega$
N_{plug}	$6.5\cdot10^{25}\,\mathrm{m^{-3}}$	$R_{th,line}$	$90\,471.5\,\mathrm{W\cdot K^{-1}}$
a	$0.25\,\mathrm{nm}$	α_{line}	$3.92\cdot10^{-3}\,\mathrm{K^{-1}}$

Here, p_1 and p_2 are fitting parameters. Note that the equation is applied only when it is smaller than the original $N_{disc,min}$ for the defect-free device, and is $-1\,\mathrm{V}$ in our case.

2) Electrical Defect Modeling: Following the physical defect analysis, the affected physical parameters (e.g., the Vo concentration) are incorporated into the electrical parameters (e,g., V_{RESET}, R_{RESET}, I_{TE}) in this step. The compact model JART VCM v1b is written by Verilog-A and can be directly integrated into the circuit-level simulation. The model takes $N_{disc,min}$ as an input parameter and can therefore be directly integrated into a SPICE simulator to analyze the effect of inadequate O^{2-} recombination on the switching electrical behavior (e.g., current, resistance) in the presence of the modeled defect. In the defect-free model, the temporal evolution of N_{disc} is described as [41]

$$\frac{\mathrm{d}N_{disc}}{\mathrm{d}t} = \frac{I_{ion}}{zVo\cdot e\cdot A\cdot l_{det}}. \tag{2}$$

Here, zVo (Vo charge number, 2) and e (charge of an electron) are constants; A and l_{det} are the cross-section and length of the filament; I_{ion} denotes the ionic current in the device and is calculated as suggested by Genreith-Schriever [42]. Thus, the change in ionic current is proportional to the Vo concentration (N_{disc}) and is set to zero if either $N_{disc,max}$ or $N_{disc,min}$ is reached [41]. Hence, by connecting it to N_{disc} utilizing model simulations, the electrical behavior of the defective device switching comprising current changes can be examined.

3) Fitting and Model Optimization: The fitting is carried out using MATLAB R2021a to match the I-V measurements from Section III. The fitting process consists of the following two steps: 1) the fitting for defect-free device behavior, 2) the fitting for defective device behavior with defective parameter $N_{disc,min}$. We applied the JART VCM v1b model to calibrate the defect-free measurement data with fitted parameter values listed in Table I. In the simulation, a transistor with the same dimensions as those devices used during characterization is connected with the RRAM model in series. The voltage (V_{TE}) is ramped from $0\,\mathrm{V}$ to $-1.8\,\mathrm{V}$, and back to $0\,\mathrm{V}$ for RESET; from $0\,\mathrm{V}$, then to $1.2\,\mathrm{V}$, and back to $0\,\mathrm{V}$ for SET. Fig. 8b shows the fitting result of the BS device model simulation as well as the measurements of the defect-free device in different RESET-SET cycles. The model matches the measurements well, showing a BS behavior.

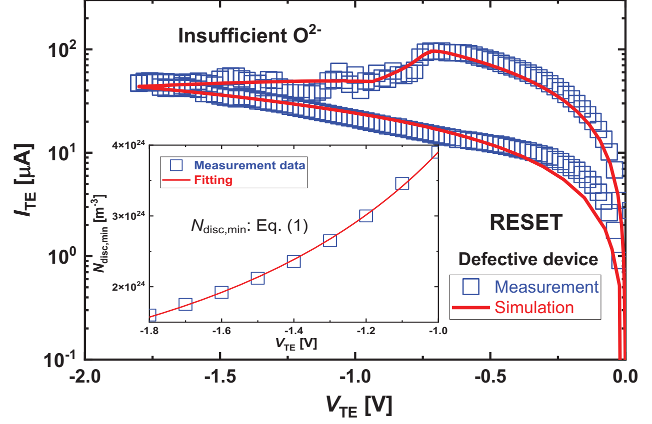

Fig. 9. The ion depletion defective device fitting in the logarithmic y-axis.

Next, we calibrate the defective device measurements. Fig. 9 shows the simulation result of the calibrated model and measurement data for an ID-defective device. We use the same parameters as in Table I but fit $N_{disc,min}$ to the measurements by changing the values of parameters p_1 and p_2 using least squares. The parameters p_1 and p_2 are calculated as 0.0611 and 0.4209 to fit Equation 1, respectively. The inset of Fig. 9 shows that lower negative RESET voltages lead to a smaller value of $N_{disc,min}$ (but still larger than $N_{disc,min}$ for defect-free device), which is consistent with the real RRAM mechanism observed in [25]. Fig. 10a presents the simulated I-V curve for both defect-free and defective devices. Fig. 10b presents the simulated R-V curve with the RESET/SET voltage sweep to compare the fitting results for both defect-free and defective devices. First, the two devices exhibit similar LRS, which increases at the same rate as RESET voltage decreases (①). Then, the abnormal RESET is observed with a slower rise in resistance for the defective device (②). The defective R_{RESET} is stuck at an intermediate state (③, ④) but decreases normally with the positive SET voltage (⑤), and switches to a normal LRS (⑥). Fig. 10b also shows that the HRS of the model simulation at the beginning of SET is larger than the HRS at RESET (④). This is explained that the Schottky contact at the BE/oxide interface is modeled as a diode in the RRAM model; hence it can be divided into the forward (negative RESET voltage applied) and reverse (positive SET voltage applied) directions [41]. The potential barrier height of the diode equals the difference between the work function of BE and the electron affinity of the oxide [41]. Different electronic conduction mechanisms are applied, leading to a small Schottky current and a higher device resistance during the SET process, especially in the HRS. The model matches the measurements well, except for the V_{SET} reduction of the defective device (⑤). That is because the model contains the initial resistance state-dependent thermoelectric coupling during the SET process, which causes a shorter delay time in transition for lower initial HRS [41]. Besides, the final LRS is independent of the initial state but only depends on the applied voltage amplitude, which is supported by both the model simulation and measurements [41]. Hence, both defect-

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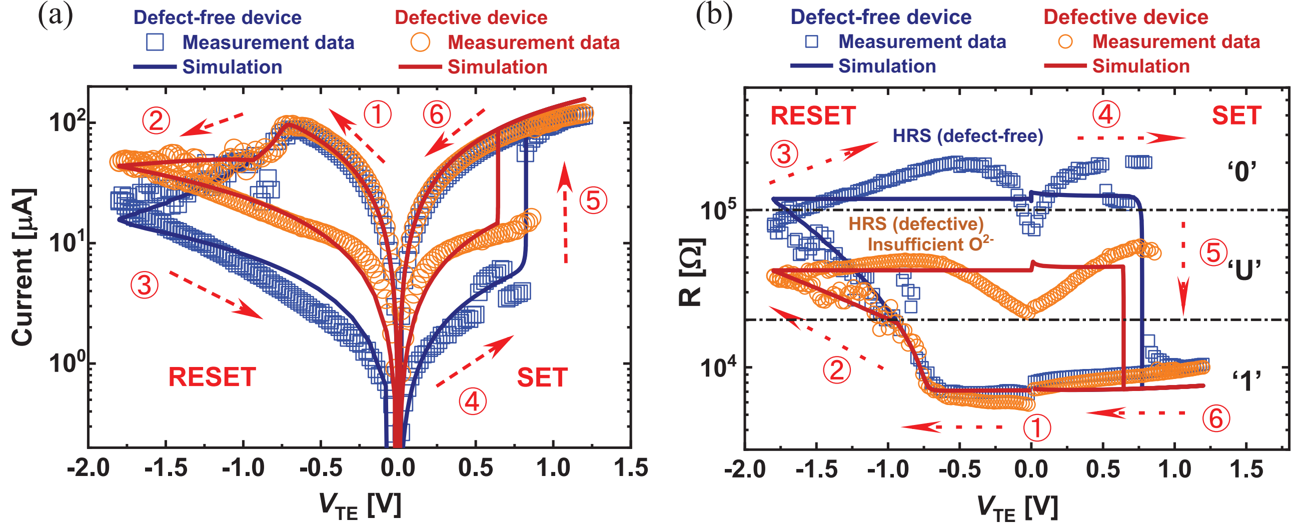

Fig. 10. Defect-free and defective device simulation and measurements. (a) Simulation vs. measurements of the I-V curve, (b) Simulation vs. measurements of the R-V curve.

free and ID-defective devices start from the normal LRS in the next RESET cycle. The fitting results indicate that the model is able to accurately describe the ID-defective RRAM device in a circuit simulator. Finally, the output of device-aware defect modeling is a calibrated Verilog-A ID-defective RRAM compact model.

V. Device-Aware Fault Modeling of ID

The second step of the DAT approach is device-aware fault modeling, which includes two aspects: 1) fault space definition, and 2) fault analysis. First, we define and classify the fault space. Then, the fault analysis based on the circuit simulation using the electrical models will be given.

A. Fault Space Definition and Classification

A fault space is the defined set of all possible modeled faults that can occur in the circuit [40]. There is a systematical method, the Fault Primitive (FP) notation, to describe all faults leading to incorrect logical behaviors: $\langle$S/F/R$\rangle$ [40], as illustrated in Table II. Here, S denotes the sensitizing sequences of the cell. F describes the stored value in the cell after sensitizing S is applied. Finally, R indicates the output of the read circuit, where $\mathrm{R} \in \{0, 1, ?, -\}$. ? is a random read outcome (e.g., the sense amplifier voltage is an intermediate value due to the sensing and reference current being too close); and $-$ denotes the case where the last performed operation in the cell is not r. For example, $\langle$0r0/U/1$\rangle$ describes a 0r0 operation is applied on an HRS cell (S = 0r0), where the cell flips to an incorrect undefined state (F = U), the read output returns '1' (R = 1) instead of the expected '0'.

Static and *dynamic* faults are two categories of faults. Dynamic faults need multiple operations to be sensitized, but static faults can be sensitized by as few as one operation. Faults can also be classified into *strong* and *weak* faults. Only strong faults can be presented by an FP; weak faults are parametric faults and do not result in any functional errors, e.g., a voltage drop in the BL during a writing operation. *Easy-to-Detect (EtD)* faults are a subset of those strong faults that can be *guaranteed* to be sensitized and detected by regular memory operations. *Strong/weak Hard-to-Detect (sHtD/wHtD)* faults are strong faults that have no deterministic behavior (e.g., random read) and weak faults.

TABLE II
Fault Primitive Notation [40].

	Explanation	Values
S	Sensitizing sequence	0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1
F	Faulty behavior	L, 0, U, 1, H
R	Readout value	0, 1, ?, -

B. Fault Analysis

1) Simulation Setup: This step is based on the simulation of the obtained electrical model in Section IV. In order to analyze the ion depletion effect, Cadence Spectre is adopted to establish the simulation by using the Predictive Technology Model (PTM) 130-nm transistor library [43] and the RRAM compact model from [41]. It comprises a 1T-1R cell (with the same dimensions as the devices used for characterization) and the necessary circuitry to drive the three control lines (BL, SL, and WL) at the proper voltages. Regular voltage-based SA is applied for reading purposes [44]. We perform two experiments for the fault analysis. The first experiment is built to validate faults with varying ID defect strengths. The ID defect injection is carried out by replacing the defect-free RRAM model with the model of the ID-defective RRAM device obtained in Section IV. The defect strength of $N_{\mathrm{disc,min}}$ is varied from $0.005 \cdot 10^{26}\,\mathrm{m}^{-3}$ to $0.065 \cdot 10^{26}\,\mathrm{m}^{-3}$ to ensure the correct operation of the model, as well as fitting within realistic physical limits [41]. Following the characterization of measurements, the voltage sweep is applied via the SL from 0 V to 1.8 V back to 0 V for RESET operation to sensitize the fault. The simulation results are inspected for the final resulting resistance of the defective devices (i.e., R_{RESET} after RESET

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TABLE III
FAULT ANALYSIS RESULTS FOR ION DEPLETION DEFECT.

$N_{\mathrm{disc,min}}$ $[10^{26}\,\mathrm{m}^{-3}]$	R_{RESET} $[\mathrm{k}\Omega]$	Fault	Type
0.065	15.21	$\langle 1\mathrm{w}0/1/-\rangle$	EtD
0.05	17.76	$\langle 1\mathrm{w}0/1/-\rangle$	
0.0415	20.03	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	sHtD
0.035	22.51	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	
0.016	41.34	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	
0.0113	55.55	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	
0.0077	78.57	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	
0.006	99.64	$\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$	
0.005	118.42	Fault free	

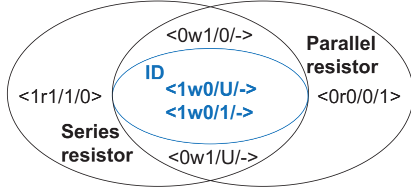

Fig. 11. Static faults.

operation), which are used to derive the faulty behavior in the presence of the modeled defect. For example, if the final R_{RESET} is out of the HRS boundary (i.e., $[100\,\mathrm{k}\Omega, 1\,\mathrm{M}\Omega]$), then $\mathrm{F}=\mathrm{U}$. The second experiment is built to validate the fault space in presence of a linear resistor that is either in parallel (R_{p}) or in series (R_{s}) with a defect-free device. The strength of a resistor defect is swept from $1\,\Omega$ to $100\,\mathrm{M}\Omega$.

2) Fault Modeling and Results: Table III presents the simulation result of varying defect strengths. In the table, both sHtD ($\langle 1\mathrm{w}0/\mathrm{U}/-\rangle$) and EtD ($\langle 1\mathrm{w}0/1/-\rangle$) faults are observed depending on the defect strengths. It can be shown that when the value of $N_{\mathrm{disc,min}}$ increases, more faults are sensitized. sHtD faults are sensitized for $N_{\mathrm{disc,min}}$ between $0.006\cdot 10^{26}\,\mathrm{m}^{-3}$ and $0.0415\cdot 10^{26}\,\mathrm{m}^{-3}$, while EtD faults are observed for $N_{\mathrm{disc,min}}$ above $0.042\cdot 10^{26}\,\mathrm{m}^{-3}$. Here, $N_{\mathrm{disc,min}}=0.016\cdot 10^{26}\,\mathrm{m}^{-3}$ (bold in the table) is calibrated with the defective measurement data shown in Section III. A higher $N_{\mathrm{disc,min}}$ gives more room for vacancies to be recombined in the disc region, which makes it easier for the device to exhibit undesired RESET failure. As the applied negative RESET voltage decreases, more O^{2-} are appealed towards oxide bulk to recombine with Vo, leading to a decrease of Vo concentration. Nevertheless, ID-defective devices fail to release enough O^{2-} back into the oxide bulk, increasing the final Vo concentration while simultaneously decreasing the R_{RESET}; hence, faults can be sensitized at such voltages. The larger $N_{\mathrm{disc,min}}$ represents more O^{2-} depletion (inadequacy) and a higher defect strength.

Next, we compare the static faults that are sensitized with the conventional approach (linear resistor model) as well as the DAT approach for all R_{p}, R_{s}, and $N_{\mathrm{disc,min}}$, as listed in Fig. 11. The figure clearly presents the difference between the two approaches. The conventional defect model approach triggers 4 faults which are not realistic when modeling ID defects; hence, tests for them will lead to unnecessary yield loss. Furthermore, the comparison result also helps us distinguish and diagnose ID defects from linear resistor defects.

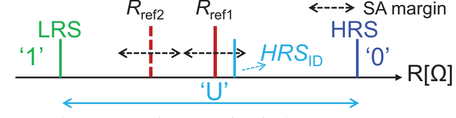

Fig. 12. Resistances for faulty RRAM state.

VI. DEVICE-AWARE TEST DEVELOPMENT

The final step of the DAT approach is to develop efficient test solutions for the validated RESET faults in Section V. First, test generation for ID will be discussed. Then, we will present an overview on the comparison of different RRAM defects, e.g., over- and under-forming, for diagnosis.

A. Test generation

As presented in Table III, the ID defect may cause EtD and sHtd faults with the RESET operation. One straightforward test solution is the following March algorithm:

$$\text{March-ID} = \{\Updownarrow(\mathrm{w}1)\,;\Updownarrow(\mathrm{w}0,\mathrm{r}0)\}\,.$$

Here, '$\Updownarrow$' indicates an irrelevant addressing direction. The first march element initializes all memory cells to state '1', w0 denotes a RESET operation, and r0 a read 0 operation to detect faults. This test algorithm can guarantee the detection of EtD faults, i.e., $N_{\mathrm{disc,min}} > 0.0415\cdot 10^{26}\,\mathrm{m}^{-3}$ in our simulation. However, due to the *intermittent* nature of the ID, the proposed test algorithm will only *probabilistically* detect the fault. Hence, repeated 1w0 (to sensitize) and read (to detect) operations are required to enhance the detection probability. If we assume the occurrence possibility of ID is P_{ID}, then the detection probability is: P_{d}=$1-(1-P_{\mathrm{ID}})^{k}$, k indicates the number of times the sequence is applied. In our case of P_{ID}=$45\,\%$, k=8 is required to realize over $99\,\%$ fault coverage.

Besides, this March algorithm does not satisfy the fault coverage requirement for sHtD faults that are in the 'U' state and may cause a random read output. Hence, DfT schemes targeting those sHtD faults should be applied. It is possible to add different reference resistors (or RRAM devices) so that the SA can distinguish resistance states between 'U'/'1' or 'U'/'0' instead of distinguishing only the regular '0'/'1'. Fig. 12 illustrates the DfT concept with multiple references to detect the intermediate HRS of ID-defective devices. R_{ref1} is set to $(\mathrm{HRS}+\mathrm{LRS})\,/2$ for the defect-free device. R_{RESET} of the ID-defective device is referred to as HRS_{ID}, which is close to the R_{ref1} (within the SA margin) and cannot be distinguished as logic '0'. To detect the faulty state, the reference can be set to R_{ref2} of $(HRS_{\mathrm{ID}}+\mathrm{LRS})\,/2$ for the ID-defective device. For example, Singh *et al.* presents a DfT scheme that deploys multiple references in the SA for a single read to perform a logic NOR operation and find the resistance of RRAM devices [45]. However, this DfT scheme has a large area overhead and not includes process variation impacts.

Therefore, we develop an adaptable DfT scheme with a reference tunable structure that is compatible with normal read operations. In Fig. 13a, we illustrate a regular voltage-based SA [44]. During a read operation, the SA compares the

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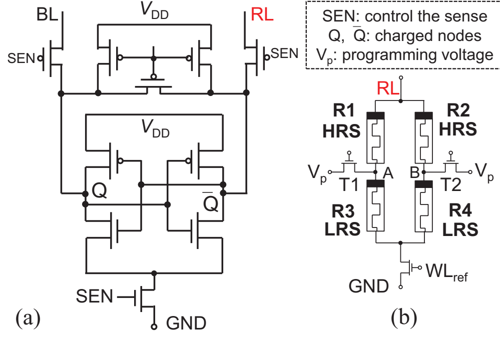

Fig. 13. SA for DfT scheme. (a) SA circuit schematic [44], (b) Modified reference cells.

resistance of a cell to that of a reference cell by discharging the BL and Reference Line (RL) connected to either the cell or the reference cell. The reference cell is typically set in the middle of HRS and LRS. We propose the tunable reference cells composed of two RRAM devices in series in parallel with two other RRAM devices in series, with additional two transistors (T1, T2), as shown in Fig. 13b. For example, one RRAM device is set to LRS and the other to HRS in a single connection. The parallel two links set the equivalent cell resistance exactly between these two values. T1 and T2 are used as switches to control whether voltage pulses (i.e., V_{P}) can be applied at nodes A and B to program the reference cells. For example, when the T1 turns on, a high voltage of V_{p} can be applied on node A, tuning the resistance of R1.

To implement the DfT scheme, a Cadence Spectre-based simulation including a 1T-1R cell and SA in Fig. 13 is built. First, the defect-free circuit is validated to be defect free. During a 1w0 operation, a 1.8 V RESET voltage is applied to the SL, and the BL is grounded; the resistance state changes from LRS to HRS. The fault-free HRS can be then read correctly by the used SA. Next, we replace the defect-free cell with the ID-defective device model. After applying the same 1w0r0 operation, the faulty HRS is read as an incorrect/random value because the differential BL/RL voltage ($\Delta \mathrm{V} = V_{\mathrm{BL}} - V_{\mathrm{RL}}$) is smaller than the SA margin ($\Delta \mathrm{V}_{min}$). By tuning the original HRS in the reference cell to the HRS_{ID}, the faulty HRS_{ID} can be correctly distinguished from the LRS by the readout value.

To further reduce the test time, specific DfTs are required. Such approaches could aim at decreasing the occurrence of the ID defect by e.g., increasing the current through the device during SET or over-forming the device. This will result in a higher concentration of Vo generated which decreases the final RESET resistance of ID-defective device [2, 18]. To achieve this approach, we can boost the BL or WL in test mode. The limitation of this scheme is a resulting lower R_{SET}, which increases energy consumption and the write latency.

B. Comparison of RRAM Defects for Diagnosis

Multiple defects in RRAM devices are reported that can sensitize similar undefined state faults. However, identifying the defect nature from similar faulty behaviors facilitates the development of efficient test solutions. Next, we present an overview (see Table IV) to diagnose the ID defect and other unique defects (i.e., Over/under-forming, IUSF) based on the physical mechanism of defects [8, 18, 23]. Over and under-forming defects occur due to the fact that the external tester channels performing the forming process are not absolutely stable and the forming process suffers a device-to-device variation [23]. In this case, the forming current is more or less than the nominal forming current. Both over-forming and ID defects may cause an undefined state fault. However, both R_{RESET} and R_{SET} of an under-forming defective device are stuck at the undefined state, while R_{SET} of an ID-defective device is still in '1' state. The R_{SET} of a defective cell due to over-forming may stay in an 'H' state. Thus, it is sufficient to compare R_{SET} in diagnosing the two defects. The IUSF causes the RRAM device to intermittently switch from BS to CS, resulting in undefined state faults [18]. Besides, the IUSF only occurs during the SET process and has a certain probability of fault. Hence, the 0w1 (SET) operation can diagnose the two defects. We can conclude that although other RRAM defects may also cause undefined state faults, they can still be diagnosed by other behaviors to identify ID defects.

TABLE IV
FAULT ANALYSIS RESULTS FOR ION DEPLETION DEFECT.

Defect/Fault	Faulty Behaviors	Fault Models (sHtD)
Over forming	Low $R_{\mathrm{SET}}/R_{\mathrm{RESET}}$, high V_{RESET}	⟨1w0/U/−⟩ ⟨0w1/H/−⟩
Under forming	High $R_{\mathrm{SET}}/R_{\mathrm{RESET}}$, low V_{RESET}	⟨1w1/U/−⟩ ⟨1w0/L/−⟩
IUSF	Intermittent, high R_{SET}	⟨0w1/U/−⟩
ID	Low R_{RESET}, normal $R_{\mathrm{SET}}/V_{\mathrm{RESET}}$	⟨1w0/U/−⟩

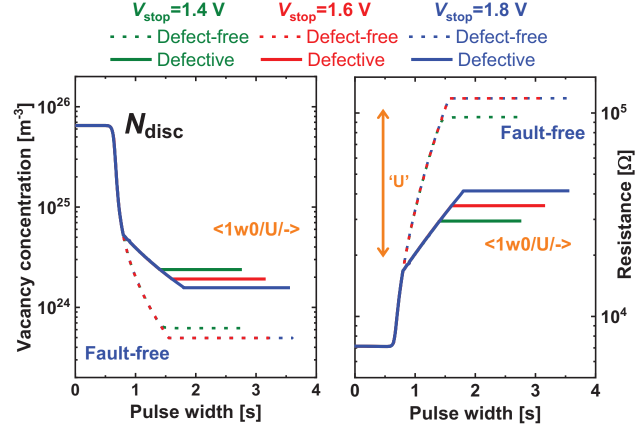

Fig. 14. Influence of V_{stop} on the HRS during the RESET process.

VII. Discussion and Conclusion

This paper demonstrates the existence of a unique RRAM defect: an ID defect, which can not be modeled using conventional linear resistors. Given the nature of ID defect, it is worth noting the following.

- **Reliability problem:** The RESET failure (i.e., HRS decrease with constant LRS) is also reported and investigated in terms of endurance problem [25–27]. The similar RESET failure makes it possible to use the proposed defect model and predict the endurance degradation in the circuit-level simulation.

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- **Vulnerability to low voltage:** In device down-scaling, low voltages are adopted for energy-saving purposes; hence, the ID defect may cause severe problems. An experiment is built for stop voltage study, employing triangular voltage pulses, but the maximum sweep voltages are $1.4\,\mathrm{V}$, $1.6\,\mathrm{V}$, and $1.8\,\mathrm{V}$, respectively. Fig. 14 shows with different V_{stop}, ID-defective devices are more prone to faults. It is also worth noting that increasing V_{stop} results in varying HRS for ID-defective devices, but constant HRS for defect-free devices (e.g., V_{stop} of $1.6\,\mathrm{V}$ and V_{stop} of $1.8\,\mathrm{V}$). That can be explained by an evolution of drift-diffusion equilibrium, which leads to constant values for disc concentration and an HRS saturation [41]. However, O^{2-} can still migrate back to decrease the N_{disc} under large RESET voltage amplitudes of $1.6\,\mathrm{V}$ and $1.8\,\mathrm{V}$ for the ID-defective device. Therefore, ID-defective devices are able to sensitize faults at a large negative RESET voltage.

Consequently, this work presents the power of the DAT approach in identifying and modeling RRAM-related unique defects in an appropriate manner. As devices scale down, complex and additional manufacturing steps in RRAMs could cause new defect mechanisms that are not investigated completely yet. Therefore, this requires a deeper understanding of emerging defect mechanisms, as well as improved fault modeling and testing methods, such as the DAT approach.

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