# Versatile DAC-less successive approximation ADC architecture for medium speed data acquisition

Pourahmad, Ali ; Dehghani, Rasoul ; Ahmadi-Mehr, Seyed Amir-Reza ; Lotfi, Reza

**DOI**
10.1016/j.mejo.2022.105585

**Publication date**
2022

**Document Version**
Final published version

**Published in**
Microelectronics Journal

Microelectronics Journal 129 (2022) 105585

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# Versatile DAC-less successive approximation ADC architecture for medium speed data acquisition

Ali Pourahmad [a], Rasoul Dehghani [a,*], Seyed Amir-Reza Ahmadi-Mehr [a], Reza Lotfi [b,c]

[a] Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 84156-83111, Iran
[b] Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
[c] Microelectronics Department, Bioelectronics Section, Delft University of Technology, Delft, the Netherlands

ARTICLE INFO

*Keywords:*
Analog-to-digital converter (ADC)
Successive approximation register (SAR)
Digital-to-analog converter (DAC)
Binary search algorithm
Asynchronous control logic
DAC-less SAR (DLSAR)

ABSTRACT

Implementation of the DAC is usually the bottleneck in designing a SAR ADC. Here an innovative DAC-less SAR (DLSAR) ADC architecture is presented which alleviates some drawbacks of the conventional SAR counterpart. The proposed DLSAR binary search algorithm is comprised of two arithmetic operations of division-by-two and subtraction to emulate the DAC function. The hardware of the DLSAR ADC is implemented using ordinary circuit building blocks of a SAR ADC but with less complexity and more robustness against PVT variations as DAC is removed. The developed DLSAR architecture is versatile so that the converter hardware could be readily reconfigured for different sampling rates and resolutions. Based on post-layout simulations in 0.18 μm CMOS process, the designed 8-bit DLSAR ADC consumes 150 μW of power at 2 MS/s including the asynchronous control logic circuit. The SFDR of the converter is up to 62 dB and the ENOB reaches 7.8 bits while it remains above 7.5 bits across most PVT corners without calibration. Also, by reconfiguring the DLSAR ADC to 9-bit resolution at 1 MS/s, the ENOB is generally around 8.2 bits achieving a scaled figure-of-merit (SFoM) better than 3.0 Ç/c-s.

## 1. Introduction

One of the main circuit blocks in almost every electronic device is the analog-to-digital converter (ADC) which is responsible for generating digitized codes to represent an analog signal. Based on the application requirements, several types of ADCs have been developed pushing to improve the converter performance in aspects of linearity, speed, area and power. Successive approximation register (SAR) is proven to be a common and efficient ADC topology for low to medium range sampling rates and resolutions. Modern SAR ADC designs are frequently being used in various applications such as radio receivers [1], internet of things (IoT) sensor nodes [2], low-power biomedical instrumentations [3] and fully synthesizable system-on-chips (SoC) [4].

The conventional SAR ADC is comprised of four main building blocks, i.e. sample and hold circuit (S/H), comparator, digital-to-analog converter (DAC) and control logic circuit as shown in Fig. 1. In this structure, on every clock transition one bit of the digital output code (DOC) is generated. Hence, for an $N$-bit ADC, a conversion cycle at least takes $N + 1$ clocks to finish, including the initial sampling phase. It is evident that the bottleneck in a SAR ADC is designing its DAC circuit which mainly determines the converter performance [5,6]. In integrated circuits, capacitive DAC topologies are employed that embody the S/H circuit as well.

Capacitive DACs are commonly implemented using charge redistribution (CR) or charge sharing (CS) structures where each one has its own pros and cons [6]. Nonetheless, the CR-DACs are usually preferred for their superior linearity, insensitivity to parasitics and simpler switching scheme. Regarding the large number of capacitors and switches, capacitive DACs suffer from various circuit parasitics and non-idealities that eventually leads to performance degradation of the SAR ADCs. Therefore, designing a flawless DAC requires rather extensive care in drawing the layout and complex circuitry to implement a proper switching scheme [7–9].

In a conventional SAR ADC, linearity characteristic deteriorates as input/reference voltage reaches the supply rail due to imperfect switching of the DAC circuit. This will confine full-scale and dynamic range of the converter [10,11]. On the other hand, mismatches of capacitor bank and process, voltage and temperature (PVT) sensitivity of DAC should be compensated by hard or soft calibration [12–14]. Utilizing calibration circuits increase area and power consumption of the converter. The on-chip reference voltage generator/buffer circuit

* Corresponding author.
*E-mail addresses:* a.pourahmad@ec.iut.ac.ir (A. Pourahmad), dehghani@iut.ac.ir (R. Dehghani), a.ahmadimehr@iut.ac.ir (S.A.-R. Ahmadi-Mehr), rlotfi@ieee.org (R. Lotfi).

https://doi.org/10.1016/j.mejo.2022.105585
Received 25 August 2022; Received in revised form 11 September 2022; Accepted 12 September 2022
Available online 29 September 2022

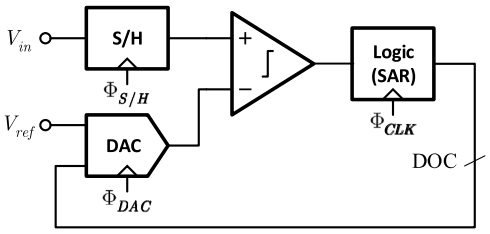



**Fig. 1.** Basic circuit building blocks of a conventional SAR ADC.

is also another problematic design aspect, especially in CR-DACs that usually leads to increasing the power dissipation and chip area [15–17].

This work introduces an innovative DAC-less SAR (DLSAR) ADC architecture in 0.18 μm CMOS process which brings some advantages in terms of linearity, robustness within PVT corners and hardware reconfigurability. By eliminating DAC completely, the proposed DLSAR ADC has achieved excellent performance with process/parasitics insensitivity without any calibration. Furthermore, the implemented circuit can be easily reconfigured for different sets of sampling rate and resolution just by modifying the controller. The cyclic ADC [11,18,19] and more especially the two-capacitor (2C-DAC) SAR [20,21] can be regarded as the analogous topologies to the DLSAR architecture. However, all these topologies employ analog circuitry while the proposed DLSAR ADC is implemented by default building blocks of the conventional SAR architecture, that will be discussed shortly.

The remainder of the paper is organized as follows. Architecture and operation of the proposed DLSAR ADC is illustrated in Section 2. Circuit implementation at transistor level is studied in Section 3 in depth. Next, Section 4 elaborates error propagation model of the designed hardware. Asynchronous control scheme of the DLSAR ADC is described in Section 5. Comprehensive simulation results of the designed converter are provided in Section 6, and eventually Section 7 summarizes and concludes the paper.

## 2. DLSAR ADC architecture

In order to remove the DAC from a SAR ADC, the converter binary search method must be altered. Here a new DAC-less binary search algorithm is illustrated that still works in accordance to the successive approximation principle. Afterwards, two possible circuit realizations are studied that can be used to implement the proposed DLSAR ADC.

### 2.1. Binary search algorithm

The binary search flowcharts of the proposed DAC-less SAR ADC architectures is demonstrated in Fig. 2. Here $V_{in}$ is the analog input signal, $V_{ref}$ is the reference voltage and the $N$-bit DOC is denoted by $D_{out} = (b_{N-1} \cdots b_1 b_0)_2$. Each conversion cycle consists of N-steps of successive approximation. Binary search algorithm in the proposed DLSAR architecture replaces DAC function by combining two arithmetic operations of *division-by-two* and *subtraction*. In addition to the input voltage, the reference voltage is also to be sampled in the DLSAR binary search which will be halved consecutively within each step of a conversion cycle. The conventional SAR binary search keeps the input voltage intact and scales the reference voltage via DAC for comparison phase. Yet, in the proposed DLSAR binary search algorithm the input voltage is scaled using subtractor if it is greater than the corresponding $1/2^k$ ratio of the reference voltage. Hence, the comparison phase can be carried out to ascertain the next bit.

As mentioned before, the DLSAR binary search is partially similar to that of the pipelined or cyclic ADCs. However, the subtraction result (residue) is not here amplified (doubled) which requires high-speed op-amp for implementation. As it will be clarified later, the voltage halving block is here realized by switched-capacitor (SC) circuit with good

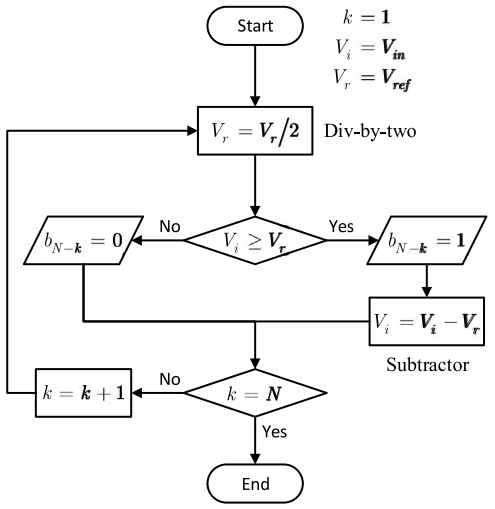



**Fig. 2.** Binary search algorithm in the proposed DLSAR ADC architecture.

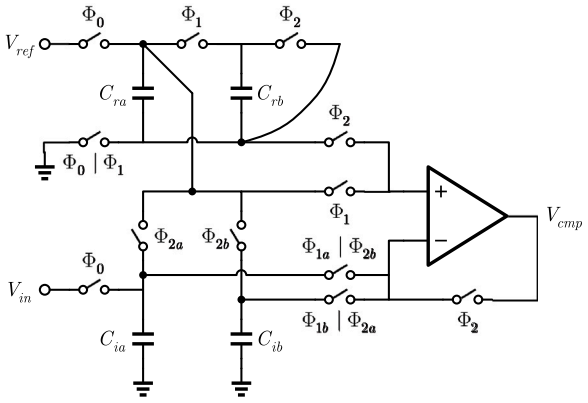



**Fig. 3.** Conceptual circuit implementation for the proposed DLSAR ADC based on operational amplifier (op-amp).

enough precision. Moreover, the developed DLSAR circuit performs the subtraction by just one comparator in discrete-time without any analog circuitry. This would alleviate the error due to the amplifier offset and noise comparing to these topologies as long as the comparator inaccuracy can be tolerated. Besides, in pipelined SAR or cyclic ADCs, op-amps dissipate a considerable amount of power to meet the circuit requirements that is eliminated in the DLSAR architecture.

The 2C-DAC architecture with inherent first-order noise shaping (NS) characteristic uses the exact DLSAR binary search algorithm yet the division-by-two and subtraction operations are there realized by an op-amp-based SC amplifier. As a result, the converter bandwidth would be typically limited to a few kilohertz. In addition to consuming more power, the SAR ADC utilizing 2C-DAC is proven to be more vulnerable to process/parasitics than the designed DLSAR hardware, and thus it needs to be calibrated [21].

### 2.2. Abstract hardware design

By inspecting the DLSAR binary search of Fig. 2 we see that each approximation step has two separate arithmetic phases, i.e. division-by-two and subtraction. Consequently, time budget in the proposed DLSAR architecture is twice that of the conventional SAR ADC.

#### 2.2.1. Op-amp-based hardware

Fig. 3 shows a straightforward hardware design for the DLSAR binary search algorithm. This conceptual circuit employs two identical

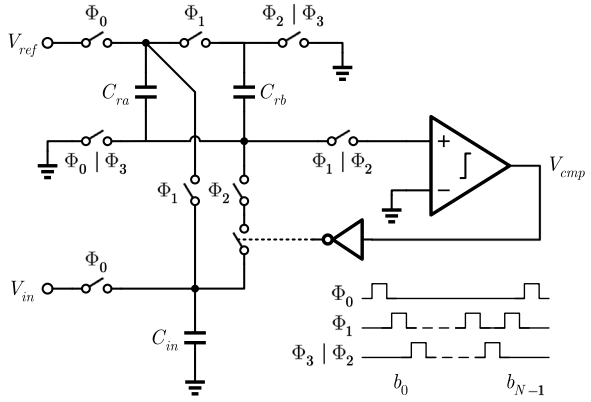



**Fig. 4.** Abstract circuit model of the proposed DLSAR ADC utilizing default building blocks of the conventional SAR architecture.

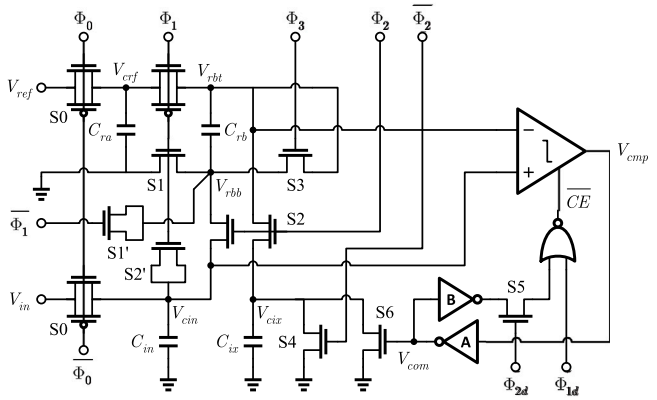



**Fig. 5.** Simplified transistor-level circuit implementation of the comparator-based DLSAR ADC architecture.

pairs of input/reference capacitors for voltage sampling and performing the division-by-two and subtraction operations. The arithmetic operations are realized via SC circuits while the op-amp is used as a buffer to store the subtraction result on the input capacitors, and also it functions as a comparator in open-loop configuration. Here, the subtraction operation is fulfilled by placing the input and reference capacitors in series with reversed polarity, and division-by-two is accomplished by paralleling the reference capacitors pair in each approximation step. Power dissipation of the voltage halving circuit and reference voltage ratio generator equals $C_{ra}V_{ref}^2 f_s$ with $f_s$ being the converter sampling frequency.

Operation of the circuit can be illustrated as follows. First at phase zero $\Phi_0$, the input and reference voltages are sampled on capacitors $C_{ia}$ and $C_{ra}$, respectively. Then at phase one $\Phi_1$, secondary reference capacitor $C_{rb}$ with zero initial charge is placed in parallel with $C_{ra}$. As a result, the voltage of the reference capacitor is halved and by activating $\Phi_{1a}$, the first comparison of the conversion cycle is executed to compute the MSB. At phase two $\Phi_2$, capacitor $C_{rb}$ is discharged and if MSB is 1, by activating $\Phi_{2a}$ the subtraction result of $V_i - V_r = V_{in} - V_{ref}/2$ is stored on secondary input capacitor $C_{ib}$. For the subsequent approximation steps, the procedure is repeated and the subtraction result would be swapped among the input capacitors pair by enabling $\Phi_{2a}$ or $\Phi_{2b}$, while it is read in comparison phase by enabling $\Phi_{1a}$ or $\Phi_{1b}$, correspondingly.

#### 2.2.2. Comparator-based hardware

The DLSAR hardware designed in Fig. 2 can accurately perform the subtraction operation, however the op-amp requirements may rise some difficulties in practical implementation. For higher sampling rates, the op-amp must satisfy a relatively small settling time and high slew rate that will lead to a power hungry or perhaps infeasible design. Thus, another hardware will be introduced in the following which can perform all the arithmetic operations using SC circuits and one comparator.

As depicted in Fig. 4, operation of the new circuit is analogous to the op-amp-based implementation for phases zero and one. During phase two by closing the associated switches, the input capacitor begins to discharge into $C_{rb}$ until the voltage across $C_{rb}$ becomes zero. Then, the comparator output changes its state, and by opening the switch controlled via the NOT gate, the two capacitors disconnect from each other. Since an equivalent discharge current passes through the identical capacitors of $C_{in}$ and $C_{rb}$, regardless of its waveform, the secondary reference capacitor voltage is exactly subtracted from that of the input capacitor. Based on the comparison result at phase one, if the subtraction operation is not to be executed in the next step ($V_i < V_r$), phase $\Phi_3$ is activated instead of $\Phi_2$ for discharging $C_{rb}$ to zero.

There are some practical issues regarding the comparator-based DLSAR hardware that need to be taken into account. Dynamic comparators usually employ positive feedback in form of a latch circuit to enhance their response time during the evaluation phase [22]. As a result, the comparator output will be locked after initial power-on based on the current state of its input signal and it no longer responses to the ongoing input signal changes. Therefore, the circuit is incapable to detect the right moment for halting the subtraction phase as the voltage of $C_{rb}$ goes down to zero, unless the comparator is to be consecutively reset and turned on in oscillation mode. On the other hand, at phase one, the voltage halving circuit requires some time to reach the steady state so the comparison operation could be correctly performed afterwards.

## 3. Transistor-level implementation

For compensating non-idealities of the comparator circuitry and the MOS switches, the abstract comparator-based DLSAR hardware is implemented as the transistor-level circuit of Fig. 5. In the designed DLSAR hardware, MOS switched are rearranged symmetrically so that error due to the clock feedthrough and channel charge injection would be minimized. Nevertheless, dummy switches S1' and S2' are required to further mitigate these effects. Control signals $\Phi_{1d}$ and $\Phi_{2d}$ are delayed version of phases one and two which are used to enable the comparator via active low signal $\overline{CE}$.

### 3.1. Subtractor circuit operation

The designed circuit for the DLSAR ADC employs two identical pairs for input/reference capacitors. Here an auxiliary capacitor, i.e. $C_{ix}$, is also added that enables the circuit to execute the subtraction phase more accurately and with less power dissipation. The subtraction operation is carried out within two passive and active stages as explained below. At the beginning of phase two, the input capacitor starts to discharge into the floating (secondary) reference capacitor $C_{rb}$ while its top plate is connected to the auxiliary capacitor $C_{ix}$ with zero initial charge, rather than ground in the abstract hardware. Accordingly, the subtraction operation is partially performed in passive mode before the comparator turns on.

#### 3.1.1. Passive subtraction

Passive subtraction will continue while the auxiliary capacitor voltage reaches the total voltage drop across $C_{in}$ and $C_{rb}$. This can be expressed as

$$V_i + V_r - \left(\frac{Q_x}{C_{in}} + \frac{Q_x}{C_{rb}}\right) = \frac{Q_x}{C_{ix}} \tag{1}$$

such that $V_i$ and $V_r$ are the initial voltage of the input and reference capacitors and $Q_x = C_{ix}V_x$ is the total transferred charge creating a voltage of $V_x$ across the auxiliary capacitor. By setting $Q_x = C_{rb}V_r$,

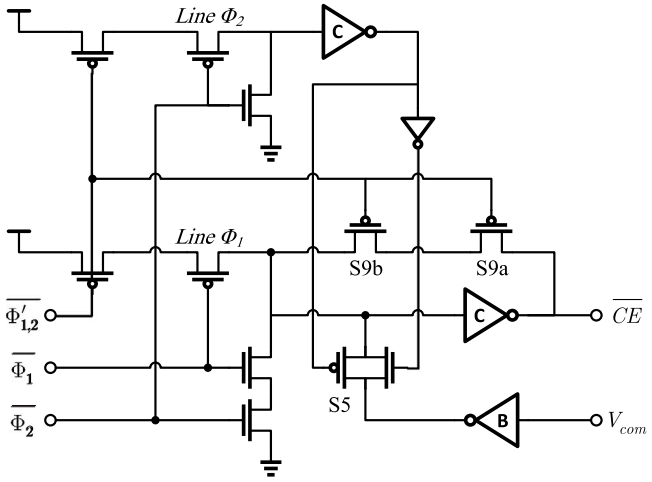



**Fig. 6.** Circuit realization of the phase delay line associated with the comparator enabling signal generator.

the optimum value of the auxiliary capacitor which leads to perfect realization of subtracting the input capacitor by $V_r$, can be found as

$$C_{ix,opt} = C_{in}\frac{V_r}{V_i - V_r}. \quad (2)$$

By selecting all the capacitors equally, the voltage drop across the input capacitor and final voltage of $C_{ix}$ would be the same. Subsequently, the maximum voltage drop does not exceed $V_{x,\max} = V_r$, noting that at subtraction phase always $V_r < V_i \leqslant 2V_r$. Thereby, passive subtraction will not cause any error by over-discharging the input capacitor.

### 3.1.2. Active subtraction

In the rest of phase two, the comparator will be enabled after a specified delay (as passive subtraction is finished) and the subtraction operation continues in active mode if $V_i \neq 2V_r$. As mentioned earlier, at active subtraction the comparator should function in oscillation mode in order for detecting the exact moment to halt the subtractor circuit. The latter is established through the positive feedback loop involving inverters A and B, the NOR gate and the comparator. The comparator must be designed such that its output in the reset state ($\overline{CE} = 1$) is high. Consequently, by closing switch S5, the enabling signal $\overline{CE}$ = not $\left(\overline{V_{com}}\right)$ goes low and the comparator turns on.

While the voltage across the floating reference capacitor, i.e. $V_{rbt} - V_{rbb}$, is positive, the comparator output becomes low as it has been enabled. This results in discrete-time and step-like discharging of the input capacitor consecutively as the comparator output begins to oscillate until the comparison result of $V_{cin}$ vs $V_{rbt}$ becomes zero. It is worth noting that the subtractor circuit inherently opposes with over-discharging the input capacitor because $V_{cin}$ maintains a higher voltage level than the bottom plate of $C_{rb}$, i.e. $V_{rbb}$.

## 3.2. Detailed circuit structure

### 3.2.1. Phase delay line

Fig. 6 depicts the circuit schematic of the phase delay line utilized for generating the comparator enabling signal by adding an appropriate delay after phase one/two is activated. Here the NOR gate is realized using inverter C and five MOS switches to boost up the circuit speed. This will increase the oscillation frequency of the comparator at active subtraction which in turn amends the accuracy of the subtractor circuit. Since in the first approximation step (computing the MSB), the voltage level of input/reference capacitors is larger, the circuit takes more time for halving the reference voltage or discharging the input capacitor during the passive subtraction phase. Thus, the amount of delay should

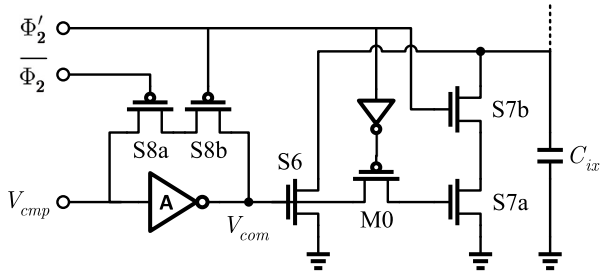



**Fig. 7.** Detailed structure of the driver circuit for the auxiliary capacitor discharge switch S6 embedding break and acceleration mechanism.

be adjusted accordingly for each step of the conversion cycle to improve the time budget and attain the maximum sampling rate in the DLSAR ADC architecture.

The circuit employs two similar delay lines, for phases one and two consisting of two PMOS transistors in series and inverter C. Control signal $\Phi'_{1,2}$ is enabled by the asynchronous control logic circuit after phases one and two has been activated, by adding an proper amount of delay. Additionally, combination of the resistance of the PMOS switches and the input capacitance of inverter C will create a small delay before setting $\overline{CE}$ to zero in order for soft starting the comparator. To further enlarge this extra delay, inverter C could be designed with hi-skewed characteristic curve. As phase one or two is activated, enabling $\Phi'_{1,2}$ is postponed so that in the first/second approximation step a large delay is produced prior to begin the comparison/active subtraction phase. For the subsequent approximation steps, control signal $\Phi'_{1,2}$ is set to one faster that results in reducing the amount of delay.

To ensure that the voltage comparison is accurately fulfilled at phases one and two, PMOS switches S9a,b are placed between the input and output terminals of inverter C. In addition to guaranteeing that the comparator is turned on if the delay line is too slow, this also prevents the enabling signal $\overline{CE}$ from becoming absolutely zero which in turn reduces the positive feedback intensity in the comparator circuit. As a result, the comparator functions as an amplifier to some extent leading to a better robustness against PVT variations of the phase delay line circuit. Along with soft starting the comparator, this will also alleviate input offset voltage of the comparator due to the kickback noise.

### 3.2.2. Break and acceleration mechanism

Although the oscillation frequency of the comparator is rather high and thus step size of the voltage reduction across the input capacitor is small within the active subtraction phase, it is still possible that in the last subtraction step, the input capacitor is over-discharged. To address this issue, a *break* mechanism have to be devised for controlling switch S6 to discharge $C_{ix}$ in the proposed DLSAR ADC hardware of Fig. 5. Furthermore, when the input capacitor voltage and the reference voltage ratio on $C_{rb}$ are close to each other, they reduce to almost zero as the subtraction operation is being executed. As discussed later and according to (13), this would decrease the discharge current to a very small amount. Hence, the subtraction operation will continue too slowly towards the end of phase two. Under this condition, an *acceleration* mechanism is also needed to be embedded into the driver circuit in order to increase the speed of performing the subtraction operation.

The driver circuit schematic of the discharge switch S6 via inverter A is depicted in Fig. 7. The operation of break mechanism can be explained as follows. At the beginning of phase two, control signal $\Phi'_2$ is zero and by closing switches S8a,b the comparator oscillation frequency is increased while the fall time of inverter A output signal, i.e. $V_{com}$, is decreased. Besides, inverter C in Fig. 6 must be hi-skewed while inverter B should be designed with an over low-skewed characteristic. This will enhance the comparator's recovery time and lower the step

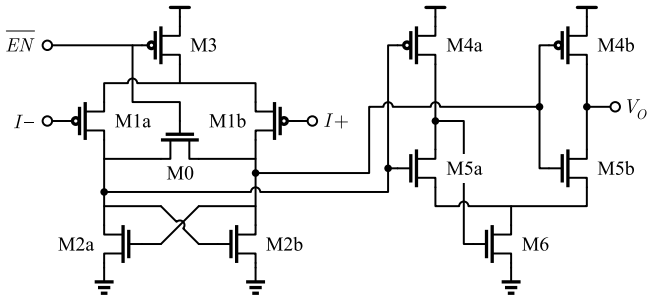



**Fig. 8.** Circuit schematic of the high-speed two-stage dynamic comparator designed for the DLSAR ADC architecture.

size of discharging the auxiliary capacitor, leading to improve the subtractor circuit accuracy.

By S8b being open and activating $\Phi'_2$, acceleration mechanism is enabled that results in enlarging the discharge current of the input capacitor through series switches S7a,b. More precisely, while $V_{com}$ goes down to zero, switch S7a remains closed for a small amount of time since it is derived via the delayed version of $V_{com}$ through PMOS transistor M0. Subsequently, the auxiliary capacitor is partially discharged even with $V_{com}$ being low. After the subtraction operation is completed, $V_{com}$ stays low and thus S7a will turn off momentarily securing that the input capacitor would not be over-discharged. The acceleration mechanism is activated by the asynchronous controller only if subtraction phase persists more than a defined time period.

### 3.3. High-speed comparator design

The comparator is to be designed based on circuit requirements of the DLSAR ADC hardware regarding its operation. Hence, the two-stage topology shown in Fig. 8 is devised to implement the comparator. The first stage is a fully differential preamplifier utilizing NMOS latch to build up positive feedback and boost the comparator speed and response time. Here PMOS input transistors are used since the input common-mode voltage is always below 75% of the supply voltage. The second stage is a self-biased differential amplifier with both NMOS and PMOS driver where the upper tail transistor is removed to decrease the output rise time [23]. This structure is also capable of driving rather large capacitive loads.

The comparator must be designed so that its low-to-high output transition takes place very fast while fall time is kept low enough. In that way, resetting the comparator can be quickly carried out which prevents over-discharging of the input capacitor during the active subtraction. The NMOS cross-coupled M2a,b will reduce the propagation delay as the first/second stage output goes low/high by creating positive feedback. Moreover, adding transistor M0 between the first stage output terminals will significantly improve the comparator's recovery time [24]. It is easy to check that the small-signal voltage gain of the comparator's first stage is

$$\frac{V_{od}}{V_{in}} = \frac{g_{m1}\left(r_{o1} \parallel r_{o2}\right)}{1 - g_{m2}\left(r_{o1} \parallel r_{o2}\right)}. \tag{3}$$

In practice, unequal capacitive loads seen from two outputs of the comparator's second stage may impose systematical offset error. To remedy this, dummy transistors could be connected to the left output. The designed high-speed comparator dissipates 120 μW of power with an operating frequency of 1 GHz and its output propagation delay with respect to the enabling signal $\overline{EN}$ is less than 0.3 ns and 0.4 ns, during the recovery and evaluation phases, respectively.

## 4. Error model and analysis

Here error sources associated with the DLSAR ADC circuit of Fig. 5 will be investigated. A conventional SAR ADC might produce a total unadjusted error (TUE) of more than 1 LSB if it diverges from the correct binary search path [5]. Yet, in the proposed DLSAR binary search algorithm, the TUE is confined below 1 LSB if the converter hardware meets the required conditions, as it is proven shortly. The error model is studied for three operations of comparison, division-by-two and subtraction as well as mismatches of the input/reference capacitors pair. For the sake of simplicity, in each part, the effect of error due to the other sources is ignored.

### 4.1. Comparator input offset

During the comparison phase, offset voltage of the comparator, its loading effect and MOS switches non-idealities could result in an incorrect decision. All these factors could be integrated into the comparator input offset for calculating their associated error in the final DOC. Obviously, the comparator only makes a wrong decision when the scaled input voltage $V_i$ is close the reference voltage ratio $V_r$.

If in the $k$th approximation step of the conversion cycle, the voltage of the input and reference capacitors are nearly equal, e.g. $V_i[k] = V_0 + \varepsilon$ and $V_r[k] = V_0$ such as $|\varepsilon| \ll V_0$, even a small offset voltage $V_{off}$ at the comparator input can cause the corresponding comparison result of $V_i[k] > V_r[k] \equiv \left\langle (V_0 + \varepsilon) - V_0 > -V_{off} \right\rangle$ and the value of bit $b_{N-k}$ to be asserted one for $\varepsilon < 0$ while $V_{off} > 0$, or zero for $\varepsilon > 0$ while $V_{off} < 0$, incorrectly.

For the first case as $b_{N-k} = 1$, the subtraction phase is also performed in the current approximation step. Consequently, because of existing an offset error at the comparator input, the input and floating reference capacitors would be discharged to voltage of $\varepsilon + V_{off}$ and $V_{off}$, respectively. The comparison operation for the next step can be expressed as

$$\begin{aligned} &V_i[k+1] > V_r[k+1] \\ &\quad \equiv \left\langle (V_{off} + \varepsilon) - \left(\frac{V_0}{2} + \frac{V_{off}}{2}\right) > -V_{off} \right\rangle \\ &\quad \cong \left\langle \frac{3V_{off}}{2} - \frac{V_0}{2} > 0 \right\rangle. \end{aligned} \tag{4}$$

Thereby, it is straightforward to check that the comparison result will be asserted zero until the $(k+n)$-th step if $\left|V_{off}\right| < V_0/2^{n+1}$. For the second case as $b_{N-k} = 0$, in the next step, the reference voltage ratio is halved and now the comparison operation is to be fulfilled for

$$\begin{aligned} V_i[k+1] > V_r[k+1] &\equiv \left\langle (V_0 + \varepsilon) - \frac{V_0}{2} > -V_{off} \right\rangle \\ &\cong \left\langle \frac{V_0}{2} + V_{off} > 0 \right\rangle \end{aligned} \tag{5}$$

which most likely its result will be asserted one. Then, in the rest of the current approximation step, subtraction phase is executed and while the offset error is positive/negative, both capacitors would under/over-discharge by amount of $V_{off}$. Hence, voltages of the input and reference capacitors in the next step can be written as $V_i[k+2] = V_0/2 + \varepsilon + V_{off}$ and $V_r[k+2] = V_0/4 + V_{off}/2$, repetitively.

By repeating the same procedure, for comparison phase in the $(k+n)$-th step we get

$$\begin{aligned} &V_i[k+n] > V_r[k+n] \\ &\equiv \left\langle \begin{aligned} &\left(\frac{V_0}{2^{n-1}} + \varepsilon + \frac{\left(2^{n-1}-1\right)V_{off}}{2^{n-2}}\right) \\ &-\left(\frac{V_0}{2^n} + \frac{\left(2^{n-1}-1\right)V_{off}}{2^{n-1}}\right) > -V_{off} \end{aligned} \right\rangle \\ &\cong \left\langle \frac{V_0}{2^n} + \frac{\left(2^{n-1}-1\right)V_{off}}{2^{n-1}} + V_{off} > 0 \right\rangle. \end{aligned} \tag{6}$$

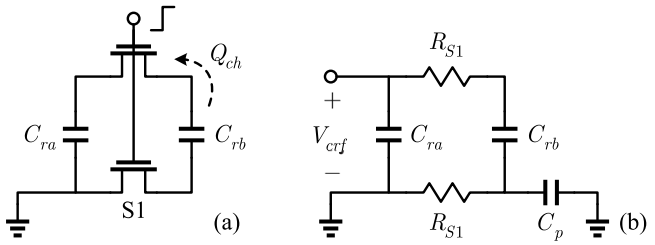



**Fig. 9.** Error model of the voltage halving circuit including (a) channel charge injection, (b) switches resistance and parasitic capacitance.

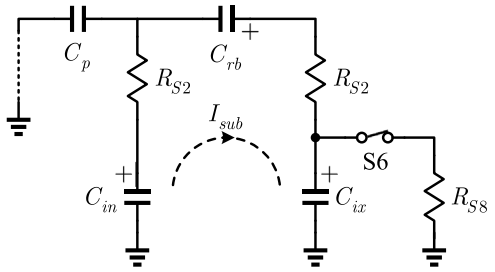



**Fig. 10.** Circuit model of the subtraction operation within one step as the input capacitor discharges into $C_{rb}$ by discharging $C_{ix}$.

The latter indicates that the comparator offset error is not unrestrainedly propagated through the subsequent approximation steps and it is always below $2V_{off}$. To keep the converter TUE below 1 LSB under the first/second scenario, all the comparison results and output bits ahead of the $k$th step must be asserted zero/one to the end of the conversion cycle. According to (6), this can be guaranteed by design provided that magnitude of the input offset voltage $V_{off}$ is kept smaller than the equivalent voltage of 0.5 LSB.

Assuming perfect matching, the designed DLSAR hardware only imposes systematical negative offset at the comparator input where it is effectively compensated via two dummy switches S1' and S2'. The comparator offset error varies within each step of a conversion cycle and it is ideally mitigated for smaller amounts of the input common-mode voltage, as the PMOS input transistors goes to the moderate inversion region where their transconductance enlarges. Hence, the offset error is smaller in determining the lower bits that will improve the converter accuracy.

### 4.2. SC voltage halving circuit

In the proposed DLSAR circuit, the division-by-two operation is realized by paralleling the reference capacitor $C_{ra}$ with the floating reference capacitor $C_{rb}$ holding an initial zero charge. Noting that the comparison operation is executed during switches S1 being closed, the channel charge of the upper NMOS switch is sunk from the reference capacitors altering their voltage. This phenomenon is demonstrated in Fig. 9-a while it is assumed that the total channel charge of the upper switch would pass through $C_{rb}$ as channel charge of an NMOS transistor is negative and the initial voltage of $C_{rb}$ is zero. It must be noted that the PMOS S1 switch will cancel out some of the injected channel charge yet it is here omitted for the sake of simplicity. The channel charge of the upper switch in the $k$th approximation step, and after the circuit is stabilized, can be written as

$$Q_{ch}[k] = -WLC_{ox}\left(V_{DD} - \frac{V_r[k-1]}{2} - V_{Tn}\right). \tag{7}$$

Thereby, the excess voltage error created due to the channel charge injection is computed as $\Delta V_{div} \approx -Q_{ch}[k]/C_{rb}$ which will be halved in the next approximation step.

From (7) it is concluded that the channel charge error enlarges within the last approximation steps in which the reference voltage ratio $V_r$ is reduced to a few LSBs. If the maximum channel charge is presumed to be $Q_{ch,\max} = -WLC_{ox}(V_{DD} - V_{Tn})$, the total error associated with the reference voltage is always smaller than

$$E_{div}[k] < \frac{\left(2^{k-1}-1\right)\Delta V_{div,\max}}{2^{k-1}} + \Delta V_{div,\max} \tag{8}$$

in the worst case. Ultimately, the errors due to the channel charge injection and clock feedthrough of S1 switches in the voltage halving circuit appear as negative offset voltage at the comparator input that is suppressed by the dummy switch S1' and can be controlled, as justified earlier.

To study the effect of switches resistance and bottom plate parasitic capacitance of the floating reference capacitor $C_{rb}$, the circuit model shown in Fig. 9-b can be used. The voltage of the reference capacitor in s-domain, by assuming an initial zero charge for $C_{rb}$, is obtained as

$$V_{crf}(s) = \frac{V_{r0}}{s}\left[1 - \frac{\tau_p\left(s+\frac{1}{\tau_p}\right)/\tau_{div}}{s+\tau_p\left(s+\frac{1}{\tau_p}\right)\left(s+\frac{1+C_{ra}/C_{rb}}{\tau_{div}}\right)}\right] + \frac{V_{p0}}{s}\left[\frac{s/\tau_{div}}{s\left(s+\frac{2}{\tau_{div}}\right)+\frac{2}{\tau_p}\left(s+\frac{1}{\tau_{div}}\right)}\right] \tag{9}$$

where $V_{r0}$ and $V_{p0}$ are the initial voltage of $C_{ra}$ and $C_p$, $\tau_{div} = R_{S1}C_{ra,b}$ is the time constant of the voltage halving circuit and $\tau_p = R_{S1}C_p \ll \tau_{div}$. Using the final value theorem, $V_{crf}$ can be calculated at the steady state as follows

$$\lim_{t\to\infty} V_{crf}(t) = \lim_{s\to 0} sV_{crf}(s) = V_{r0}\left(\frac{C_{ra}}{C_{ra}+C_{rb}}\right). \tag{10}$$

Thereby, the final value of the reference capacitor voltage equals $V_{r0}/2$ independent of resistance of the switches and $V_{p0}$ provided that the reference capacitors are perfectly matched. In summary, any error from the voltage halving circuit can be adequately eliminated by applying the proper amount of delay prior to executing the comparison phase so that the reference voltage ratio reaches the steady state beforehand.

### 4.3. Discrete-time subtractor circuit

In the DLSAR ADC architecture, the subtractor emulates the DAC function and thus it is sensible that it would be the main error source of the converter. Since continues-time and perfect realization of the subtraction operation is infeasible using comparator, the devised discrete-time subtractor circuit might over or under discharge the input capacitor and cause the converter TUE to be further magnified. This can be perceived by regarding step-like decreasing of the input capacitor voltage as the auxiliary capacitor discharge switch is closed and opened during the active subtraction phase. Moreover, the parasitic capacitance associated with the floating reference capacitor bottom plate can deteriorate the subtractor circuit accuracy and need to be compensated.

#### 4.3.1. Parasitic capacitance suppression

At the beginning of phase two, the input, floating reference and auxiliary capacitors are placed in series as shown in Fig. 10. In the presence of the parasitic capacitance $C_p$, the input capacitor would not entirely discharge into $C_{rb}$ especially during the passive subtraction phase. The corresponding error propagates through the next comparison phase as $C_{in}$ and $C_{rb}$ get over and under discharged, respectively. It can be verified that the final voltage of the input capacitor, after passive subtraction is fulfilled and prior to closing switch S6, equals

$$V_{cin} = \frac{2V_i - V_r}{3 + 2C_p/C_{in}} \tag{11}$$

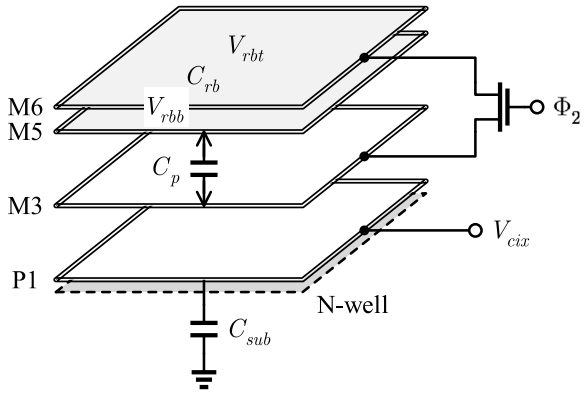



**Fig. 11.** Shielding technique for cancellation of the bottom plate parasitic capacitance of the floating reference capacitor at phase two.

that will approximately produce an under/over-discharge error of $0.22(C_p/C_{in})(2V_i - V_r)$ on $C_{in}/C_{rb}$ voltage. Although perfect cancellation of the bottom plate capacitance is not feasible in practice, it can be mitigated by shielding.

Fig. 11 demonstrates the devised shielding technique that employs two planes in metal 3 and polysilicon layer guarded by an N-well under the metal–insulator–metal (MIM) capacitor $C_{rb}$ formed among metal 6 and 5, i.e. nodes $V_{rbt}$ and $V_{rbb}$ in the DLSAR ADC circuit. At subtraction phase, the M3 shield plane is connected to the top plate of $C_{rb}$ so that the parasitic capacitance $C_p$ is isolated and the coupling capacitance between its bottom plate and the substrate is minimized. On the other hand, the P1 shield plane and N-well is directly tied to the top plate of $C_{ix}$, i.e. node $V_{cix}$. Under this situation, the capacitor formed between the two M3 and P1 shield planes becomes parallel with switch $S2$ and the surplus coupling capacitance to the substrate, i.e. $C_{sub}$, would be absorbed by the auxiliary capacitor where it could be compensated by reducing $C_{ix}$. It is worth noting that $C_p$ does not alter the total charge of $C_{rb}$ and create more error since it has an initial zero voltage. Therefore, the final charge of the input capacitor is equal to $C_{in}V_i - C_{rb}V_r = C_{in}(V_i - V_r)$ when the floating reference capacitor is entirely discharged and the subtraction operation is completed.

#### 4.3.2. Active subtraction error

The error due to the subtraction operation can be studied using circuit model of Fig. 10 such that all the capacitors are assumed to be equal and $C_p = 0$. If in a conversion cycle, the first subtraction operation takes place in the $k$th approximation step, we presume that after finishing the passive subtraction, the voltage of the input, floating reference and auxiliary capacitors is $V_i[k] = V_{i0}$, $V_r[k] = V_{r0}$ and $V_x[k] = V_{x0}$. The active subtraction phase begins by closing switch S6. Subsequently, the input capacitor discharge current in s-domain is computed as

$$\begin{aligned} I_{sub}(s) &= \frac{sC_{ix}\left(s+\frac{1}{\tau_2}\right)\left(\frac{V_{i0}+V_{r0}}{s}-\frac{V_{x0}}{s+\frac{1}{\tau_2}}\right)}{s+2R_{S2}C_{ix}\left(s+\frac{1}{\tau_1}\right)\left(s+\frac{1}{\tau_2}\right)} \\ &= \frac{\tau_2^{-1}\left(V_{i0}+V_{r0}\right)}{2R_{S2}(s+\alpha)(s+\beta)}+\frac{s\left(V_{i0}+V_{r0}-V_{x0}\right)}{2R_{S2}(s+\alpha)(s+\beta)} \end{aligned} \tag{12}$$

where $\tau_1 = R_{S2}C_{in}$, $\tau_2 = R_{S6}C_{ix}$, and $\alpha$ and $\beta$ are the roots of the transfer function denominator.

As clarified earlier, after completing the passive subtraction is finished, the voltage of the auxiliary capacitor $C_{ix}$ is equal to the sum of the input and reference capacitor voltages. As a result, the second term in (12) could be omitted and the discharge current in time domain equals

$$I_{sub}(t) = \frac{V_{i0}+V_{r0}}{2R_{S2}R_{S6}C_{ix}} \cdot \frac{1}{\beta-\alpha}\left(e^{-\alpha t}-e^{-\beta t}\right). \tag{13}$$

Provided that the comparator oscillation frequency is high enough, the time interval in which switch S6 is closed is much smaller than the subtractor circuit time constant. Then, using the approximation of $e^{-x} \approx 1 - x$ we get

$$\Delta I_{sub} = \lim_{\Delta t \to 0} I_{sub}(\Delta t) = \frac{V_{i0}+V_{r0}}{2R_{S2}R_{S6}C_{ix}}\Delta t. \tag{14}$$

The latter implies that the step size of the input capacitor voltage reduction is proportional to its initial voltage and also that of $C_{rb}$ and it can be written as

$$\Delta V_{sub} \approx \frac{\Delta I_{sub}\Delta t}{C_{in}} = \frac{V_{i0}+V_{r0}}{2} \cdot \frac{\Delta t^2}{\tau_1\tau_2}. \tag{15}$$

According to (15), the subtraction error in the $k$th approximation step in the worst case is

$$E_{sub}[k] = \pm\delta\left(V_i[k]+V_r[k]\right) \triangleq V_{err} \tag{16}$$

such that factor $\delta = 0.5\Delta t^2/(\tau_1\tau_2)$ is very small because the comparator oscillation frequency is high and the circuit works with the break mechanism. Now the voltage of the input and reference capacitors by including the subtractor circuit error in the next step can be computed as $V_i[k+1] = V_{i0} - V_{r0} - V_{err}$ and $V_r[k+1] = (V_{r0} - V_{err})/2$. Thereby, the subtraction error in this step (by assuming $V_{err} \ll V_{r0}$) is obtained as

$$\begin{aligned} E_{sub}[k+1] &= \pm\delta\left(V_i[k+1]+V_r[k+1]\right) \\ &\approx \pm\left|\frac{V_{err}}{2}\right| \mp \delta\left(V_{r0}-\frac{V_{i0}}{2}\right) \end{aligned} \tag{17}$$

which is always less than $E_{sub}[k]/2$.

If the subtraction operation is not to be performed from the current step ahead, by substituting $E_{sub}[k+n] = V_{err}/2^n$, the comparison of the scaled input voltage and reference voltage ratio in the $(k+n)$-th step can be expressed as

$$\begin{aligned} &V_i[k+n] > V_r[k+n] \\ &\equiv \left\langle \begin{matrix} \left(V_{i0}-\frac{(2^n-1)V_{r0}}{2^{n-1}}-\frac{(2^n-1)V_{err}}{2^{n-1}}\right) \\ -\left(\frac{V_{r0}}{2^n}-\frac{V_{err}}{2^n}\right) > 0 \end{matrix} \right\rangle \\ &\equiv \left\langle V_{i0}-\frac{(2^{n+1}-1)V_{r0}}{2^n}-\frac{(2^{n+1}-3)V_{err}}{2^n} > 0 \right\rangle. \end{aligned} \tag{18}$$

From (18) it is evident that the under/over-discharge error due to the discrete-time subtraction could be referred to input offset voltage of the comparator with a magnitude lower than $2V_{err}$. Hence, the subtraction error will not unrestrainedly propagate. In another case, if the subtraction operation should be executed until step $(k+n-1)$-th, it can be verified that comparison phase in the next step is corresponding to

$$\begin{aligned} &V_i[k+n] > V_r[k+n] \\ &\equiv \left\langle \begin{matrix} \left(V_{i0}-\frac{(2^n-1)V_{r0}}{2^{n-1}}-\frac{nV_{err}}{2^{n-1}}\right) \\ -\left(\frac{V_{r0}}{2^n}-\frac{nV_{err}}{2^n}\right) > 0 \end{matrix} \right\rangle \\ &\equiv \left\langle V_{i0}-\frac{(2^{n+1}-1)V_{r0}}{2^n}-\frac{nV_{err}}{2^n} > 0 \right\rangle. \end{aligned} \tag{19}$$

This time, the subtractor circuit error is not magnified through the subsequent approximation steps and instead it is ideally suppressed in which lower bits are being determined.

### 4.4. Capacitors mismatch

So far it was assumed that the input/reference capacitors are equal and perfectly matched. In the DLSAR ADC, the mismatch error of capacitors is not crucial as much as binary capacitor bank in the conventional SAR ADC since the proposed architecture only employs four identical

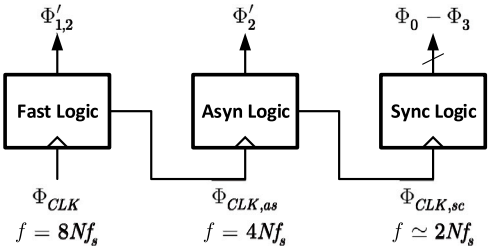



**Fig. 12.** Abstract schematic of the asynchronous control logic circuit developed for the DLSAR ADC showing its three building blocks.

and rather large capacitors. If the discrepancy between the reference capacitors pair equates to $\pm\Delta C$, in the division-by-two operation, an error of $0.5(\Delta C/C_0)V_r$ is produced compared to the ideal amount of $V_r$ where $C_0$ corresponds to the average value of the capacitors. On the other hand, the discrepancy between the input and reference capacitors will impose an under/over-discharge error of $(\Delta C/C_0)\Delta V_{sub}$ within the subtraction operation. Ultimately, the capacitors mismatch error can be again attributed to the comparator offset or the subtraction circuit error that have been already elaborated.

The theoretical analysis carried out in this section proves that the DLSAR architecture is fairly robust against various error sources of the implemented circuit. In summary, the SC voltage halving circuit is almost error free and the error due to the subtractor circuit would be mitigated if the subtraction operation is to be executed repeatedly in several approximation steps. Channel charge injection of MOS switches, capacitance loading, offset voltage of the comparator and single-step subtraction phase are the main causes for magnifying the DLSAR ADC TUE. However, these errors can be controlled in a well-designed circuit implementation.

## 5. Control logic circuit

As clarified earlier, in the DLSAR binary search, each step of a conversion cycle is comprised of two consecutive operational phases. During the first phase, the reference voltage ratio is halved and compared with the scaled input voltage and at the second phase, subtraction operation or discharging the floating reference capacitor would be performed. Accordingly, in a synchronous control scheme the clock frequency of the DLSAR ADC must be at least twice the conventional SAR counterpart, i.e. $2Nf_s$, where $N$ is the number of bits and $f_s$ is the sampling frequency of the converter. Synchronous control is preferred for lower sampling rates and its logic circuit may be simply realized using a counter that generates the phase control signals, i.e. $\Phi_0$ to $\Phi_3$, in the right order.

### 5.1. Asynchronous control scheme

While achieving high sampling rates is desired, synchronous control scheme is not an optimum choice for SAR ADCs [25,26]. In the designed DLSAR hardware, that is because the time period required for executing the division-by-two and especially the subtraction operations differ from one approximation step to another as the analog input signal varies. Therefore, an asynchronous control scheme is devised which adaptively schedules and retimes each step within a conversion cycle. In order to guarantee that the controller could properly determine the beginning and final time instants of phases one and two fast enough, the time budget of the asynchronous control logic circuit must be doubled once more.

To reduce the power dissipation, the asynchronous DLSAR control logic is realized via three circuit blocks as depicted in Fig. 12, namely the fast, asynchronous and synchronous logic circuits. The $8Nf_s$ high clock frequency is only needed for the fast logic block which is a small circuit responsible for generating the control signal $\Phi'_{1,2}$ for the phase delay lines. The fast logic circuit also produces the asynchronous logic clock $\Phi_{CLK,as}$ with a duty cycle of 75% to decrease the time interval in which all the phases are deactivated and the converter is idle. As a result, the time budget and sampling rate of the converter is enhanced. The clock of the synchronous logic $\Phi_{CLK,sc}$ is provided by the asynchronous logic circuit that is adaptively scheduled for each comparison/subtraction phase within a conversation cycle.

Obviously, the asynchronous controller for the DLSAR architecture is more complicated than the synchronous one or the SAR counterpart. Nonetheless, the proposed DLSAR ADC would not require any hard/soft calibration which may be regarded as an advantage in return. In the proposed asynchronous DLSAR control logic, time duration of each phase is controlled via the corresponding threshold parameters with respect to the number of passed clock pulses within the activated phase. Also, a parameter defines the threshold number for enabling the acceleration mechanism. The optimum values of the threshold parameters and the main clock duty cycle could be found under various PVT working condition as a low cost soft calibration method. Nevertheless, the proposed DLSAR ADC would achieve the desired performance even though the controller is to be set permanently.

**Table 1**
Hardware utilization report of the asynchronous DLSAR control logic synthesis by digital standard cells.

| | Fast logic | Asyn logic | Sync logic | Total |
|---|---|---|---|---|
| Cell count | 14 | 62 | 89 | 165 |
| Area (%) | 9.2 | 38.7 | 52.1 | 3e3 μm$^2$ |

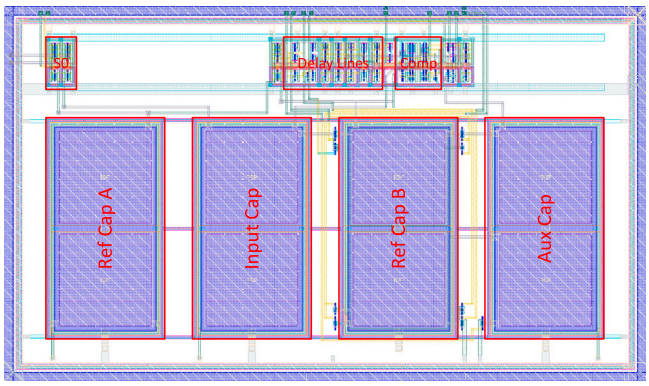



**Fig. 13.** Layout of the designed DLSAR hardware excluding the asynchronous control logic circuit. The circuit area is about 175 μm × 100 μm.

### 5.2. Logic circuit implementation

The asynchronous control logic circuit of the DLSAR ADC is implemented using the standard cell library in 0.18 μm CMOS process with the synthesis report given in Table 1. The average power dissipation of the DLSAR logic circuit is about 65 μW at the clock frequency of 128 MHz, that is corresponding to a sampling rate of 2 MS/s for 8-bit resolution. If the DLSAR ADC is to be utilized for lower sampling rates, the synchronous control scheme may be employed that will substantially reduce the complexity and power consumption of the logic circuit.

One main feature of the proposed DLSAR architecture is its versatility in a sense that the DLSAR hardware is not dependent on the number of bits. Hence, the converter can be easily reconfigured for other sets of sampling rate and resolution only by reprogramming the controller, as long as $4Nf_s$ is lower than its maximum operating frequency. In many applications, the ADC works next to a digital processor, e.g. an ARM Cortex-M core. Subsequently, the digital processors can directly control

**Table 2**
Optimal Design Set for Transistors Aspect Ratio ($L = 0.18$ μm) of the Developed 8-bit 2 MS/s DLSAR ADC.

| Switch | S0 | S1,2 | S3,4 | S5 | S6,7 | S8 |
|---|---|---|---|---|---|---|
| W (μm) | N:2<br>P:4 | N:2<br>P:2 | 1.5 | N:0.5<br>P:0.25 | 0.5 | 0.25 |
| Inverter | A | B | C | | | |
| W (μm) | N:0.25<br>P:0.5 | N:0.5<br>P:0.25 | N:0.25<br>P:1 | | | |
| Delay line | M0 | S9 | SxN | SxP | | |
| W (μm) | 0.5 | 0.25 | 0.5 | 0.25 | | |
| Comp. | M0 | M1 | M2 | M3 | M4 | M5,6 |
| W (μm) | 0.5 | 2 | 1 | 1 | 1 | 1 |

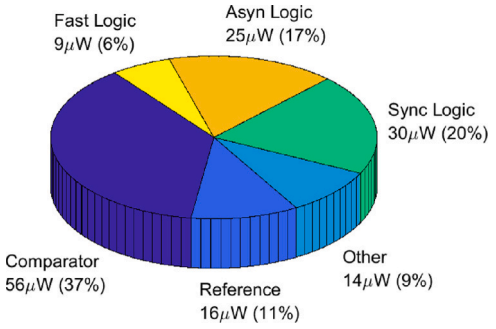



**Fig. 14.** Power breakdown associated with the different circuit blocks of the developed 8-bit 2 MS/s DLSAR ADC at 1.8 V supply voltage.

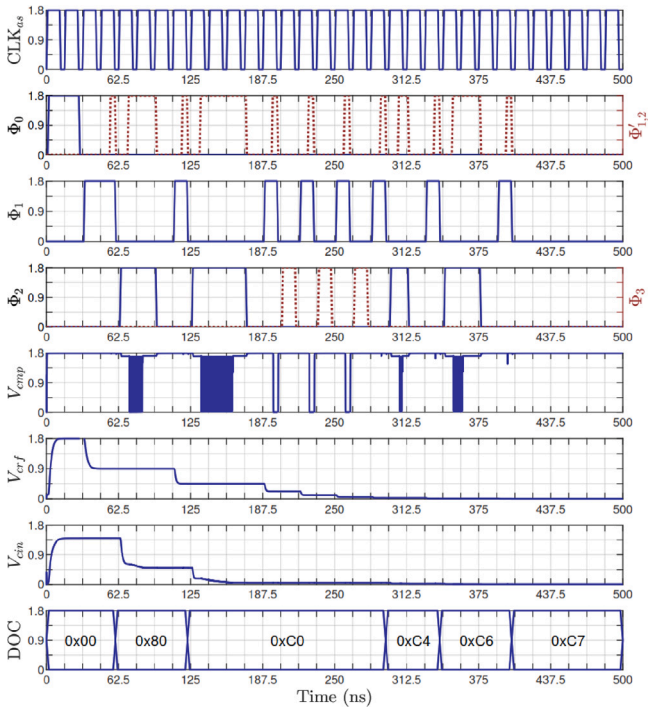



**Fig. 15.** Phase control, comparator output and input/reference capacitors voltage signals within a conversion cycle for 1.4 V analog input.

the DLSAR ADC by generating the phase control signals and compute the converter DOC by reading the comparator output. This approach would enhance the system flexibility and adaptability as the converter control procedure is integrated with the software.

## 6. Results and discussion

As the clock frequency in the DLSAR architecture is four times larger than that of the SAR counterpart, it might be inefficient to design the DLSAR ADC for very high sampling rates. Thus, we have designed and optimized the DLSAR ADC for 8-bit resolution and 2 MS/s sampling rate, based on Table 2. Size of the input/reference capacitors pair is chosen as 2.5 pF each implemented via the MIM structure. The capacitors size must be selected large enough to ensure that $kT/C$ noise from the S/H circuit, and also the error due to the division-by-two and subtractor circuits will remain below the quantization noise, based on the theoretical analyses in Section 4.

Fig. 13 shows the designed layout of the DLSAR ADC hardware. It can be seen that the MIM input/reference capacitors have occupied around 80% of the total circuit area. At 1.8 V supply voltage, the developed DLSAR ADC consumes 85 μW of power while it attains a figure-of-merit (FoM) of 0.19 pJ/c-s, without including the logic circuit. The decomposed power consumption of the converter's main building blocks is depicted in Fig. 14. As expected, the amount of power is mostly determined by the asynchronous controller and the comparator within the subtraction phase.

### 6.1. DLSAR waveforms and operation

As an example, the waveforms of the internal and control signals of the designed DLSAR ADC are plotted in Fig. 15 for one conversation cycle for 1.4 V analog input. The converter's final DOC equates to 199 which is updated right after the latest comparison phase leaving the converter in the idle state for the next six clock pulses. The voltage halving circuit operation could be observed from the reference capacitor voltage waveform, and passive and active stages of the subtraction phase can be easily distinguished regarding the input capacitor voltage waveform. At active subtraction, the comparator oscillation frequency is up to 1.4 GHz while the step size of discharging the input capacitor is averagely 6.7 mV and 0.2 mV at the first and last subtraction, respectively. The latter is depicted with more details in Fig. 16.

### 6.2. Performance metrics simulation

In the following, performance of the designed DLSAR ADC is investigated based on post-layout simulations. The corresponding metrics have been extracted by conservative transient analysis with including noise from the MOS devices to ensure getting reliable results.

#### 6.2.1. Static error

The differential non-linearity (DNL) and integral non-linearity (INL) of the designed DLSAR ADC are plotted in Fig. 17. Here the full-scale range of the converter is swept by a ramp signal with a half period of 0.9 ms. Therefore, the voltage resolution of the test is 1 mV corresponding to about 0.14 LSB. Absolute value of the DNL is less than 0.5 LSB and 0.25 LSB for 97% and 75% of DOCs, respectively. As proven earlier in Section 4-C, the DNL has mostly peaked around the DOCs in which the subtraction operation is performed only once or twice. Yet, the DNL magnitude is relatively smaller for DOCs below 128 that would enhance the converter performance since the ratio of error-to-DOC determines the overall linearity.

The offset and gain error of the converter is equal to 0.57 and 0.13 LSB. The TUE can be approximated by [27]

$$TUE = \sqrt{E_{OS}^2 + E_G^2 + INL^2} \tag{20}$$

which gives $TUE \approx 0.81$ LSB over full-scale range of the DLSAR ADC, i.e. 0–1.8 V.

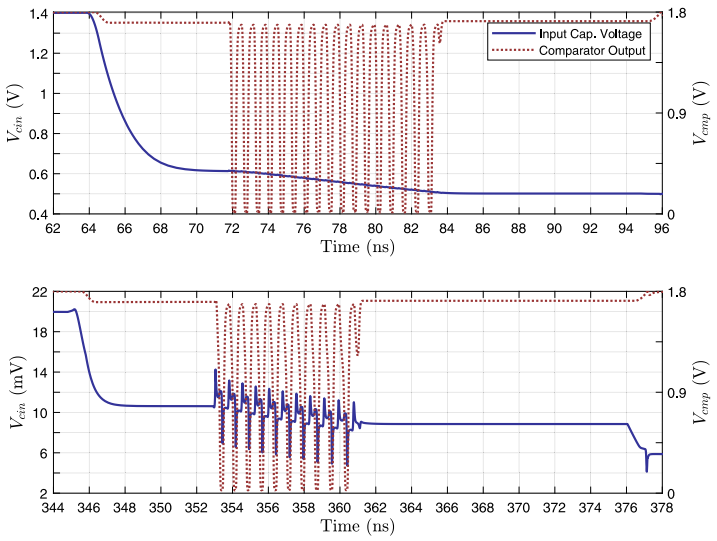



**Fig. 16.** Magnified view of the input capacitor voltage waveform as the first and last subtraction operation is being executed.

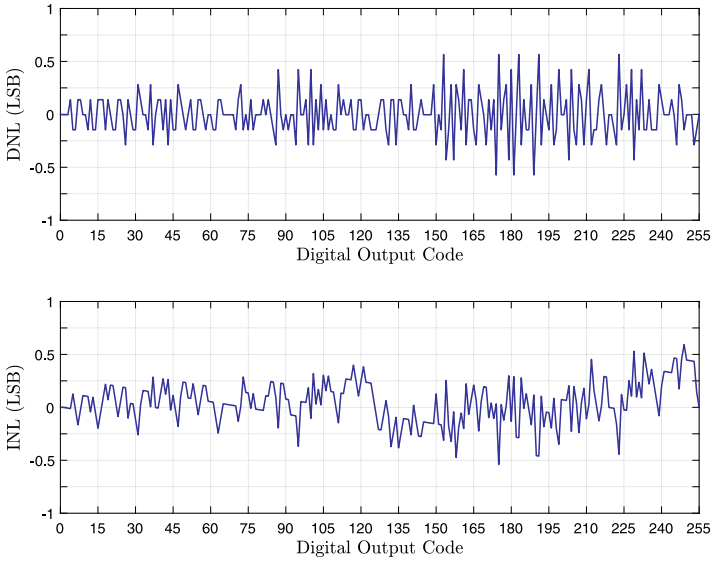



**Fig. 17.** Differential and integral non-linearity profiles of the developed DLSAR ADC obtained by applying a full-scale input ramp signal.

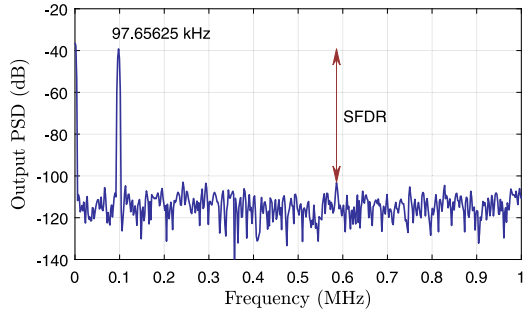



**Fig. 18.** Power spectral density of the DLSAR ADC digitized output for a full-scale sinusoidal input signal with $OSR = 10.24$.

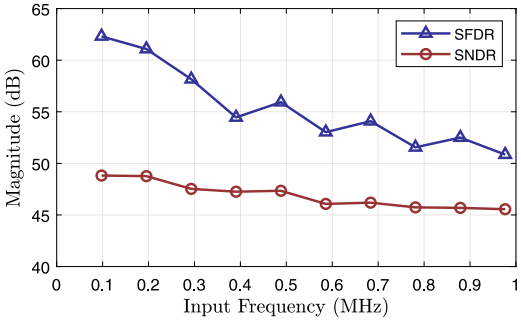
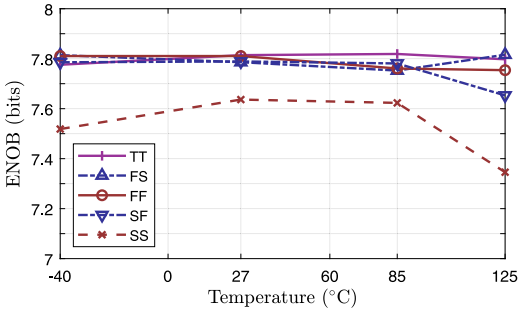



**Fig. 19.** SFDR and SNDR of the DLSAR ADC for different input frequencies with 8-bit resolution at 2 MS/s.

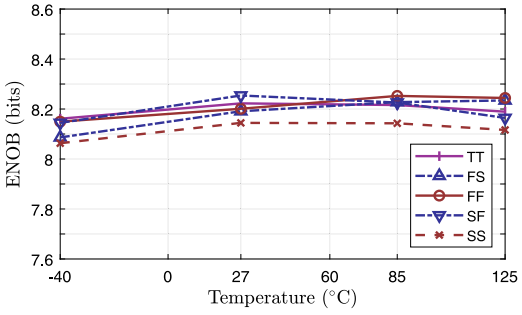
**Table 3**
Simulated DLSAR ADC characteristics across various process corners and temperatures.

| $T$ (°C) | TT | | | FF | | | FS | | | SF | | | SS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | −40 | +27 | +85 | −40 | +27 | +85 | −40 | +27 | +85 | −40 | +27 | +85 | −40 | +27 | +85 |
| SFDR (dB) | 63.1 | **62.3** | 62.8 | 62.5 | **62.9** | 62.0 | 61.7 | **62.2** | 62.1 | 63.1 | **63.1** | 61.4 | 57.0 | **59.8** | 61.3 |
| SNDR (dB) | 49.0 | **48.7** | 49.2 | 49.2 | **49.2** | 48.9 | 48.7 | **48.5** | 48.8 | 49.0 | **49.0** | 48.5 | 45.4 | **47.6** | 47.6 |
| FoM (fJ/c-s) | 181 | **192** | 187 | 211 | **221** | 239 | 163 | **171** | 170 | 217 | **224** | 254 | 243 | **187** | 192 |
| Power (μW) | 82.9 | **85.4** | 88.7 | 99.1 | **104** | 109 | 72.8 | **74.6** | 76.6 | 101 | **104** | 110 | 71.8 | **73.5** | 75.0 |

* Calculated by excluding power consumption of the control logic circuit.




(a) 8-bit resolution and at $f_s = 2$ MS/s




(b) 9-bit resolution and at $f_s = 1$ MS/s

**Fig. 20.** The DLSAR ADC effective number of bits with 97.65625 kHz input frequency vs various process corners and temperatures.

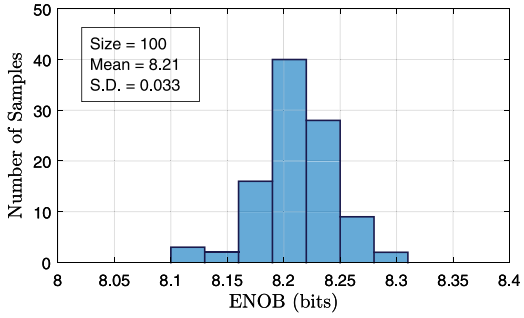



**Fig. 21.** Monte Carlo histogram for the DLSAR ADC effective number of bits obtained with $OSR = 5.12$ and 9-bit resolution.

### 6.2.2. Dynamic behavior

In order for computing the dynamically related metrics of the designed DLSAR ADC, a full-scale sinusoidal input signal is employed. For the input frequency of 97.65625 kHz and equivalent oversampling ratio (OSR) of 10.24, the power spectral density (PDS) of the converter output is shown in Fig. 18. Thereby, the spurious-free dynamic range (SFDR) and signal-to-noise-and-distortion ratio (SNDR) are calculated as 62.3 dB and 48.7 dB, respectively. Accordingly, the optimum value of effective number of bits (ENOB) of the DLSAR ADC is up to 7.8 bits.

Fig. 19 plots the SFDR and SNDR versus the input frequency for the designed 8-bit DLSAR ADC. If the input frequency is doubled ($OSR = 5.12$), SFDR and SNDR are obtained as 61.1 dB and 48.6 dB, respectively, that is corresponding to an ENOB of 7.7 bits. It can be observed that the effective resolution bandwidth (ERBW) of the converter extents to $f_s/2$ where the low frequency SNDR would be dropped by −3 dB, corresponding to an ENOB of 7.3 bits. The SFDR is also up to 62 dB within lower frequencies and it is reduced to 51 dB near the Nyquist input.

## 6.3. Corner and mismatch analysis

### 6.3.1. Process and temperature

The characteristics of the designed DLSAR ADC have been evaluated within several process corners and temperatures as given in Table 3. The results clarify that the proposed DLSAR architecture maintains a good robustness against PVT variations with no need for calibration. According to Fig. 20(a), the DLSAR ADC holds its optimal operating condition in all the process corners over the temperature interval of −40 to +125 °C, excluding the SS corner. Nevertheless, the ENOB is always preserved above 7.5 bits for temperatures lower than +85 °C. In the DLSAR ADC architecture, if the comparison or subtraction operation could not be fulfilled in the specified time period, the converter may fail to function properly. This is the reason that in slow corners and at high temperatures the ENOB might be degraded considerably.

To address the latter issue, the converter clock frequency or its number of bits can be reduced to enlarge the evaluation time for each phase and improve the converter time budget. Besides, with 1.8 V reference voltage and a TUE of 6 mV, the affordable resolution of the designed DLSAR ADC is not greater than 8-bit. Obviously, the number of bits can be further increased for larger amounts of reference voltage, and the sampling rate can be boosted up using the pipelined topology as well as interleaving two or more converters. The resolution could be also enhanced if the DLSAR ADC is combined with pipelined SAR topology. For instance, two 6-bit DLSAR converters can be placed in series while the amplified error of the first stage is fed to the second one. Hence, the resolution would be increased to 12 bits readily, however this requires analog circuitry for amplification.

If the converter resolution increments by 1-bit and the clock frequency decreases from 128 MHz to 72 MHz, a sampling rate of 1 MS/s would be attained. It must be noted that these adjustments are only applied to the controller and the DLSAR hardware is remained untouched. By enlarging the time budget and adding one extra bit, the DLSAR ADC performance is expected to be partially improved. The ENOB under the aforesaid situation is plotted in Fig. 20(b) where it is around 8.2 bits across the majority of PVT corners.

### 6.3.2. Mismatches

As justified before, mismatch error due to the input/reference capacitors pair and also the comparator circuitry can degrade the DLSAR ADC performance to some extent. Fig. 21 demonstrates Monte Carlo simulation result of the ENOB obtained by applying a full-scale 97.65625 kHz sinusoidal input signal while the converter is reconfigured to 9-bit resolution at 1 MS/s. Also, the mean SFDR is correspondingly obtained as 62.5 dB with a standard deviation of 0.8 dB. Thereby, it can be observed that the DLSAR ADC ENOB has

**Table 4**
Performance summary of the proposed DLSAR ADC and comparison with state-of-the-art SAR ADCs.

| Specs $f_{CLK,as}$ | This work[a] | | MEJ'22[a] | TVLSI'21[a] | TCASI'21 | MEJ'20[a] | JSSC'19 | TVLSI'19 | MEJ'18 | MEJ'17 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 64 MHz | 36 MHz | [11] | [28][b] | [21][b] | [29] | [12][b] | [30][b] | [31] | [32] | |
| Technology | 0.18 μm | | 0.11 μm | 0.13 μm | 0.13 μm | 0.13 μm | 40 nm | 0.18 μm | 0.18 μm | 0.18 μm | |
| SAR type | DLSAR Asyn. | | Cyclic | NS Syn. | 2C-DAC | NS Syn. | Asyn. | Cyclic | Asyn. | Syn. | |
| Resolution | 8 | 9 | 10 | 9 | 10 | 8 | 12 | 12 | 10 | 10 | bit |
| Sampling rate | 2M | 1M | 333k | 2M | 128k | 1M | 1M | 1.67M | 100M | 1M | S/s |
| OSR[c] | 10.24 | 5.12 | 83.3 | 8 | 32 | 8 | 5 | 4.18 | 1.25 | 1.01 | |
| $[DNL/INL]_{pp}$ | 1.1/1.2 | 2.2/2.3 | 0.8/2.1 | N/A | N/A | N/A | ?/2.8 | 1.0/1.7 | 1.4/1.5 | 1.2/1.6 | LSB |
| SFDR | 62.3 | 62.5 | 69.6 | 92.9 | 90.9 | 97.3 | 88.0 | 55.0 | 62.9 | 67.3 | dB |
| SNDR | 48.7 | 51.2 | 60.6 | 78.7 | 82.6 | 76.9 | 68.1 | 60.1 | 53.7 | 56.7 | dB |
| ENOB | 7.80 | 8.21 | 9.77 | 12.8 | 13.4 | 12.5 | 11.0 | 9.69 | 8.62 | 9.12 | bits |
| $V_{DD}/V_{FS}$ | 1.8/1.8 | | 1.5/1.2 | 1.2/1.13 | 1.6/1.26 | 1.2/1.2 | 1.1/1.1 | 1.8/1.8 | 1.8/1.7 | 3.0/2.0 | V |
| FoM | 337 | 340 | 370 | 34.1 | 925 | 134 | 15.0 | 579 | 123 | 106 | fJ/c-s |
| SFoM | 3.02 | 2.93 | 16.8 | 1.40 | 26.7 | 5.16 | 6.97 | 4.95 | 0.95 | 0.40 | Ç/c-s |
| Power | 150$\mu$ | 100$\mu$ | 107$\mu$ | 59.9$\mu$ | 40.8$\mu$ | 96$\mu$ | 31.1$\mu$ | 0.8m | 5.23m | 59$\mu$ | W |
| Circuit area | 0.020 | | N/A | 0.202 | 0.20 | 0.259 | 0.073 | 0.045 | 0.216 | 0.327 | $mm^2$ |

[a]Papers that have presented simulation results.
[b]Employed hard/soft calibration.
[c]For Nyquist rate converters $OSR = f_s/(2f_{in})$, and for noise shaping converters $OSR = f_s/(2BW)$.

remained up to 8.2 bits and 8.15 bits for 67% and 96% of samples, respectively, while the SFDR is greater than 61.0 dB for 98% of samples. These results imply that the DLSAR architecture is highly robust against the process mismatches with no need for calibration.

### 6.4. Scaled figure-of-merit

The common definition for ADC FoM is given by

$$\text{FoM} = \frac{Power}{2^{ENOB} \cdot \min\{f_s, 2 \times ERBW\}}. \tag{21}$$

In the latter definition, some important metrics of an ADC are not taken into account, such as the supply and full-scale input voltage, OSR in which the ENOB is obtained and the technology scaling factor. To address the aforesaid shortcomings, a range of modified FoMs have been utilized in the literatures that can be reviewed in [33]. Here a scaled FoM (SFoM) is introduced that includes all these factors mentioned above. Denoting the converter full-scale input voltage by $V_{FS}$ and the technology feature size (minimum length) by $L$, SFoM can be computed by

$$\text{SFoM} = \frac{\text{FoM}}{V_{DD}V_{FS} \cdot L^2 \cdot 2^{\beta}} \tag{22}$$

where $\beta = ENOB/N_b(OSR + 1) < 0.5$ represents the ENOB efficiency quantifying that how much the converter was able to reach the performance of a counterpart ideal ADC. The $2^{\beta}$ term then compensates for the ENOB dependency to the input frequency ($\propto OSR$) since the ENOB usually degrades near the converter bandwidth. For Nyquist rate ADCs, $N_b$ is equal to the physical number of bits ($N$), and for the noise shaping ones, it is the sum of $N$ and the theoretical maximum extra bits which can be gained by oversampling.

The SFoM metric roughly normalizes ADC power consumption regardless of the technology node as dynamic power is proportional to $V_{DD}^2$ and gate area of MOS switches, that can be expressed by $L^2$. Also, we have used the term $V_{DD}V_{FS}$ instead to further involve the converter full-scale range. The dimension of SFoM can be written as Ç/c-s where Ç is the normalized capacitance per area in the unit of $F/m^2$.

Table 4 summarizes characteristics of the designed DLSAR ADC and compares them to recent state-of-the-art SAR ADCs. As the power dissipation of the asynchronous control logic and subtractor circuit is rather high in the DLSAR architecture, the converter FoM is relatively larger than other conventional SAR counterparts. Nonetheless, some papers does not include the power consumption of the calibration or reference voltage generator/buffer circuits in their total power report. Yet, inspecting the SFoM reveals that the DLSAR ADC performance is superior compared to most of the relevant designs regarding its higher ENOB efficiency and extended full-scale range. Consequently, we can claim that the DLSAR architecture is highly scalable to smaller technology nodes. Furthermore, the circuit area of the DLSAR ADC is much smaller as it does not require the formal reference voltage generator/buffer with large on-chip decoupling capacitors.

## 7. Conclusion

The DAC block realization is usually challenging in SAR ADCs and confines the converter's overall performance in terms of linearity and dynamic range. Because of embedding lots of switches and capacitors, capacitive DACs are difficult to tune within all PVT corners and thus they must be calibrated in general. In this work, a versatile DAC-less SAR ADC architecture has been introduced which eliminates some drawbacks of the SAR counterpart rising from the DAC limitations. The DLSAR ADC employs an alternative binary search algorithm emulating the DAC function by combining two arithmetic operations of division-by-two and subtraction. The DLSAR hardware is implemented in 0.18 μm CMOS process using the default circuit building blocks of a SAR ADC, i.e. one comparator, four capacitors and switches.

We have designed the DLSAR ADC for 8-bit resolution and the sampling rate of 2 MS/s. The average power of the DLSAR hardware is 85 μW and the asynchronous controller has a power consumption of 65 μW at the clock frequency of 128 MHz. Based on extensive post-layout simulations, the designed converter achieves a SFDR up to 62 dB and ENOB of 7.8 bits in the typical corner, showing low sensitivity to temperature changes as well. Furthermore, the ENOB is generally maintained above 7.5 bits across various PVT corners without any calibration. The FoM of the DLSAR ADC is equal to 0.34 pJ/c-s while its SFoM metric reaches 3.0 Ç/c-s, indicating that the DLSAR architecture would work more efficiently in smaller technology nodes.

Comparing to the state-of-the-art SAR ADCs, the designed DLSAR ADC dissipates more power but it occupies smaller circuit area. This relatively large power firstly stems from the asynchronous controller and secondly by performing the discrete-time subtraction phase above the speed of 1 GHz. Yet, speed and power efficiency of the proposed DLSAR architecture is superior next to the analogous topologies of cyclic and 2C-DAC as analog circuits have been omitted. Although it might seem inefficient, noting that the DLSAR ADC shows excellent static and dynamic performance with negligible sensitivity to PVT variations without calibration, this surplus power overhead will become justifiable. Besides, at lower sampling rates, simple synchronous control scheme can be employed which in turn leads to a significant reduction in total power consumption.

## CRediT authorship contribution statement

**Ali Pourahmad:** Conceptualization, Methodology, Software, Writing – original draft. **Rasoul Dehghani:** Supervision, Investigation, Validation, Writing – review & editing. **Seyed Amir-Reza Ahmadi-Mehr:** Supervision, Investigation, Validation, Writing – review & editing. **Reza Lotfi:** Investigation, Validation, Writing – review & editing.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

Data will be made available on request.

## References


[1] F. Celik, A. Akkaya, Y. Leblebici, A 32 Gb/s PAM-16 TX and ADC-based RX AFE with 2-tap embedded analog FFE in 28 nm FDSOI, Microelectron. J. 108 (2021) 104967, http://dx.doi.org/10.1016/j.mejo.2020.104967.

[2] M. Savitha, R.V.S. Reddy, Dual split-three segment capacitor array design based successive approximation ADC for IoT ecosystem, Integration 69 (2019) 279–288, http://dx.doi.org/10.1016/j.vlsi.2019.05.004.

[3] W. Bai, Z. Zhu, A 0.5-V 9.3-ENOB 68-nW 10-kS/s SAR ADC in 0.18-$\mu$m CMOS for biomedical applications, Microelectron. J. 59 (2017) 40–46, http://dx.doi.org/10.1016/j.mejo.2016.11.007.

[4] J. Park, Y. Hwang, D. Jeong, A 0.5-V fully synthesizable SAR ADC for on-chip distributed waveform monitors, IEEE Access 7 (2019) 63686–63697, http://dx.doi.org/10.1109/ACCESS.2019.2915365, URL https://ieeexplore.ieee.org/document/8708173.

[5] F. Maloberti, Data Converters, Springer, Netherlands, 2007.

[6] M. Liu, Low-Power Area-Efficient SAR ADCs with on-Chip Voltage Reference (Ph.D. thesis), Eindhoven University of Technology, 2019, URL https://pure.tue.nl/ws/files/133033750/20190828_Liu.pdf.

[7] Y.H. Chung, C.W. Yen, P.K. Tsai, B.W. Chen, A 12-bit 40-MS/s SAR ADC with a fast-binary-window DAC switching scheme, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 26 (10) (2018) 1989–1998, http://dx.doi.org/10.1109/TVLSI.2018.2849008.

[8] M. Akbari, O. Hashemipour, F. Khateb, F. Moradi, An energy-efficient DAC switching algorithm based on charge recycling method for SAR ADCs, Microelectron. J. 82 (2018) 29–35, http://dx.doi.org/10.1016/j.mejo.2018.10.011.

[9] B. Jajodia, A. Mahanta, S.R. Ahamed, Energy-efficient DAC switching technique for single-ended SAR ADCs, AEU - Int. J. Electron. Commun. 124 (2020) 153334, http://dx.doi.org/10.1016/j.aeue.2020.153334.

[10] P. Nuzzo, C. Nani, C. Armiento, A. Sangiovanni-Vincentelli, J. Craninckx, G. van der Plas, A 6-bit 50-MS/s threshold configuring SAR ADC in 90-nm digital CMOS, IEEE Trans. Circuits Syst. I. Regul. Pap. 59 (1) (2012) 80–92, http://dx.doi.org/10.1109/TCSI.2011.2161368.

[11] K. Nie, Z. Pan, J. Xu, Z. Gao, A low reference voltage interference 10-bit cyclic ADC based on current sub-DAC, Microelectron. J. 125 (2022) 105468, http://dx.doi.org/10.1016/j.mejo.2022.105468.

[12] J. Shen, A. Shikata, A. Liu, B. Chen, F. Chalifoux, A 12-bit 31.1-$\nu$W 1-MS/s SAR ADC with on-chip input-signal-independent calibration achieving 100.4-dB SFDR using 256-fF sampling capacitance, IEEE J. Solid-State Circuits 54 (4) (2019) 937–947, http://dx.doi.org/10.1109/JSSC.2018.2883084.

[13] H. Fan, Y. Liu, Q. Feng, A reliable bubble sorting calibration method for SAR ADC, AEU - Int. J. Electron. Commun. 122 (2020) 153227, http://dx.doi.org/10.1016/j.aeue.2020.153227.

[14] H.-W. Lu, X.-P. Yu, S.-Q. Wang, Y.-Y. Liu, Z.-Y. Huang, Z.-H. Lu, K.-S. Yeo, J.-M. Chen, A digital background calibration scheme for non-linearity of SAR ADC using back-propagation algorithm, Microelectron. J. 114 (2021) 105113, http://dx.doi.org/10.1016/j.mejo.2021.105113.

[15] B. Samadpoor Rikan, D. Lee, K.-Y. Lee, A.6-bit.4. MS/s, VCM-based sub-radix-2 SAR ADC with inverter type comparator, Microelectron. J. 62 (2017) 120–125, http://dx.doi.org/10.1016/j.mejo.2017.02.009.

[16] M. Liu, A.H.M. van Roermund, P. Harpe, A 10-b 20-MS/s SAR ADC with DAC-compensated discrete-time reference driver, IEEE J. Solid-State Circuits 54 (2) (2019) 417–427, http://dx.doi.org/10.1109/JSSC.2018.2873711.

[17] Y. Liang, C. Li, S. Liu, Z. Zhu, A. 14-b, 20-MS/s 78.8dB SNDR energy-efficient SAR ADC with background mismatch calibration and noise-reduction techniques for portable medical ultrasound systems, IEEE Trans. Biomed. Circuits Syst. 16 (2) (2022) 200–210, http://dx.doi.org/10.1109/TBCAS.2022.3147954.

[18] Y. Huang, T. Lee, A 0.02-mm$^2$ 9-bit 50-MS/s cyclic ADC in 90-nm digital CMOS technology, IEEE J. Solid-State Circuits 45 (3) (2010) 610–619, http://dx.doi.org/10.1109/JSSC.2009.2039275.

[19] J. Zhu, J. Xu, K. Nie, A low-power column-parallel cyclic ADC for CMOS image sensor with capacitance and current scaling, Microelectron. J. 105 (2020) 104908, http://dx.doi.org/10.1016/j.mejo.2020.104908.

[20] C.H. Chen, Y. Zhang, J.L. Ceballos, G.C. Temes, Noise-shaping SAR ADC using three capacitors, Electron. Lett. 49 (3) (2013) 182–184, http://dx.doi.org/10.1049/el.2012.4204, URL https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/el.2012.4204.

[21] L. Shi, E. Thiagarajan, R. Singh, E. Hancioglu, U.K. Moon, G.C. Temes, Noise-shaping SAR ADC using a two-capacitor digitally calibrated DAC with 82.6dB SNDR and 90.9dB SFDR, IEEE Trans. Circuits Syst. I. Regul. Pap. 68 (10) (2021) 4001–4012, http://dx.doi.org/10.1109/TCSI.2021.3098471.

[22] M. Hassanpourghadi, M. Zamani, M. Sharifkhani, A low-power low-offset dynamic comparator for analog to digital converters, Microelectron. J. 45 (2) (2014) 256–262, http://dx.doi.org/10.1016/j.mejo.2013.11.012.

[23] P.E. Allen, D.R. Holberg, CMOS Analog Circuit Design, third ed., Oxford University Press, New York, 2012.

[24] B. Nikolic, V.G. Oklobdzija, V. Stojanovic, W. Jia, J.K.-S. Chiu, M.M.-T. Leung, Improved sense-amplifier-based flip-flop: Design and measurements, IEEE J. Solid-State Circuits 35 (6) (2000) 876–884, http://dx.doi.org/10.1109/4.845191.

[25] C. Huang, J. Lin, Y. Shyu, S. Chang, A systematic design methodology of asynchronous SAR ADCs, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 24 (5) (2016) 1835–1848, http://dx.doi.org/10.1109/TVLSI.2015.2494063.

[26] Y. Liang, R. Ding, Z. Zhu, A 9.1 ENOB 200 MS/s asynchronous SAR ADC with hybrid single-ended/differential dac in 55-nm CMOS for image sensing signals, IEEE Sens. J. 18 (17) (2018) 7130–7140, http://dx.doi.org/10.1109/JSEN.2018.2856103.

[27] V. Agarwal, ADC accuracy part 2: Total unadjusted error explained, 2014, URL https://e2e.ti.com/blogs_/archives/b/precisionhub/posts/adc-accuracy-part-2-total-unadjusted-error-explained.

[28] Q. Zhang, N. Ning, J. Li, Q. Yu, K. Wu, Z. Zhang, A second-order noise-shaping SAR ADC using two passive integrators separated by the comparator, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 29 (1) (2021) 227–231, http://dx.doi.org/10.1109/TVLSI.2020.3033415.

[29] Q. Zhang, J. Li, N. Ning, Q. Yu, K. Wu, Z. Zhang, A second-order noise-shaping SAR ADC with error-feedback structure and data weighted averaging, Microelectron. J. 105 (2020) 104905, http://dx.doi.org/10.1016/j.mejo.2020.104905.

[30] A. Kaur, D. Mishra, M. Sarkar, A. 12-bit, 2.5-Bit/phase column-parallel cyclic ADC, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 27 (1) (2019) 248–252, http://dx.doi.org/10.1109/TVLSI.2018.2871341.

[31] R. Ma, L. Wang, D. Li, R. Ding, Z. Zhu, A 10-bit 100-MS/s 5.23-mW SAR ADC in 0.18-$\nu$m CMOS, Microelectron. J. 78 (2018) 63–72, http://dx.doi.org/10.1016/j.mejo.2018.06.007.

[32] B. Samadpoor Rikan, H. Abbasizadeh, Y.-J. Park, H.-Y. Kang, S. Kim, Y. Pu, M. Lee, K.C. Hwang, Y. Yang, K.-Y. Lee, A 10-bit 1 MS/s segmented dual-sampling SAR ADC with reduced switching energy, Microelectron. J. 70 (2017) 89–96, http://dx.doi.org/10.1016/j.mejo.2017.11.005.

[33] B.E. Jonsson, Using figures-of-merit to evaluate measured a/d-converter performance, in: Proceedings of 2011 IMEKO IWADC and IEEE ADC Forum, Orvieto, Italy, 2011, pp. 248–253, URL https://www.imeko.org/publications/iwadc-2011/IMEKO-IWADC-2011-43.pdf.