An Area- and Energy-Efficient Ultrasonic Pulser Based on Self-timed Stepwise Charging

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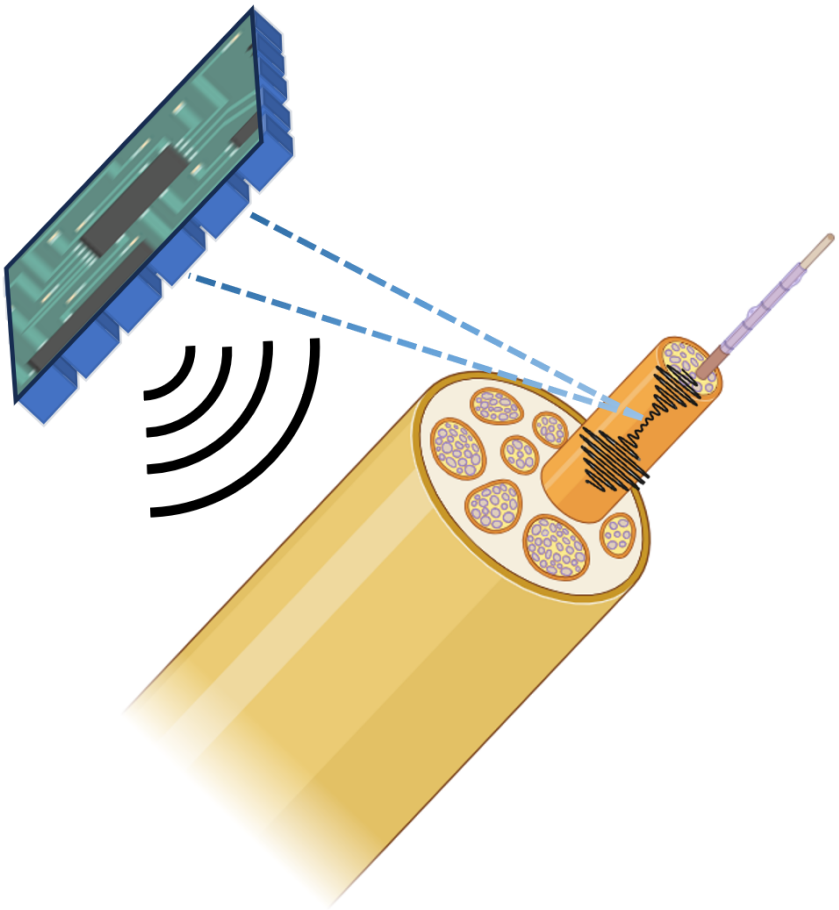

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An Area- and Energy-Efficient Ultrasonic Pulser Based on Self-timed Stepwise Charging

by

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This thesis is confidential and cannot be made public until October 31, 2025.

TU Delft imec

Preface

The past year has been the most thrilling rollercoaster ride in my life. Got COVID at the end of this three-year-long raging pandemic, followed by an unexpected attack from two kidney stones that sent me into the emergency for the first time in my life. Schoolwork took a backseat for a solid four months, and hospital visits became a weekly routine. Then everything was put back together. I met my incredible supervisor, joined a world-leading company, met a fantastic mentor team, and got the opportunity to dig into a whole new system design. Fortunately enough, I can now reflect and conclude my master's journey.

"ASIC design is not a goal, it is a way." During my bachelor's internship and many other projects, I've always been told the "goal" is to design circuits that meet the specs, but without knowing and thinking about where these specs come from. The most profound growth during this two-year journey was developed every time I met with Professor Wouter A. Serdijn. It's always been a joy to travel from Eindhoven to Delft to have meetings in the EWI building. I used to write drafts before meeting with Wouter to help me go through things quickly since I thought he was too busy to spend time with me. I really appreciate this extraordinary person for spending extra time during every campus meeting and joining the company's meeting during lunchtime from the school side, sharing his experience in circuit and system design, criticizing my academic view, and helping me patiently when I was stuck at the midway.

The time spent with imec at Holst Centre has been rewarding and meaningful. The foremost appreciation goes to an ultrasound expert, Dr. Meiyi Zhou, for helping me from the system-level simulation down to the simplest mismatch transistor setup and for coaching me to perform good analog design. The initiators of this project are Dr. Yao-Hong Liu and Dr. Fabian Beutel, and I want to thank them and Meiyi for patiently sharing with me and guiding me to a higher level of system-oriented thinking. I would also like to thank Ph.D. candidate Marios Gourdouparis for sharing his design experiences. All those technical discussions we had were stimulating. Thanks to the R&D manager, Dr. Mario Konijnenburg, for allowing me to join the team and being so kind to share career advice with me. I also thank Dr. John Morales Tellez for letting me experience a brain stimulation experiment and sharing his interesting stories. The student corner is a good place to work. Thank Cina, Shenqi, Pietro, and Heqi for those great talks.

The time in Delft will always be missed. The greatest gifts were from those incredible lecturers in the Department of Microelectronics, especially Professor Fabio, Klaas, Michiel, Qinwen, Marcel, Dante, Wouter, Leo, Masoud, and Henk. Their expertise spanned the realms of analog, digital, RF, and semiconductor fabrication, weaving a rich tapestry of knowledge that has become an enduring part of my academic journey. Special thanks to an excellent tennis player and mentor, Dr. Chang Gao, for playing tennis with me and introducing me to the world of hardware-software co-design. Appreciation goes to Dr. Michiel Pertijs for being a wonderful lecturer and serving as one of my graduation committee members. Thanks to those friends I met in Delft, especially those who played tennis with me day and night.

I thank my parents and cousin for their dedicated love and unconditional support during my time in the Netherlands.

Yuan Lei
Delft, October 2023

Abstract

Acoustoelectric imaging is an emerging technology confirmed by in-vivo experiments that can help diagnose and evaluate peripheral nerve neuropathy. The ultrasound transmitter (TX) is required in such systems to selectively focus and apply acoustic pressure on the target volume. Within the ultrasound TX, the power amplifier (PA, commonly called pulser) can dominate up to 99% of total TX power consumption. In this case, the pulser must be power-efficient and integrated with modern complementary metal-oxide semiconductor (CMOS) compatible transducers to enable miniaturized AE imaging systems. However, the small form factor is the natural limit for high-energy-efficiency pulser design.

The class-D switched-mode PA is the most common approach to drive ultrasonic transducers in recent research publications and commercialized products (e.g., TUSS 4470 by Texas Instruments™, STHVUP32 by STMicroelectronics™). Although the class-D PA manifests inherently simple and area-efficient features, it suffers from power loss on switching the plate parasitic capacitor C_p of the transducer. Prior arts use excessive off-chip capacitors, inductors, and high-frequency switch-clocking signals generated by frequency synthesizers to switch the PA in different configurations to save power on C_p. However, these approaches increase the system form factor and introduce high-speed clock routing. Additionally, efforts to flip and short both terminals of the transducer for increased PA efficiency are not practical for CMOS-compatible transducer arrays. The trade-offs involved in optimizing switched-mode pulser efficiency extend beyond a simple consideration of C_p.

This work proposes a new baseline power-efficiency analysis that comprehensively explains the switched-mode PA efficiency considering transducer characteristics. A switched-mode pulser based on the stepwise-charging technique, controlled by a stepwise sequencer based on a symmetrically-modulated delay cell, is implemented in 130 nm technology. The proposed architecture achieves an overall acoustic efficiency of 82.5% in simulation while maintaining an average efficiency of 81% in global PVT and mismatch corners. The PA achieves a 9.9% acoustic-efficiency improvement compared to its baseline and significantly outperforms the work with a similar baseline by 6.9%. The achieved efficiency is also comparable to the work featuring a 9.1% higher baseline, while this work demonstrates a 20x saving in capacitance budget. The PA signal chain is estimated to have an area of 108 μm x 520 μm, which can be fit into a 115μm-pitch 1-D transducer channel without extra reference resources, offering promising prospects for compact multi-channel integrations.

Keywords— Acoustoelectric imaging, ultrasound transmitter, power amplifier, stepwise charging, self-timed circuit.

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Acronyms

1-D one-dimensional

3-D three-dimensional

AE acoustoelectric

AEI acoustoelectric interaction

ASIC application-specific integrated circuit

BPF bandpass filter

BVD Butterworth-Van Dyke

CMOS complementary metal-oxide semiconductor

CMUTs capacitive micromachined ultrasonic transducers

CP charge-pump

IC integrated circuit

LS level shifter

MC Monte Carlo

PA power amplifier

pMUTs piezoelectric micromachined ultrasonic transducers

PVT Process-Voltage-Temperature

PZT lead zirconate titanate

RLC resistor-inductor-capacitor

RMS root-mean-square

RX receiver

SC switched-capacitor

SNR signal-to-noise ratio

TX transmitter

1 Introduction

Peripheral nerves are crucial in transmitting signals between the brain, the spinal cord, and the rest of the body. These nerves control voluntary movements, convey sensory information, and regulate vital bodily functions. Consequently, any damage or impairment to these delicate neural pathways can result in a wide range of debilitating conditions, from chronic pain and motor dysfunction to loss of sensation and muscle weakness. The overall prevalence of peripheral neuropathy is 2.4%; however, it increases to 8% in individuals above 55 years old [1].

Diagnosing and evaluating peripheral nerve neuropathy posed significant challenges. Traditional clinical diagnosing relied heavily on subjective assessment from clinicians, often leading to delayed or misdiagnosed conditions. The advent of imaging techniques for peripheral nerve systems (e.g., magnetic resonance imaging [2], high-resolution ultrasound [3]) offers healthcare professionals a highly accurate means of visualizing these intricate nerve networks in real-time. Among these imaging techniques, acoustoelectric (AE) imaging is an emerging technology confirmed by in-vivo experiments [4, 5] for nerve systems to provide sub-millimeter resolution of current flow mapping.

The application-specific integrated circuit (ASIC) serves as a promising means to minimize the system form factor. This thesis explores the ASIC specifications for the transmit channel in AE imaging applications and aims to design a miniaturized and highly power-efficient ultrasound power amplifier (PA, commonly referred to as a pulser in ultrasonic applications) suitable for future biomedical implants.

This chapter serves as an introduction to this adventure. The basic principle and the measurement setup of AE imaging prototypes are introduced at the beginning. Following this, the conceptual application for this thesis is presented. Essential specifications for the system are summarized together with state-of-the-art high-efficiency PA circuit design methodologies. Based on these, the research questions of this work are proposed. The final section presents the structure of this thesis.

1.1. Acoustoelectric Imaging

1.1.1. Theory

The acoustoelectric effect was initially predicted by Debye [6] in 1933 and then observed and reported by Fox [7] in 1946, revealing that the electrical conductivity of

saline solutions can be modulated periodically by focused ultrasound waves. Over the ensuing decade, scientists have strived to quantitatively measure the AE effect in different solutions [8, 9] as well as within living tissues [5]. The analysis and modeling for such phenomena are intensively researched to understand the strict mechanism behind this effect [10–14].

The general principle of the AE effect is depicted in Fig. 1.1(a). When a focused ultrasound wave is applied to a volume Ω of biological tissue, a change in pressure ΔP is induced at the focal area. This pressure fluctuation subsequently alters the focal region's electrical conductivity σ. If a current with density J conducts through the volume, a voltage difference, also known as acoustoelectric interaction (AEI) voltage V_{AEI}, can be measured at the volume boundary.

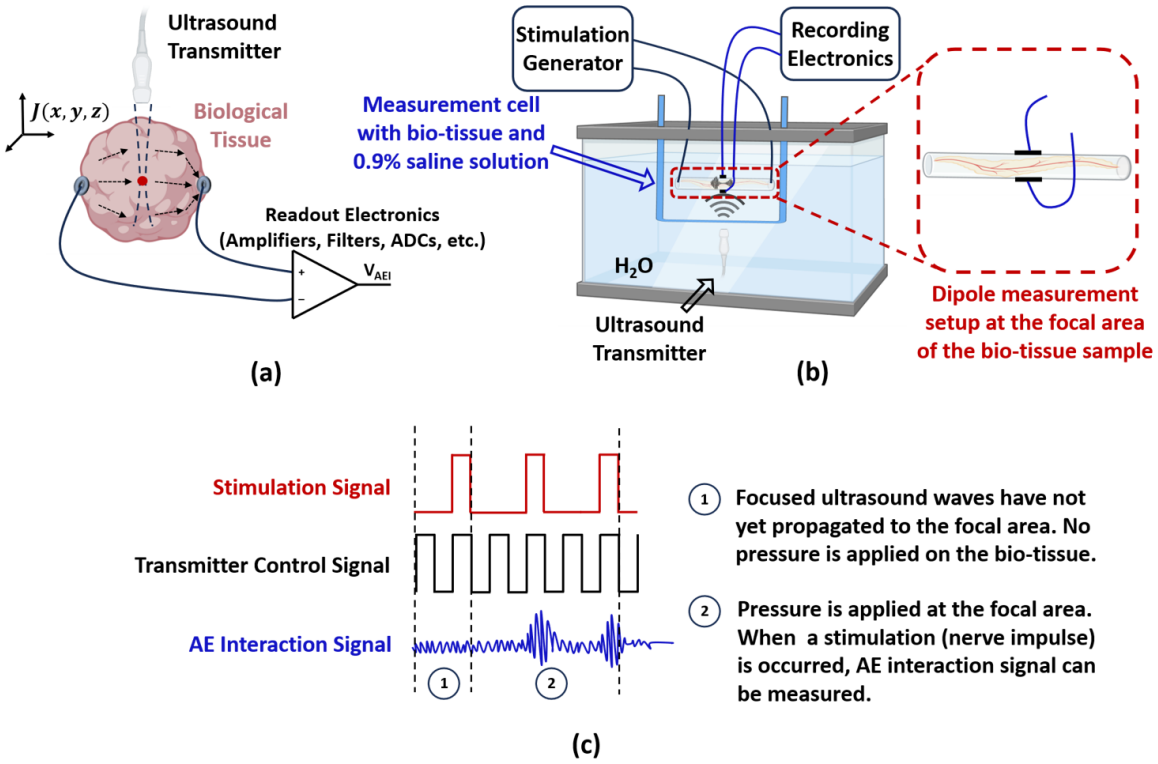


Figure 1.1: Generalized principle and measurement setup of acoustoelectric imaging in [8, 9, 15], (a) a conceptual diagram of AE imaging for bio-current mapping with implanted electrode pair forming a dipole (or so-called lead), (b) side view of the measurement setup, (c) the timing diagram illustrates a set of motion-mode AE scans.

Sub-diagram (a) shows the concept of acoustoelectric imaging. An implantable ultrasound transmitter (TX) is positioned close to the imaging area. It emits acoustic pulses to perform scanning with a three-dimensional (3-D) pattern. The tissue current can be captured with depth and time information by adjusting the focal position (x, y, z) and sampling the boundary potential variation via electrodes. The readout channel would acquire a voltage V_{AEI} and then send it to the post-processing system. Sub-diagram (b) depicts the side view of the AE measurement setup. A single-element transducer is placed deep inside a water tank. A measurement cell filled with 0.9% saline solution is merged into the water tank on top of the transducer. A biomedical tissue sample held by a flexible tube is positioned within the measurement cell. The

stimulation and recording electronics are connected to the sample in a dipole configuration and operate simultaneously. In the timing diagrams (c), the red waveform represents the stimulus that imitates the behavior of nerve current. When performing a scan, the ultrasound transducer starts pulsing acoustic waves to apply focal pressure at different depths within the measurement cell. The acoustoelectric signal is shown in blue, of which the amplitude indicates the potential variation that electrodes measured in the focal depth.

The precise mechanism of acoustoelectric field generation in electrolytic liquids and biological tissues is still under debate. Several works proposed different mathematical models to demonstrate the phenomena, including but not limited to the acoustic momentum theory [16], the Hitherto model [8, 17], and the Gauss model [18]. Exploring the math of the acoustoelectric effect falls beyond the scope of this thesis, but acknowledging the valuable modeling and measurement results from biomedical scientists is crucial. These insights enable us electrical engineers to build ASIC prototypes.

Two following conclusions can be drawn from published acoustoelectric measurements [8, 9, 19, 20]:

(1) The amplitude of the acoustoelectric interaction signal, V_{AEI}, is directly proportional to the magnitude of the current I injected into the tissue and the level of applied acoustic pressure P:

$$V_{AEI} \propto I, P. \tag{1.1}$$

(2) The acoustoelectric interaction constant, denoted as K in Equation (1.2), is an inherent property of various materials. This constant quantifies the extent to which the resistivity σ changes in response to the local pressure variation ΔP induced by acoustic waves. The conductivity of the medium and the corresponding variation are denoted by σ_0 and $\Delta\sigma$.

$$K = -\frac{\Delta\sigma}{\sigma_0 \Delta P} \tag{1.2}$$

1.1.2. Conceptual System for Peripheral Nerve Recording

The conceptualized system for this work is presented in Fig. 1.2. The application is intended to selectively monitor peripheral nerve activities based on the acoustoelectric effect to serve as a method of prediagnosis or long-term treatment for peripheral nerve disease.

Let's take the sciatic nerve bundle as an illustrative example. This type of nerve bundles the tibial and fibular nerves together in the same connective tissue sheath [21]. The ultrasound phased-array transmitter should be implanted near the peripheral nerve bundle. Once in place, the transmitter emits focused ultrasonic waves towards the target nerve within the bundle. These waves exert pressure on the target volume, leading to local potential variations. By observing and analyzing these variations, the system can glean valuable insights into the physiological responses and characteristics of the targeted nerve.

Measuring the potential variation within the bundle in vivo remains challenging, both biologically and in terms of invasive surgical procedures [22–24]. This thesis will not discuss the design of the receiver (RX) channel for AE imaging systems.

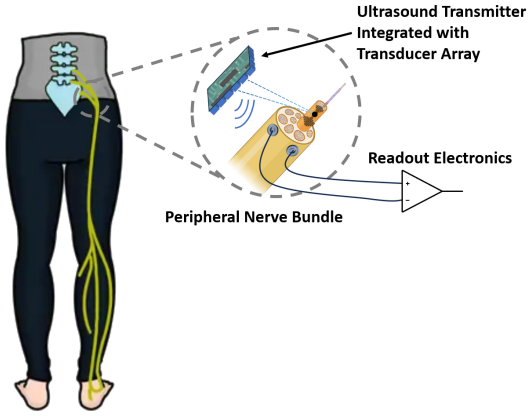


Figure 1.2: Conceptualized system for peripheral nerve recording based on AE effect.

1.1.3. System Specifications

To the best of the author's knowledge, AE-effect-based nerve activity recording systems are still in the prototyping stage. To enable miniaturization for future invasive purposes, aligning the biological measurement results with electrical system specifications is essential. The main system specifications include pressure level, current intensity, heat density, potential variation, and resolution, as can be concluded from available AE prototypes [4, 5, 8, 9].

Pressure Level

The suitable pressure level for acoustoelectric imaging mainly depends on the action potential threshold of the neuron. According to AE theory, neural activities can be recorded only when the ultrasound waves are precisely focused and exert a certain pressure upon the nerve tissue. The applied pressure should remain balanced while avoiding extremes because the nerve would be excited if the ultrasonic-induced potential variation between the cell membrane exceeds the action potential of a neuron (typically around -53 mV as indicated in [25]); conversely, if the amplitude of the AEI signal is too low, readout electronic design can be particularly challenging due to the signal-to-noise ratio (SNR) limit. Owing to the above reasons, unlike ultrasound-powered neural stimulation [26] and medical imaging applications [27], which typically require tunable focal pressure of above 1 MPa to enable fine control of the stimulus intensity or to improve the SNR at the largest imaging depth, acoustoelectric measurements are predominantly performed in hundreds of kPa range [8, 9, 18].

Current Intensity

Measuring the current intensity threshold during the peripheral-nerve excitation period remains challenging, as it highly depends on the nerve type, the contact position, the nerve-to-contact distance, and the sampling rate [28–30]. As listed in Table 1.1, results from publications suggest that the thresholds are within the range of a few milliamperes.

Nerve Type	Current Intensity
Elbow [29]	0.12 - 4 mA
Axillary [29]	0.28 - 5 mA
Brachial Plexus [28]	0.06 - 0.32 mA
Motor Axons [31]	5 - 9 mA
Sciatic [30]	0.3 - 1.9 mA

Table 1.1: Measurement results of action current amplitude for different types of nerves.

Heat Density Limit

Furthermore, the constraints posed by battery size and thermal considerations within biological tissue hold back the upper power dissipation achievable for electronic implants. As examples highlighted in the marketing clearance regulation for ultrasound systems and transducers from the United States Food and Drug Administration [32], the acoustic output exposure level for the spatial-average temporal-average intensity I_{SATA} of the ultrasound transducer face[1] for heart monitoring applications, as expressed by Equation (1.3), where P is the ultrasonic power at the transducer face, D is the area corresponding to entrance beam dimensions, should stay below 20 mW/cm^2. In the absence of sufficient empirical data, this value is adopted as an established guideline for invasive AE imaging systems.

$$I_{SATA} = \frac{P}{D} \tag{1.3}$$

Acoustoelectric Interaction Signal Amplitude

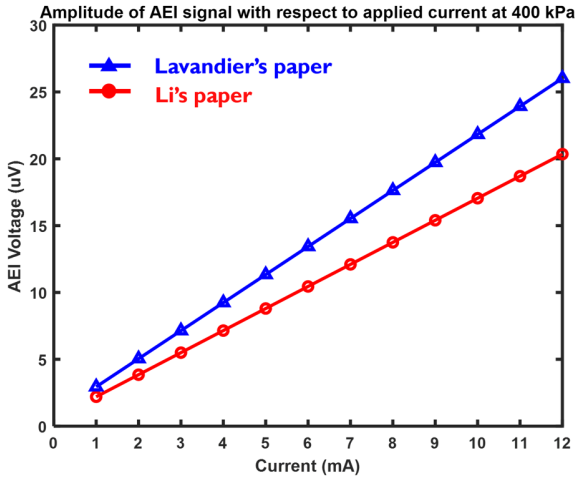


Figure 1.3: A plot of fitted acoustoelectric measurement results from Lavandier's [8] and Li's [9] publications with the same biological conditions: 0.9% NaCl solution, 400 kPa of focal pressure, injected current in mA range. The original voltage scale in Li's paper is in peak-to-peak format with a current range from 0 mA to 5 mA. The author fitted the diagram with the same 3.3 mΩ slope stated in the original article, plotted the corresponding voltage amplitude, and extended the current range to 12 mA for better comparison with Lavandier's result.

[1] It is not explained what the 'transducer face' is in the original regulation file.

The acoustoelectric interaction signal is the directly measurable electrical signal of the system. The amplitude of the AEI signal is proportional to the potential variation of the focal volume. Fig. 1.3 shows the fitted result from two similar measurement setups [8, 9]. The measurements are performed in 0.9% saline solution to emulate the biological environment. In both cases, currents are injected externally into the measurement cell with 400 kPa of ultrasonic focal pressure. The measured AE interaction voltage amplitudes closely align with a current sweeping from 1 mA to 12 mA. Since the AEI signal's amplitude is proportional to the applied pressure, a voltage range from noise floor up to around 50 μV can be estimated with a pressure below 1 MPa.

Focal Resolution
Regarding focal resolution, it is observed from the samples that the diameter of most fibers within the human peripheral nerve bundle is larger than 200 μm [33]. This suggests that the resolution of focal pressure should be around or below 200 μm to ensure that sufficient pressure can be applied to most of the fibers.

To conclude, the general system specifications for implantable acoustoelectric imaging prototypes are shown in Table 1.2.

Target Area	Nerve bundle with 4mm diameter
Focal Pressure Limit	< 1 MPa
Range of Current Density	0.12 - 9 mA
Range of AEI Signal Amplitude	< 50 μV
Heat Flux Density Limit	20 mW/cm^2
Focal Resolution	< 200 μm

Table 1.2: General system specifications for implantable acoustoelectric imaging prototype.

1.2. Ultrasound Transmitter

The integration of ultrasound transducers with ASICs based on complementary metal-oxide semiconductor (CMOS) technology has emerged as a significant breakthrough over conventional FPGA-based systems with discrete transducers [34]. This integration reduces components' wiring and routing, enhances energy efficiency, and shrinks overall form factors, enabling smart and portable ultrasound systems. One critical component in AE imaging systems is the ultrasound transmitter, which is responsible for producing the required pressure in the target area. This section introduces the typical signal chain of the ultrasound transmitter. A review of high-efficiency pulser design is briefed to raise research questions.

1.2.1. Typical Transmitter Signal Chain

A representative ultrasound transmitter architecture for phased-array systems is shown in Fig. 1.4. During the transmitting phase, the ultrasound transducer is driven by a power amplifier, converting electrical signals into acoustic pulses. This process is controlled by a beamforming controller (or so-called beamformer), which provides digitized delay patterns for pulsers in different channels to ensure that the emitted ultrasound waves can be properly focused on the target spatial position.

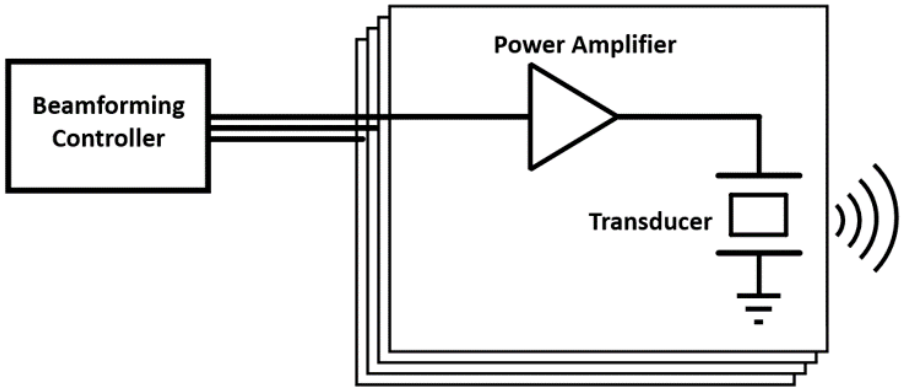


Figure 1.4: Typical ultrasound transmitter array architecture.

1.2.2. High-Efficiency Pulser State-of-the-Art

The ultrasound power amplifier (PA), or so-called pulser, is the core block in the transmit channel. Depending on applications, prior works on ultrasound ASIC design suggest that the TX can be up to 10x more power-hungry than the RX channel [27]. Within the TX channel, the consumed power on the pulser itself can dominate up to 99% of the total TX power [35]. High energy efficiency is the biggest challenge in making such a power-consuming block suitable for biomedical implants, which require compact integration and often have limited or no access to batteries.

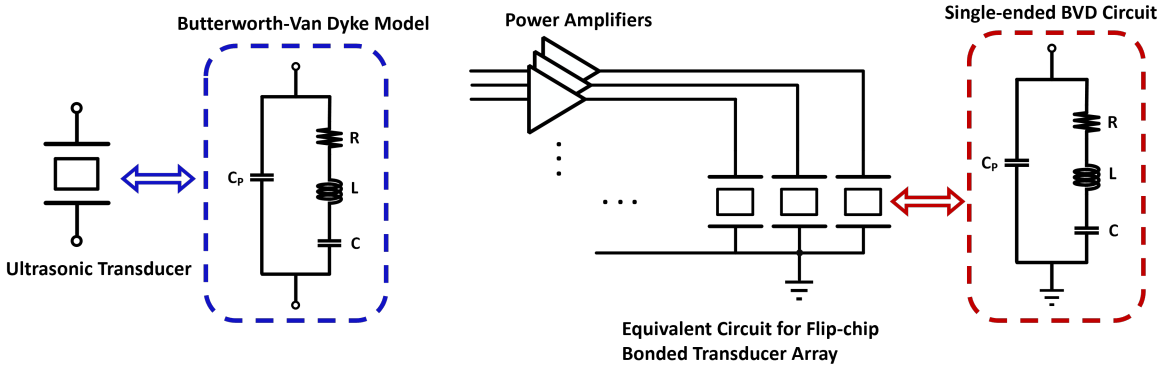


Figure 1.5: Butterworth-Van Dyke equivalent circuits for ultrasound transducer (resonator) and flip-chip bonded transducer array.

The transducer, which provides the load for ultrasonic pulsers and is by nature a resonator, is commonly modeled using the Butterworth-Van Dyke (BVD) model first published in 1928 [36]. The increased precision in characterizing the BVD model [37] over the past century, as well as the simplicity of the model itself, have contributed significantly to the model's prevalence in contemporary circuit design practices. Other models, such as the Krimholtz-Leedom-Matthaei [38] model and Mason's model [39], provide a more precise way to separate the behavior of the electrical, mechanical, and acoustic domains. However, these models can be challenging to characterize [40] and can be overly complex for circuit design.

Two methods are commonly used to drive a transducer/resonator: negative-resistance

circuits and amplifiers. In clock reference applications, the resonator is driven by active $-g_m$ circuits to provide reference signals with clean spectra and high rail-to-rail swing. However, this approach suffers from slow start-up and redundant energy loss during the starting period. The starting procedure usually takes hundreds of oscillation cycles [41] and up to 7360 cycles, as reported in [42]. On the contrary, a spectral-clean reference is out of interest for ultrasonic transducers, but a fast response is necessary to excite duty-cycled acoustic bursts. Linear amplifiers, such as class-A, class-B, and class-AB amplifiers, can provide excellent linearity and low harmonic distortion. However, the efficiency of linear amplifiers is generally low.

Due to the above reasons, the most common approach to drive ultrasonic transducers in recent research publications and commercialized products (e.g., TUSS4470 by Texas Instruments™ [43], STHVUP32 by STMicroelectronics™ [44]) is the switched-mode power amplifier, especially the class-D PA [45]. The idea of switched-mode PA is to generate a fast-switching squarewave signal with a frequency equal to the transducer's series resonance frequency f_s at the PA output node. In this case, the transducer can be operated at its intrinsic mechanical oscillation.

Although the class-D PA manifests inherently simple and area-efficient features, it still suffers from drastic switching power loss P_{SW} during charging and discharging the plate parasitic capacitor C_p of the transducer. As a result, the reported class-D mode pulser efficiency, defined as the ratio between the power delivered to the resistive load of the BVD model and the total power consumption, is usually very low, typically around 50%, as stated in [46].

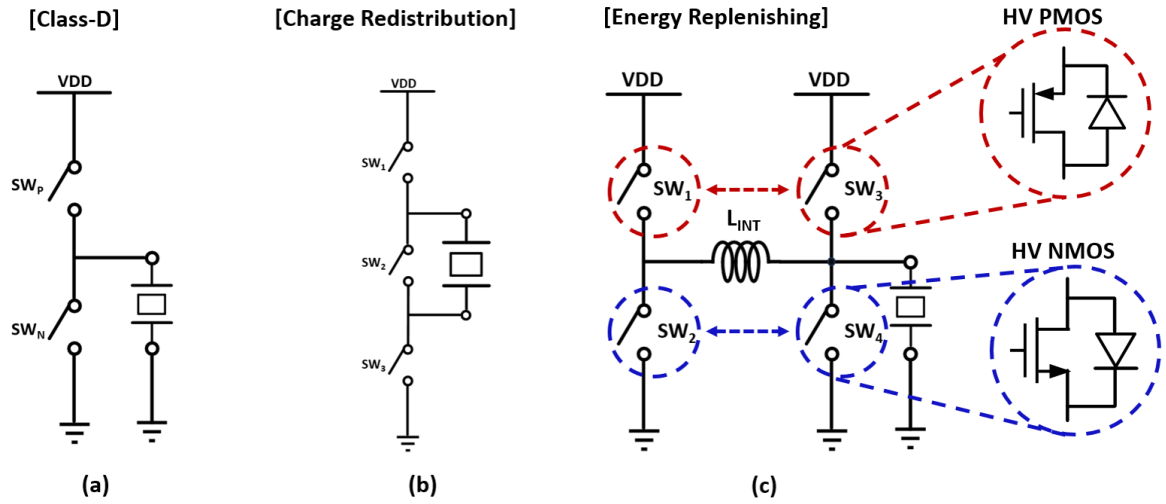


Figure 1.6: Ultrasonic switched-mode pulser architectures, (a) class-D PA, (b) charge-redistribution PA, (c) energy-replenishing PA.

Several techniques have been proposed to reduce the switching loss in ultrasound pulsers. The charge-redistribution pulser is proposed in [47, 48]. The loss on C_p is saved by shortening the two electrodes of the transducer during the off phase of the class-D driver. This helps balance the charge within the transducer so that the potential on both plates returns to the common mode. In this case, the potential difference ΔV between the plates becomes zero, forcing the piezoelectric layer to its initial state (no relaxation). This approach would ideally achieve 50% $C_p V_{DD} f_s$ loss saving

on the plate capacitance. However, it introduces inevitable challenges to integrated transducer fabrication and signal routing, since the CMOS-compatible flip-chip bonding solution for piezoelectric thin film transducer [49, 50] ties the top electrodes of all transducer channels together as a global ground, which means all channels need to be switched at the same time, increasing the difficulty for precise timing control for beamforming. In addition, routing the electrodes from the top plate would require long wiring and affect the design of the transducer matching layer. Efforts have been made in [51] to customize the transducer fabrication process, introducing two electrodes within each array channel. However, this is at the cost of significantly decreasing the quality of the piezoelectric membrane. Hence, this technique is not suitable for high-efficiency CMOS-transducer integration.

To achieve above 50% of switching loss saving, a two-stage energy-replenishing pulser [52] is proposed, which ideally would save all power loss on C_p and, as reported, achieved 73.1% of loss reduction. However, this approach requires a high-quality inductor in every PA channel to preserve the energy loss on C_p, and it must incorporate the body diodes of high-voltage (HV) transistors. Therefore, the energy-replenishing pulser is unsuitable for low-power implantable applications in which system miniaturization is highly prioritized.

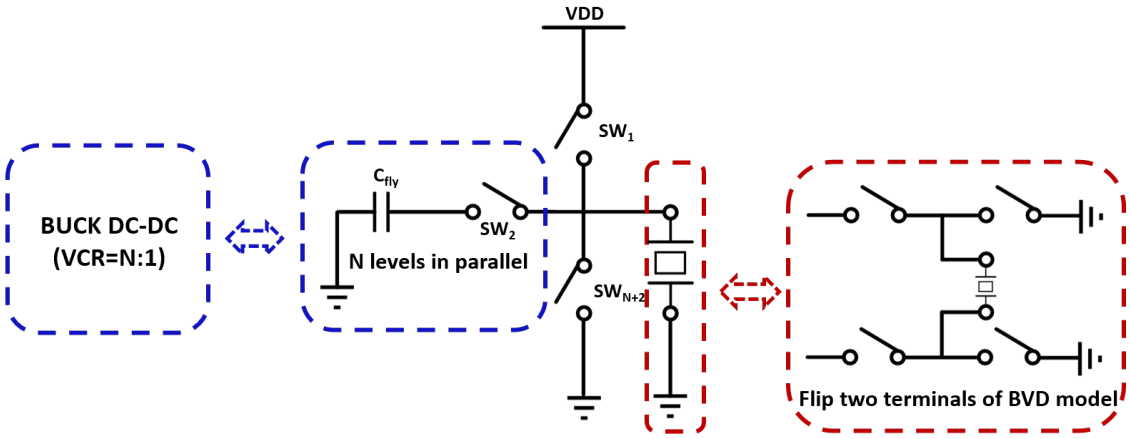


Figure 1.7: Stepwise pulser and its variants. The parallel capacitors can be replaced by BUCK DC-DC converters with different voltage conversion ratios (VCR) [53] at the cost of a larger system form factor. The output can also be differential to boost the output power by flipping two terminals of the BVD circuit.

Another way to save most switching loss is through so-called stepwise charging. Since it was first proposed in 1994 [54], stepwise charging has drawn extensive research interest in different applications. The idea is to extract the charge on C_p with N levels of flying capacitors and recharge the C_p using the charge preserved on these capacitors. Once this process reaches the steady state, the voltage levels on the capacitors are roughly equal [55]. In this pattern, the power loss on the capacitor can be ideally reduced to $\frac{1}{N}CV^2f$ [54]. This approach was widely used in different applications as long as the load is a pure capacitor, for example, capacitive readouts [56], clock drivers [57], DC-DC converters [58, 59], memory circuits [60], screen driver [61], high-speed IOs [62]. These works can achieve significant energy savings using multiple capacitor levels with a very large flying-capacitor-to-load-capacitor ratio (Φ_{CAP}, cap ratio) of up to 2.5×10^6 in [56]. However, excessive capacitors are area-consuming

and, thus, not well-suited for system miniaturization.

Stepwise charging an ultrasound transducer was initially introduced in [53] by implementing a switched-capacitor (SC) BUCK DC-DC converter with off-chip capacitor tanks, which leads to a large form factor with extra clocking resources. To address this issue, follow-up works tried to implement charge sharing across different PA channels, but still, a large cap ratio is needed [63]. Besides, this work only characterized their pulser with a pure capacitive load, and no consideration for either stepwise rising/falling time or the characteristics of the resonating branch are investigated. In [64], the internal levels of stepwise circuits are implemented by cascaded charge pumps, boosting the maximum output swing to N times supply voltage by using N charge pumps, leading to the highest acoustic efficiency of 81.7% (performed in simulation) in the reported literature. Nevertheless, massive sub-drivers are used to protect the cascaded cells from high-voltage breakdown, and nF-level external capacitors are used to provide enough energy for high-swing resonance. Additionally, three transducers with different quality and electrical characteristics are used in this design to randomly search for the maximum efficiency and C_p loss saving point without reasoning. In [46], it reported an acoustic efficiency of 75.6% in simulation by implementing a differential stepwise charging structure similar to [56], which doubled the output swing leading to ideally quadrupled output power on the resistive part while only doubling the power loss on C_p. Nonetheless, as previously mentioned, periodically flipping the supply and ground terminals of the transducer can be costly in flip-chip bonding array fabrication.

1.3. Design Challenges and Research Questions

The design challenges of a high-efficiency pulser for acoustoelectric imaging applications are as follows:

- **From a system-design perspective:** While the primary goal of this thesis is not to design a complete transmitting system, it is essential to ensure that the functions and performance of the designed PA signal chain align with the implantable system specifications concluded in the prior sections as much as possible.

- **From a circuit-design perspective:** In the application scenario of this work, the pulser design needs to achieve state-of-the-art energy efficiency while maintaining a minimal form factor, enabling integration of the complete pulsing signal chain with CMOS-compatible transducers. The small form factor is a natural limit for high-energy-efficiency pulser design. To increase the energy efficiency, prior arts use excessive off-chip capacitors, inductors, and high-frequency switch clocking signals generated by frequency synthesizers, which significantly increase the system form factor and high-speed clock routing. These works also tend to flip or short both terminals of the transducer to increase the power efficiency inherently; however, they are not practical for CMOS-compatible transducers.

- **From an analysis perspective:** A more analytical and systematic approach is needed to understand the relationship between high C_p loss saving and acoustic efficiency. The pursuit of extremely high Cp saving is a common goal for

existing efficiency-oriented switched-mode ultrasonic pulser designs. However, no publication analytically testifies that a high C_p saving would lead to a higher acoustic efficiency. Despite the fact that modeling the transducer and measuring the power transferred into the acoustic domain remains challenging, most publications only measure the pulser with pure capacitive loads, while few publications illustrate the motivation for omitting the resonance behavior of the transducer. Some attempts have been made to fabricate different transducers with varying quality to search for the pulser-transducer combination with the highest efficiency. However, no explanation is provided for such a random search.

The objective of this thesis is to investigate the system specifications for invasive acoustoelectric imaging systems. A comprehensive approach, which takes into account the entire system, from system specifications down to individual transistors, is employed to analyze and alleviate the above-mentioned design challenges. The final goal is to develop a high-efficiency ultrasonic PA signal chain that achieves high efficiency and a small form factor without needing off-chip components and complex routing. The area and power consumption of the circuit design should align with the system requirements, facilitating future integration into the overall system and enabling surgical experiments.

1.4. Thesis Outline

This thesis presents the author's journey in conceptualizing and designing a high-efficiency power amplifier for implantable acoustoelectric imaging applications. The article is organized into five chapters, each contributing to a comprehensive understanding of the subject matter.

This opening chapter serves as a concise introduction to the implantable acoustoelectric imaging system concept. It outlines the basic principle and design target for the prospective application. An overview of state-of-the-art pulser designs emphasizing high energy efficiency is presented. The design challenges for the system and circuits are explored.

Chapter 2 focuses on system design for the intended application. Thorough analyses of the switched-mode PA driving a transducer are presented. The acoustic simulation is conducted to serve as a step in estimating detailed ASIC specifications and system performance.

Chapter 3 dives into the circuit-design strategy for the proposed pulser signal chain, including the main PA, level shifter, and self-timed sequencer. Different circuit architectures are systematically investigated, paving the way to the proposed high-efficiency design.

Chapter 4 demonstrates the overall circuit-design results.

Chapter 5 ends this research journey, presenting performance comparisons with state-of-the-art high-efficiency pulser designs. The thesis contribution and future work are discussed in the end.

2

System Analysis

This chapter evaluates the system-level design of the proposed transmitter signal chain for AE imaging applications. The design starts with the analysis and modeling of the ultrasonic transducer. Following this, the energy efficiency baseline for conventional switched-mode PA is proposed to demonstrate the basic constraints of high-efficiency switched-mode PA design. The last section presents the result of acoustic modeling for the application scenario to settle basic TX specifications.

2.1. Transducer Analysis

The initial phase of designing an ultrasound system for specific applications generally starts with the transducer, given its pivotal role within the signal chain. When the transducer acts as the load for the transmit channel, it converts electrical signals into the acoustic domain, and as the receiver channel's input (e.g., in ultrasonic imaging applications), it performs conversion reversely. For invasive AE imaging applications, the transducer is the immediate interface between the human body and the ultrasound transmitter, leading to more complex biological and surgical considerations.

2.1.1. Transducer Types

Rather than relying on bulky clinical transducer probes (e.g., the ClearVue series from Phillips^{TM} Professional Healthcare [65]), CMOS-compatible transducers are preferred for implantable electronics due to their compact size and seamless integration with modern integrated circuit (IC) technology. These transducers are typically categorized based on the materials used for their fabrication, including lead zirconate titanate (PZT) transducers (or so-called ceramic piezo transducers), piezoelectric micromachined ultrasonic transducers (pMUTs), and capacitive micromachined ultrasonic transducers (CMUTs).

CMUTs offer several advantages, including higher acceptance angle, reduced temperature sensitivity, higher RX spectral sensitivity, and wider reception fractional bandwidth over PZT [66]. However, in CMUT ASICs, a large DC bias voltage (typically tens of volts), known as collapse voltage, is typically required for both transmission and reception to ensure that the electrostatic forces between the transducer's membrane and the substrate are strong enough to cause the membrane to collapse and contact

with the substrate. Another inherent limitation arises from the fabrication process: the intrinsic frequency of CMUTs generally cannot go below 1MHz [67], limiting its applications to high-resolution scenarios only. Additionally, the bias electrode is often directly exposed to the patient, thus limiting the system reliability as well as its form factor [68].

To date, pMUTs have gained considerable research interest from both research institutes and companies. This interest grew substantially, especially after Qualcomm^{TM} successfully commercialized the world's first pMUT-based ultrasonic fingerprint sensor in 2018 [69]. Compared to CMUT, pMUT does not require a large DC bias, and it has a higher capacitance and lower electrical impedance. These characteristics enhance the transducer sensitivity, facilitating the integration with low-voltage CMOS technology nodes [70]. However, it comes at the cost of a reduced MUT coupling factor since the piezoelectric material layer of pMUT is deposited with plasma-enhanced chemical vapor deposition, making it suffer more from material degradation issues [67]. Nevertheless, at this stage, pMUT fabrication and electrical modeling remain challenging with concerns including the fragility of the membrane, interconnect fabrication for arrays, and piezoelectric thin-film fabrication [71, 72].

The PZT transducer stands as a well-established and commercialized technology widely employed in conventional ultrasound equipment. However, single-element piezo-ceramic transducers face challenges related to labor-intensive production processes and difficulties in miniaturization [67]. The transducer utilized in this work is a flip-chip-bonded PZT transducer array, as detailed in [73]. This technology enables the PZT transducer to seamlessly integrate with CMOS circuits, addressing some of the miniaturization challenges associated with single-element piezo-ceramic transducers. Fig. 2.1 illustrates the simplified PZT-on-CMOS structure. On top of the silicon ASIC, a metallic interconnection layer is applied to the bond pads. A nonconductive epoxy layer is deposited to bridge the gaps between the metals. Subsequently, the PZT matrix is constructed by connecting the electrodes and the back side of the PZT using a conductive glue layer. For acoustic matching purposes, a conductive matching layer is applied over the piezoelectric layer. The stack is then diced to form a transducer array. Finally, a ground foil is affixed to the matching layer, serving as a common counter electrode for all elements.

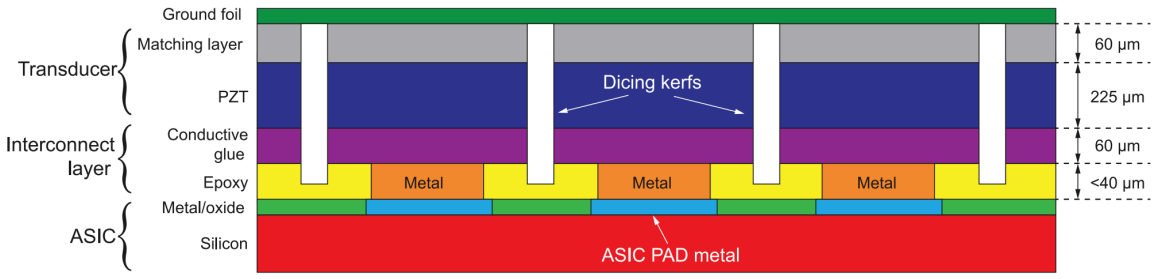


Figure 2.1: Simplified structure scheme of PZT with flip-chip bonding integration [73].

A noteworthy distinction between the off-chip transducer array and the on-chip one is that the ground terminal of the on-chip array cannot be readily interchanged between the power supply and ground, as demonstrated in [35, 46], leading to mal-

function in array beamforming. This is due to the fact that the ground connections of on-chip transducer arrays are intricately linked through a dedicated ground layer [73]. In attempts to address this limitation, modifications to the pMUT fabrication process have been explored, as seen in [35], where two electrodes are introduced between two layers of piezoelectric material inside each channel. This modification enables beamforming with terminal flipping. However, it comes at the cost of a significant reduction in the pMUT quality factor, approximately 30x lower compared to that in [64], as indicated in Table 2.2. This reduction in quality factor could lower the efficiency baseline and potentially complicate the circuit design strategy.

The challenges in designing and fabricating different transducers impose limitations on the considerations for designing an integrated AE imaging system. The intricacies of on-chip transducer arrays, especially regarding ground terminal interchangeability, demand careful circuit design strategies to ensure proper functionality and beamforming capabilities. These challenges underscore the importance of a holistic approach that takes both transducer fabrication and circuit design into account to achieve optimal performance.

2.1.2. Electromechanical Modeling

Modeling the behavior of transducers serves as a foundation for system engineers and IC designers to properly design an integrated system. The mechanical-to-electrical conversion of film bulk acoustic resonators (FBARs) can be accurately characterized by equipment and represented by the lumped Butterworth-Van Dyke (BVD) model in Fig. 2.2(a). This model is adopted in most modern ultrasound ASIC designs [27, 46, 48] thanks to its simplicity and effectiveness. While alternative circuit models like the KLM model [38] and Mason's model [39] exist, which separate the behavior of the electrical, mechanical, and acoustic domains, they can be challenging to characterize and may introduce unnecessary complexity for circuit design [40]. The adoption of the BVD model reflects a pragmatic approach that balances accuracy and simplicity in the context of ultrasonic transducer modeling for integrated circuit design.

The BVD model represents the mechanical resonance of the transducer through a resistor-inductor-capacitor (RLC) branch. Additionally, the electrical parasitics on the transducer plates are modeled by the capacitance term C_p in parallel with the RLC branch. Agilent™ reports that this model can achieve below 3% inaccuracy [37], and a study in [74] indicates an error less than 1% in finite-element-method analysis. This level of accuracy makes the BVD model a reliable choice for capturing the essential characteristics of ultrasonic transducers in circuit simulations.

$$Z_{BVD} = \frac{1}{sC_p} // \left(R + sL + \frac{1}{sC} \right) = \frac{s^2LC + sRC + 1}{s^3LCC_p + s^2RCC_p + s\left(C + C_p\right)} \tag{2.1}$$

Thanks to the author's colleagues, the BVD parameters of the PZT transducer used in this work have been characterized. The transducer is diced to a one-dimensional (1-D) array with 115 μm pitch and 25 μm kerf. The transducer array has a channel length of 920 μm. The BVD circuit acts as a resonator or a bandpass filter (BPF). The impedance seen in the two-terminal network can be calculated in the s-domain by Equation (2.1), and its frequency response is depicted in Fig. 2.2(b).

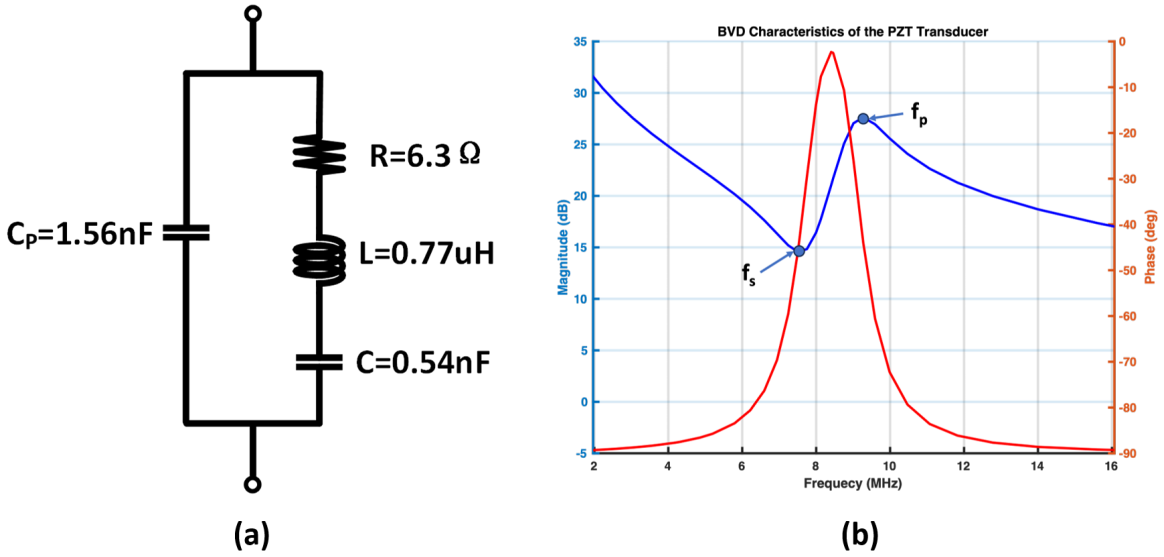


Figure 2.2: The BVD model and its frequency response, (a) lumped BVD circuit model with parameters characterized for 5 mm x 5 mm PZT transducer, (b) frequency response of the BVD model.

The BVD load has two intrinsic resonance frequencies that are inversely proportional to the thickness of piezoelectric material, namely series resonance f_s and parallel resonance frequency f_p, where

$$f_s = \frac{1}{2\pi\sqrt{LC}}, \tag{2.2}$$

$$f_p = \frac{1}{2\pi}\sqrt{\frac{1}{L_s}\left(\frac{1}{C}+\frac{1}{C_p}\right)} = f_s\sqrt{\frac{C+C_p}{C_p}}. \tag{2.3}$$

The intrinsic mechanical frequency of the piezoelectric material is the series resonance f_s, at which the inductance and capacitance on the RLC branch cancel each other so that the branch exhibits a resistive behavior. On the other hand, parallel resonance occurs when the plate parasitic capacitance cancels the impedance of L and C.

Two commonly used methods to drive a resonator are the negative-resistance circuit and the switched-mode power amplifier. The negative-resistance circuits have the advantage of producing reference signals with sufficiently clean spectra across the bandwidth. However, they suffer from extended startup time issues and energy losses during the starting period [41, 75, 76]. The startup time for LC circuits ranges from hundreds to thousands of oscillation periods [41]. On the contrary, in the case of ultrasound transmitter design, the generation of acoustic bursts requires precise duty-cycling and delay control to perform phased-array beamforming with minimal energy loss. Due to these reasons, it's desirable to drive the ultrasonic transducer with a switched-mode PA at the series oscillation frequency f_s to maximize the acoustic power.

Fig. 2.3 shows the simulated plot of the root-mean-square (RMS) current I_{RMS} on the RLC branch versus the class-D mode driving frequency with a fixed 5 V supply.

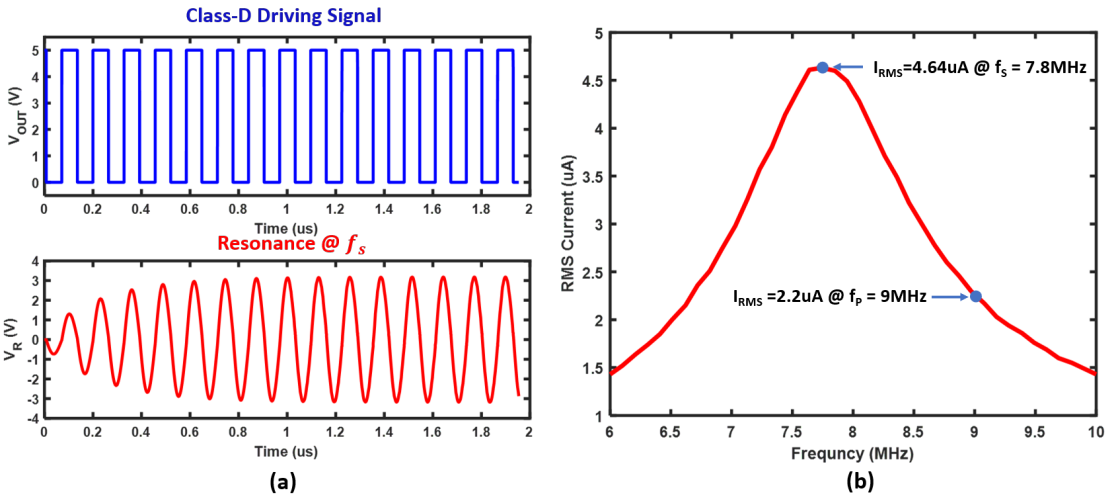


Figure 2.3: Simulated waveforms of a class-D PA driving a transducer. (a) The class-D driving signal with a 5 V swing (in blue) and the resonance waveform across the resistance on the RLC branch at f_s (in red), (b) the RMS current on the RLC branch with different driving frequencies. It is observed that I_{RMS} reaches its maximum when the transducer is being driven at f_s.

The peak RMS current occurs at series oscillation, suggesting that the highest output power is obtained when the transducer is driven at f_s.

To quantify the intrinsic performance of a resonator, quality factor Q and pulling factor P are further introduced. The quality factor [77], which indicates the ratio between the energy stored and dissipated per oscillation cycle, can be expressed as:

$$Q = 2\pi f_s \frac{L}{R} = \frac{1}{2\pi f_s RC}. \tag{2.4}$$

BVD Specifications	5 mm x 5 mm PZT Transducer	115 μm x 920 μm PZT
R	6.3 Ω	2430 Ω
L	0.77 μH	297.5 μH
C	0.54 nF	1.4 pF
C_p	1.56 nF	4.04 pF
f_s	7.8 MHz	7.8 MHz
f_p	9.05 MHz	9.05 MHz
Q	6	6
P	16.04%	16.04%

Table 2.1: Characterized BVD parameters for the flip-chip bonding PZT 5H transducer. The scaled parameters are based on the assumption that dicing would remove the piezoelectric material within the kerf completely, and the dicing procedure would not change the intrinsic properties of the transducer but only decrease the output power of each transducer element.

In order to correlate the behavior of C_p, the pulling factor P was first introduced in a high-performance crystal reference design in 1988 [78]. It describes the relative amount of frequency pulling above the mechanical resonant frequency caused by the plate parasitic C_p. In the context of transducer design, the pulling factor can be adopted

to characterize the capacitive nature of the transducer. This factor can be expressed as a percentage by the formula:

$$P = \frac{f_p - f_s}{f_s} = \sqrt{1 + \frac{C_s}{C_p}} - 1 \approx \frac{C_s}{2C_p}. \tag{2.5}$$

The above-mentioned electrical specifications for the PZT model used in this work are concluded in Table 2.1.

2.1.3. Pulsing Pattern

The desired pulse repetition frequency f_{PR} of acoustic scans in AE imaging applications highly depends on the frequency of the neural impulse, which, as suggested, lies in the range below 500 Hz [79]. Hence, according to the Nyquist sampling criterion, the transducer should produce a sequence of ultrasound bursts with a f_{PR} at least above 1 kHz, ensuring acoustic pressure is applied on nerve tissue when neural impulses are presented.

The desired pulsing pattern can be visualized in Fig. 2.4. The control signal is duty-cycled to have a burst of five consecutive pulses with a repetition frequency larger than 1 kHz. The resulting acoustic output follows the same pattern.

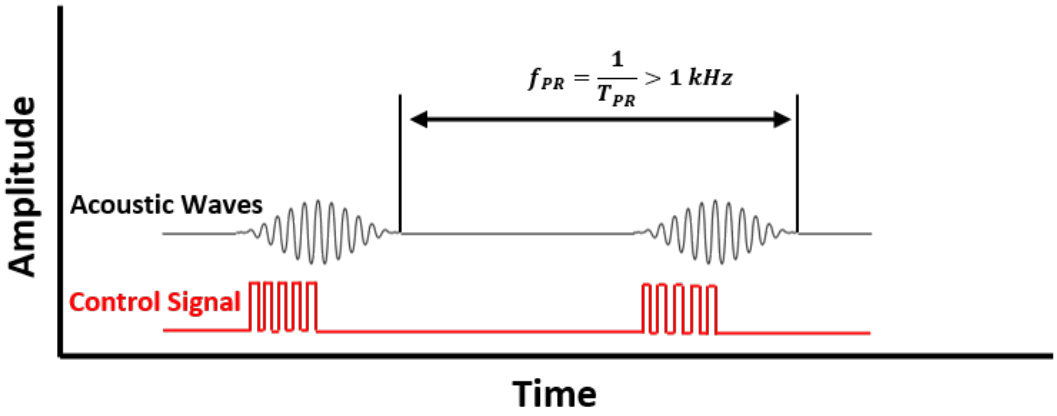


Figure 2.4: Transmit switching control and pulse pattern for AE imaging.

2.2. Transmitter Efficiency

The ultrasound PA is the driver of the transducer and represents the most power-consuming block in the ultrasound transmit chain, dominating up to 99% of the total TX power [35]. The conventional class-D approach wastes a large portion of the energy on charging and discharging the parasitic capacitance of the transducer. This can lead to a low overall TX efficiency.

In the pursuit of higher energy efficiency, it's essential to model and understand the behavior of a switching mode PA driving a BVD load. This section employs a pulser-BVD co-analysis approach to evaluate the efficiency of PA designs with transducer loads.

2.2.1. Definition

The transmitter efficiency is defined as the ratio between the output acoustic power P_A and the total power consumption P_{tot} of the TX. However, measuring the exact acoustic power in ultrasound systems can be challenging due to the medium degradation and hydrophone positioning. Therefore, many studies [46, 64] approximate the acoustic power as the electrical power delivered to the resistive part of the BVD model in circuit simulation. This concept is adopted in this work as well to describe the energy efficiency of the pulser. It's important to note that this approximation does not capture the complete real-world scenario as the resistive component accounts for the resistive behavior of the electrodes, the mechanical resistance of the membrane, and the actual acoustic power generated.

$$\eta_A = \frac{P_A}{P_{tot}} \times 100\% \tag{2.6}$$

In various studies [47, 52, 59, 63, 64], the concept of "C_p loss saving" is adopted to characterize the efficiency of the pulser. As indicated in Equation (2.7), it represents the percentage of power saved in relation to the charge and discharge of the transducer's parasitic capacitor in the case of class-D PA ($C_p V_{DD}^2 f_s$). The concept is under the assumption that the energy loss on C_p is the primary bottleneck for the TX efficiency degradation. The more the C_p loss saving, the higher the total TX efficiency.

$$\eta_{C_p} = \frac{C_p V_{DD}^2 f_s - P_{loss,C_p}}{C_p V_{DD}^2 f_s} \times 100\% \tag{2.7}$$

Attempts are made in prior art [64] to fabricate multiple transducers with varying characteristics. These transducers are driven by the same PA in order to empirically identify the best combinations that would result in the highest efficiency and the greatest C_p loss saving. Interestingly, it is reported that the combination for maximized power efficiency does not necessarily align with the one that achieved the most C_p loss saving. This finding may suggest a more intricate relationship between transducer characteristics and PA efficiency, which is one of the research questions to be addressed in the next chapter.

2.2.2. Efficiency Baseline Derivation

The BVD parameters (R, L, C, C_p) alone can not properly describe the performance of the transducer. Hence, attention needs to be paid to how the transducer's intrinsic performance affects the energy efficiency of the switched-mode power amplifier. To observe this relation, the author proposes to analyze the PA efficiency using a pulser-BVD co-analyze approach. An efficiency baseline for conventional class-D PA driving an ultrasound transducer is introduced. This novel method can serve as a guideline to systematically design and compare a high-efficiency combination of PAs and transducers.

If an ideal class-D driving signal with a frequency of f_s and a peak-to-peak amplitude of V_{DD} is applied to drive the transducer, the driving signal can be expressed by the following Fourier series:

$$V(t) = \sum_{n}^{\infty} v_n(t) = \frac{2V_{DD}}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin(n\omega_s t), n = 1, 3, 5... \tag{2.8}$$

where $v_n(t)$ is the n-th corresponding harmonic of the class-D driving signal.

The power of each harmonic, P_n, can be calculated by integrating the instantaneous power in a complete oscillation period T and then taking the average over time:

$$P_n = \frac{1}{T}\int_0^T \frac{v_n^2}{R} dt = \frac{1}{T}\frac{(2V_{DD})^2}{(n\pi)^2 R}\int_0^T \sin^2(n\omega_s t) dt = \frac{1}{T}\frac{(2V_{DD})^2}{n^2\pi^2 R}\int_0^T \frac{1-\cos(2n\omega_s t)}{2} dt. \tag{2.9}$$

The band-pass resonance branch of the BVD model ideally filters out every harmonic component except the fundamental wave. Assuming zero output impedance of the class-D PA, the transient voltage on the resistive part of the BVD load can be expressed as:

$$V_R(t) = |V_R| \sin(\omega_s t) = \frac{2}{\pi} V_{DD} \sin(\omega_s t). \tag{2.10}$$

Furthermore, the power delivered to the resistive part can be expressed by:

$$P_R = \frac{\left(\frac{|V_R|}{\sqrt{2}}\right)^2}{R} = \frac{\left(\frac{2}{\pi} \times V_{DD}\right)^2}{2R} = \frac{2V_{DD}^2}{\pi^2 R}. \tag{2.11}$$

The power loss during charge and discharge of the plate capacitance of the transducer, denoted as the switching loss P_{SW}, can be expressed as:

$$P_{SW} = C_p V_{DD}^2 f_s. \tag{2.12}$$

Finally, the total power consumption of the class-D PA can be shown by:

$$P_{tot} = P_R + P_{SW} = \frac{\left(\frac{2}{\pi} \times V_{DD}\right)^2}{2R} + C_p V_{DD}^2 f_s = \frac{2V_{DD}^2}{\pi^2 R} + C_p V_{DD}^2 f_s. \tag{2.13}$$

Neglecting the power consumption of any other semiconductor-technology-dependent block (e.g., digital control logic, level shifting, switch driver), the total acoustic efficiency of the class-D PA driving a transducer is:

$$\eta_D = \frac{P_R}{P_{tot}} = \frac{\frac{2V_{DD}^2}{\pi^2 R}}{\frac{2V_{DD}^2}{\pi^2 R} + C_p V_{DD}^2 f_s} \tag{2.14}$$

Expressing the BVD parameters by the quality and pulling factor of the resonator, the factors become as followed:

$$C_p = \frac{C}{(1+P)^2 - 1}, \tag{2.15}$$

$$RCf_s = \frac{1}{2\pi Q}. \tag{2.16}$$

Substituting Equations (2.15) and (2.16) into (2.14), the relation between class-D PA efficiency and the intrinsic properties of the transducer can be concluded by:

$$\eta_D = \frac{\frac{2V_{DD}^2}{\pi^2 R}}{\frac{2V_{DD}^2}{\pi^2 R} + C_p V_{DD}^2 f_s} = \frac{1}{1 + \frac{\pi^2}{2} RC_p f_s} = \frac{1}{1 + \frac{\pi}{4Q[(1+P)^2+1]}}. \tag{2.17}$$

2.2.3. Comparative Study to Prior Works

Three important observations can be found in Equation (2.17). When driving an ultrasound transducer with a switched-mode PA:

(1) **The baseline indicates the best efficiency achievable for a class-D PA driving a transducer with different characteristics**: Once the BVD parameters are accurately characterized with an error below 3% or 1%, as reported in [37] and [74], it becomes possible to derive an efficiency baseline for a conventional switch-mode PA using Equation (2.17). This equation reveals that the maximum achievable acoustic efficiency, without considering silicon-technology-dependent factors, is fixed for a given transducer. A well-designed class-D pulser has the potential to maintain acoustic efficiency close to this baseline. This understanding establishes a benchmark for efficient pulser design.

(2) **High-quality Q (narrowband) and high pulling P (low capacitive) transducers are preferred for high-efficiency design**: In pulser design that prioritizes energy efficiency, it is desirable to have a transducer with a high quality factor Q (narrowband) and a high pulling factor P (low capacitive). It is worth noting that the P factor plays a much more significant role in the overall efficiency compared to the Q factor, as it has a quadratic relation with energy efficiency.

(3) **The co-optimization of the pulser and transducer becomes imperative when integrating a large amount of transmit channels to reduce channel area and routing complexity**: Transducers with a high efficiency baseline are particularly beneficial because they work efficiently with simple class-D PAs. This synergy between efficient transducers and area-efficient PAs can lead to significant die area savings and simplified routing, making it more feasible to implement large-scale ultrasound transceiver systems.

The relation between switched-mode PA efficiency baseline, quality factor Q, and pulling factor P is visualized in Fig. 2.5. In general, a transducer with higher Q and higher P (lower capacitive) can achieve relatively high efficiency.

Transducer models reported in publications have significant differences in BVD parameters as shown in Table 2.2. For example, [51] and [46] use PZTs with similar quality factors; however, the one with 14% higher pulling factor has a baseline almost doubled.

A higher baseline for the transducer indicates that using simple class-D driver can already achieve high efficiency if properly designed. In such cases, further efforts

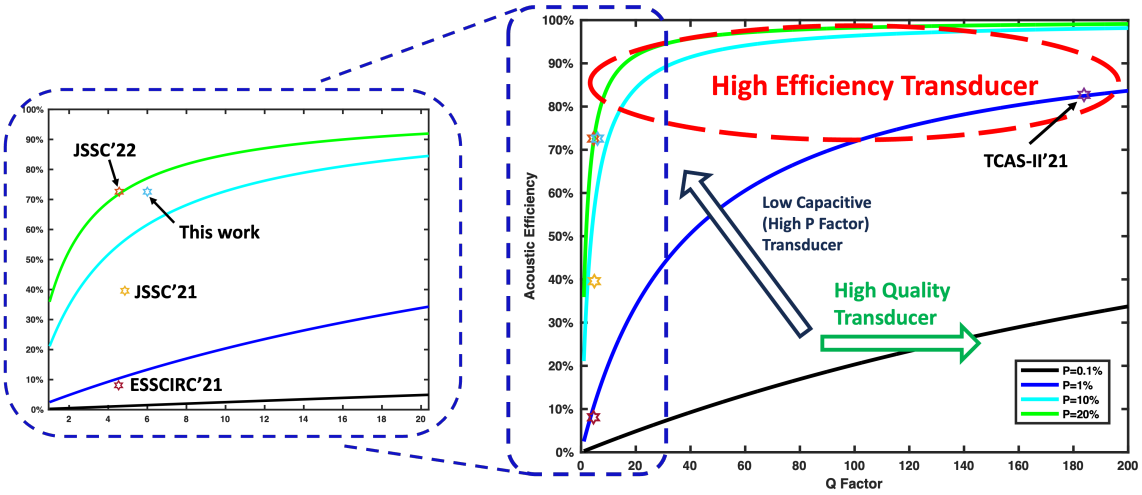


Figure 2.5: Acoustic efficiency for class-D switched-mode PAs with different Q and P factors. Hexagonal stars note calculated baseline efficiency for transducer models in different publications.

	JSSC'22 [46]	TCAS-II'21 [64]	JSSC'21 [51]	ESSCIRC'21 [63]	This work
R	358 Ω	1100 Ω	3870 Ω	410 kΩ	2430Ω
L	333 μH	31.5 mH	0.68 mH	1.69 H	297.5 μH
C	125 pF	0.77 pF	1.93 pF	490 fF	1.4 pF
C_p	278 pF	37.7 pF	15.4 pF	32 pF	4.04 pF
Q	4.56	183.87	4.85	4.53	6
P	20.4%	1.016%	6.08%	0.7%	16.04%
f_s	780 kHz	1.02 MHz	4.39 MHz	175 kHz	7.8 MHz
f_p	939 kHz	1.03 MHz	4.66 MHz	176 kHz	9.05 MHz
Efficiency Baseline	72.3%	82.7%	39.6%	8.1%	72.6%
Achieved Efficiency	[1]75.6%	[1]81.7%	N.A.	N.A.	[1]82.5%
Achieved C_p Saving	N.A	N.A.	[2]42.6%	[2]80%	[1]47.7%

[1] Simulated result.
[2] Measured result.

Table 2.2: Comparison of BVD parameters and efficiency baselines of different transducers in prior arts.

to save more energy loss, such as power loss on C_P, might not be as meaningful and could potentially over-complicate the circuit design without significant efficiency gains. It highlights the importance of striking a balance and tailoring the design strategy based on the inherent characteristics of the transducer.

For the transducer model used in this work, the efficiency baseline is determined to be 72.6%, which is only 0.3% higher than the baseline reported in [46]. In that work, the model had a 72.3% baseline, and the power amplifier achieved a 3.3% improvement relative to their baseline. This suggests that a successful PA design for this work should aim for an efficiency higher than 72.6%.

In fact, the effect of nonidealities plays an important role in switched-mode PA design. However, if the PA and transducer are co-designed properly, nonidealities can be readily mitigated. Details are discussed in the circuit design chapter.

2.3. Acoustic Modeling

Focusing ultrasonic waves and exerting targeted pressure on a specific volume requires the use of phased-array beamforming. To enable this technique, the transducer must be diced into an array with multiple channels, each of which has a precisely controlled driving-signal delay. This section illustrates the acoustic simulation for an AE imaging application targeting a peripheral nerve bundle with a 4-mm diameter. More detailed research on beamforming techniques and acoustic modeling is beyond the scope of this thesis. The primary goal of this part is to investigate fundamental TX specifications for the application, including array size, pressure range, quantization bit, and covered area.

2.3.1. Model Setup

In AE imaging, the function of the transmitter is to induce pressure variations in the peripheral nerve bundle. Fig. 2.6 provides a simplified cross-section view of the nerve bundle. The transmitter should be placed close to the epineurium. The specific target in this application scenario would be a 1-D cross-section area of the nerve bundle. Consequently, the use of a 2-D beamforming control and a 1-D transducer array should satisfy the application purpose.

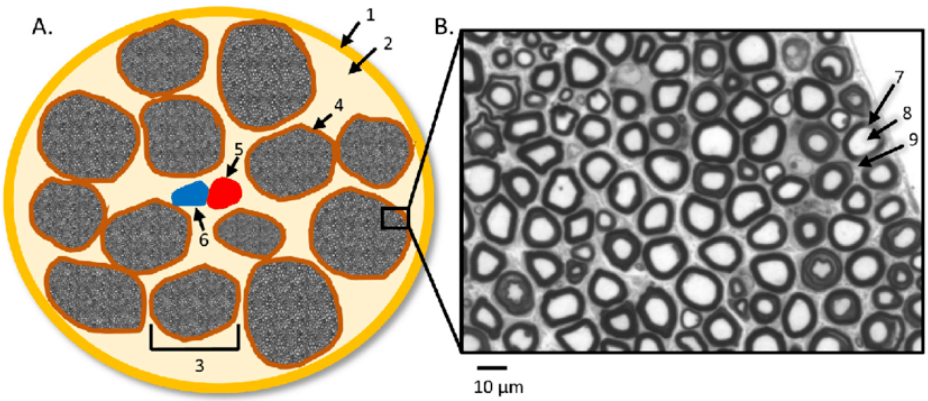


Figure 2.6: Cross-sectional anatomy of a peripheral nerve bundle [80]. Basic structures include (1) epineurium, (2) lipid-equivalent connection tissues, (3) individual nerve fascicle, (4) perineurium, (5) artery, and (6) vein. (B) Representative myelinated nerve fibers under light microscopy from a control sciatic nerve, stained with Toluidine blue: (7) myelin sheath, (8) axon, and (9) endoneurium.

The acoustic modeling is based on k-Wave in MATLAB. The model that the author uses is adopted from examples in [81] and [82], where the code and toolbox already include the functions of grid setup, 1-D-transducer initialization, computation of the full width at half maximum (FWHM) resolution, and computation of the beam pattern.

The author's contribution is modifying the grid and medium properties using data from the ITIS Foundation bio-tissue database [83] as shown in Table 2.3, so that the model can reflect the acoustic behavior within the actual tissue. The author also adds multiple transducers with custom locations to the grid to see how the angle between the transducer would affect the resolution. Lastly, a quantizer has been added to the beamformer to check how the resolution and pressure would change with different quantizer bits.

The k-Wave simulation setup is concluded in Table 2.3. The model employed in this simulation provides a rough estimation. It assumes a homogeneous medium, which implies that no reflection would occur during the propagation of waves. The simulation grid is set to 5 mm × 5 mm, leaving a 1 mm margin to place the transducer.

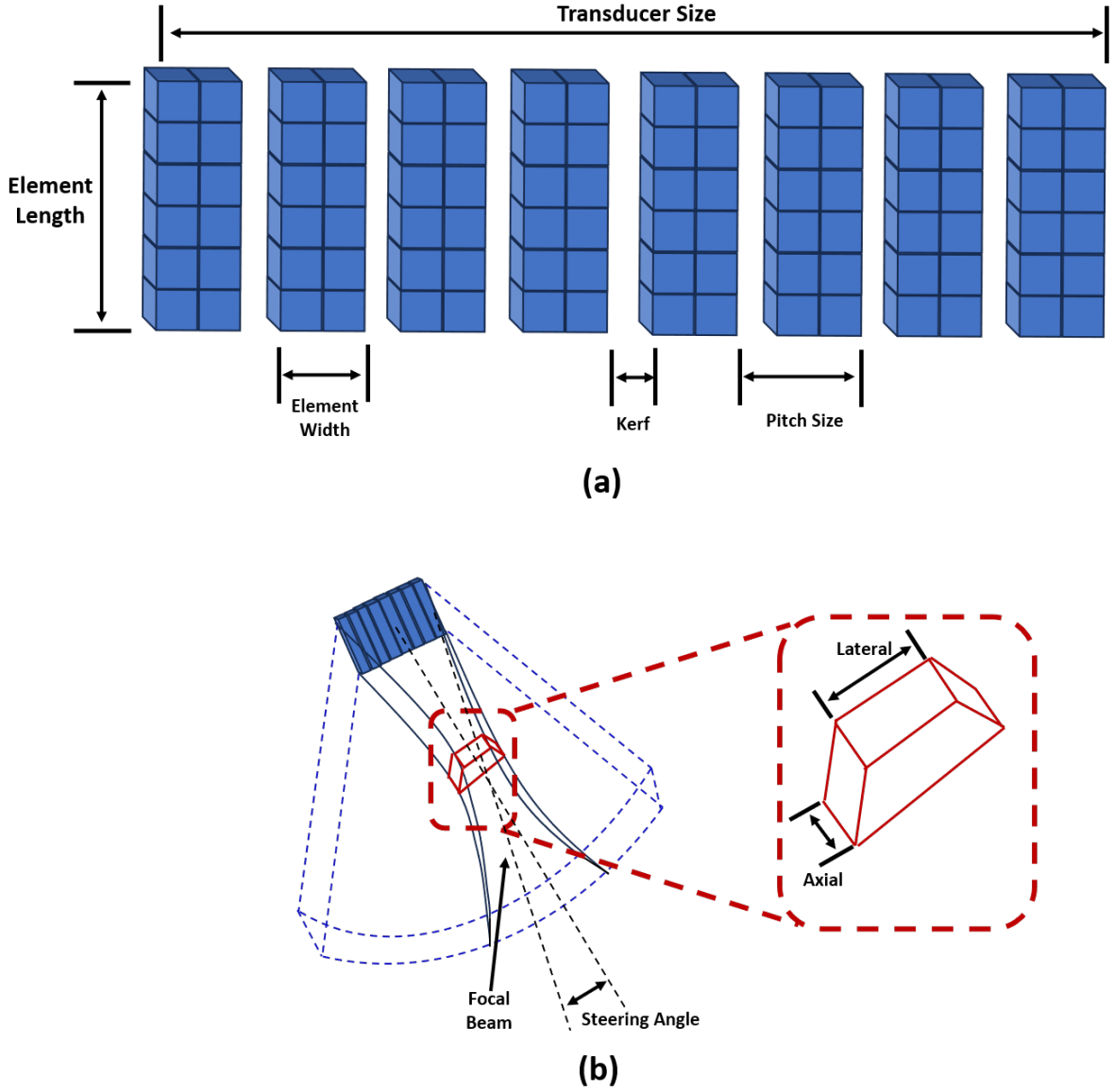


Figure 2.7: (a) Main physical parameters for 1-D transducer, (b) 3-D beam pattern of a 1-D transducer. The red square highlights the 3-D beam pattern around the focal volume. The difference between axial resolution and lateral resolution is noted on the graph. Please note that the actual shape of the focal area is not a cuboid. The simplified beam shape only serves as an illustrative purpose to understand the lateral and the axial resolution.

The 5mm x 5mm transducer used in this work is initially diced into a 1-D array with a 115 μm pitch size and a 25 μm of kerf width to meet the 2-D beamforming requirement. To avoid grating lobes, it is ideal for the pitch size to be smaller than half of the wavelength λ [84], expressed by Equation (2.18), where c is the speed of sound in the medium, f_s is the transducer frequency. According to results in prior

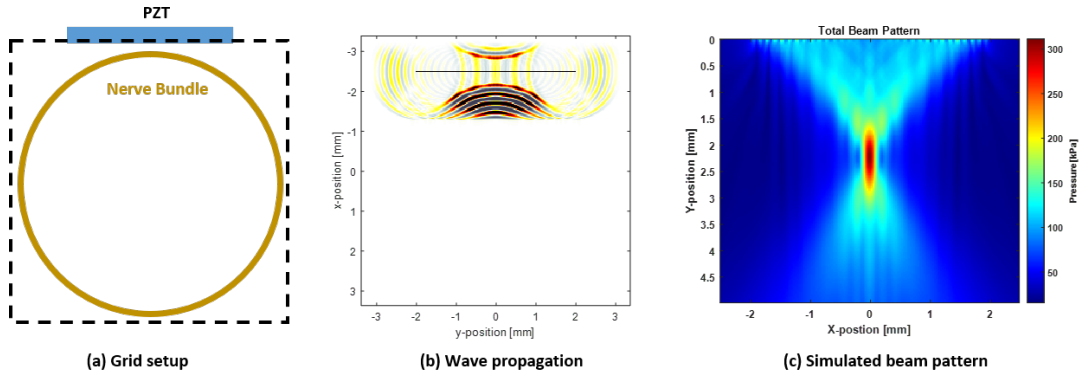
works [26, 85], when the pitch size is close to half the wavelength, the side lobes do not have a significant impact on focal pressure performance. In general, a smaller pitch size would enable finer delay control of each channel, potentially leading to higher focal resolution. However, decreasing the pitch size can make the transducer more sensitive to parasitics [85]. Further decreasing the pitch size also reduces the pressure produced in each channel.

$$Pitch < \frac{\lambda}{2} = \frac{c}{2f_s} \tag{2.18}$$

Model Properties	Values and Units
Transducer Dimension	32x1 1-D array
Grid Size	5 mm × 5 mm
Speed of Sound	1630 m/s
Wavelength	209 μm
Nerve Density	1075 kg/m^3
Attenuation Factor	0.5 dB/cm·MHz
Source Frequency	7.8 MHz
Source Strength	20 kPa/V
Pitch Size	115 μm
Max Steering Angle	45 degrees

Table 2.3: Parameters of acoustic modeling setup.

2.3.2. Beam Pattern and Pressure



(a) Grid setup (b) Wave propagation (c) Simulated beam pattern

Figure 2.8: (a) A simplified diagram of the k-Wave grid setup with a single 32-channel 1-D transducer array. The grid is outlined by dashlines. The size ratios between the grid, transducer, and nerve bundle are 1:1:1. (b) Ultrasonic waves are pulsed with different delays. The wavefronts are shown in deep color. (c) Simulation shows the focal point would have a focal pressure of around 280 kPa and a resolution of 270 μm.

In ultrasound beamforming, a beam pattern is a graphical representation of how the ultrasound energy is distributed in space as the ultrasound beam is transmitted or

received by the transducer array. By analyzing the beam pattern, important characteristics such as resolution and pressure can be derived.

The grid setup and the simulated pattern using parameters in Table 2.3 are shown in Fig. 2.8. The simulated resolution is around 270 μm, suggesting that the performance of the setup is close to the requirements for sub-200μm resolution. However, the pressure is only around 280 kPa at the center point of the grid, which falls way below the average pressure range for AE measurement, as discussed in the first chapter.

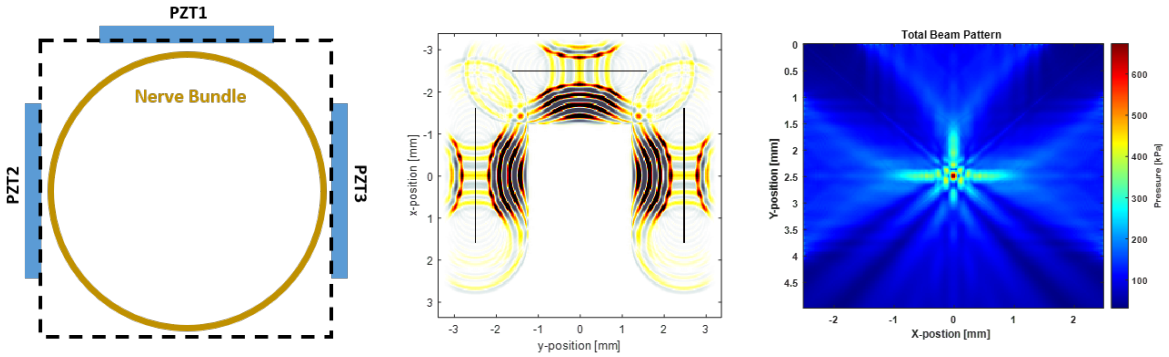


Figure 2.9: (a) A simplified diagram of the k-Wave grid setup with three 32-channel 1-D transducer arrays. The grid is outlined by dashlines. The size ratios between the grid, transducer, and nerve bundle are 1:1:1. (b) Ultrasonic waves are pulsed with different delays. The wavefronts are shown in deep color. (c) Simulation shows the focal point would have a focal pressure of around 820 kPa and a resolution of 100 μm.

Inspired by the curved transducer in [86], placing multiple transducers around the nerve bundle can be an option to boost the focal pressure and suppress the side lobes. A similar setup is simulated with a curved shape transducer, as shown in Fig. 2.9. For simplicity reason, the transducers are placed along the three sides of the grid. Results show the produced pressure is around 820 kPa at the focal point. The results satisfy the requirements for pressure and resolution.

2.3.3. Beamforming Resolution

The beam pattern in the previous subsection is generated by adding beamforming delays between adjacent channels. These delays are usually quantized and controlled digitally. Fig. 2.10(a) shows an array with 5 channels, where the delay between the channel in the middle and the i-th channel towards the edge can be expressed by Δt. The quantizer's least significant bit (LSB) can be expressed by the max delay between two channels and the number of bits N:

$$LSB = \frac{\Delta D_{max}}{2^N - 1} = \frac{D_{MAX} - D_{MIN}}{2^N - 1}. \tag{2.19}$$

The full scale of the delay difference can be expressed as:

$$FS = \frac{\Delta D_{max}}{c}. \tag{2.20}$$

In this work's simulation setup, the maximum distance difference is calculated to be around 2500 μm. The full scale of the quantizer is 1.5 μs. Determining the

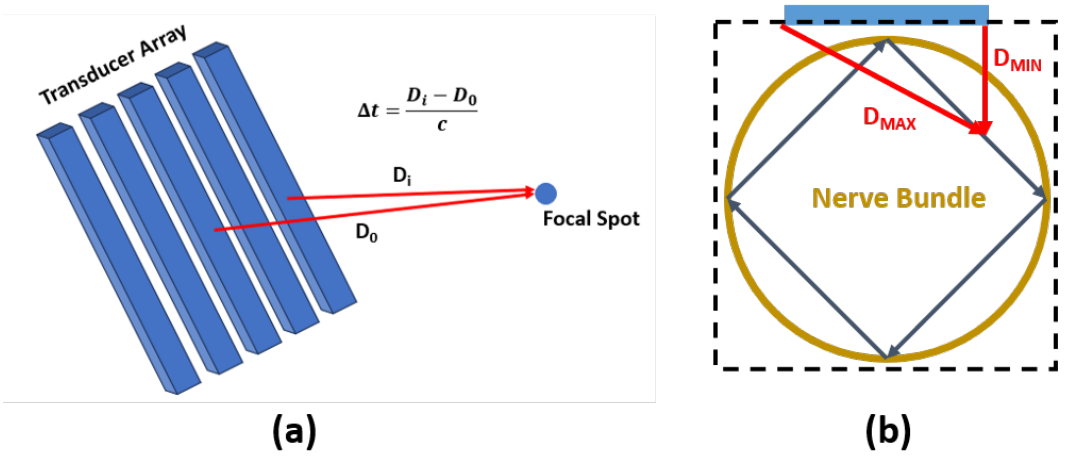


Figure 2.10: Beamforming for 1-D transducer array, (a) A simplified diagram of 1-D transducer array beamforming, (b) with 45° of steering angle for all transducers, 64% of the grid area can be covered. The maximal delay difference is found at the point indicated in the diagram (b).

beamforming-delay resolution can be tricky since it impacts focal resolution, pressure, and system complexity. These variations also depend on the steering angle of the beam. For this design, the quantization bit is varied from 1 bit to 8 bits to find the optimal trade-off point.

The simulated beam patterns for both the one-transducer and the three-transducer setups are depicted in Fig. 2.12. From sub-graph (a) to (e), a noteworthy observation is the substantial reduction in side lobes when using a 5-bit quantizer. However, when a 45-degree steering angle is applied, as depicted in sub-diagram (f), the side lobes remain prominent. Thus, the quantization bit is further increased to 6. As revealed in Fig. 2.13 and Fig. 2.11 (a), no significant pressure loss occurs at the focal point, and the occurrence of side lobes is greatly suppressed when employing a 6-bit quantizer. This indicates that a 6-bit quantizer makes an optimal balance between resolution, pressure, and circuit complexity.

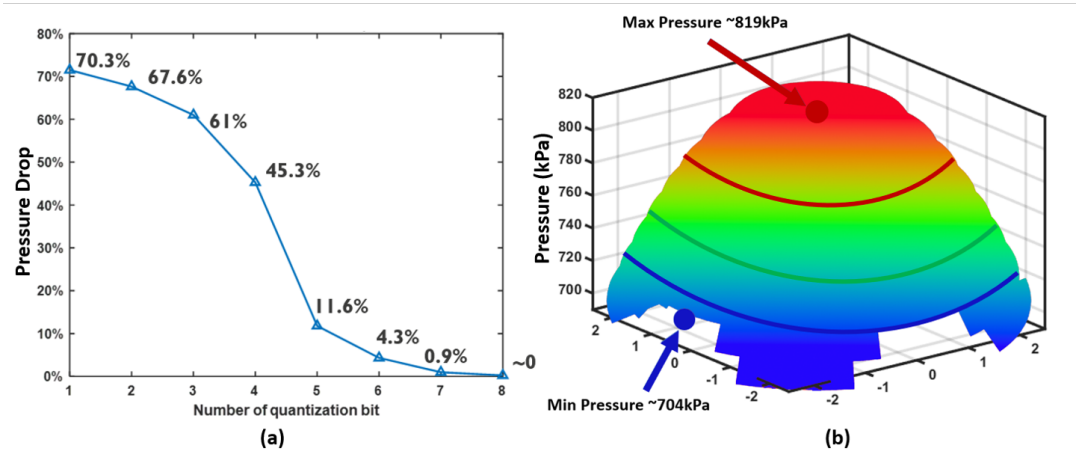


Figure 2.11: (a) Focal pressure loss as a function of the number of quantization bits. (b) Pressure map of the nerve bundle. The minimum pressure of 704 kPa is achieved at the edge of the bundle. A peak pressure of 819 kPa at the center of the grid can be obtained.

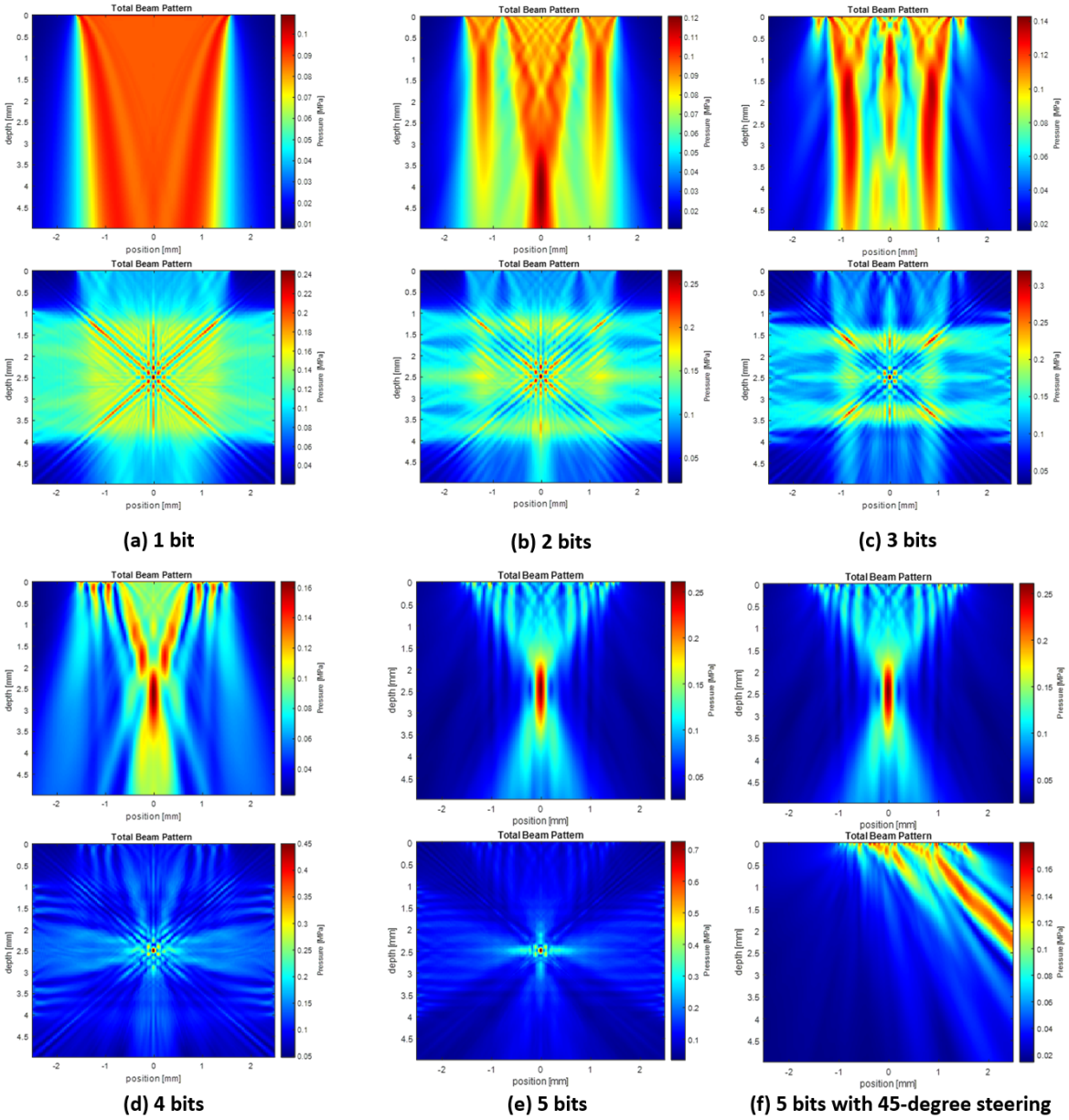


Figure 2.12: Simulated beam pattern diagram with different numbers of quantization bits. From (a) to (e), the upper diagram is the result of the single-array setup while the lower diagram is the result of the three-transducer array. One can observe that when the bit number reaches 5, the side lobes become less significant with no steering angle. However, if 45-degree steering is applied, there still exist massive side lobes that lower the resolution and focal pressure.

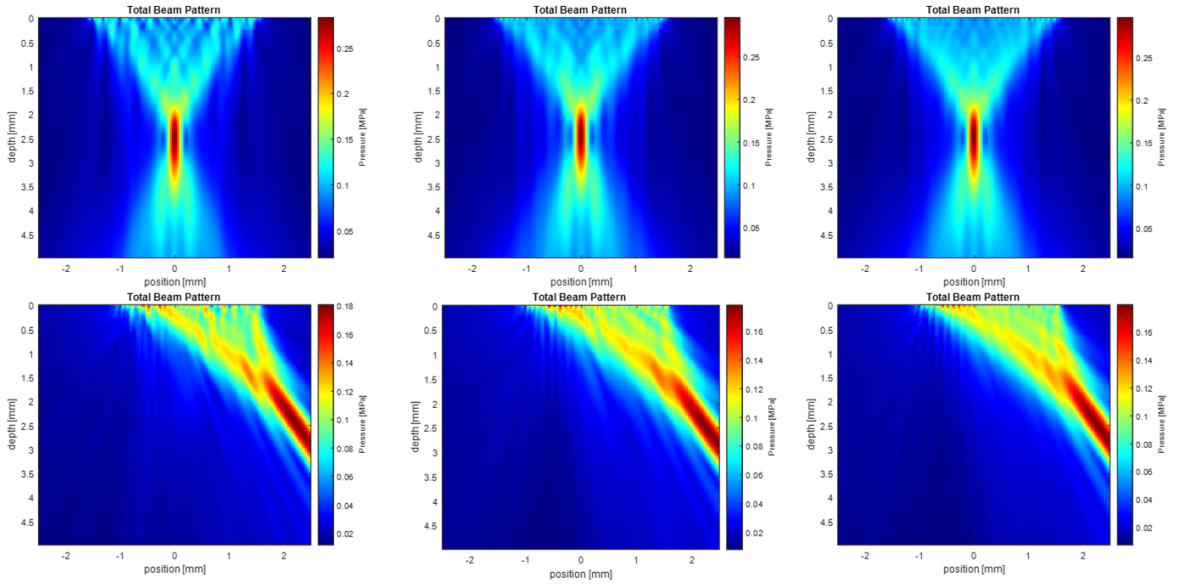


Figure 2.13: Beamforming diagram with 6 bits to 8 bits of the quantizer and 45-degree steering angle. No significant side lobes exist with 6 bits or higher.

2.4. System Performance

The estimated TX performance derived from transducer analysis, PA efficiency estimation, and acoustic modeling is summarized in Table 2.4.

System Specifications	
Target Area	Nerve bundle with 4 mm diameter
Transducer	32x1 1-D PZT
Pitch Size	115 μm
Acoustic Power / Channel	$\sim$ 2.08 mW
Frequency	7.8 MHz
Range of Pressure	704 kPa - 819 kPa
Focal Resolution	100 μm
Quantization Bit	6 bits
Delay Resolution	24 ns
Power Efficiency	> 72.6%

Table 2.4: System specifications for the transmitting channel.

3

Circuits Design

This chapter explores the circuit design for the PA signal chain. It is divided into four sections, each addressing a specific aspect of the design process. The first section focuses on the impact of non-idealities on PA energy efficiency. The second section dives into the modeling and design of the main stepwise pulser, considering various topologies to determine the optimal design strategy for this work. Modeling and design of the stepwise circuit are performed. The third section illustrates the design of the level-shifting channel. The fourth section introduces the design of a low-power stepwise controller to relieve routing issues for large array integration. Finally, the chapter concludes by presenting the performance of the signal chain.

3.1. Non-idealities of the Switched-Mode Pulser

In the previous chapter, the derivation of the class-D PA efficiency baseline highlights the significant influence of the physical properties of the transducer load on PA efficiency. However, this baseline efficiency does not take into account any technology-dependent non-idealities inherent to the circuit. Therefore, in this section, the main non-idealities affecting the efficiency of the switched-mode PA are examined to pave the way for circuit modeling and design.

3.1.1. Gate Charge Loss

The gate charge loss P_Q is the power dissipated to turn a switch on and off. It is one of the intrinsic losses of switched-capacitor circuits and can be expressed by

$$P_Q = C_g V_{DD}^2 f_{SW}. \tag{3.1}$$

For a switched-mode PA driving a transducer, switching frequency f_{SW} is fixed by the series resonance frequency f_s, and supply voltage V_{DD} is held constant within a power-supply domain. Gate capacitor C_g exhibits a directly proportional relationship with the physical dimensions of the switch. Fig. 3.1 presented the extracted gate capacitance under different gate-to-source voltage (V_{GS}) and width-to-length ratio (W/L) conditions. Hence, to reduce the total gate-charge loss, the number and size of the switches used should be as small as possible.

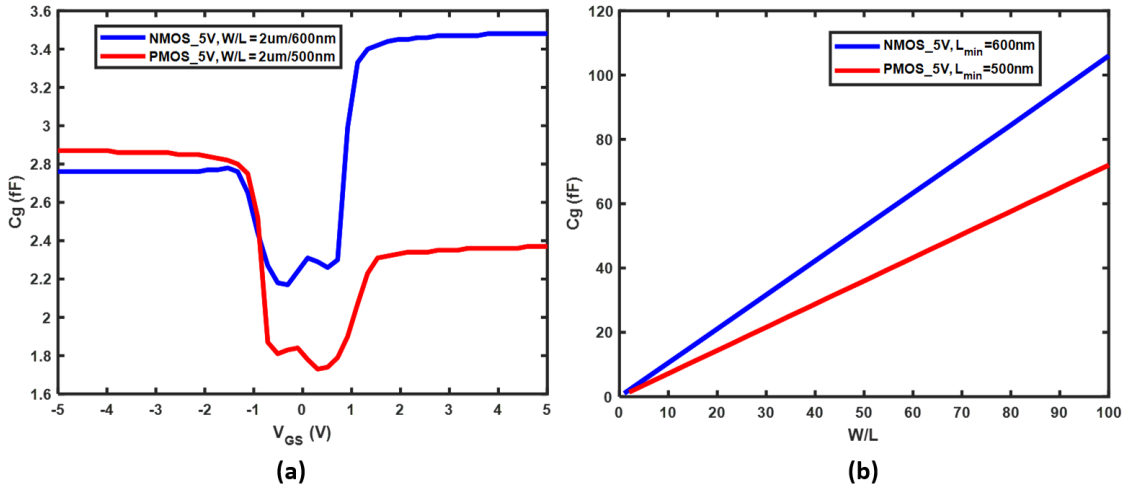


Figure 3.1: Simulated C_g with varying V_{GS} and W/L, V_{DS} is fixed to 10 mV. (a) C_g v.s. V_{GS}, (b) C_g v.s. W/L ratio.

3.1.2. Output Resistance

The output resistance of a switched-mode PA, denoted as R_{OUT}, considerably impacts the overall power efficiency. Take the class-D PA as an example.

The simplified circuitry for the conventional switched-mode class-D PA is depicted in Fig. 3.2. The pull-up and pull-down networks comprise a PMOS and an NMOS switch to maximize the voltage swing at output. The switches are driven by level shifters and buffers with a reference frequency f_s, which in our case is 7.8 MHz. Ultrasonic transducers typically operate in the kilohertz to tens of megahertz range. The output voltage V_{OUT} undergoes complete switching between V_{DD} and ground. This switching action incurs a potential drop across the switch resistance, resulting in conduction loss P_{cond}.

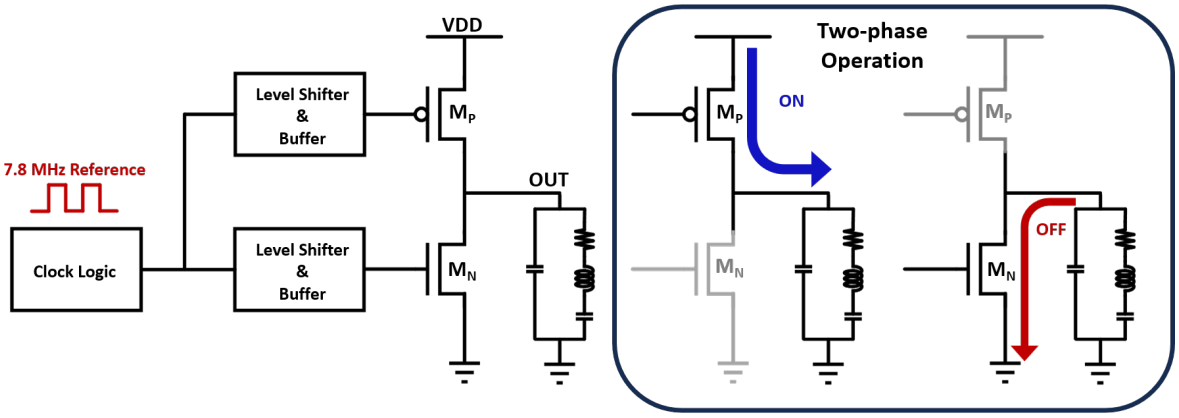


Figure 3.2: Circuit diagram of a class-D PA. It operates in a two-phase fashion. During the ”ON” phase, the transducer is charged to the supply voltage, and during the ”OFF” phase, it is discharged to the ground.

The switching behavior of this circuit is abstracted by the network in Fig. 3.3, where R_{OUT} represents the equivalent output resistance of the PA. When driving the transducer at series resonance frequency f_s, L and C cancel each other. In this case,

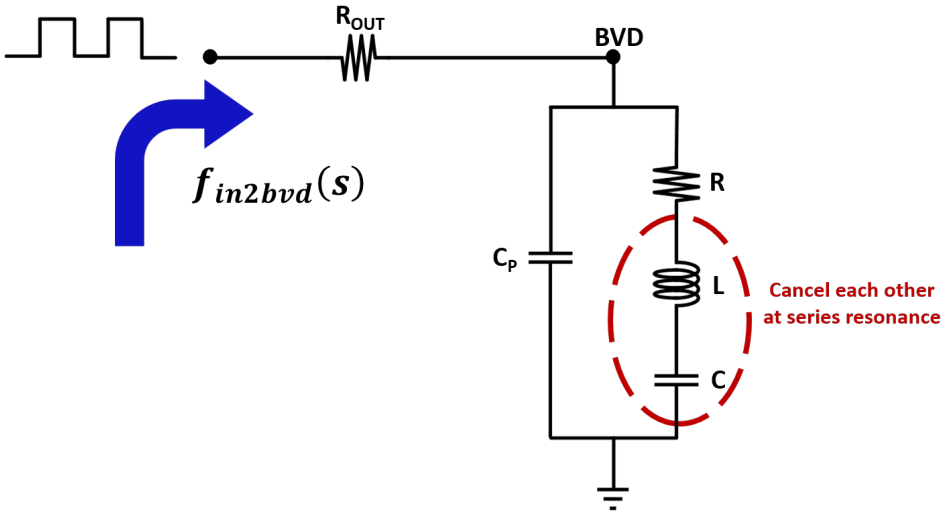


Figure 3.3: Equivalent circuit of class-D PA driving a transducer load.

the transfer function from the input to the resistive load R in the Laplace s-domain can be expressed as:

$$f_{in2bvd}(s) = \frac{R//\frac{1}{sC_p}}{R_{OUT} + R//\frac{1}{sC_p}} = \frac{1}{1 + \frac{R_{OUT}}{R} + sR_{OUT}C_p}. \tag{3.2}$$

As previously discussed, the intrinsic nature of the transducer's frequency response resembles that of a narrow-band resonator. Most of the out-of-band harmonics of the class-D driving signal are effectively suppressed. Therefore, it is reasonable to focus primarily on the fundamental power loss associated with R_{OUT} when analyzing the energy efficiency of the PA. Applying the transfer function to Equation (2.11), the fundamental power delivered to the resistive component of the BVD load can be reformulated as:

$$P_{R,OUT} = \frac{\left(\frac{|V_R \times f_{in2bvd}|}{\sqrt{2}}\right)^2}{R} = \frac{2\alpha^2 V_{DD}^2}{\pi^2 R}, \tag{3.3}$$

where α^2 represents the squared magnitude of the transfer function (3.2), defined as:

$$\alpha^2 = |f_{in2bvd}(s)|^2 = \frac{1}{\left(1 + \frac{R_{OUT}}{R}\right)^2 + (R_{OUT}C_p f_s)^2}. \tag{3.4}$$

Substituting $R_{OUT}C_p f_s$ by the intrinsic Q and P factors of a transducer, α^2 can be further modified to:

$$\alpha^2 = \frac{1}{\left(1 + \frac{R_{OUT}}{R}\right)^2 + \left(\frac{\frac{R_{OUT}}{R}}{2\pi Q[(1+P)^2 - 1]}\right)^2}. \tag{3.5}$$

Finally, to account for the fundamental power loss on the output resistance, the energy efficiency of the switched-mode pulser can be expressed as:

$$\eta_D = \frac{\frac{2\alpha^2 V_{DD}^2}{\pi^2 R}}{\frac{2V_{DD}^2}{\pi^2 R} + C_p V_{DD}^2 f_s} = \frac{\alpha^2}{1 + \frac{\pi}{4Q[(1+P)^2+1]}}. \tag{3.6}$$

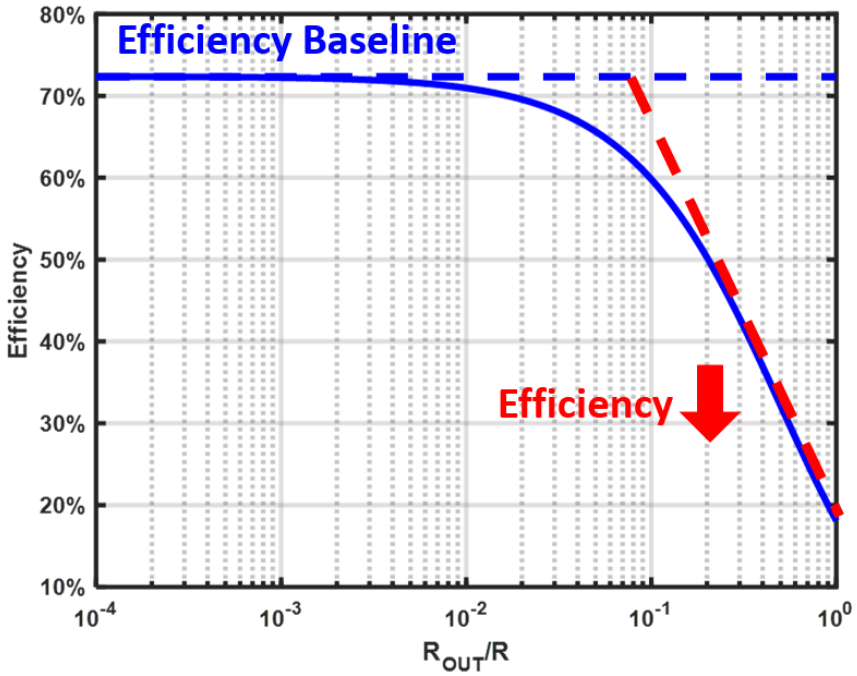


Figure 3.4: Efficiency baseline as a function of the R_{ON}/R ratio for the PZT model used in this work.

The efficiency drop caused by the voltage drop on R_{OUT} can be visualized in Fig. 3.4. It is evident that as the ratio between R_{OUT} and the resistance R becomes greater than 10^{-2}, the class-D efficiency would experience a significant drop compared to the baseline efficiency (which is 72.6% for the PZT transducer used in this work). When the R_{OUT}/R ratio increases to unity, the efficiency drops to only 19%. The above analysis highlights two considerations for maximizing switched-mode pulser efficiency.

Firstly, given a fixed transducer load, minimizing the ratio between output resistance R_{OUT} and resistance R of the RLC branch is critical. This minimization ensures that the factor α^2 approaches unity, thus maximizing the energy efficiency. Otherwise, in case the switches are not appropriately sized, the class-D efficiency would drop significantly, following a logarithm relationship. Prior research studies [46, 51, 63] have demonstrated that the value of R is strongly dependent on the transducer type and its element size, typically falling within the range of hundreds to thousands of ohms. Additionally, the output resistance of the PA is heavily influenced by the semiconductor technology. Typical values of R_{OUT} reported fall within the range of tens to hundreds of Ohms [87]. An important trade-off to consider is that smaller values of R_{OUT} result in wider transistors, which can lead to higher gate-charge losses.

Secondly, when the R_{OUT}/R ratio is sufficiently small, the efficiency stays approximately the same, thus increasing the number of transducer elements in each channel becomes feasible. This increase in element size leads to higher output power from the

transducer, effectively diminishing the significance of other power losses (e.g., digital control power, level shifting power) so that the overall efficiency can be improved. Notably, the analysis explains a similar approach employed during measurements in [46], where a single pulser channel drives two adjacent elements to achieve better efficiency.

In conclusion, the primary trade-offs in switched-mode PA design revolve around balancing considerations in gate-charge loss P_Q and conduction loss P_{cond}, as well as optimizing output power P_R relative to P_{cond} in the switches. The R_{OUT}/R ratio should be small to avoid power loss on R_{OUT}, which can be done by increasing the switch size but at the cost of more considerable gate-charge loss.

3.1.3. Slew-Rate Modulation

The slew rate of a driving signal is defined as the slope of its rising and falling edges. For a switched-mode PA driving a transducer, a reference signal is required to drive the transducer at series resonance. Altering the architecture of the switched-mode pulser can potentially modulate the rising/falling time. If the supply voltage is fixed, this would further change the slew rate of the driving signal, introducing non-ideal characteristics. In fact, all switched-mode PA architectures more or less have modulated slew rates, for instance:

- In the case of a charge-redistribution pulser with current source calibration [35], the slew rate can be influenced by the bias of the current source.
- For an energy-replenishing pulser [52], the slew rate is primarily determined by the resonance frequency of the internal inductor and plate parasitic C_P (rising time is $\frac{2\pi\sqrt{LC_p}}{4}$ as stated in the paper, in which a pure capacitive load is considered).
- In stepwise pulsers [46, 63], the slew rate of the waveform can be modulated by adjusting the interval and the number of steps introduced.

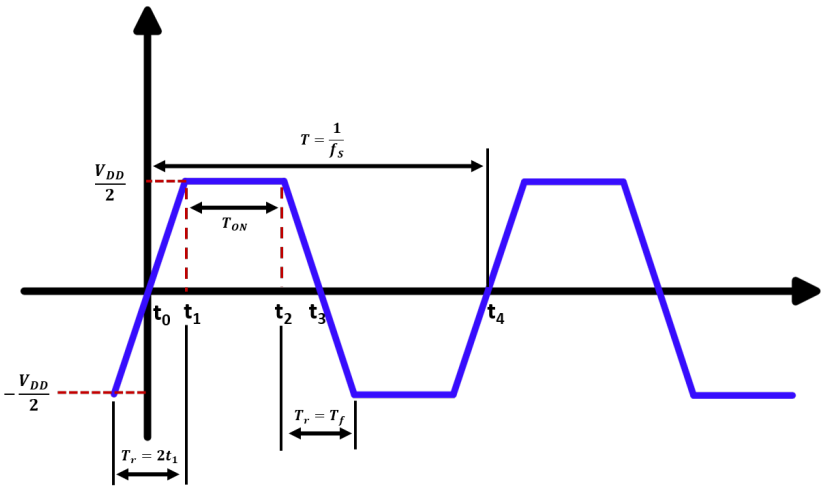


Figure 3.5: Switched-mode driving signal with finite slew rate.

The modulation of slew rate can be effectively modeled by a square wave with finite rising and falling speed, as illustrated in Fig. 3.5. It is assumed in this analysis that the waveform exhibits a 50% duty cycle (t_3/t_4 = 50%) with a peak-to-peak value equals to the supply voltage, V_{DD}.

The fundamental components of this square wave can be expressed as:

$$V_{sq,1}(t) = 2V_{DD}\frac{T_r + T_{ON}}{T} sinc\left(\frac{T_r + T_{ON}}{T}\right) sinc\left(\frac{T_r}{T}\right) \sin(\omega_s t). \tag{3.7}$$

Given the assumption of a 50% duty cycle ($\frac{T_r+T_{ON}}{T}$=0.5), the fundamental power delivered to the resistive part of the load can be revised as:

$$\begin{aligned} P_{R,SR} &= \frac{\left(\frac{|V_{sq,1}|}{\sqrt{2}}\right)^2}{R} = \frac{\left(\frac{2V_{DD}}{\pi}\right)^2 sinc^2\left(\frac{T_r}{T}\right)}{2R} \\ &= \frac{2V_{DD}^2}{\pi^2 R} sinc^2\left(\frac{T_r}{T}\right) \\ &= sinc^2\left(\frac{T_r}{T}\right) P_R, \end{aligned} \tag{3.8}$$

where P_R is the power delivered to the resistive part when an ideal class-D driving signal is applied. The acoustic efficiency of a class-D PA can be further revised as:

$$\eta_D = \frac{P_{R,SR}}{P_{R,SR} + P_{SW}} = \frac{sinc^2\left(\frac{T_r}{T}\right) P_R}{sinc^2\left(\frac{T_r}{T}\right) P_R + C_p V_{DD}^2 f_s} = \frac{sinc^2\left(\frac{T_r}{T}\right)}{sinc^2\left(\frac{T_r}{T}\right) + \frac{\pi}{4Q[(1+P)^2+1]}}. \tag{3.9}$$

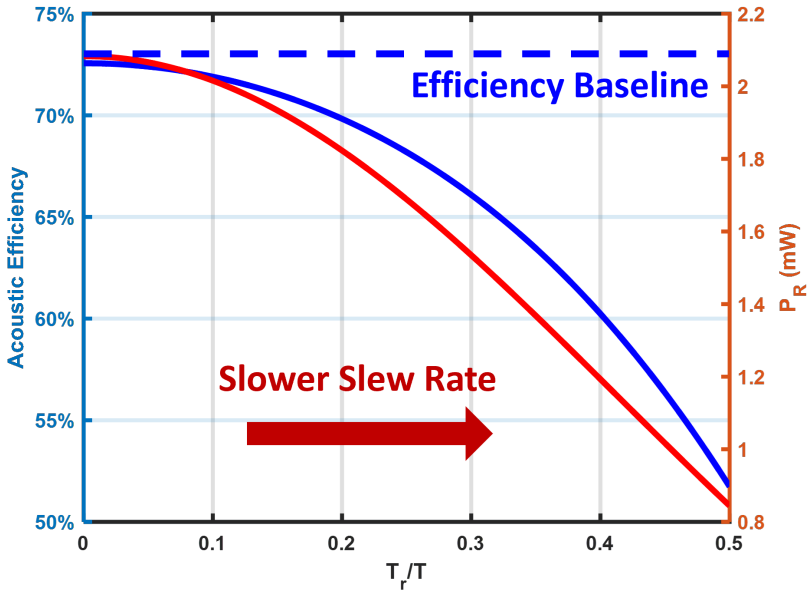


Figure 3.6: Efficiency baseline and output power vary with the slew rate of the driving signal.

The above analysis shows that a slower slew rate, indicated by a larger T_r/T ratio, would result in less power delivery to the transducer and lower overall efficiency, as visualized in Fig. 3.6. The closer the T_r/T ratio is to zero, the higher the output power and overall efficiency. Depending on the types of PAs, it's also possible that the slew-rate modulation causes a short circuit from supply and ground, leading to other associated losses.

3.1.4. Efficiency Trade-offs

The analysis in this section reveals the trade-offs among gate-charge loss, conduction loss, and slew-rate modulation to attain high energy efficiency in the switched-mode PA. The overall trade-offs for high-efficiency PA design can be shown through the graph below.

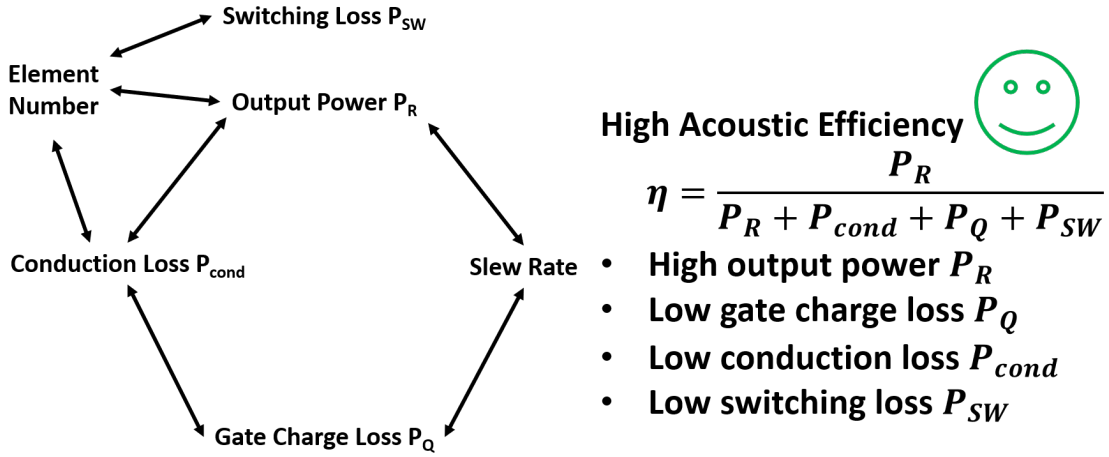


Figure 3.7: Trade-offs of high-efficiency switched-mode PA design.

3.2. High-Efficiency Power Amplifier Design

The ultrasound power amplifier is an extremely power-consuming component within the transmit chain. The primary goal of this work is to design a PA channel with high energy efficiency suitable for invasive biomedical applications. After analyzing the main power losses of the switched-mode PA, it becomes feasible to discuss and develop high-efficiency PA architectures.

This section begins by exploring various PA architectures, each aligned with distinct design strategies. Following this exploration, the design strategy, modeling, and circuit design for this work are presented.

3.2.1. Topologies and Design Strategies

Based on the trade-off relationship in Fig. 3.7, the design strategies employed in prior works can be categorized into two main directions: enhancing acoustic power and reducing power losses.

Enhancing Acoustic Power

The main idea of this strategy is to increase the power dissipated on the resistive part of the transducer while minimizing associated losses.

The study conducted by [56] introduced a differential stepwise charging circuit to enhance the output swing of a capacitive load and reject the common mode during readout. This concept was subsequently adopted in [46], where a similar differential scheme is used to periodically flip the polarity of the transducer. The operation principle in these two works can be simplified and illustrated in Fig. 3.8. Assuming the top terminal of the transducer is initially charged to the supply voltage, a stepwise charging process extracts charge from the top plate of C_p. Concurrently, when C_p is switched to ground, the switches S_6 and S_7 in the ”H” bridge configuration are closed, and S_5, S_8 are opened simultaneously. In the subsequent phase, the charge stored in C_{fly} is used to recharge the transducer from the bottom terminal, and the top terminal becomes the ground. When the bottom terminal is charged to the supply voltage again, the process repeats.

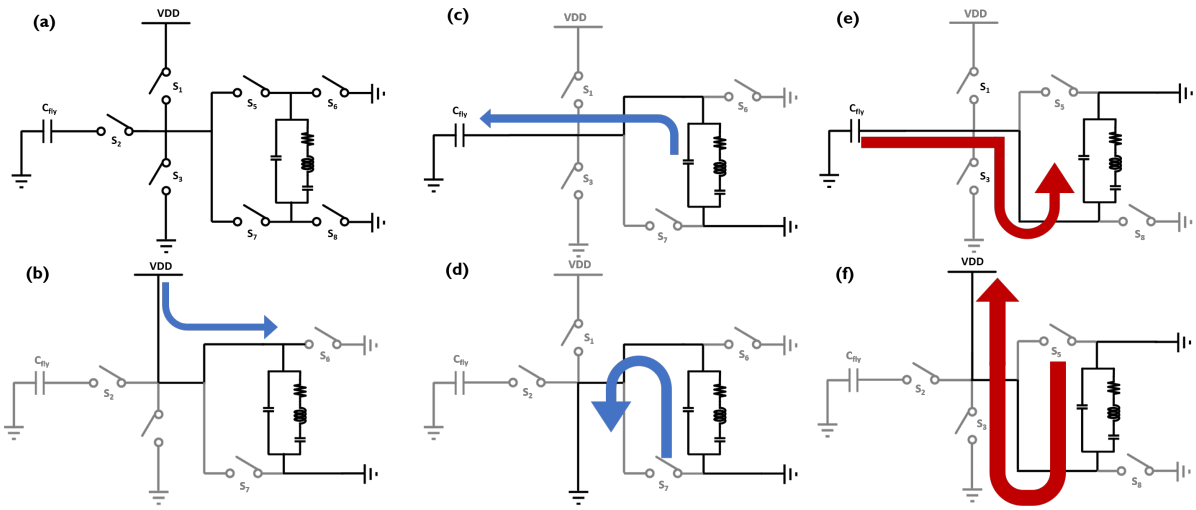


Figure 3.8: Stepwise charging with transducer flipping, (a) overall circuit diagram, (b) charging top plate to supply, (c) extract charge from the top plate to flying capacitor, (d) discharge top plate to the ground, (e) charge the bottom plate using the flying capacitor, (f) charge the bottom plate to supply.

This approach provides a notable enhancement, effectively doubling the output swing of the differential signal between two terminals. Consequently, the power delivered to the resistive load is quadrupled without the need for an increase in the supply voltage. Furthermore, this approach can lead to increased overall efficiency, as the switching loss on C_p only doubles during polarity flipping. Although there would be extra gate-charge loss introduced by the switches in the ’H’ bridge, this becomes negligible when C_p is significantly larger than the gate parasitic of switches, which is generally the case as seen in Fig. 3.1.

Despite the numerous advantages offered by this approach, the formidable challenge of large-array integration poses a significant obstacle to its practical implementation. A prevalent fabrication method for pMUT and PZT transducer arrays, both in academic research [49, 73] and industry applications [67], involves connecting the ground of the entire array to a single common foil. Consequently, the flipping proce-

dure cannot be applied to beamforming, where dedicated control for each channel is a necessity.

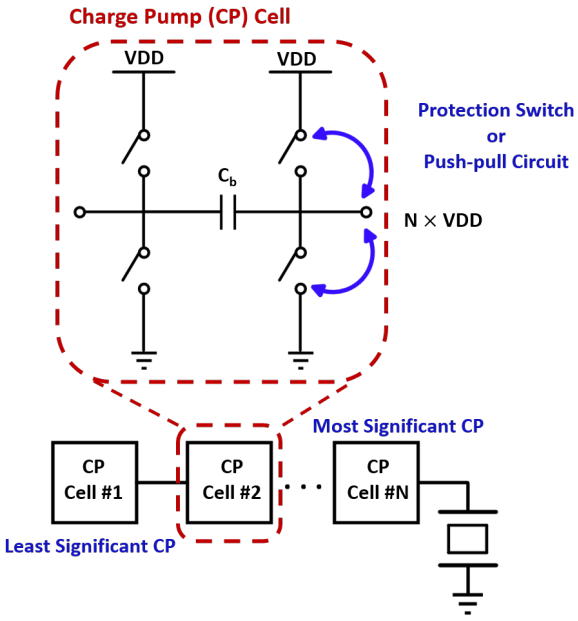


Figure 3.9: Stepwise circuit based on cascaded charge pumps driving a transducer load. The simplified charge pump cell is depicted in the figure, where C_b is the boosting capacitor. The output of the N-th charge pump cell is $N \times V_{DD}$. Protection switches or push-pull circuits of each switch are simplified.

Efforts have been invested in increasing the output power using single-ended structures. One such approach is to use DC-DC boost converters, as demonstrated in [88]. However, for invasive AE imaging applications, the foremost priority is to enhance the energy efficiency of the pulser. Introducing additional DC-DC converters to boost the power supply is not a viable option for small-footprint applications, as in such cases, the overall efficiency would be determined by the efficiencies of two separate circuit blocks, the DC-DC converter and the pulser. An alternative approach, as shown in Fig. 3.9, is to employ cascaded charge-pump (CP) cells to boost the output power [64]. In theory, using N CP-cell stages can boost the output node of the N-th cell to $N \times V_{DD}$ if the load is purely capacitive. However, several issues make it a less promising solution when driving a transducer. Firstly, the charge pump needs extra protection switches or push-pull circuits to protect transistors from breaking down. The more CP cells implemented (higher voltage at the output node), the more complex the protection circuits. Additionally, when the output is boosted to its maximum, the transducer is entirely supplied by the energy stored in the most significant CP cell. This can pose challenges when driving a less capacitive transducer. In such cases, a substantial portion of energy sharing occurs between C_b and the RLC branch. Consequently, the capacitor of the most significant CP cell must be excessively large to provide enough energy for the RLC oscillation during T_{ON}, as depicted in Fig. 3.5. Due to these factors, the transducer used in [64] is deliberately made highly capacitive so that most of the energy in the most significant CP cell is delivered to the capacitive part. In this case, the voltage level at the output node can be close to $N \times V_{DD}$. Even though a highly capacitive transducer is implemented in [64] (with a P factor of only 1%, as can be seen in Table 2.2), the achieved energy efficiency is still 1% lower than

its class-D baseline. This implies that this approach is ineffective in enhancing the overall PA efficiency.

In conclusion, the strategy of enhancing the power by flipping the polarity of transducer plates proves effective in boosting the power delivered to the resistive part of the transducer. Little energy loss would be introduced during the flipping, hence, this can lead to increased overall efficiency. However, it involves the swapping of both transducer terminals, which is impractical for flip-chip bonding arrays. The single-ended boosting strategy, whether using DC-DC converters or charge pumps, serves the same power-boosting purpose. Nevertheless, it requires extensive protection circuits and large boosting capacitors to address challenges such as high-voltage breakdown and conduction loss during energy sharing between the most significant charge-pump cell and the RLC branch of the transducer. These drawbacks make single-ended boosting structures less promising for achieving higher energy efficiency compared to differential architectures.

Reducing Power Loss

Another widely used design strategy for high-efficiency PAs is reducing energy loss within the circuit. The previous section identified and analyzed two types of loss sources: conduction loss P_{cond} and switching loss of C_p. As the derivation of the class-D efficiency baseline demonstrated, the impact of conduction loss can be safely disregarded as long as the transducer array's switch size and element length are properly designed. This allows the pulser efficiency to approximate the baseline efficiency better. Fig. 2.5 illustrates that the P factor, which is related to the switching loss on C_p, plays a more significant role than the Q factor in determining the total energy efficiency. Therefore, the primary focus in prior arts is on reducing the loss on C_p.

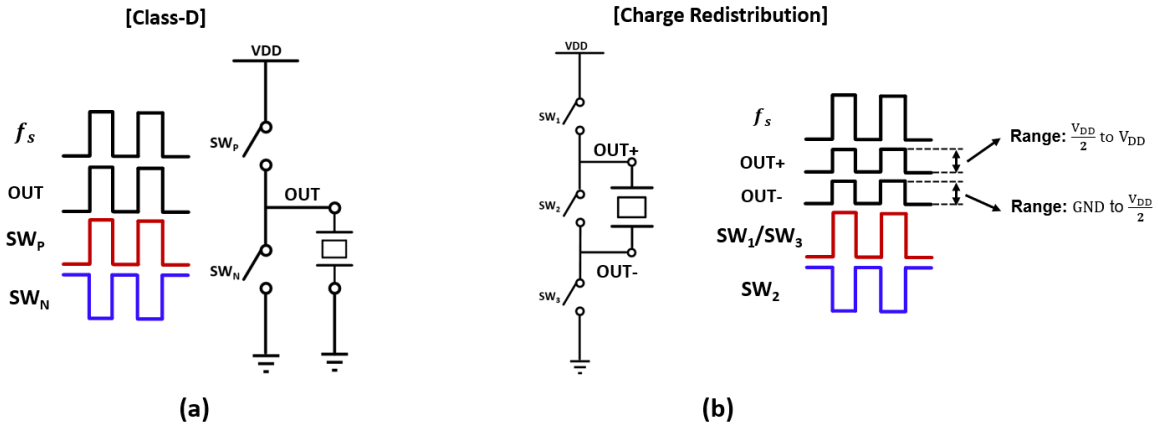


Figure 3.10: Class-D and charge-redistribution pulsers and their timing waveforms. When the timing signal is high, the corresponding switch is on. When the signal is low, the corresponding switch is off. (a) Class-D PA, the swings of all signals are V_{DD}. (b) Charge-redistribution PA, the signals swing from the ground to the supply voltage except for OUT+ and OUT-.

In [47, 48], the charge-redistribution pulser has been implemented. As depicted in Fig. 3.10(b), the primary distinction between this approach and the class-D pulser in Fig. 3.10(a) is that the two plates of the transducer are shorted together during the off phase of the class-D driving signal. In this way, the relaxation of the piezoelectric

membrane comes to a halt, and the potential at both terminals would return to the common mode $V_{DD}/2$. Consequently, this configuration results in the saving of half of the loss on C_p. It is worth noting that a customized pMUT transducer is implemented in this work, where two electrodes are introduced between the two layers of piezoelectric material. In this case, beamforming can be successfully employed by controlling both electrodes within each channel (please note that the conventional flip-chip bonding array has only one common ground). However, as indicated in Table. 2.2, this achievement comes at the expense of a significant reduction in the quality factor of pMUT, which is only 4.85. When compared to [64], where a pMUT with a Q factor of over 180 and a baseline efficiency of 82.7% is used, the efficiency for this customized pMUT is notably lower, only 39.6%. Saving 50% of C_p loss ideally leads to around 70% of total acoustic efficiency, which is still lower than most of the class-D baseline efficiencies available in publications.

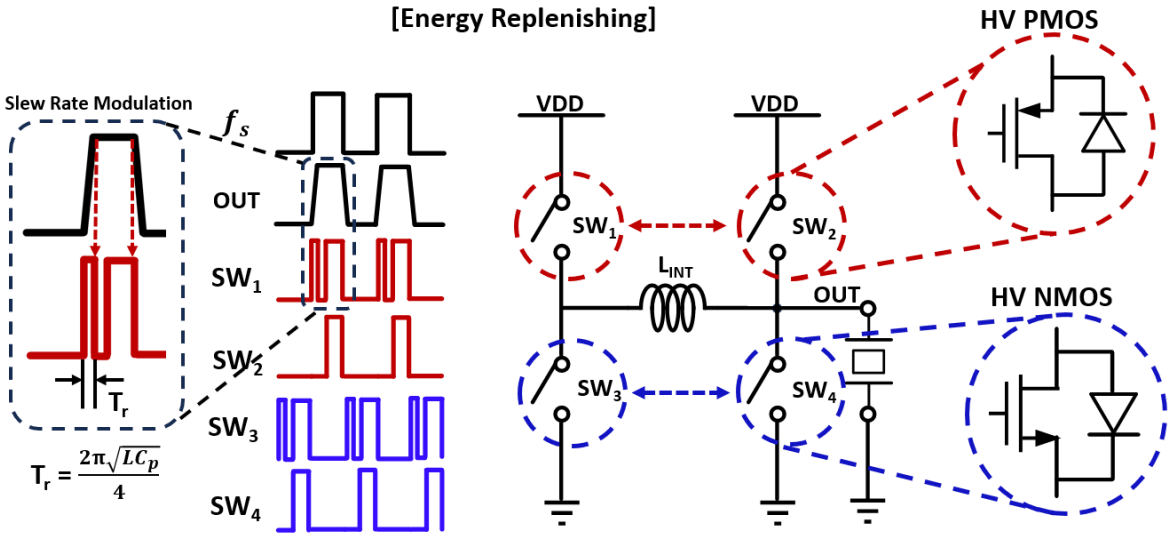


Figure 3.11: Energy-replenishing pulser and its timing waveforms. When the timing signal is high, the corresponding switch is on. When the signal is low, the corresponding switch is off. The voltage swings of all signals are V_{DD}.

The energy-replenishing pulser [52] introduces a high-quality inductor L_{INT} between two class-D stages to conserve the energy loss on C_p. As shown in Fig. 3.11, SW_1 is first closed to charge the load to V_{DD}. When SW_1 is open, the energy stored in the inductor will flow back to the power supply through the body diode of SW_2. In the discharging phase, SW_3 is closed to discharge the transducer to the ground, and the energy stored in C_p is transferred to the inductor. In this pattern, when SW_3 is opened, the energy stored in the inductor would go back to the supply through the body diode of SW_1. Ideally, all energy on C_p can be saved.

However, the operation of the energy-replenishing pulser introduces certain challenges. Firstly, the switching of SW_1 and SW_3 must establish another resonance point between L_{INT} and C_p, which is time-consuming in general. As reported, the required settling time takes hundreds of oscillation periods, significantly longer than conventional class-D pulser. Due to this slow settling, the energy-replenishing pulser is less suitable for producing fast bursts as required in AE imaging. Furthermore, the out-

put slew rate of this PA highly depends on the resonance frequency of L_{INT} and C_p. As discussed in the previous section, achieving a fast rising edge is essential for a switched-mode PA to attain high efficiency. When the load is fixed, L_{INT} should ideally be small to achieve a fast slew rate, but the choice of a smaller inductor inevitably results in higher ripple loss [89] and less energy saving. Hence, a high-quality inductor in the mH range is desired for each PA channel, making highly miniaturized array design in modern technology impossible. Moreover, this approach relies on the body diode of HV transistors, posing difficulties in implementing it in low-voltage technology. Another assumption made in this design is that the transducer is highly capacitive. For a less capacitive transducer, such as PZT, the resonance between the inductor and the RLC branch can form another series resonance frequency close to the resonance frequency of L_{INT} and C_p, leading to more complicated design considerations.

Design Choice for This Work

In the light of the preceding discussions, stepwise charging emerges as the most promising solution to reduce most of the switching losses while still enabling a fast slew rate and easy control for acoustic bursts. The detailed reasons are as follows:

(1) **Feasible for sing-ended pulsers**: Unlike the charge-redistribution pulser and the 'H' bridge pulser, stepwise charging can be seamlessly implemented in a single-ended pulser without periodical flipping both plates of the transducer.

(2) **Fast response**: unlike the energy-replenishing pulser and negative-conductance circuits, the stepwise circuit offers the advantage that the driving waveform can be recovered quickly to produce acoustic bursts once the voltage steps are established on the flying capacitors. This enables the generation of fast pulses without experiencing slow startup.

(3) **Fine control of slew rate**: the slew rate of the stepwise waveform can be precisely controlled by adjusting the pulse width of each switch. Conversely, in the energy-replenishing pulser, the slew rate is primarily determined by the value of the internal inductor L_{INT} and C_p of the transducer.

To realize the full potential of stepwise charging and achieve a minimized form factor, several key improvements are expected:

(1) **Optimize rising/falling edge**: previous works have not analyzed or modeled the design choices for the rising and falling time. As discussed previously, faster rising/falling edges lead to higher PA efficiency. However, this comes at the cost of shorter switch pulses, which, in turn, consume more power to drive the switch.

(2) **Optimize gate-charge loss**: the effect of gate-charge loss on the total efficiency has not been adequately modeled in previous works. However, as discussed, this loss is inherent to switched-capacitor circuit design and can be challenging to mitigate.

(3) **Minimize capacitance budget**: off-chip capacitors are commonly employed when form factor is not a limitation, allowing for the use of excessively large flying capacitors. In some cases, the flying-capacitor-to-load-capacitor ratio has been reported to reach as high as 2.5×10^6 [56]. However, such an approach is not suitable for the application in this work.

3.2.2. Modeling of Stepwise Charge-Sharing System

As concluded in the previous section, stepwise charging is adopted as the design choice for this work. It is a promising solution to effectively reduce the major loss in the pulser while enabling precise control of the slew rate of the output signal. To design such a circuit, one can design from at least 3 levels [53] to potentially tens of levels [59] and use large flying capacitor or DC-DC converters to establish the internal levels. However, this is tedious and could lead to significant over-design. To fully unlock the potential of stepwise circuits for a miniaturized high-efficiency ultrasonic pulser, this work proposed a modeling method to facilitate the design of a highly miniaturized and energy-efficient stepwise pulser.

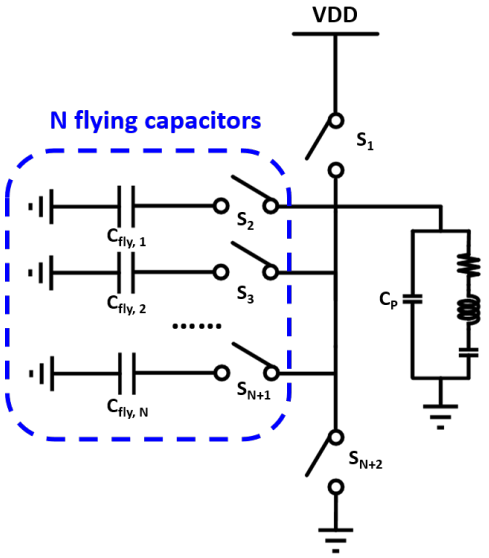


Figure 3.12: The general architecture for stepwise charge-sharing circuits with flying capacitors driving a transducer.

The stepwise circuit with N flying capacitors is used in this work to minimize the system form factor. The general architecture for a stepwise charge-sharing circuit driving a single-ended transducer is shown in Fig. 3.12. This section will introduce the modeling pipeline from bottom to top.

Charge Sharing of Capacitors

The most fundamental principle of stepwise charge-sharing circuits is the conservation of charge. As shown in Fig. 3.13, two capacitors C_p and C_{fly} with initial states V_p and V_{fly} are connected by a switch that exhibits an on-resistance of R_{SW}. The switch is first open. Once the switch is closed, two capacitors start charge sharing. The final state of the charge-sharing process is noted as V_F. Based on charge conservation, V_F can be calculated by:

$$C_p V_p + C_{fly} V_{fly} = (C_p + C_{fly}) V_F, \tag{3.10}$$

$$V_F = \frac{C_p V_p + C_{fly} V_{fly}}{C_p + C_{fly}}. \tag{3.11}$$

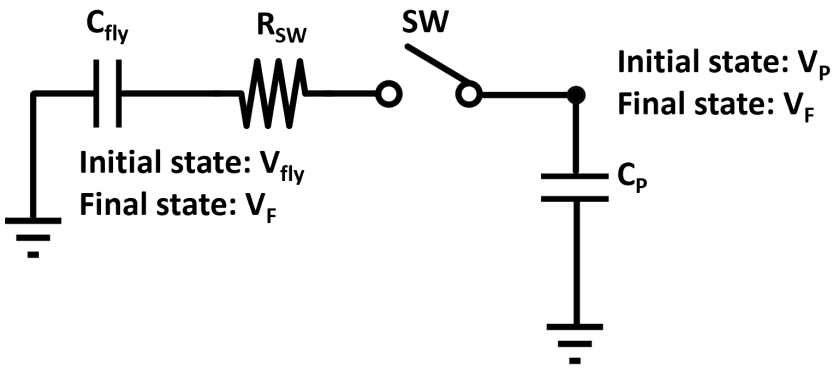


Figure 3.13: Charge sharing behavior between C_p and C_{fly}.

The time constant τ during the charge-sharing process can be expressed as:

$$\tau = R_{SW}C_{eq} = R_{SW}\frac{C_pC_{fly}}{C_p + C_{fly}}. \tag{3.12}$$

Aiming to integrate the complete circuit into a single channel, the design focus is more on the ratio between the flying capacitor C_{fly} and the parasitic capacitor C_p of the transducer (Φ_{CAP}, cap ratio). The time constant and final state can be revised by Φ_{CAP}:

$$V_F = \frac{V_P + \Phi_{CAP}V_{fly}}{1 + \Phi_{CAP}}. \tag{3.13}$$

$$\tau = \frac{R_{SW}C_P\Phi_{CAP}}{1 + \Phi_{CAP}}. \tag{3.14}$$

Stepwise Charge Sharing

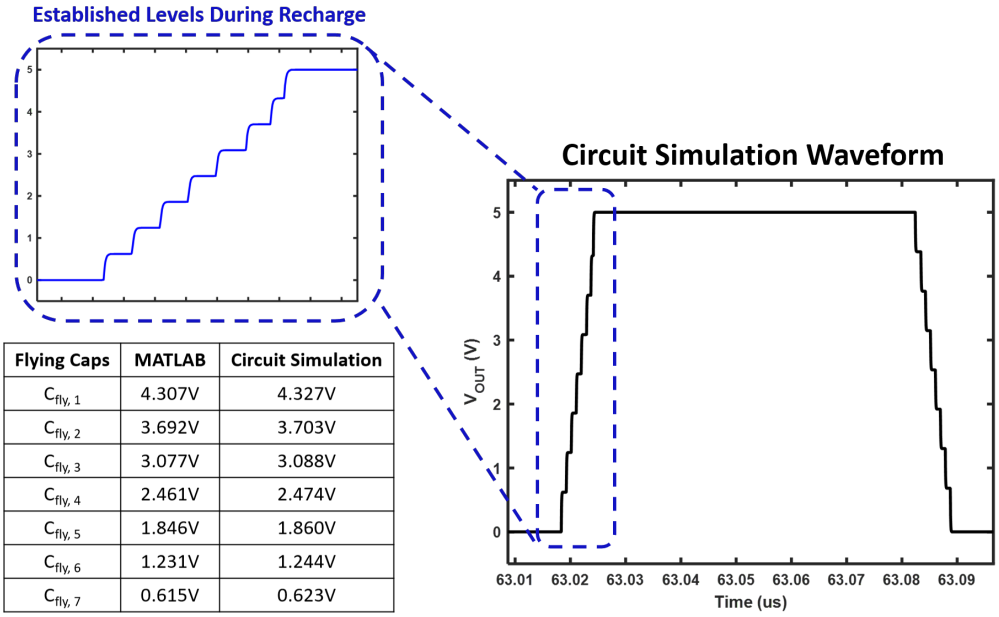
Stepwise charging and discharging a capacitor with N flying capacitors can be abstracted to be $2N$ charge-sharing processes in parallel (except the steps that charge C_p to V_{DD} and discharge it ground). The rising and falling edges both perform N times charge sharing.

The discharge process from the supply to the ground ($C_{fly,1}$ to $C_{fly,N}$) can be expressed by:

$$\begin{gathered} C_pV_{DD} + C_{fly,1}V_{fly,1} = (C_p + C_{fly,1})V_{F,1}, \\ C_pV_{F,1} + C_{fly,2}V_{fly,2} = (C_p + C_{fly,2})V_{F,2}, \\ \cdots\cdots \\ C_pV_{F,N} + C_{fly,N}V_{fly,N} = (C_p + C_{fly,N})V_{F,N}, \\ C_pV_{F,N+1} = 0, \end{gathered} \tag{3.15}$$

The recharge procedure from the ground to the supply can be expressed by the following equations:

$$\begin{gathered} C_p \times 0 + C_{fly,N}V_{fly,N} = (C_p + C_{fly,1})V_{F,N}, \\ C_pV_{F,3} + C_{fly,2}V_{fly,2} = (C_p + C_{fly,2})V_{F,2}, \\ \cdots\cdots \\ C_pV_{F,2} + C_{fly,1}V_{fly,1} = (C_p + C_{fly,1})V_{F,1}, \\ C_PV_{F,0} = C_PV_{DD}, \end{gathered} \tag{3.16}$$



Flying Caps	MATLAB	Circuit Simulation
$C_{fly,1}$	4.307V	4.327V
$C_{fly,2}$	3.692V	3.703V
$C_{fly,3}$	3.077V	3.088V
$C_{fly,4}$	2.461V	2.474V
$C_{fly,5}$	1.846V	1.860V
$C_{fly,6}$	1.231V	1.244V
$C_{fly,7}$	0.615V	0.623V

Figure 3.14: The simulated output waveform of a 7-cap stepwise circuit charging a capacitive load. The table shows the circuit-level simulation and MATLAB prediction results of the voltage level established on each flying capacitor when the load is being recharged. The switches are sized such that each step can settle more than 4τ (recharge to at least 98.2% of the final state).

The stepwise charging system is implemented in MATLAB and checked with circuit-level simulations. The circuit is tuned such that each pulse can have a settling time longer than 4τ. The waveform of 7-step charging is presented here. The simulated internal levels match with those from MATLAB with negligible error.

Driving a Transducer with Stepwise Circuit

To model the behavior of a stepwise circuit driving a transducer, several approximations need to be claimed at first:

(1) It is assumed that the stepwise waveform resembles a square wave with finite rising/falling speed. Since the resonator behaves as a band-pass filter, it is safe to further assume the fundamental power is delivered to the transducer while other harmonics are greatly suppressed.

(2) The power dissipated on R of the BVD model is 100% converted into the acoustic domain. In reality, the delivered power also includes the energy dissipated in the thermal domain.

(3) The gate capacitor C_g and the on-resistance R_{SW} scale linearly with the area of the transistor.

(4) The RLC branch would not have an impact on the charge-sharing process.

The modeling pipeline is described as follows. First of all, the inputs of the model include:

- **Technology-dependent parameters**: gate capacitance C_g and on-resistance $R_{SW,unit}$ of unit-size NMOS and PMOS switches, total capacitance budget (area budget of capacitance $\times$ capacitance density).

- **Transducer parameters**: characterized BVD model parameters for the transducer.
- **Design variables**: the number of flying capacitors N, the ratio between the rising time T_r and the oscillation period T.

The second thing is to estimate the power delivered to the transducer, which can be readily performed by Equation (3.8). Rewriting the equation here:

$$P_{R,SR} = \frac{2V_{DD}^2}{\pi^2 R} sinc^2\left(\frac{T_r}{T}\right) \tag{3.17}$$

The switching loss during stepwise charging can be approximated to the power loss to charge C_p from $V_{fly,1}$ to V_{DD}, where $V_{fly,1}$ can be derived by Equations (3.15) and (3.16). The power loss during charging and discharging C_p can be expressed by:

$$P_{SW} = C_p V_{DD} \Delta V f_{SW} = C_p V_{DD}(V_{DD} - V_{fly,1}) f_{SW}, \tag{3.18}$$

where $V_{fly,1}$ is the established voltage level on $C_{fly,1}$ when the charge-sharing process is stable, and ΔV is the potential difference between the supply and the steady voltage established on $C_{fly,1}$.

The last step is to model the gate-charge loss during stepwise charging. Although the gate capacitance for a unit-size switch is much lower than C_p as discussed previously, the gate-charge loss cannot be neglected when modeling the stepwise charging, as the size of each switch highly depends on the slew rate. For example, if the slew rate is fast, but the switches are small, the stepwise charging can not settle properly to save loss on C_p. This is the same case for other types of switched-mode pulser. Assuming the rising time is T_r, with N flying caps, the pulse width for each step would be:

$$T_P = \frac{T_r}{N+1}. \tag{3.19}$$

To make sure the charge sharing in the internal level settles properly to form a stepwise waveform, a sharing time of 4τ, which means settling to 98.2% of the final level, is set for each short pulse. The relationship between Equations (3.14) and (3.19) can be expressed by:

$$\tau = \frac{T_P}{N_\tau} = \frac{T_r}{N_\tau(N+1)} = \frac{R_{SW} C_p \Phi_{CAP}}{1 + \Phi_{CAP}}, \tag{3.20}$$

where N_τ is the number of τ spent to settle each step. Since N, T_r, and Φ_{CAP} are design parameters, an average R_{SW} for each level can be estimated by:

$$R_{SW} = \frac{T_r(1 + \Phi_{CAP})}{N_\tau C_p \Phi_{CAP}(N+1)}. \tag{3.21}$$

After determining the average on-resistance, the gate capacitance on each switch can be estimated by

$$C_{g,SW} = \frac{R_{SW,unit}}{R_{SW}} C_{g,unit}. \tag{3.22}$$

The on-resistance R_{SW} of the switch can be modulated by the gate-to-source voltage, V_{GS}. For example, for a square-law device [90], R_{SW} has the relation of

$$R_{SW} \propto \frac{1}{\lambda \frac{W}{L}(V_{GS} - V_{TH})^2}, \tag{3.23}$$

where λ is the channel-length-modulation coefficient and V_{TH} is the threshold voltage of the switch.

The on-resistance variation must be compensated by increasing the switch sizes from S_{N+1} to S_2. This necessity arises due to the linear variation in voltage on each flying capacitor as the step transitions from the bottom to the top level, illustrated in Fig. 3.14. Assuming constant channel lengths, threshold voltages, pulse widths, and switch driver supply levels, the V_{GS} of each switch would also exhibit a linear variation from S_{N+1} to S_2. Suppose the sizes of all switches remain the same. In that case, the on-resistance of the higher-level switches will increase proportionally with the square of $V_{GS} - V_{TH}$, leading to a significantly slower charge-sharing process between C_p and higher-level flying capacitors. In this case, the voltage level established on each flying capacitor would decrease, further degrading the loss saved from C_p.

Increasing the switch size leads to a bigger gate capacitance that needs to be charged. The total gate capacitance can be roughly estimated by summing a sequence of squares:

$$C_{g,tot} \approx C_{g,SW} \times (1^2 + 2^2 + 3^2 + \cdots + N^2) = C_{g,SW} \times \frac{N(N+1)(2N+1)}{6}. \tag{3.24}$$

The total gate-charge loss can then be calculated by:

$$P_{Q,tot} = C_{g,tot} V_{DD}^2 f_{SW} = C_{g,SW} V_{DD}^2 \times 2f_s \times \frac{N(N+1)(2N+1)}{6}, \tag{3.25}$$

where f_{SW} is the switching frequency of the stepwise switches. Each switch would open and close twice within one oscillation cycle, thus, $f_{SW} = 2f_s$.

The final acoustic efficiency for a stepwise charging-sharing circuit driving an ultrasound transducer can be expressed by:

$$\eta_R = \frac{P_R}{P_R + P_{SW} + P_{Q,tot}} \times 100\%. \tag{3.26}$$

Another figure of merit "C_p loss saving" discussed in many other publications [48, 52, 91], where they only consider saving as much energy loss on C_p as possible, can be calculated as follows:

$$\eta_Q = \frac{C_p V_{DD}^2 f_s - P_{SW} - P_{Q,tot}}{C_p V_{DD}^2 f_s} \times 100\%. \tag{3.27}$$

Limitations of the Model

The main non-ideality of this model is that the motional branch continuously draws current from the capacitor tank during the stepwise charging process. The current supplied by the flying capacitors can lead to extra conduction loss in each switch. As

a result, the voltage level established on each capacitor will always be lower than it would be with a pure capacitive load. These non-idealities result in a lower voltage level established on the top flying capacitor, leading to less overall C_p loss saving.

The effect of the current drawn by the RLC branch can indeed be challenging to model. This is because charge sharing and RLC conduction occur simultaneously, making it impossible to apply the conservation law of charge as a straightforward principle.

The error introduced by the current on the motional branch plays a more significant role when the rising edge of the stepwise waveform is slow, meaning that more time is spent on the stepwise charging process, thus, more power established on flying capacitors is lost. This suggests that the optimal design point may move slightly to a faster rising time in order to compensate for the extra loss on C_{fly}.

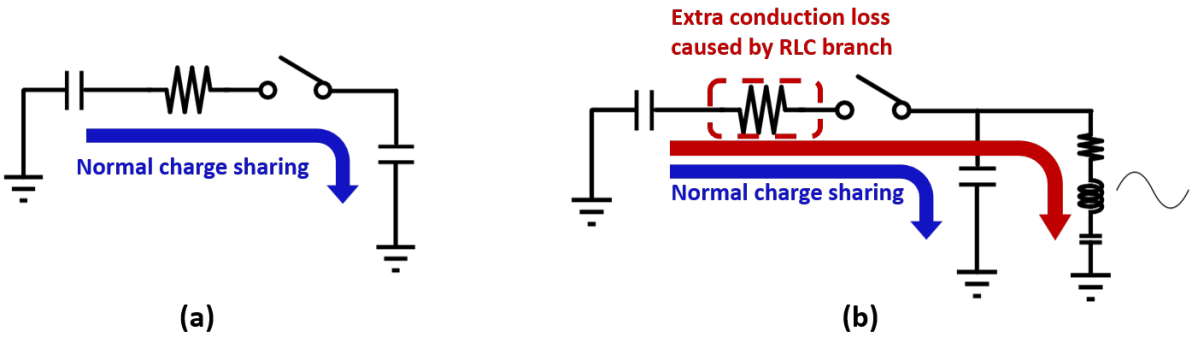


Figure 3.15: The difference between the stepwise charging of a capacitive load and of a transducer, (a) the stepwise charging of a capacitive load can be fully modeled by the conservation of charge, (b) the case is more complicated for the stepwise charging of a transducer, as the RLC branch draws current from the flying capacitors as well.

There are other minor non-idealities. For example, the gate capacitance and on-resistance do not scale linearly with transistor size due to the second-order effect of the device, and also, there would be non-idealities introduced during the physical fabrication of transistors. However, this model is safe to give a rough estimation of the optimal design choice with a limited capacitance budget, as it already takes into account all the major losses in switched-mode PA as analyzed in the previous section.

3.2.3. Stepwise Pulser Circuit Design

The model built in the previous section can significantly accelerate the circuit design of a miniaturized stepwise pulser. This model effectively approximates all associated losses while accounting for the capacitance budget of the transmit channel. The model is built in MATLAB and visualized in Fig. 3.16 and Fig. 3.17. Two notable observations can be derived from the results:

(1) **High C_p loss saving and high energy efficiency may not be synonymous design goals for switched-mode pulsers**: The figures demonstrate that C_p loss saving in switched-mode PAs driving a transducer is primarily related to the number of implemented levels. As long as the saved loss with each additional step surpasses the introduced gate-charge loss, it is feasible to use numerous steps

to achieve high C_p loss savings, as in [59]. However, in scenarios where high acoustic efficiency is in demand and delivering more power to the resistive load is a priority, the rising and falling edges of the driving signal should be considered properly. This trade-off can be observed in Fig. 3.17, where the top view of the performance surface is separated into different divisions. The estimated design choice for high acoustic efficiency and high C_p loss saving is in markedly different divisions.

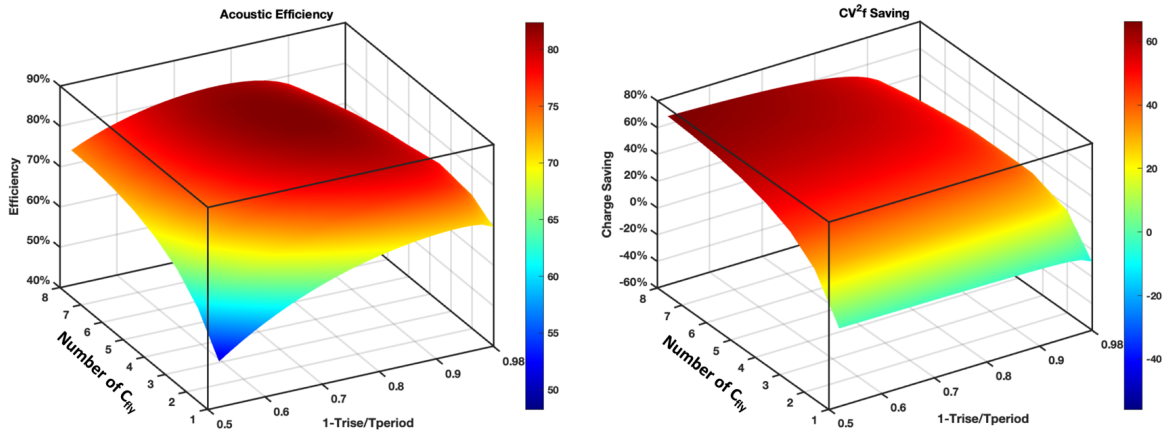


Figure 3.16: 3-D surface of acoustic efficiency and C_p loss saving versus different numbers of flying capacitors and rising-time-to-oscillation-period ratio.

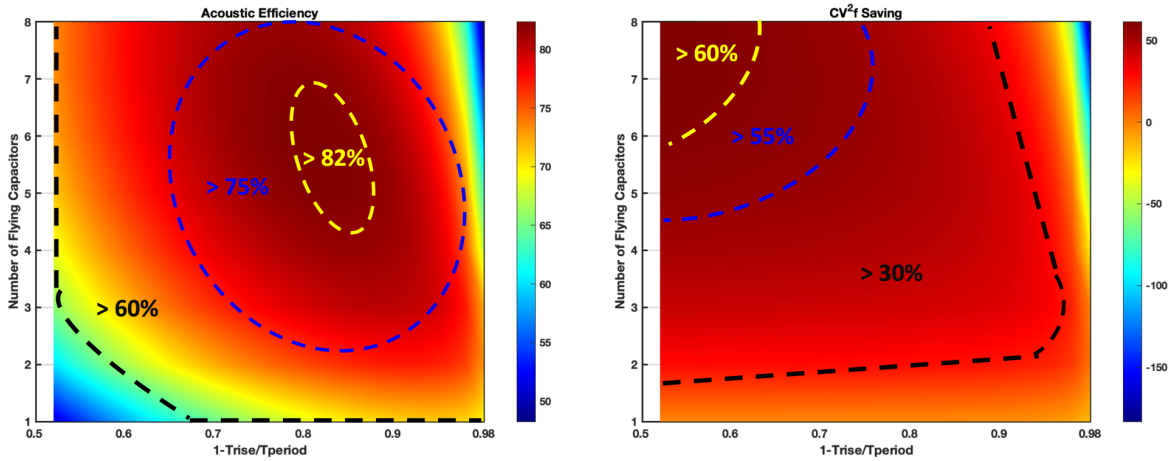
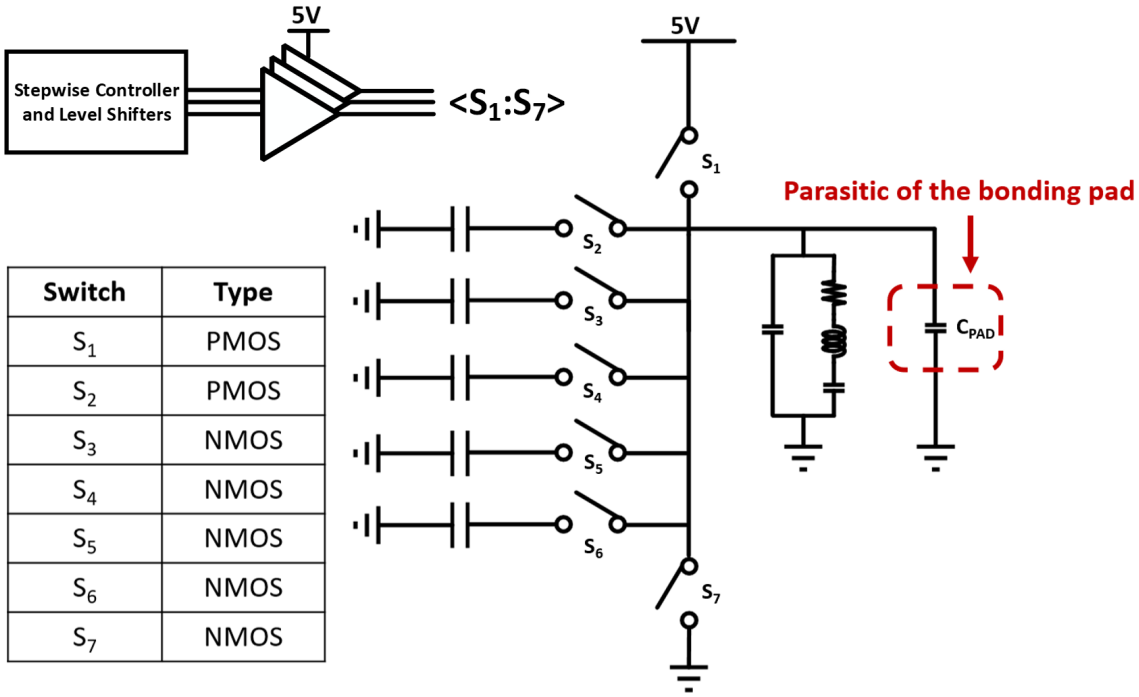


Figure 3.17: Top view of the 3-D surface of acoustic efficiency and C_p loss saving versus different numbers of flying capacitors and rising-time-to-oscillation-period ratio.

(2) **The total efficiency of the pulser exhibits an optimal trade-off between the number of stepwise levels introduced and the pulse width of each step**: in general, implementing more levels of stepwise charging would save more power loss on C_p, and aiming for a faster rising edge would deliver more power to the resistive load. However, more levels and faster step intervals would introduce more gate-charge loss. The proposed model is able to estimate a more optimal trade-off between these major losses within a limited area budget.

Finally, the transistor-level design choices can be roughly determined. A stepwise pulser featuring five flying capacitors (N = 5) and a cap ratio of 3 (~40% of channel area budget using MOSCAP) is designed. The switches that control the sharing of each flying capacitor are sized to have increased W/L ratios from the bottom to the top level. To maximize the output swing, S_1 and S_2 are implemented using PMOS switches. Additionally, to optimize the output resistance of the PA, the sizes of switches S_1 and S_7 are further increased to reduce the R_{OUT}, as analyzed in Equation (3.6) and depicted in Fig. 3.4.

3.2.4. Simulation Results



Switch	Type
S_1	PMOS
S_2	PMOS
S_3	NMOS
S_4	NMOS
S_5	NMOS
S_6	NMOS
S_7	NMOS

Figure 3.18: Testbench of the 5-caps stepwise pulser and the type of each switch.

The testbench of the pulser is shown in Fig. 3.18, and the types of switches used are denoted as well. The transmission gates, a commonly-used type of low-voltage switches, are not used as switches in this design, even though they can mitigate the on-resistance variation introduced by V_{GS}. It is because the supply domain of the PA is in 5V, not technically a low-voltage domain in the used technology. Extra 5V switches and 5V inverters are brought together with transmission gates, which are area-consuming and can introduce extra gate-charge loss. A stepwise PA with 5 flying capacitors is used to drive an ultrasonic transducer. To account for the non-ideality of the wire-bonding pad, a 500 fF C_{PAD} is added in parallel with the BVD model. The exact capacitance value extracted from the 5V I/O pad layout is 367 fF. A parasitic capacitor of 500 fF is taken here to leave some margin. The non-overlapping control signals for each switch are generated from the stepwise controller with level shifters, which will be discussed in the following sections. The control signals are buffered to drive S_1 to S_7, within which S_1 and S_2 are PMOS switches, and the rest are NMOS switches. S_1 and S_7 should be particularly large to reduce the equivalent output resistance of the PA.

The size of NMOS switches should follow the pattern $S_3 > S_4 > S_5 > S_6$ to compensate for on-resistance variation due to differences in V_{GS}. Each buffer is sized according to the size of each switch to have balanced driving capabilities.

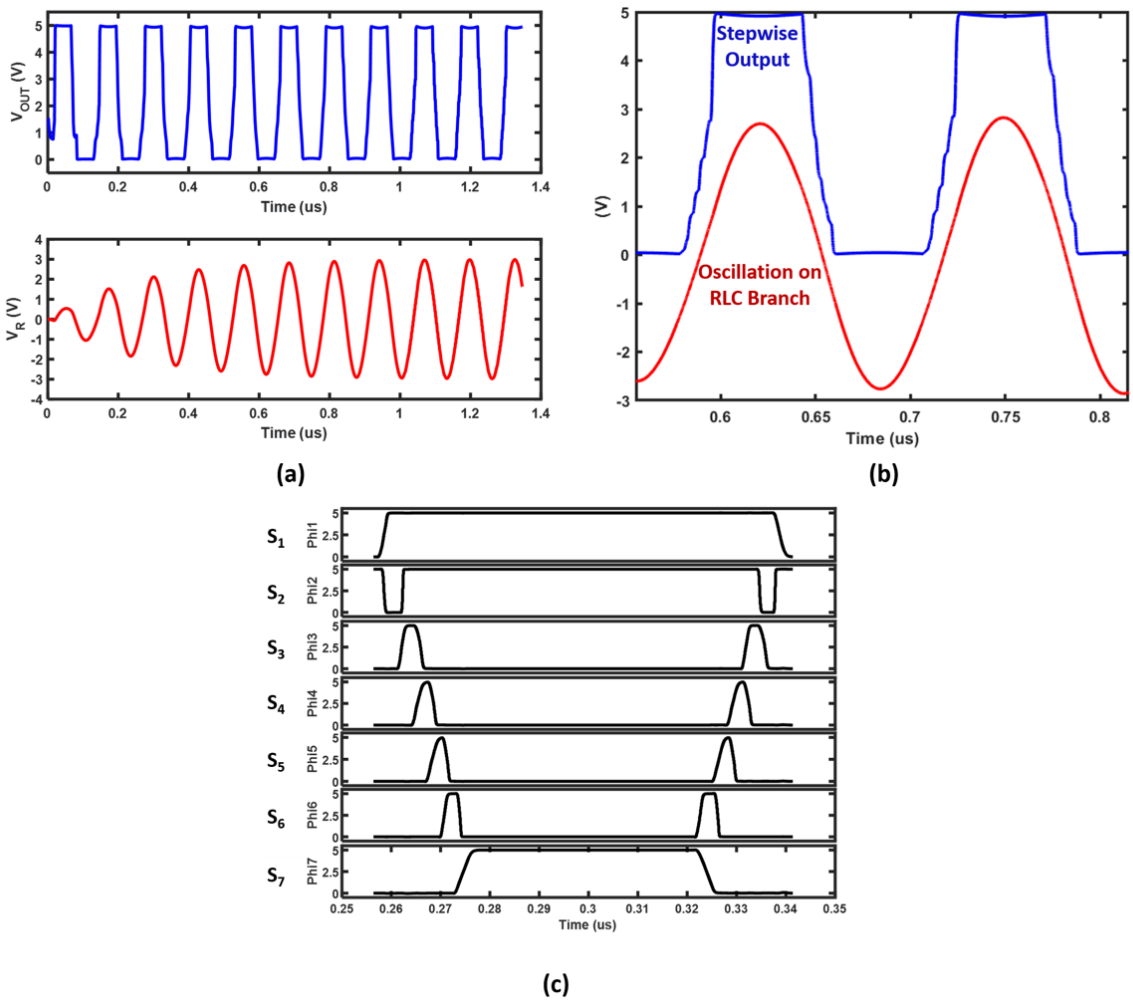


Figure 3.19: The output and timing control waveform of the stepwise pulser with a reference frequency of 7.8 MHz, (a) startup waveform at the output of the stepwise PA, (b) the stepwise waveform when the stepwise circuit is table, (c) the timing waveform of each switch.

The output waveform of the stepwise pulser and the timing diagram of S_1 to S_7 are depicted in Fig. 3.19. This stepwise pulser can provide a fast response with a start-up time of approximately 5 switching cycles. The control timing of each switch is depicted in Fig. 3.19 (c). Sizing the corresponding buffer to ensure that PMOS switches S_1 and S_2 do not turn on simultaneously is crucial, as it would cause extra conduction losses on S_1 and S_2 when the supply is directly connected to $C_{fly,1}$. On the other hand, slight overlaps in the other clock phases are acceptable. The supply is not engaged in these phases, so any possible phase overlap would have minimal impact on the efficiency of the PA. This is because the equivalent on-resistance and capacitance seen from the C_{fly} roughly double when the adjacent sharing channels are connected. Consequently, the increased time constant τ slows down the charge sharing, making the associated power loss less critical.

The total PA power consumption is calculated by integrating the current on the 5V supply and taking the average over time. The power delivered to the resistive part of the load is obtained by calculating the average power of 7.8 MHz oscillation on the resistive part of the load. After the transistor-level optimization, it is found that the optimal T_r/T ratio tends to be smaller (faster rising/falling edge), which also aligns with the analysis regarding model non-idealities in the previous section. Excluding the power consumptions on level shifters and the stepwise controller, the stepwise PA efficiency is simulated to be 84.6% at the typical corner.

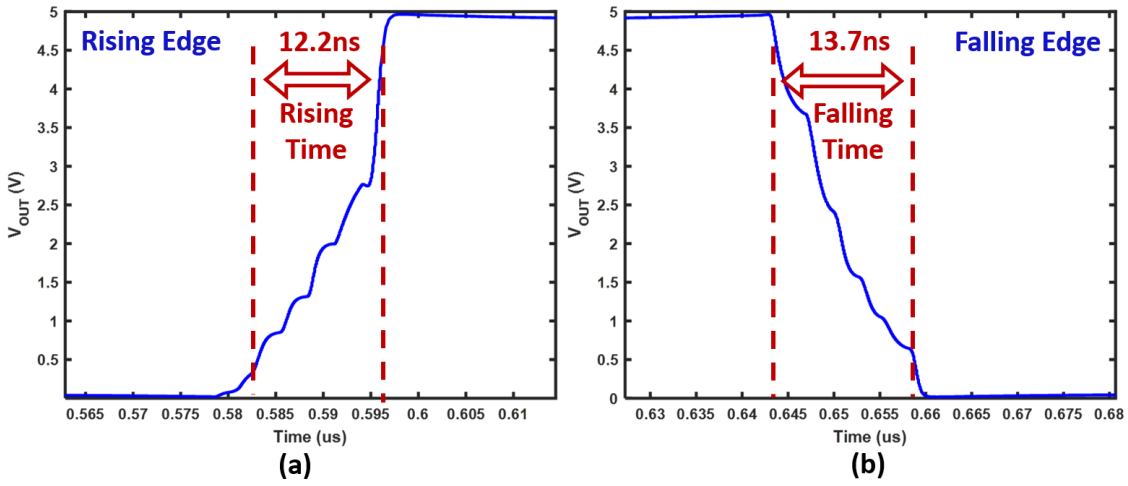


Figure 3.20: The rising edge and falling edge of the stepwise output. Transistor mismatch would introduce a rising/falling time mismatch.

The mismatch of the switches would introduce variations in rising/falling time as illustrated in Fig. 3.20. This can potentially affect the pulser efficiency and phase alignment of the beamforming control. However, this mismatch would not have a significant impact on either the efficiency or phase alignment of the PA, as will be demonstrated later in the next chapter on circuit design results.

The achieved performance for the stepwise PA is summarized in Table 3.1.

Pulser Performance	Estimated	Achieved
[1]**Acoustic Efficiency**	> 82%	84.6%
Output Power / Channel	1.93 mW	1.85 mW
Rising Time Tr	~ 19.23 ns	12.2 ns
Falling Time Tf	~ 19.23 ns	13.7 ns
Tr/T	~ 15%	9.5%
Tf/T	~ 15%	10.7%
Cp Loss Saving	~ 50%	54.4%

[1] The power consumption includes both power dissipated by the stepwise PA and 5V buffers.

Table 3.1: Estimated stepwise pulser performance using MATLAB model and the achieved result with transistor-level design.

3.3. Level Shifter

In modern semiconductor chipset designs, seamless cooperation between different supply voltage domains is essential. The level shifter (LS) is the bridge for the signal to communicate between different supply domains. In the context of this work, driving the transducer at 5V is required to produce the desired pressure within the target area. As shown in Fig. 3.21, the LS of this work should convert the 1.5V timing signal to the 5V domain in order to drive the stepwise PA. This section focuses on the design of the level shifter.

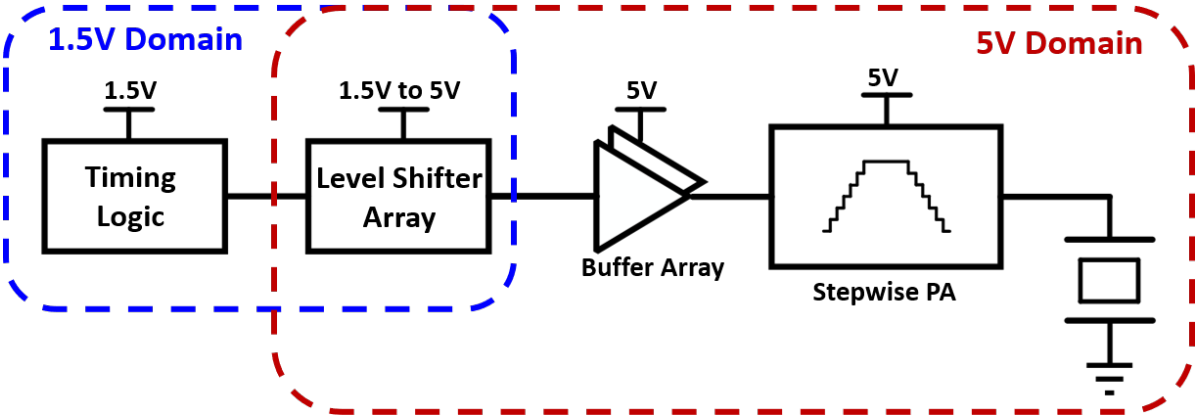


Figure 3.21: Different voltage domains of the stepwise PA signal chain.

3.3.1. Topologies

Fig. 3.22 demonstrates two conventional architectures for level-shifting circuits. In sub-diagram (a), the cross-coupled LS is depicted. The input signal comes from the low-voltage domain. When a low-to-high transition occurs at the input, the MN_1 transistor turns on, pulling its drain terminal down to the ground. Consequently, the cross-coupled PMOS MP_2 on the output branch enters the triode region, causing the output signal to rise to the high-voltage supply level. During this phase, the output of the low-voltage inverter transitions from high to low with a delay shorter than the output's rise time. This transition turns MN_2 off, thus enhancing the speed of the output node during the pull-up phase. However, if the driving strength of the PMOS transistor significantly exceeds that of the NMOS, the output node may fail to discharge to the ground. This design challenge, known as contention, becomes particularly critical when converting signals from a below-1V supply domain [92].

Diagram (b) illustrates the structure of a current-mirror-based level shifter. When a signal transitions from low to high at the input, a change of current is generated in the input branch, which is then mirrored to the output branch to charge the output node. This approach alleviates the contention problem by current-mode control. However, a large static current is presented when the input signal is high, resulting in an increased overall power consumption. In general, assuming equivalent output capacitances and output swings, the current-source-based approach is considered less energy-efficient. This is primarily due to its inherent presence of static current.

In addition to the contention problem and power consumption, another concern is the variation in delay time within the level-shifting path. The low-to-high transition

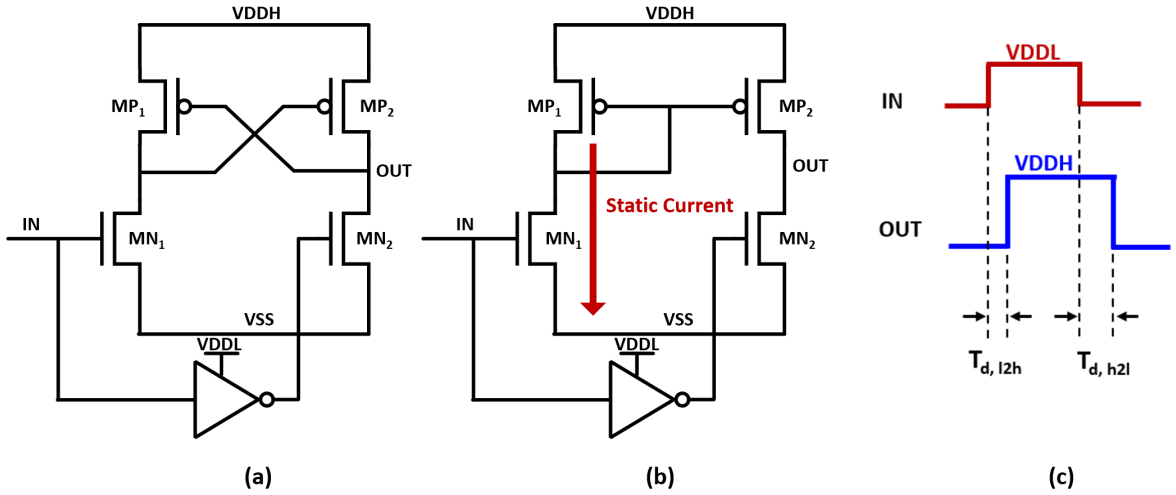


Figure 3.22: Conventional level-shifter topologies, (a) cross-coupled LS, fast but power consuming, (b) current-mirror-based level shifter, less contention problem, but a large static current exists when input is high, (c) the timing of single-ended output LS, the delay $T_{d,l2h}$ and $T_{d,h2l}$ are not always equal.

delay $T_{d,l2h}$ can differ significantly from the delay for high-to-low transitions $T_{d,h2l}$. For example, in the case of the cross-coupled structure, $T_{d,l2h}$ is influenced by the time it takes for MN_1 and MP_2 to turn on, while $T_{d,h2l}$ is determined by the time for the low-voltage inverter to inverse the signal and turn on MN_2. These two delay values may also vary based on the sizing of the transistors used, which further affects the power consumption of the level shifter.

3.3.2. Design Choice

The primary design goal for the PA signal chain is centered around achieving optimal power efficiency. This entails not only the efficient driving of the transducer but also the minimized power consumption of the peripheral circuits. This section focuses on the design choice for the level-shifting channel.

Low Power

As discussed previously, the cross-coupled LS offers better energy efficiency when compared to the current-source-based configuration. This advantage is mainly due to the elimination of static current. However, it does suffer from contention if not properly designed.

Previous works [93, 94] have combined the cross-coupled and current-mirror-based LS to strike a balance between power, delay, and voltage swing for ultra-low-power and ultra-low-input applications.

In the scope of this study, the primary goal is to achieve low power consumption during voltage transitions. Specifically, the desired input signal swing is 1.5 V, while the expected output swing is 5V, leading to a voltage-conversion ratio of approximately 3.3. In comparison to other works [93–95], these specifications fall outside the ultra-low-input range, which typically involves inputs below 1V and conversion ratios larger than 10. Besides, the level-shifter power is relatively low compared to other power losses in the PA as reported in [63, 64]. Therefore, there is no need to overcomplicate the design considerations of low-power LS.

Low Area

When considering area constraints, prior works have proposed different LS topologies, with the number of high-voltage transistors ranging from 4 up to 18 [93–95]. It's important to note that high-voltage transistors occupy a considerable amount of silicon area. The area of a 5V transistor is around 50% larger than that of a 1.5V transistor in the technology used in this work.

The stepwise pulser in this work comprises 7 switches, and each switch necessitates a dedicated level-shifting channel. Employing an 18-transistor structure, as in [95], would result in unnecessary use in the silicon area. As both power consumption and silicon cost are important design considerations, the design in [96] is adopted in this work. This design uses 10 high-voltage transistors (including an output high-voltage out buffer), almost half the size compared to [95], while still achieving significant power reduction compared to other topologies as reported in the paper.

The schematic of the topology used is depicted in Fig. 3.23. The input pair, MN_1 and MN_2, is the same as can be found in conventional level shifters. The regulated cross-coupled (RCC) pull-up network serves to limit the maximum voltage level at node Q_P to one threshold below the high-voltage supply. This voltage reduction at internal node Q_P reduces the power of the level-shifting path. Besides, a diode-connected PMOS pair, of which the equivalent resistance is $\frac{1}{g_m}$, is added between the pull-up and pull-down network to create a potential difference between node Q_P and node Q_N. By tuning the equivalent resistance of this pair of current limiters, the simultaneous conduction of MP_{OUT} and MN_{OUT} transistors can be greatly suppressed, further reducing the power consumption of the output buffer.

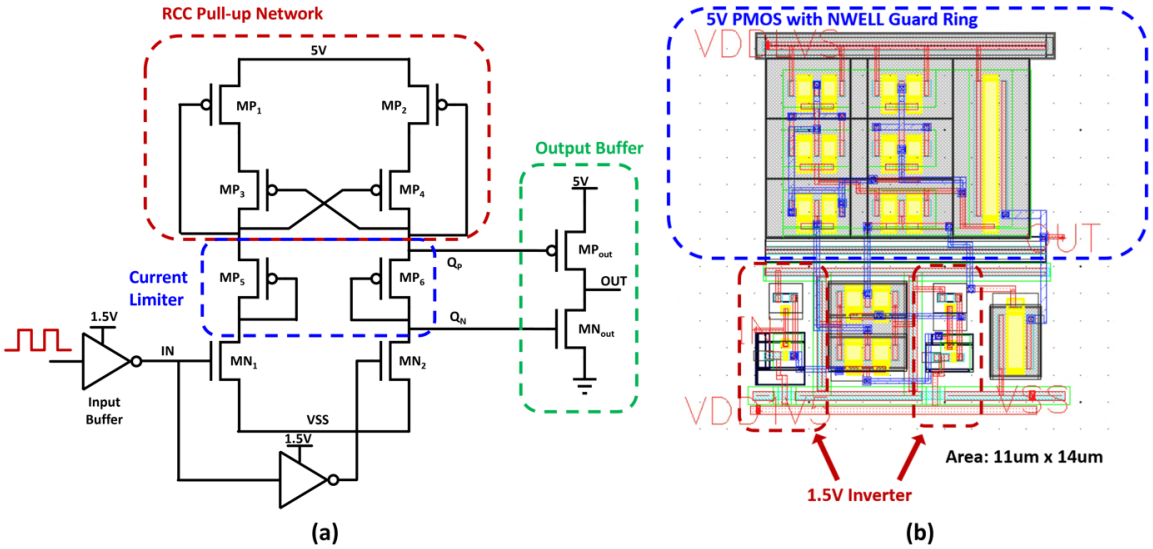


Figure 3.23: Regulated cross-coupled level shifter with current limiter [96], (a) schematic of the level shifter, (b) layout of the level shifter.

3.3.3. Simulation Results

The pre-layout and post-layout simulation waveforms for the chosen topology are shown in Fig. 3.24. A reference signal with a 1.5V peak-to-peak swing and 50%

duty cycle is provided as the input to test the circuit operation. The output signal can be shifted to 5V with several μWs of power. Due to the delay difference in the rising and falling edges, the level shifter would introduce a 900 ps mismatch in the on-time.

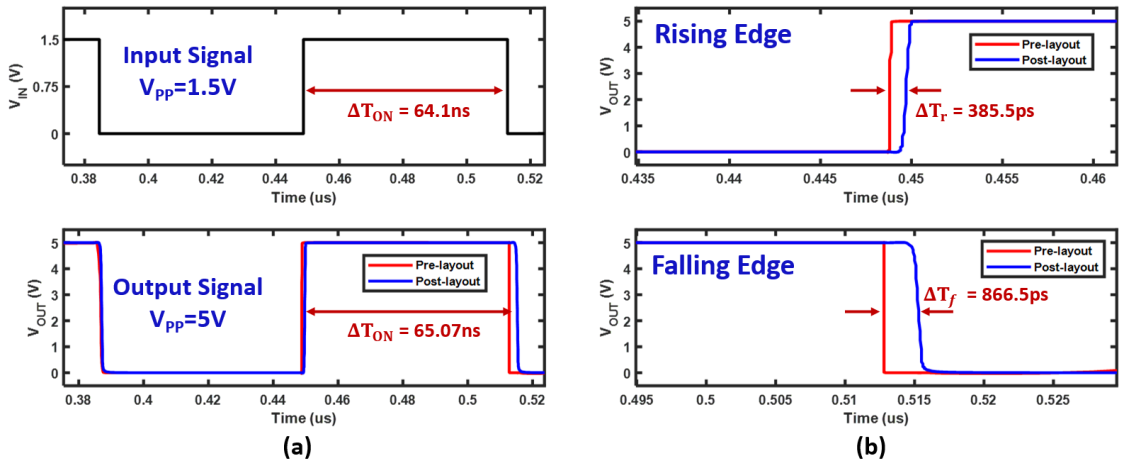


Figure 3.24: Simulation results of the level shifter.

The size of the level-shifting channels and the output buffers are optimized according to the sizes of stepwise charge-sharing switches. The layout of the biggest level-shifting channel (for S_1 in Fig. 3.18) is shown in Fig. 3.23, which occupies an area of about 11 μm x 14 μm. The transistors and metal routing of the input buffer, MN_1, MN_2, MP_1 to MP_6 are made as symmetrical as possible. However, since this is a single-ended output structure, the layout introduces approximately 400 ps of rising- and falling-edge variation, as can be seen from Fig. 3.24(b). The power consumption of the level shifter is simulated to be 1.7 μW per channel with the stepwise timing diagram in Fig. 3.19(b). When driving the same switch, the power consumption is 2x lower than that of the cross-coupled LS, 2.2x lower than a current-mode LS driving an NMOS, and drastically lower (100x) when driving a PMOS switch. This substantial reduction is attributed to the larger duty cycle of the PMOS driving signal as shown in Fig. 3.19.

3.4. Stepwise Sequencer

3.4.1. Motivation

The motivation for this sequencer design is to enable stepwise charging with the same clocking routing configuration without adding extra reference sources, as depicted in Fig. 3.25.

For conventional class-D ultrasonic PA design, it is common practice to use an external reference signal with frequency f_{ref}, configured to match the transducer's series-resonance frequency f_s. This allows for the simple and synchronous switching of the PA to enable beamforming without the need for additional reference sources while achieving compact array integration.

Generating precise control signals for short pulses on each step in a stepwise PA can be challenging, especially for low-power applications. A straightforward tim-

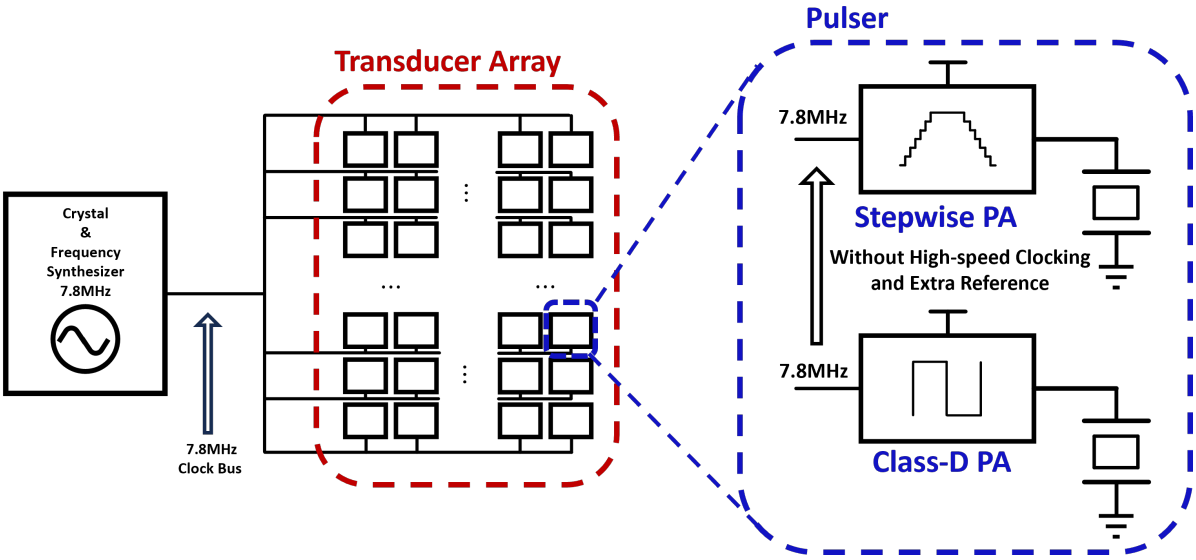


Figure 3.25: Clock routing for the transducer array. The motivation is to enable high-efficiency stepwise PA with the same routing resource as class-D PA for beamforming purposes.

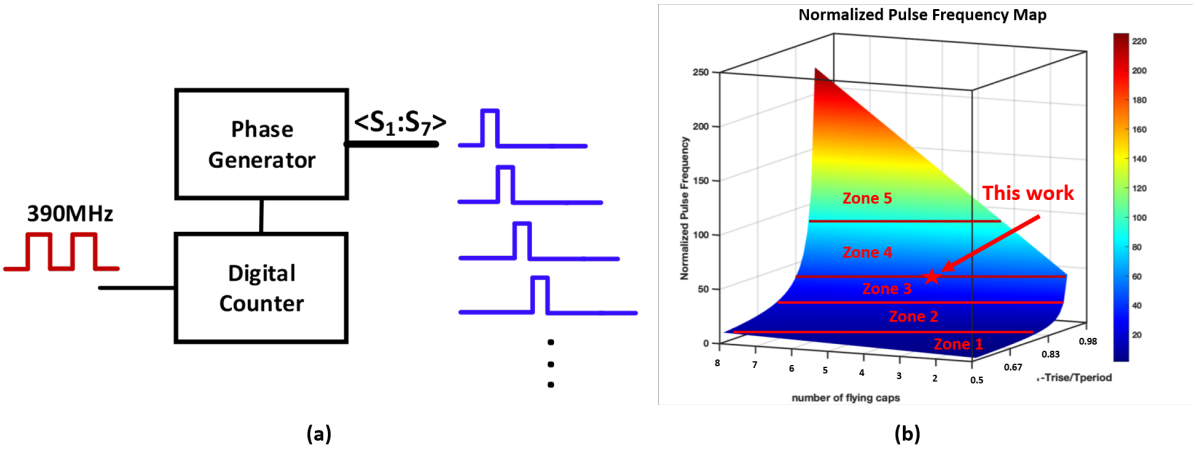


Figure 3.26: (a) Generation of short pulses using a digital counter. The required reference frequency estimated in MATLAB is around 390 MHz (T_r/T = 15%) for the stepwise PA design in this work, the actual frequency in circuit design is 468 MHz ($T_r/T \sim$ 10%). (b) The surface of normalized pulse frequency f_{ref} to transducer frequency f_s with different T_r/T ratios and numbers of flying capacitors. Zone 1: f_{ref} is below $10f_s$; Zone 2: f_{ref} ranges from $10f_s$ to $25f_s$; Zone 3: f_{ref} ranges from $25f_s$ to $50f_s$; Zone 4: f_{ref} ranges from $50f_s$ to $100f_s$; Zone 5: f_{ref} is above $100f_s$

ing method involves injecting a reference signal with a frequency equal to that of the short stepwise pulses into a digital counter and a phase generator as illustrated in Fig. 3.26(a). The stepwise-timing waveforms can then be readily produced. However, depending on the T_r/T ratio and number of steps introduced, this approach requires a clocking signal tens or even hundreds of times faster than the f_s of the transducer. Fig. 3.26 shows the normalized pulse-frequency map with different T_r/T ratios and numbers of flying capacitors. This presents challenges in high-speed clock routing and distribution for massive array fabrication, as higher-speed clock routing needs more power spent on local buffers to recover the clocking signal and ensure the alignment of clock phases between each channel [97].

	ISSCC'17 [57]	**JSSC'22 [46]**	**ESSCIRC'21 [63]**	**TCAS-II'21 [64]**
Process	45 nm	180 nm	180 nm	180 nm
†**Reference**	$5f_s$ Off-chip PLL	$4f_s$ External	f_s=780 kHz External	f_s=1 MHz External
Phase Generator	Ring OSC	In-channel DLL	Full Digital	Delay Line + Digital
Tr/T	24%	25%	20%	19.5%
ᵀ**Power/channel**	N.A.	N.A.	140 μW	70 μW

† Reference clock that feeds into the digital logic.
ᵀ Measured power dissipation to control the stepwise circuit.

Table 3.2: Performance of stepwise waveform controllers in prior arts.

Table 3.2 provides the performance of stepwise controllers for different stepwise PAs [46, 57, 63, 64], including details such as the reference clock frequency, phase generation method, T_r/T ratio, and the power dissipated on the timing controller per channel. These works prefer to use full-digital phase generators or delay-locked loops (DLLs) to generate the required control signals for stepwise PAs, as their total power consumption is in the tens and hundreds mW range per channel, making the digital power negligible. However, conventional delay lines or DLLs are usually power-consuming and may require extra reference sources [46]. The power dissipation of the controller is approximately 100 μW per channel in these works.

In our application, where the area is constrained and the output power per channel is around or below 1 or 2 mW, saving digital power and reducing the area consumed by the delay line can further enhance PA performance. This section introduces the design of an area-efficient self-timed sequencer for a stepwise PA to reduce the power and area consumption further.

3.4.2. Topologies

Conventional approach

The conventional approach to generating high-frequency timing signals using a low-frequency reference typically involves delay lines, as illustrated in Fig. 3.27. The input clock reference undergoes a series of inverter stages, and the adjacent phases within the delay line are processed by XOR operations to produce high-frequency pulses.

This approach is inherently simple and extensively used in modern IC design [98], but it has certain limitations on self-timing applications. For instance, in [46], where 14 clock phases are needed to control the stepwise PA, using a delay line would require

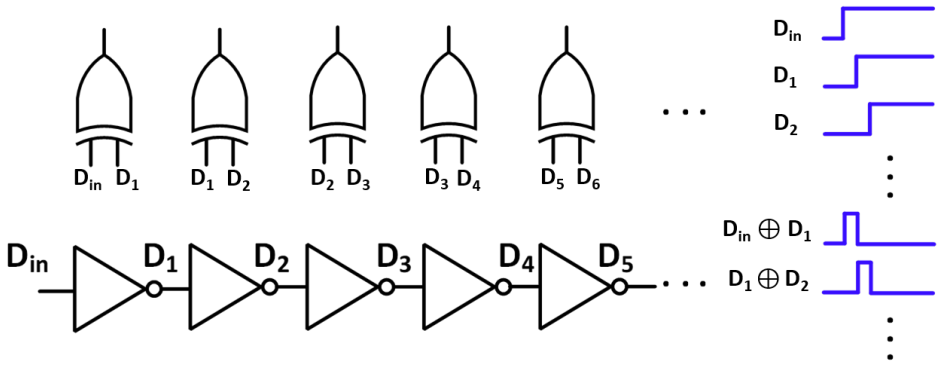


Figure 3.27: Conventional delay line to generate high-frequency pulses.

at least 14 stages of delay cells. This can become problematic when the required pulse frequency is in the range of hundreds of MHz, as the equivalent RC constant of the delay cell needs to be large enough to provide the delay, increasing both power and area consumption [99].

Delay Cell with Feedback

The delay cell with a feedback structure in Fig. 3.28 is an effective approach to reducing the number of delay cells in a timing circuit. The feedback loop would initiate self-oscillation when a reference signal triggers the control logic. The oscillation frequency depends on the delay cell, and the clock can be extracted by a regenerative buffer and fed to a phase generator to produce different phases.

This architecture is effective in reducing the power and area in timing circuits, making it widely used in various applications such as low-power ADCs [100], micro-energy harvesting [101], and low-power, low-area clock references [41].

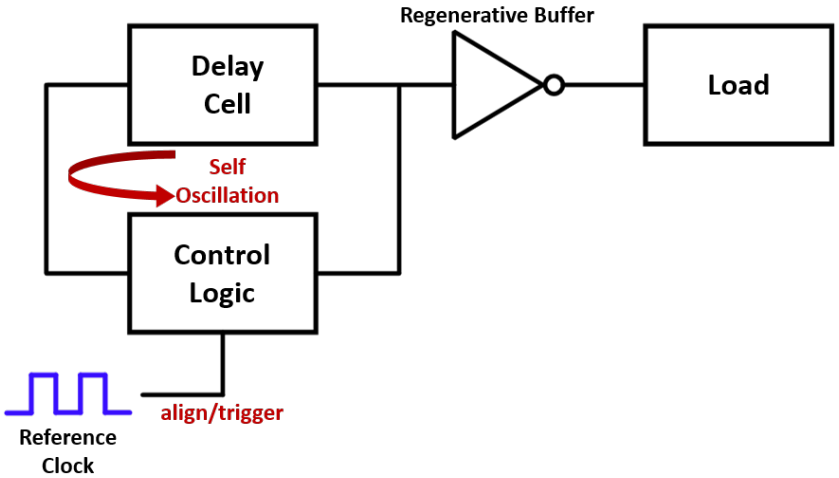


Figure 3.28: Delay cell with feedback architecture for self-timing application.

The core block for this architecture is the delay cell, which controls the timing of oscillation and determines the power consumption. A popular approach to implement a low-power delay unit in both academia [91] and industry [102] is by using a precision current source I_{ref} to charge a capacitor C as shown in Fig. 3.29. A comparator

with a reference voltage V_{ref} is used to detect the voltage level on the capacitor. This approach can achieve low power consumption and high-precision delay tuning expressed by Equation (3.28). However, extra reference circuitry and routing are needed for this design.

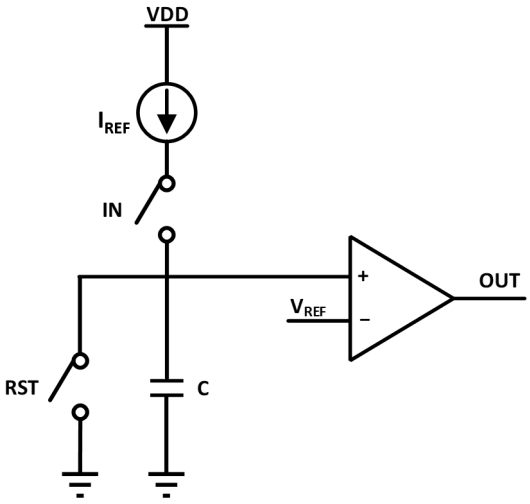


Figure 3.29: Current-source-based delay cell.

$$T_d = \frac{CV_{ref}}{I_{ref}} \tag{3.28}$$

In low-power applications where precision is not of high priority, the ring oscillator dominates the implementation of timing circuits. The fundamental structure of a single-ended ring oscillator is shown in Fig. 3.30. An odd number of inverter-based delay stages is cascaded in a loop to enable oscillation [103]. The oscillation frequency can be determined by the number of delay stages N and the delay T_d of each stage:

$$f_{osc} = \frac{1}{2NT_d}. \tag{3.29}$$

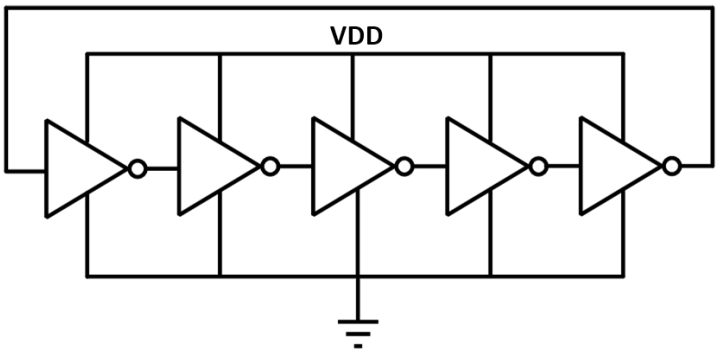


Figure 3.30: Conventional single-ended ring oscillator.

To reduce the power consumption of the inverter-based delay stage, supply-modulated delay cells are proposed to produce longer delay with the same area and power budget. Fig. 3.31 shows two different approaches to modulating the supply of delay cells. However, still, extra circuitry and references are still needed for these designs.

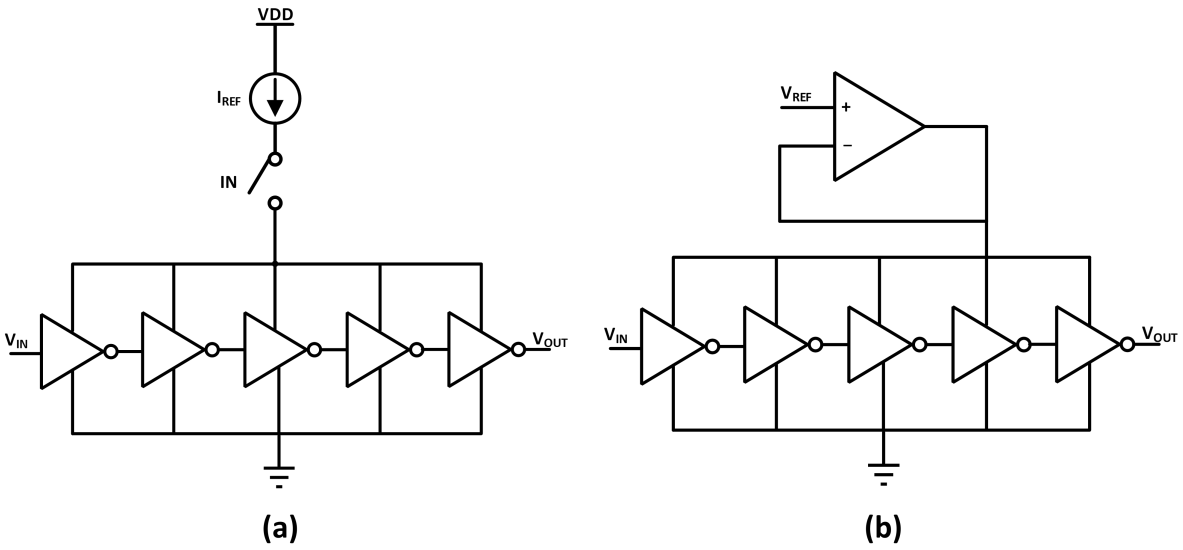


Figure 3.31: Two types of supply-modulated inverter-based delay cells, (a) current-mode delay cell, or so-called current-starved inverter [104], (b) voltage-mode delay cell with regulative amplifier [105].

3.4.3. Proposed Design

To achieve further reductions in area and power for the stepwise timing circuit, as well as a compact reference-free PA that resembles a conventional class-D mode driver, this work proposes a symmetrically-modulated delay line to implement a local oscillator (LO). The simplified diagram is shown in Fig. 3.32.

The idea of this circuit is inspired by the delay-cell structure in Fig. 3.31(b) [105], where an amplifier modulates the supply voltage of the inverter delay line by means of negative feedback. This modulation lowers the supply voltage of the delay cell, reducing the current used to charge each delay stage. Consequently, this circuit can produce a longer delay with lower power consumption.

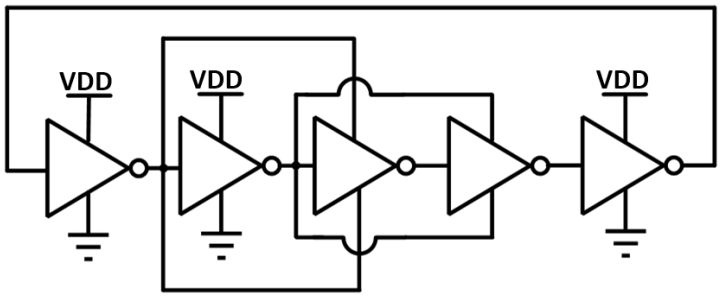


Figure 3.32: Proposed symmetrically-modulated ring oscillator.

The equivalent circuit of the proposed delay cell during pull up and pull down is depicted in Fig. 3.33. Instead of using an amplifier in feedback mode, the supply and the ground of stages 3 and 4 of the delay chain are symmetrically self-modulated by the output of stages 1 and 2. The equivalent resistance at the output nodes of stages 3 and 4 is roughly doubled compared to the normal inverter delay cell. At the same time, the equivalent capacitance seen at these nodes remains the input capacitance of the following stage. In this case, the power dissipation of this delay cell stays almost

the same compared to the regular inverter-based delay line, but a longer delay can be generated. The fifth inverter stage serves as a regenerative buffer to recover the signal to full swing.

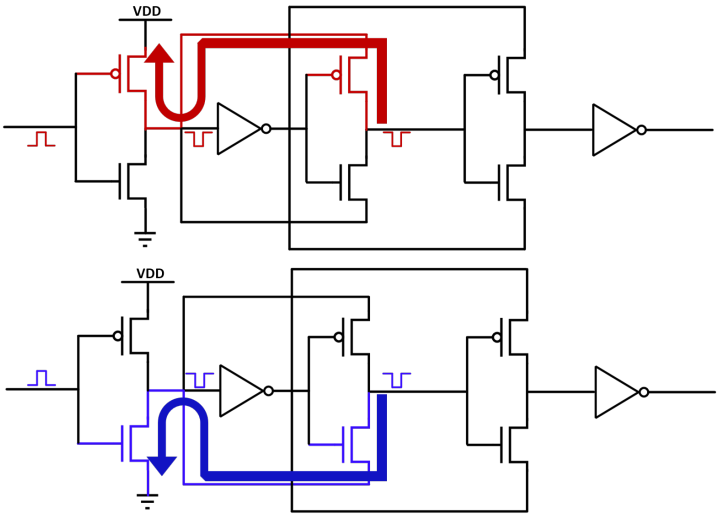


Figure 3.33: Equivalent circuit of the proposed symmetric supply modulated delay cell. During the pull-up and pull-down phases, the equivalent RC constant seen from the outputs of the 3rd and 4th stages of inverters is ideally doubled, thereby producing longer delay with the same area and power consumption.

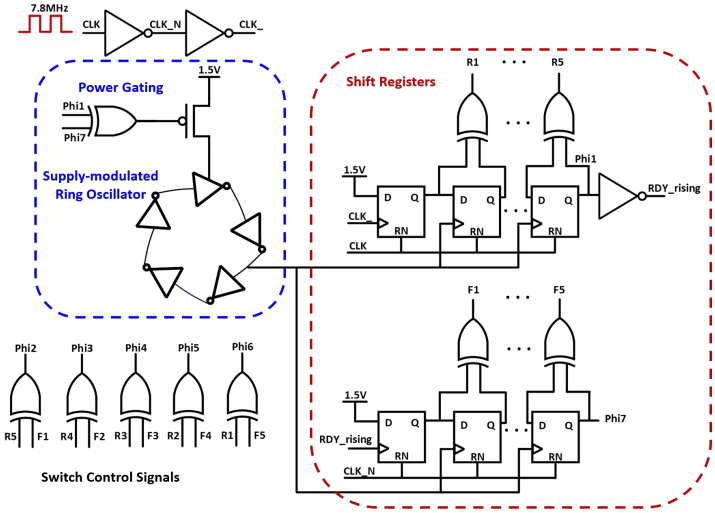


Figure 3.34: Complete schematic of the proposed stepwise sequencer based on a symmetrically supply-modulated local oscillator.

Compared to the conventional inverter delay chain, this delay cell can achieve a longer delay with a smaller silicon area and less power consumption. If the input is further connected with the output of the fifth buffer, it becomes a supply-modulated ring oscillator. This essentially means that the output of the previous stages modulates the supply of the third and fourth inverter stages. The frequency of this LO is the same as expressed by Equations (3.29). This design is reference-free and can be used in compact standard-cell design.

Digital shift registers are added at the output of the regenerative buffer of this modified ring oscillator to generate different phases. Power gating logic has also been introduced to halt the oscillation when the stepwise circuit is charged to any of the supply rails, providing further power savings in the timing logic. The complete schematic of the stepwise sequencer is shown in Fig. 3.34.

3.4.4. Simulation Result

The simulation of this supply-modulated delay cell is compared with a conventional delay line. The delay cell is configured to generate the required 2.5 ns delay for each stepwise pulse with 5 stages. The first 4 stages are sized to have relatively long channels (W / L = 150 nm / 1 μm), while the regenerative buffer is unit size (W/L = 150 nm / 130 nm). The simulation indicates that to produce a 2.5 ns delay, the power consumed by the proposed delay cell is 0.78 μW, while the conventional delay chain requires two additional long-channel inverters (W / L = 150 nm / 900 nm) to achieve the same delay time with 6% higher power consumption.

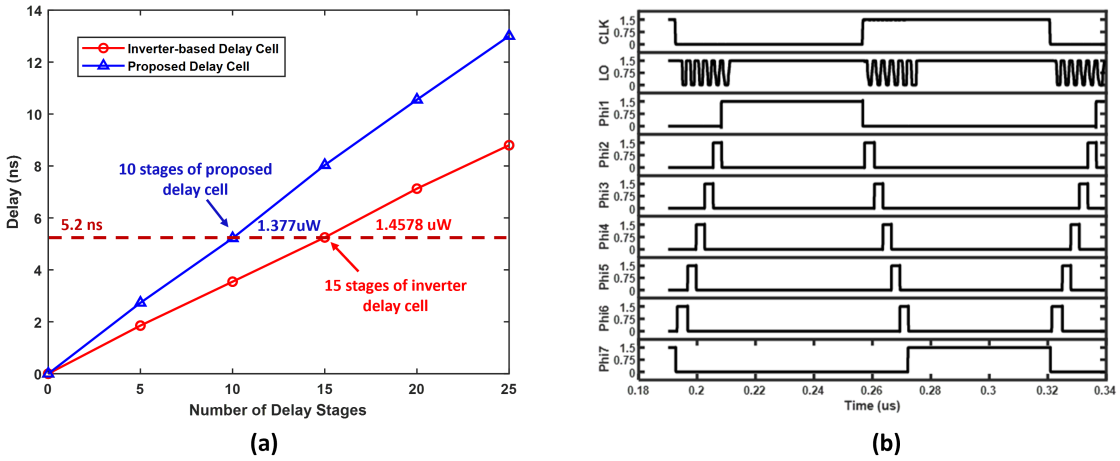


Figure 3.35: The performance of the proposed delay cell and the simulated timing diagram of the stepwise sequencer, (a) simulated results of generated delay versus the number of delay stages used, (b) simulated timing diagram of the stepwise sequencer.

The effectiveness of the area reduction with the proposed delay cell design is illustrated in Fig. 3.35(a). The proposed delay cell (4 long channel inverters + 1 regenerative buffer) is cascaded and compared to the conventional inverter-based delay chain with the same transistor sizing. Let's take a 5.2 ns of delay generation as an example, as depicted in Fig. 3.35(a). A 7.8 MHz reference signal is used as the input. The rising and falling edges of the reference signal are both delayed once within one cycle. The power dissipated by this delay cell within one cycle is calculated. The results indicate that the proposed delay cell needs 10 stages to generate the delay with 1.377 μW of power consumption. In comparison, the conventional inverter delay cell needs 5 extra stages to generate the same delay with 6% higher power dissipation. This suggests that the proposed delay cell can roughly save 30% of the area compared to the conventional inverter-based delay cell when generating delays in the ns range. Besides, this design is as compact as the conventional approach. Thus, it can be potentially used as a standard cell design.

The output waveforms of the complete sequencer design are illustrated in Fig. 3.35(b). The 7.8 MHz reference is denoted as CLK, and the local oscillation waveform is denoted as LO. The stepwise phases Phi 1 to Phi 7 align perfectly with the reference signal. When the output of Phi 1 (charge to V_{DD}) or Phi 7 (discharge to ground) is high, the LO ceases oscillation to save power.

The power breakdown of the stepwise sequencer is depicted in Fig. 3.36. The results reveal that power gating effectively reduces the power consumption on LO by a factor of 3. The final sequencer design achieved a power consumption of 23.5 μW per channel, making it suitable for low-power stepwise PAs. A performance comparison with stepwise controllers in other works is summarized in Table 3.3, where this design achieves the lowest power dissipation per channel. The use of more digital-energy-efficient technology but a much faster pulse-switching frequency makes it difficult to compare with other works. Anyhow, this design achieves a 3x reduction compared to [64]. Regarding PVT and mismatch performance, the delay cell and the sequencer can successfully operate across global PVT and mismatch corners with $\pm 10\%$ of supply variations. Details will be discussed in the upcoming design result chapter.

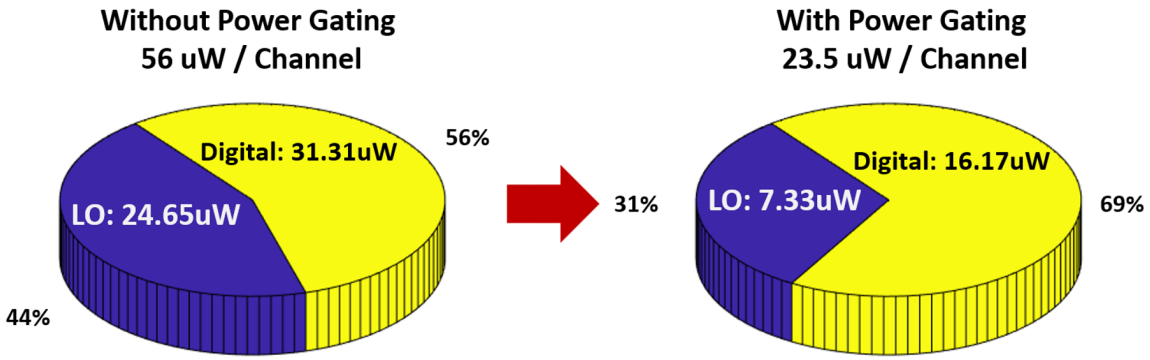


Figure 3.36: Power breakdown of the stepwise sequencer with and without power gating.

	ISSCC'17 [57]	JSSC'22 [46]	ESSCIRC'21 [63]	TCAS-II'21 [64]	This Work
Process	45 nm	180 nm	180 nm	180 nm	130 nm
†**Reference**	$5f_s$ Off-chip PLL	$4f_s$ External	f_s=780 kHz External	f_s=1 MHz External	f_s=7.8 MHz External
Phase Generator	Ring OSC	In-channel DLL	Full Digital	Delay Line + Digital	Symmetrically-modulated LO + Digital
Tr/T	24%	25%	20%	19.5%	10.1%
ᵀ**Power/Channel**	N.A.	N.A.	[1]140 μW	[1]70 μW	[2]**23.5 μW**

† Reference clock that feed into the PA.
ᵀ Power dissipated to control stepwise circuit.
[1] Measured result.
[2] Simulated result.

Table 3.3: Performance of stepwise waveform controllers.

4

Simulation Results

In this chapter, the functionality and the specifications of the designed PA signal chain are verified by means of circuit simulations.

4.1. Duty Cycling Control

The complete stepwise-PA signal chain is depicted in Fig. 4.1. To test if the designed circuits meet the requirements for producing an acoustic burst with a fast response, a duty-cycled reference clock with a frequency of 7.8 MHz is fed into the designed signal chain. Given that the targeted application involves an extremely small duty cycle, such as an acoustic scan with 5 consecutive 7.8 MHz acoustic pulses at a repetition frequency of 1000 Hz, which occupies only $\frac{1}{1560}$ of the complete 1000 Hz repetition cycle, the simulation time becomes too long. The figure might not be easy to read with such a small duty cycle.

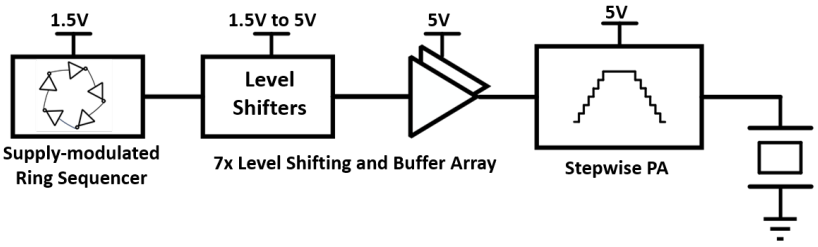


Figure 4.1: Simplified block diagram of the proposed PA signal chain.

For illustrative purposes, the control timing is duty-cycled to have 5 consecutive pulses and a 15-pulse-long interval. The simulated duty-cycled waveform and its timing diagram are shown in Fig. 4.2(a) and (b). A clear stepwise waveform can be established within 5 oscillation cycles, enabling a fast response on the transducer. During the sleep state, the simulated leakage current of the 1.5V logic and the 5V pulser is between several hundreds of pA and 1 nA, which is negligible. The transient waveform of the voltage on each flying capacitor in duty-cycling mode is shown in Fig. 4.2(c). The stepwise voltage levels can be successfully established in a similar manner as in continuous mode. The circuit is completely settled after approximately 25 cycles.

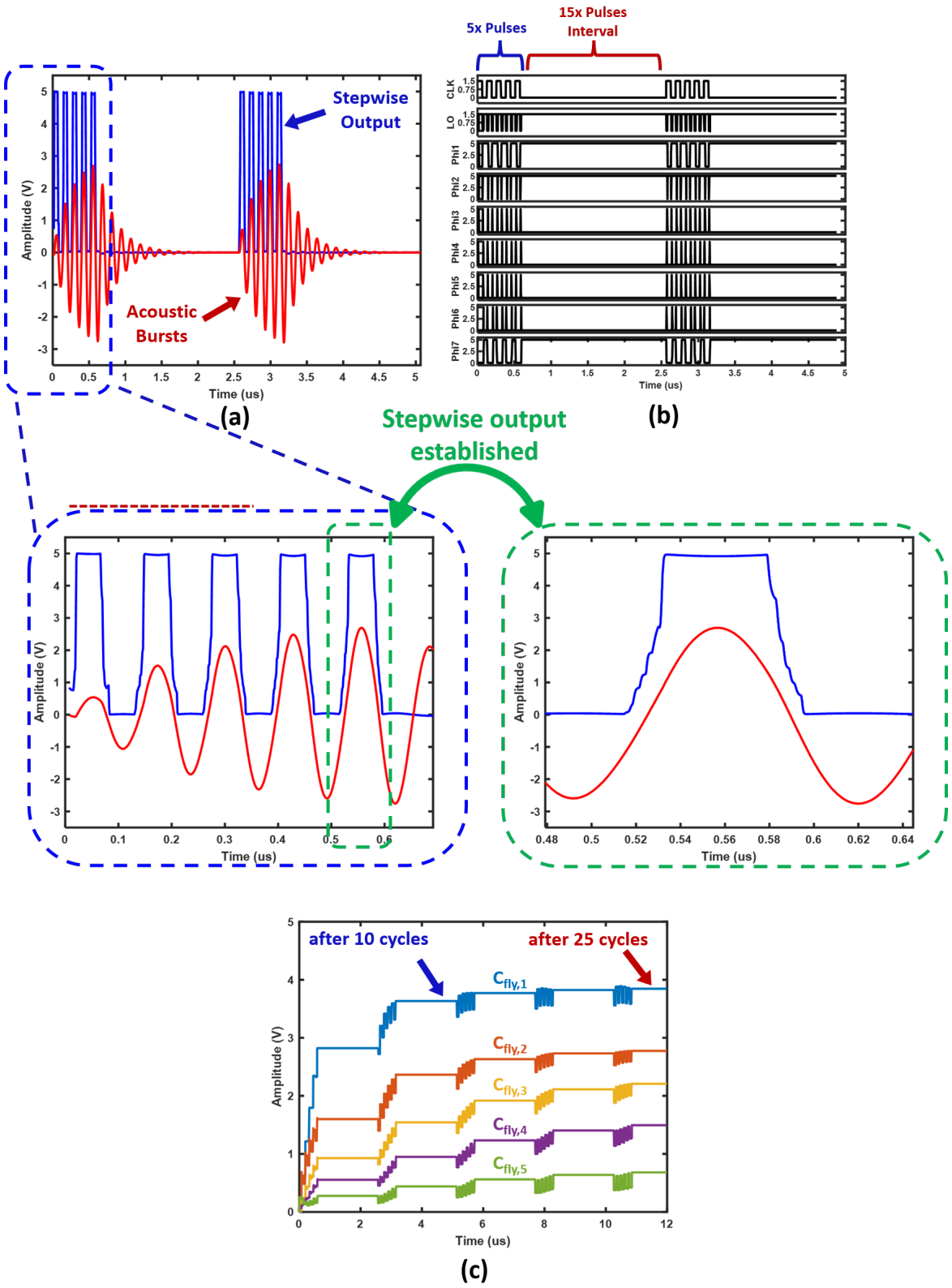


Figure 4.2: Simulated pulser response with duty-cycled clock reference, the stepwise pulser is able to establish a clear stepwise waveform at the 5^{th} oscillation cycle, (a) simulated stepwise output waveform and the voltage across the resistance in the RLC branch of the transducer, (b) simulated control timing for duty-cycled stepwise PA, (c) simulated voltage that established on each flying capacitor for the first 25 oscillation cycles (5 bursts).

4.2. Power Consumption and Efficiency

The power breakdown for the complete signal chain in continuous mode is depicted in Fig. 4.3, where 82% of the total power is delivered to the resistive part of the transducer. Notably, the conduction loss of the switched-mode pulser and the gate-charge loss dissipated on the 5V buffers combined make up for 15% of the total power consumption, representing the major losses in the signal chain. These results align with the analysis regarding PA non-idealities.

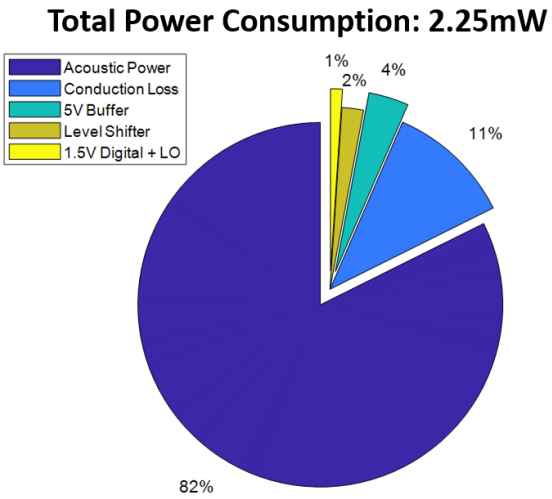


Figure 4.3: Power breakdown of the designed PA signal chain.

Considering the fact that the leakage current during the off phase is negligible and the targeted application scenario would require duty-cycled acoustic bursts to perform beamforming scanning, the power consumption under duty-cycled mode P_{DT} can be safely calculated using Equation (4.1):

$$P_{DT} = \frac{N_P f_{PR}}{f_s} P_{tot} = \frac{5 \times 1000Hz}{7.8 \times 10^6 Hz} \times 2.25mW = 1.44\mu W, \tag{4.1}$$

where the results highly depend on the number of pulses N_P used in each repetition cycle (N_P = 5 is taken here for illustrative purposes). This can be easily programmed after the beamforming controller and all the associated power and reference blocks in the transmitter have been designed.

4.3. PVT and Mismatch Performances

To demonstrate the effect of PVT and mismatch on the performance of the PA signal chain, a Monte Carlo (MC) simulation with 200 sampling points is performed across the global Process-Voltage-Temperature (PVT) and mismatch corners of the technology with $\pm$10% logic supply voltage variation. The corner setups are as follows:

- **Corner 1 (Typical)**: 1.5 V logic supply, 5 V PA supply, 27°C.
- **Corner 2 (Worst Corner)**: 1.65 V logic supply, 5 V PA supply, 45°C.

- **Corner 3 (Worst Corner)**: 1.35 V logic supply, 5 V PA supply, 10°C.

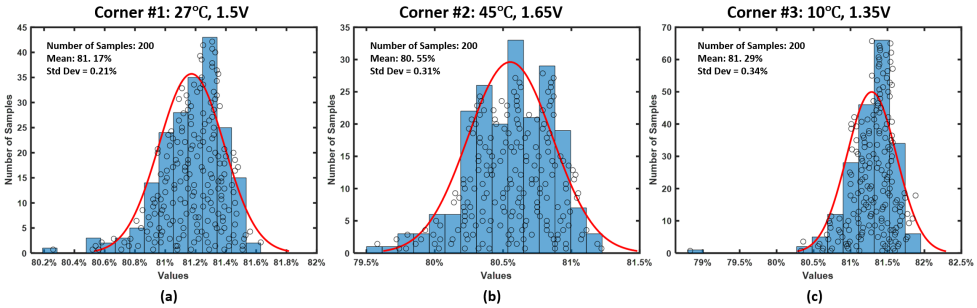


Figure 4.4: Global PVT and mismatch performance of the PA signal chain on acoustic efficiency, (a) the typical corner, (b) the worst corner with high temperature and +10% of supply variation, (c) the worst corner with low temperature and -10% of supply variation.

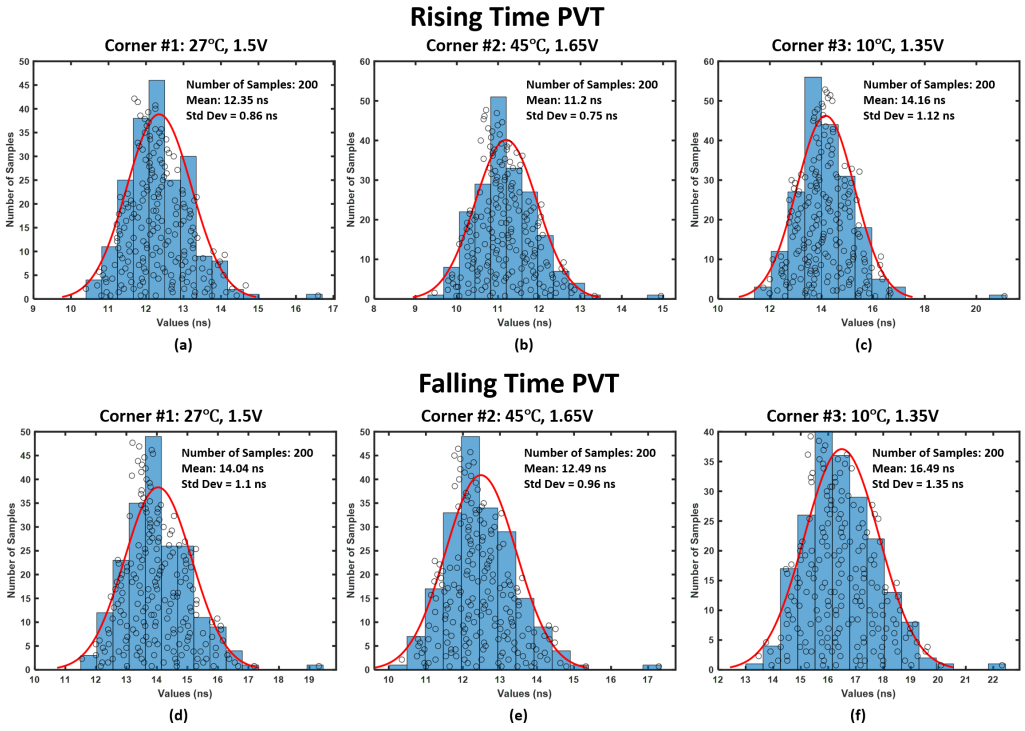


Figure 4.5: Global PVT and mismatch performance of the PA signal chain under (a) the typical corner, (b) the worst corner with high temperature and +10% of supply variation, (c) the worst corner with low temperature and -10% of supply variation.

The MC simulation results in Fig. 4.4 and Fig. 4.5 affirm the performance of the designed stepwise pulser. For the acoustic efficiency, the pulser consistently maintains an average efficiency of above 81% across the global corner, with a small part of the outliers below 80% in the worst corner. None of the sample points fails to work across the PVT and mismatch domains.

The mismatch between falling and rising times can potentially impact the phase alignment between different channels. For example, if the mismatch exceeds the

required delay resolution of the application, the expected focal pressure would drop, leading to a worse overall Tx performance. The Monte-Carlo simulation results in Fig. 4.5 show that the PVT-mismatch variations would introduce a maximum average rising/falling time mismatch of around 2.33 ns at corner 3, which accounts for only 1.8% of the total oscillation period and only 9.7% of the required beamforming-delay resolution.

These results demonstrate the robustness of the designed stepwise pulser in both energy efficiency and beamforming performance.

4.4. Floor Plan and Area Estimation

The layout of the complete design is not yet design-rules-check (DRC) and layout-versus-schematic (LVS) clean. The floor plan of the design is shown in Fig. 4.6. The total die area for each PA channel is estimated to be 108 μm x 520 μm, which occupies around 53% of the total transducer channel area. The size of the capacitor banks can be optimized for better overall efficiency.

According to the author's experiences, optimizing buffers' and level shifters' sizes based on charge-sharing switch sizes proves to be a challenge in physical design, often consuming significant time and effort. This complexity arises from the role of LS as the interface between two different supply domains. Since the LS is usually not fully differential, the corresponding layout can introduce a mismatch between the rising and falling times, as depicted in Fig. 3.24. This mismatch would not only affect the gate-charge loss but also introduce a variation on the C_p loss saving. The introduced loss variation becomes more significant when the LS and buffer drive a larger sharing switch. Increasing the speed of LS and buffers can easily help mitigate this effect but at the cost of significantly increasing the driving power. According to pre-layout and post-layout simulations of the level shifting channel, the sizing and layout can introduce up to around 30% of total efficiency variation, which is mainly due to the low-power requirements of this signal chain design.

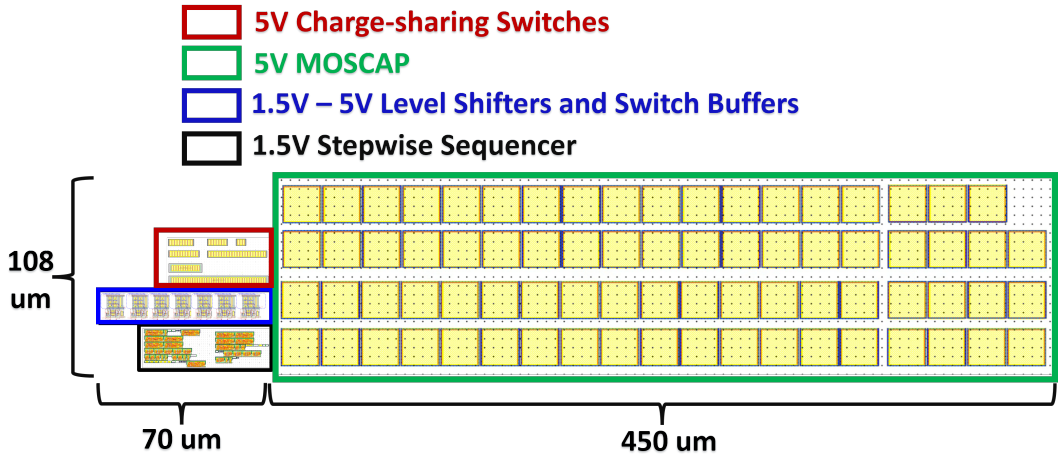


Figure 4.6: Floor plan of the pulser for one TX channel.

4.5. Summary

The performance of the complete PA signal chain is summarized in Table 4.1.

Pulser Performance	Estimated	Achieved
[1]**Acoustic Efficiency**	> 82%	[2]82.5%
Output Power / Channel	1.93 mW	1.85 mW
[3]**Maximum Tr/Tf Mismatch**	N.A.	2.33 ns (9.7% of beamforming-delay resolution)
Tr/T	~ 15%	9.5%
Tf/T	~ 15%	10.7%
Cp Loss Saving	~ 50%	47.7%

[1] The power consumption includes all associate blocks in the signal chain.
[2] The simulated result in the typical corner is 82.5%. The average efficiency across global PVT and mismatch corners is 81%.
[3] The maximum average rising/falling time mismatch occurs with low temperature and -10% of supply variation.

Table 4.1: Performance of the complete PA signal chain.

5

Conclusion

This chapter concludes the design of a high-efficiency stepwise ultrasonic pulser for invasive acoustoelectric imaging applications. The design results are first compared with state-of-the-art solutions. The author's contributions are summarized, and recommendations for future work are discussed in the end.

5.1. Performance Comparison with State-of-the-art

	ISSCC'21 [52]	TCAS-II'21 [64]	JSSC'21 [51]	ESSCIRC'21 [63]	JSSC'22 [46]	This work
Process	180 nm	180 nm	180 nm	180 nm	180nm	130 nm
Method	Energy Replenish	Charge Redistribute	Stepwise	Stepwise	Stepwise	Stepwise
†Transducer Flipping	No	Yes	No	No	Yes	**No**
Q	N.A.	4.85	183.87	4.53	4.56	6
P	N.A.	6.08%	1.016%	0.7%	20.4%	16.04%
ΔCap Ratio	Inductor	N.A	60	15.6	1/9	**2.8**
Number of Caps	N.A.	N.A	5	5	4	**5**
Class-D Baseline	N.A.	39.6%	82.7%	8.1%	72.3%	**72.6%**
Achieved Efficiency	N.A.	N.A.	[1]81.7%	N.A.	[1]75.6%	[1]**82.5%**
Efficiency Improvement	N.A.	N.A.	-1%	N.A.	3.3%	**9.9%**
Achieved Cp Saving	[2]73.1%	[2]42.6%	N.A.	[2]80%	N.A	[1]**47.7%**
***Psc / Channel**	N.A.	N.A.	[2]70 μW	[2]140 μW	N.A	[1]**23.5 μW**

† **Flipping the transducer's terminals would make the PA less suitable for massive array integration.**
Δ **The flying-cap-to-load-cap ratio of each stepwise level. Using a big cap ratio is not suitable for miniaturized integration.**
* **Power dissipated on the stepwise controller.**
[1] **Simulated result.**
[2] **Measured result.**

Table 5.1: Performance comparison with state-of-the-art ultrasonic pulsers.

The designed PA exhibits promising performance when compared to state-of-the-art PAs, as detailed in Table 5.1. In the simulation, the PA signal chain achieves an overall acoustic efficiency of 82.5% in the typical corner and an average of 81% across global PVT and mismatch corners. This marks a noteworthy improvement of 9.9% compared to the transducer's class-D baseline. This result outperforms the efficiency of [46] by 6.9%, where a transducer with 0.3% lower baseline efficiency was used. The simulated efficiency is also comparable and slightly higher than [64], where a transducer with a 30x higher quality factor and 20x higher cap ratio was employed. Additionally, the proposed stepwise sequencer, based on an area-efficient symmetrically-modulated delay cell, achieves the lowest power consumption among prior art controllers for stepwise circuits. The PA signal chain is estimated to have a

compact area of 108 μm x 520 μm, making it suitable for integration into a 115μm-pitch transmit channel while eliminating the need for extra reference sources and off-chip components, aligning with the compact nature of conventional class-D PAs.

5.2. Thesis Contributions

In this thesis, the following contributions have been made through systematic analysis and circuit design:

- **Derivation of system specifications for an invasive acoustoelectric imaging application**: This involves an extensive review of the literature on AE prototyping and ultrasound systems. The acoustic modeling is performed in MATLAB to establish the necessary system specifications.

- **Introduction of a new baseline power-efficiency analysis to quantify the relation between switched-mode PAs and transducers with different electrical characteristics**: This analytical approach establishes a correlation between the efficiency of switched-mode PAs and the quality and parasitic capacitance of the transducer. The analysis is based on the common assumption that the transducer is properly characterized using the BVD model, and the acoustic power is the power delivered to the resistive part of the BVD model.

- **Model and design of an area- and energy-efficient stepwise PA signal chain**: The PA design starts with a MATLAB model that is capable of roughly estimating the key energy losses of a stepwise PA driving a transducer. The designed signal chain demonstrates a significant efficiency improvement when compared to the class-D efficiency baseline of the utilized transducer in simulation. A stepwise controller (sequencer) is proposed based on a symmetrically-modulated delay cell. The stepwise controller attains the lowest power consumption per channel compared to those of prior arts. Compared to conventional class-D PA, the design does not require additional reference and routing resources or off-chip components, which makes it a promising solution for large-array integrations.

5.3. Future Work

While the current study established a foundation for an efficient stepwise ultrasonic pulser in invasive acoustoelectric imaging, there are several avenues for future exploration and improvement:

- **Adding tunability to the stepwise sequencer**: Introducing tunability to the stepwise sequencer can be a valuable enhancement for adaptive performance. Currently, the stepwise sequencer is manually tuned to achieve optimal efficiency. Future work can involve the development of a self-calibration loop that relates the output-node voltage to the delay of the sequencer (by means of a voltage-to-frequency converter, VCO). This mechanism would allow the sequencer to dynamically track the stepwise waveform and adjust the LO frequency accordingly. By automatically optimizing the rising/falling edge based on the characteristics of different transducers or adapting to variations in trans-

ducer behavior, the stepwise sequencer may help the PA achieve higher efficiency across a broader range of operating conditions.

- **Implementing a full analog stepwise sequencer**: The current design incorporates digital shift registers for phase generation. Since around 70% of the digital power in the final design is dissipated in dissipated in the shift register, an analog phase generator could potentially further lower the overall power consumption for stepwise sequencer.

Bibliography

[1] C. Martyn and R. Hughes, “Epidemiology of peripheral neuropathy.” *Journal of Neurology, Neurosurgery, and Psychiatry*, vol. 62, no. 4, p. 310, 1997.

[2] S. Thawait, V. Chaudhry, G. Thawait, K. Wang, A. Belzberg, J. Carrino, and A. Chhabra, “High-resolution MR neurography of diffuse peripheral nerve lesions,” *American Journal of Neuroradiology*, vol. 32, no. 8, pp. 1365–1372, 2011.

[3] K.-H. Chen, K.-F. Lee, H.-C. Hsu, W.-C. Huang, K.-Y. Hsiao, and K.-M. Fang, “The role of high-resolution ultrasound in the diagnosis of a traumatic neuroma in an injured median nerve,” *American Journal of Physical Medicine & Rehabilitation*, vol. 88, no. 9, pp. 771–774, 2009.

[4] X. Song, X. Chen, J. Guo, M. Xu, and D. Ming, “Living rat SSVEP mapping with acoustoelectric brain imaging,” *IEEE Transactions on Biomedical Engineering*, vol. 69, no. 1, pp. 75–82, 2021.

[5] A. Alvarez, C. Preston, T. Trujillo, and R. S. Witte, “Acoustoelectric imaging for beat-to-beat cardiac activation wave mapping in an in vivo swine model,” in *2020 IEEE International Ultrasonics Symposium (IUS)*, 2020, pp. 1–4.

[6] P. Debye, “A method for the determination of the mass of electrolytic ions,” *The Journal of Chemical Physics*, vol. 1, no. 1, pp. 13–16, 1933.

[7] F. E. Fox, K. F. Herzfeld, and G. D. Rock, “The effect of ultrasonic waves on the conductivity of salt solutions,” *Physical Review*, vol. 70, no. 5-6, p. 329, 1946.

[8] B. Lavandier, J. Jossinet, and D. Cathignol, “Experimental measurement of the acousto-electric interaction signal in saline solution,” *Ultrasonics*, vol. 38, no. 9, pp. 929–936, 2000.

[9] Q. Li, R. Olafsson, P. Ingram, Z. Wang, and R. Witte, “Measuring the acousto-electric interaction constant using ultrasound current source density imaging,” *Physics in Medicine & Biology*, vol. 57, no. 19, p. 5929, 2012.

[10] R. H. Parmenter, “The acousto-electric effect,” *Physical Review*, vol. 89, no. 5, p. 990, 1953.

[11] X. Song, Y. Qin, Y. Xu, P. Ingram, R. S. Witte, and F. Dong, “Tissue acoustoelectric effect modeling from solid mechanics theory,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 64, no. 10, pp. 1583–1590, 2017.

[12] Y. Zhou, X. Song, X. Chen, X. Zhao, Y. Ke, and D. Ming, “A source signal modulation mechanism with pulse focused ultrasound for acoustoelectric brain imaging,” in *2019 9th International IEEE/EMBS Conference on Neural Engineering (NER)*, 2019, pp. 766–769.

[13] J. Shilton, D. Mace, V. Talyanskii, Y. Galperin, M. Simmons, M. Pepper, and D. Ritchie, “On the acoustoelectric current in a one-dimensional channel,” *Journal of Physics: Condensed Matter*, vol. 8, no. 24, p. L337, 1996.

[14] K. Sonowal, A. Kalameitsev, V. Kovalev, and I. Savenko, “Acoustoelectric effect in two-dimensional Dirac materials exposed to Rayleigh surface acoustic waves,” *Physical Review B*, vol. 102, no. 23, p. 235405, 2020.

[15] C. Preston, “Acoustoelectric imaging of deep brain stimulation currents,” *Ph.D. Thesis, The University of Arizona*, 2021. [Online]. Available: http://hdl.handle.net/10150/661607

[16] A. Rose, “Radiation pressure and the acoustoelectric effect,” *Materials Research Bulletin*, vol. 6, no. 10, pp. 1057–1064, 1971.

[17] R. Olafsson, R. S. Witte, and M. O’Donnell, “Measurement of a 2D electric dipole field using the acousto-electric effect,” in *Medical Imaging 2007: Ultrasonic Imaging and Signal Processing*, vol. 6513. SPIE, 2007, pp. 226–235.

[18] J. L. Rintoul, E. Neufeld, C. Butler, R. O. Cleveland, and N. Grossman, “Remote focused encoding and decoding of electric fields through acoustoelectric heterodyning,” *Communications Physics*, vol. 6, no. 1, p. 79, 2023.

[19] J. Jossinet, B. Lavandier, and D. Cathignol, “Impedance modulation by pulsed ultrasound,” *Annals of the New York Academy of Sciences*, vol. 873, no. 1, pp. 396–407, 1999.

[20] G. Kristín Inga, “The development of an experimental setup to measure acousto-electric interaction signal,” *Current Directions in Biomedical Engineering*, vol. 1, no. 1, pp. 5–9, 2015.

[21] B. A. Giuffre and R. Jeanmonod, “Anatomy, sciatic nerve,” 2018.

[22] J. P. Kim, W. Lee, J. Suh, H. Lee, K. Lee, H. Y. Ahn, M.-J. Seo, S.-T. Ryu, K. Aristovich, D. Holder, and S. J. Kim, “A 10 nV$\sqrt{Hz}$ noise level 32-channel neural impedance sensing ASIC for local activation imaging on nerve section,” in *2020 42nd Annual International Conference of the IEEE Engineering in Medicine Biology Society (EMBC)*, 2020, pp. 4012–4015.

[23] J.-H. Suh, H. Choi, Y. Jung, S. Oh, H. Cho, N. Koo, S. J. Kim, C. Bae, S. Ha, and M. Je, “A 16-channel impedance-readout IC with synchronous sampling and baseline cancelation for fast neural electrical impedance tomography,” *IEEE Solid-State Circuits Letters*, vol. 6, pp. 109–112, 2023.

[24] D. K. Piech, B. C. Johnson, K. Shen, M. M. Ghanbari, K. Y. Li, R. M. Neely, J. E. Kay, J. M. Carmena, M. M. Maharbiz, and R. Muller, “A wireless millimetre-scale implantable neural stimulator with ultrasonically powered bidirectional communication,” *Nature Biomedical Engineering*, vol. 4, no. 2, pp. 207–222, 2020.

[25] B. P. Bean, “The action potential in mammalian central neurons,” *Nature Reviews Neuroscience*, vol. 8, no. 6, pp. 451–465, 2007.

[26] H. Rivandi and T. L. Costa, “A 2D ultrasound phased-array transmitter ASIC for high-frequency US stimulation and powering,” *IEEE Transactions on Biomedical Circuits and Systems*, pp. 1–12, 2023.

[27] M. Tan, E. Kang, J.-S. An, Z.-Y. Chang, P. Vince, T. Matéo, N. Sénégond, and M. A. P. Pertijs, “A 64-channel transmit beamformer with ±30-V bipolar high-voltage pulsers for catheter-based ultrasound probes,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1796–1806, 2020.

[28] T. Wiesmann, A. Bornträger, T. Vassiliou, A. Hadzic, H. Wulf, H.-H. Müller, and T. Steinfeldt, “Minimal current intensity to elicit an evoked motor response cannot discern between needle-nerve contact and intraneural needle insertion,” *Anesthesia & Analgesia*, vol. 118, no. 3, pp. 681–686, 2014.

[29] A. R. Sauter, M. S. Dodgson, H. Kalvøy, S. Grimnes, A. Stubhaug, and Ø. Klaastad, “Current threshold for nerve stimulation depends on electrical impedance of the tissue: a study of ultrasound-guided electrical nerve stimulation of the median nerve,” *Anesthesia & Analgesia*, vol. 108, no. 4, pp. 1338–1343, 2009.

[30] G. Y. Zhang, Y. F. Chen, W. X. Dai, D. Zhang, Y. Huang, W. Z. He, and C. X. Lin, “Diabetic peripheral neuropathy increases electrical stimulation threshold of sciatic nerve: a prospective parallel cohort study,” *Diabetes, Metabolic Syndrome and Obesity*, pp. 4447–4455, 2020.

[31] H. Bostock, K. Cikurel, and D. Burke, “Threshold tracking techniques in the study of human peripheral nerve,” *Muscle & Nerve: Official Journal of the American Association of Electrodiagnostic Medicine*, vol. 21, no. 2, pp. 137–158, 1998.

[32] The United States Food and Drug Administration, “Marketing clearance of diagnostic ultrasound systems and transducers,” *Available online: https://www.fda.gov/regulatory-information/search-fda-guidance-documents/marketing-clearance-diagnostic-ultrasound-systems-and-transducers*, 2023.

[33] N. A. Pelot, G. B. Goldhagen, J. E. Cariello, E. D. Musselman, K. A. Clissold, J. A. Ezzell, and W. M. Grill, “Quantified morphology of the cervical and subdiaphragmatic vagus nerves of human, pig, and rat,” *Frontiers in Neuroscience*, vol. 14, p. 601479, 2020.

[34] G.-D. Kim, C. Yoon, S.-B. Kye, Y. Lee, J. Kang, Y. Yoo, and T.-K. Song, “A single FPGA-based portable ultrasound imaging system for point-of-care applications,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, no. 7, pp. 1386–1394, 2012.

[35] J. Lee, K.-R. Lee, B. E. Eovino, J. H. Park, L. Y. Liang, L. Lin, H.-J. Yoo, and J. Yoo, “A 36-channel auto-calibrated front-end ASIC for a pMUT-based miniaturized 3-D ultrasound system,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1910–1923, 2021.

[36] K. Van Dyke, “The piezo-electric resonator and its equivalent network,” *Proceedings of the Institute of Radio Engineers*, vol. 16, no. 6, pp. 742–764, 1928.

[37] J. Larson, P. Bradley, S. Wartenberg, and R. Ruby, “Modified Butterworth-Van Dyke circuit for FBAR resonators and automated measurement system,” in *2000 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No.00CH37121)*, vol. 1, 2000, pp. 863–868 vol.1.

[38] D. Leedom, R. Krimholtz, and G. Matthaei, “Equivalent circuits for transducers having arbitrary even- or odd-symmetry piezoelectric excitation,” *IEEE Transactions on Sonics and Ultrasonics*, vol. 18, no. 3, pp. 128–141, 1971.

[39] W. P. Mason, “Electromechanical transducers and wave filters,” 1948.

[40] G. Lockwood and F. Foster, “Modeling and optimization of high-frequency ultrasound transducers,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 41, no. 2, pp. 225–230, 1994.

[41] H. Li, K.-M. Lei, P.-I. Mak, and R. P. Martins, “A 12/13.56MHz crystal oscillator with binary-search-assisted two-step injection achieving 5.0nJ startup energy and 45.8µs startup time,” in *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, 2023, pp. 64–66.

[42] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, “A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8- μ W steady-state power,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2624–2635, 2018.

[43] Texas Instruments, “Transformer drive ultrasonic sensor IC with logarithmic amplifier,” *TUSS4470 Datasheet*, December 2019, revised May 2022.

[44] STMicroelectronics, “32-channel pulser with integrated beamformer channel,” *STHVUP32 Datasheet*, October 2022.

[45] K. Agbossou, J.-L. Dion, S. Carignan, M. Abdelkrim, and A. Cheriti, “Class D amplifier for a power piezoelectric load,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 47, no. 4, pp. 1036–1041, 2000.

[46] E. So, P. Yeon, E. J. Chichilnisky, and A. Arbabian, “An RF-ultrasound relay for adaptive wireless powering across tissue interfaces,” *IEEE Journal of Solid-State Circuits*, vol. 57, no. 11, pp. 3429–3441, 2022.

[47] J. Tillak, S. Akhbari, N. Shah, L. Radakovic, L. Lin, and J. Yoo, “A 2.34µJ/scan acoustic power scalable charge-redistribution pMUT interface system with on-chip aberration compensation for portable ultrasonic applications,” in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2016, pp. 189–192.

[48] H. Wu, M. Zhang, Z. Shao, J. Guo, K. A. Ng, L. Lin, and J. Yoo, “An ultrasound ASIC with universal energy recycling for >7-m all-weather metamorphic robotic vision,” *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3036–3047, 2022.

[49] H.-Y. Tang, Y. Lu, X. Jiang, E. J. Ng, J. M. Tsai, D. A. Horsley, and B. E. Boser, “3-D ultrasonic fingerprint sensor-on-a-chip,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2522–2533, 2016.

[50] C. Chen, S. B. Raghunathan, Z. Yu, M. Shabanimotlagh, Z. Chen, Z.-y. Chang, S. Blaak, C. Prins, J. Ponte, E. Noothout, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, “A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 1, pp. 47–59, 2016.

[51] J. Lee, K.-R. Lee, B. E. Eovino, J. H. Park, L. Y. Liang, L. Lin, H.-J. Yoo, and J. Yoo, “A 36-channel auto-calibrated front-end ASIC for a pMUT-based miniaturized 3-D ultrasound system,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1910–1923, 2021.

[52] J. Choi, Y. Park, J. B. Oh, J.-Y. Kim, J. Y. Hwang, S. Ha, C. Kim, and M. Je, “An energy-replenishing ultrasound pulser with 0.25CV2f dynamic power consumption,” in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 486–488.

[53] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, “Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2734–2745, 2013.

[54] L. Svensson and J. Koller, “Driving a capacitive load without dissipating fCV/sup 2/,” in *Proceedings of 1994 IEEE Symposium on Low Power Electronics*, 1994, pp. 100–101.

[55] S. Nakata, R. Honda, H. Makino, S. Mutoh, M. Miyama, and Y. Matsuda, “General stability of stepwise waveform of an adiabatic charge recycling circuit with any circuit topology,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 10, pp. 2301–2314, 2012.

[56] J. Park, Y.-H. Hwang, J. Oh, Y. Song, J.-E. Park, and D.-K. Jeong, “A mutual capacitance touch readout IC with 64% reduced-power adiabatic driving over heavily coupled touch screen,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1694–1704, 2019.

[57] L. G. Salem and P. P. Mercier, “26.4 A 0.4-to-1V 1MHz-to-2GHz switched-capacitor adiabatic clock driver achieving 55.6reduction,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 442–443.

[58] S. Nakata, H. Makino, J. Hosokawa, T. Yoshimura, S. Iwade, and Y. Matsuda, “Energy efficient stepwise charging of a capacitor using a DC-DC converter with consecutive changes of its duty ratio,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 7, pp. 2194–2203, 2014.

[59] E. J. Carlson and J. R. Smith, “A ±0.5-mV-minimum-input DC-DC converter with stepwise adiabatic gate-drive and efficient timing control for thermoelectric energy harvesting,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 2, pp. 977–990, 2023.

[60] S. Nakata, H. Suzuki, R. Honda, T. Kusumoto, S. Mutoh, H. Makino, M. Miyama, and Y. Matsuda, “Adiabatic SRAM with a shared access port using a controlled ground line and step-voltage circuit,” in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, 2010, pp. 2474–2477.

[61] B.-D. Choi and O.-K. Kwon, “Stepwise data driving method and circuits for low-power TFT-LCDs,” *IEEE Transactions on Consumer Electronics*, vol. 46, no. 4, pp. 1155–1160, 2000.

[62] H. Wu, J. H. Park, M. Zhang, L. Lin, R. Jiang, J.-H. Choi, and J. Yoo, “A 0.95pJ/b 5.12Gb/s/pin charge-recycling IOs with 47data applications,” in *2022 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2022, pp. 1–3.

[63] J. Pelgrims, K. Myny, and W. Dehaene, “A 36V ultrasonic driver for haptic feedback using advanced charge recycling achieving 0.20CV2f power consumption,” in *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 159–162.

[64] K.-J. Choi, H. G. Yeo, H. Choi, and D.-W. Jee, “A 28.7V modular supply multiplying pulser with 75.4% power reduction relative to CV2f,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 858–862, 2021.

[65] P. P. Healthcare, “Ultrasound transducer,” https://www.usa.philips.com/healthcare/solutions/ultrasound/ultrasound-transducer.

[66] M. Vallet, F. Varray, J. Boutet, J.-M. Dinten, G. Caliano, A. S. Savoia, and D. Vray, “Quantitative comparison of PZT and CMUT probes for photoacoustic imaging: Experimental validation,” *Photoacoustics*, vol. 8, pp. 48–58, 2017.

[67] R. van Schaijk, “CMUT and PMUT: New Technology Platform for Medical Ultrasound,” *Philips Application Report*, November 2018.

[68] I. O. Wygant, X. Zhuang, D. T. Yeh, O. Oralkan, A. S. Ergun, M. Karaman, and B. T. Khuri-yakub, “Integration of 2D CMUT arrays with front-end electronics for volumetric ultrasound imaging,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 55, no. 2, pp. 327–342, 2008.

[69] “Qualcomm 3D sonic sensor,” 2019. [Online]. Available: https://www.qualcomm.com/products/features/fingerprint-sensors

[70] A. Hajati, D. Latev, D. Gardner, A. Hajati, D. Imai, M. Torrey, and M. Schoeppler, “Three-dimensional micro electromechanical system piezoelectric ultrasound transducer,” *Applied Physics Letters*, vol. 101, no. 25, 2012.

[71] F. Sammoura, K. Smyth, and S.-G. Kim, “Optimizing the electrode size of circular bimorph plates with different boundary conditions for maximum deflection of piezoelectric micromachined ultrasonic transducers,” *Ultrasonics*, vol. 53, no. 2, pp. 328–334, 2013.

[72] Y. Qiu, J. V. Gigliotti, M. Wallace, F. Griggio, C. E. Demore, S. Cochran, and S. Trolier-McKinstry, “Piezoelectric micromachined ultrasound transducer (PMUT) arrays for integrated sensing, actuation and imaging,” *Sensors*, vol. 15, no. 4, pp. 8020–8041, 2015.

[73] C. Chen, S. B. Raghunathan, Z. Yu, M. Shabanimotlagh, Z. Chen, Z.-y. Chang, S. Blaak, C. Prins, J. Ponte, E. Noothout *et al.*, “A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography,” *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 63, no. 1, pp. 47–59, 2015.

[74] I. S. Uzunov, M. D. Terzieva, B. M. Nikolova, and D. G. Gaydazhiev, “Extraction of modified butterworth — Van Dyke model of FBAR based on FEM analysis,” in *2017 XXVI International Scientific Conference Electronics (ET)*, 2017, pp. 1–4.

[75] J. Jung, S. Oh, J. Kim, G. Ha, J. Lee, S. Kim, E. Park, J. Lee, Y. Yoon, S. Bae, W. Kim, Y. Lim, K. Lee, J. Huh, J. Lee, and T. B. Cho, “A Single-Crystal-Oscillator-Based Clock-Management IC with 18× Start-Up Time Reduction and 0.68ppm/ºC Duty-Cycled Machine-Learning-Based RCO Calibration,” in *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 58–60.

[76] H. Luo, S. Kundu, T. Huusari, S. Shahraini, E. Alban, J. Mix, N. Kurd, M. Abdel-Moneum, and B. Carlton, “A fast startup crystal oscillator using impedance guided chirp injection in 22 nm FinFET CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 57, no. 3, pp. 688–697, 2022.

[77] W. Sansen, *Design of crystal oscillators*. Boston, MA: Springer US, 2006, pp. 677–709. [Online]. Available: https://doi.org/10.1007/0-387-25747-0_22

[78] E. Vittoz, M. Degrauwe, and S. Bitz, “High-performance crystal oscillator circuits: theory and application,” *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 774–783, 1988.

[79] C. Neudorfer, C. T. Chow, A. Boutet, A. Loh, J. Germann, G. J. Elias, W. D. Hutchison, and A. M. Lozano, “Kilohertz-frequency stimulation of the nervous system: A review of underlying mechanisms,” *Brain stimulation*, vol. 14, no. 3, pp. 513–530, 2021.

[80] Y. Chen, E. M. Haacke, and J. Li, “Peripheral nerve magnetic resonance imaging,” *F1000 Research*, vol. 8, 2019.

[81] B. E. Treeby and B. T. Cox, “k-Wave: MATLAB toolbox for the simulation and reconstruction of photoacoustic wave fields,” *Journal of biomedical optics*, vol. 15, no. 2, pp. 021 314–021 314, 2010.

[82] M. Zhou, “Integrated circuits for ultrasound harmonic imaging: Modelling, design, and in-vitro experiments,” Ph.D. dissertation, Electrical Engineering, May 2022, proefschrift.

[83] B. C. N. E. L. B. G. M. P. D. K. A. K. N. Hasgall PA, Di Gennaro F, “IT’IS Database for thermal and electromagnetic parameters of biological tissues,” *itis.swiss/database*, vol. 15, no. 2, pp. 021 314–021 314, 2022.

[84] T. L. Szabo, *Diagnostic ultrasound imaging: inside out*. Academic press, 2004.

[85] T. Costa, C. Shi, K. Tien, J. Elloian, F. A. Cardoso, and K. L. Shepard, “An integrated 2D ultrasound phased array transmitter in CMOS with pixel pitch-matched beamforming,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 4, pp. 731–742, 2021.

[86] S. Kawasaki, V. Giagka, M. de Haas, M. Louwerse, V. Henneken, C. van Heesch, and R. Dekker, “Pressure measurement of geometrically curved ultrasound transducer array for spatially specific stimulation of the vagus nerve,” in *2019 9th International IEEE/EMBS Conference on Neural Engineering (NER)*, 2019, pp. 1239–1242.

[87] E. Kang, Q. Ding, M. Shabanimotlagh, P. Kruizinga, Z.-Y. Chang, E. Noothout, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, “A reconfigurable ultrasound transceiver ASIC with 24×40 elements for 3-D carotid artery imaging,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 2065–2075, 2018.

[88] X. Jiang, W. T. Ng, and J. Chen, “A miniaturized low-intensity ultrasound device for wearable medical therapeutic applications,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1372–1382, 2019.

[89] C. Vaucourt, “Choosing inductors and capacitors for DC/DC converters,” *Texas Instruments Application Report SLVA157*, 2004.

[90] K. Bult and H. Wallinga, “A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation,” *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 357–365, 1987.

[91] L. M. Alvero-Gonzalez, G. Gielen, and E. Gutierrez, “Delay cell for highly-linear current-controlled oscillator-based analog-to-digital conversion,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3238–3242, 2023.

[92] C. Tran, H. Kawaguchi, and T. Sakurai, “Low-power high-speed level shifter design for block-level dynamic voltage scaling environment,” in *2005 International Conference on Integrated Circuit Design and Technology, 2005. ICICDT 2005.*, 2005, pp. 229–232.

[93] C. Huang and H. Jiao, “C3MLS: An ultra-wide-range energy-efficient level shifter with CCLS/CMLS hybrid structure,” *IEEE Journal of Solid-State Circuits*, vol. 58, no. 10, pp. 2685–2695, 2023.

[94] J. Park and H. Jeong, “Energy-efficient wide-range level shifter with a logic error detection circuit,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 31, no. 5, pp. 701–705, 2023.

[95] R. Matsuzuka, T. Hirose, Y. Shizuku, K. Shinonaga, N. Kuroki, and M. Numa, “An 80-mV-to-1.8-V conversion-range low-energy level shifter for extremely low-voltage VLSIs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 8, pp. 2026–2035, 2017.

[96] S. Kabirpour and M. Jalali, “A low-power and high-speed voltage level shifter based on a regulated cross-coupled pull-up network,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 909–913, 2019.

[97] S. Boon, S. Butler, R. Byrne, B. Setering, M. Casalanda, and A. Scherf, “High performance clock distribution for CMOS ASICs,” in *1989 Proceedings of the IEEE Custom Integrated Circuits Conference*, 1989, pp. 15.4/1–15.4/5.

[98] H. Park, J. Sim, Y. Choi, J. Choi, Y. Kwon, S. Park, G. Park, J. Chung, K.-M. Kim, H.-K. Jung, H. Kim, J. Chun, and C. Kim, “A 1.3–4-GHz quadrature-phase digital DLL using sequential delay control and reconfigurable delay line,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1886–1896, 2021.

[99] B. Razavi, “The delay-locked loop [a circuit for all seasons],” *IEEE Solid-State Circuits Magazine*, vol. 10, no. 3, pp. 9–15, 2018.

[100] B. Wu, S. Zhu, B. Xu, and Y. Chiu, “A 24.7 mW 65 nm CMOS SAR-assisted CT $\Delta\Sigma$ modulator with second-order noise coupling achieving 45 MHz bandwidth and 75.3 dB SNDR,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2893–2905, 2016.

[101] E. Ferro, V. M. Brea, P. López, and D. Cabello, “Micro-energy harvesting system including a PMU and a solar cell on the same substrate with cold startup from 2.38 nW and input power range up to 10 μW using continuous MPPT,” *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5105–5116, 2019.

[102] A. Devices, “Ds1135 3-in-1 high-speed silicon delay line,” *DS1020/DS1021 Datasheet*, September 2012.

[103] B. Razavi, “The ring oscillator [a circuit for all seasons],” *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 10–81, 2019.

[104] C. Q. Liu, Y. Cao, and C. H. Chang, “ACRO-PUF: a low-power, reliable and aging-resilient current starved inverter-based ring oscillator physical unclonable function,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 12, pp. 3138–3149, 2017.

[105] C.-K. K. Yang *et al.*, “Delay-locked loops-an overview,” *Phase Locking in High Performance Systems*, pp. 13–22, 2003.