RF Power Silicon-On-Glass VDMOSFETs

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***Abstract*—Applicability of vertical double-diffused MOSFETs for future base station power amplifiers has been demonstrated by characterizing the first devices fabricated in a substrate transfer silicon-on-glass technology. For a gate length of 0.8 μm and gate width of 350 μm, the measured $f_T/f_{\max}$ is 6/10 GHz, and the breakdown voltage approaches 100 V. The devices feature an output power of 12 dBm at the 1-dB compression point, excellent linearity (IM3/IM5 of $-50/-70$ dBc at 10-dB backoff) and high power gain (14 dB) at 2 GHz, and are the first vertical DMOSFETs suitable for 2-GHz power applications. Excellent heat sinking and no significant degradation of the quiescent current due to hot-carrier injection ensure thermal stability and good long-term reliability of the fabricated devices.**

***Index Terms*—Self-heating, silicon-on-glass (SOG), silicon RF power MOSFETs, substrate transfer, vertical double-diffused MOSFETs (VDMOSFET).**

I. Introduction

MODERN communication systems require highly linear and high power gain transistors. Bulk-silicon vertical double-diffused MOSFETs (VDMOSFETs) have excellent linearity, but suffer from limited high-frequency gain due to a large gate-drain capacitance and source lead inductance to ground. To reach higher RF power gain while maintaining good linearity, laterally diffused MOSFETs (LDMOSFETs) were developed [1], [2] and have become the state-of-the-art silicon devices for highly linear RF power applications [3], [4].

The RF performance of bulk-silicon LDMOSFETs has been improved mainly by introducing a field-plate electrode [5], which is shortened to the source and redistributes the fields at the edge of the gate. Thus, the breakdown voltage is increased, feedback capacitance reduced and device linearity improved. A field-plate electrode, combined with reduction of the gate area, has also been introduced in a bulk-silicon VDMOSFET [6]. However, even though gate-drain capacitance is significantly reduced, large leads inductance from source to ground still limits the RF gain of bulk-silicon VDMOSFETs.

To meet the demands of future generations of highly integrated wireless systems, new RF power device concepts are required. For instance, a thin-film silicon-on-insulator (SOI) LDMOSFET was demonstrated to be a promising technology [7]. Nevertheless, in both bulk-silicon and especially SOI device realization, inefficient heat removal from the active device negatively affects the RF performance [8]. A recently developed substrate transfer technology [9] opens possibilities of improving heat transport. Moreover, it allows freedom of choice with respect to substrate so that low loss substrates can be applied for even better passive integration, and further reduction in cross-talk and power consumption. New device and circuit topologies are also enabled by adding technological advances like back-wafer low-ohmic contacting [10] and three-dimensional IC fabrication [11].

We have combined the principle of a field-plate electrode with substrate transfer and back-wafer low-ohmic contacting in the design and fabrication of silicon-on-glass (SOG) VDMOSFETs. This letter presents the device layout and process flow along with the characterization of the first devices fabricated in a modified 0.8-μm LDMOS process, currently in production within Philips. The excellent properties of the SOG VDMOSFETs are demonstrated by measurements and simulations, and suggest that, if realized with the state-of-the-art process technology, VDMOSFETs will be a serious candidate for highly linear integrated wireless applications.

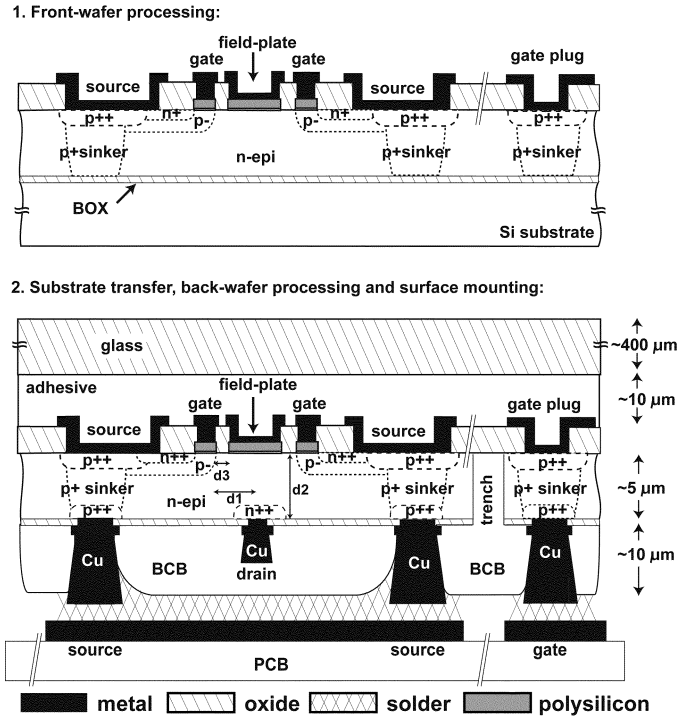

Fig. 1. Schematic of the SOG VDMOS process flow.

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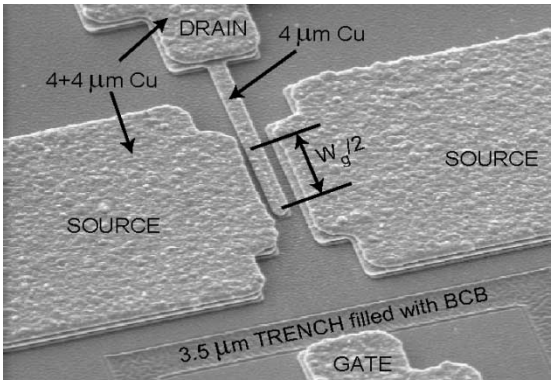

Fig. 2. Scanning electron microscopy image of two levels of copper electroplated on the back-wafer of SOG VDMOSFET. Gate width is $W_g = 70\ \mu$m.

II. Device Design and Fabrication

The substrate transfer technology divides the SOG VDMOS process flow (Fig. 1) into first a conventional front-wafer processing on the SOI starting material and second the wafer transfer to glass together with the back-wafer processing below 300 °C.

In the front-wafer processing, a production 0.8-μm bulk-silicon RF LDMOS process at Philips Semiconductors has been modified to realize the source, gate and drain epi-profile of the VDMOSFET. The n^- drain is doped to 3×10^{15} cm^{-3} by growing an n-epi followed by a blanket implantation/diffusion. The modified LDMOS processing includes p^+-sinker source and gate implantation/diffusion, a 40-nm thermal gate oxidation, poly-Si field-plate and gate electrode formation with self-aligned p-well and n^+-source implantation/diffusion, and metallization.

The substrate transfer to glass and the bulk-Si removal to the buried oxide by TMAH etching follows. This is a Philips production process, but is run at DIMES with several enhancements: the back-wafer is patterned with the same high-precision lithography as the front-wafer [12] and low ohmic n- and p-type contacts are formed by implanting, laser annealing, and metallizing with sputtered Al/Si. The gate p^+-sinkers are isolated by trench etching from the back-wafer to the front-wafer oxide. The trenches are then filled with BCB and etched back to the Al/Si. The processing continues with electroplating of a two level thick copper interconnect on the back-wafer with a Ti/TiN diffusion and adhesion barrier. The copper is covered with BCB before the devices can be soldered to a PCB. The first 4-μm-thick copper layer on the drain minimizes debiasing over long drain fingers, and the second $4 + 4\ \mu$m-thick layer to the source improves thermal conductance to the thermal ground (Figs. 1 and 2). In contrast to conventional bulk-Si VDMOSFETs, the back-wafer contacting along with copper electroplating allow the elimination of the source lead inductance and the introduction of a common thermal and electrical ground.

III. Device Characterization

In the development of the SOG VDMOSFET, several device layouts and process flows were previously considered and thoroughly analyzed [13], [14] to arrive at the device design

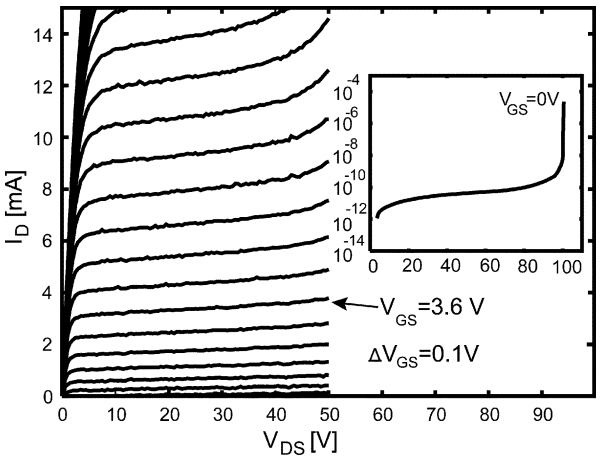

Fig. 3. Measured off-state breakdown voltage and output characteristics. Note that the measurements of the output characteristics have been performed in pulsed (isothermal) mode to avoid self-heating of on-wafer devices. Therefore, the behavior of the mounted (well cooled) devices has been resembled.

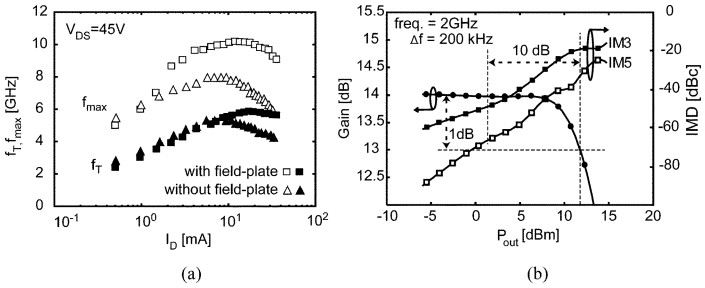

Fig. 4. (a) Measured f_T and $f_{\max}$ versus current for devices with and without field-plate electrode. (b) Two-tone transducer gain and third- and fifth-order intermodulation distortion versus output power derived with the Smoothie database model, in class AB bias condition with supply voltage $V_{\rm DD} = 26\ V$ and quiescent current $I_{\rm dq}$ of 2.1 mA. The calculation has been based on *S*-parameters measured on a large grid of drain and gate bias voltages [15]. The 1-dB compression point at an output power of 12 dBm is shown explicitly. The input and output matching networks have been optimized for a tradeoff between power gain and linearity: $\Gamma_S = 0.87\angle 25$ and $\Gamma_L = 0.90\angle 5$.

presented here. The first fully processed VDMOS transistors that are measured have a gate-to-drain distance $d_1 = 5.6\ \mu$m, a n-epi thickness $d_2 = 3.5\ \mu$m, and a distance between the gate and field-plate electrode $d_3 = 1\ \mu$m, where all the distances are specified in Fig. 1. We focus on on-wafer measurements of single-cell devices in ground–signal–ground configuration, suitable for RF characterization, with a gate width of $W_g = 350\ \mu$m. Fig. 3 displays measured output characteristics and an off-state breakdown voltage of nearly 100 V. Pulsed *S*-parameters of the devices were measured versus bias and frequency up to 11 GHz, and f_T and $f_{\max}$ were extracted at each bias point from 20-dB/dec current gain and maximum available gain ($k > 1$) characteristics, respectively. The measured values are $f_T/f_{\max} = 5/8$ GHz for $V_{\rm DS} = 25$ V and 6/10 GHz for $V_{\rm DS} = 45$ V. In Fig. 4(a), f_T and $f_{\max}$ are plotted versus current for $V_{\rm DS} = 45\ V$ and compared to those of the device without the field-plate electrode. Furthermore, pulsed *S*-parameters were measured on a large grid of bias points. This measured data, which also contains all the device parasitics, was used without scaling as input for the Smoothie database model that has already been proven to yield very accurate calculations of RF performance [15]. Smoothie load-pull analysis at

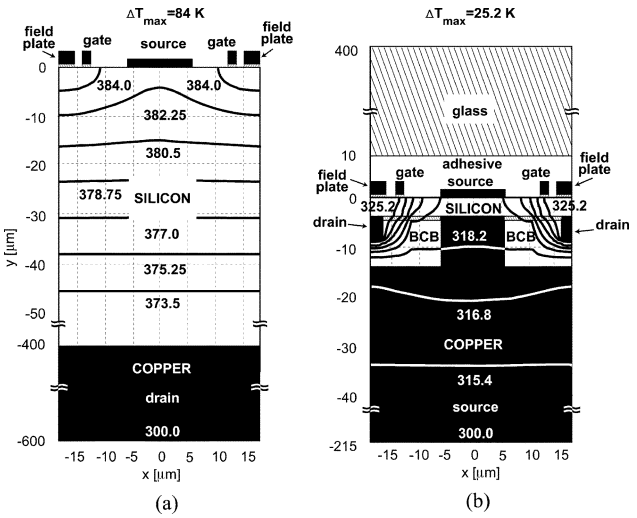

Fig. 5. Numerically calculated temperature profile of a middle section of devices with infinite number of sections: (a) bulk-Si and (b) SOG VDMOSFET. The power density distribution is calculated by MEDICI [18] for $V_{\rm DS} = 26$ V and $I_D = 25\ \mu$A/μm and used as an input for the thermal simulator Femlab [17]. The thermal simulations have been performed for an input dc power of $I_D V_{\rm DS} = 0.650$ mW/μm. For sections with $W_g = 350\ \mu$m this corresponds to power of 227 mW per section. The thermal conductivities of silicon, copper, glass (oxide, adhesive), and BCB are 150, 400, 1.4, and 0.7 W/mK, respectively.

2 GHz yields, in class-AB bias conditions, a two-tone power gain as high as 14 dB, and IM3/IM5 of $-50/-70$ dBc at 10-dB backoff [Fig. 4(b)]. This procedure, applied to bulk-Si RF-LDMOSFET with comparable W_g and fabricated in the same production line, yields two-tone power gain of 15 dB and IM3/IM5 of $-40\ -55$ dBc at 10-dB backoff.

SOG VDMOSFETs experience no significant degradation of the quiescent current $I_{\rm dq}$ due to hot-carrier injection, since the maximum electric field along the current path is far away from the gate oxide [14]. Standard $I_{\rm dq}$ degradation measurements [16] confirm this and indicate degradation of less than 10% in 20 years, which is very good considering their RF performance and also much better than the same production line LDMOSFETs. No additional efforts have been made here to engineer the drain profile in order to minimize the degradation. Furthermore, temperature distributions shown in Fig. 5, numerically calculated [17] for large, high-power devices, predict that a SOG VDMOSFET, when soldered onto a thermally conducting substrate, features much lower temperature increase than the corresponding bulk-silicon device soldered to the same substrate. This is due to the much closer proximity of the heat sink to the active devices achieved by substrate transfer and surface mounting.

IV. Conclusion

The first fabricated SOG VDMOSFETs feature an $f_T/f_{\rm max}$ of 6/10 GHz, breakdown voltage of 100 V, excellent linearity and high power gain at 2 GHz, very good thermal stability and long-term reliability. The special elements of this device design have been proven to be instrumental in enhancing RF performance of power MOSFETs.

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