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A Novel Modular Heatsink Antenna Array with Beam Scanning and Cooling Benefits

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***Abstract*—An antenna array with dual-functionality - electromagnetic radiation and thermal cooling - is proposed. An iterative array design procedure is developed to improve cooling, mutual coupling, side lobe levels, and gain levels in dual-functional antenna arrays with adaptive beam steering. Heatsink-attached patch elements are combined with complementary split ring resonator (CSRR) structures in between the elements, resulting in a novel modular heatsink antenna array. Based on the proposed design, the beam scanning performances of four-element and eight-element linear arrays at 26 GHz are studied. A conventional shorted patch antenna array is used for benchmarking. Through thermal and electromagnetic simulations, it is demonstrated that the proposed antenna array decreases the maximal array temperature by more than 40^oC as compared to the benchmark. Moreover, the new design resolves the pattern performance degradation problems in heatsink arrays, while approaching to the electromagnetic performance of the benchmarked array.**

***Index Terms*—antenna cooling, beam switching, complementary split-ring resonator, heatsink antenna, mutual coupling.**

I. Introduction

In active phased arrays for next-generation communication and sensing applications, heat-generating beamformer circuits (chips) are integrated with the antenna elements [1]–[3]. At millimeter-waves and beyond, the inefficiency of the power amplifiers with linearity requirements leads to an extreme heat density [4]–[6]. Attaching a large conventional heatsink or coldplate at the chip surfaces allows transferring and removing part of the heat via natural or forced convection at the air or liquid interfaces [7], [8]. However, the cooling of such systems is single-sided, the capacity of which is limited by the fin or plate efficiencies [9].

Dual-functional antennas with heat dissipation capabilities offer attractive design solutions to enhance cooling [10]. Researchers demonstrated the potential of using planar [11] and metal-based three-dimensional heatsink-shaped antenna elements [12]–[14], as well as frequency selective surfaces (FSS) in between the elements [15]. Modern additive manufacturing techniques promise low-cost realization of such unconventional designs [16], [17]. However, to the authors knowledge, there is still a gap in fundamental knowledge on how to combine the heatsink antennas with FSS to mitigate the mutual coupling and to achieve adaptive beam steering.

In our recent work [18], we presented a two element array of pin-finned heatsink antennas at 26 GHz with complementary split ring resonator (CSRR) embedded isolation wall. While reducing the chip temperature by 40^oC as compared to conventional patches, the design achieves below -25dB mutual coupling at the design frequency. However, the radiation pattern performance was limited to beam switching under three beam states looking at -30^o, 0^o and 30^o, with an average gain of 7 dBi over the field-of-view. In this paper, inspired by our earlier works in this topic [13], [18], we propose a novel design extension towards an adaptive beam steering array with modularity in the unit cell (i.e. element and FSS) layout. We also study, for the first time, (i) the effect of heatsink array length on the beam scanning performance, and (ii) the effect of number of chips on the cooling performance. We compare our results with a standard shorted-patch antenna array for benchmarking.

The rest of the paper is organized as follows. Section II describes and motivates the antenna arrays under study. Section III lists the settings and parameter values for the thermal and electromagnetic simulations. Section IV presents and discusses the simulation results. Section V concludes the paper.

II. Antennas Under Study

In this study, we consider five different 4-element antenna array designs labeled as Ant. A-E. This section gives an overview of the selected antenna arrays, and explains the design iterations with the thermal and electromagnetic motivation behind them. This motivation will then be linked to the simulation results in Section IV.

All antenna variations employ a rectangular patch, which is fed with a probe fed with a coaxial line. The conventional shorted patch antenna (Ant. A), is shown in Fig. 1(a). It inherently has a thermal conduction path (the shorting wall) combined with the well-known properties of the rectangular patch antenna. Although Ant. A has a thermal path from the ground plane (which can be thermally-connected to an RF chip) to the antenna surface, the additional cooling provided by it is not sufficient [7].

Ant. B combines the shorted patch with a heatsink that we introduced in our earlier work [13]. The heatsink increases the convection surface, yielding lower RF chip junction temperature (T_{junc}). The isometric view of the HS array can be seen in Fig. 1(b).

Despite its enhanced cooling capacity, Ant.B has mutual coupling and gain problems in the high scan angles. To address this problem, another iteration is made by adding a CSRR wall [18], which results in Ant. C. The CSRR reduces mutual

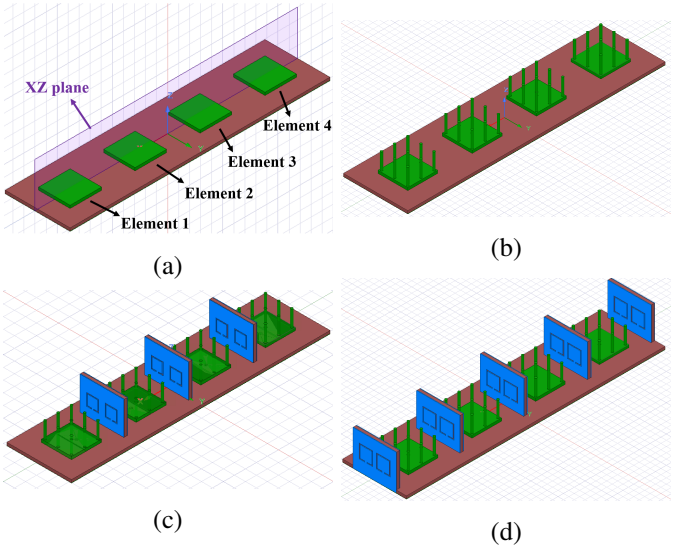


Fig. 1. Isometric view of the antennas under study: (a) shorted patch array (Ant. A), (b) heatsink antenna array (Ant. B), (c) heatsink array with three uniform CSRR walls (Ant. C), (d) heatsink array with five uniform CSRR walls (Ant. E). Note that Ant. D is not shown due to invisible differences in the picture as compared to Ant. C.

coupling caused by radiation. The walls are placed between elements 1-2, 2-3, and 3-4, as can seen in Fig. 1(c).

Ant. C performs very well in terms of the isolation between elements 1-2 and 3-4. However, the middle elements of the array still suffer from excessive coupling, resulting in high side lobe levels in high scan angles. This problem is further addressed by applying non-uniform CSRR walls between elements. The dimension of the CSRR wall in the middle is optimized to reduce coupling between elements 2-3. This non-uniform design is called Ant. D.

Since Ant. D increases the complexity of the design by non-uniform CSRR strategy without supplying sufficient radiation improvement, in the final iteration, uniform CSRR structures are used again. However, now the CSRR walls are also used at the end of the Element 1 and 4, which leads to Ant. E. The isometric view and the placement of the uniform CSRR walls in Ant E can be seen in Fig. 1(d).

III. Simulation Model Settings

A. Thermal Aspects

A computational fluid dynamics (CFD) based simulation is performed using ANSYS ICEPAK software. In these simulations, RF chips are modeled by following the two-resistor compact thermal model [7]. In the model, we assumed a thermal lumped network for a chip with $R_{jc} = 10K/W$ and $R_{jb} = 14K/W$ [7], [8]. The simulation environment is arranged to fit in the cooling under a slow air motion scenario; therefore, a constant air input with 1 m/s velocity is applied in the zy-plane. The chip heat power value is arranged to 0.5W per channel in the simulations, which follows the observations from a mm-wave array prototype [8]. The side view of the ICEPAK simulation environment can be seen in Fig. 2. The thermal model consists of an RF chip that makes a thermal

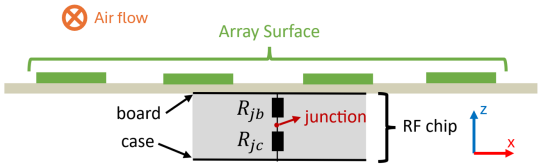


Fig. 2. Side view of the generic ICEPAK simulation environment and the thermal model of the RF chip (with four channels in this figure) [18].

connection to the ground of the array. The antenna elements at the array surface are modified for the corresponding antenna under test.

B. Electromagnetic Aspects

Throughout this study, all antennas are designed by employing Rogers 4003 dielectric with 0.25 mm thickness. Also, all the arrays are formed with the interelement distance equal to half-wavelength ($\lambda/2$) at 26 GHz. Starting from Ant. B designs include heatsink antenna structures. In these arrays, a square patch with a 2.73 mm edge length is employed, and nine cylindrical fins are separated by a 1.2mm distance that has a 1.75 mm height and 0.1 mm radius.

The CSRR design in the other antennas under test follows the LC model of the resonator. The relationship between the resonator dimension and the notch frequency can be found in Eq. 1.

$$f_0 = 1/(2\pi\sqrt{L_{net}C_{net}}) \quad (1)$$

This formulation relates the induction and capacitance introduced by split ring resonator (SRR) and can also be used for CSRR due to duality. L_{net} is the total inductance introduced by the slot, and it is related to the circumference of the resonator and the gap distance. On the other hand, the C_{net} illustrates the capacitance introduced by the slot and the parallel plate structure; therefore, it depends on the dielectric constant and characteristic impedance of the slot as well as the dimensions of the slot [18], [19].

In our designs, an initial dimension value is calculated by Eq. 1, and the dimensions are adjusted in a full wave simulation environment. Rogers 4003, with 0.25 mm thickness, is used as the dielectric material of the CSRR. After deciding the dimension of one slot, another slot is added with

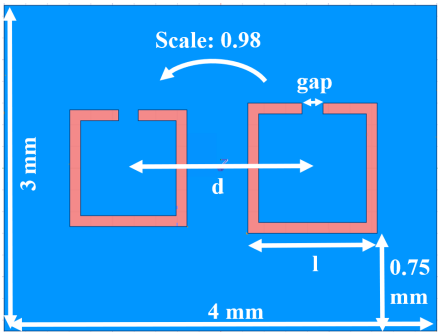


Fig. 3. Side view and dimensions of the CSRR wall.

a small scale factor to provide bandwidth similar to the antenna itself. The CSRR wall and its dimensions can be seen in Fig. 3. Dimensions of the CSRR wall illustrates small changes compared to Ant C, D, and E. The dimension values of CSRR walls employed in these antennas can be seen in Table I.

TABLE I
DIMENSIONS OF THE CSRR WALL USED IN ANT C, D, AND E

		gap [mm]	d [mm]	l [mm]
Ant C		0.2	1.9	1.28
Ant D	Middle	0.2	1.7	1.26
	Side	0.2	1.7	1.28
Ant E		0.2	1.6	1.26

IV. SIMULATION RESULTS

A. Thermal Performance

The analysis is conducted considering two RF chip cases. The first case uses RF chips that have two channels feeding two antennas per chip. In this configuration, 1W per chip is generated. On the other hand, the second configuration assumes each RF chip has four channels; therefore, it employs one chip per four antennas. The chip power of the second case is selected as 2W, assuming the generated heat increases linearly with the increase in the channel and number of power amplifiers. The junction temperatures simulated for these chip conditions are summarized in Table II. As the difference between Ant C and D is the shape of the slot in the middle CSRR structure, they have same thermal performance.

Each antenna iteration increases the cooling ability of the array considerably. The introduction of the heatsink antenna instead of a shorted patch reduces the T_{junc} by 20.5 C^0. The T_{junc} is further reduced by 22 C^0 with the addition of the CSRR walls. T_{junc} values of the 2-channel chip are better than the 4-channel chip. This is because the 2-channel chip uses multiple heat sources, so it spreads the heat more evenly compared to the 4-channel chip. The surface temperature distribution and the airflow vectors of 2 and 4-channel chip cases can be seen in Fig. 4.

The cooling benefits in Ant. E can also be observed in larger arrays with modularity. The eight-element array extension of the Ant. E results in almost the same T_{junc} values with a difference smaller than 1^oC.

TABLE II
COMPARISON OF THE T_j OF ANT. A, B, C, D AND, E CONSIDERING DIFFERENT NUMBER OF RF CHIPS

	Ant A T_j [C^0]	Ant B T_j [C^0]	Ant C & Ant D T_j [C^0]	Ant E T_j [C^0]
2 Channel Chip (1W per chip)	143.28	122.68	107.4	100.52
4 Channel Chip (2W per chip)	166.92	146.43	130.3	124.4

B. Electromagnetic Performance

1) Coupling and Maximal Gain Performance: The initial step in the design iteration from Ant. A to Ant. B is taken due to thermal considerations. Although Ant. B satisfies the thermal constraints, it suffers from the high mutual coupling having $S_{21} = -8.9$ dB and $S_{32} = -12.7$ dB, as can be seen in Table II.

Another antenna iteration is made to improve coupling performance by adding a uniform CSRR structure introduced between elements. The CSRR structure is designed for 26 GHz by following the dimensions mentioned in Fig. 3. The introduction of the CSRR wall improved the coupling parameters. The S-parameters of Ant. C reduced to $S_{21} = -24.4$ dB and $S_{32} = -15.9$ dB as seen in Fig. 5. The increase in port isolation plays an important role in determining the realized gain values at the high scan angles. Maximal realized gain for the $\theta = 45^0$ scan is increased from 6.51 dB to 8.71 dB, as can be seen in Table III.

Although Ant. C performs well in the maximal gain, it needs an improvement in the side lobe level and S_{32} parameter. The coupling mechanism experienced by the Element 1&4 (edge elements) and element 2&3 (middle elements) are different. To compensate for coupling differences, we change the dimensions of the CSRR located in the middle of the array to compensate for additional interference experienced by the middle elements.

The S-Parameter graph in Fig. 5 illustrates that the S_{32} curve has a local minimum at 26.3 GHz in Ant. C. The idea of using a non-uniform CSRR arises from this observation; it aims to shift the local minimum point of the S_{32} value to 26 GHz by changing the dimension of the slot on the middle wall only. After optimizing the CSRR dimension of the middle wall, the local minimum point of the S_{32} is shifted to the 26 GHz, leading to Ant. D. The shift in the S_{32} is obtained by scaling slots on the CSRR surface with the factor 0.96. Ant. D reduces the S_{32} parameter to -25.64 dB. Although Ant. D improves the coupling performance, it suffers from two issues;

- The non-uniform CSRR design introduces another level of complexity both in design and manufacturing perspectives,
- Uniform CSRR (Ant. C) provides higher gain values, especially in high scan angles.

The antenna iterations starting from Ant. B to Ant. D highlight the importance of the CSRR wall regarding isolation

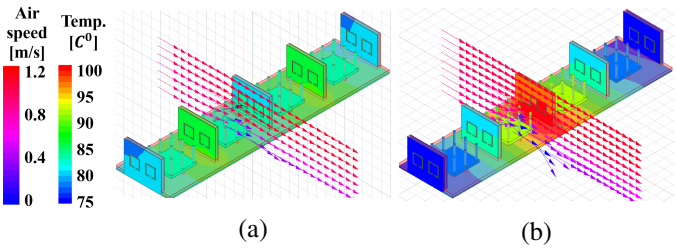


Fig. 4. Surface temperature and air vector distribution in Ant. E: (a) 2-channel, and (b) 4-channel chips.

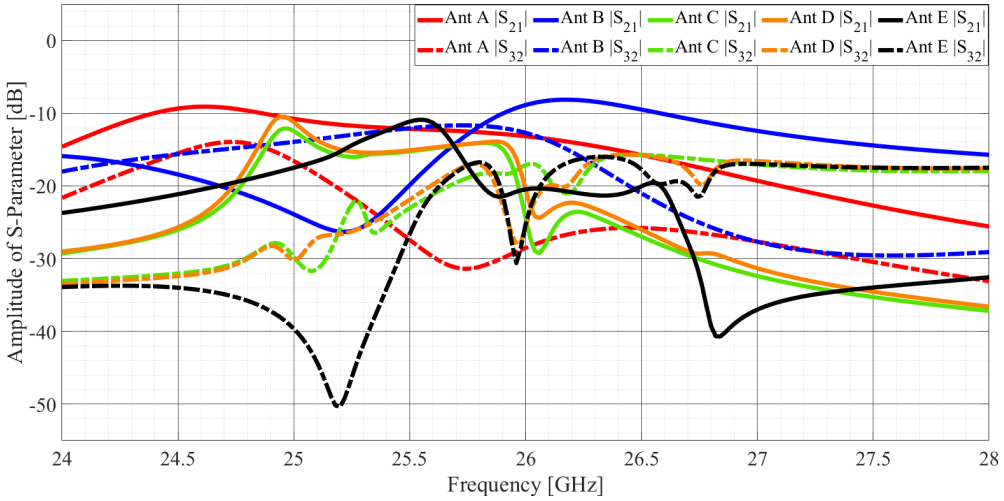


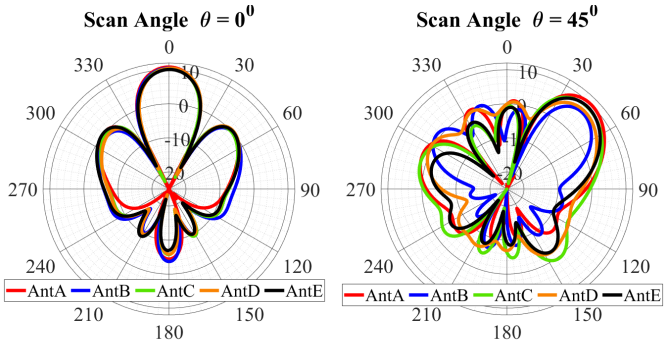
Fig. 5. S_{21} and S_{32} values for Ant. B,C,D and E.

TABLE III
COMPARISON OF S_{21}, S_{32}, MAX. REALIZED GAIN AND NORMALIZED SIDE LOBE LEVELS OF ANT. A, B, C, D,AND E

Array Type	S-Parameter @ 26GHz [dB]	Max Realized Gain [dB]		Normalized Side Lobe [dB]	
		Scan Angle $\theta = 0^0$	Scan Angle $\theta = 45^0$	Scan Angle $\theta = 0^0$	Scan Angle $\theta = 45^0$
Ant A	$S_{21} = -13.17$ $S_{32} = -28.5$	10.8	10	-10.56	-8.2
Ant B	$S_{21} = -8.9$ $S_{32} = -12.7$	10.51	6.51	-10.48	-5.43
Ant C	$S_{21} = -24.4$ $S_{32} = -15.9$	10.37	8.71	-10.51	-7.14
Ant D	$S_{21} = -20.49$ $S_{32} = -25.64$	10.46	7.24	-10.03	-6.59
Ant E	$S_{21} = -20.5$ $S_{32} = -25.26$	10.08	8.81	-9.91	-10.01

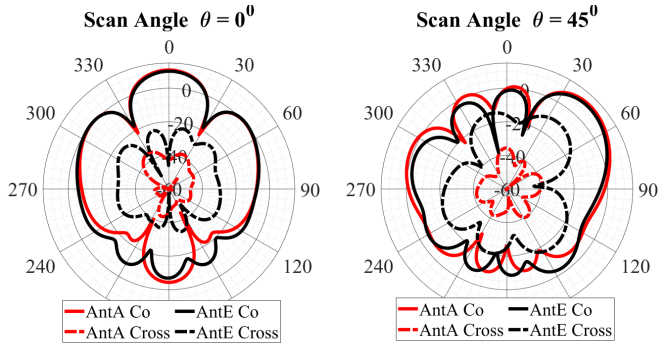
and maximum realized gain values. Although the CSRR wall improves these measures, the gain values at high scan angles are not improved. Therefore, in the final iteration (Ant. E), we propose using uniform CSRR walls for both sides of the edge elements. Using five consecutive CSRR walls improves the coupling levels, maximum gain at high scan angles and thermal performance.

2) Padiation Pattern Performance: The radiation pattern of the array is also highly improved through the design procedure. The realized gain plots of all the arrays under study in the xz plane can be seen in Fig. 6. It is observed that Ant. E outperforms the others in terms of the side lobe and maximal gain values in the $\theta = 45^0$ scan case. Furthermore, the co- and cross-polarization patterns of linearly-polarized Ant. E can be seen in Fig. 7. The large difference between its co- and cross-polarization components proves the linear polarization of the array. Even though Ant. E preserves its linear polarization behavior, the cross-polarization value is increased compared to Ant A. This increase occurs due to the vertical positioning of the fins in the heatsink structure. The currents extended on the fins increase the cross-polarized radiation.



(a) (b)

Fig. 6. Realized gain (in dBi) of Ant. A, B, C, D and E: (a) broadside radiation, (b) $\theta = 45^o$ scan angle.



(a) (b)

Fig. 7. Co- and cross-polarization pattern of Ant. A and Ant. E: (a) $\theta = 0^o$ and (b) $\theta = 45^o$ scan.

So far, all array investigations are done considering four-

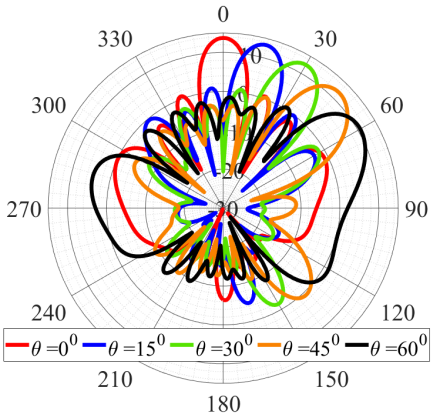


Fig. 8. Array pattern of the eight-element array of Ant. E under beam scanning.

element topologies. However, the pattern performance of a four-element array is limited in terms of the maximum scan angle. In order to scan the beam to higher angles, a modular extension of Ant. E is also studied. The eight-element array version of Ant. E is capable of continuous steering from $\theta = 0^o$ to $\theta = 60^o$ as seen in Fig. 8. Thanks to the CSRR walls, the relative side lobes always stay under -10 dB, even in the high scan angles. The eight-element array also has relatively low coupling levels such that all S_{ij} magnitudes are less than -18.5 dB at 26 GHz.

V. Conclusion

By combining heatsink-attached patch elements with CSRR structures, a unique modular heatsink antenna array has been designed. The proposed iterative design procedure enhances the antenna system performance by simultaneously addressing cooling, mutual coupling, side lobe level, and gain requirements. Evaluation of the beam scanning abilities of four-element linear arrays operating at 26 GHz based on this design has illustrated the dual-functional performance benefits and trade-offs. Comparative studies with a traditional shorted patch antenna array as a benchmark have demonstrated that the proposed antenna array significantly reduces the maximum chip temperature by over 40^{o}C. Furthermore, the proposed design provides high port isolation values of $|S_{ij}| < -20$ dB while keeping beam scanning capability ($\pm 45^o$) and realized gain values (around 10 dBi) similar to the benchmark. In exchange, the heat-dissipating fins increase the cross-polarization levels. With the modularity, increasing the array size enables beam scanning towards higher angles, reaching up to $\pm 60^o$ with eight elements while maintaining the same cooling performance.

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