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Development of metal contacts with screen printing for n^+ polysilicon/SiO_x passivated silicon solar cells

Development of metal contacts with screen printing for n^+ polysilicon/SiO_x passivated silicon solar cells

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by

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To my parents and sister

Science is a wonderful thing
if one does not have to earn one's living at it.
Albert Einstein

Contents

Summary

The continued reliance on fossil fuels to satisfy the world energy demand is leading to climate change, accelerating the melting of polar ice shelf, and is dealing irreversible damage to the flora and fauna of earth, to name few of the adverse effects from fossil fuel utilisation. In addition to not being renewable, fossil-fuel resources are also limited. Therefore these resources cannot meet the energy demand at some point in future. The most plausible way is to utilise renewable sources of energy to meet the increasing demand of energy. The Sun, our closest star is the answer to this demand. Utilising the abundant solar radiation arriving at earth to generate electricity is a great way. A photovoltaic (PV) solar cell can achieve this by converting the incident sunlight directly to electricity.

The most commonly used PV solar cells are made using crystalline silicon (c-Si) as absorber material. The theoretical maximum efficiency that can be achieved with c-Si solar cells is 29.43% (depending on the thickness), while the highest efficiency achieved by researchers is 26.7%, at the time of writing this thesis. Currently, the industrially produced c-Si cells have efficiencies in between 21-23%, hence it becomes imperative to develop strategies and architectures that can have even higher efficiencies in order to bridge the gap to the theoretical efficiency as much as possible. One of the most promising strategy involves the use of a highly doped n^+ polysilicon layer and a thin interfacial oxide passivating layer stack. To utilise this layer stack to its potential it is important to suppress the recombination and current transport losses after the metallisation process.

This thesis provides the results of a systematic investigation into screen-printed metallisation for a stack consisting of highly doped n^+ polysilicon layer and a thin interfacial oxide (SiO_x) passivating layer. Finally, the studies presented in this thesis culminate to an industrial sized (M2) champion device with an efficiency of 22.26% with a rear side n^+ polysilicon/SiO_x passivated contact, which is completely fabricated with high through-put industrial process.

This thesis is divided into nine different chapters. The first chapter presents a brief overview to renewable energy and photovoltaic energy conversion in particular. The next chapter explains fundamental concepts of c-Si solar cells and discusses in more detail different c-Si solar-cell architectures. Special attention is paid to the metal-semiconductor contacts as this is the main topic of this thesis. In Chapter 3, sample processing steps as well as the metallisation process used throughout this work are explained. Chapter 4 discusses the characterisation and measurement techniques used in this work.

Chapter 5 is dedicated to the experiments with different fire-through silver pastes with the objective to find the silver paste that provides the lowest metal-polysilicon recombination current density ($J_{0\mathrm{met}}$) and contact resistivity (ρ_c) for the n^+ polysilicon/SiO_x based contact. These two parameters are used throughout the

thesis in order to quantify the Ag-n^+ polysilicon/SiO_x contact. In order to investigate the damage to the n^+ polysilicon/SiO_x layer stack after metallisation, we utilised high resolution SEM images. We also present a Python-based analysis routine in order to analyse the SEM images quantitatively for comparison between different samples. Using this routine we computed the density of sites where the n^+ polysilicon/SiO_x layer stack was damaged, and correlated these data to the $J_{0\mathrm{met}}$ values. The silver paste with which the best results for the contact properties were obtained is used in the later experiments presented in this thesis. $J_{0\mathrm{met}}$ values below 50 fA.cm^{-2} coupled with ρ_c values below 2 mΩ.cm^2 are obtained, which demonstrates the high potential of a passivating contact based on n^+ polysilicon/SiO_x layer stack. A section in this chapter is specifically dedicated to understanding the contact resistivity of the Ag-n^+ polysilicon/SiO_x. The experiments in this section show that the effect of the n^+ polysilicon/SiO_x layer underneath the metal contact is a dominating factor in the contact resistivity measurements based on transmission line method. When varying the n^+ polysilicon/SiO_x width we found that the contact resistivity increases if the width is reduced.

In Chapter 6, we compare the properties of n^+ polysilicon/SiO_x contact structures to conventional phosphorus diffused contacts. For this comparison we also varied the fast-firing peak temperature during final metal contact formation, as this temperature affects the metal-polysilicon recombination current density and contact resistivity. We found that samples with n^+ polysilicon/SiO_x contacts had higher implied open-circuit voltage and lower recombination current density than samples with phosphorus diffused contacts. The metal-polysilicon recombination current density and contact resistivity that characterize the contact properties are also presented. We found that the metal-polysilicon recombination current density for the samples with a n^+ polysilicon/SiO_x contact is significantly lower than those of the samples with a conventional phosphorus diffused contact. The contact resistivity, meanwhile is also lower for the samples with the n^+ polysilicon/SiO_x contact as compared to the samples with conventional phosphorus diffused contacts. This motivates the use of n^+ polysilicon/SiO_x contact in place of the conventional phosphorus diffused contact (especially at the rear side of cells).

Chapter 7 presents the results of studies pertaining to the effect of n^+ polysilicon layer thickness on the passivating (implied open-circuit voltage and recombination current density) and contact properties ($J_{0\mathrm{met}}$ and ρ_c) of the contact. We find that the n^+ polysilicon layer thickness has no apparent effect on the implied open-circuit voltage and recombination current density. However, a change in thickness does influences the contact properties. Samples with thicker polysilicon layer have lower $J_{0\mathrm{met}}$ and ρ_c values than samples with thinner polysilicon layer. The changes in the $J_{0\mathrm{met}}$ and ρ_c of the samples with different thickness of polysilicon layer are explained by the removal of the n^+ polysilicon layer by the silver paste constituents, as observed in cross-sectional SEM images, and exposing the underlying silicon that is not passivated anymore.

Chapter 8 details a systematic study on the influence of different substrate surface finish/morphology on the contact properties of the n^+ polysilicon/SiO_x contact. It is important to understand the effect of the morphology on the passivation and

contact properties of the n^+ polysilicon/SiO_x contact, as the processing flow during cell fabrication leads to different surface morphologies. This study reveals that a planar substrate surface finish has a lower $J_{0\mathrm{met}}$ than surfaces that are more rough and hence will lead to a better solar-cell performance when combined with n^+ polysilicon/SiO_x layer stack. We also show that by increasing the polysilicon layer thickness the recombination losses arising due to the use of rougher surfaces can be compensated. However, a thick polysilicon layer is not recommended in an optimally designed solar cell as it leads to extra absorption losses. Hence, there is no apparent overall gain in performance.

Based on the results of the earlier chapters, in Chapter 9 a process chain is demonstrated in order to upgrade the existing industrial nPERT solar cell to a higher efficiency solar cell using a n^+ polysilicon/SiO_x passivated contact at the rear. We utilise different silver grid designs as well as improved front side passivation strategies involving aluminium oxide layer in order to increase the device efficiency. Finally, we demonstrate the best efficiency of 22.26% for devices with rear side n^+ polysilicon/SiO_x passivated contact, which is 1.4% absolute efficiency improvement from our champion nPERT cell. Simulations with Griddler 2.5PRO are also used in understanding the losses in the fabricated cells as well as the pathways to further increase the device efficiency. The simulations point out that the recombination losses on the emitter side are limiting the efficiency of the rear side n^+ polysilicon/SiO_x passivated contact cell.

Samenvatting

De afhankelijkheid van fossiele brandstoffen om aan de energievraag van de wereld te voorzien leidt tot klimaatverandering, versnelt het smelten van de ijskappen, en resulteer in onherstelbare schade aan de flora en fauna van de aarde, om een paar nadelige effecten van het gebruik van fossiele brandstoffen te noemen. Naast dat energie gebaseerd op fossiele brandstoffen niet hernieuwbaar zijn, zijn de reserves daarvan ook beperkt. Daarom zullen deze brandstoffen op enig moment in de toekomst niet aan de energievraag kunnen voldoen. De meest voor de hand liggende manier is de inzet van hernieuwbare energiebronnen om aan (groei van) de energievraag te voldoen. Het gebruik maken van overvloedig beschikbare zonne-energie die de aarde bereikt is een mooie manier om elektriciteit te genereren. Een fotovoltaïsche (photovoltaic; PV) zonnecel kan dit realiseren door de directe omzetting van zonlicht naar elektriciteit.

De meest toegepaste PV zonnecellen gebruiken kristallijn silicium (c-Si) als licht absorberend materiaal. Het theoretisch maximaal energieconversie rendement dat met zonnecellen gebaseerd op c-Si behaald kan worden is 29,43% (afhankelijk van de dikte), terwijl het hoogst door onderzoeker behaalde rendement nu 26,7% is, bij het schrijven van dit proefschrift. Op dit moment hebben industrieel geproduceerde zonnecellen van c-Si rendementen van 21-23%, en daarom is het belangrijk om strategieën te ontwikkelen waarmee nog hogere rendementen behaald kunnen worden om zo het gat met het maximale theoretisch rendement zoveel mogelijk te dichten. Een van de meest veelbelovende strategieën is het gebruik van een laag van zwaar gedoteerd $^{+}$ polysilicium in combinatie met een dunne oxidelaag aan het interface als passiverende lagen. Om deze lagen optimaal te benutten is het belangrijk om recombinatie- en transportverliezen na het aanbrengen van de metaallagen te onderdrukken. Dit proefschrift beschrijft de resultaten van een systematisch onderzoek naar het aanbrengen van metaallagen met behulp van de zeefdruk techniek (screen printing) op lagen bestaande uit een laag van zwaar gedoteerd n+ polysilicium en een dunne siliciumoxidelaag (SiO_x) aan het interface. De resultaten van het onderzoek gepresenteerd in dit proefschrift hebben uiteindelijk geleid tot het beste rendement van 22,26% voor een zonnecel met een n^+ polysilicium/SiO_x passiverend contact aan de achterzijde en met een industriële afmeting M2. Deze cel is geheel gefabriceerd met een industrieel proces dat gericht is op hoge doorvoer.

Dit proefschrift is onderverdeeld in negen hoofdstukken. Het eerste hoofdstuk presenteert een beknopt overzicht in hernieuwbare energie en fotovoltaïsche energieconversie in het bijzonder. In het tweede hoofdstuk worden fundamentele aspecten van c-Si zonnecellen uitgelegd en worden verschillende ontwerpen in detail meer bediscussieerd. In het bijzonder wordt aandacht besteedt aan metaal-halfgeleider contacten, omdat dit het hoofdonderwerp van dit proefschrift vormt.

In hoofdstuk 3 worden de fabricagestappen van samples alsook het maken van metaallagen uitgelegd zoals het in het werk voor dit proefschrift is gebruikt. De karakteriserings- en meettechnieken die in dit werk zijn gebruikt worden bediscussieerd in hoofdstuk 4.

In hoofdstuk 5 komen de resultaten van experimenten aan bod waarin verschillende fire-through zilverpasta's zijn gebruikt met het doel om de zilverpasta te vinden die de laagste recombinatiestroomdichtheid ($J_{0\mathrm{met}}$) aan de overgang tussen zilver en polysilicium geeft en de laagste contactweerstand (ρ_c) voor het contact gebaseerd op n^+ polysilicium/SiO_x lagen. Deze twee parameters worden door het gehele proefschrift gebruikt om het contact tussen het zilver en n^+ polysilicium/-SiOx lagen te kwantificeren. Om de schade aan de n^+ polysilicium/SiO_x lagen te onderzoeken na het aanbrengen van de zilverlaag, hebben we SEM foto's genomen. We presenteren ook een analyseroutine gebaseerd op Python waarmee de SEM foto's van verschillende samples kwantitatief vergeleken kan worden. Gebruikmakend van deze routine hebben we de dichtheid van locaties berekend waar de n^+ polysilicium/SiO_x lagen beschadigd waren en deze gegevens gecorreleerd met de $J_{0\mathrm{met}}$ data. De zilverpasta waarmee de beste resultaten voor de contacteigenschappen werden behaald, is gebruikt in experimenten die later in dit proefschrift worden gepresenteerd. $J_{0\mathrm{met}}$ waarden beneden 50 fA.cm^{-2} samen met ρ_c waarden beneden 2 mΩ.cm^2 zijn verkregen, wat het hoge potentieel laat zien van passiverende contacten gebaseerd n^+ polysilicium/SiO_x lagen. Een sectie in dit hoofdstuk is specifiek gewijd aan het begrijpen van de contactweerstand van de overgang tussen het zilver en n^+ polysilicium/SiO_x lagen. De resultaten van experimenten die in deze sectie beschreven worden laten zien dat de dikte van n^+ polysilicium/SiO_x lagen een dominerende factor is in de metingen van de contactweerstand met de zogenaamde transmission-line methode. We vonden dat de contactweerstand groter werd als de dikte van de n^+ polysilicium/SiO_x lagen kleiner werd.

In hoofdstuk 6 vergelijken we de eigenschappen van n^+ polysilicium/SiO_x contact structuren met conventionele fosfor-gediffundeerde contacten. Voor deze vergelijking hebben we ook de piektemperatuur tijdens het fast-firing proces gevarieerd tijdens het maken van het metaalcontact, aangezien deze temperatuur de recombinatiestroomdichtheid aan de overgang tussen metaal en polysilicium, en de contactweerstand beïnvloedt. We vonden dat n^+ polysilicium/SiO_x contacten een hogere geïmpliceerde openklemspanning en lagere recombinatiestroomdichtheid hadden dan fosfor-gediffundeerde contacten. De recombinatiestroomdichtheid aan het aan de overgang tussen metaal en polysilicium en de contactweerstand die de contacteigenschappen karakteriseren worden ook getoond. We vonden dat de recombinatiestroomdichtheid aan de overgang tussen metaal en polysilicium van samples met een n^+ polysilicium/SiO_x contact significant lager was dan van samples met een conventioneel fosfor-gediffundeerd contact. Ook de contactweerstand van samples met een n^+ polysilicium/SiO_x contact is lager in vergelijking met een conventioneel fosfor-gediffundeerd contact. Op basis van deze bevindingen zullen n^+ polysilicium/SiO_x contacten worden gebruikt in plaats van conventionele fosfor gediffundeerde contacten (vooral aan de achterkant van de cellen).

Hoofdstuk 7 laat resultaten zien van een studie waarin het effect van de dikte

van de n^+ polysilicium laag op de passivering- (gekarakteriseerd door de geïmpliceerde openklemspanning en de recombinatiestroomdichtheid) en contacteigenschappen (gekarakteriseerd door $J_{0\mathrm{met}}$ en ρ_c) van het contact is onderzocht. We hebben gevonden dat de dikte van de n^+ polysilicium laag geen effect heeft op de geïmpliceerde openklemspanning en de recombinatiestroomdichtheid. Echter, de verandering van de dikte heeft wel invloed op de contacteigenschappen. Samples met een dikkere polysilicium laag hebben lagere $J_{0\mathrm{met}}$ en ρ_c waarden dan samples met een dunne polysilicium laag. De verandering van $J_{0\mathrm{met}}$ en ρ_c met de dikte van de lagen wordt verklaard door het weghalen van de n^+ polysilicium laag door bestanddelen in de zilverpasta, zoals te zien is in SEM foto's van een doorsnede van de samples, waardoor het onderliggende silicium niet meer gepassiveerd is.

In Hoofdstuk 8 worden de resultaten van een systematische studie beschreven waarin de invloed van verschillende oppervlaktestructuren (morfologie) op de contacteigenschappen van n^+ polysilicium/SiO_x contacten zijn onderzocht. Het is belangrijk om het effect van de morfologie op de passiverings- en contacteigenschappen van n^+ polysilicium/SiO_x contacten te begrijpen, omdat de volgorde van de processtappen gedurende celfabricage tot een andere morfologie kan leiden. Deze studie laat zien dat een vlak substraat een lagere $J_{0\mathrm{met}}$ heeft dan ruwe oppervlakken en daarom tot een zonnecel zal leiden met een hoger rendement wanneer n^+ polysilicium/SiO_x contacten gebruikt worden. Ook laten we zien dat recombinatieverliezen als gevolg van ruwere oppervlakken gecompenseerd kunnen worden door dikkere polysilicium lagen te gebruiken. Echter, het wordt niet aanbevolen om een dikkere polysilicium laag in een zonnecel, omdat een dikkere laag leidt tot extra absorptieverliezen waardoor er geen winst is in de prestatie van de zonnecel.

Gebaseerd op de resultaten uit de eerdere hoofdstukken, wordt in hoofdstuk 9 een proces gedemonstreerd waarmee het rendement van een industriële nPERT zonnecel verhoogd kan worden, gebruikmakend van een n^+ polysilicium/SiO_x passiverend contact aan de achterzijde van de cel. Om het rendement verder te verhogen, maken we gebruik van nieuwe ontwerpen voor de zilvercontacten aan de voorzijde van de cel alsook van passiveringstrategieën aan de voorzijde van de cel gebruikmakend van een laag van aluminiumoxide. Uiteindelijk laten we zien dat het beste rendement van 22,26% gehaald wordt voor een zonnecel met een n^+ polysilicium/SiO_x passiverend contact; dit rendement is 1,4% hoger dan de beste nPERT zonnecel tot dan toe. Met behulp van computersimulaties met Griddler 2.5PRO hebben we meer inzicht verkregen in de verliezen in deze cel en verkrijgen we een beter inzicht in manieren waarmee het rendement nog verder verhoogd kan worden. De simulaties laten zien dat in deze cel recombinatieverliezen aan de zijde van de emitter het rendement beperken.

1

Introduction

Wherever you go, no matter what the weather,
always bring your own sunshine.

Anthony J. D'Angelo

1

1.1. Outlook for renewable energy

The UN Climate Change Conference (COP)-26 in Glasgow, UK, in November 2021 again brought to attention the ever-increasing global warming due to carbon dioxide (CO_2) emission and the need to increase the amount of renewable energy in world´s current energy mix. Studies have predicted an average global temperature increase of 2-5 °C by the year 2100 [1, 2]. The predicted temperature rise will be catastrophic for the low-lying areas near oceans and several countries surrounded by oceans [3, 4]. A study predicts that it would take at least 1000 years to reverse the human-induced changes (climate change) on earth [5].

A containment strategy to climate change and global warming problem is to reduce CO_2 emissions in the energy sector by increasing the use of renewable energy sources, which would allow for a phase-out of fossil-fuel based energy sources such as coal and oil. This change is often referred to as the energy transition. This transition requires substantial financial investment in the development of technologies, such as photovoltaics (PV) and wind energy, and is expected to go hand in hand with the increase in the market size of clean energy technologies. Figure 1.1 presents the predicted market size for selected clean energy technologies [6]. Two models are utilised in these predictions: Stated Policies Scenario (STEPS), which is based on current policies, and Net-zero Emissions (NZE) scenario, which requires an extensive increase in clean energy investment in order to achieve net zero CO_2 emissions by 2050 [6]. The estimated market size in Figure 1.1 shows that the utilisation of clean energy technologies will increase in the future and it will offer new avenues of jobs, which will also benefit society. As mentioned by the World Energy Outlook 2020 report, the annual market opportunity for the five major clean technologies (wind turbines, solar panels, lithium-ion batteries, electrolysers, and fuel cells) will grow ten times to about USD 1.2 trillion, far exceeding the oil industry and its associated fields [6].

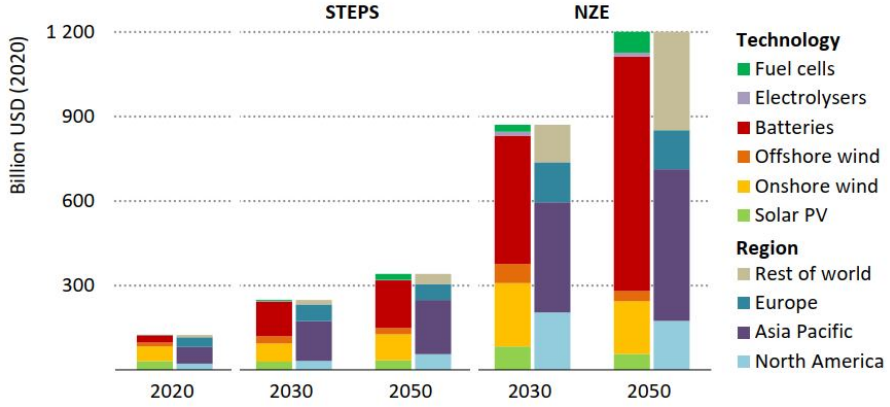

Figure 1.1: Estimated market size for selected clean energy technologies with the regions for the years 2020-2050 [6].

Photovoltaic (PV) technologies offer great promise due to the abundant avail-

ability of solar energy, and the easy scalability and installation in commercial and domestic applications. Apart from large PV farms and classical roof-top systems, buildings can be integrated with PV modules, generating electricity for their consumption; this is called as building-integrated photovoltaic (BIPV) [7]. PV modules can also be integrated into vehicles, and hence the need for gasoline or diesel can be reduced or even eliminated; this is referred to as Vehicle Integrated PV (VIPV) [8]. Agro-photovoltaics has also acquired steam in the last years, with the union of solar panels and agriculture [9, 10].

In the last couple of years, there has been tremendous work on the breakthroughs in the implementation of large-scale PV [11–14]. The Renewable 2020 Global Status report shows that almost 100 GW of PV capacity has been added every year from 2017 [15]. It is reported that 15 countries had enough capacity to meet at least 5% of their electricity demands with PV [15]. Some advanced economies such as Germany and Japan have almost 8 to 10% of their annual electricity requirements met by PV [15]. According to BP statistical review-2021, in 2020 almost 707.5 GW of installed PV power capacity was available, producing 700 TWh of electricity [14]. Dismally this is only 2.6% of the total electricity generated in the world [14].

1.2. Photovoltaic (PV) cell

To generate electricity from the sunlight, we need to install PV cells, which are simply called solar cells, across the regions which are conducive to their use. The first device to demonstrate the conversion of sunlight to electricity was developed by Charles Fritts in the year 1883 [16]. This device was based on the photovoltaic effect, which was discovered in 1839 by a 19-year old scientist Alexandre Edmond Becquerel in solutions with metal electrodes. The device created by Fritts had an efficiency of 1% and was based on a selenium layer with a thin layer of gold [16]. The first practical solar cells using silicon were developed at Bell Labs in the year 1954 [17], with subsequent patents in the year 1957 for an 8% efficient solar cell by the same group [18]. Since then various materials have been used for solar cells, such as crystalline as well as amorphous silicon, III-V materials (i.e. GaAs, GaInP etc), II-VI materials (i.e. CdTe, copper indium gallium diselenide (CIGS), perovskites, etc.

In this thesis, we will constrain ourselves to crystalline silicon (c-Si) wafer based solar cells only. Solar cells based on c-Si dominate the PV market, because silicon is the most abundant semiconductor material and the cost of c-Si based solar cells has decreased because of continual technology development. This development has led to highly efficient solar cells that can be produced at high throughput and at low cost. [19–21]. Currently, 95% of the current photovoltaic market is dominated by c-Si cells [21].

A c-Si solar cell consists of the following main components, namely:

1. An absorber layer that absorbs the incident photons and generates electron-hole pairs, which in a c-Si cells is the silicon wafer.

2. Charge separation layers, which provide selectivity to one charge carrier flow.

A junction of p-type and n-type semiconductor is used for this purpose.

3. Doped regions for the collection of charge carriers, after the separation.
4. Metal contacts that transport the charges to the external load.

A schematic cross-section of a bifacial c-Si solar cell is shown in Figure 1.2.

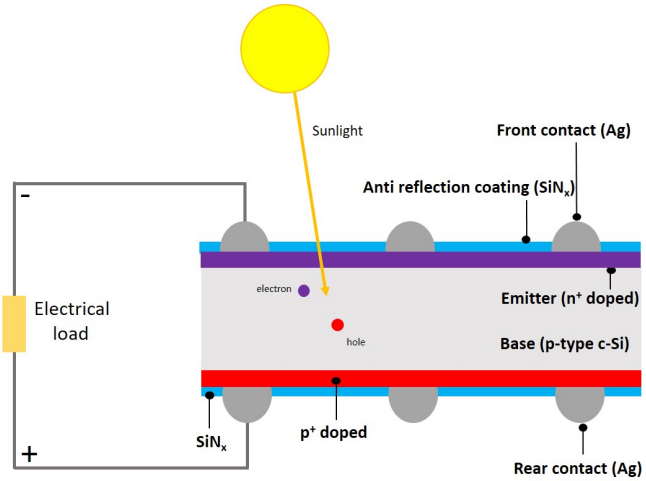

Figure 1.2: Schematic cross-section of a typical bifacial c-Si solar cell.

The incident photons, with energy more than the band gap of the silicon (1.12 eV), are absorbed by the silicon absorber. This generates electron-hole pairs in the absorber as the doped regions collect the charge carriers. By collecting the electrons on one end and the holes at the other end of the absorber layer, a photo-current is generated. The collection of the charge carriers is done by using p-type material and an n-type material, usually made by doping the crystalline silicon with boron and phosphorus. These are called emitter and surface field. As an example, for a p-type c-Si absorber (also called as the base), n^+ diffused region acts as the emitter, and an p^+ doped region on the other side is called surface field (can be back or front). In this case, the emitter collects the electrons, and the surface field region collects the holes. A schematic representation is shown in Figure 1.2. The anti-reflection coating (silicon nitride) reduces the reflection of the sunlight from the cell and hence reduces the optical losses.

1.2.1. Current technology of c-Si solar cells

From the years of the first silicon solar cell, tremendous strides have been made in improving the efficiencies further, with the record efficiency of 26.7% [22] for a crystalline silicon solar cell being achieved. The continued improvement in the highest confirmed efficiencies of solar cells is presented in Figure 1.3, as compiled by National Renewable Energy Laboratory. The crystalline silicon technology has been marked in bold in the chart.

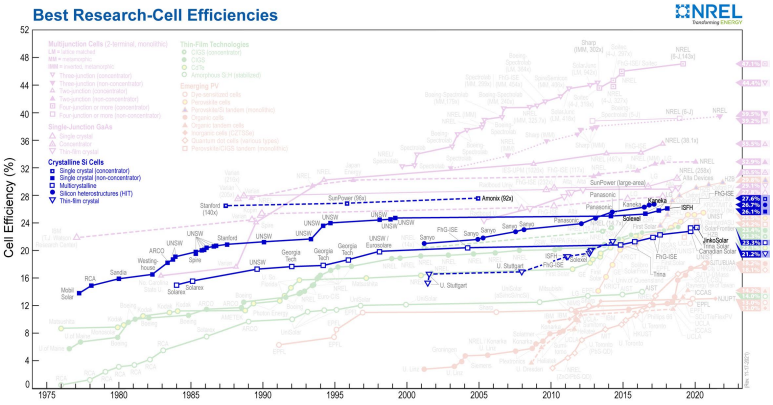

Figure 1.3: Highest confirmed solar cell efficiencies with regards to the years, as compiled by National Renewable Energy Laboratory [23].

In Figure 1.3, most of the devices shown are lab scale small area devices and utilise processes that often are difficult to implement in industrial production. Figure 1.4 shows the development of the conversion efficiencies in this decade for c-Si solar cells in mass production as predicted in the 12th International Technology Road map for Photovoltaics (ITRPV), at the time of writing this thesis. In this figure, the predicted cell efficiencies of different cell architectures are listed and a more detailed discussion of these architectures is presented in Chapter 2. In the last decade, the c-Si solar-cell efficiencies in production have been increasing by almost 0.4-0.6% absolute per year [24, 25]. The ITRPV report predicts that the rate of increase will continue for the next 7-8 years [25].

Figure 1.4: Crystalline silicon solar cell efficiency values in mass production as predicted in 12th ITRPV [25].

Currently, the most used architecture for c-Si solar cells is called passivated

emitter and rear cell (PERC) [25]. Further, details about PERC cell architecture will be presented in Chapter 2. PERC cells have efficiencies in the range of 21-23% at industrial level, as compared to the theoretical limit for c-Si solar cells (Richter limit) of 29.43% (depending on the absorber thickness) [26–28]. Hence, there is scope to increase the efficiency.

1.2.2. PV cell- Recombination losses

The performance of solar cells (PERC) is limited by recombination and resistive losses, specifically at the doped region [29, 30]. Work from Muller et al. provides a detailed loss analysis of industrially produced PERC cells with Technology Computer-Aided Design (TCAD) Sentaurus device modelling. Their simulations results point out that primary recombination and resistive losses are related to the emitter region [30]. Another detailed study utilising experimental results and Sentaurus by Saint-Cast et al. also points out that a major increase in efficiency can be obtained by optimising the emitter region and the metal contact [31]. Reducing these losses is pivoted to lead to increased efficiency. Before discussing the reduction of these losses, first the underlying mechanism is explained.

Surfaces and interfaces in a c-Si solar cell form an abrupt change in the crystal lattice structure. In the energy band diagram such changes are reflected by energy states in the band gap near these interfaces, usually related to defects in the lattice, like dangling bonds or lattice imperfections. These defects facilitate recombination that lead to the loss of free charge carriers. Mathematically, the total recombination rate can be characterised by effective surface recombination velocity, S_{eff}. A good estimation of the surface recombination can be done by approximating the recombination of the interface states of all energies, into a concentration (D_{it}) of states at a single energy level in the middle of the band gap [32].

The effective surface recombination velocity in turn, depends on the steady-state carrier concentration and the electron and hole surface recombination velocity, as shown in the Equation 1.1 [32];

$$S_{\text{eff}} = \frac{1}{\Delta n_d} \frac{n_s p_s - {n_i}^2}{\frac{n_s + n_i}{S_{p0}} + \frac{p_s + n_i}{S_{n0}}} \tag{1.1}$$

Here, n_s and p_s denote the steady-state electron and hole concentration at the surface respectively, Δn_d is the excess minority carrier concentration at the edge of the space charge region, n_i is the intrinsic carrier concentration, and the terms S_{n0} and S_{p0}, are the electron and hole recombination velocity, respectively [32, 33]. S_{n0} and S_{p0} depend on the interface trap density (D_{it}) and the capture cross-section. The lower the effective surface recombination velocity, the fewer carriers are lost due to recombination, leading to higher conversion efficiency.

From Equation 1.1 two pathways of reducing the S_{eff} can be obtained. The first pathway is to reduce, S_{n0} and S_{p0}, which can be done by reducing the defect density at the surface or interface. In practice, this is achieved by using a dielectric coating or a chemical species such as hydrogen. This is termed chemical passivation. The second pathway is to change the ratio of the surface charge carriers (n_s to p_s ratio

or vice-versa). An electric field generated from a fixed charge density (inversion layer) in a dielectric layer can be used to change the ratio. The strategy of using the electric field is called field-effect passivation. The method of introducing a high concentration of free charge carriers at the surface of the substrate is another strategy to have field effect passivation.

Another important contributor to the overall recombination rate is the metal-semiconductor interface (metal contact). For extraction of carriers a metal- semiconductor contact is required. This metal-semiconductor contact is a sink for minority carriers and due to this the output voltage is reduced. A study by Benick et al. shows that about 66% of the total recombination in the emitter region of the solar cell is due to the contact between metal and silicon [34]. Reducing the minority-carrier density by the introduction of a high concentration of majority charge carriers leads to a reduction of the recombination rate at the metal-semiconductor interface [35]. However, a very high majority carrier concentration at the surface or interface leads to increased Auger recombination, which needs to be avoided. One of the solutions to avoid Auger recombination is to reduce the width of the region with high majority carrier concentrations to the area below the contacts (selective emitter). This points out the importance of the metal-silicon contact in increasing the efficiency of the c-Si solar cells: metal contacts are needed to extract generated charge carriers from the solar cell, yet also induce recombination processes that limit the efficiency.

Hence, it becomes imperative to develop strategies to simultaneously have a high degree of passivation in the metallised and unmetallised area in order to reduce the recombination losses. The passivation quality is often represented by the implied open-circuit voltage (iV_{oc}) and recombination current density ($J_{0\mathrm{pass}}$) (surface property), as will be explained in more detail in Chapter 4. In this thesis, we will use these two quantities to compare the passivation quality between different samples. An additional requirement is to achieve low contact resistance between the metal and the semiconductor. A highly doped region (high carrier concentration region) leads to an ohmic contact, which is desirable in electrical conduction.

1.3. Motivation

The most widely accepted way of mitigating the losses mentioned previously is to utilise novel so-called passivating contact schemes. Two passivating contact schemes can be used for this purpose: low- and high-temperature schemes. The demarcation between these two processes comes from the materials used for passivation and the thermal budget limitation for achieving low effective surface recombination velocity and low contact resistance. Both processes have their benefits and shortcomings [21, 35–37]. In this thesis we will focus on the high-temperature scheme, which utilises a highly doped polysilicon/SiO_x layer stack. The highly doped polysilicon/SiO_x layer stack not only provides a high level of passivisation but also good electrical transport. A schematic representation of a solar cell based on n^+ polysilicon/SiO_x passivating contact is shown in Figure 1.5. This high temperature scheme has the advantage that is more acceptable as compared to the low-temperature scheme for large-scale implementation, because the existing solar-cell

manufacturing lines can be upgraded to produce polysilicon/SiO_x passivated solar cells. This has been recently demonstrated by Trina Solar and JinkoSolar [38–40]. Various other large solar-cell manufacturers are also working on polysilicon/SiO_x passivated solar cells [40–43].

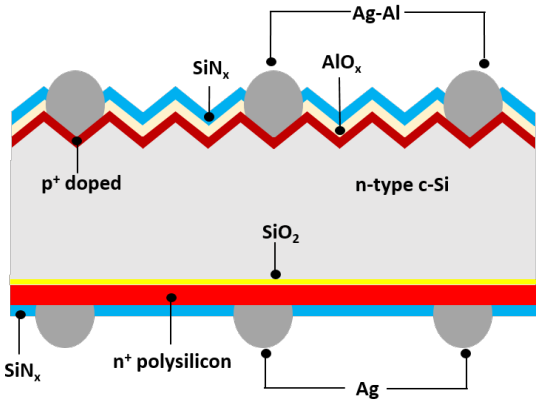

Figure 1.5: Schematic cross section of the bifacial c-Si solar cell that is the topic of study in this thesis. Note the n^+ polysilicon/SiO_x layer stack at the rear side of this cell.

The main aim of the work in this thesis is to understand and mitigate the losses at the silver-n^+ polysilicon/SiO_x contact by reducing the metal-silicon contact recombination current density ($J_{0\mathrm{met}}$) and the contact resistivity (ρ_c). The metallisation in this work is performed by screen printing of fire-through silver paste, which involves a high-temperature sintering step. Screen printing is chosen because it is the most widely used method of metallisation for industrial solar cells [44]. Among the many unanswered questions, this work will address the following questions in detail:

1. How does the silver paste interact with the n^+ polysilicon/SiO_x layer stack?
2. What are the critical factors that influence the contact properties for the silver-n^+ polysilicon/SiO_x contact?
3. How can the contact properties be optimised in order to achieve high efficiency for the rear side n^+ polysilicon/SiO_x solar cell?

To the best of our knowledge, no complete and precise answer exists for the above questions. We will try to answer them with systematic studies in this work.

1.4. Outline

Operation of a crystalline silicon solar cell is described in detail in Chapter 2. This chapter also discusses the basics of the four most commonly used architectures of c-Si solar cells, namely, aluminium back surface field (Al-BSF), Passivated Emitter

and Rear Cell (PERC), Polysilicon/SiO_x passivated contact cells and Interdigitated Back Contact (IBC) cells. The sample fabrication techniques used in the thesis are explained in Chapter 3. It is divided in two parts: in the first part the deposition techniques are explained and in the second part the metallisation process is described, in particular screen printing and the fast-firing process. The characterisation techniques are explained in Chapter 4, with a special focus on microscopic and optical techniques used in the thesis. This chapter also explains the method of extraction of metal-silicon recombination current density $J_{0\mathrm{met}}$ from calibrated Photoluminescence pictures.

Chapter 5, contains the results of experiments conducted to find the most optimum silver paste for n^+polysilicon/ SiO_x passivating layer stack. Contact properties ($J_{0\mathrm{met}}$ and contact resistivity) for different silver pastes are presented. The evolution of contact properties is also studied with respect to the peak fast-firing temperature. The paste with the lowest contact resistivity and metal-polysilicon recombination current density is found and used for the later experiments in this thesis and development of a solar cell with n^+ polysilicon/ SiO_x passivating layer stack at the rear. In this chapter, an extensive study on the measurement of contact resistivity of n^+polysilicon/ SiO_x passivating layer stack is also presented. In Chapter 6, comparison between the phosphorus diffused silicon layer and the n^+ polysilicon/SiO_x passivated contact in terms of their passivation quality and contact properties is presented. Cross-sectional SEM images are used to explain the differences between the two contact stacks. Chapter 7 contains the study on the metallisation of passivated contacts with different thicknesses of the n^+ polysilicon layer. This chapter answers the vital question of how thin the polysilicon layer can be to have good passivating and contact properties simultaneously. The experimental work aimed at understanding the effect of different substrate surface morphology/finish on the passivation and contact properties for the n^+ polysilicon/SiO_x passivating layer stack is presented in Chapter 8. A planar substrate surface morphology is found out to be the most optimum for implementation of n^+ polysilicon/SiO_x passivating layer stack. The process chain to develop the final device that utilises a rear side n^+ polysilicon/SiO_x passivating layer stack is presented in Chapter 9. We demonstrate an champion efficiency of 22.26% for this device and explain how it can be further increased. In Chapter 10 the main conclusions of this work are summarized and a future outlook is presented.

1.5. Contributions to photovoltaics

This doctoral thesis presents a number of experimental results and insights into the silver- n^+ polysilicon/SiO_x passivating contact. The following significant contributions to the field have been realized:

- The influence of different silver pastes and the thermal budget on the contact properties (metal-semiconductor recombination current density and contact resistivity) has been studied. When reducing the thermal budget we found that the metal-polysilicon recombination current density decreases, whereas the contact resistivity remains almost unchanged for a wide range of tem-

peratures. Based on SEM images we conclude that the above findings are related to the increase in damage to the polysilicon layer following metallisation [45, 46].

- This work shows excellent values of both metal-polysilicon recombination current density ($J_{0\mathrm{met}}$) and contact resistivity (ρ_c) for a Ag/n^+ polysilicon/SiO_x passivating contact. The values ($J_{0\mathrm{met}} \leq 50$ fA.cm^{-2} and $\rho_c \leq 2$ mΩ.cm^2) presented are within the lowest reported in the literature [47]. This justifies and supports the use of n^+polysilicon/SiO_x based passivated contacts as a means of reducing solar cell losses. The polysilicon layer favours more the crystallisation of silver as compared to phosphorus diffused layers, as concluded from the SEM images presented in Chapter 6 [48].

- A comprehensive study on the dependence of the passivation quality (implied open-circuit voltage and recombination current density) and contact properties (metal-polysilicon recombination current density and contact resistivity) on the polysilicon layer thickness has been carried out. The reduction in polysilicon-layer thickness leads to an increase of the metal-polysilicon recombination current density and contact resistivity values [47].

- Compared to any textured surface, a planar substrate surface is most favourable to be used with n^+ polysilicon/ SiO_x passivating layer with respect to the contact properties [49].

- A pathway to upgrading the nPERT cells to cells with rear side n^+ polysilicon/ SiO_x passivating layer is presented. A 244.32 cm^2 sized champion device with an efficiency of 22.26% (V_{oc} of 694 mV, J_{sc} of 40.30 mA.cm^{-2} and FF of 79.64%) has been presented. Griddler 2.5PRO simulations are also utilised in order to improve the solar cell efficiencies as well as perform loss analysis [50].

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2

Crystalline silicon solar-cell architectures

If you believe in science, like I do,
you believe that there are certain laws that are always obeyed.

Stephen Hawking

This chapter discusses the relevant background related to this work. The chapter is divided into three sections. The first section explains the operation of solar cells. The second section is about metal-semiconductor contacts. The third section describes the different types of crystalline silicon solar cell architectures and recent developments.

2.1. Introduction

This chapter contains a description of solar cells based on crystalline silicon (c-Si) and an overview of the most important architectures. In the first section, the underlying operation of the solar cell is presented. The second section is about the metal-semiconductor contact, which is an essential part of the thesis. The third section is about the prevalent crystalline silicon solar cell architectures. The four architectures defined are aluminium Back Surface Field (Al-BSF), Passivated Emitter Rear Cell (PERC), polysilicon/SiO_x passivated contact and Interdigitated Back Contact (IBC) cells. The polysilicon/SiO_x passivated contact cells form the backbone of this thesis and it is important to understand how they differ from the other cell architectures as well as what are their advantages.

2.2. Crystalline silicon solar cell basics

The operation of solar cells is based on the photovoltaic (PV) effect that leads to a potential difference at the junction of two different materials upon light illumination. The important aspect is that photons interact with electrons in the valence band of the semiconductor materials. If the photon energy is sufficiently high, the electron can be excited to the conduction band, thus creating electron-hole pairs. The generated charge carriers are free and are available for conduction.

The mathematical relation describing the photo-generated current (I_{ph}) to the voltage across the cell is written as:

$$I(V) = I_{ph} - I_0(e^{\frac{qV}{nkT}} - 1) \tag{2.1}$$

The above equation considers the single diode equivalent model for the solar cell and is generated by the superposition principle. Notice that this equation does not take into account any resistive components. The voltage across the cell is V, and I_0 is the saturation current, sometimes called the reverse-bias current or the diode leakage current. For an ideal diode, the saturation current is determined by the transport properties of minority charge carriers but in more realistic descriptions, the saturation current includes recombination in the device. The elementary charge is represented with q, k the Boltzmann constant, T is the temperature, and n is the ideality factor (1 for an ideal diode). An equivalent electrical circuit diagram of a solar cell with resistive components is shown in Figure 2.1.

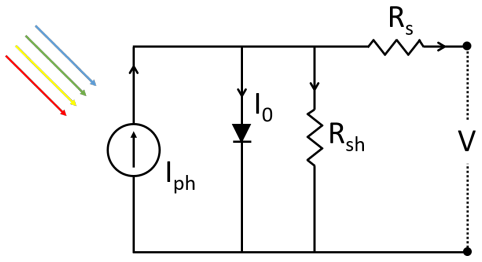

Figure 2.1: Equivalent electrical model with an ideal diode for a standard solar cell.

Under the condition of short-circuit, $V = 0$, $I(V = 0) = I_{sc}$, and wherein I_{sc} is the short-circuit current. In photovoltaics, we can use current density (J) instead of current. At open-circuit condition, the external current density is zero (i.e J=0) and the voltage equals the open-circuit voltage V_{oc}. Thus for an ideal diode the V_{oc} is given by [1],

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{2.2}$$

When taking into account the effect of Shockley-Read-Hall recombination, the Equation 2.1 is modified :

$$J(V) = J_{ph} - J_{01}\left(e^{\frac{qv}{n_1 kT}} - 1\right) - J_{02}\left(e^{\frac{qv}{n_2 kT}} - 1\right) \tag{2.3}$$

The parameters n_1 (is equal to 1) and J_{01} are the ideality factor and dark saturation current density of an ideal diode, respectively. The parameters n_2 and J_{02} are for the non-ideal diode, which are related to the recombination in the space charge region. The n_2 parameter can be larger than 2 in real devices [2].

In Equation 2.3, only the effect of recombination is taken into account. Adding the effect of series and parallel resistances modifies the mathematical equation as follows:

$$J(V) = J_{ph} - J_{01}\left(e^{\frac{qV - J(V)R_S}{n_1 kT}} - 1\right) - J_{02}\left(e^{\frac{qV - J(V)R_S}{n_2 kT}} - 1\right) - \frac{V - J(V)R_s}{R_{sh}} \tag{2.4}$$

The component, R_s, represents the series resistance and R_{sh} is the shunt resistance. R_s contains the contribution from the metallisation, the fingers and the busbars, lateral flow of current through the absorber and the emitter. The shunt resistance is associated with the losses in the p-n junction and the losses due to material defects. For instance, shunts may occur when metal impurities are present in the junction or at the edge or grain boundaries in the material. Equation 2.4 shows that the R_{sh} value determines how much current will flow through the cell junction and hence will reduce the voltage output. Therefore, the value of R_{sh} should be as high as possible. The equivalent model considering the recombination and the resistive components is presented in Figure 2.2.

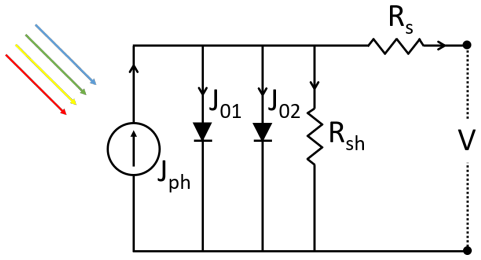

Figure 2.2: Equivalent electrical model with recombination and resistive components for a standard solar cell.

An example of an IV characteristic of a polysilicon/SiO_x passivated contact solar cell (developed in this thesis), with an area of 244.32 cm^2, is shown in Figure 2.3. This IV characteristic has been measured under Standard Test Conditions (STC). At STC the AM1.5 spectrum is used (in which AM is the air mass that refers to the attenuation of light by 1.5 times the atmosphere before reaching the Earth's surface), having an irradiance of 1000 W/m^2 and the cell is measured at a temperature of 25°C.

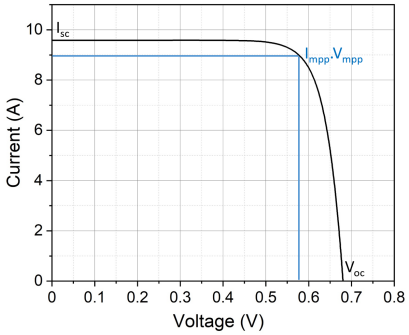

Figure 2.3: IV curve for a polysilicon/SiO_x passivated contact solar cell developed in this thesis.

The efficiency (η) of a solar cell is determined from the IV plot as shown in Figure 2.3, using the mathematical expression presented in Equation. 2.5.

$$\eta = \frac{V_{mpp} I_{mpp}}{P_{in}} = \frac{J_{sc} V_{oc} FF}{P_{in}} \tag{2.5}$$

The term "mpp" stands for maximum power point, i.e the operating point of the cell where it generates the maximum power. The incident power is denoted by P_{in} in the above equation. FF is the fill factor that contains the contributions from the series and shunt resistance.

For a c-Si solar cell with absorber thickness of 110 µm Richter et al. [3] determined that the theoretical maximum conversion efficiency is 29.43%, with the following external parameters: J_{sc} = 43.3 mA/cm^2, V_{oc} = 761.3 mV, and FF = 89.26%. In their calculation, they took into account radiative and Auger recombination mechanisms, as well as bandgap narrowing effects.

2.3. Metal-semiconductor contacts

In an ideal case, the metal-semiconductor contact of a solar cell would be an ohmic contact (non-rectifying) with a linear current-voltage dependence and negligible resistance. However, due to the energy barrier between the metal and semiconductor, the contact between the two is often a rectifying contact. This was first shown by Schottky, hence the metal-semiconductor contacts are called as Schottky contact [4]. According to Schottky, when the metal and semiconductor are joined

the Fermi energy levels of the metal and the semiconductor align. This leads to a formation of a depletion or an accumulation contact depending on the work function of the metal and the semiconductor [5]. Accordingly, the potential barrier between a metal contact and n-type silicon (ϕ_{Bn}) is mathematically described as:

$$\phi_{Bn} = \phi_m - \chi_{\mathrm{Si}} \tag{2.6}$$

where, ϕ_m is the metal work function, χ_{Si} is the silicon electron affinity.

The theory provided by Schottky was not able to completely explain the experimental data obtained with different metal contacts. The theory was expanded by Bardeen [6], and Cowley and Sze [7] to incorporate two important aspects of a metal-semiconductor contact, i.e. image-force lowering and Fermi-level pinning. Due to the presence of an electric field in the semiconductor at the interface to the metal contact, the barrier height is lowered, and thus Equation 2.6 is not entirely accurate. This effect is called as image force lowering. Bardeen [6], and Cowley and Sze [7] in their work explain also the importance of the surface states at the interface, which according to them is more significant than the metal work function on determining the barrier height. This is called Fermi-level pinning.

The current transport across the metal-semiconductor contact is explained with three transport models, namely, Thermionic Emission (TE) (dominant for a semiconductor with a donor doping of less than 1×10^{17} cm^{-3}), Field Emission (FE) (dominant for a semiconductor with a donor doping of more than 1×10^{20} cm^{-3}) and a combination of TE and FE, called Thermionic Field Emission (TFE) (dominant for a semiconductor with a donor doping of between 1×10^{17} and 1×10^{20} cm^{-3}) [8]. Thermionic Emission is the transport of electron by thermal excitation, Field Emission is due to the tunneling across the thin barrier [1, 9, 10]. In case of n$^+$ polysilicon-Silver contact, the dominant current transport mechanism is FE, due to the doping of above 1×10^{20} cm^{-3} in the polysilicon layer. This ensures good current transport across the contact, and a low contact resistivity value [11–13].

2.4. Crystalline silicon solar cell architectures

In this section, different solar-cell architectures will be discussed. First, the Aluminium Back Surface Field (Al-BSF) is explained and then the Passivated Emitter Rear Cell (PERC) and its derivative, the Passivated Emitter and Rear Totally diffused cell (PERT) will be presented. After PERC, the next evolutionary cell architectures, Polysilicon/SiO$_x$ passivated contact cells and Interdigitated Back Contacted (IBC) solar cells will be explained.

2.4.1. Aluminium Back Surface Field (Al-BSF) cell

Al-BSF cells were the first truly industrialised solar cells. They have been mass-produced and have been the dominant cell architecture untill the arrival of PERC and its derivative PERT in the second half of the first decade of this century [14]. A schematic cross-section of the Al-BSF cell is shown in Figure 2.4. This simple architecture consists of a p-type silicon substrate (monocrystalline or multicrystalline) with an n$^+$ emitter on the front and aluminium-based hole contact on the rear.

The aluminium layer at the rear leads to the formation of a p^+/p junction with the crystalline silicon, as aluminium acts as a p-type dopant. This is called the back surface field. The presence of this field presents a barrier for the electrons to travel to the back contact and hence reduces recombination. The front side is capped with an anti-reflection coating of silicon nitride. The silicon nitride layer also acts as a passivation layer reducing the surface recombination. Further, it also serves as a source of hydrogen, which helps in further improving the passivation of the silicon surface when exposed to a high temperature step. The metallisation for this kind of cell is performed using screen printing and subsequent fast-firing process [15, 16]. This is because screen printing and fast firing ensure high throughput and cost-effectiveness. Efficiencies in range of 14-20% can be obtained with this architecture [17].

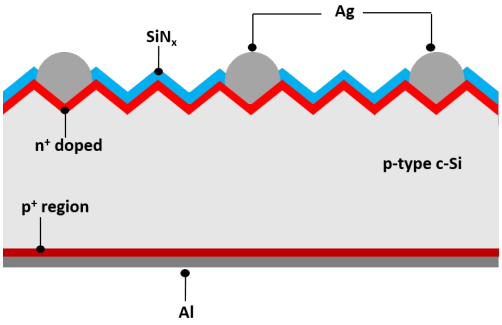

Figure 2.4: Schematic representation of an Al-BSF cell.

Despite the relatively easy large-scale manufacturing of Al-BSF cells, they are inherently limited in their efficiency due to the fairly high recombination rate at the rear metal contact resulting from the full-area aluminium and the IR absorption at the aluminium contact.

2.4.2. Passivated Emitter and Rear Cell (PERC)

The first research work on PERC solar cells was published in 1989 by the group from the University of New South Wales, Australia. They presented an efficiency of 22.8% for the p-type float zone PERC cell [18], which was well beyond the highest efficiency of solar cells at that time. The salient feature of the cell involved the use of inverted pyramids on the front side for light management in order to increase the short-circuit current density in combination with the selective emitter. The front metallisation involved titanium and palladium evaporated contacts coupled with plated silver in order to reduce damage to the emitter due to metallisation. The rear side was passivated with oxide with local contact openings for contacting with aluminium, thereby reducing the area of metal-semiconductor contact and thus the recombination rate at the rear of the solar cell. The original schematic of the cell is shown in Figure 2.5.

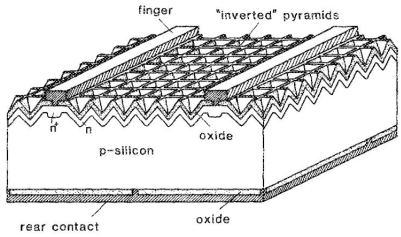

Figure 2.5: Schematic representation of an early PERC cell [18].

After almost 30 years, PERC technology has matured to a level where it is the dominant cell architecture that is available. This is partly due to the advancements in the overall processes involved in PERC cell production. Improvement in screen printing metallisation, availability of unique screen printed paste enabling lower metal recombination and lower contact resistivity, and improvement in the passivation layers, such as the use of AlO_x layers are a few of the advancements [19]. In recent times, PERC cells and their derivatives such as PERT/PERL occupy the majority share of the solar cell market [14, 20].

The PERC cells utilise p-type (Boron doped) c-Si substrates and are sensitive to Light Induced Degradation (LID), and Light and elevated Temperature Induced Degradation (LeTID), which is the gradual decay in efficiency due to exposure to light and heat [21–24]. The degradation has been countered with the use of n-type wafers, such as in the cell concept called BIfacial SOlar cell on N-type wafer (BiSoN), developed by the group from ISC-Konstanz [25–28]. This cell is an n-type Passivated Emitter and Rear Totally Diffused cell (nPERT) front junction cell. A schematic representation of this cell is shown in Figure 2.6.

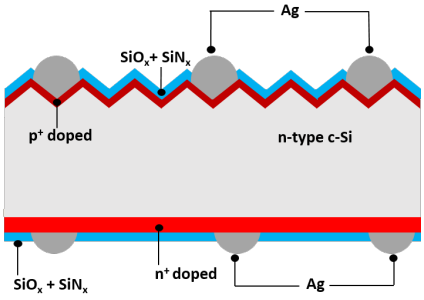

Figure 2.6: Schematic representation of the BiSoN cell.

The efficiency of the PERC cell concept is constrained by the recombination at the metal-silicon interface and the emitter passivation quality [29–33]. Thus, the next step in the evolution of solar cell architectures is about dealing with these two issues.

2.4.3. Polysilicon/SiO_x passivated contact cells

Initially, research on polysilicon/SiO_x layer stacks was motivated due to their potential to be used in solid-state electronics, especially Bipolar Junction Transistors (BJT) and Metal-Oxide-Semiconductor (MOS) technology in the 1970's [34–36]. The utilisation of polysilicon/SiO_x in BJT and MOS devices motivated researchers to implement this layer stack in c-Si cells in 1980's, with an architecture called Semi-Insultaing POly-crystalline Silicon (SIPOS) [37–39]. This layer stack was not further developed for implementation in c-Si solar cells. A renewed interest in this layer stack came about in 2010 with a publication showing a 24.2% efficient IBC c-Si cell by SunPower Corporation [40]. Shortly afterwards, researchers from Fraunhofer ISE and ISFH, also demonstrated cell architectures utilising polysilicon/SiO_x layer stacks [41, 42].

A polysilicon/SiO_x passivated contact consists of: (i) a highly doped polysilicon layer, and (ii) a thin interfacial oxide, which supports charge transport across it. The highly doped polysilicon layer (active doping concentration in the order of 1 to 3×10^{20} cm^{-3}), reduces metal-polysilicon recombination current density and enhances field-effect passivation. The interfacial oxide, which is 1.3 to 2.6 nm thick, provides a high level of surface passivation for the silicon substrate surface and suppresses the diffusion of dopants from the polysilicon layer into the c-Si absorber. These features of the polysilicon/SiO_x stack improve the passivation quality as characterized by a suppressed recombination rate, enabling increased iV_{oc} values as compared to the PERC concept. Recombination current density values of the order of 1 $fA.cm^{-2}$ and iV_{oc} values in the range of 745 mV have been demonstrated for a n^+ polysilicon/SiO_x contact [42–45]. The properties of the polysilicon/SiO_x contact have been characterised by the contact resistivity and metal-polysilicon recombination current density. Extensive work has been performed on this in recent times [45–49]. The work in this thesis presents some of the best values of contact resistivity and metal-polysilicon recombination current density obtained for the n^+ polysilicon/SiO_x layer stacks.

In the PV community, two charge-carrier transport mechanisms from the absorber to the polysilicon layer have been discussed: (i) direct tunneling through the interfacial oxide [41] and (ii) charge transport through the pinholes created during annealing of the polysilicon layer [42]. For a long time there has been disagreement on which mechanism is dominant. This is the reason for the different acronyms for polysilicon/SiO_x based solar cells such as Tunnel Oxide Passivated Contact (TOPCon) cells from Fraunhofer ISE and Poly-Si on Oxide (POLO) cells from ISFH. The concept of POLO utilises an oxide that is thicker than 2 nm and hence the transport is dominated by pinholes. However, many researchers think that the transport across the interfacial oxide is both from tunneling and pinholes [42, 50, 51]. Depending on the thickness of the oxide, annealing temperature, and oxidation method, one of the transport mechanisms can dominate, although the other mechanism may still contribute, as there is not yet conclusive evidence that only one mechanism is present [50]. For this reason, we will call the silicon oxide layer as interfacial oxide, not tunneling oxide.

Some of the examples of solar-cell architectures with polysilicon/SiO_x layer

stacks are Passivated Emitter Rear Polysilicon (PERPoly) cells from ECN, POLO cells from ISFH and TOPCon cells from Fraunhofer ISE and the monoPoly™ cells from SERIS [41, 42, 44–46, 52–57]. The highest efficiency achieved with polysilicon/SiO_x layer stack-based cells is 26.1% for all back contacted cell (IBC cell, POLO), 25.7% and 26% for front and rear contacted cell (TOPCon: on n and p-type wafer substrate, respectively). These cells are small area lab devices (1 to 4 cm^2). A schematic representation of a cell with front and rear side polysilicon/SiO_x contact is shown in Figure 2.7, based on the work from Peibst et al. [42]. A sketch of the corresponding band diagram is shown in Figure 2.8. This band diagram shows that the heavily doped polysilicon regions lead to a band offset, which suppresses the minority charge carrier transport and leads to field-effect passivation and charge selectivity.

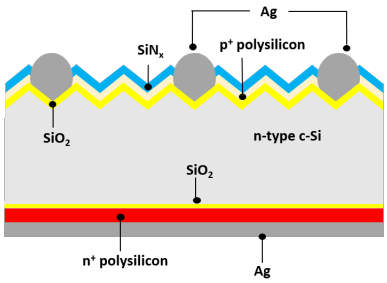

Figure 2.7: Schematic representation of a front and rear polysilicon/SiO_x cell based on the work from Peibst et al. [42].

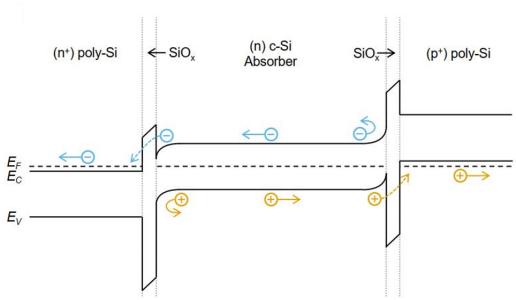

Figure 2.8: Band diagram sketch for the front and rear polysilicon/SiO_x cell [42, 58].

In industry, the implementation of polysilicon/SiO_x layer-based cells is also progressing rapidly. Large PV manufacturers, like GCL, Trina Solar, Jinko Solar, Jolywood, and SunPower, have reported research on polysilicon-based contacts [59–61]. Efficiencies beyond 24.5% have already been reported on large-area polysilicon/SiO_x based cells, at the time of writing this thesis [62].

The thickness of the polysilicon and the oxide layers are critical aspects of the polysilicon/SiO_x passivated contacts. These define the performance of the

polysilicon/SiO_x cell: a too thick polysilicon layer leads to increased parasitic absorption (free carrier absorption), while a too thin layer is not conducive to screen printed fire through metallisation [63, 64]. A too thin oxide layer would not be able to block the in-diffusion of the dopants in the crystalline silicon, while a too thick layer would be insulating to the charge flow. The advantage of the polysilicon/SiO_x layer stack is its stability at high temperatures (above 700°C), which makes its implementation in existing solar cell lines relatively easy and less capital intensive as compared to the alternative route of heterojunction cells.

2.4.4. Interdigitated back contact (IBC) cells

Interdigitated Back Contact (IBC) solar cells were first developed at Stanford University as a cell for concentrator purposes in the latter half of the 1980s [65]. A schematic of an IBC cell is shown in Figure 2.9 [66].

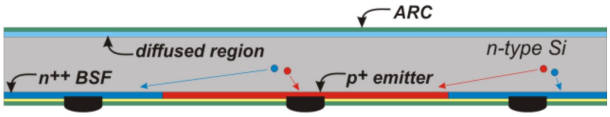

Figure 2.9: A schematic representation of an IBC solar cell, taken from [66].

The essential feature about this architecture is that the front side of the cell is devoid of any metallisation. Hence there is no shading loss. Both polarities are on the rear side of the cell. This makes cell processing more complicated than the earlier-mentioned cell architectures. Recent work from ISC Konstanz has provided a processing sequence, which has been introduced into mass production, with cells reaching efficiencies of 23% and above in mass production [67, 68].

The important features of IBC cells are as follows:

- There is no need for optimisation of metal prints in view of optical losses. Thus the metal contacts need to be optimised only for the electrical properties.
- The front surface can be optimised to have low recombination, without any constraint on electrical flow.
- The substrate needs to have high bulk lifetime, as carrier collection is far from carrier generation.
- The front surface recombination needs to be as low as possible, so that the carriers do not recombine at the surface.
- The printing of the metal contacts needs careful alignment so as to avoid shunting between the two polarities.

Different IBC solar-cell design features, such as front surface field and front floating emitter, are available, with each design having its own advantage [69]. The current world record solar cell with an efficiency of 26.7% utilises an IBC-Silicon Hetero-Junction architecture [70, 71].

2.5. Conclusion

This chapter discusses the metal-semiconductor contact and the different crystalline silicon solar-cell architectures. In particular, the polysilicon/SiO_x cell architecture is discussed which forms the basis of the solar cells in this thesis. The advantages and disadvantages of each architect are explained. In the remainder of this thesis, we will specifically look into the rear side n^+ polysilicon/SiO_x based solar cell.

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3

Sample Processing and Metallisation

Regard everything as an experiment.

Corita Kent

This chapter is dedicated to techniques for sample processing used in this work. The last section in this chapter explains metallisation processes, with a particular focus on screen printing and fast firing.

3.1. Introduction

This chapter is divided into three main sections: the first section provides the sample preparation process sequence. The second section explains the three main techniques used to grow/deposit the layers on the silicon substrate to have the required layer stack for the polysilicon based passivated contacts. The three techniques which are explained are: Nitric Acid Oxidation of Silicon (NAOS) for growing an interfacial oxide, Low Pressure Chemical Vapor Deposition (LPCVD) for n^+ in-situ doped silicon (a-Si) layer, and Plasma Enhanced Chemical Vapor Deposition (PECVD) for silicon nitride layers.

The third section in this chapter explains the processes done after the deposition of the required layer stack to develop the final devices. This includes an annealing process to achieve the necessary crystallisation and active dopant profiles for the LPCVD deposited layers. The last part in this chapter is about screen printing metallisation and fast firing process for the final metal polysilicon contact formation.

3.2. Sample preparation process sequence

Two kinds of samples are utilised for the experiments throughout the work, the symmetrical samples, which have the same layer stacks on both sides of the substrates and the other are the solar cells. The symmetrical samples are used for the characterisation as well as the study of the metal polysilicon contact. Eventually, using the knowledge gained from the study on the symmetrical structures, polysilicon based passivated cells are developed and optimised. Chapter 10 is dedicated to the cell development activities done throughout the work. So, the main details about the cell architecture are presented in that chapter.

In the current chapter, the details about the preparation for the symmetric sample are explained. We used n and p-type solar-grade Czochralski wafers (Cz) as the substrates for the experiments. The step-by-step process chain involved in the symmetric sample preparation is as follows:

1. Removal of the saw damage. This is done by immersion in 22% concentrated sodium hydroxide (NaOH) solution. A specific thickness of the wafer is etched, unless specified this is 10 µm per side. We call these type of wafers as saw damage etched substrates or planar surface finish substrates.

2. Cleaning of the wafers by dips in HCl/HF (2%/2%) solution and Piranha solution (H_2SO_4 and H_2O_2), to remove metal and organic impurities.

3. After the cleaning of the wafers, an interfacial oxide is grown on the wafers. Unless specified differently, an approximately 1.4-nm thick wet chemical oxide is used.

4. After the growth of interfacial oxide, LPCVD based n^+ insitu doped a-Si layers are deposited.

5. After the LPCVD step, annealing is performed at 825°C for 30 minutes. In case of different annealing parameters, they will be specified.

6. A PECVD based silicon nitride layer is deposited after the annealing step.
7. Finally, the steps of metallisation process, involving screen printing and fast-firing are performed.

A schematic illustration of the symmetric sample before metallisation is presented in Figure 3.1.

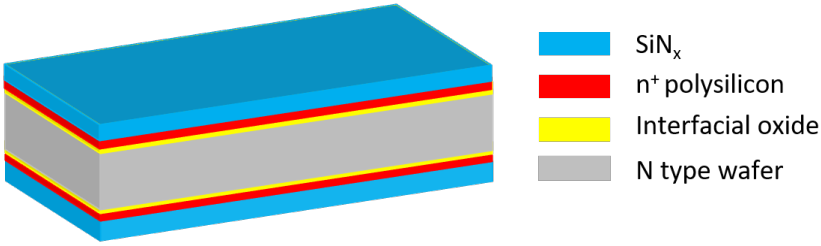

Figure 3.1: Schematic cross-section of a n^+ polysilicon/SiO_x symmetric sample.

3.3. Layer Deposition/Growth Techniques

3.3.1. Nitric Acid Oxidation of Silicon (NAOS)

Interfacial oxide is an essential component of polysilicon based passivated contact. There are various techniques by which the interfacial oxide can be grown, such as wet chemical processes, thermal oxidation, and UV/O_3 photo-oxidation [1–3]. The growth of oxide on silicon surfaces has been well established in microelectronics; an important aspect is that the thin oxide (less than 2-nm) is a suboxide layer. Hence it is SiO_x, not stoichiometric silicon oxide (SiO_2) [4]. The Nitric Acid Oxidation of Silicon (NAOS) process involves the generation of oxygen which oxidises the silicon substrate surface [5]. The chemical reaction involving HNO_3 is shown in Equation. 3.1 below:

$$2HNO_3 \rightarrow 2NO + H_2O + 3O \tag{3.1}$$

The maximum oxide thickness that can be obtained with 61% and 68% concentrated HNO_3 is 1.2-nm and 1.4-nm, respectively, within 10 minutes at the temperature of 112.0 and 120.7°C [3]. In our process sequence, we use 68% concentrated HNO_3 at room temperature (25°C) and immerse the samples for 30 minutes. This leads to a growth of approximately 1.4-nm thick interfacial oxide.

In passivated contact structures with polysilicon, this interfacial oxide is generally between 1 to 2.5-nm thick [6, 7]. It acts as surface passivation for the crystalline silicon wafer. This thin oxide also acts as a diffusion barrier, hence keeping the majority of the dopants in the polysilicon layer, avoiding the deep dopant tails. This results in excellent passivation quality for the polysilicon/ SiO_x passivated contacts.The interfacial oxide allows for current transport via tunneling and through pin holes or locally reduced oxide thickness [8]. In this work, the wet chemical process NAOS is used to grow an approximately 1.4-nm thick oxide. Unless otherwise stated, this will be the standard oxide used throughout the work.

3.3.2. Low Pressure Chemical Vapor Deposition

Low Pressure Chemical Vapor Deposition (LPCVD) is one of the Chemical Vapor Deposition (CVD) methods of deposition. In CVD methods, the vapor phase constituents are introduced in a reaction chamber, where they are adsorbed on a temperature-controlled substrate. They might be diluted with an inert carrier gas depending on the requirements of the deposition. Two types of reactions can take place in a CVD process homogeneous reactions (reactions that occur in gas phase) and heterogeneous reactions (reaction that occur of the surface of substrate) [9]. One of the advantages of these processes is that by varying the gas flows and the substrate temperature the growth rate and the material properties of the layer can be manipulated [10, 11].

In the LPCVD process, a low pressure environment (0.25-2 Torr) is used in conjugation with high temperature (400-900°C) to deposit the layers. The advantage of these settings is the excellent uniformity and high throughput in comparison to other CVD methods. The only disadvantage of this technique is that it is not a single-sided deposition process and low deposition rates. A schematic of an LPCVD reactor is shown in Figure 3.2. We use a Centrotherm tool for our depositions.

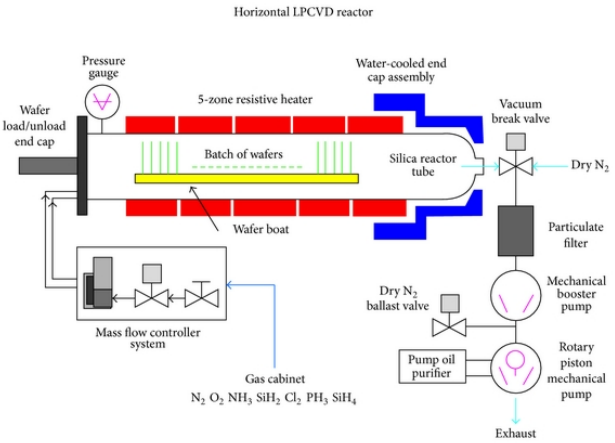

Figure 3.2: A schematic of an industrial vertical LPCVD chamber [12].

In this work, insitu n^+ doped polysilicon layers are used, as the processing of these layers have advantage of having a simpler process chain. A gas mixture of silane (SiH_4) and phosphine (PH_3) is used to deposit the layer. The depositions are carried out at a temperature of 580 °C and a pressure of 250 mTorr, unless specified otherwise.

The LPCVD boat we used has 420 slots. We have a gap of one slot between two wafers and hence we can have 210 wafers throughput per deposition in the system. The boat is divided into three zones, namely Load Zone, Center Zone and Gas Zone.

3.3.3. Annealing

To develop the polysilicon/SiO_x passivated contacts, we need to anneal the LPCVD deposited layers for solid-phase crystallisation. As a result of this annealing step a fraction of the dopants in the polysilicon layer diffuse into the silicon wafer. As an example, Figure 3.3 shows the doping profile for an approximately 150-nm thick n^+ polysilicon layer annealed at 825 °C for 30 minutes. This profile was measured using Electrochemical Capacitance Voltage (ECV) profiling, which will be discussed in detail in Chapter 4. The dopants that diffuse into the crystalline silicon wafer lead to a tail in the dopant concentration as a function of position. In the Figure 3.3, the thickness of the polysilicon layer is marked with a light blue area to make the distinction easy between the polysilicon layer and the crystalline silicon wafer.

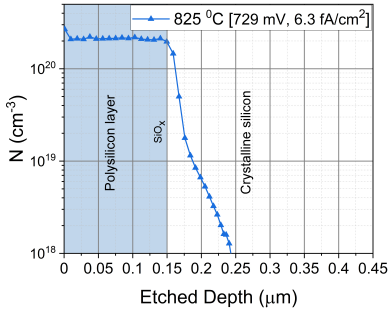

Figure 3.3: Doping profiles for n^+ polysilicon/SiO_x passivated samples. The nominal thickness of the polysilicon layer is 150-nm.

The annealing tube in the previously mentioned Centrotherm tool is used for annealing the samples. The annealing process is carried out in an inert environment with N_2 gas for 30 minutes (plateau time) throughout the work, unless specified.

3.3.4. Plasma Enhanced Chemical Vapor Deposition

PECVD is a type of low-temperature chemical vapour deposition in which gas-phase chemical reactions lead to deposition of material on a substrate. As the energy is supplied by plasma, the substrate temperature required for depositions is low compared to LPCVD. The complexity of the plasma process and the subsequent reactions often led to non-stoichiometric layers. This causes the incorporation of hydrogen or nitrogen in the deposited layers. The incorporation of hydrogen is especially beneficial in applications where a source of hydrogen is needed to improve on the surface passivation [13]. Another advantage of PECVD is that it is a single-side deposition technique, with a good layer thickness homogeneity across the carrier and the substrates.

In this process different gas mixtures can be used. The mixture is ignited to create a plasma through the application of an electric field at radio frequency (13.56 MHz) or very high frequency (40 MHz). These frequencies are internationally agreed upon for use in scientific and industrial applications for material deposi-

tions. Although different frequency can also be used. After the plasma is ignited the electrons are accelerated. This leads to the ionisation of precursor gases through collisions leading to formation of charged radicals. The substrate is mounted on the grounded electrode that has a lower potential than the plasma (plasma is at positive potential). Thus only neutral or positively charged particles can diffuse towards it, which form the thin-film layer. This is how a direct plama PECVD system works. The system used in this work is different, although it is also a direct plasma system. A schematic of the PECVD reactor used in this thesis is shown in Figure 3.4.

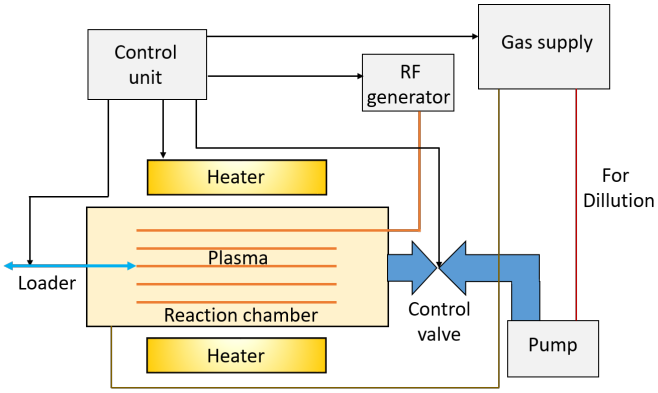

Figure 3.4: A schematic of a PECVD chamber, inspired from [14].

The PECVD tube in our Centrotherm tool is used to deposit anti-reflection layers (SiN_x and SiO_xN_y) and aluminium oxide passivation layers. The system has the capability to have silane (SiH_4), hydrogen (H_2), ammonia (NH_3), nitrogen (N_2) and trimethylaluminium ($Al_2(CH_3)_6$) gases. The plasma generated remains in between the two plates and in this way the layers are deposited on the samples. We use a frequency between 10-100 KHz for our application. We use an approximately 80-nm thick SiN_x:H as the anti-reflection coating and the hydrogenation source. The hydrogen passivates the defects present at the interface between the silicon wafer and silicon-oxide layer [15, 16]. The wafers are flipped after the first deposition and then the second side deposition is performed to achieve the symmetric sample structure. The second deposition time is altered in such a way that the SiN_x thickness is approximately 80-nm on both sides.

3.4. Metallisation

In this section, the two essential steps related to the final sample preparation are explained: screen printing and fast firing.

3.4.1. Screen Printing

In 1975 screen printing was for the first time presented as a metallisation technique for solar cells by Ralph et al. [17].

The technique evolved rapidly and now is the dominant technique of metallisation for solar cells [18]. The reason for the popularity of this technique are due to the low capital investment involved and high throughput. Screen printing has also proved to be a cost-effective, reproducible, and robust technique [19]. The continuous improvements in screen design and the pastes used has enabled screen-printing to continuously evolve as now structures can be printed more accurately and with high aspect ratios (for fingers of solar cells, a higher aspect ratio is preferred) [20, 21]. This has kept screen-printing compatible and, in many cases more optimum for use as compared to other techniques of metallisation [22].

A schematic of the screen-printing process is presented in Figure 3.5. There are three main phases involved in screen printing [23]:

1. Filling/flooding phase: In this step, the paste is filled in the openings in the screen areas by the flood bar.

2. Contact phase: After flooding of the paste, the squeegee presses the screen on the substrate. This forces the paste in the screen through the openings on the substrate.

3. Final phase: In this phase, the paste is released from the screen, as the screen moves away from the substrate.

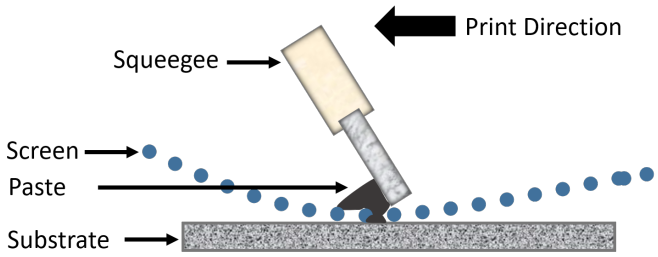

Figure 3.5: A schematic of screen printing process.

In this work, two screen printers were used: a Baccini printer and an ASYS screen printing line with Ekra XH-2 screen printer. The ASYS/EKRA line is fully automated with a belt dryer also coupled to it, as shown in Figure 3.6. This system is designed for high throughput. Different screens are used throughout the work depending on the requirements of the experiments and the devices.

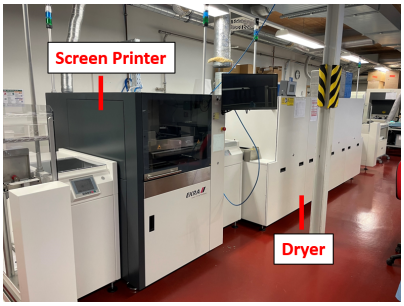

Figure 3.6: Actual picture of the ASYS screen printing line with Ekra XH-2 screen printer.

3.4.2. Fast firing- contact sintering

A rapid pass through successively increasing temperature zones is required to form the final metal-silicon contact. This is usually performed in a fast-firing furnace with IR lamps for achieving high temperature. We use a commercial Centrotherm D0-FF-8.600-300 fast-firing belt furnace in this work. This furnace has six zones where the temperatures can be set to achieve the desired temperature profile. The whole length of the furnace is 8.6 m.

An example of a typical fast-firing profile is shown in Figure 3.7. This profile was measured using a thermocouple attached to the sample. In addition to the set temperature, the belt speed can also be varied to change the thermal budget for contact formation. Throughout the work whenever necessary all the parameters pertaining to the fast-firing process will be mentioned.

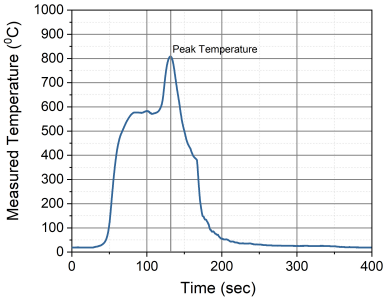

Figure 3.7: An example of a typical fast-firing temperature profile used for contact sintering of silver paste.

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4

Characterisation Techniques

Scientific research is one of the most exciting and rewarding of occupations.

Frederick Sanger

This chapter explains the characterisation and measurement techniques used throughout the work. Commonly used microscopic and optical techniques are explained in the first section. The second and third section are about the Electrochemical Capacitance-Voltage (ECV) technique and the photoconductance method, respectively. The forth section is about the contact resistivity measurement from transmission line method (TLM). The fifth section explains the method for extraction of metal-polysilicon recombination current density (J_{0met}) from photoluminescence imaging.

This chapter is about the different characterisation and measurement techniques used in this work. The two most important quantities: Contact resistivity and $J_{0\text{met}}$, for the characterisation of the metal-polysilicon contact are also explained in detail.

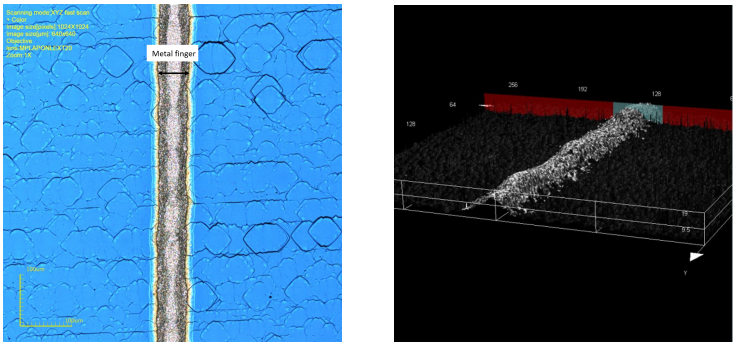
4.1. Microscopic and Optical measurements

In this section laser scanning microscope, scanning electron microscope, Spectral Ellipsometer and Spectrophotometer are explained.

4.1.1. Laser scanning microscopy

A laser scanning microscope (LSM) is based on the principle of confocal optical system. In a confocal system, a spatial pinhole is used, which blocks the out of focus light during image formation. In a laser scanning microscope a specific wavelength of laser light is used, which travels in a straight line, such that the unnecessary scattered light is avoided. This improves the contrast as compared to an optical microscope, which illuminate the sample evenly. Using a laser scanning microscope information is only drawn from the focal position as the reflected light from places other than the focal position is blocked at the pinhole. This makes the LSM form a perfectly focused clear image with good contrast.

We used an Olympus OLS 400 LEXT microscope for taking images to view the surface topography for the samples. These images were also used to determine the width and height of the screen printed contacts. In this work, surface finish were statistically evaluated with regards to the Sdr (%) values. The Sdr value is defined as the developed interfacial area ratio, i.e. additional area contributed by the texture as compared to the flat area. A higher Sdr value corresponds to a higher increase in the total surface area of the sample. These values were calculated from the laser scanning microscope images using a calculation routine in Mountain Map software, which is well explained in the literature[1]. An example of an optical and 3-dimension screen printed finger is shown in Figure 4.1a and 4.1b, respectively.



(a) (b)

Figure 4.1: Example of images of a screen printed finger from Olympus OLS 400 LEXT microscope; a) optical image, b) 3-dimensional image.

4.1.2. Scanning electron microscope

Scanning electron microscope (SEM) is one of the most versatile tools in examining and analysing microstructure morphology and microscopic topographical features. The SEM works on producing signals from the interaction of electrons, generated by an electron source, with the sample. The interaction of electrons with the sample produces: secondary electrons, back-scattered electrons, and diffracted back-scattered electrons. The secondary electrons emitted from the sample are used primarily to detect the morphology and the topography of the sample, while the back-scattered electrons show the contrast in the elemental composition of the sample. An additional advantage of SEM is that it can be used to get chemical information from the characteristic X-rays generated from the interaction of the electron beam with the sample. [2]. The main components of a SEM apparatus are:

1. Electron source: This generates the electron beam which interact with the sample. Normally, there are three types of electron sources; i.e. Field emission gun (FEG), Tungsten filaments, Lanthanum hexaboride.
2. Lenses: Several condenser lenses are used for focusing the electron beams.
3. Scanning coils: They deflect the electron beam over the sample.
4. Detector: The detectors differentiate the electrons generated from the samples.
5. Accessory: Power supply, vacuum system and output devices.

The SEM images in this work were taken by the University of Konstanz using a Zeiss Neon 40 EsB thermal field emission SEM apparatus. The system is equipped with two detectors for secondary electrons: A so-called in-lens detector located inside the electron column and an Everhart-Thomley detector that is positioned next to the electron column, resulting in a stronger topography contrast. Throughout the work, we compare images with same magnification as well as from the same detector.

For taking the top-view images, the samples were pre-processed with a sequence of chemical processes (Chemical etch back), which involves HNO_3 and HF dips for different duration. This is done so as to remove the bulk silver (65% HNO_3 dip of 45 min), to remove the glass layer (5% HF dip for 5 min) and finally to remove the silver crystallites left from the glass layer (65% HNO_3 dip of 45 min).

We used different kinds of sample preparation in order to obtain: top-view images, cleaved images and cross-sectional images from the SEM apparatus. This was done to see different features in the samples. An example for the top-view images after the chemical etching steps are shown in Figure 4.2. The different features in the images will be explained in the later chapters in detail. The cleaved images were taken by cleaving with a diamond tip cutter, for cross-sectional images we milled the samples separately after chemical etch back. We also took cross-sectional images without chemical etch back. These images were ion milled using

a Hitachi ArBlade 5000, which uses Argon ions to sputter the target. The ion gun is fixed, and the sample holder moves during milling.

An example of a cleaved sample after the complete etch back of the metal finger is shown in Figure 4.3. The polysilicon layer on top of a crystalline wafer is marked in this figure. The various topographic features will be studied in later chapters. An example of a cross-sectional SEM image is shown in Figure 4.4. This image is for a sample without any chemical etching steps.

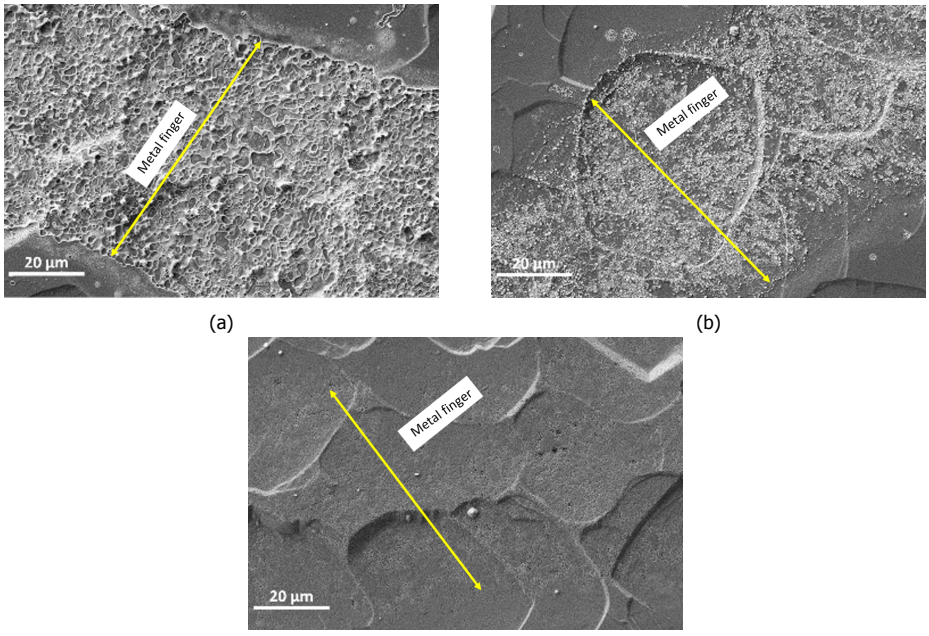


Figure 4.2: Example of top view images after the chemical etching steps; a) Bulk silver removed, b) Glass layer removed, and c) silver crystallites removed .

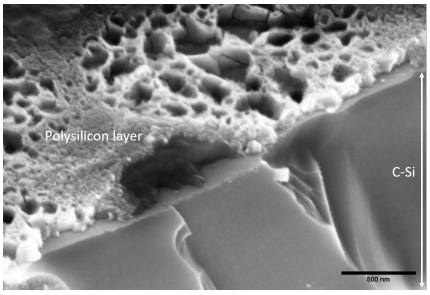


Figure 4.3: An example of an oblique view SEM image of a cleaved sample.

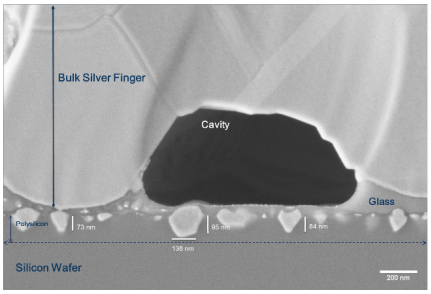


Figure 4.4: An example of a cross-sectional SEM image.

4.1.3. Spectroscopic ellipsometer

Ellipsometry is an optical measurement technique that characterizes light reflection from samples [3]. Ellipsometric measurement are very precise and reproducible owing to the measurement of the change in polarized light upon reflection from a sample. The name 'ellipsometry' comes from the fact that polarized light often becomes 'elliptical' upon light reflection. Ellipsometry measures the two values Ψ and Δ. These represent the amplitude ratio (Ψ) and phase difference (Δ) between light waves known as p- (parallel) and s- (perpendicular) polarized waves. Mathematically, these two values are related by what are called as fundamental equations of ellipsometry. These equations are derived by using Fresnel equations and reflection coefficients (r^p and r^s) [3]. In short, the most important equations are shown below,

$$\rho = \tan(\Psi) \cdot e^{j \cdot \Delta} \tag{4.1}$$

$$\rho = R^p / R^s \tag{4.2}$$

$$R^p = |r^p|^2, R^s = |r^s|^2 \tag{4.3}$$

In our work, we use ellipsometry for determination of the thickness of polysilicon, of SiO_x and SiN_x layers. The thickness of SiO_x and SiN_x layers on c-Si wafers can be measured easily, as the refractive index is quite different. For measurement of polysilicon layer thickness, it was beneficial to prepare dedicated samples. The samples were saw damage etched and then a thermal oxide with thickness of 180 to 190-nm was grown on it. This approach was followed to facilitate the ellipsometer model fitting. Afterwards the polysilicon layer was deposited on the oxide and the thickness measured with a fixed silicon oxide thickness. A SENTECH SE 800-PV tool is used for spectroscopic ellipsometery in the work.

4.1.4. Spectrophotometer

Spectrophotometer is used for the estimation of the optical properties (reflection, transmittance and angular intensity distribution) of the samples. From the measurements of reflection and transmittance, we can estimate the absorption in the spectral range of 300 - 1200 nm. This range is selected on account of the optical absorption associated with the silicon cells. In this work, a Perkin Elmer Lambda

950 spectrophotometer is used. It utilises a deuterium arc lamp for ultraviolet light and a tungsten-halogen lamp for visible and infrared light, hence covering a broad spectrum from wavelength of 175 to 3300-nm. The measurements of reflection and transmittance were done utilising integrating sphere as shown in Figure 4.5.

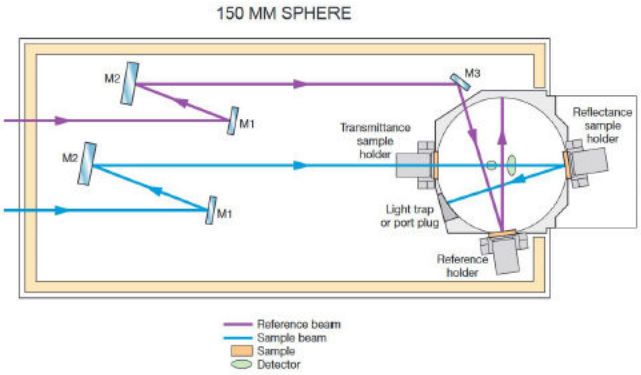


Figure 4.5: A schematic with the integrating sphere set-up used in this work [4].

By comparison with a reference beam the values of reflection (R) and transmittance (T) are computed.The absorptance (A) by the film is calculated from the following relation:

$$A = 100 - (R + T) \tag{4.4}$$

All the above values are in percentages as they are taken relative to the reference beam.

4.2. Electrochemical capacitance-voltage technique

In this work we use Electrochemical Capacitance-Voltage (ECV) technique for determining the doping profiles for the samples. In ECV technique, an buffered electrolyte solution (Ammonium hydrogen fluoride,$NH_4F{\cdot}HF$) is used to create Schottky contact, by etching of the sample surface. This allows control over the etching depth. The ECV method consists of recurring sequence of measuring C-V and then controlled etching of the sample. For the measurement of the active dopant concentration, an external voltage is utilised, which depletes the sample surface of the majority carriers. This enables the measurement of the capacitance. Then, the active doping concentration (N) is obtained using Equation 4.5 [5, 6].

$$N = \frac{-2}{q \cdot \epsilon_0 \cdot \epsilon_r \cdot A^2 . \frac{d(C^{-2})}{dV}} \tag{4.5}$$

Here, C is the capacitance, q the elementary charge, ϵ_0 is the vacuum permittivity, ϵ_r is the c-Si relative permittivity, and A is the area. Schematic of an ECV set-up is shown in Figure 4.6. We used an Wafer profiler CVP21 set up for the

doping profile measurements. In our work, we used the ECV measurements for dopant concentration profiles for n^+ polysilicon/SiO_x layer stacks.

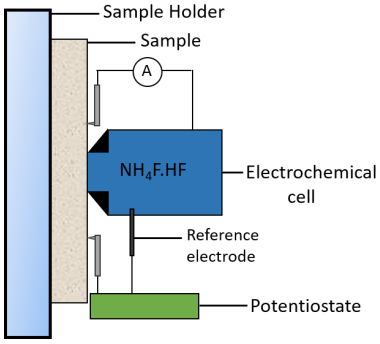


Figure 4.6: A schematic representation of the ECV measurement setup.

4.3. Photoconductance decay measurements

In this work we utilise, Photoconductance decay (PCD) measurements for determining the effective minority carrier lifetime (τ_{eff}), the recombination current density from the doped layers ($J_{0\text{pass}}$) and implied open-circuit voltage (iV_{oc}). The $J_{0\text{pass}}$ and iV_{oc} are used to classify the passivation quality of the samples studied in this work. A WCT-120 Sinton photoconductance lifetime tester was used in this work. During a PCD measurment, a flash is used to generate extra electron-hole pairs in the sample. A reference cell and a RF coil measure the light intensity and the conductance ($\Delta\sigma$) of the sample. From these measurements the excess charge carrier density (Δn) is computed using the Equation 4.6,

$$\Delta n = \frac{\Delta\sigma}{q \cdot (\mu_n + \mu_p)} \tag{4.6}$$

Herein, q is the elemental charge, μ_n is the electron mobility and μ_p is the hole mobility. The iV_{oc} is calculated according to the Equation 4.7 [7, 8].

$$iV_{oc} = \frac{k \cdot T}{q} \cdot ln(\frac{n \cdot p}{{n_i}^2}) \tag{4.7}$$

where n and p are the total electron and hole concentrations. For a n-type silicon, the n=N_{d}+Δn, and p=Δn. In our measurements, we always use the Quasai-Steady-State Photoconductance (QSSPC) state. In this state the carrier concentration is in steady-state, such that the generation and recombination are in balance. An estimate of the recombination in the diffused region is also provided by $J_{0\text{pass}}$, it is calculated using the Kane and Swanson slope method [8, 9]. According to the method by Kane and Swanson the slope of the Auger corrected inverse effective lifetime ($1/\tau_{corr}$) versus minority carrier concentration (Δn) plot, gives the $J_{0\text{pass}}$ [10]. The mathematical expression which relates the Δn and the total recombination is:

$$\frac{\Delta n}{\tau_{eff}} = \frac{\Delta n}{\tau_{int}} + \frac{\Delta n}{\tau_{SRH}} + \frac{J_{0pass} \cdot (N_d + \Delta n) \cdot \Delta n}{q \cdot W \cdot {n_i}^2} \tag{4.8}$$

In Equation 4.8, W is the substrate thickness, N_{d} is the substrate doping, $1/\tau_{corr} = 1/\tau_{eff} - 1/\tau_{int}$, τ_{int} is the lifetime corresponding to radiative and Auger recombination in the base and $1/\tau_{SRH}$ is obtained by linear approximation at Δn=- N_{d}, ${n_{\mathrm{i}}}^2$ is the intrinsic carrier density. The WCT-120 device use the Richter Auger model and considers the Schenk bandgap narrowing [11, 12].

To ensure accurate estimation of $J_{0\mathrm{pass}}$, all the parameters were always extracted in condition where the inverse lifetime had linear dependence with the excess charge carrier density. We would also like to point out that in literature sometimes $J_{0\mathrm{pass}}$ is referred as J_0, which mean the same things. In this work, we use $J_{0\mathrm{pass}}$ so as to avoid confusions with $J_{0\mathrm{met}}$ and J_{01}.

4.4. Contact resistivity

A metal silicon contact has a resistance associated to it. This resistance is defined by contact resistivity or contact resistance value. As this value is a direct measure of the resistive losses, it influences the series resistance and ultimately the fill factor of solar cell. A higher value of contact resitivity leads to a bigger fill factor loss, hence the aim is to reduce the contact resistance between the metal and silicon.

In this work, we have used Transmission Line Method (TLM) to determine the contact resistivity. This method was first proposed by Shockley, wherein current voltage measurements were done on metal contacts separated by variable distances [13]. Berger further improved the method and offered a more convenient way of determining the contact resistivity [14]. Later in the year 1984, Meier and Schroder presented the use of this method for application in solar cells in their work [15, 16].

In this method, parallel metal lines of fixed length and width (w) are printed, separated by a distance/pitch (d) on a sample. A schematic of the structure is shown in Figure 4.7. The resistance between any two contacts is measured and plotted as a function of d. From this plot the contact resistivity is determined.

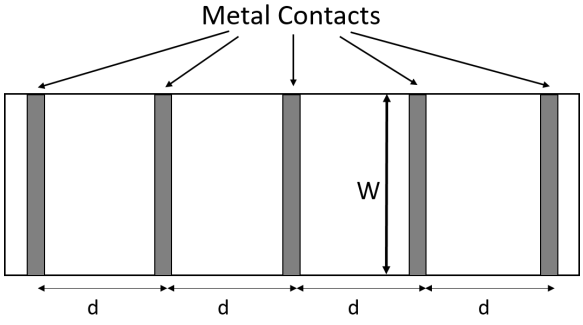


Figure 4.7: Top down view of a standard TLM structure.

From the IV measurement between each metal line, the resistance is plotted. An example is shown in Figure 4.8. In Figure 4.8, d_1 is equal to d, d_2 is 2.d and so on. From this plot, sheet resistance (R_{sh}) and the contact resistance (R_c) are obtained.

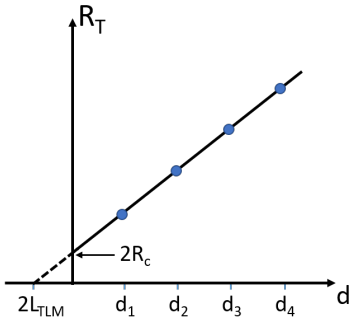


Figure 4.8: An example of the plot of resistance (R_T) Vs distance (d) for standard TLM.

The mathematical Equation 4.9, shows the total resistance (R_T) of the TLM structure from the plot.

$$R_T = 2 \cdot R_c + \frac{R_{sh} \cdot d}{W} \tag{4.9}$$

In semiconductor devices such as solar cell, the current is not homogeneously distributed. This phenomenon is refereed as current crowding effect. Hence, the definition of ρ_c, where the supposition of a uniform current density per unit area is considered becomes ambiguous. For this purpose,a lumped circuit or the distributed resistive network model is used. In this way, the current flow under the contact can be explained better. This is why it becomes important to define the transfer length (L_{TLM}). The transfer length can be thought of as the effective length of the contact. The value of the transfer length can be computed from the relation in Equation 4.10.

$$L_{TLM} = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{4.10}$$

With further mathematical analysis the contact resistivity can be related to contact resistance as presented in the Equation 4.11 [16]. Using this relation the contact resistivity values are generated from the plot of the resistance and distance.

$$\rho_c = \left(\frac{R_c \cdot W}{\coth(L/L_{TLM})} \right)^2 \cdot \frac{1}{R_{sh}} \tag{4.11}$$

The Equation 4.11 can further be simplified, considering two scenarios, For L $\leq$0.5 L_{TLM}), $\coth(L/L_{TLM}) \approx L_{TLM}/L$ and,

$$\rho_c = R_c \cdot L \cdot W \tag{4.12}$$

and for L ≥1.5 L_{TLM}), $\coth(L/L_{TLM}) \approx 1$ and,

$$\rho_c = R_c \cdot L_{TLM} \cdot W \tag{4.13}$$

For the accurate estimation of the contact resistivity the majority of the current flow should be through the thin layer, that means there is no flow to the bulk of the material. To maintain this, usually an opposite polarity base is used and the thin layers are deposited on top of it. This makes the junction resistivity so high that no current flow to the base. Throughout the work, we used 10-mm width for metal fingers with a spacing of 2-mm. In case of a variation from the above finger width and spacing, it will be mentioned.

We only measure a lumped (effective/apparent) contact resistivity containing potential contributions between metal paste and polysilicon layer and to a smaller extent between interfacial oxide and bulk wafer. The schematic of the structure we use for measurement of the contact resistivity in this work is shown in Figure 4.9. Until specified, this is the structure we will use throughout the work. The contact resistivity values are always presented with the corresponding standard deviation throughout the thesis. In Chapter 5, we will present experiments to further understand contact resistivity for n^+polysilicon/SiO_x-silver contact.

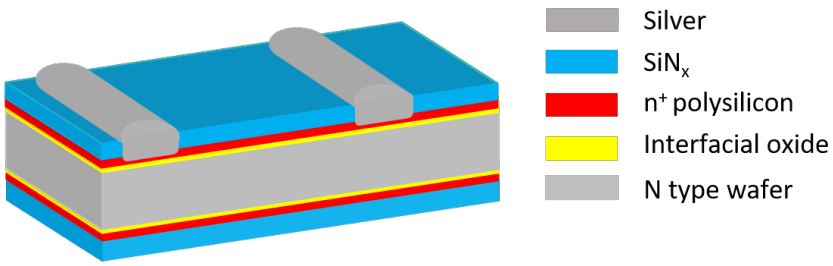


Figure 4.9: Schematic of the structure used for TLM in this work. The samples are symmetric in nature, with only one side metallised. The schematic is not to scale.

4.5. Metal-polysilicon recombination current density

After contact resistivity, the second important parameter for comparing metal polysilicon contacts is the metal-polysilicon recombination current density ($J_{0\mathrm{met}}$). This parameter is used to quantify the recombination which happens at the metal-polysilicon interface. As explained in previous chapters a perfect passivating contact is such that there is no additional recombination after metallisation. This means that the recombination at the metal-polysilicon interface is equal to the recombination in the unmetallised areas. Thus, the value of recombination current density remains same in the metallised and unmetallised areas of the sample. This enables reaching high open circuit voltages for the cells with polysilicon based passivated contacts, as no additional recombination comes from metallisation.

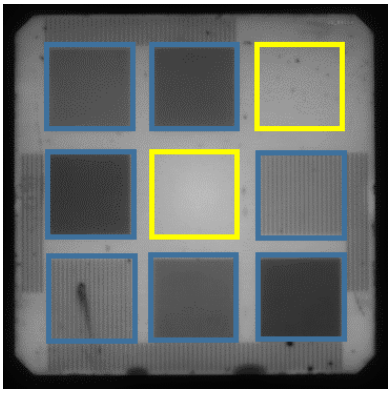


Figure 4.10: An example of PL image with the print pattern of the sample used in this work. The blue boxes show the areas with different finger spacing and the yellow boxes are the unmetallised areas. The fingers at the edges were used for contact resistivity measurements.

Various methods exist which can be used to compute the metal-polysilicon recombination current density. Hoenig utilises a method which uses the difference between pseudo fill factor and fill factor to get the J_{02} term in order to calculate the metal-silicon recombination current density. The method used by Hoenig requires the fabrication of the complete solar cell structure, with different front metallisation patterns, so as to have metal area fraction variations [17]. Due to the need to fabricate the complete cell structure this method is not easy to utilise. Ciftpinar et al. utilise two different approaches to compute the contact recombination value. One wherein the Quokka generated PL images are fitted to the experimentally obtained PL images, with the contact recombination as the variable. The other approach uses metallization of cell structures and then utilizes the V_{oc} values to get the contact recombination [18]. Padhamnath et al. utilise another approach in computing the metal-polysilicon recombination current density. They utilises a combination of PL images and a finite element simulator, Griddler [19]. Chen et al. utilise a method, wherein they use symmetrical samples. The samples are screen printed metallised to have 9 regions of different metal area fraction. Afterwards the metal is etched off in aqua-regia solution and the $J_{0\mathrm{pass}}$ is estimated from the PCD measurements for each of the 9 different regions. From these values the $J_{0\mathrm{met}}$ is computed. The similar aspect in the above methods is to print a dedicated pattern on the layer stacks. Various research groups have their own designed metal patterns [18, 20–27].

The methods utilised in this thesis is based on photoluminescence (PL) images, combined with photoconductance measurements and fitting. This method is simple, easy to understand and implement. Symmetrical samples which are easy to process are utilised, as well the method used does not require the use of any wet chemical steps. The uncertainties arising from the sample processing are also taken into account in the $J_{0\mathrm{met}}$ computations. We use a layout with five different metal patterns. An example of a sample with the layout is shown in Figure 4.10. These metal patterns have different finger pitches and hence the metal fraction is different. To incorporate the variations which can be due to process differences and

inhomogeneity in the layer thickness, we add redundancy to the metal pattern. Two squares remain unmetallised, these areas are used to do the QSSPC measurements for implied open circuit voltage and the saturation current density from the doped layers ($J_{0\text{pass}}$) after fast firing. The layout also contains TLM structures for measurement of the contact resistivity and metal structures for measuring line resitivity. Hence, the layout used in this work, serves three purposes: for estimation of $J_{0\text{met}}$, contact resistivity measurements and line resistivity measurements. Further details on this method can be found out in literature. [28–30] Extraction of the $J_{0\text{met}}$ from the PL is done in the following steps in this work:

- A layout containing patterns with different metal fractions is printed on the symmetric samples. After fast firing of the sample, a PL image is recorded.
- The PL image is converted into an iV_{oc} image. This is done with the use of the quasi-steady-state photocoductance (QSSPC) measurement [8]. The iV_{oc} measured in the centre of the sample is used to scale the PL intensity and thus a complete iV_{oc} image is created.
- The next step is to calculate J_{01} from the iV_{oc} image. This is done taking into account the one diode model of a solar cell.
- Finally, the $J_{0\text{met}}$ value is determined from the linear fit of the J_{01} versus the metal fraction plot. This utilises the measured $J_{0\text{pass}}$ as an input value.

In Figure 4.11 the iV_{oc} calibrated image is presented, from this image the J_{01} is calculated for each metal fraction using the 1-diode model.

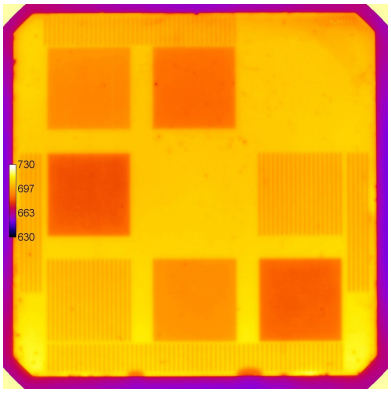


Figure 4.11: An example of implied V_{oc} calibrated image.

An example of the J_{01} plot versus the metal fraction is shown in Figure 4.12. As shown in the values generated from the fitting, an error in the slope is also computed. We have two squares per metal fraction, hence this error corresponds to the variations that might have cropped in due to sample preparation processes or wafer handling during metallisation.

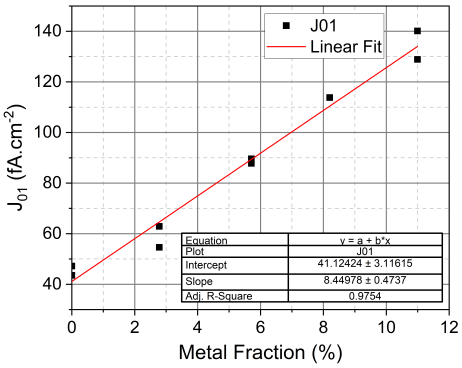


Figure 4.12: The J_{01} Vs metal fraction plot for the sample shown in Figure 4.11.

From this plot, the J_{Omet} is derived from the equation of line in the linear fit. The equation which relates the different recombination current densities steaming from the doped regions (J_{Opass}), the bulk (J_{Obulk}) and from the metal contact (J_{Omet}) with the metal fraction (f) is shown in Equation 4.14:

$$J_{01} = J_{0bulk} + (1 - f) \cdot J_{0pass} + f \cdot J_{0met} \tag{4.14}$$

The Equation. 4.14, can be transformed as in Equation. 4.15. This equation can now be directly related to the equation of the line from the linear fit from the plot in Figure 4.12. This yields the relation for the J_{Omet} as in Equation. 4.16, with the slope calculated from the plot in Figure 4.12.

$$J_{01} = J_{0bulk} + J_{0pass} + f \cdot (J_{0met} - J_{0pass}) \tag{4.15}$$

$$J_{0met} = Slope + J_{0pass} \tag{4.16}$$

The error in the slope of the linear fit is a measure of the uncertainties arising due to the inhomogeneities from processing, which could have crept in during the deposition steps or the chemical steps. We will use this uncertainty in the later plots of J_{Omet} with the statistical uncertainties coming from multiple samples in a group.

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5

Firing through silver paste for contacting n^+ polysilicon layers

The very nature of science is discoveries,
and the best of those discoveries are the ones you don't expect.

Neil deGrasse Tyson

In this chapter, different firing through silver pastes for metallisation of n^+ polysilicon/SiO_x layer stacks are used. From the results of contact properties (J_{0met} and ρ_c) and the print quality, the best suited silver paste application on the n^+ polysilicon/SiO_x layer stacks is found out. The contact properties are also studied with respect to the thermal budget during contact sintering process. Photoluminesce and SEM images are used to visualise the silver-polysilicon contact. J_{0met} of the order of J_{01}, with appreciably low ρ_c is obtained justifying the name passivated contacts for this contact architecture. A detailed study on contact resistivity measurements for n^+ polysilicon/SiO_x layer stacks is also presented in this chapter.

This chapter is based on the following publications:

- *A. Chaudhary, J. Hoß, J. Lossen, R. van Swaaij, and M. Zeman,Screen printed Ag contacts for n-type polysilicon passivated contacts,in AIP Conference Proceedings, Vol. 2147 (AIP Publishing LLC, 2019) p. 040002.*
- *A. Chaudhary, J. Hoß, J. Lossen, R. van Swaaij, and M. Zeman, Advancement in screen printed fire through silver paste metallisation of polysilicon based passivating contacts,in AIP Conference Proceedings, Vol. 2367 (AIP Publishing LLC, 2021) p. 020003.*

5.1. Introduction

The improvement in the solar cell efficiencies goes hand in hand with the progress made in the silver pastes [1]. A paste can be defined as a homogeneously dispersed mixture of organic and inorganic components [2]. Most of the silver pastes applied in this work are fire-through pastes, which use a high-temperature step (exposure to temperatures in between 700-850°C) for contact formation. These are called as fire-through silver pastes as a sintering step is needed to etch the silicon nitride layer and form the contact. The melting point of silver is 961°C [3]. However, in silver pastes, sub-micrometer or nanometer-sized particles are used, and due to the size, the melting point is reduced. This phenomenon is called as melting point depression [4, 5]. This is one of the reasons why for forming the metal-silicon contact, the requirement of reaching the melting point of silver is not required. Hence, lower temperatures are enough to achieve good contact. Another reason for the reduced melting point of silver in the pastes is the addition of lead glass particles. This can be understood more as the colligative property of solutions. The phase diagram for the two-component system of silver and lead glass is good for understanding this lowering [6]. It also explains that for melting the silver and lead, temperatures above the eutectic point are required. This can be considered as the minimum temperature required to start the contact formation process.

The major components of the sliver pastes are:

1. Silver particles, constitute almost 70-85% by weight.
2. Organic solvents, make up 10-25% by weight of the paste. They are usually mixtures of ethyl cellulose based compounds and terpineol [7].
3. Additives, they are almost 1-5% by weight.
4. Glass frits, are almost 1-5% by weight.

The combination of the above components determines how the silver paste will make contact with the silicon layers. According to [7, 8], the contact formation can be described by the following steps: Step 1: The glass frits contain glass particles based on lead oxide which etch the silicon nitride anti-reflection coating (ARC) exposing the silicon layer below to the paste constituents, at temperatures below 550°C. Step 2: In the temperature range of 550-700°C, the lead formed in this reaction alloys with the silver particles and helps in liquid phase assisted sintering. Step 3: The silver dissolves in the liquid formed before and diffuses to the silicon surface in the next step. In this step, silver ions participate in the reactions involving oxidisation of silicon to silicon oxide and start attaching to the silicon substrate. Afterwards, in the step 4, the samples are cooled such that the silver precipitates and forms nanocrystals [9, 10]. There are many research groups and industrial manufacturers optimising the performance of the screen printing pastes by modifying the glass powder additive, silver particle size and the fast firing temperature profiles [11, 12], in order to improve the contact properties and the print quality.

As passivating contact structures were of big interest during the time our research started, we could source first paste versions adapted to the use on passivation contact structures. This was done to find the most suitable silver paste for our polysilicon/SiO_x layer stacks. This is the essence of the work presented in this chapter. The main requirements which we looked at are listed below:

1. Good electrical properties: contact resitivity (ρ_c) (less than 10 $m\Omega.cm^2$) and finger line resistance (R_l) (less than 2 $\Omega.cm^{-1}$))

2. Low recombination at the metal polysilicon interface (J_{0met})

3. Printability (no breakages or gaps in the printed lines) and high aspect ratio with line widths in between 40-60 µm .

We compare commercially available silver pastes in this chapter. For simplicity, we call them generation 1 (G1) pastes. These pastes were provided by Heraeus Photovoltaics and are used for phosphorus diffused layers. From the feedback, that we provided to Heraeus, they modified the silver pastes and provided dedicated pastes for polysilicon layers, called as generation 2 (G2) and generation 3 (G3). The generation 2 pastes were developed in 2018 and early 2019, and generation 3 in 2019 and 2020. One additional paste is also investigated and was supplied by another silver pastes manufacturer in the year 2020.

This chapter is divided into five sections. In Section 5.2 the design of experiments and sample preparation is discussed. In Section 5.3 the properties of the contacts made using the G1 and G2 pastes are compared. Subsequently, in Section 5.4 the contacts made using the G3 paste are presented. The second last section expands on the understanding of contact resistivity for the silver-n^+ polysilicon/SiO_x stack. Finally, in Section 5.5 the conclusions of the results presented in this chapter are given.

5.2. Experimental design and sample preparation

In the experiments presented in this Chapter, n^+ polysilicon/SiO_x passivated layer stacks were metallised. M2 sized n-type CZ silicon wafers of ≈ 180 µm thickness were used as the substrate for this experiment. The substrates used for the experiments had a base resistivity of approximately 1 Ωcm. The substrates were saw damage etched and cleaned in piranha solution, before deposition of the layer stacks. In the first experiment, where the first generation and second generation pastes are compared, the samples were processed by an external partner as at that time we did not have the capability to deposit LPCVD polysilicon layers in house. These samples were annealed at a temperature of 900°C for 30 minutes for a 150-nm thick polysilicon layer and 850°C for 30 minutes for a 75-nm thick n^+ polysilicon layer. The other experiments in this section were performed with samples which had standard silicon nitride layers between 75 and 80-nm thickness and were annealed at a temperature of 825 °C for 30 minutes, with a 150-nm thick n^+ polysilicon layer which was deposited in house. The screen printing design for metallisation is

explained in Chapter 4, which is used for measuring the contact resitivity and the PL images.

Measurements of implied open-circuit voltage (iV_{oc}) and the saturation current density ($J_{0\mathrm{pass}}$) from the doped layers were performed using a Sinton WCT-120 lifetime tester [13]. The measurements were carried out in the center region of the samples. This was done because the center region remains unmetallised throughout the process. This is explained in Chapter 4.

Samples were metallised by screen printing with different pastes. I have marked them as Paste G1a, G2a, G2b, G2c, G3a, G3b and G3c. Major paste manufacturer Heraeus supplied these pastes. A paste from another manufacturer was also compared and is referred to G3d. In the names, a,b,c,d,e denote the different pastes from the same generation. After metallisation, another QSSPC measurement was carried out and the Photoluminescence (PL) images were recorded. Based on the QSSPC results, the PL images were converted into iV_{oc} calibrated images. From these the recombination current density (J_{01}) is calculated using the single diode model, which is then plotted as a function of metal fraction. Finally, the $J_{0\mathrm{met}}$ is extracted from the linear fit of this data. Contact resistivity was measured using Transmission Line Measurement (TLM) method.

The fast-firing peak temperature is also varied in the high temperature zones, to see the effect of thermal budget on the contact properties. This also provides us with the information about the possible process window which can be utilised for contacting when we develop n^+ polysilicon/SiO_x passivated solar cells.

Furthermore, Scanning Electron Microscope (SEM) images were used to visualize and analyse the interface in order to gain understanding of possible microscopic explanations for the observed macroscopic characteristics. Three step chemical etch back of silver and glass frit was used to prepare the samples for SEM, as explained in Chapter 4. After each step, SEM images were recorded and compared with corresponding images for the other pastes.

5.3. Generation 1 and Generation 2 silver pastes

In this experiments, samples with 150-nm and 75-nm thick polysilicon layer were used. For all samples the passivation quality was measured. Good values for $iV_{0\mathrm{C}}$ (greater than 710 mV) and $J_{0\mathrm{pass}}$ (less than 15 fA.cm^{-2}) are obtained.

Table 5.1 shows the results from the generation 1 and generation 2 pastes. The contact resistivity values presented in the tables also contain the standard deviation. Standard deviation is used to show the variability in the measured values of the contact resistivity throughout the thesis. The values of $J_{0\mathrm{met}}$ obtained for Paste G2a and G2b are lower as compared to the Paste G1a. The lowest $J_{0\mathrm{met}}$ of 69 fA.cm^{-2} on a 150-nm thick polysilicon layer is obtained is for the paste G2b For equivalent samples metallised with paste G2a the lowest $J_{0\mathrm{met}}$ value is 81 fA.cm^{-2}. Contact resistivity for these samples was between $\approxeq$ 3 and 6.5 mΩ.cm^2, which is higher as compared to the state-of-the-art contacts on diffused surfaces [14–18].

From the results in Table 5.1, we selected paste G2b for further experiments, because of its lower $J_{0\mathrm{met}}$ value (in this experiment we did not take the uncertainty in $J_{0\mathrm{met}}$ into account) and fingers without any areas of low or no lay-down as compared

to Paste G2a. In the following experiments, the passivation quality for the samples after fast firing was also measured and the plot is presented in Figure 5.1. The passivation level is similar for all the groups of samples and hence the fast-firing range we investigate is good enough for hydrogenation of defects at the SiO_x/Silicon interface.

Table 5.1: The best values for $J_{0\text{met}}$ and ρ_c values obtained.

Paste	Polysilicon layer thickness (nm)	$J_{0\text{met}}(fA.cm^{-2})$	ρ_c $(m\Omega.\text{cm}^2)$
G1a	150	346	2.8±0.7
G1a	75	503	3.5±0.7
G2a	150	81	4.2±1.3
G2b	150	69	4.7±1.6

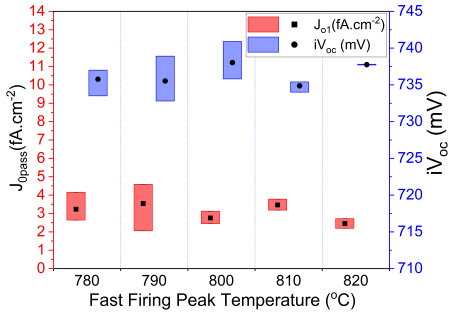


Figure 5.1: Passivation quality of samples (150 nm polysilicon layer, metallised with paste G2b) after fast firing.

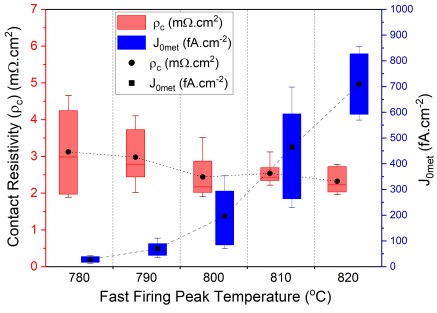


Figure 5.2: $J_{0\text{met}}$ and ρ_c values for the samples (150 nm polysilicon layer, metallised with paste G2b) fired at different fast-firing peak temperatures.

The results of the $J_{0\text{met}}$ and ρ_c are presented in the Figure 5.2. This plot shows

that a lower fast-firing peak temperature leads to a decrease in the $J_{0\mathrm{met}}$. A reduction of 96% in the mean $J_{0\mathrm{met}}$ value is obtained when the fast-firing peak temperature is lowered from 820°C to 780°C, while the contact resistivity does not increase substantially. The mean $J_{0\mathrm{met}}$ value at 780°C is 28 fA.cm^{-2}.

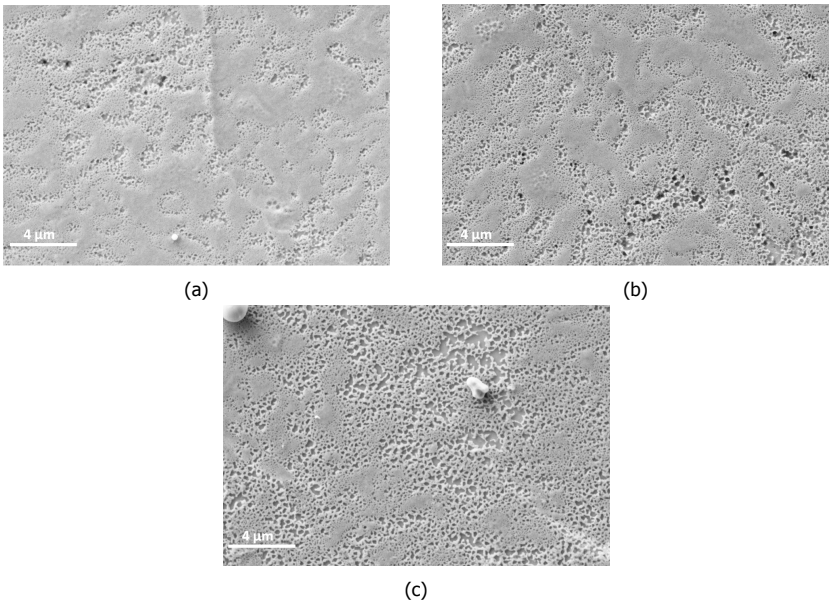


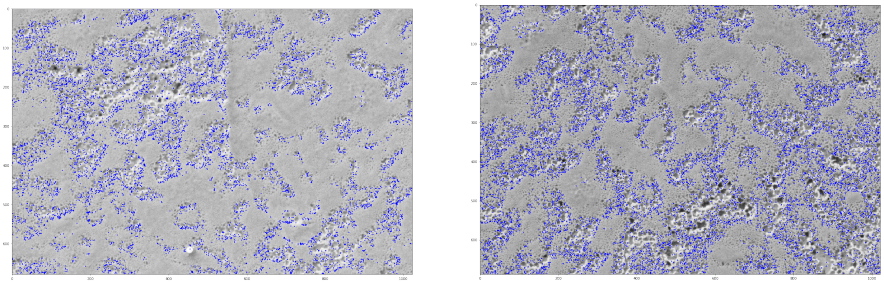
Figure 5.3: Top-view SEM images, fast fired at peak temperature of (a) 780°C, (b) 800°C and (c) 820°C. The polysilicon layer is shown after the removal of silver and the glass layer. The silicon wafer is also visible in areas where the polysilicon is missing (darker regions).

The contact resistivity values remain similar when the fast-firing peak temperature is increased from 780 to 820°C. The measured values are comparable to the values obtained for screen-printed fire-through silver paste on diffused silicon surfaces [14–19]. The reason for the similar values of contact resistivity across the fast firing peak temperature range will be investigated in later chapters.

To figure out the reason for a drastic increase of $J_{0\mathrm{met}}$ values from below 50 fA.cm^{-2} at a firing temperature of 780°C to values of 800 fA.cm^{-2} at 820°C, we compare top-view SEM images of the samples. Figure 5.3 shows the top-view SEM images of samples fired at 780, 800 and 820°C. The area which appears higher and brighter in the images is the polysilicon layer. The regions which appears as valleys/holes in the figures are the regions where the polysilicon layer has been removed/consumed by the silver paste constituents. It can be seen that the fraction of area with removed polysilicon increases as we increase the fast-firing peak temperatures. We think that this is an important reason for the lower $J_{0\mathrm{met}}$ values for samples fired at lower temperatures and this suggests that the increased $J_{0\mathrm{met}}$ values are due to a larger contact area between silver paste and silicon wafer. This also seems reasonable from the higher thermal budget enhancing the reactions of

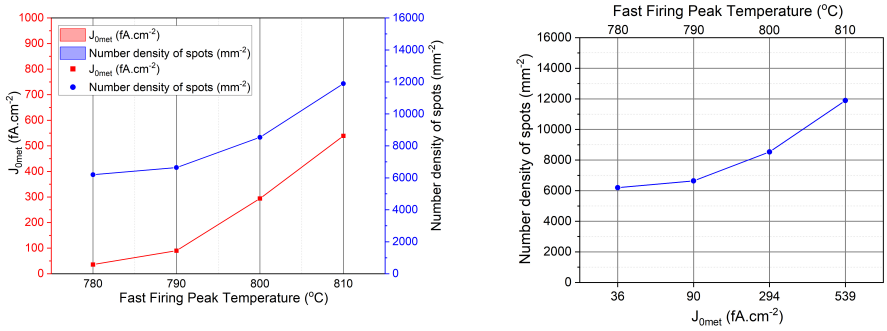
the silver paste constituents. From the presented images it is difficult to estimate how deep the silver crystallites reach into the polysilicon layer and this aspect will be studied in detail in the next chapters.

To quantify the increase in the number of sites, which corresponds to the polysilicon removed area, a python script was developed. The input to the Python script was the SEM image and the output was an image with the sites marked with blue spots and the number of these spots. The spots marked in the images correspond to the sites without polysilicon layer. Then this number is divided by the area of the image to generate a number density. Similar kind of methods have been used to analyse TEM (Transmission Electron Microscopy) images, although the method used in this work is easy to use and simpler [20]. The script used is added in Appendix A. To illustrate the results from the script, in Figure 5.4 the corresponding converted image for the samples fast fired at peak temperature of 780 and 800 °C are shown, the original SEM images are shown in Figure 5.3.



(a) (b)

Figure 5.4: Example of the converted SEM images for sample fast fired at peak temperature of (a) 780°C and (b) 800°C, showing the sites without polysilicon marked with a blue spot.

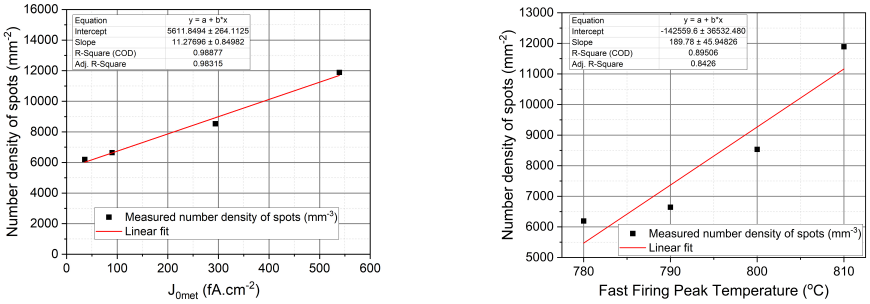


(a) (b)

Figure 5.5: (a) $J_{0\mathrm{met}}$ and the number density of spots for the samples fired at different fast firing peak temperature, (b) The number density of spots Vs $J_{0\mathrm{met}}$ of the sample.

Similar conversion was done for the other samples and Figure 5.5 shows the

number density of spots with the $J_{0\mathrm{met}}$ value for the sample with respect to the fast-firing peak temperature. As can be observed in Figure 5.5b, there appears to be a strong correlation between the number density of spots and the $J_{0\mathrm{met}}$ value with respect to the fast-firing peak temperature. A higher $J_{0\mathrm{met}}$ value corresponds to a higher number density, as seen in Figure 5.5b.



(a) (b)

Figure 5.6: (a)$J_{0\mathrm{met}}$ and number density of spots for the samples fired at different fast firing peak temperature, (b) Fast firing peak temperature Vs the number density of spots.

Assuming that all the spots contribute equally to $J_{0\mathrm{met}}$, a number density can be determined for which the $J_{0\mathrm{met}}$ would be zero, meaning that there is no recombination coming from the metallisation. For this purpose we have fitted the data to a linear relationship, as shown in Figure 5.6a. The number density of spots where $J_{0\mathrm{met}}$ is zero is the intercept from the plot, and is 5611 mm^{-2} with less than 5% error. As a further step, we plot the fast-firing peak temperatures with the measured number density as shown in Figure 5.6b. From the fit to the data we find that at a temperature of 782 $\pm$ 16°C the number density becomes 5611 mm^{-2} at which $J_{0\mathrm{met}}$ would become zero. Thus, this result shows that below 780 °C, there would be a possible temperature at which the metal polysilicon recombination would be zero for our samples, as well as there would be enough spots (places where the polysilicon layer is penetrated by the silver crystallites) such that electrical contact is established.

Although, when using this script for sample fast fired at the peak temperature of 820 °C, a problem arises. As seen in Figure 5.3c, the size of the area of removed polysilicon is large; this causes a problem in the script as the script takes a predefined size of the area as one spot. This was carefully done for the other samples, but it failed when the area became larger than the threshold. This points out that the script can be further improved. Although this script has revealed a strong correlation between the number density in the SEM images and $J_{0\mathrm{met}}$ within the range of fast-firing peak temperature from 790 to 810°C, this script is not utilised in further chapters due to the above-mentioned reason. The next comparison for samples metallised with silver paste G2b and G2c was also performed, in this comparison, the samples were fast-fired at 820°C. From the results, the mean $J_{0\mathrm{met}}$

values were similar at 655 fA.cm^{-2} for both the pastes, although the mean values for contact resistivity were different. The mean contact resistivity for the paste G2b was 1.8±0.3 mΩ.cm^2, while for G2c this was 2.1±0.6 mΩ.cm^2. These values are one of the lowest values obtained for polysilicon-based contacts [21]. From the generation 1 and 2 pastes, Paste G2b showed the best performance in terms of $J_{0\mathrm{met}}$ and contact resistivity.

5.4. Generation 3 silver pastes

The passivation quality of the samples used in this experiment, measured in the non-metallised area with the QSSPC are presented in Figure 5.7.

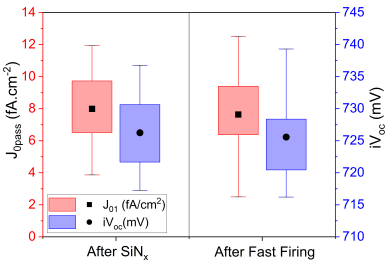


Figure 5.7: $J_{0\mathrm{pass}}$ and iV_{oc} for samples metallised using Generation 3 paste, after SiN$_x$ deposition and after fast firing.

An appropriate level of passivation is obtained for the samples, both directly after SiN$_x$:H deposition and after fast firing in the belt furnace, with mean iV_{oc} above 725 mV. This points out to the excellent passivation quality and the stability in the investigated fast-firing range of the n$^+$ polysilicon/SiO$_x$ layer stack.

We also analysed a wider window of fast-firing peak temperatures ranging from 760 to 820°C, in steps of 15°C. The lowest peak temperature was chosen to be 760°C, as going to a lower temperature could have adverse effects on the contact resistivity [22]. While going above 820°C, blistering was observed on the samples and hence 820°C is the upper limit. In Figure 5.8, the PL images of the samples metallised by Paste G3a, G3b and G3c, and fast-fired at peak temperature of 820 and 790°C are presented. The darker the metal print as compared to the unmetallised areas, the higher the recombination from metallisation. We can see how the contrast between the metallised and the unmetallised areas become almost negligible at fast firing peak temperature of 790°C. This shows the transition to a fully passivated contact when lowering the fast-firing peak temperature in conjugation with low contact resistivity values. For the samples metallised with Paste G3a, the transition is more profoundly visible.

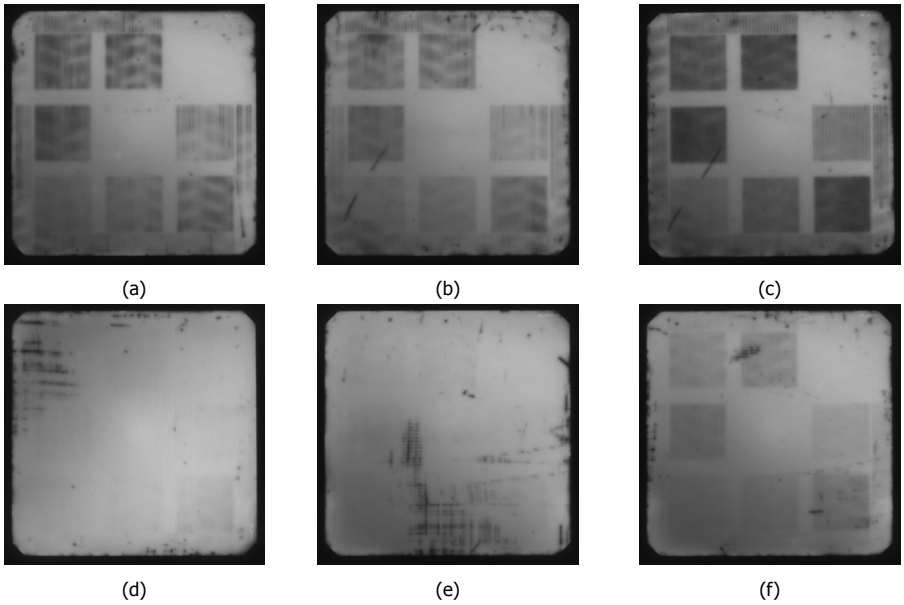


Figure 5.8: PL images of samples:(a) printed using Paste G3a and fired at 820°C; (b) printed using Paste G3b and fired at 820°C; (c) printed using Paste G3c and fired at 820°C; (d) printed using Paste G3a and fired at 790°C; (e) printed using Paste G3b and fired at 790°C; (f) printed using Paste G3c and fired at 790°C All the PL images were taken at the same optical parameters (illumination, aperture and integration time). Irregular black features like in the upper left corner of picture (d) are believed to be due to scratches. Squared black area, like in picture (c) are due to metal recombination.

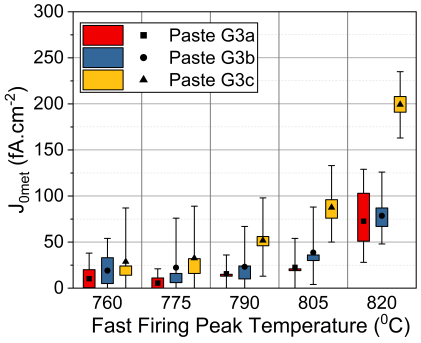
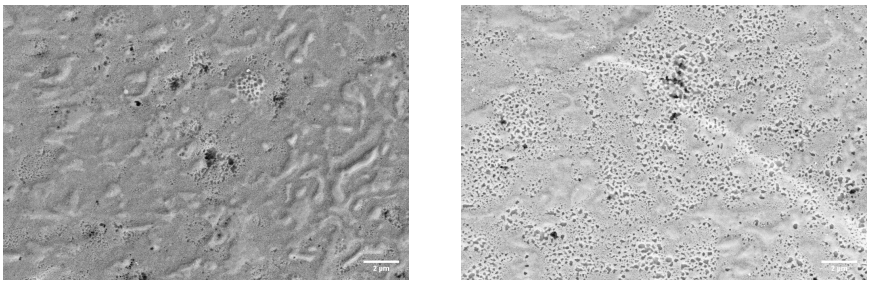


Figure 5.9: $J_{0\text{met}}$ values for the samples metallised with generation 3 pastes fired at different fast-firing peak temperatures.

In the same way, PL pictures were recorded for the entire investigated range of fast-firing peak temperatures. To quantify the metal semiconductor recombination, the $J_{0\text{met}}$ values were computed. Figure 5.9 shows the $J_{0\text{met}}$ obtained at different fast-firing peak temperature for the samples metallised with the three pastes. Of the

three pastes, paste G3c shows higher metal polysilicon recombination as compared to the other two generation 3 pastes. Pastes G3a has the lowest mean $J_{0\text{met}}$ values across the investigated range of fast-firing peak temperatures. For example, at fast-firing peak temperature of 805°C, it is 41% lower than paste G3b and 74% lower than for Paste G3c. At fast-firing peak temperatures below 805°C, the $J_{0\text{met}}$ is $\cong J_{01}$. The $J_{0\text{met}}$ values for the three pastes increases when the fast-firing peak temperature is increased. This is similar to what was observed earlier for the Paste G2b. To further understand and validate the reason for the trend as done for Paste G2b, SEM images were compared. The SEM images of samples metallised with Paste G3a, after the removal of metal and glass layer are presented in Figure 5.10.



(a) (b)

Figure 5.10: SEM images of samples metallised with Paste G3a and fired at a fast-firing temperature of (a) 760°C and (b) 820°C.

We can ascertain that the sample fired at higher fast-firing peak temperature have more sites where the polysilicon layer has been removed or damaged (visible as dark valleys and black spots in the images) as presented in the SEM images in Figure 5.10. These are the sites where the silver crystallites might get in contact with the silicon wafer. These sites were called as spots earlier. A lower number density of sites with damaged and removed polysilicon layer correlates with a low $J_{0\text{met}}$ value. This was also observed for other generation 3 pastes.

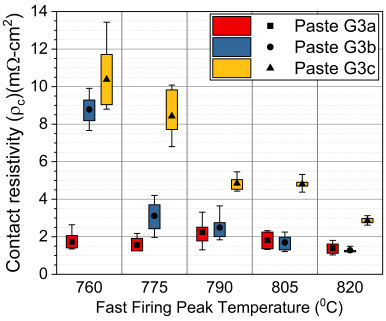


Figure 5.11: Contact resistivity values for the samples metallised with different generation 3 silver pastes.

The results for the contact resistivity are presented in Figure 5.11. For paste G3a, we do not observe a significant difference in the values at different fast-firing peak temperatures. The mean value of the contact resistivity remains below 2 mΩ.cm^2 for the fast- firing peak temperatures investigated, except at 790°C where it is slightly above at 2.2 ±0.7 mΩ.cm^2. Paste G3a shows good performance even at a low fast firing peak temperature of 760°C. The lowest mean value of 1.4 ±0.3 mΩ.cm^2 is obtained for Paste G3a fired at 820°C. However, for Paste G3b and G3c the contact resistivity increases on reducing the fast-firing peak temperatures. For example, for Paste G3c the contact resistivity increases from 2.8 ±0.2 mΩ.cm^2 at 820°C to 10.4 ±2.1 mΩ.cm^2 at 760°C. The rise in contact resistivity on reducing the fast-firing peak temperature is usually observed for fire-through silver paste used for contacting diffused silicon surfaces. Coupled together with the values of $J_{0\mathrm{met}} \cong J_{01}$ for samples metallised with Paste G3a, we can justify the name passivated contacts for our silver-polysilicon/SiO$_x$ contacts.

As a final check on the electrical properties of the Paste G3a, the line resistance was also measured. The results are presented in Figure 5.12. Line resistance is a parameter that defines the flow of the current through the printed finger. This relates to the print quality, like breaks in the print, to the cross-section (geometry/lay-down) of the paste as well as the overall conductivity of the paste used [23]. The values we obtain are comparable and even better than screen-printed fire through silver paste used on diffused surfaces with similar finger aspect ratios [19, 24].

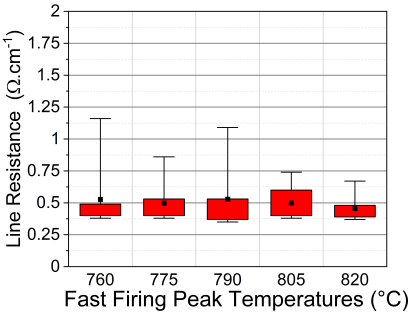
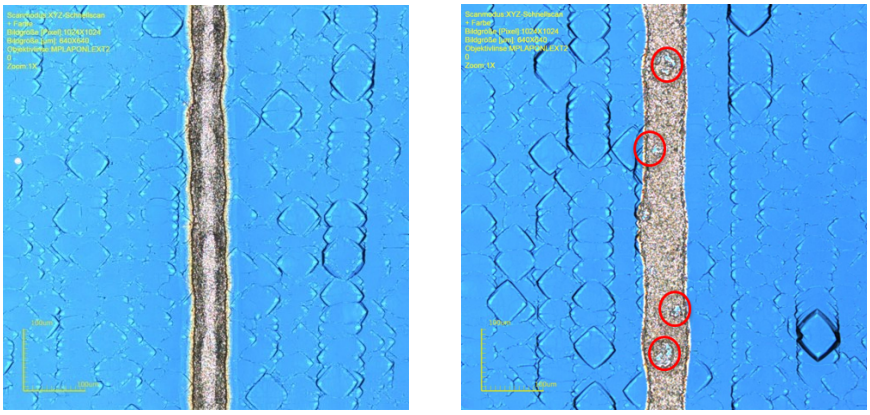


Figure 5.12: Line resistance values for the samples metallised with paste G3a.

The last paste comparison performed in this chapter is between Paste G3a and G3d. Paste G3d was manufactured by a different paste manufacturer. The LSM pictures of the fingers printed by the two pastes are presented in Figure 5.13. The aspect ratio for the two pastes was also calculated. For the fingers printed with Paste G3a it was around 0.32 and for Paste G3d was 0.12. The low aspect ratio for fingers printed with Paste G3d is due to the low height of the fingers (7±3 µm) as well as a slightly higher width than those printed with Paste G3a. The fingers printed with Paste G3a had a height of 16±4 µm, with finger width of 53±3 µm. The aspect ratio obtained with Paste G3a is comparable to that obtained for fingers, screen printed using fire-through silver pastes with similar screen openings [19].

As seen in Figure 5.13b, the finger printed with Paste G3d has holes and breakages. These features are marked with red circles to guide the eye. In an attempt to remove these breakages the printing parameters were optimized, but it turned out not to be possible to remove these features. For this reason Paste G3d is not considered for further utilisation.



(a) (b)

Figure 5.13: Representative LSM images of fingers metallised with (a) Paste G3a and (b) Paste G3d. Red circles denote the areas with no or little lay-down of paste in the fingers.

We found that Paste G3a outperforms all the other pastes tested so far and owing to this we regard this paste to be the best for our applications.

5.5. Contact resistivity for Ag-n$^+$ polysilicon/ SiO_x contact

Other than the high surface passivation quality and reduced metal-polysilicon recombination current density, low values of contact resistivity are also required for implementing n$^+$ polysilicon/SiO_x contact stacks in a wide array of solar cell architectures.

Currently transmission length method (TLM) is used for determining contact resistivity values for metal-polysilicon/SiO_x based layer stacks. For samples with only one conductive layer and one interface, 1D analytical TLM model is used. In this method, all the conductive layers, such as the heavily doped polysilicon layer, the diffused layer generated due to dopant in-diffusion during the annealing step, are considered as a single layer. Also, in this approach the influence of the interfaces are lumped together. Eidelloth and Brendel provide another approach to determine the contact resistivity values from the TLM data by utilising analytical expressions, taking into account the current flowing through the bulk [25].

Kokbudak et al. provide extensive work on the contact resistivity in polysilicon/-SiOx passivated contact utilising the analytical 2D method developed by Eidelloth and Brendel [26]. Still, in this method, the individual layers are lumped together

and the method does not take into account current flow at the edges of the metal contact, making it also unreliable [26].

As the contact stack involves resistance components arising from metal- polysilicon, polysilicon- SiO_x and the SiO_x-silicon substrate, the value generated using the 1D and 2D analytical method only provides a lumped value. In addition, in case the polysilicon layer is not structured such that the current flow is confined through the silicon substrate, the measured value contains components from the later current flow through the polysilicon layer as well.

A comprehensive attempt to understand the contact resistivity for the polysilicon based passivated contact was presented in the work of Gan et al. [27]. In the work from Gan et al. a value of less than 0.1 $m\Omega.cm^2$ for n and p-type polysilicon is presented. The samples in this work had a thermal interfacial oxide with thickness below 2 nm. The samples had ex-situ doping with an annealing step before doping. Another detailed study has been performed by Romer et al. in 2014 [28]. Combined contact resistance values of 12 $m\Omega.cm^2$ with a wet chemically grown oxide for aluminium-ITO-n^+polysilicon layer stack are presented by Romer et al. QSSPC measurements were used by Romer et al. to determine the overall sheet resistance of the samples inductively. Different interfacial oxides were used in this study. Rienacker et al utilises various TLM test structures with evaporated aluminium contacts to determine the junction resistivity [29]. The combined junction resistivity for n^+POLO junction is shown to be 0.6 $m\Omega.cm^2$. Work by Kokbudak et al. presents Quokka 3 simulation results of specific contact resitivity of 0.21 $m\Omega.cm^2$ for samples with n^+ polysilicon/SiO_x on n type silicon substrate [26]. Their simulation results show a specific contact resistivity of 0.11 $m\Omega.cm^2$ and 0.10 $m\Omega.cm^2$ for the interfaces between metal-polysilicon and polysilicon-bulk c-Si, respectively. Similar samples measured in this study by TLM method (four point) had values of 3.45 (1D analytical) and 1.39 (2D analytical) $m\Omega.cm^2$.

It is imperative to study in detail the contact resistivity specifically for our layer stacks and screen printed fire through silver contacts. As there does not exist dedicated literature on layer stacks similar to our layer, the below experiments are done to have a comprehensive study in understanding the contact resistivity for Ag-n^+ polysilicon layer/ SiO_x contact.

In this section we try to understand the critical factors which influence the contact resistivity of the n^+ polysilicon/ SiO_x-silver contact. The components we study in the first experiment are: the base resistivity, polarity of the wafer type (substrate) and the thickness of the interfacial oxide. Four different groups with; samples with no oxide, 1.4 nm wet chemical oxide (standard interfacial oxide), 47-nm thick thermal oxide and 186-nm thermal oxide are used. We use n and p-type wafers, with two base resistivities for each wafer type, 4.39 $\pm$ 0.02 Ω.cm (low base resistivity) and 21.6 $\pm$ 1.24 Ω.cm (high base resistivity) for n-type wafers. For the p-type wafers it is 0.72 $\pm$ 0.04 Ω.cm (low base resistivity) and 3.41 $\pm$ 0.03 Ω.cm (high base resistivity). We only use one fast firing peak temperature and 150 nm thick n^+polysilicon layer annealed at 825°C, for 30 min for all the samples. Paste G3a is used for these experiments. The symmetric samples were capped with a silicon nitride layer.

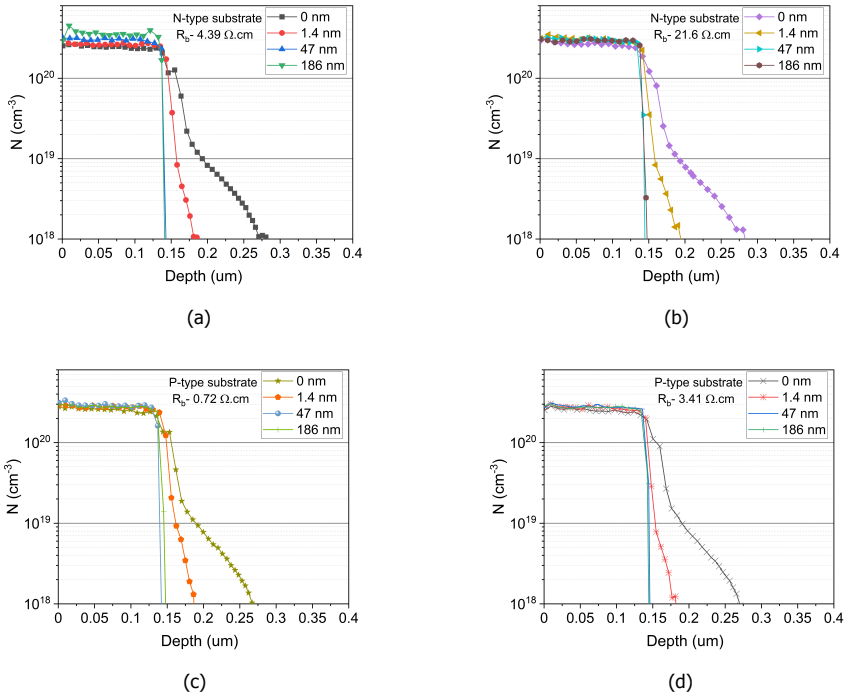


Figure 5.14: Doping profile for (a) N-type wafer with low base resistivity and (b) N-type wafer with high base resistivity (c) P-type wafer with low base resistivity and (d) P-type wafer with high base resistivity, the oxide thickness are mentioned in the plots.

The active doping profiles of the samples are shown in Figure 5.14. The active doping profiles shown in these figures can be divided into three categories:

1. Steep profile: For samples with 46 nm and 187-nm thick oxide, there is no in diffusion in the crystalline silicon.

2. Intermediate deep profile: The samples with 1.4-nm interfacial oxide, show phosphorus diffusion in the c-Si substrate, we call this as the doping tail.

3. Deep profile: Samples having no oxide layer, show a deep doping tail.

From the doping profile results presented in Figure 5.14, we can conclude that the active doping profiles are not dependent on the substrate type used. The implied open circuit voltage of the samples from different groups are presented in Figure 5.15.

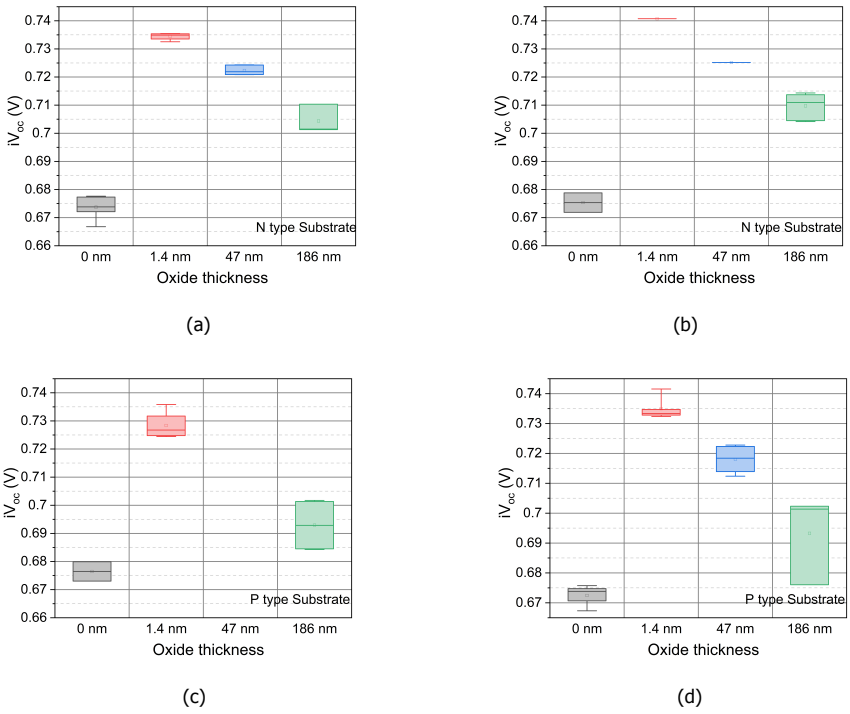


Figure 5.15: iV_{oc} for (a) N-type wafer with low base resistivity and (b) N-type wafer with high base resistivity (c) P-type wafer with low base resistivity and (d) P-type wafer with high base resistivity, the oxide thickness are mentioned in the plots.

The iV_{oc} values depend on the thickness of the interfacial oxide. Without any interfacial oxide, the values are below 680 mV for samples irrespective of the silicon substrate. For the samples which have no oxide, there are two reasons which lead to low passivation values. The first is the absence of surface passivation provided by the interfacial oxide, and the second is the increased Auger recombination coming from the deep doping tail in the c-Si substrate. The value increases to above 730 mV for the samples with the 1.4-nm interfacial oxide. One thing that is to be mentioned is that the thick oxides were thermal oxide. The type of oxide used has an effect on the passivation quality of the polysilicon/SiO_x based layer stack [30]. The values decreases when the interfacial oxide thickness is increased. We hypothesis that with the increase in the interfacial oxide the hydrogen migration to the c-Si-SiO_x interface is hampered and a high value of passivation is not obtained. We also consider that due to the increase in the oxide thickness the inversion layer created at the interface of oxide and silicon substrate is not adequate for achieving high level of passivation, and also no diffusion in c-Si wafer leads to reduced field effect passivation [30]. As there is no in-diffusion of phosphorus in the c-Si substrate (c.f. Figure 5.14) for the samples belonging to the groups with 46 nm and 187 nm thick interfacial oxide, it is clear that the change in the passivation comes from the oxide

thickness. Also the $J_{0\text{pass}}$ values support this conclusion. As an example, the mean $J_{0\text{pass}}$ value for the samples with high base resistivity n-type substrate and 47 and 186-nm thick interface oxide are, 5.8 ±0.1 and 15 ±4 fA.cm^{-2} respectively. For the samples high base resistivity n-type substrate and 1.4-nm thick interface oxide, the value is 1.2 ±0.01 fA.cm^{-2} and for 0-nm it is 64.5 ±11 fA.cm^{-2} Combining these results with the results presented in [31], where in it is shown that a deeper doping tail leads to decreased iV_{oc} values, it can be concluded that the iV_{oc} and $J_{0\text{pass}}$ values for n$^+$ polysilicon/SiO_x passivating contacts are dependent on the two factors; the interface oxide thickness, how deep the phosphorus diffusion is in the c-Si wafer (doping tail).

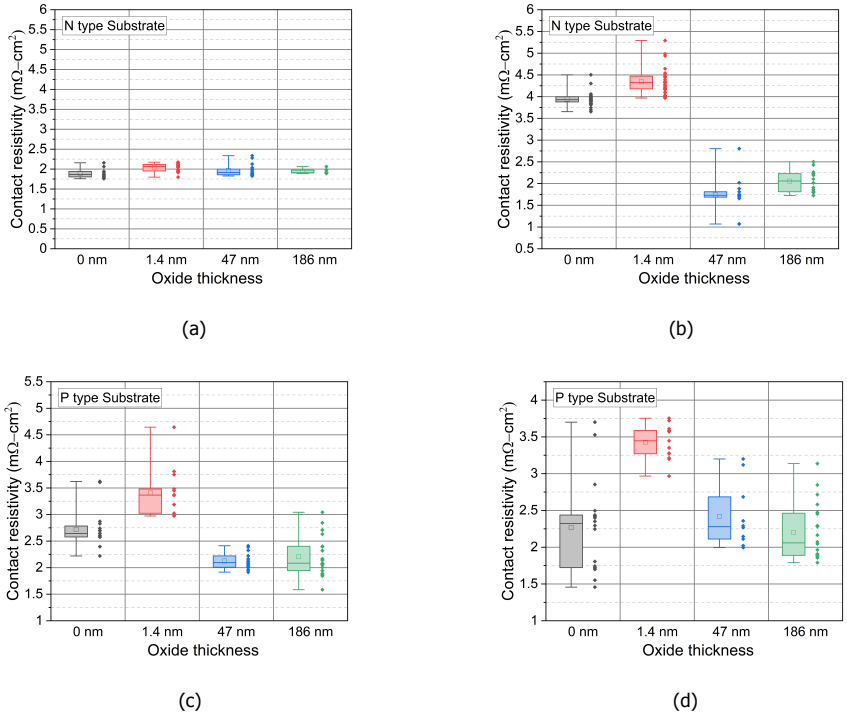


Figure 5.16: Contact resistivity for (a) N-type wafer with low base resistivity and (b) N-type wafer with high base resistivity (c) P-type wafer with low base resistivity and (d) P-type wafer with high base resistivity, the oxide thickness are mentioned in the plots.

The contact resistivity for the different groups is presented in Figure 5.16. From the results shown in Figure 5.16, it can be seen that there is no effect from the oxide thickness when a low base resistivity n-type substrate is used. For the other samples, the base resistivity does influence the measured contact resistivity, only when either there is no oxide or the 1.4-nm thin oxide. For the samples with thicker oxide (47 and 186-nm), majority of current flow is through the n$^+$polysilicon layer and hence the values are similar, even when a P type wafer is used. As there is no

influence of the wafer below the thick oxide. For majority of the groups, the mean values remain around 2 mΩ.cm^2, which are excellent values of contact resitivity [21, 32]. When the p-type substrate is used, the contact resistivity values become independent of the base resistivity of the wafers used, as now the current flow is majorly through the polysilicon layer. The measured values for the samples with 1.4-nm thick interface oxide are higher as compared to the other groups, as we think there is a flow of current through the in-diffused phosphorus region (doping tail) in the wafer. The other groups with p-type substrate show similar values as with n-type wafers except for the samples with the high base resistivity substrate and the 0 and 1.4-nm interfacial oxide. Hence, the effect of the wafer type is present, this could be also due to the fact that the base resistivity of the high base resistivity n-type wafer (21.6 $\pm$ 1.24 Ω.cm) for the groups with 0 and 1.4-nm is almost 5 times as compared to other wafers.

From the measured values of the different groups, we conclude that the n$^+$ polysilicon layer to metal contact resistivity is not dominating the obtained contact resistivity values from the TLM measurements. It is the cumulative effect coming from the resistances from the oxide and the wafer that defines the measured values.

5.5.1. Structured Ag-n$^+$ polysilicon/SiO_x contact for contact resistivity measurement

To further understand the components of the lumped contact resistivity values (can also be called as effective/apparent contact resistivity) i.e. the resistance values coming from the interfacial oxide and the wafer, we performed another experiment. In this experiment, we took n-type wafers, but processed them in a different way as compared to our previous symmetrical samples. After growing the interfacial oxide, LPCVD based n$^+$ polysilicon layer was deposited. A layer of almost 180 nm was deposited. After this, the samples were oxidised and a thermal oxide was grown on the polysilicon layer. This consumed the polysilicon layer, thus the overall thickness of polysilicon was reduced to 150 nm. Afterwards a laser step was performed to ablate the thermal oxide. Afterwards the polysilicon without the silicon oxide capping layer was etched of by a chemical dip in NaOH solution. The thermal oxide was removed by a dip in HF solution. This led to formation of regions which had polysilicon layer but with gaps in between. A schematic of the sample structure is shown in Figure 5.17.

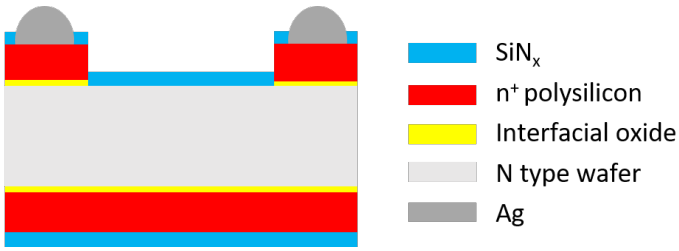


Figure 5.17: Schematic of the structure with selective n$^+$polysilicon/ SiO_x-silver contact. It is important to mention that the rear side also has the same n$^+$ polysilicon/SiO_x and SiN_x stack.

The metal print was done in a way that the silver finger lies on top of the n$^+$ polysilicon/SiO_x stack. Using the laser ablation we varied the width of the n$^+$ polysilicon/ SiO_x stack. We also varied the set fast firing peak temperatures to 760, 775 and 790°C at a constant belt speed of 3 m.min^{-1}.

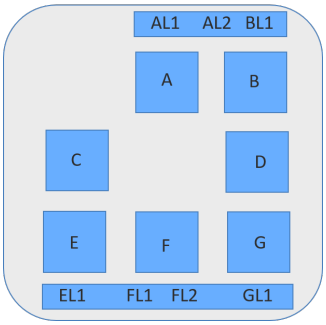


Figure 5.18: Schematic of the print pattern used, with the different fields marked.

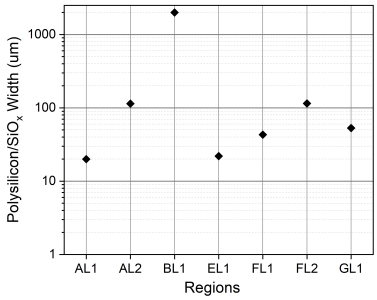


Figure 5.19: Mean value of oxide/polysilicon width measured using LSM images.

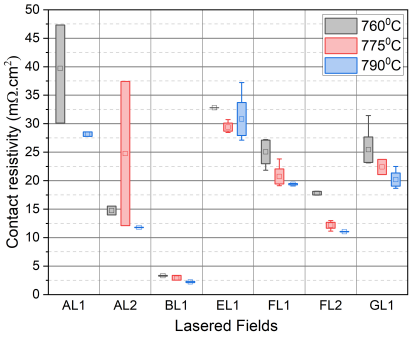


Figure 5.20: Contact resistivity for the different lasered fields.

The Figure 5.18 shows the print scheme and the different regions of the lasered areas. The naming nomenclature is used to denote areas with different width of the n^+ polysilicon/SiO_x stack. The fields AL1, AL2, BL1, EL1, FL1, FL2 and GL1 are the regions used for contact resistivity measurements. BL1 is the region which has the standard dimensions i.e 1 cm width with 2 mm finger distance. The squares are for the computation of J_{0met}, which is explained in the later section.

The Figure 5.19 shows the mean values of the width of polysilicon /SiO_x stack with respect to the different regions. The results for the samples with respect to the different regions and the peak fast firing temperature are presented in Figure 5.20.

From the results it can be observed that the apparent contact resistivity values are dependent on the polysilicon/SiO_x underlying layer width. The measured apparent contact resistivity values are the maximum for the regions with the lowest polysilicon/SiO_x width. The regions AL1 and EL1 have the lowest width of polysilicon/SiO_x underlying layers, they show the highest values. Although one thing to be pointed out here should be that the silver fingers are wider and hence they also directly connect with the n type wafer. The region BL1, which has the highest width shows the minimum values. This is not the case when the polysilicon/SiO_x width is reduced as a large component of current is forced to flow via the crystalline silicon. This effect will have implications when selective polysilicon fingers are utilised, where the polysilicon/SiO_x oxide stack is not on the full area of the sample.

We conclude that the effect of the polysilicon/SiO_x width is a major factor in the lumped contact resistivity measurements as the silicon oxide resistance is dominating. More work is needed to further differentiate the contributions from the interfaces to the experimentally measured lumped contact resistivity.

5.6. Conclusion

Different generations of fire-through silver paste were used to metallise n^+ polysilicon/ SiO_x based symmetrical samples. The passivation quality of the samples was also monitored, and our layer stack provides a high level of passivation. It does not deteriorate after fast firing in the investigated range of fast-firing peak temperatures. Excellent J_{0met} values below 50 fA.cm^{-2} coupled with ρ_c values below 2 mΩ.cm^2 were obtained for a number of samples fast fired at peak temperatures below 805 °C. To the best of our knowledge the values obtained for Paste G3a are the lowest obtained for J_{0met} and ρ_c. With the values we consider our contact architecture as a fully passivated contact.

The SEM images proved instrumental in explaining the trend in the J_{0met} values in response to the fast-firing peak temperature. A Python based script was developed and used to identify and quantify density of holes in the n^+ polysilicon layer as visible in the SEM images. The result obtained from the script fit well with the experimental results and the observations. The print quality is also studied and an appropriate value (0.32) of aspect ratio is obtained for Paste G3a. The measured contact resistivity values for the n^+ polysilicon/SiO_x contact stack are understood by

using different base resistivity and different polarity wafers. Utilising a structured layer stack furthered the understanding on the contribution of the different layers in the n^+ polysilicon/SiO_x contact stack's measured contact resistivity (lumped/ apparent contact resistivity). The study points out that silicon oxide resistance is the dominating factor in the contact resistivity measurements by TLM.

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6

Comparison with contacts on diffused layers

Be near science and technology, and you will never fail.

Arunachalam Muruganantham

In this chapter, the differences between phosphorus diffused contacts and n^+ polysilicon/ SiO_x contacts are studied in details. The passivation quality and the contact properties are the two aspects we have examined in detail.

This chapter is based on the following publication :

- *A. Chaudhary, J. Hoß, J. Lossen, F. Huster, R. van Swaaij, and M. Zeman, Screen printed fire-through contact formation for Polysilicon Passivated Contacts and Phosphorus Diffused Contacts, IEEE Journal of Photovoltaics,12(2),462-468 (2022).*

6.1. Introduction

The development of metal pastes is important for improving the performance of silicon based solar cells. Therefore it is essential to understand how the metallisation of the n^+ polysilicon/SiO_x-based passivating contact differs from that of a phosphorus-doped silicon contact. In this chapter, a detailed and systematic study to understand the contacting of the n^+ polysilicon-based-passivated-layer stack and phosphorus doped silicon layer is presented. In order to study the metallisation with fire through silver paste we utilised our stacks consisting of a 150-nm thick n^+ polysilicon layer, and a standard phosphorus-doped silicon surface (not a polysilicon layer) with a thickness of approximately 450-nm.

Four properties are detailed and compared in this chapter:

- Passivation quality (iV_{oc} and $J_{0\mathrm{pass}}$)
- $J_{0\mathrm{met}}$
- Contact resistivity (ρ_c)
- Surface morphology and features of the Ag-glass-silicon interface

6.2. Experimental design and sample preparation

Two sets of symmetrical samples were utilised in this study. Sample A refers to layer stacks of 150-nm thick n^+ polysilicon on top of a thin interfacial oxide layer. Sample B refers to structures consisting of a phosphorus diffused layer.

We used standard M2 n-type solar-grade Czochralski wafers (CZ) with a nominal thickness of 180 $\pm$ 10 µm and a base resistivity of 1.6 $\pm$ 0.3 Ω.cm. The wafers were immersed in a 22% NaOH solution for about 500 sec to remove the saw damage. After this, an approximately 1.4 nm thick interfacial oxide was grown wet chemically (nitric acid oxidation of silicon (NAOS)) on the wafers. This was followed by deposition of in-situ phosphorous doped silicon layers with a thickness of 150 nm by Low Pressure Chemical Vapor Deposition (LPCVD) at a temperature of 580°C. To form polysilicon layers by solid-phase crystallization, the samples were annealed at 825°C for 30 minutes. A schematic cross-section of a symmetric n^+ polysilicon/SiO_x sample is shown in Figure 6.1.

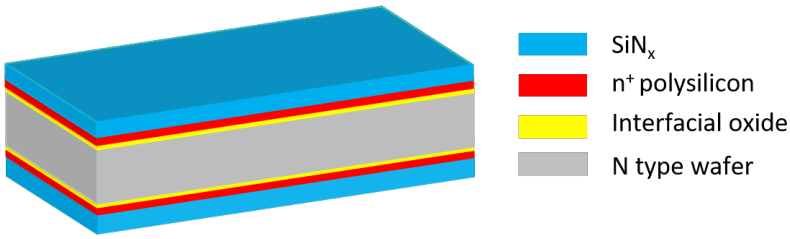


Figure 6.1: Schematic cross-section of the sample A used in this work.

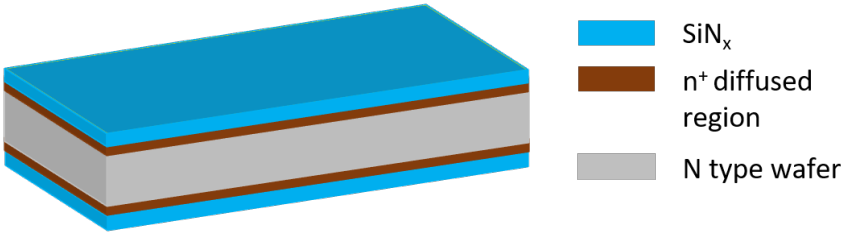


Figure 6.2: Schematic cross-section of the sample B used in this work.

For sample type B, we also used M2 n-type CZ silicon wafers (thickness= 180 ± 10 µm, base resistivity = 1 ± 0.2 Ω.cm), which were also saw damage etched in NaOH solution. The difference in base resistivity between sample types A and B was unintentional. Using a diffusion tube an n^+-doped region was created with $POCl_3$ gas. This resulted in a doped layer of approximately 450-nm and a sheet resistance of 150 Ω/□. The phosphate silicate glass after the doping step was completely removed before silicon nitride deposition. A schematic cross-section of the sample is shown in Figure 6.2.

On both sample types later a silicon nitride layer with a thickness of ≈ 80 nm was deposited by PECVD on both sides of the wafers. An identical fire-through silver paste (Paste-G2a) was used for contacting the two types of samples. The fast firing was done in our Centrotherm fast firing furnace. In this experiment, we varied the set point for the zone with the highest temperature, hereafter referred to as fast-firing peak temperature, from 760 °C to 820 °C in steps of 15 °C. The belt speed was kept constant at 3 $m.min^{-1}$ throughout. We also took SEM images: top view and cross-sectional images. To view the metal-semiconductor interface, we took cross-sectional SEM images after milling the metallised fingers. This was done without any further chemical treatment. A free open source software (ImageJ) was utilised to measure the dimensions of the silver crystallites which build in the polysilicon layer.

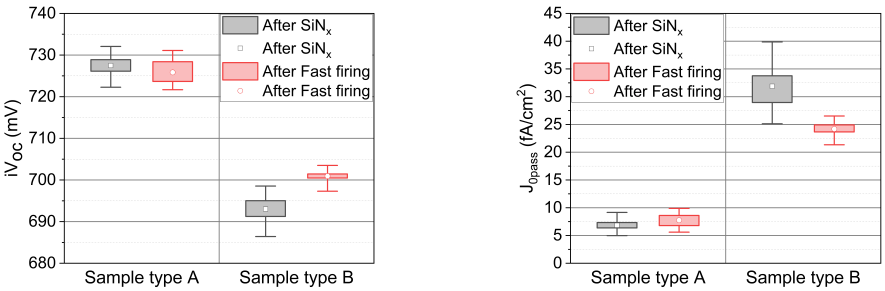
6.3. Results and discussion

6.3.1. Passivation quality in non metallised areas

Figure 6.3, shows the implied open circuit voltage iV_{oc} and the recombination current density in the doped regions J_{0pass}. The iV_{oc} after SiN_x deposition shows that the polysilicon based samples have substantially higher passivation quality. The average iV_{oc} for these samples is almost 32 mV higher as compared to the phosphorus diffused samples. Similarly, the J_{0pass} value was almost 25 $fA.cm^{-2}$ less. This result is associated to the high level of passivation from the interfacial oxide as well as the field-effect passivation from the highly doped polysilicon layer.

After fast firing, the results for the iV_{oc} of the samples are also shown in Figure 5. The fast firing process did not lead to a change of the passivation quality of Sample type A. For Sample type B, fast firing led to an increase in iV_{oc}. Still, the samples with interfacial oxide and n^+ polysilicon have higher iV_{oc} as compared to

the phosphorus doped samples after fast firing.



(a) (b)

Figure 6.3: (a) The implied open-circuit voltage (iV_{oc}). (b) The $J_{0\mathrm{pass}}$ values for 25 samples each for sample type A and B.

6.3.2. Metallisation

Herein, we present iV_{oc} calibrated PL images for the two types of samples fast-fired at the peak temperature of 820 and 760°C in Figure 6.4. The metallised areas appear dark as compared to the unmetallised areas of the samples. The difference between the iV_{oc} in metallised patches and the unmetallised patches is due to the additional recombination coming from the metal semiconductor interface as seen in Figure 6.4a. Going to lower fast firing temperature of 760°C the iV_{oc} drop between the metallised and unmetallised patches becomes negligible for Sample type A as shown in Figure 6.4b. This is a fully passivated contact, as irrespective of the metallisation and metal fraction, there is no drop in the iV_{oc} after metallisation. For Sample type B a drop in iV_{oc} in the metallised patches is present as seen from the dark areas in Figure 6.4c and 6.4d.

Utilising these iV_{oc} calibrated PL images, $J_{0\mathrm{met}}$ values were extracted, as presented in Figure 6.5. In the plot, we have shown the uncertainty arising from the inhomogeneity in individual samples due to processing steps, as well as the uncertainty in the extracted values (generated in response to the line fitting in the J_{01} Vs metal fraction) for the 4-5 samples in a group, as explained in Chapter 4.

The $J_{0\mathrm{met}}$ values for Sample type B are higher in the investigated range of fast firing peak temperature. A small increase in the mean value of $J_{0\mathrm{met}}$ occurs when the fast-firing peak temperature is increased from 760°C to 820°C. Although these values are high as compared to sample type A, they are still comparable and lower to state of art values reported for samples with similar kind of phosphorus emitters [1–3]. This could be because of the silver paste (Paste-G2a), which is used for the shallow contacting. As for Sample type A, we obtained $J_{0\mathrm{met}}$ of the order of J_{01}, for fast firing peak temperatures below 820°C, as shown in the plot with the values going to zero. Even the $J_{0\mathrm{met}}$ of samples fired at 820°C, is below 200 fA.cm^{-2}, which is almost three times smaller than that for comparable samples of type B. Because the $J_{0\mathrm{met}}$ is of the order of J_{01}, the samples fast fired with peak temperatures below

820°C, with polysilicon/SiO_x layer stack can be called nearly perfectly passivated contacts.

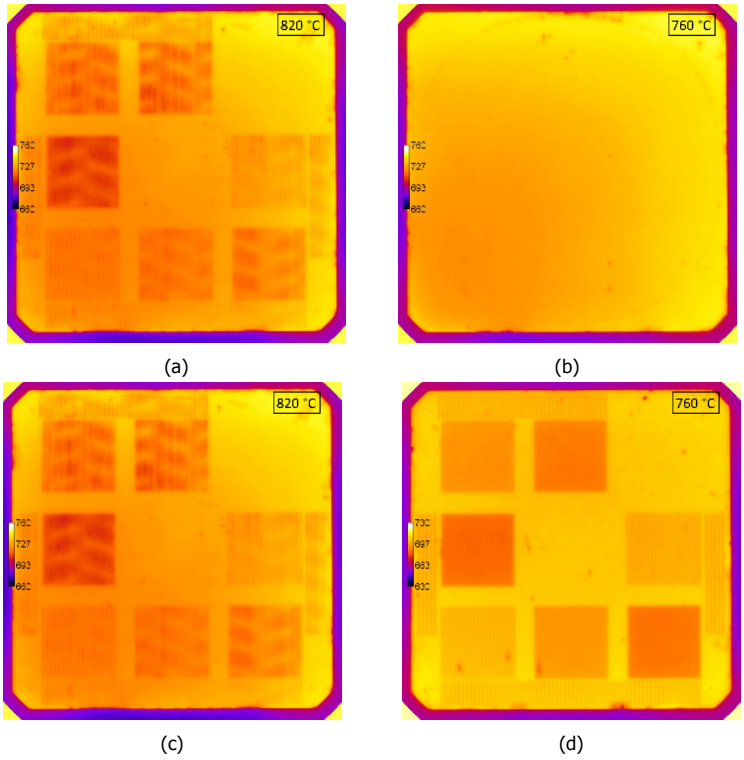


Figure 6.4: iV_{oc} calibrated PL images for (a) Sample type A (150-nm n^+ polysilicon) fast fired at peak temperature of 820 and (b) 760°C (c) Sample type B (phosphorus diffused c-Si) fast fired at peak temperature of 820 and (d) 760°C

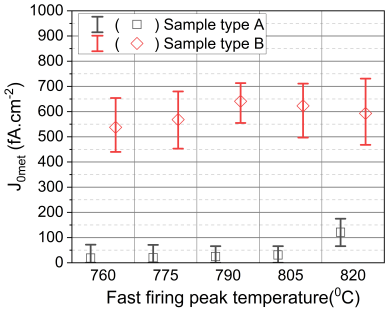


Figure 6.5: $J_{0\mathrm{met}}$ values for the sample type A and B fired at different fast-firing peak temperatures.

The contact resistivity values are presented in Figure 6.6, the mean values remain below 2 mΩ.cm^2 for sample type A for a large range of fast firing peak temperatures. The values for sample type B are higher, and they increase with the reduction in fast firing peak temperature, going to greater than 50 mΩ.cm^2, for fast firing peak temperature of 760°C. This means that optimum contact is not formed if we reduce the fast firing peak temperature. To understand the contact microstructure for the two sets of sample, we took cross-sectional SEM images.

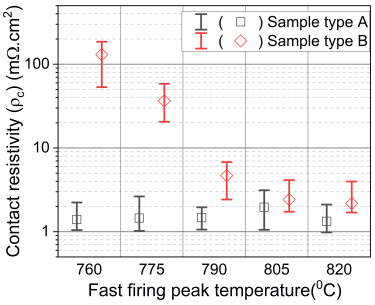


Figure 6.6: ρ_c values for the sample type A and B fired at different fast firing peak temperature.

In Figure 6.7, the cross-sectional SEM images for Sample type A (150-nm n$^+$ polysilicon) and B (phosphorus diffused c-Si) fast fired at the peak temperature of 760°C, 790°C and 820°C are presented. We have marked the different components in the images, the bulk silver, glass layer, silver crystallites. From the images of Sample type A, we can conclude that as the fast firing peak temperature is increased, the number and size of the silver crystallites in contact with the polysilicon layer starts to increase. This could be the reason for the increase in $J_{0\text{met}}$ value when the fast firing peak temperature is increased. As a higher thermal budget is favorable to increase the crystallization of silver, it leads to more sites where silver is in contact with the polysilicon layer. Still, the number of crystallites at 760°C is enough to provide good electrical conductivity (mean $\rho_c \leq 2$ mΩ.cm^2).

For Sample type B, cross-sectional images are also presented in Figure 6.7. At 760°C there is almost no silver crystallite penetrating the diffused layer. This corresponds to a situation where the contact resistivity goes above 50 mΩ.cm^2. Increasing the fast firing peak temperature from 760 to 820°C, leads to an increase in the size of the crystallites as seen in the cross-sectional images. Although the silver crystallites are not as big as seen in the case of sample A, still at 820°C, the mean contact resistivity value for Sample B is close to 2 mΩ.cm^2.

In the samples fired at 820°C, we marked the length of the silver crystallites penetrating the silicon layer in the samples using an open-source image processing software. For better visualization, we marked the 150-nm nominally thick polysilicon layer with a dashed line.

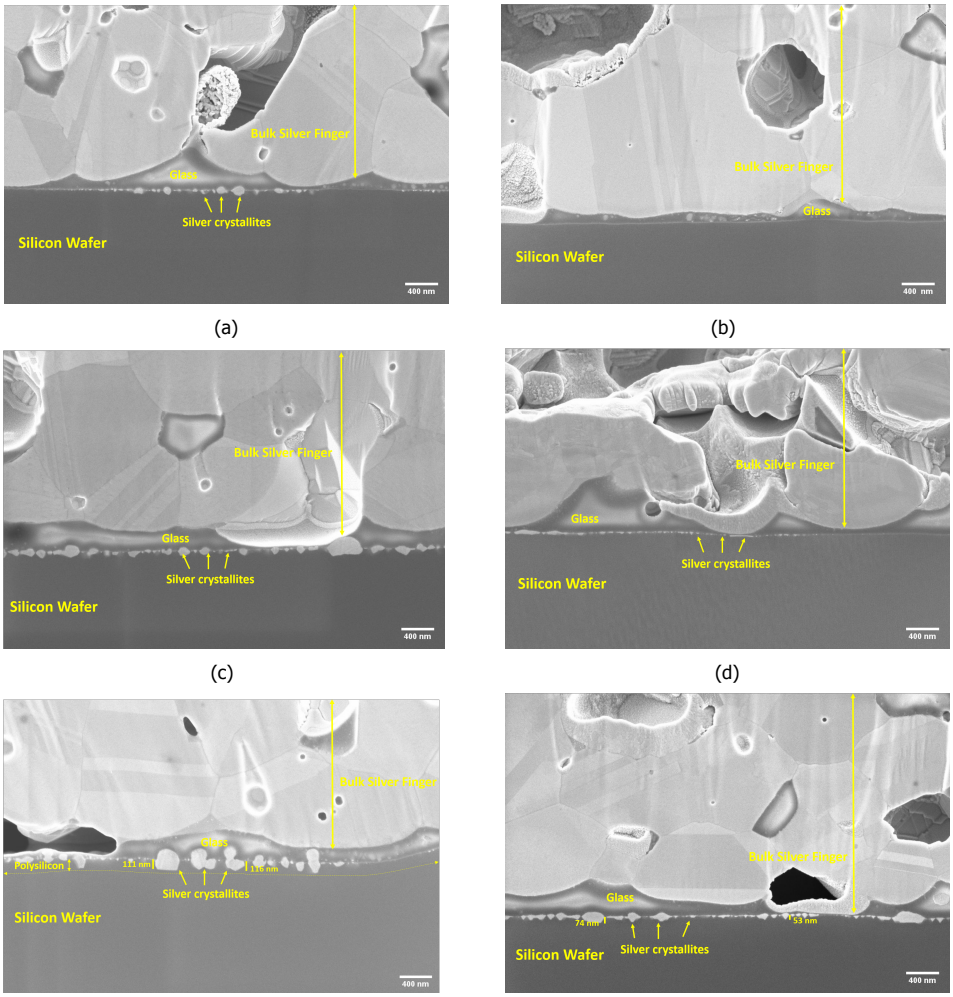


Figure 6.7: Cross-sectional SEM images for sample type A and B fast fired at peak temperature of (a), (b) at 760, (c), (d) at 790 and (e), (f) at 820°C.

For Sample Type B, the silver crystallites are not as deep ($\leqslant$ 100-nm) as compared to those for Sample type A. This makes it clear that the polysilicon layer favors the formation of deeper crystallites as compared to diffused surface even at the same fast firing peak temperature. One of the reasons for the increased size of the silver crystallites can be attributed to the low sheet resistance in Sample type A. This is assuming that the change in sheet resistance leads to a change in the surface doping concentration, which in turn influences the silver crystal formation [4]. In Figure 6.8, we present doping profiles for the Sample type A and B, fast fired at peak temperature of 820°C. There is a difference of magnitude in active

phosphorus (surface doping) in the two types of samples. Another reason that can be behind the higher crystallization in polysilicon is the higher oxidation rate of polysilicon as compared to crystalline silicon (<100>) [5]. A higher oxidation rate leads to higher reduction rate of silver oxide, enhancing the deposition of silver [6, 7]. Another reason we think could be the presence of silicon grains in the polysilicon layers which could facilitate the silver crystallite formation as compared to crystalline silicon.

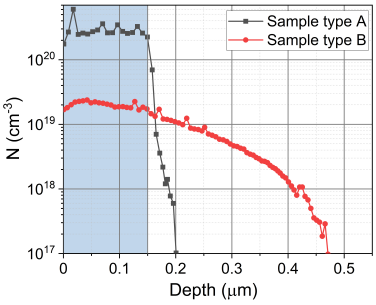
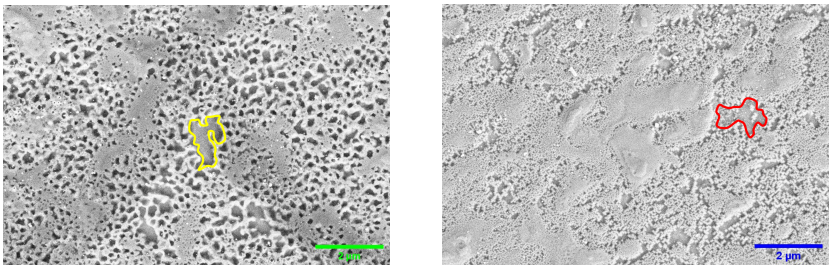


Figure 6.8: Doping profile for the sample type A and B fired at fast firing peak temperature of 820°C.



(a) (b)

Figure 6.9: Top view SEM images of (a) Sample type A and (b) Sample type B, fast fired at peak temperature of 820°C.

We further investigated the samples and took SEM images after removing the bulk silver, glass layer and silver crystallites as explained in Chapter 4. In Figure 6.9a, the top view (exemplary area) for Sample type A and B are presented; these samples were fast-fired at the peak temperature of 820 °C.

In the image in Figure 6.9a, we have marked a region where the damage to the polysilicon has happened with a yellow boundary. This kind of damage to the polysilicon layer by the silver paste constituents has also been observed previously [8, 9]. From the results of $J_{0\mathrm{met}}$ presented in Figure 6.5, we conclude that this damage to the polysilicon does not lead to an excessively high $J_{0\mathrm{met}}$ (> 200 fA.cm^{-2}). Similarly, in Figure 6.9b, as an example, we also marked damage (holes) to the

silicon wafer with a red boundary. This damage to the crystalline silicon wafer is detrimental, leading to high values of $J_{0\mathrm{met}}$. For Sample type B, we observe that when the fast firing temperature is increased or decreased the $J_{0\mathrm{met}}$ remains similar. This is unexpected as from the contact resistivity measurements and the cross-sectional SEM we expected to have low values of $J_{0\mathrm{met}}$ at low fast firing temperature, as there are almost no silver crystallites in contact with the silicon layer. We also took SEM images for samples fired at lower fast firing peak temperature. We found out that the damage to silicon decreases (pits/cavities and etched surfaces), but still for Sample type B, the damage is enough to lead to higher $J_{0\mathrm{met}}$ values as compared to that for Sample type A. As an example in Figure 6.10, we present top-view SEM image for Sample type B fast fired at peak temperature of 790 °C. Here also the damage to the crystalline silicon is visible. An example of it is marked with a red boundary. This means that the damage to the silicon layer in the case of Sample type B is detrimental to the $J_{0\mathrm{met}}$ value. We suggest that in addition to the damage caused to the diffused layer, the etching of silicon nitride passivation layer by the paste constituents is also an additional contributor. These two factors lead to a reduction of the passivation quality of the layers, which translates, into a high value of $J_{0\mathrm{met}}$.

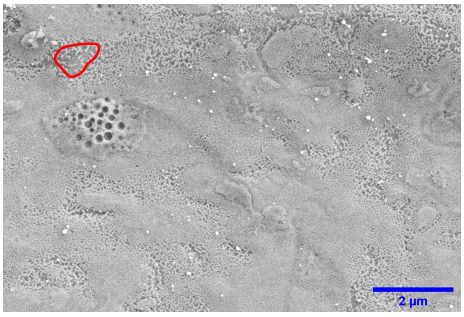


Figure 6.10: Top view SEM images of Sample type B fast fired at peak temperature of 790°C.

To investigate the influence of silicon nitride passivation layer etching on the high $J_{0\mathrm{met}}$ for sample type B, we completely etched the silicon nitride layer on unmetallised areas of the fast fired samples in a 2% HF solution and then performed the QSSPC measurements. From the measurements, an absolute drop of 7-12 mV in iV_{oc} is present for sample type A. The drop in iV_{oc} for sample type B is 110-112 mV. This large drop for sample type B, comes from the reduced surface passivation owing to the absence of the silicon nitride passivation layer. While for sample type A, passivation is dominated by the interfacial oxide and polysilicon, hence a smaller drop. It might be argued, that no loss should appear, as the SiN_x-silicon interface is replaced by an SiO_x-silicon interface constituted by the glass layer visible in the SEM. However, a molten and recrystallized glass, potentially induces a lot of surface tension/stress, and can not be suspected to passivate as well, as a chemically or thermally grown SiO_x layer.Further the glass contains dissolved silver oxide and lead, hence it does not have a similar glass morphology as the silicon oxide used

for passivation. Still the the removal of silicon nitride layer for the diffused samples is factor and adds to higher recombination after metallisation.

6.4. Conclusion

The passivation quality achieved with n^+ polysilicon layers with an interfacial oxide is superior as compared to samples with a phosphorus diffused layer. Metal silicon recombination current density and the contact resistivity values were compared and the polysilicon based contacts outperform the phosphorus diffused samples. Excellent values ($J_{0\mathrm{met}} \approxeq J_{01}$ and $\rho_c \leq 2$ mΩ.cm^2) are obtained for polysilicon based samples. Presence of a larger number and bigger size of silver crystallites is observed in the cross-sectional SEM images for samples with a polysilicon layer as compared to samples with a phosphorus diffused sample fast fired at the same peak temperature. The polysilicon layer favors formation of deeper, larger and more silver crystallites as compared to phosphorus doped layers. This is thought to be because of higher surface doping and higher oxidation rate, as well as the presence of silicon grains for polysilicon layer as compared to crystalline silicon. The damage to the crystalline silicon wafer during the metallisation in the case of phosphorus diffused samples is very critical because the concentration of minority carriers is still high at this surface, while for the passivating contact, the concentration of minority carriers is effectively suppressed at the depth were the metal crystallites are found (Same is true for the surfaces, where the SiN_x passivation is etched away). This in addition to the damage to the silicon nitride passivation layer is the reason for higher $J_{0\mathrm{met}}$ for sample type B.

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7

Influence of polysilicon layer thickness on metallisation

Solar energy is bound to be in our future.
There's a kind of inevitability about it.

Jim Inhofe

This chapter investigates how the thickness of the polysilicon layer and the peak temperature during contact sintering influences the properties of n^+ polysilicon/ SiO_x passivated contacts. Samples with three different n^+ polysilicon layer thicknesses of 50, 100 and 150-nm are considered in this work.

This chapter is based on the following publication:

- *A. Chaudhary, J. Hoß, J. Lossen, F. Huster, R. Kopecek, R. van Swaaij, and M. Zeman, Influence of polysilicon thickness on properties of screen-printed silver paste metallized silicon oxide/polysilicon passivated contacts, physica status solidi (a) , 2100243 (2021).*

7.1. Introduction

Understanding the influence of the polysilicon-layer thickness on the passivating quality (iV_{oc} and J_{0pass}) and contact properties is of great importance for several reasons. On one hand, reducing the thickness yields a reduction of parasitic absorption in the polysilicon layer [1–4] thus increasing the short-circuit current density and hence the conversion efficiency of the respective solar cell [5, 6]. On the other hand, a low recombination current density and a low contact resistivity of the contact should be maintained for the thinner polysilicon layer in order not to compromise passivation, and hence the open-circuit voltage and the fill factor of the solar cell. Another advantage of using a thinner polysilicon layer is the reduced deposition time, which makes the process for industrial production more cost effective.

This chapter shows how the contact properties (metal-polysilicon recombination and contact resistivity) depend on the polysilicon layer thickness and the contact sintering temperatures. A wide temperature range is explored for this purpose. Photoluminescence (PL) images are also presented to show the transition to a passivated contact with J_{0met} of the order of J_{01}. In addition, the top view SEM images and the cross-sectional SEM images of different samples are presented to illustrate how recombination and contact resistivity are influenced by silver crystallite growth within the polysilicon layer.

Work from Stodolny et al. presents a metal semiconductor recombination current density (J_{0met}) value of 100-200 fA.cm^{-2} for a 100 - 200 nm thick ex-situ n$^+$ doped LPCVD polysilicon layers [7]. A study on the screen printed metallization with fire through silver pastes of ex-situ doped polysilicon on top of a thermal oxide with a textured wafer surface was presented in the work of Ciftpinar et al.. They obtained a contact recombination value of 400 fA.cm^{-2} (calculated from V_{oc} measurements on their polysilicon cell structures), with a contact resistivity value above 4 mΩ.cm^2 for a 200 nm thick n$^+$ polysilicon layer samples [8]. In this work, they utilize two different approaches to compute the contact recombination value. One wherein the Quokka generated PL images are fitted to the experimentally obtained PL images, with the contact recombination as the variable. The other approach uses metallization of cell structures and then utilizes the V_{oc} values to get the contact recombination.

A contact resistivity of 2.7 mΩ.cm^2 is presented for an 80-150 nm thick n$^+$ LPCVD deposited polysilicon, with screen printing of a fire-through silver paste in the work of Chang et al [9]. Papers from Padhamnath et al. from SERIS also show excellent J_{0met} value below 50 fA.cm^{-2} with excellent contact resistivity below 2 mΩ.cm^2 for ex-situ doped LPCVD deposited polysilicon layers on top of a thin thermal oxide [5, 10]. The J_{0met} values in this work were generated from their in-house developed software. This requires contact resistivity, sheet resistance and the photoluminescence images of screen printed metallised samples as input to the software. Recent study by Padhamnath et al. [11] detailing the impact of firing temperature on metallisation for an $\approx$ 150-nm thick n$^+$ doped polysilicon layer shows the variation in contact resistivity and metal-semiconductor recombination current density (J_{0met}) with the fast-firing peak temperature. The polysilicon layers

used in their work are exsitu doped and have a thermal oxide below them. In their study they detail the impact of glass layer thickness and the density of silver crystallites on the contact resistivity with respect to the fast-firing peak temperature. Their method of computation of $J_{0\text{met}}$ utilises a combination of photoluminescence (PL) images and a finite element simulator, Griddler. Excellent results are shown in this study, still this study differs from the layer stacks and the methodology used in our work. The group at Trina Solar also shows a $J_{0\text{met}}$ of 50 fA.cm^{-2} for their thick polysilicon (≈ 300-nm) ex-situ doped LPCVD deposited polysilicon layer [1].

7.2. Experimental design and sample preparation

Three different polysilicon thicknesses of 50, 100, 150-nm have been used for the experiments presented in this chapter. The iV_{oc} and $J_{0\text{pass}}$ of the n$^+$ polysilicon/SiO$_x$ layer stack samples was monitored before and after metallisation by QSSPC measurements. Photoluminescence imaging was used to observe the impact of metallisation on passivation quality. Further, we used Scanning Electron Microscope (SEM) imaging to investigate the micro-structures at the interface of silver paste and polysilicon layer. Symmetric samples with an n$^+$ polysilicon layer on top of a thin interface oxide layer were deposited on standard M2 n-type solar grade Czochralski wafers (CZ) with a nominal thickness of 180 $\pm$ 10 µm and base resistivity of 1 $\pm$ 0.2 Ω.cm. The wafers were etched to remove the saw damage in NaOH solution before growing an approximately 1.4-nm thick interfacial oxide in nitric acid (NAOS) at room temperature. In-situ phosphorous doped silicon layers were deposited by Low Pressure Chemical Vapor Deposition (LPCVD) in our Centrotherm quartz tube furnace from a gas mixture of Silane and Phosphine at a temperature of 580°C. In order to obtain different thicknesses for the polysilicon layers, we adjusted the deposition time during the LPCVD deposition step.

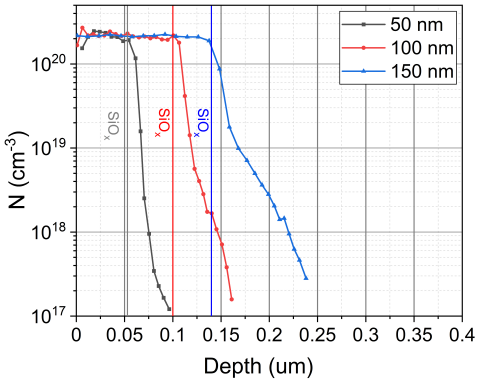


Figure 7.1: Doping profiles for samples with 50, 100, 150-nm thick n$^+$ polysilicon layer used in the work measure by ECV profiling.

All layers were annealed at 825°C for 30 minutes in the Centrotherm quartz

tube furnace to form polysilicon layers by solid-phase crystallization. SiN_x layers with a thickness of ≈ 80 nm were deposited on both sides of the samples. The doping profiles for representative samples with different polysilicon thickness are shown in Figure 7.1. The sharp drop in the active dopant concentration relates to the presence of interfacial oxide at that point. This point depends on the polysilicon layer thickness in the sample.

The thickness of the polysilicon layers was measured using spectroscopic ellipsometry with a SENTECH SE 800-PV tool. For accurate measurement of the polysilicon thickness, we prepared special test samples with a thick thermal oxide (≈ 187 nm) below the polysilicon layer to facilitate ellipsometer model fitting.

The samples were screen printed using the fire-through silver Paste G3a. We tested and compared this paste to other available silver pastes as presented in Chapter 5, and found that a contact made using this paste has lower metal-polysilicon recombination current density and maintains appreciably good contact resistivity compared with other silver pastes in our inventory. Contact formation was performed in the 8.6 m fast-firing belt furnace. In this experiment, we varied the set point for the zone with the highest temperature, hereafter referred to as fast-firing peak temperature, from 700°C to 820°C in steps of 15 °C, as it is known from our previous work that temperatures below 800°C can substantially reduce the $J_{0\mathrm{met}}$. We explored a large temperature range in this experiment to understand the effect of the fast-firing peak temperature on the different thickness polysilicon layers. The belt speed in this experiment was kept constant at 3000 mm.min^{-1}.

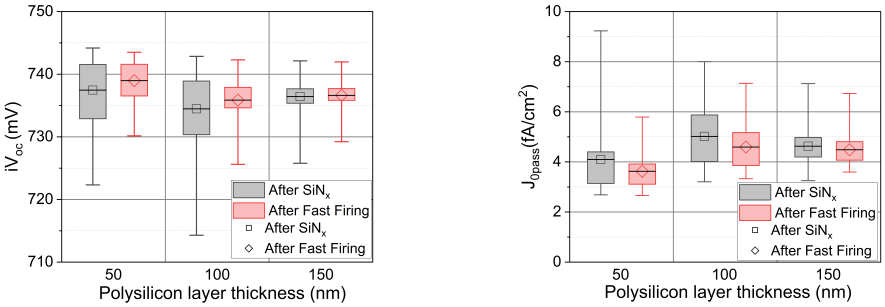
7

7.3. Results and discussion

7.3.1. Passivation Quality in non-metallised areas

To compare the passivation quality of samples with different polysilicon thickness, the iV_{oc} and the $J_{0\mathrm{pass}}$ after SiN_x deposition were measured. The results are presented in Figure 7.2. As the samples used are symmetrical, we show $J_{0\mathrm{pass}}$ per side. From this figure, we conclude that the thickness of the polysilicon layer has no significant influence on the passivation quality in the non-metallised areas in the range from 50 to 150 nm. This is expected since these layers have a thickness greater than the Debye length, which is a few nanometers in highly doped silicon [12]. Hence the effect of polysilicon thickness on the passivation is not significant as also shown in literature [5, 8, 13]. These samples were later on used for the metallisation and fast-firing experiment. The majority of the samples achieve appreciable passivation quality with the best sample achieving an iV_{oc} of 744 mV and $J_{0\mathrm{pass}}$ of 2.7 fA.cm^{-2}.

The plots in Figure 7.2 show the iV_{oc} and the $J_{0\mathrm{pass}}$ of these samples after metallisation and fast firing (marked as After Fast Firing in the plot). The QSSPC lifetime measurements were performed in the non-metallised area of the sample. We can conclude from these plots that the print, drying processes and the fast firing process did not lead to an adverse affect on the passivation in the non-metallised part of the wafer.



(a) (b)

Figure 7.2: (a)iV_{oc} and (b)$J_{0\mathrm{pass}}$ values, with different polysilicon-layer thickness, after SiN$_x$ and after fast-firing..

7.3.2. Metallisation

In order to investigate, the dependence of metal polysilicon recombination on the fast-firing peak temperature, we present representative PL images for selected samples with 100-nm thick polysilicon layers in Figure 7.3. This figure shows the PL images with identical exposure time and intensity for samples with fast-firing peak temperature ranging from 820 to 700°C. The 100-nm thick polysilicon layer samples are taken as an example to show how the PL signal from the metallised parts approaches that from the non-metallised parts when reducing the fast-firing peak temperature. The contrast between the metallised region and the non-metallised region is due to the additional recombination at the metallised sites and not from shading, since the samples were measured with metal facing downwards. For temperatures of 760°C and below, the contrast difference between the metallised and non-metallised region vanishes as seen in Figure 7.3c. A vanishing contrast indicates that the recombination rate below the contacts is approaching the recombination rate in the non-metallised area.

This qualitative description can be quantified by extracting $J_{0\mathrm{met}}$ values from the PL pictures for different polysilicon thickness and fast-firing peak temperature as described in Chapter 4. The results are presented in Figure 7.4, where the data point markers show the average $J_{0\mathrm{met}}$. The uncertainty bars in Figure 7.4 indicate both the spread among individual samples (process variation) and the uncertainty estimated for the fit used for extracting individual $J_{0\mathrm{met}}$ values as descried in Chapter 4.

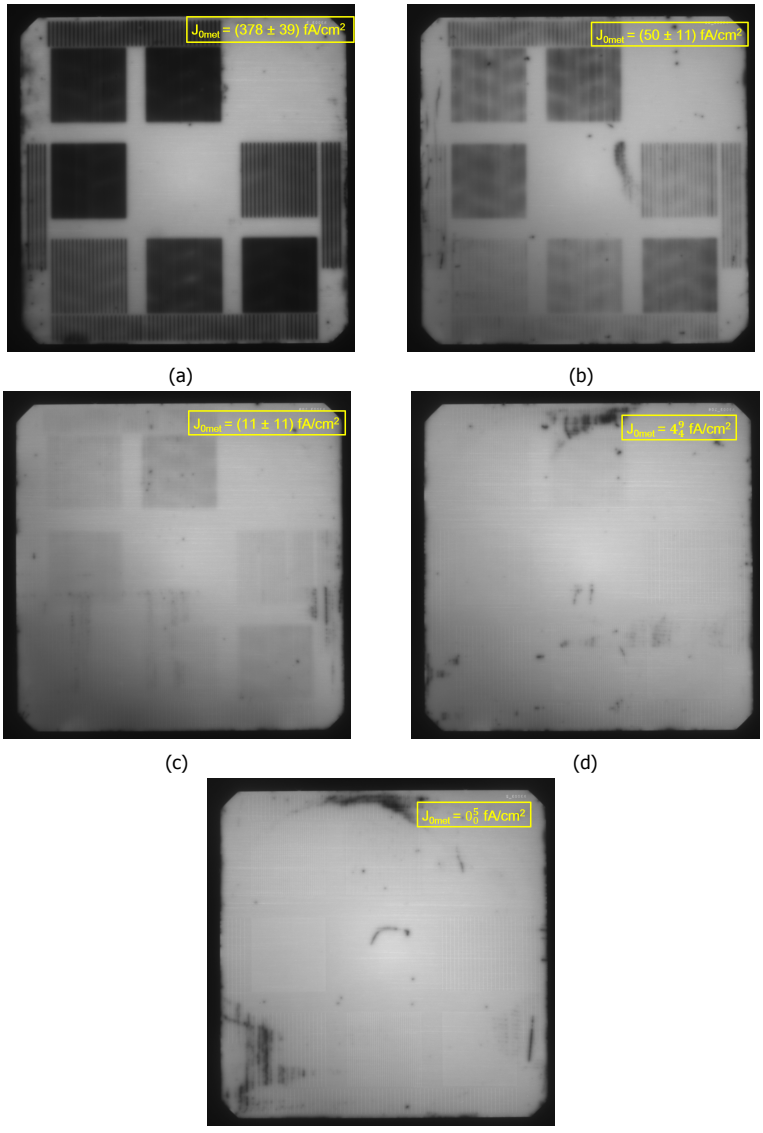


Figure 7.3: iV_{oc} calibrated PL images for samples with a 100-nm thick polysilicon layer, metallised at different fast-firing peak temperature (a) 820°C, (b) 790°C, (c) 760°C, (d) 730°C and (e) 700°C

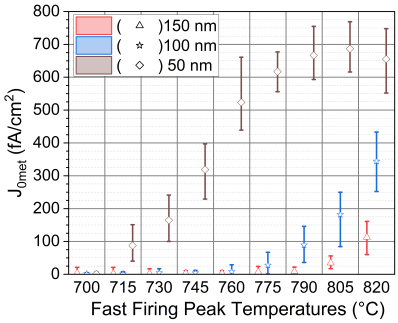


Figure 7.4: J_{0met} values for the samples fired at different fast-firing peak temperatures.

A difference in the magnitude of $J_{0\text{met}}$ can be seen between the samples of different polysilicon thickness that are fired at the same fast firing peak temperature. Examining the results for a specific polysilicon thickness, shows that $J_{0\text{met}}$ increases with increasing fast-firing peak temperature. For example, for the 50-nm thick polysilicon layer, an increase in $J_{0\text{met}}$ by almost a factor of 7 is observed when the fast-firing peak temperature is raised from 715 to 820°C.

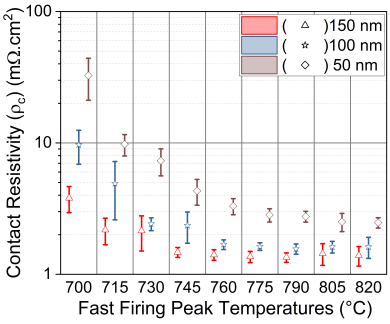


Figure 7.5: Contact resistivity values for the samples fired at different fast-firing peak temperatures.

For achieving a good passivated contact, it is vital to achieve good electrical contact in addition to low $J_{0\text{met}}$ values. In order to demonstrate that this requirement is met for our structures, we use TLM contact resistivity measurements (lumped contact resistivity measurements without any etching between the metal fingers). The results are presented in Figure 7.5. Error bars in this figure represent the standard deviation obtained from 6 to 15 measurements. Excellent values below 2 mΩ.cm^2 (for 150 and 100-nm thick polysilicon layers) for fast-firing peak temperatures from 745 to 820°C are achieved. These values are comparable to previously reported values for polysilicon layers [4, 5, 8, 11, 14]. As explained in Chapter 4, the measured values here are lumped contact resistivity values. These values take into account

the current flow through the whole structure, as we do not isolate the metal finger electrically , and hence represent the lumped contact resistivity.

Increasing the fast-firing peak temperatures, the contact resistivity remains constant within a relatively wide range of fast-firing peak temperatures (for example, for 150-nm polysilicon layer between 745 to 820°C).

For further analysis of the contact, we removed the bulk silver metal, the glass layer between bulk silver and polysilicon and the silver crystallites embedded in the polysilicon by sequential chemical etching steps as described in Chapter 4 and then took SEM images to inspect the polysilicon layer. As an example, SEM images for the samples with different polysilicon layer thickness fired at the peak temperature of 820 °C are shown in Figure 7.6.

As can be observed in Figure 7.6a, for the sample with a 150-nm thick polysilicon layer the polysilicon layer is intact in most parts of the sample. Conversely, for the samples with 100 and 50-nm thick polysilicon layers, the silver paste constituents partially consumed the layer, as presented in Figure 7.6b and 7.6c, respectively. In order to facilitate the interpretation, we marked representative regions where the polysilicon layer has been consumed with blue boundaries in Figure 7.6c. It can be seen that the percentage of these areas in which polysilicon has been etched away by the paste constituents increases with decreasing layer thickness from 150 to 50-nm. This is consistent with the results from the earlier Chapters 5 and 6 as well in the work of Stodolny et al. and Mack et al. [7, 15].

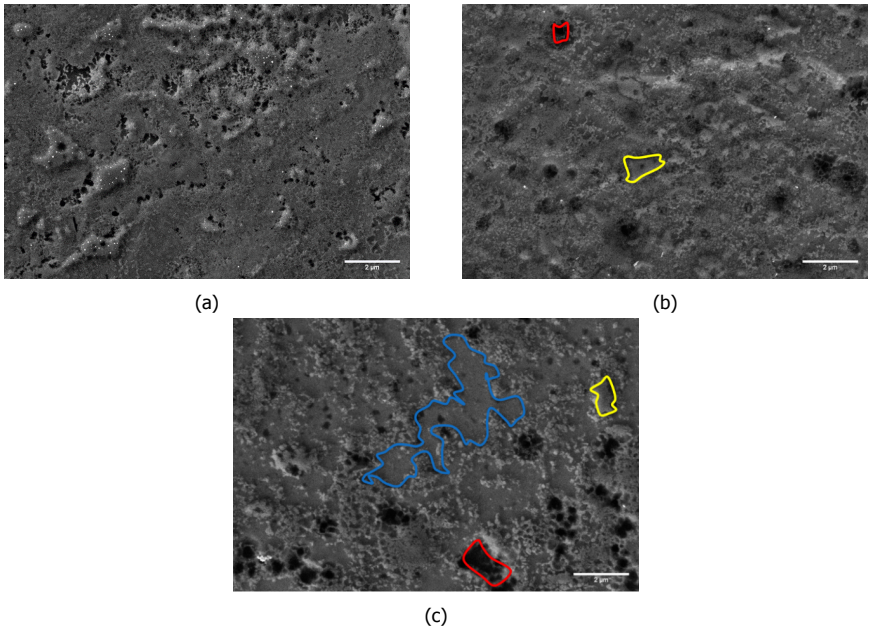


Figure 7.6: SEM images for the different polysilicon thickness after complete etch back of the metal finger: (a) 150 nm, (b) 100 nm and (c) 50 nm. All samples shown here were fast-fired at a peak temperature of 820°C.

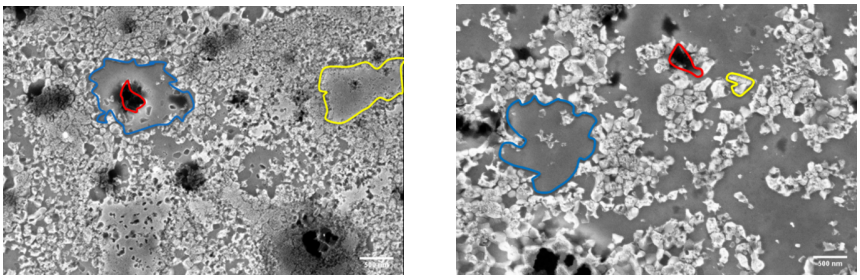
To distinguish between these areas and the areas where polysilicon is intact, we marked representative areas with an intact polysilicon layer with a yellow boundary in Figure 7.6b and 7.6c. This is done based on with the contrast gradient visible in the images. The intact polysilicon appears brighter in the images. Additionally, we can observe deep pits in the wafers. We have marked an example of a deep pit with a red outline. These are almost exclusively visible for the samples with 100 and 50-nm thick polysilicon layers.

Figure 7.7 shows the samples with 100 and 50-nm thick polysilicon layer with higher magnification, again with characteristic surface features highlighted with the color scheme introduced above. The regions where polysilicon has been etched off are larger and more prominent for the thinner polysilicon layer of 50-nm. Conversely, the regions with intact polysilicon layer are larger for the sample with a 100-nm thick polysilicon layer. Similar observations were also made for samples fired at different fast-firing peak temperatures.

Further, we also characterize the contacts with cross-sectional SEM images, which are shown in Figure 7.8. In these images, the silver finger, glass layer and the polysilicon layer on top of the crystalline silicon wafer have not been etched off. Besides bulk silver and a glass layer, silver crystallites embedded in the polysilicon are visible. We have also marked the polysilicon thickness in these images by adding a dashed horizontal line where the interface oxide is expected according to ellipsometer measurements. This approach has been chosen because it is not possible to distinguish between polysilicon layer and substrate in these images.

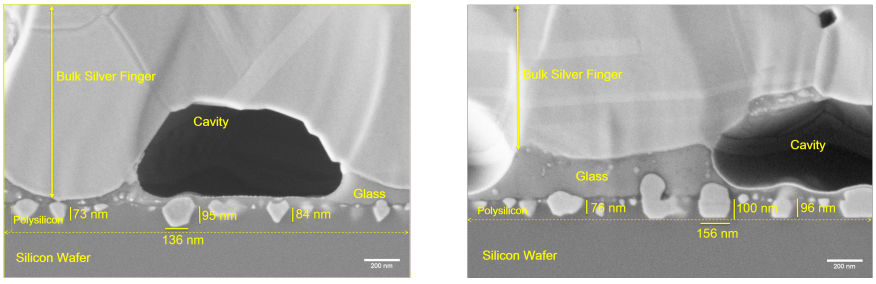
As seen in the cross-sectional SEM images in Figure 7.8, the amount of silver in contact with the thin interface oxide increases as the polysilicon layer thickness is reduced. In Figure 7.8c, the vertical height of crystallites for the samples with 50 and 100-nm thick polysilicon layers is of the order of the polysilicon thickness. Once the silver crystallites get in contact with the thin interface oxide, they appear to grow in the horizontal direction rather than penetrating the interface oxide. This effect leads to more widespread consumption of polysilicon for thin layers. For the sample with a 150-nm thick polysilicon layer, the silver crystallites have vertical dimensions of around 100 nm and only few of them reach the interface oxide. Therefore, no lateral widening of the crystallites occurs, leading to an overall smaller area percentage with consumed polysilicon. This is in accordance with the top view SEM images in Figure 7.6, where we see less intact polysilicon in the sample with 50-nm thick polysilicon layer than the sample with the 150-nm thick polysilicon layer.

In the top-view SEM images, we additionally observed areas with deeper cavities in the wafer surface (red outlines), which can be interpreted as residuals of silver grown into the crystalline silicon bulk in places where the interface oxide was penetrated. However, as these features are scarce in the top view images, we could not identify such features in cross sectional SEM images within the scope of this experiment.

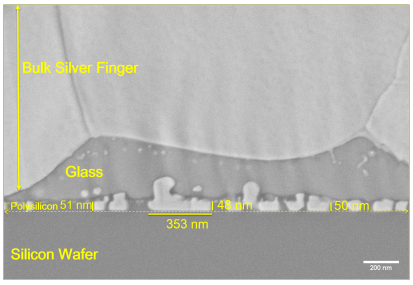


(a) (b)

Figure 7.7: SEM images for samples with: (a) 100 nm and (b) 50 nm thick polysilicon layer. These samples were fast fired at a peak temperature of 820°C.



(a) (b)

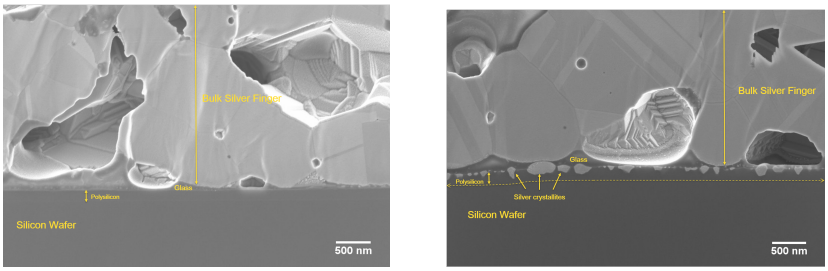


(c)

Figure 7.8: Cross-sectional SEM images for the different polysilicon thickness after complete etch back of the metal finger: (a) 150 nm, (b) 100 nm and (c) 50 nm. All samples shown here were fast-fired at a peak temperature of 820°C.

Based on these findings, we can interpret the dependence of $J_{0\mathrm{met}}$ on the polysilicon layer thickness observed in Figure 7.4. For samples with thin polysilicon layers, a larger fraction of the polysilicon layer is removed due to the horizontal growth of the silver crystallites, and more silver comes in contact with the thin interface. In such areas, the field effect passivation from highly doped polysilicon might be canceled, leading to an increased surface recombination. Additionally, a larger area fraction with silver in direct contact with the interface oxide increases the probabil-

ity for the contact to penetrate the interface oxide and to grow into the crystalline silicon substrate, leading to the deep pits observed in top view SEM images for thin polysilicon layers (Figure 7.6 and 7.7). Such features, where silver is in direct contact with the substrate, are likely to contribute to the substantial increase in $J_{0\mathrm{met}}$ observed with thin polysilicon layers at high contact firing temperatures observed in Figure 7.4.



(a) (b)

Figure 7.9: Cross-sectional SEM images of samples with a 150-nm thick polysilicon layer fast fired at peak temperature of (a) 700 °C and (b) 820°C.

To further investigate the decrease in contact resistivity when the fast-firing peak temperature is increased (c.f. Figure 7.5), we present additional cross-sectional SEM images in Figure 7.9. Here, the interface between the silver and the polysilicon layer is presented for samples with a 150-nm thick polysilicon layer, fast fired at a peak temperature of 700 and 820°C. A large number of silver crystallites are embedded in the polysilicon layer for the sample fired at 820°C. In comparison, no crystallites are observed in the polysilicon layer for the sample fired at 700°C. For the latter sample, some silver precipitates are observed within the glass layer. However, they are not in contact with the highly doped polysilicon layer. This explains the increased contact resistivity at low fast-firing peak temperature as, seen in Figure 7.5. However the increase in Figure 7.5 is remarkable low, considering the big differences at microscopic level. Additionally, it was observed in Figure 7.5, that the contact resistivity increases at a given firing temperature with decreasing layer thickness. This could be caused by a reduced contact surface area between silver crystallites and polysilicon. As shown in Figure 7.6 and 7.7, with the reduction in polysilicon thickness, a less intact polysilicon layer is present after metallisation and fast firing. Hence, the highly doped regions in contact with the metal are reduced, leading to an increase in contact resistivity [16].

7.4. Conclusion

In conclusion, we found that in order to obtain a passivating contact ($J_{0\mathrm{met}} \approx J_{0\mathrm{pass}}$) with a sufficiently low contact resistivity, we need to choose a sufficiently thick polysilicon layer thickness (100 - 150 nm) and an appropriate fast-firing peak temperature. In terms of cell application, the polysilicon layer thickness plays an important role. Too thick polysilicon layers can provide a good passivating contact,

however, at the cost of higher parasitic absorption and an increased production cost. Nevertheless, for samples with polysilicon layers of 100 and 150-nm thickness, a large process window is available where the $J_{0\mathrm{met}}$ and contact resistivity are both low enough to achieve a good passivating contact. For example, for a 150-nm thick polysilicon layer, a fast-firing peak temperature between 745 and 805°C is suitable for application in solar cells.

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8

Polysilicon/SiO_x stack on substrates with different surface finish

The scientist is motivated primarily by curiosity and a desire for truth.

Irving Langmuir

This chapter discusses the influence of different surface finish/morphology of the silicon substrate on the passivation and contact properties of the n^+ polysilicon/ SiO_x passivated contact. Additionally, two different thickness of the polysilicon layers i.e 150 and 200-nm are used in this study.

This chapter is based on the following publication:

- *A. Chaudhary, J. Hoß, J. Lossen, F. Huster, R. Kopecek, R. van Swaaij, and M. Zeman, Influence of Silicon substrate surface finish on the screen-printed silver metallisation of polysilicon based passivating contacts, physica status solidi (a) (2022): 2100869.*

8.1. Introduction

Excellent results of contact resistivity and contact recombination (metal polysilicon recombination current density) have been obtained when polysilicon layers are used in the passivating stacks, with values of 1-2 $m\Omega.cm^2$ for contact resistivity and 250 to 20 $fA.cm^{-2}$ for the metal polysilicon recombination current density [1–5]. In chapter 7, we also showed excellent contact resistivity and metal-polysilicon recombination current density values for 150 and 100-nm thick n^+ polysilicon layers [6]. The mentioned values have been shown on planar silicon substrate samples. It is unclear whether these values can be replicated or achieved if the substrate finish/morphology is changed.

Passivation and contact properties for polysilicon/SiO_x layer stacks with textured silicon substrate were presented by Ciftpinar et al. [2]. In that work, LPCVD based polysilicon layers doped with $POCl_3$ diffusion (ex-situ doping) were used with a thin thermal oxide. Two methods were used to compute the contact recombination in this work, one using modeling of PL maps and other by V_{oc} measurements for different metal coverage. Metal-polysilicon recombination current density of about 400 $fA.cm^{-2}$ for a sample with 200-nm thick polysilicon is presented in that study, however, the influence of different substrate surface finish/morphology was not analysed. Recent study in the year 2022 presented by Firat et al., shows a recombination current density in the screen–printing metallised region on saw-damage removed surface of 25.6 $fA.cm^{-2}$ and a contact resistivity for fingers to polysilicon of 4.9 $m\Omega.cm^2$. While for the samples with a textured surface, the corresponding values were 56.7 $fA.cm^{-2}$ and 1.8 $m\Omega.cm^2$ for a 200-nm thick polysilicon layer with a 1.3-nm thick thermal oxide [7]. Another study by Firat et al., in the same year, shows a recombination current density in the screen–printing metallised region and contact resistivity value for samples with a polished surface of 65.8 $fA.cm^{-2}$ and 2 $m\Omega.cm^2$ respectively for samples with a 150-nm thick polysilicon layer and 1.5-nm thermal oxide. For the semi textured surface finish in the same experiment, they obtain values of around 150 $fA.cm^{-2}$ and 2.5 $m\Omega.cm^2$ [8].

For the utilization of polysilicon-based passivated contacts for front as well as rear surfaces of solar cells, it is useful to understand how the surface finish influences the contact properties. This understanding will also allow a more accurate estimation of the potential gain from utilizing polysilicon-based passivated contact in different cell structures and helps to compose lean productions-process sequences with maximum performance. Many processes involved in the fabrication of the polysilicon/SiO_x cell use single-sided etching (SSE) to eliminate unwanted residuals of quartz tube diffusion processes from one side. This SSE process was performed for many years in HNO_3-HF solutions, but now combined acidic-alkaline and purely alkaline-based processes are available too [9, 10].

In this chapter, a systematic study on the dependence of the contact properties of the polysilicon-based passivated layer stack on the substrate surface finish is presented. Two different polysilicon thicknesses and a wide range of fast-firing peak temperatures are utilised in this study in order to study the effect of the thermal budget and the influence of the polysilicon thickness on the contact properties for substrates with different surface finish. High-resolution SEM images are utilized to

see the differences in contact formation between the samples at microscopic level and explain the trends observed in macroscopic contact properties.

8.2. Experimental design and sample preparation

Symmetric samples with n^+ polysilicon layer on top of a thin tunnel oxide layer were prepared. Standard M2 n-type solar grade Czochralski wafers (CZ) with an average thickness of 180 $\pm$ 10 µm and a base resistivity of 3.9 $\pm$ 0.1 Ω.cm were used. The surface finish was obtained in the following way. The planar surface was obtained by saw damage etch using a dip in 22% concentrated NaOH solution at 80°C. The random pyramidal texture was obtained by immersing the planar wafers in an alkaline solution of KOH and texturing additive MonoTexM (provided by RENA). For the chemically polished surface, a RENA InOxide inline tool was used, filled with HNO_3-HF solution. Textured samples were used for fabricating the polished surface substrates (etching of almost 5-8 µm was done for this purpose).

After obtaining the desired surfaces, an approximately 1.4-nm thick interfacial oxide in nitric acid was grown at room temperature (25 °C). In-situ phosphorous doped silicon layers were deposited by Low Pressure Chemical Vapor Deposition (LPCVD). To get the different thickness, the deposition time during the LPCVD deposition step was changed. Two different thicknesses of silicon layer were used, 150 and 200-nm. These layers were annealed in an industrial tube furnace to form polysilicon layers by solid phase crystallization at 825°C, for 30 minutes.

SiN_x layers were then deposited on both sides of the samples using the Centrotherm cPLASMA PECVD tube reactor. The SiN_x deposition time was adjusted to have the same thickness for the three surface finish. The depositions on both sides of the substrate were done subsequently in two separate depositions. For metallisation, we used Paste G3a with belt speed kept at 3000 mm.min^{-1} with different fast-firing peak temperatures ranging from 760 to 820°C with steps of 15°C.

To give a quantitative estimate of the difference in the surface finish, Sdr (%) values are used. The Sdr value is defined as the developed interfacial area ratio, i.e., additional area contributed by the texture as compared to the flat area:

$$Sdr = \left(\frac{A_{\text{surface}}}{A_{\text{flat}}} - 1\right) \cdot 100\% \tag{8.1}$$

Where, A_{surface} is the area of the surface and A_{flat} is the area of the flat surface. A higher Sdr value corresponds to a larger increase in the total surface area of the sample.

The Sdr values were calculated for 11 to 16 points across samples with different surface finish and are presented in Figure 8.1. These values were calculated from the laser scanning microscope images using a calculation routine in Mountain Map software, which is well explained in the literature [11]. The images were recorded using Olympus OLS400 LEXT microscope. As can be seen in Figure 8.1, the textured surface has the highest Sdr value, with the mean value of 54%. This implies that there is a 54% increase in the surface area after texturing as compared to before texturing. The value for chemically polished samples lies in between the textured and planar values. For the planar samples, the mean value is almost zero.

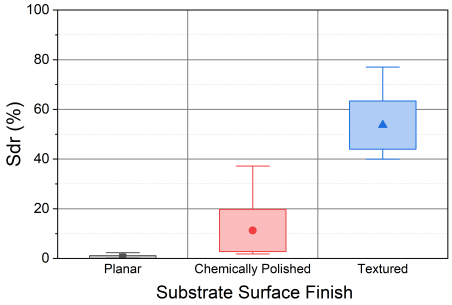


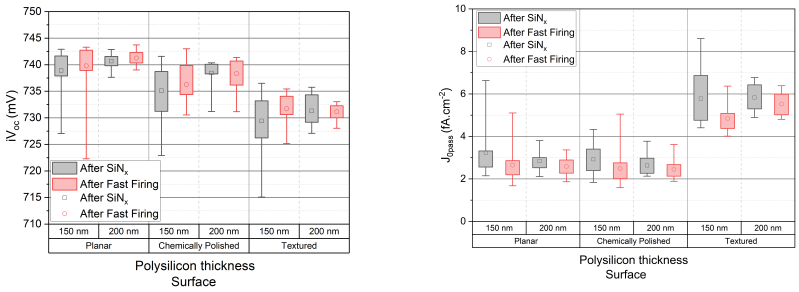
Figure 8.1: The Sdr values for the three surface finish/morphology: planar, chemically polished and alkaline textured samples.

8.3. Results and discussion

8.3.1. Passivation quality for the different surface finish

The implied open-circuit voltage (iV_{oc}) and recombination current density ($J_{0\mathrm{pass}}$) after SiN_x deposition are presented in Figure 8.2. The iV_{oc} of the planar samples is higher as compared to the chemically polished and textured samples. This could be attributed to the surface roughness of the different finish [12, 13]. The trend in the iV_{oc} is similar for both the 150 and 200-nm thick polysilicon layer, for which the mean values are in the same range. These observations are in agreement with reports in literature [2, 14]. Thus, the passivation quality is not substantially affected by the thickness of polysilicon layer. This was also observed in the previous chapter. The mean $J_{0\mathrm{pass}}$ values for the samples remain below 4 fA.cm^{-2} for planar and chemically polished samples, while for textured they are higher at almost 6 fA.cm^{-2} before and after fast firing. The highest iV_{oc} of 743 mV and lowest $J_{0\mathrm{pass}}$ of 2.15 fA.cm^{-2} is obtained for the planar sample with a 150-nm thick polysilicon layer.

The plots in Figure 8.2 also show the iV_{oc} and $J_{0\mathrm{pass}}$ of the samples after metallisation and fast firing. The unmetallised area in the center of the sample was used for this purpose. From these results it is concluded that the iV_{oc} and $J_{0\mathrm{pass}}$ are mostly independent of the polysilicon-layer thickness and from passing through the metallisation process, but are influenced by the surface morphology. Samples with higher surface roughness (higher Sdr value) show a lower iV_{oc} and higher $J_{0\mathrm{pass}}$ as compared to samples with lower surface roughness.



(a) (b)

Figure 8.2: Passivation quality of the samples, with different substrate surface finish, (a) iV_{oc} and (b) $J_{0\mathrm{pass}}$.

The doping profile measured using ECV for the samples with different surface finish are presented in Figure 8.3. Area scaling was done for the textured samples as the surface area is larger for the textured samples as compared to other samples. The surface concentration and the doping tails are similar for the different surface, indicating that the difference in passivation is not because of surface concentration or the doping tails, as we use insitu doped LPCVD layer. LPCVD process is known to be conformal and hence the polysilicon thicknesses are also similar for the different surfaces. This has also be observed in literature [15]. We think that the difference in the passivation quality for the samples with different surface finish is due to difference in the hydrogenation process (from the SiN_x) and the quality of interfacial oxide. Although this needs to be investigated further.

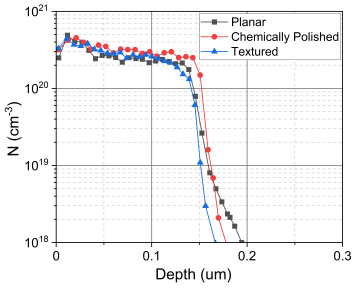


Figure 8.3: Doping profiles for samples with different surface finish.

8.3.2. Metallisation

The contact resistivity as a function of the fast-firing peak temperatures is presented in Figure 8.4. It was measured on five to seven TLM structures per sample. The contact resistivity values for samples with a 200-nm thick polysilicon layer are slightly lower compared to the values for 150-nm thick polysilicon layer. Thus utilising thicker polysilicon layers leads to a reduced contact resistivity. This has also

been observed and explained in the previous chapter. For samples having a planar surface a higher contact resistivity is observed, irrespective of the polysilicon thickness. Only at the fast-firing peak temperature of 760°C, the textured samples show the mean value of contact resistivity which is slightly higher than the planar samples. The lowest mean contact resistivity of 2.5 $\pm$ 0.1 mΩ.cm^2 for the 150-nm thick polysilicon is obtained for textured sample fired at 820 °C. Similarly, the chemically polished samples at this temperature have a mean contact resistivity of 2.5 $\pm$ 0.2 mΩ.cm^2. For the samples with a 200-nm thick polysilicon, the lowest value of 2.0 $\pm$ 0.1 mΩ.cm^2 for the chemically polished sample fired at the peak temperature of 820 °C. Similarly, for the textured sample with a 200-nm thick polysilicon layer fired at 820 °C the mean contact resistivity of 2.1 $\pm$ 0.1 mΩ.cm^2 was obtained. Lower contact resistivity for the textured samples compared to flat surfaces has also been observed when n^+ diffused surfaces are used [13, 16]. The possible reason for the samples with diffused surfaces has been explained by the increased surface area available for contacting as well as more pronounced glass etching due to increased surface roughness, leading to better contact [13, 16].

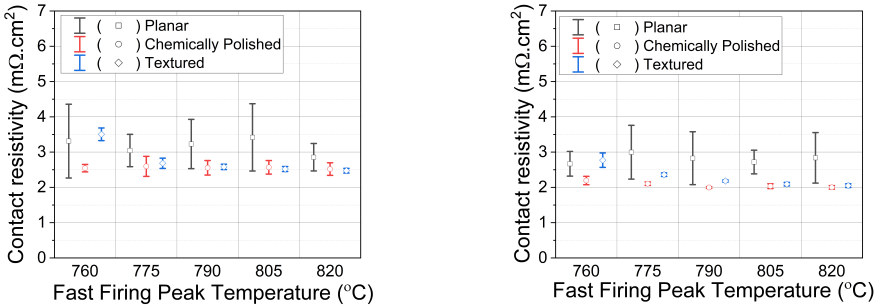


Figure 8.4: Contact resistivity values for samples with (a) 150-nm and (b) 200-nm polysilicon layer thickness and different substrate surface finish.

Cross-sectional SEM images for samples with different surface finish fired at a fast-firing peak temperature of 820°C are presented in Figure 8.5. The bulk silver finger, glass layer, and silver crystallites penetrating the polysilicon layer have been marked in the images. In Figures 8.5a and 8.5b, the location of the interface between the n^+ polysilicon layer/ SiO_x and the c-Si has been marked with a dashed line. The thickness of the polysilicon layer as marked in these images is in accordance with the thickness of the polysilicon layer measured from ellipsometer and cleaved SEM images. This measurement is used to mark the n^+ polysilicon layer/ SiO_x and the c-Si interface. For the samples with chemically polished substrate in Figures 8.5c and 8.5d it is difficult to ascertain the exact thickness of the polysilicon layer, as the interface between the polysilicon layer and crystalline-silicon wafer cannot be differentiated clearly.

From Figures 8.5e and 8.5f it is concluded that for textured samples most of the

silver crystallites are present at the tips and the flanks of the pyramids. This feature has also been observed for fire-through silver paste metallisation on textured surfaces with diffused layers [16, 17]. For the planar surface and chemically polished samples, shown in Figures 8.5a, 8.5b, 8.5c and 8.5d, the crystallites are present all across the surface. The current flow occurs from these silver crystallites to the bulk silver in the places where they are in direct contact to it. Further, for fire-through silver contacts to diffused layers it was presumed that current might also flow via the glass layer by multi-step tunneling, if the glass layer is not too thick [17, 18]. It is assumed that also for the interface between the silver crystallites and polysilicon layer, the silver crystallites and the glass layer determine the current flow through the interface. Compared to the samples with 150-nm thick polysilicon layers, the contact resistivity is lower for the samples with 200-nm thick polysilicon layer, even though there is no significant difference visible in the SEM images. It is thought that this is due to the reduced sheet resistance for the thicker polysilicon layer, making the lateral current flow easier between the silver crystallites.

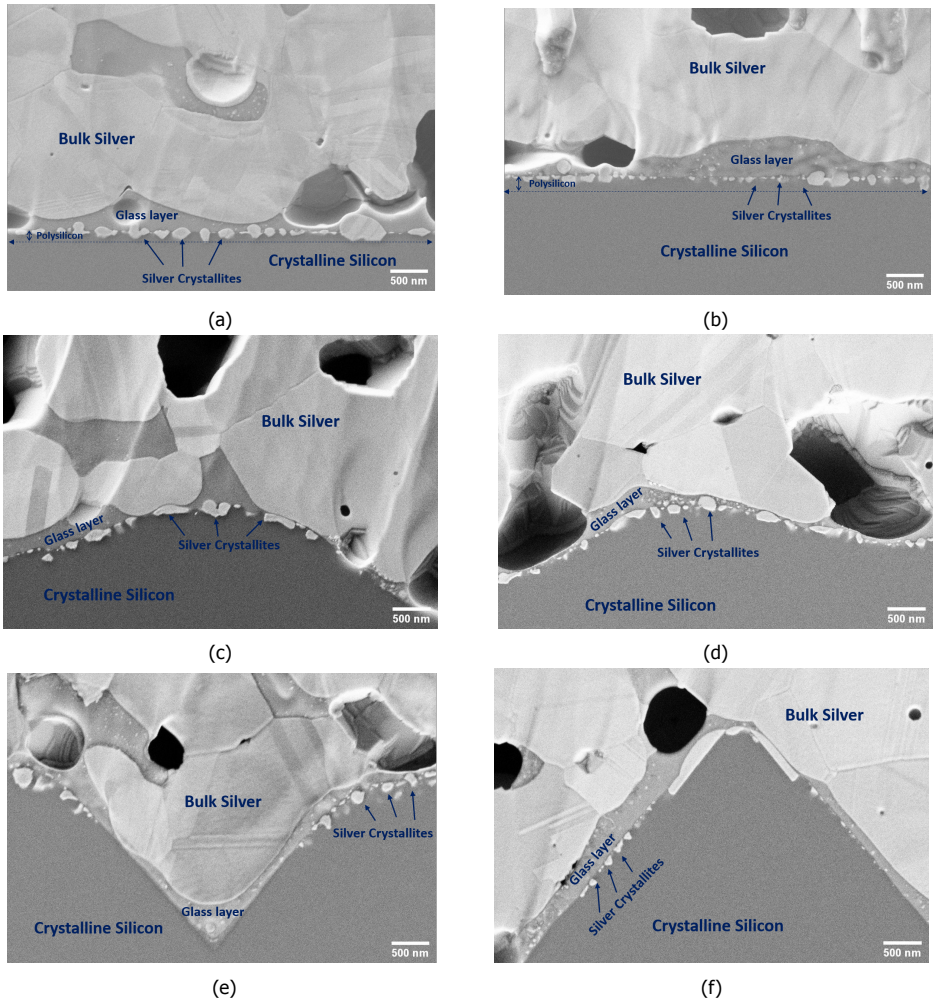


Figure 8.5: Cross-sectional SEM images for samples with 150-nm thick polysilicon layer (left) and 200-nm thick polysilicon (right) fast fired at peak temperature of 820°C: (a) and (b) are with planar surface, (c) and (d) with chemically polished surface, and (e) and (f) are with textured surface.

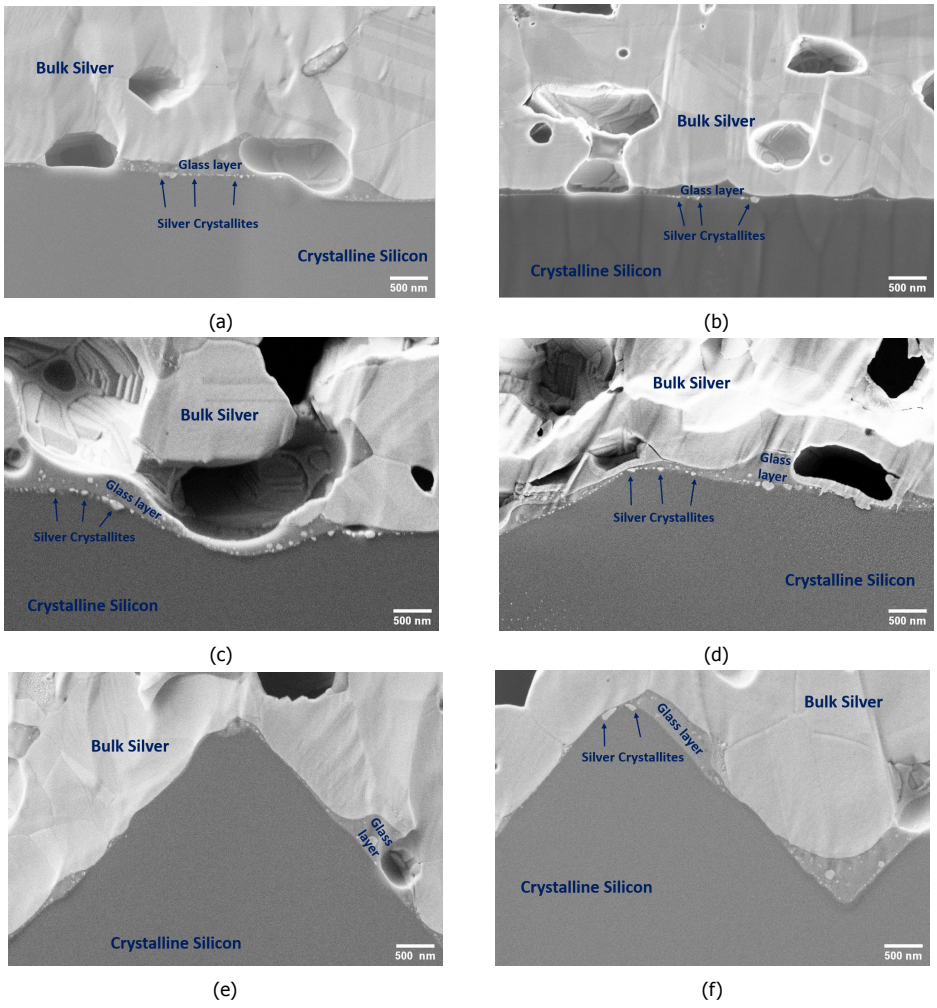


Figure 8.6: Cross-sectional SEM images for samples with 150-nm thick polysilicon layer (left) and 200-nm thick polysilicon (right) fast fired at peak temperature of 760 °C: (a) and (b) are with planar surface, (c) and (d) with chemically polished surface, and (e) and (f) are with textured surface.

At the fast-firing peak temperature of 760°C, the density and size of the silver crystallites in contact with the polysilicon layer is reduced, as seen in Figure 8.6. However, this has no significant impact on the contact resistivity for chemically polished and planar samples. Only in the case of textured samples, a rise in contact resistivity is seen only when the fast-firing peak temperature is reduced. In the SEM images of the textured samples there are almost no silver crystallites penetrating the polysilicon and it is thought that the low density of these penetrating crystallites could be the reason for the rise in contact resistivity. In Figure 8.7, cross-sectional SEM images with higher magnification for the textured surface are presented and places where the glass layer is very thin can be seen. If tunneling through the glass

layer has a contribution to contact resistance, the occurrence of such regions might be important. Also in these images, silver particles embedded in the glass layer, also called precipitates can be seen. They are also visible in Figure 8.6e and 8.6f (as well as in 8.6c and 8.6d). The presence of the silver particles in the glass layer might further enhances the conduction through the glass. It is concluded that at places where no silver crystallites are penetrating the polysilicon layer, a thin glass layer with silver particles embedded in it can contribute to sufficiently high electrical conductivity.

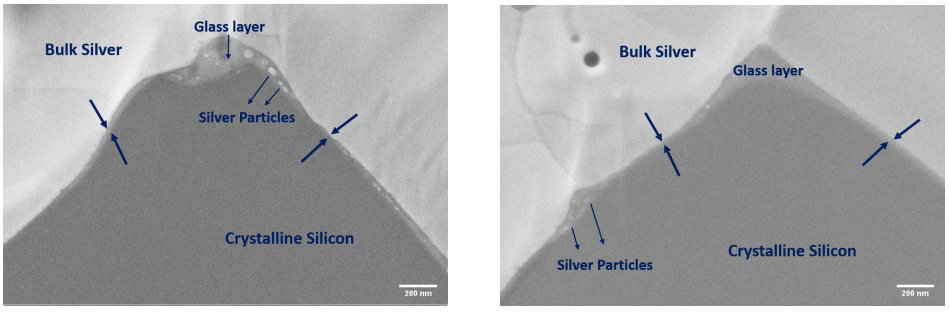


Figure 8.7: Cross-sectional SEM images for samples with (a) 150 nm and (b) 200 nm polysilicon layer with textured surface, fast fired at peak temperature of 760°C.

Utilising the above results and the SEM images, four potential conduction mechanisms are proposed, that can contribute to the low contact resistivity, as displayed in Figure 8.8. In this picture, only planar sample is illustrated to show the different regions in the metallised area; marked with bold letters from A to D. Region A shows the case when the silver crystallite is in direct contact with the bulk silver and penetrating into the polysilicon layer. The current flow here is directly to the bulk silver via the silver crystallite. Looking at region B, where the silver crystallite are penetrating the polysilicon layer, the current flow is from silver crystallite to the bulk silver via the glass layer. This conduction is ascribed to multistep trap assisted tunneling. Additionally, the glass layer in this case is not a perfect insulator as it has some dissolved silver particle, hence enhancing the conduction process.

In region C and D, no silver crystallites in contact with the polysilicon layer are present rather the glass layer is thin enough to support tunneling to the bulk silver from polysilicon layer. In region C, silver precipitates further support in conduction, while in region D the glass layer is so thin that direct tunneling or a direct contact can happen. These four region and their ratio across the metalised finger explain the current flow in the metal polysilicon contact. However, it is difficult to ascertain the contribution of each mechanism based on the microscope images, as these images only show a small fraction of the cross-section.

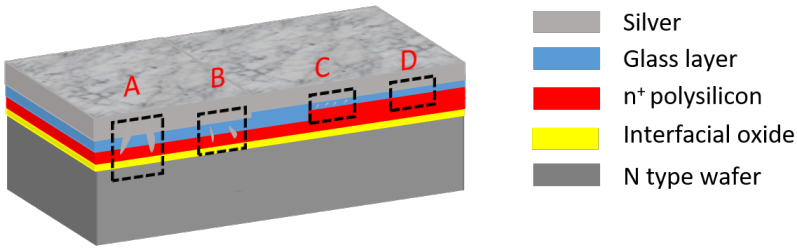


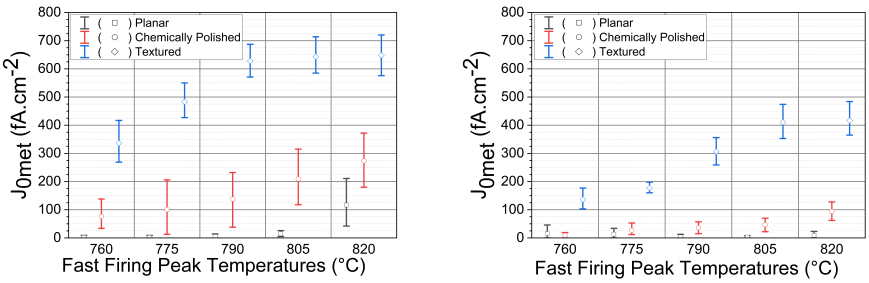
Figure 8.8: Schematic illustration of silver and polysilicon contact with different regions marked as A, B, C and D.

The $J_{0\mathrm{met}}$ values for the samples with different surface finish with respect to the fast-firing peak temperature are presented in Figure 8.9. The error bars in the plots take into account the measurement uncertainty for all the individual samples belonging to a group and the uncertainties arising from the process variations on the individual sample. This is explained in Chapter 3.

For the planar samples, fast-fired at peak temperature below 820°C the $J_{0\mathrm{met}}$ is of the order of J_{01}. Thus, there is no additional recombination from the metallised areas. Similar low values are also observed for the chemically polished samples for the 200-nm thick poly layer. The samples with a textured surface show high values of the $J_{0\mathrm{met}}$ (more than double) in comparison to the planar and chemically polished samples. For textured samples with a 150-nm thick polysilicon layer the $J_{0\mathrm{met}}$ is higher than the corresponding samples with 200-nm thick polysilicon layer. The dependence on fast firing peak temperature is same for both the thicknesses: $J_{0\mathrm{met}}$ increases with higher temperature. Even though in the cross-sectional SEM images for textured samples in Figure 8.7, almost no silver crystallites penetrating in the polysilicon layer can be seen, still the $J_{0\mathrm{met}}$ value is high for these samples as compared to chemically polished or planar samples. One reason behind this could be the reduced thickness of the polysilicon/SiO_x stack in the textured samples. It has been observed that in textured surfaces the thickness of the oxide and can vary leading to thinner oxide and polysilicon at the tips and flanks of the pyramids as compared to the valleys and flat surfaces [19, 20]. Another reason could be that the tip of a pyramid can be etched away from a much larger solid angle. The tip can be etched by the glass from $270\mathrm{deg}$ (and more, imagining phi rotation). For a flat surface, not more than $180\mathrm{deg}$ can be exposed to etching. Based on this observation it is suggested that, the tips and flanks of the pyramids are more susceptible to the damage caused by the metal paste constituents and hence lead to an overall higher metal polysilicon recombination current density.

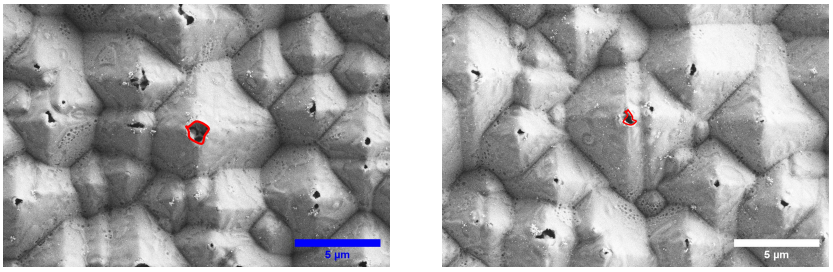
To confirm the hypothesis of damage to the polysilicon/SiO_x layer at the tips and flanks, top-view SEM images for the textured samples fast fired at a peak temperature of 760°C are presented in Figure 8.10. These images were taken after the removal of bulk silver, glass layer and silver crystallites as mentioned in Chapter 3. In these images, it can be seen that the polysilicon layer has been consumed and the tips of the pyramids show deep cavities. As an example a cavity is marked with a red outline. In the valleys, the damage to polysilicon is not observed. It is

suggested that this damage to the passivating layer and the tips of the pyramids is the reason behind high values of $J_{0\mathrm{met}}$.



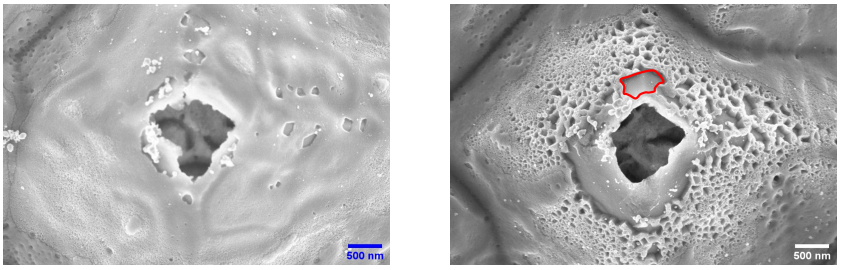
(a) (b)

Figure 8.9: J_{0met} values for samples with (a) 150-nm and (b) 200-nm polysilicon layer thickness and different substrate surface finish.



(a) (b)

Figure 8.10: Top view SEM images for samples with (a) 150-nm and (b) 200-nm polysilicon layer with textured surface, fast-fired at peak temperature of 760°C.



(a) (b)

Figure 8.11: Top view SEM images for samples with 150-nm thick polysilicon layer with textured surface, fast-fired at peak temperature of (a) 760 and (b) 820°C.

In Figure 8.11 the top view SEM image with higher magnification for the textured

sample with a 150-nm thick polysilicon fast fired at peak temperature of 760°C and 820°C, respectively are presented. Visual inspection of these images shows that the damage to pyramid tip is similar in both cases. For the sample fast fired at a peak temperature of 820°C the damage to the polysilicon layer at the flanks of the pyramids is also visible and more damage is observed as compared to sample fast fired at peak temperature of 760°C. To guide the eye, one of this region is marked with a red outline. This supports our hypothesis that the damage to the polysilicon/SiO_x stack is more pronounced at the tip and flank of the pyramids. In SEM images of planar and chemically polished samples fast fired at the same peak temperatures cavities as seen at the tips of the pyramids were not observed. Hence, the damage to the tips of the pyramids could be an important contribution to the higher $J_{0\mathrm{met}}$ for the textured samples. From Figure 8.10, it can also be concluded that the damage to the pyramid tips is less for samples with 200-nm thick polysilicon layer as compared to sample with thinner polysilicon. This could be a reason for the lower $J_{0\mathrm{met}}$ for the textured samples with 200-nm thick polysilicon layer. Hence, increasing the polysilicon thickness can reduce the $J_{0\mathrm{met}}$ value, although this comes at a price of higher parasitic absorption and higher deposition time.

8.4. Conclusion

The surface morphology of the substrate has an effect on the passivation. The planar surface outperforms the chemically polished and textured samples in terms of passivation quality as concluded from the higher iV_{oc} observed for these samples. Excellent values of contact resistivity ($\leq$ 3 mΩ.cm^2) and $J_{0\mathrm{met}}$ ($\approx J_{01}$) are obtained for the samples. Textured samples show higher $J_{0\mathrm{met}}$, while the contact resistivity is slightly lower compared to chemically polished and planar samples, however the difference is not significant. Excessive damage and the removal of polysilicon layer at the tips and the flanks of the pyramids in textured samples are suggested to be the cause of their high $J_{0\mathrm{met}}$ values. The results show that process flows which result in a flat surface, either by alkaline etching of saw damage, or from an acidic emitter etch back of a textured surface are to be preferred to process flows that result in a textured surface to be passivated by a n^+ polysilicon/ SiO_x based passivating contact.

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9

Rear side n^+ polysilicon/SiO_x passivated n-type solar cells

If there has been any success in my life, that was built on the unshakable foundation of failure.

Jagadish Chandra Bose

This chapter combines the learnings from the previous chapters for fabrication of solar cells. Herein, the rear side n^+ polysilicon/SiO_x passivated n-type c-Si solar cell is presented. The details about the fabrication and the performance of the cell are explained in this chapter.

9.1. Introduction

Currently, 95% of the photovoltaic market is dominated by crystalline silicon (c-Si) solar cells. An important reason for the dominance of c-Si can be attributed to the continual technological improvements, which have led to a gradual increase of efficiency, continued decrease of costs and hence decrease in levelised cost of electricity [1]. Over the last years the average efficiency of the solar cells and modules has been improving by 0.4-0.6% absolute per year [2, 3]. The International Technology Roadmap (ITRPV)-2021 predicts that the cell efficiencies will continue increasing in this decade. According to the predictions the efficiencies increase will be due to the development and implementation of existing and new technologies.

Presently, the main stream industrial c-Si solar cells and modules are Passivated Emitter Rear Contact (PERC) and its derivative such as Passivated Emitter Rear Total (PERT) contact cells [4, 5]. Almost 90% of the PERC cells use silicon wafers doped with boron at the time of writing this thesis. The segregation coefficient of boron (0.8) is higher than of phosphorus (0.35), which leads to a more uniform resistivity across the ingot during crystal growth than with phosphorus doping for n-type wafers [3, 6, 7]. However, the efficiency of the p-type wafer based cells is reduced under illumination. This is referred to light-induced degradation (LID), which has been attributed to boron-oxygen related defects [8, 9]. The degradation in efficiency has also been observed at elevated temperatures (above 75°C) and this is called Light and elevated Temperature Induced Degradation (LeTID). Many research groups have investigated this effect [8–13].

Efficiencies in range of 21-22% at industrial level can be achieved with p-type PERC cells, but these cells suffer from recombination losses, specifically at the metal-semiconductor interface, as well as from LID and LeTID [14, 15]. In particular, recombination in the emitter region is a major cause of the losses [16, 17]. A detailed study utilising experimental results and Sentaurus TCAD by Saint-Cast et al. also points out that the major improvement in efficiency for the PERC cells can be obtained by optimising the doped regions and the metal-silicon contact [18].

One solution to LID is using gallium-doped wafers, another solution is to use n-type (phosphorus-doped) substrate wafers. The processes and the production cost for cells with n-type wafers are now mature and low enough, respectively, to be put to mass production. As explained in Chapter 2 and 6, the recombination and resistive losses can be reduced by the use of a highly doped n^+ polysilicon/SiO_x layer stack. For this reason this chapter focuses on the development of n^+ polysilicon/SiO_x contact stacks based on n-type crystalline silicon wafers. A detailed review article from Allen et al. shows the efficiencies of cells developed in recent times, with the highest efficiencies achieved with the cells utilising polysilicon/SiO_x passivating stacks [19].

In 2017, Fraunhofer ISE presented an efficiency of 25.7% for a front- and rear-contacted cell, with a rear Tunnel Oxide Passivating Contact (TOPCon) cell [20]. The interfacial oxide used in this architecture supports tunneling, hence is called TOPCon [20, 21]. Similarly, in 2018, the Institute for Solar Energy Research in Hamelin (ISFH) reported a lab-scale efficiency of 26.1% for a solar cell utilizing a polysilicon/SiO_x contact scheme at the rear side [22]. ISFH coined the term POLO

(POLycrystalline silicon on Oxide) for the passivating contact they use. This solar cell employs a silicon oxide layer that is more than 2 nm thick and the conduction across the this oxide layer is dominated by the pin holes generated during a high temperature process (annealing process).

For the implementation of the above high-efficiency cells into industry, major changes have to be made in terms of the processes used, with major focus on metallisation. The lab devices commonly utilise evaporation as the method of metallisation. While this method leads to no damage to the layers underneath, it is not feasible for large-scale utilisation and also not cost effective.

Industrial application of polysilicon/SiO_x passivating layers has gained tremendous impetus in recent times. Extensive work on industrialisation has been performed by the group in SERIS. They have developed large-area front and back contact cells with rear-sided application of polysilicon layer, called as monoPOLY cells [23–26]. For LPCVD based polysilicon layers, monoPOLY cells show a champion efficiency of 22.6% [24], while for a PECVD based polysilicon this approach shows a champion efficiency of 23.05% [26]. Work from Lanterne et al., presents a LPCVD deposited phosphorus doped polysilicon passivated contact large area cell with an efficiency of 23% [27]. For LPCVD deposited n^+ polysilicon layers Firat et al., present M2 sized champion cell efficiency of 23.01% [28]. Fraunhofer ISE also recently demonstrated M2 sized cells based on PECVD deposited n^+ polysilicon layers and screen printed metallisation with high efficiency of 22.95% [29]. Some of the big solar-cell manufacturers, such as Jolywood, Trina Solar, JinkoSolar and GCL, have recently demonstrated champion efficiencies of 24.21%, 24.58%, and 23.04%, for large-area solar cells with polysilicon/SiO_x layers. [30–32].

In this chapter, we start from our nPERT solar cell (called as BISoN) to develop a rear-sided n^+ polysilicon/SiO_x based cell, using steps which can be used in a high-throughput manufacturing process. This development provides a pathway to upgrade the existing solar-cell manufacturing lines to increase efficiencies by utilisation of n^+ polysilicon/SiO_x passivating layers. The main objective of this chapter is to develop high efficiency cells that utilise an n^+ polysilicon/SiO_x layer stack with industrially viable steps. Griddler 2.5PRO simulations are also used in order to improve the solar-cell efficiencies by better understanding potential improvements through loss analysis [33].

9.2. Rear side n^+ polysilicon/SiO_x cell processing

As the starting point for development of our M2 sized n^+ polysilicon/SiO_x based cell, we took the already well established cell concept christened as Bifacial Solar cell on N-type wafer (BiSoN), which is an industrial M2 sized n-PERT solar cell [34–37]. The main steps involved in the BiSoN cell processing are shown in Figure 9.1. A BiSoN solar cell contains a diffused boron emitter at the front side and a phosphorus back surface field, which acts as the electron collecting layer. The metal contacts are screen printed with fire-through silver paste. A schematic representation of the n-PERT (BiSoN) solar cell is shown in Figure 9.2. The highest efficiency obtained with this cell is 20.9% and upto 21.5% in industrial production [36].

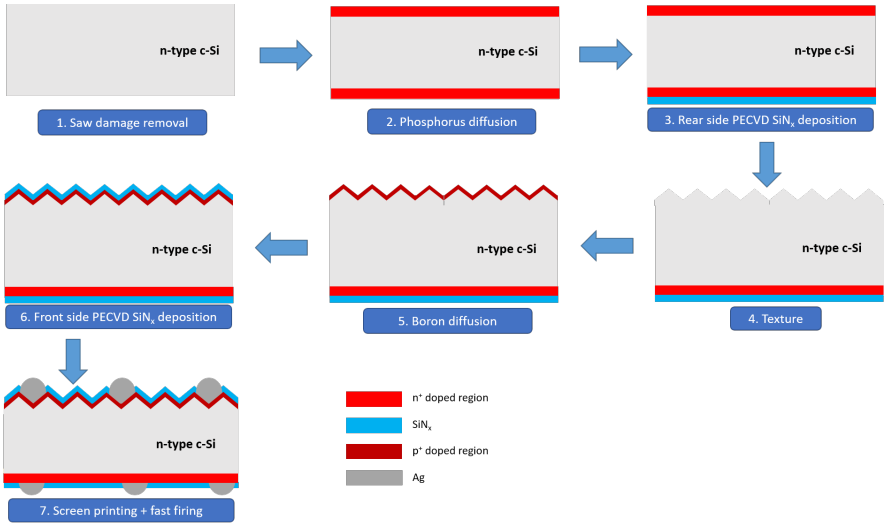

Figure 9.1: The process flow for making an nPERT (BiSoN) solar cell.

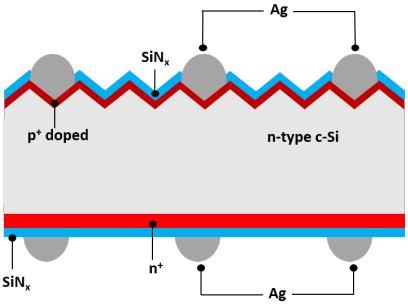

Figure 9.2: Schematic representation of the nPERT (BiSoN) cell.

9

To implement the n+ polysilicon/SiO_x layer stack, additional steps were added to the nPERT (BiSoN) process and the process sequence was altered. The new process sequence is shown in Figure 9.3. Also this process sequence starts with saw damage removal, but is then followed by texturing of the wafer and boron diffusion. This is followed by single-side acidic etching of the rear side of the sample. The single-side acidic etching step was performed in a RENA inline tool with water capping on the front side to protect the boron diffused emitter. This step was included in order to remove the boron diffused layer from the rear side. After this step, a wet chemical interfacial oxide layer of approximately 1.4 nm was grown in 68% HNO_3 at 25°C, followed by LPCVD deposition (in-situ doped layer) and solid-phase crystallisation by annealing at 825°C for 30 minutes to form a 150-nm thick n+ polysilicon layer with surface doping of 2.0×10^{20} cm^{-3}. After the annealing step, a PECVD silicon

nitride (SiN_x) deposition was performed on the rear side. Afterwards the polysilicon layer on the front side was removed by a dip in 22% NaOH at 80°C for 45 sec. The rear side polysilicon was protected by the SiN_x capping during this etching step. This was followed by PECVD deposition of a silicon nitride anti-reflection coating for the front side. The metallisation (unless specified) was performed following the sequence below:

- Rear side finger print (100 fingers)
- Drying
- Front side finger print (100 fingers)
- Drying
- Fast Firing
- Front Busbar Print (5 Busbars)
- Drying
- Rear Busbar Print (5 Busbars)
- Drying

Fire-through silver paste was used for the front and rear fingers; for the busbars a non firing-through low-temperature silver paste was used. The best performing silver paste according to the experiments from Chapter 5 and 6, Paste G3a, was used for n^+ polysilicon/SiO_x layer stack. For the boron emitter a different silver paste (Paste G1a) was used.

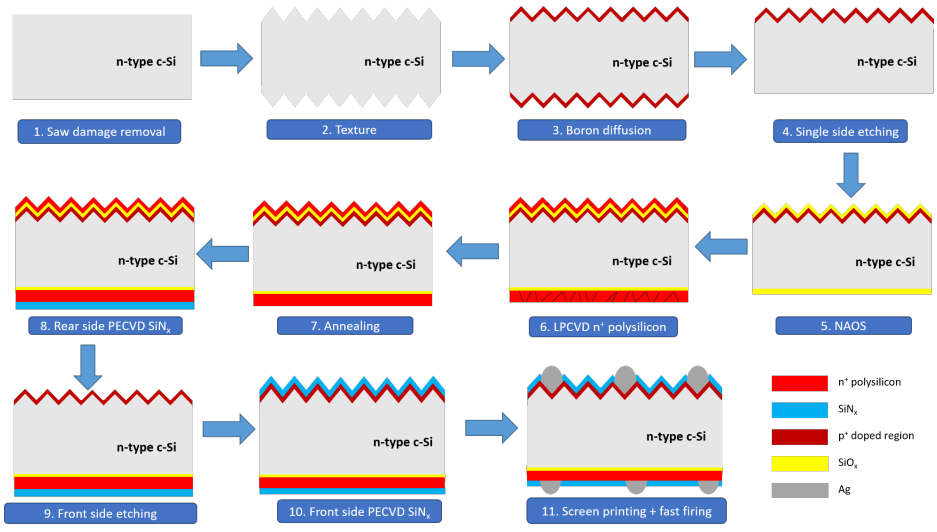

Figure 9.3: Major steps involved in rear side n^+ polysilicon/SiO_x passivated cell processing.

9.3. Optimisation of solar-cell performance

This section discusses the experiments that have been carried out for the development and optimisation of the rear side n$^+$ polysilicon/SiO$_x$ passivated contact cell with efficiency greater than 22%.

9.3.1. n$^+$ polysilicon/SiO$_x$ cell fabrication

In the first experiment the process flow was used that is displayed in Figure 9.3 and discussed in the previous section to fabricate the n$^+$ polysilicon/SiO$_x$ passivated contact cell. Silver paste G3a was used for contacting the 150-nm thick n$^+$ polysilicon/SiO$_x$ layers. Paste G3a had a lower contact resistivity and $J_{0\mathrm{met}}$ in comparison to other silver pastes for the n$^+$ polysilicon/SiO$_x$ layers as shown in Chapter 5. For the boron diffused layer, paste G1a is used as it is dedicated for use on diffused contacts. The results of the cells fabricated are presented in the Table 9.1. The mean values and the corresponding best n$^+$ polysilicon/SiO$_x$ based cell value fabricated in the first experiment are presented in this table. In this table the nPERT (BiSoN) best cell parameters are also presented [36].

Table 9.1: External parameters of the cells.

V_{oc} (mV)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)	
671	37.92	76.8	19.54	Mean value
676	37.91	77.8	19.95	Best cell
663	39.30	80.1	20.90	Best cell (BiSoN)

To understand the performance of the n$^+$ polysilicon/SiO$_x$ passivated contact cells, the shunt and series resistance for the cells fabricated in this experiment was measured. We found out that the shunt resistance was between 5-12 Ω, which is very low for solar cells and the series resistance was between 0.004-0.007 Ω, which is higher than expected [38, 39]. This is attributed to the polysilicon wrap-around region. A picture of the unmetallised cell is presented in Figure 9.4, in which the polysilicon wrap around region on the front side is marked with dashed lines. It is also visible as the pink colored region at the corners of the sample.

The polysilicon wrap-around region is caused due to incomplete etching of the polysilicon layer on the front side of the cell during the front-side etching (single side etching) process during step 9 as shown in Figure 9.3. This incomplete etching of the polysilicon layer at the corners of the front side is due to the PECVD SiN$_x$ layer deposited on it in step 8 (Rear side PECVD SiN$_x$). This unwanted SiN$_x$ layer is the by-product of the PECVD deposition process.

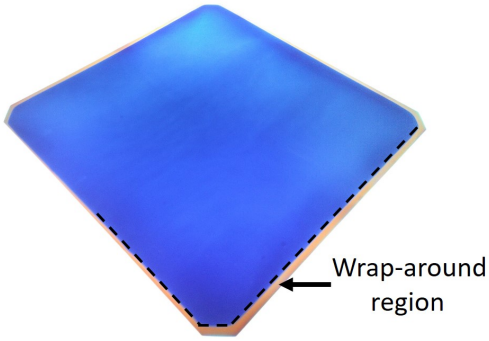

Figure 9.4: Front side image of a n^+ polysilicon/SiO_x cell, the wrap around region is marked with dashed lines.

The PECVD deposition of the SiN_x capping layer for the rear side is not a perfectly single sided process it leads to the unintentional SiN_x layer deposition at the corners of the front side. The wrap-around region forms leakage current paths [38] and ultimately leads to loss in fill factor and efficiency, hence the complete removal of the wrap-around region is essential [23, 38, 40]. To confirm that the wrap around region caused electrical losses a laser-edge isolation step after fabrication of the cells was performed. After laser-edge isolation, the I-V characteristics of the cells was measured again. The shunt resistance improved to values between 16 to 40 Ω and the series resistance decreased to 0.002-0.003 Ω. This is a substantial improvement, but compared to nPERT cells the values are still not optimal. Overall with the isolation step the fill factor increased by almost $2 \pm 0.2\%$ absolute with the J_{sc} increase of almost 0.8 $mA.cm^{-2}$ as compared to cells without edge isolation.

9.3.2. Cell performance improvement with pre-fast-firing and improved wrap-around removal

To further improve the efficiency and to remove the additional laser edge isolation step, the HF immersion time (after the rear side SiN_x deposition in step 8 in the process chain in Figure 9.3) was increased to completely remove the PECVD SiN_x layer that is unintentionally deposited at the edge of the cell´s front side. By doing so, we were able to completely etch the polysilicon layer on the front side, during the immersion in KOH, and remove the wrap-around region in step 9 of the process chain shown in Figure 9.3. All the cells prepared from now on received the increased HF immersion time.

Motivated from literature about the improvement of surface and bulk passivation by migration of hydrogen (from the PECVD SiN_x layer) to the bulk, by a high temperature step with a short holding time, we incorporated a high temperature step before the screen printing metallisation [41, 42]. We choose fast-firing to achieve this step. In order to accomplish this, we did a pre fast-firing for a group of samples, which was incorporated before the screen printing metallisation, i.e step 11. This

fast-firing step leads to hydrogen migration in the bulk/substrate which passivates the bulk defects and thus should increase the V_{oc} of the cell [41]. One group of cells were pre-fast-fired, with a peak temperature of 820°C at a belt speed of 3000 mm.min^{-1}. The other group did not receive the pre-fast-firing step. Pre-fast-firing is done using our fast-firing furnace before metallisation, using the same recipe as for metallisation, but with a higher peak fast-firing temperature. The other steps remain unchanged during processing.

The results of the external parameters of the cells from the second experiment are presented in Figure 9.5. As presented in Figure 9.5a, the cells which were not pre-fast-fired outperformed the samples which were pre-fast-fired in terms of the V_{oc}. This was not according to our expectations. We expected that the cells that were pre-fast-fired would have higher V_{oc}. The highest mean efficiency was achieved at the fast-firing peak temperature of 805°C at a belt speed of 3000 mm.min^{-1}, as seen in the Figure 9.5. The results from the best group are presented in Table 9.2.

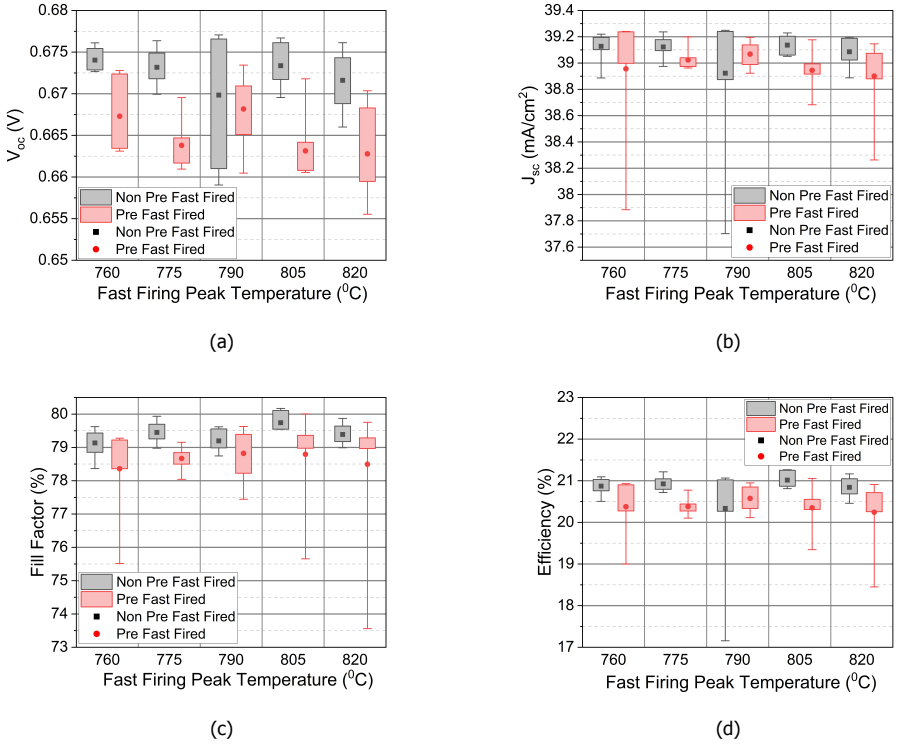

Figure 9.5: Electrical parameters of the solar cells with and without pre-fast-firing, (a) open-circuit voltage, V_{oc} (V), (b) short-circuit current density, J_{sc} (mA.cm^{-2}), (c) fill factor, FF (%) and (d) conversion efficiency, η (%).

We hypothesised that the pre-fast-firing step leads to deterioration of the n$^+$

Table 9.2: External parameters of the solar cells.

V_{oc} (mV)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)	
674	39.14	79.80	21.03	Mean value
677	39.23	80.10	21.26	Best value

polysilicon/SiO_x layer stack. For this purpose we carried out an experiment with the aim to understand the effect of pre-firing on the J_{0met} and ρ_c of the n^+ polysilicon/SiO_x layer stack. For this experiment we used 150-nm thick n^+ polysilicon/SiO_x symmetrical samples, as the n^+ polysilicon layer thickness used for the cells was also 150-nm. The symmetrical samples were prepared with the same procedure as described in Chapter 6. Two sets of samples were utilised in this experiment, one set was pre-fast-fired and the other was not. The pre-firing was done at 820°C at a belt speed of 3000 mm.min^{-1} before metallisation. The fast-firing peak temperature for metallisation was varied in steps of 15°C from 760 to 820°C, while the belt speed was kept constant at 3000 mm.min^{-1}. The corresponding J_{0met} and ρ_c are presented in the Figure 9.6. From the results presented in Figure 9.6, it can be seen that J_{0met} is higher for the samples which were pre-fast-fired, while the contact resistivity is similar for the two sets of samples. It was hypothesised that if the n^+ polysilicon/SiO_x layer stack is exposed to a thermal step before metallisation it leads to the higher metal recombination current density during metallisation due to a possible change in the material properties of the layer stack. In view of these results, we removed the pre-fast-firing step and investigated other ways to increase the efficiency of the cell further.

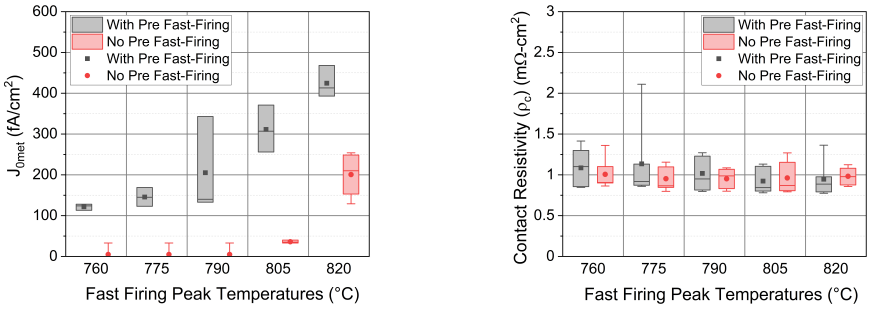

Figure 9.6: (a) J_{0met} and (b) contact resistivity values for the samples with and without pre-fast-firing.

9.3.3. Cell performance improvement with AlO_x passivation

In the third experiment, we implemented AlO_x passivation for the boron emitter in order to reduce the overall recombination current density. The reduction of recombination current density by the application of AlO_x layer has been studied extensively [43–45]. We used a 7 to 8-nm thick PECVD AlO_x layer for the front side, this

step was incorporated before the SiN_x front side deposition, i.e. step 10 in Figure 9.3. Two different recipes for deposition of AlO_x layer were used for this purpose: One using an RF power of 1800 W for 100 sec and another using 2250 W for 90 sec. In this experiment, we also utilised 100-nm thick n^+ polysilicon layer because according to the experiments presented in Chapter 7, $J_{0\text{met}}$ for 100-nm thick layer was similarly low in addition to 150-nm thick layers used in earlier experiments. The samples were fast-fired at 790°C at 3000 mm.min^{-1} belt speed.

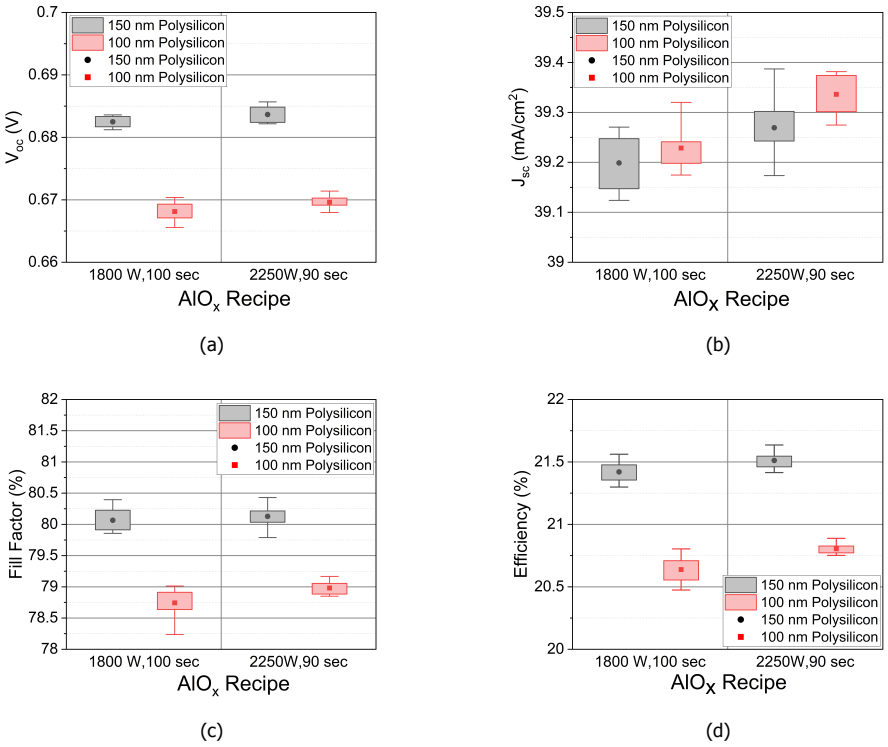

Figure 9.7: External parameters of solar cells with two different AlO_x passivation, (a) open-circuit voltage, V_{oc} (V), (b) short-circuit current density, J_{sc} (mA.cm^{-2}), (c) fill factor, FF (%) and (d) conversion efficiency, η (%).

From the plots, presented in the Figure 9.7, the solar cells with 150-nm thick n^+ polysilcion layer and AlO_x layer deposited at 2250 W for 90 sec outperform the cells in the other group. A mean efficiency of 21.5% is obtained for this group. The reason for the higher efficiency is the higher V_{oc} and a slightly higher J_{sc} obtained for this group. From these results it can also be seen that reducing the polysilicon thickness leads to a lower V_{oc} and fill factor. Eventhough the J_{sc} is higher, it cannot compensate the reduction of the other two parameters. The reason for higher J_{sc} can be attributed to reduced parasitic absorption (free carrier absorption) for the thinner polysilicon layer [46–48]. As shown in Chapter 7, reducing the polysilicon

layer thickness leads to increased $J_{0\text{met}}$ and increased contact resistivity, resulting in a reduced V_{oc} and fill factor. The mean values for the samples with 150-nm thick polysilcion and AlO_x deposited at 2250 W for 90 sec are V_{oc} of 684 mV, J_{sc} of 39.37 mA.cm^{-2}, fill factor of 80.10% and efficiency of 21.51%. The best cell had an efficiency of 21.64% (V_{oc}- 686 mV, J_{sc}- 39.33 mA.cm^{-2}, fill factor- 80.20%) .

Comparing these results to the nPERT champion cell parameters presented earlier, there is almost 0.7% absolute increase in the efficiency for the best cell. This is due to the higher V_{oc}, which is 18 mV higher in terms of mean values when compared to the best nPERT (BiSoN) cell [36]. To increase the J_{sc}, we modified the front side metallisation i.e, the bus-bars and front finger's width and number. The Griddler 2.5Pro simulations are presented in Appendix B to support the need of modifying the front side metallisation in order to further improve the cell efficiency.

9.3.4. Cell performance improvement with modified metallisation

Motivated from the past experiments and literature we used increased number of bus-bars and fingers, with reduced width in order to increase efficiency of the cell further [49–51]. The transition to thinner (fine line) fingers took many years to accomplish, from 120 µm in 2005 to less than 20 µm in 2022 [52, 53, 53, 54]. A comprehensive study is presented in the work of Timo Wenzel et al. [54]. The recent transition to thinner fingers is the result of the newly developed knotless screens which allow optimum print quality for thinner fingers [55]. To further increase the V_{oc} and J_{sc} of the cells, we modified the front metallisation scheme by increasing the number of fingers to 135, and by reducing the printed finger width to in the range of 20-25 µm. The Griddler simulation results presented in Appendix B show that this change in metallisation scheme should increase the performance. A simple calculation with the assumption that the M2 wafer is a square with side of 156.75 mm shows that with 60 µm (front finger width) and 100 fingers the metal shading is 3.8%. In comparison, with a 20 µm (nominal front finger width) and 135 fingers the metal shading is reduced to 1.7%.

The front fingers were screen printed using a knotless screen with opening of 16 µm. Also, we changed the number and design of front bus bars. In this experiment, we used 9 bus-bars with a tapered design to further reduce the shading loss instead of 5 with rectangular design. We used thinner 9 bus-bars as compared to the pattern was expected to even further reduce the shading losses as compared to the thicker 5 bus-bars of 800 µm.

In this experiment, we used a different n^+ polysilicon recipe, with increased deposition temperature which had similar passivating performance (J_{01} below 7 fA.cm^{-2} and iV_{oc} above 725 mV for symmetrical samples) with improved homogeneity (layer thickness) across the wafer and across the boat used in LPCVD deposition. This was done so as to avoid any variance in the cell performance due to inhomogeneity in polysilicon layer quality. In this experiment, we also used a silver-aluminium (Ag-Al) paste for the front boron emitter that had lower $J_{0\text{met}}$ and ρ_{c} as compared to the silver paste we were using earlier for the boron emitter. The other change was the use of a higher belt speed and different fast-firing peak

temperatures. Belt speed of 3000 mm.min^{-1} and 7000 mm.min^{-1} were used in this experiment. The fast-firing peak temperatures for the two belt speeds were chosen such that they correspond to similar thermal budget for the cells. A higher belt speed is more comparable to an industrial environment, hence this comparison was made. It was tested by us that a 1000 mm.min^{-1} increase in the belt speed leads to a decrease of 8-10°C on the wafer surface in the peak temperature zone. This was the motivation for the choice of the peak fast firing temperature. The polysilicon thickness was chosen to be 150-nm and the AlO_x layer was deposited at 2250 W power for 90 sec. To sum up, the modifications which were made in this experiment are as follows:

1. 135 front fingers.

2. 9 bus-bars.

3. Silver-aluminium (Ag-Al) paste for front side finger metallisation.

4. Higher belt speed for fast-firing process.

The electrical parameters of the cells fabricated are presented in Figure 9.8. The samples in the group fast fired at a belt speed of 7000 mm.min^{-1} and at a fast-firing peak temperature of 805°C, outperform all the other solar cells in terms of the mean efficiency values, although the champion cell in this experiment belongs to the group fast-fired at peak temperature of 820°C and 7000 mm.min^{-1}. The external parameters of the best cells are presented in Table 9.3. In this table, the value for the best cell from the group fast-fired at peak temperature of 805°C and 7000 mm.min^{-1} is also shown.

To compare the effect of silver-aluminium front fingers with respect to the silver front fingers, we processed one group with silver front fingers (Paste G1a) with 9 bus-bars and 135 front fingers. The results from this group are presented in Table 9.4.

From the results presented in Table 9.3 and 9.4, it can be concluded that the open-circuit voltage is increased with the use of silver-aluminium paste. The fill factor is also acceptable (above 79%) for the cells with Ag-Al front fingers.

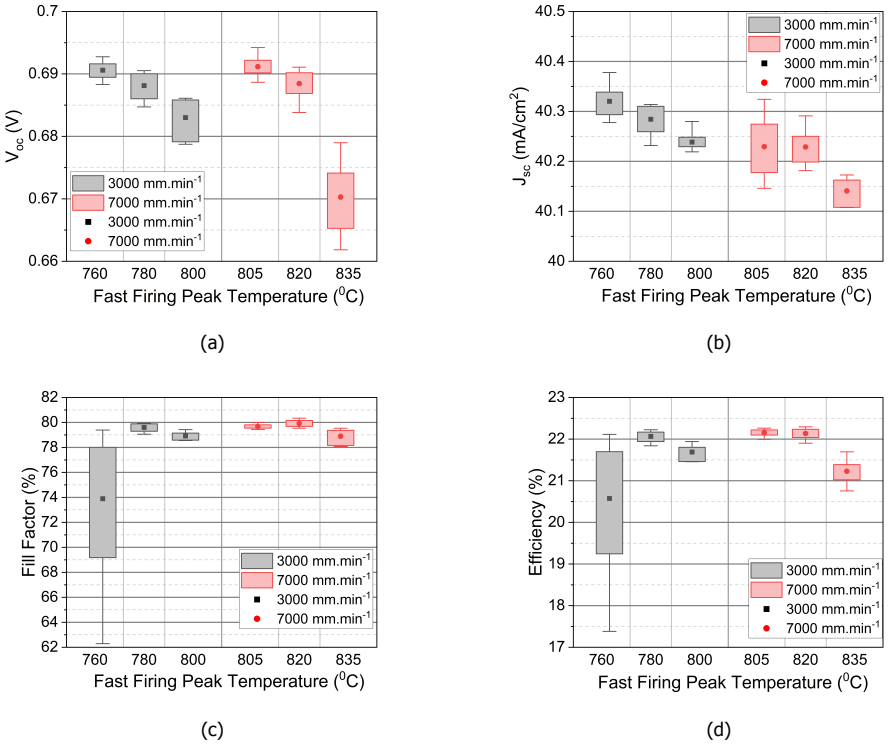

Figure 9.8: External parameters of the cells with 9 bus bars, Ag-Al front fingers and different fast-firing recipes, (a) open-circuit voltage, V_{oc} (V), (b) short-circuit current density, J_{sc} (mA.cm^{-2}), (c) fill factor, FF (%) and (d) conversion efficiency, η (%).

Table 9.3: External parameters of the best cell with 9 bus-bars and Ag-Al front fingers.The belt speed for these cells was 7000 cm.min^{-1}.

V_{oc} (mV)	J_{sc} (mA.cm^{-2})	FF (%)	η (%)	
690	40.20	80.34	22.29	Best value (820 °C)
694	40.30	79.64	22.26	Best value (805 °C)

Table 9.4: External parameters of the cells with 9 bus bars, Ag front fingers.

V_{oc} (mV)	J_{sc} (mA.cm^{-2})	FF (%)	Etta (%)	
684	40.05	79.6	21.80	Mean value
688	40.05	80.25	22.11	Best value

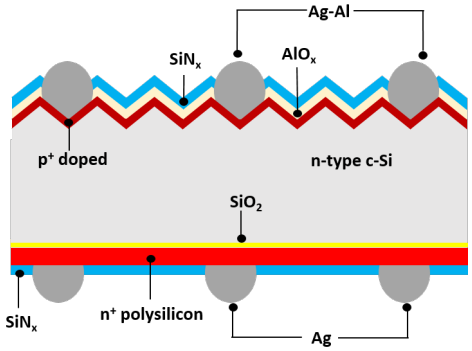

Figure 9.9: Schematic representation of the rear side polysilicon/SiO_x passivated cell.

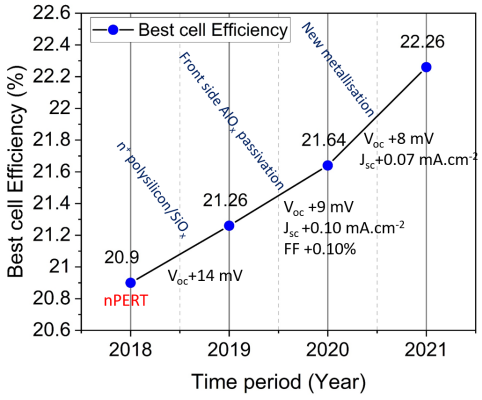

Figure 9.10: Efficiency Vs time for the best rear side n+ polysilicon/SiO_x cells fabricated in this thesis.

9

The schematic cross section of the final cell developed in the above experiments is shown in Figure 9.9. Other than the mentioned steps for fabricated the n+ polysilicon/SiO_x rear side passivated cell in Figure 9.9, the only additional step that was introduced was the PECVD AlO_x deposition with is in between step 9 and 10. The increase of the solar-cell efficiency over the years (2018-2021, time period for the development of the n+ polysilicon/SiO_x rear side passivated cell in this work) is presented in Figure 9.10. The starting efficiency of 20.9% is for the best nPERT (BiSoN) cell in the year 2018. The first jump in efficiency from the nPERT solar cell was due to the use of polysilicon/SiO_x rear contact, resulting in an increase of the V_{oc} of 14 mV, and with the fill factor remaining the same as that of the nPERT cell. In the next experiment, an AlO_x passivation layer was introduced on the front side, increasing the V_{oc} further. This increased the cell efficiency with gain of 9 mV in V_{oc}, of 0.1 mA.cm^{-2} in J_{sc} and 0.1% gain in fill factor as compared to the previous

experiment results. The final experiment described in this chapter optimised the front finger and bus-bar design, with the aim to reduce the shading losses. Silver aluminium paste was used for the front side in this experiment. Reduced shading led to a J_{sc} increase of 0.07 mA.cm^{-2}. The V_{oc} in this experiment also increased by 8 mV, due to the use of Ag-Al front side paste.

To understand how the efficiency can be increased further, we performed loss analysis on the best cell developed in the thesis (c.f. Table 9.3, 22.26% efficiency cell) using Griddler 2.5 PRO [33]. The electrical parameters obtained from Griddler (V_{oc}- 697 mV, J_{sc}- 40.23 mA.cm^{-2}, fill factor- 79.53% and efficiency of 22.3%) match well with the experimental results for the illuminated I-V curve. Figure 9.11 shows the measured illuminated I-V curve and the simulated I-V curve. The input values for the simulation are presented in Appendix B. The result from the loss analysis is presented in Figure 9.12.

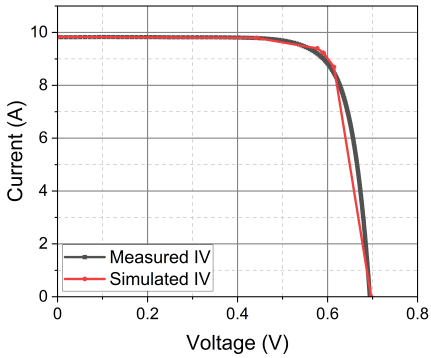

Figure 9.11: Measured and simulated I-V curve for the best rear sided n$^+$ polysilicon/SiO$_x$ cell fabricated in this thesis (Efficiency- 22.26%).

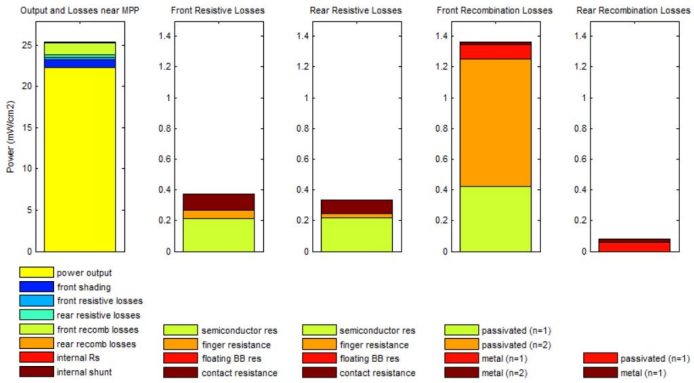

Figure 9.12: Griddler 2.5PRO loss analysis of the best rear sided n$^+$ polysilicon/SiO$_x$ cell fabricated in this thesis (Efficiency- 22.26%). Different components of the losses are mentioned in the figure.

From the results shown in Figure 9.12 it is evident that the front side recombination losses are the major contributor to the overall loss. The above figure shows the power generated by the solar cell with an incident irradiance of 100 mW.cm^{-2}. All the losses occurring are also mentioned. The major loss is the front recombination loss which accounts for almost 1.3 mW.cm^{-2}. This makes the optimisation of the front side critical in order to improve the efficiency beyond 22.26%. Improving the AlO_x passivation could be one of the strategy in order to reduce the front side recombination losses. A Griddler 2.5PRO simulation with a hypothetical cell with a low front side recombination current density of 25 fA.cm^{-2} instead of the 35 fA.cm^{-2} used for simulation of the best cell of 22.26% and a front $J_{0\mathrm{met}}$ of 200 fA.cm^{-2} instead of the 600 fA.cm^{-2}, gives a efficiency of 22.52 %, which clearly shows that improvements in the front side passivation and metallisation are critical to improve the cell efficiency.

9.3.5. Conclusion

The important conclusions from the experimental results presented in this chapter are as follows:

- The efficiency increase from nPERT cell by the use of n^+ polysilicon/SiO_x is dominated by the gain in the V_{oc}. This is due to the reduction in the recombination rate on the rear side as compared to the phosphorus diffused layers. This is also supported by the results from Chapter 6 where the n^+ polysilicon/SiO_x layer stack was compared with the phosphorus diffused layer.
- Reducing the polysilicon layer thickness to below 150 nm decreases the efficiency of the cell. There is a reduction in V_{oc} (due to increased metal recombination) and fill factor (increased contact resitivity, series resistance) when the polysilicon layer thickness is reduced. This relates directly to the results from Chapter 7.
- The reduction of the recombination rate at the boron emitter at the front is a crucial aspect in increasing the efficiency. AlO_x passivation and use of use of a different (modern) paste reduces the recombination rate at the boron emitter leading to further improvement in the V_{oc}.
- The reduction in shading losses with the use of thinner and the specially designed (tapered) busbars and fingers leads to an increase of the J_{sc} of the cell.

From the results presented in this work, the salient features of the best efficiency cells with n^+ polysilicon/ SiO_x rear side passivated layer stack are as follows:

- AlO_x layer passivation for the front boron emitter with deposition at RF power of 2250 W for 90 sec.
- n^+ Polysilicon layer with a thickness of 150 nm, with wet chemical interfacial oxide.

- 135 fingers with 16 µm screen opening with front fingers of silver-aluminium.
- 9 bus bars for front side.
- Fast firing at peak temperature of 805 °C, with belt speed of 7000 mm.min^{-1}.

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10

Conclusion

In this chapter the most important conclusions of the work presented in this thesis are summarized. It also provides an outlook for the topics studied in this thesis.

10.1. Conclusions

In **Chapter 5**, n^+polysilicon/SiO_x passivating layers were metallised with different fire-through silver pastes. Two quantities i.e. metal-polysilicon recombination current density (J_{0met}) and contact resistivity (ρ_c) are considered to be the benchmark in finding the suitable silver paste. The target in this chapter was to achieve the lowest values for both the quantities at a fast-firing temperature which is also conducive to the metallisation and passivation for the n^+ polysilicon/ SiO_x rear side passivated solar cell. The experiments in this chapter showed that the J_{0met} increases when the fast-firing peak temperature is increased. The contact resistivity values did not show a change in the investigated fast-firing peak temperature range. High resolution SEM imaging was employed to study the microstructure and the interface between the layers. A Python script was developed and utilised to correlate the damage of the polysilicon layer from the SEM images to the J_{0met} values.

The work in **Chapter 6** provides a strong argument for the use of n^+ polysilicon/ SiO_x layers in place of the phosphorus diffused n^+ layers. The study shows that the passivation level as well as the contact properties are superior for the n^+ polysilicon / SiO_x layers. In terms of the passivation an iV_{oc} of above 725 mV and a J_{0pass} below 7 fA.cm^{-2} are obtained for the samples with n^+polysilicon/ SiO_x layers as compared to the mean values of 700 mV and 25 fA.cm^{-2} for samples with a phosphorus diffused n^+ layer. The values of J_{0met} and ρ_c support the implementation of n^+ polysilicon/SiO_x layers in place of phosphorus diffused layers. From the analysis of the SEM images of the samples, we conclude that the polysilicon layer favours enhanced crystallisation of the silver as compared to the diffused silicon layers.

Influence of the thickness of the polysilicon layer on the passivation and contact properties are investigated in **Chapter 7**. This is important as an optimum thickness of polysilicon layer is required as an excessive thickness comes with increased light absorption and manufacturing costs. We studied three different kind of samples with 50, 100, 150-nm of polysilicon thickness. All the samples irrespective of their thickness achieved a mean iV_{oc} of above 735 mV and a J_{0pass} below 5 fA.cm^{-2}, which are among the best values reported at the time of experiment. The contact properties vary with the polysilicon layer thickness, with the samples having 50-nm of polysilicon layer thickness showing the highest value of J_{0met} and contact resistivity. Increasing the polysilicon thickness leads to a reduction of J_{0met} and the contact resistivity. The trend of the J_{0met} and contact resistivity is also studied as a function of the fast-firing peak temperature. Truly passivated contacts, wherein there is no additional recombination from the metallisation, with contact resistivity values below 2 mΩ.cm^2 were obtained at fast-firing peak temperature below 820 °C. The variation in J_{0met} and contact resistivity in response to the thermal budget during contact formation shows the same trends as observed in the Chapter 5 and 6. In this experiment, we studied a wide range of fast-firing peak temperature (700 to 820 °C) and at fast-firing peak temperatures below 760 °C, the contact resistivity starts to increase. This increase in contact resistivity correlates to cross-sectional SEM images that show that the number of silver crystallites in contact with the polysilicon layer decreases for fast-firing temperatures below 760 °C. Cross-sectional SEM images also show that the silver crystallites start to grow horizontally

when they come in contact with the interfacial oxide.

The surface finish of the substrate influences the passivation and contact properties of the n^+ polysilicon/SiO_x layer. This influence has been studied in detail in **Chapter 8**. Compared to textured substrates, a planar c-Si substrate has the best passivation and contact properties. The J_{0pass} and J_{0met} values of the n^+ polysilicon/SiO_x layers increase once the roughness of the substrate is increased, although the contact resistivity decreases with increased roughness. We conclude that the planar substrate is the best choice in order to reap the full benefits of the n^+ polysilicon/SiO_x based contacts, as the improvement of contact resistance with the textured surfaces does not out-weight the loss in passivation properties and J_{0met}.

In **Chapter 9** the stacks and metallisation schemes developed before are integrated into solar-cells. We use the nPERT solar cell process chain developed at ISC-Konstanz as the starting point in order to develop a high efficiency rear side n^+ polysilicon/SiO_x passivated contact cell. We achieve efficiencies above 22% with an industrial process sequence on M2 sized wafers. Loss analysis from Griddler 2.5PRO points out that the recombination losses on the emitter side are limiting the efficiency of the rear side n^+ polysilicon/SiO_x passivated contact cell.

10.2. Outlook

Based on the results presented in this thesis, the following ideas are presented for future work:

1. The advantages of using a n^+ polysilicon/SiO_x passivated contact with screen printed fire through silver paste are elaborated throughout the work. From the experiments in which the polysilicon layer thickness was varied, it is evident that reducing the thickness of polysilicon leads to high J_{0met} and contact resistivity values. From here on the paste manufacturers can work on dedicated silver paste where in thinner polysilicon layers can be utilised without increased loss in J_{0met} and contact resistivity.

2. The solar cells developed in the work can be further optimised by using novel screen printing and metallisation schemes (e.g. by further reducing the area of metal coverage). Improving the emitter passivation and metal recombination of the emitter contact was found to have the greatest leverage. Use of thinner n^+ polysilicon layer will also reduce the free carrier absorption at the rear side and further increase in short-circuit current can be expected. This is possible only if the thinner polysilicon layer can provide equivalent performance in contact and passivation quality as compared to the 150-nm thick n^+ polysilicon layers. Application for selective p^+ polysilicon/ SiO_x stacks underneath the front side fingers could also be a novel approach to reduce the recombination losses at the front side.

3. The work in this thesis involved the use of silver pastes. The cost of silver has been rising in the last years and will continue to rise due to the scarcity of silver. A good alternative to silver is copper. In terms of electrical properties,

copper is similar to silver, having a resistivity of 1.7 μΩ.cm, as compared to 1.6 μΩ.cm for silver. Copper is almost 70% cheaper than silver, thus large scale implementation is promising. Hence, it would be an interesting project on metallisation of n^+ polysilicon/SiO_x layer stacks with screen printed copper paste. Here in, the challenges would be to prevent copper mitigation into the bulk and to find a contact mechanism.

4. The high quality of passivation and high open circuit potential of the polysilicon/ SiO_x passivated contact based cells make them one of the potential candidates for use in tandem solar cell applications. This could open up possibility to develop high efficiency tandem cells especially with a top cell made of perovskite.

11

Acknowledgements

The little bird has taken wings. It feels like just yesterday that I started my PhD research. The memories are so vivid in my mind. I remember walking from my house to the lab for the first time and I saw the beautiful snow-covered Alps and was awe-struck by the sunlight reflecting from the snow. From that day onward, I always walked from my house to the lab, it took a bit longer as compared to commuting with the bicycle. For the view and the scenic beauty, I did it for four years.

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My parents and my sister have had to face the brunt of my frustrations. I talk to them almost every day and they have been patiently listening to all my problems. You have stood by me like a pillar throughout all the troubles I had in my life. My dear grandfather and my grandmother who showed me immense love and instilled in me the habit of hard work and humility deserve my special gratitude. This thesis is dedicated to you all.

A

Appendix-A

Any fool can write code that a computer can understand. Good programmers write code that humans can understand

Martin Fowler

This appendix provides the Python script used for analysing the SEM images.

A.1. Introduction

This script was used to estimate the damage to the polysilicon layer from the metallisation. The idea was to quantify the SEM images so as to clearly get an estimate of the damage to the polysilicon layer and the underneath crystalline silicon by the paste constituents. The code below was written in collaboration with Ben Kruger (University of Konstanz). The SEM images are used as an input to the script. The input images are converted to a binary image after re-scaling the pixel intensities, with a pre-defined threshold for the darkness and the size for the spots. The script then identifies the spots as circles and then computes the number of the circles. The same threshold was used for processing the images. The SEM images used as input to the script were also taken with the same input parameters. This was done to have uniform procedure for the processing of SEM images.

Listing A.1: Code for finding the spots in SEM images

```
import numpy as np
from matplotlib import pyplot as plt
from skimage import exposure
import cv2 def preprocess_to_binary (image, low_pix_value,

high_pix_value, binary_thresh):

    '''
    Converts 2D image to binary after re scaling pixel intensity
```

A

```
    image: 2D np array
    low_pix_value: pixel value below which all pixels are set to 0
    high_pix_value: pixel value above which all pixels are set to 255
    binary_thresh: number from 0 - 255, above set to 255, bellow, set to 0
    '''

    # Rescale image pixels within range
    image_rescale = exposure.rescale_intensity(
            image, in_range=(low_pix_value, high_pix_value),

            out_range=(0, 255))

    # Binarize image based on threshold
    binary_image = np.where(image_rescale < binary_thresh, 0, 255)

    return binary_image

def get_blob_info(binary_image):

    '''
Get contours from binary image. Then find center and average radius of
each contour

    binary_image: 2D image
    '''

    img, contours, hierarchy =
    cv2.findContours(binary_image.astype(np.uint8).copy(),
     cv2.RETR_TREE, cv2.CHAIN_APPROX_NONE)

    centers = []
    radii = []
    contours = [np.squeeze(contour) for contour in contours]
    for contour_ind, contour in enumerate(contours):
        # Contour is a single point
        if len(contour.shape) == 1:
            centers.append(contour)
            radii.append(1)
        else:
            centers.append(np.mean(contour, 0))
                    radii.append(np.mean(np.sqrt(np.sum((contour -
                    centers[-1]) ** 2, 1))))
    centers = np.stack(centers, 0)

    return (centers, radii)

def draw_circles_on_image(image, centers, radii, dot_size):

    '''
    Draw a bunch of circles on given image

    image: 2D or 3D image
    centers: shape(n,2) array of  circle centers
    radii: list of circle radii

    if len(image.shape) < 2:
        print('image has too few dimensions')
```

```
        return None

    if len(image.shape) == 2:
            color = 200
            print('2d image')
    else:
        if image.shape[2] == 3:
            color = (0, 0, 255)
        else:
            print('image is the wrong shape')
            return None

    for circle_ind, radius in enumerate(radii):


        cv2.circle(image, (centers[circle_ind, 0].astype(int),
        centers[circle_ind, 1].astype(int)),
                   dot_size, color, -11)

    return image
def find_holes(image, darkness_theshold=.1, size_threshold=1,
 show_images=True):
    current_image = image[:,:, 0]
    bat_thresh = darkness_theshold*255 # .15 was pretty good
    low_pix_value, high_pix_value = np.percentile(current_image,
    (50, 99.9))
    image_rescale = exposure.rescale_intensity(
            image, in_range=(low_pix_value, high_pix_value),
             out_range=(0, 255))
    binary_image = preprocess_to_binary(current_image, low_pix_value,
     high_pix_value, bat_thresh)
    centers, radii = get_blob_info(255 -
     binary_image.astype(np.uint8).copy())
    img, contours, hierarchy = cv2.findContours(255 -
     binary_image.astype(np.uint8).copy(), cv2.RETR_TREE,
     cv2.CHAIN_APPROX_NONE )

    contour_image = cv2.drawContours(image[:,:,:3].astype(np.uint8),
     contours, -1, (0,255), -1)
    # positions_list.append(bat_centers)

    contour_size_list = [contour.shape[0] for contour in contours]
    contour_size_list = np.array(contour_size_list)

    good_holes = np.squeeze(np.argwhere(contour_size_list >
     size_threshold)).astype(np.int64)

    a_centers = np.array(centers)
    a_radii = np.array(radii)

    good_centers = a_centers[good_holes]
    good_radii = a_radii[good_holes]


    circle_holes = draw_circles_on_image(image[:,:,
     :3].astype(np.uint8), a_centers[good_holes], a_radii[good_holes],
     1)
```

A

```
    if show_images:
        plt.figure(figsize=(20,20))
        plt.imshow(current_image)
        plt.figure(figsize=(20,20))
        plt.imshow(image_rescale)
        plt.figure(figsize=(20,20))
        plt.imshow(255 - binary_image)
        plt.figure(figsize=(20,20))
        plt.imshow(contour_image)
        plt.figure(figsize=(20,20))
        plt.imshow(circle_holes)
    return good_centers

image_file = '.....tif'
image = plt.imread(image_file)

hole_location = find_holes(image, darkness_theshold=.1,
 size_threshold=1, show_images=True)
print('....holes.'.format(len(hole_location)))
```

As explained in Chapter 5, this script needs to be improved in order to provide a more accurate estimate of the damage to the polysilicon layer. The shortcoming of the method explained in here, is that the script does not take into account the area of the spots. In this way we consider same effect from spots (holes in polysilicon layer) of different areas, which is not inertly true. To combat this shortcoming we have to improve the script and compute an area fraction instead of an number density. This will improve the analysis from the above script and make it more accurate.

B

Appendix-B

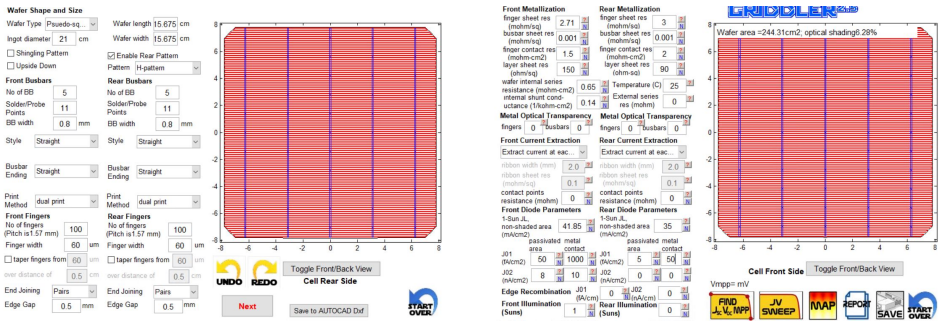
Theory provides the maps that turn an uncoordinated set of experiments or computer simulations into a cumulative exploration.

David Goldberg

This appendix provides Griddler 2.5PRO simulations of the rear side side n^+ polysilicon/ SiO_x cell, metallisation scheme [1]. Griddler 2.5PRO is a versatile tool in order to simulate solar cell[2]. The electrical parameters obtained from the simulations are verified with the experimentally obtained parameters, in order to validate the simulation results.

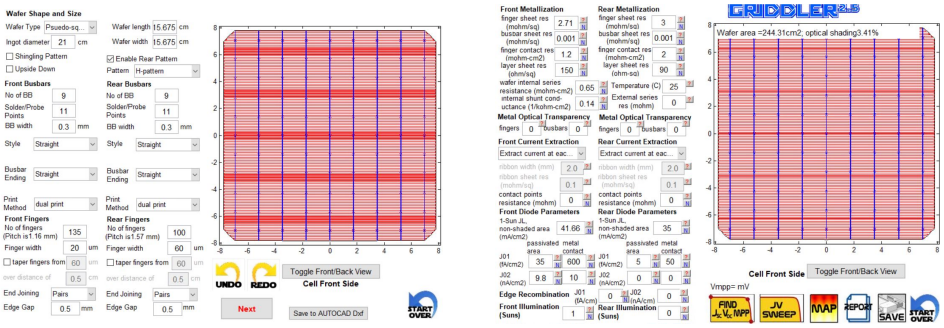
B.1. Introduction

Griddler 2.5PRO utilises a finite element model (FEM) representation of the solar cell. The solar cell in Griddler is represented by planes (1 to 8 planes), which are basically the different regions of the cell, i.e front metal grid plane, rear metal grid plane etc. In the FEM analysis the planes are broken into the triangular meshes to implement the network model for calculation of the electrical parameters. More details on the input of the simulation are shown in Figure B.1. The idea behind the simulations was to understand the effect of the metallisation.



(a) (b)

Figure B.1: The input parameters (a) the metallisation scheme and (b) electrical parameters for the cells with 5 bus-bars.



(a) (b)

Figure B.2: The input parameters (a) the metallisation scheme and (b) electrical parameters for the cells with 9 bus-bars and AlO_x layer passivation.

The inputs such as the number of fingers and bus-bars, width as well as the recombination parameters are utilised for the simulation of the cells. The recombination parameters used are from the experimental results performed in this work. First, the effect of changing the number of fingers on the solar-cell performance was investigated using these simulations. Following this first investigation, the number of bus bars was increased as well as the width of the bus bars. In addition, in these simulations the finger width was reduced from 60 to 20 µm. The error between the simulated results and the experimentally measured results of the fabricated cells was less than 5%.

B.2. Results

The first simulation involves the cell architecture with 5 floating bus-bars on the front and rear side of the rear-side n^+ polysilicon/SiO_x cell. A floating bus-bar is a screen-printed bus-bar with a low temperature silver paste which does not etch the silicon nitride layer. Hence, it is printed after the screen printing and firing of

the fingers. It is called a "dual print" in Griddler terminology. The finger width of 60 µm and the bus-bar of 800 µm width is used as the input in the simulations. The simulation results are presented in Figure B.3. The efficiency decreases with the increase in the number of front fingers, which is due to the increased shading losses as also shown in the J_{sc} results. The V_{oc} also decreases due to increase in the metal-semiconductor recombination as well as the decrease in the short circuit current due to increased shading. The increase in the fill factor due to the reduction in the series resistance cannot offset the decrease in the J_{sc} and V_{oc}.

Loss analysis pointed out that more gain can be achieved if we improved the front side passivation, hence we incorporated an AlO_x passivation layer in the later experiments to fabricate the solar cells. Motivated from the past experiments and literature we figured out that going to increased number of bus-bars and fingers with reduced width coupled with improved front side passivation is the way forward [3, 4]. The loss analysis showed that the front side recombination rate is the limiting factor, hence improving it is critical.

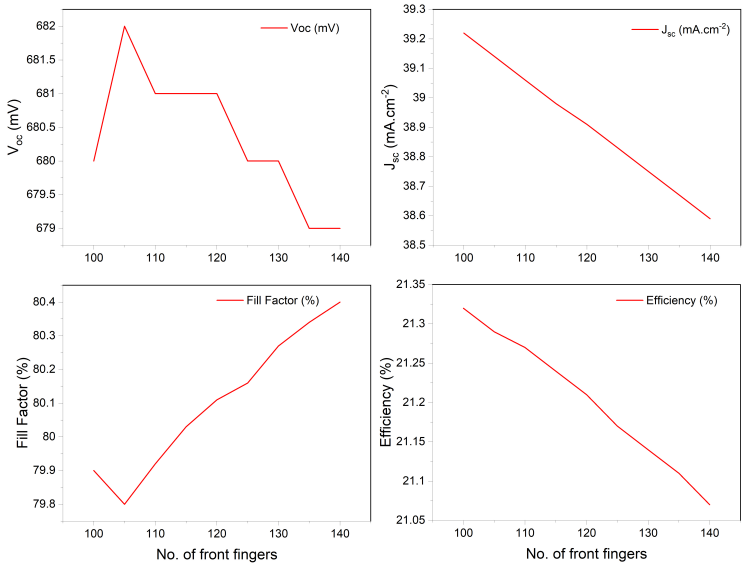


Figure B.3: Results of the external parameters as a function of the number of fingers at the front, obtained with simulations using Gridler 2.5PRO on solar cells shown in Figure B.1 : (a) open-circuit voltage, V_{oc} (V), (b) short-circuit current density, J_{sc} (mA.cm^{-2}), (c) fill factor, FF (%) and (d) conversion efficiency, η (%).

In the Figure B.4, simulation results with 9 bus-bars with 300 µm width and 20 µm thick front fingers show that the cell efficiency increases till an optimum number of front fingers and then stabilises. Hence, to further improve the efficiency, we did

loss analysis, which again pointed out that the front side recombination was limiting the efficiency. The screen manufacturer was able to produce a screen with 16 µm, which gave us a screen printed finger width of approximately 20-22 µm.

We did another set of simulations with improved front side passivation and reduced metal-semiconductor recombination current density and contact resistivity for the thinner front finger design. With a $J_{0\text{pass}}$ of 25 fA.cm^{-2} and $J_{0\text{met}}$ of 200 fA.cm^{-2} for the front side and ρ_c of 1 Ω.cm, an efficiency of 22.52 % can be obtained. With a further reduction of $J_{0\text{pass}}$ to 15 fA.cm^{-2} and $J_{0\text{met}}$ of 200 fA.cm^{-2} for the front side and $J_{0\text{pass}}$ of 2 fA.cm^{-2} and $J_{0\text{met}}$ of 10 fA.cm^{-2} for the rear side side and ρ_c of 0.5 Ω.cm an efficiency of 23.25% can be achieved, with V_{oc} of 720 mV, J_{sc} of 40.24 mA.cm^2 and fill factor of 80.27%. This points out to the potential of the M2 sized rear side side n$^+$ polysilicon/SiO$_x$ cell that can be fabricated using the procedure mentioned in this thesis.

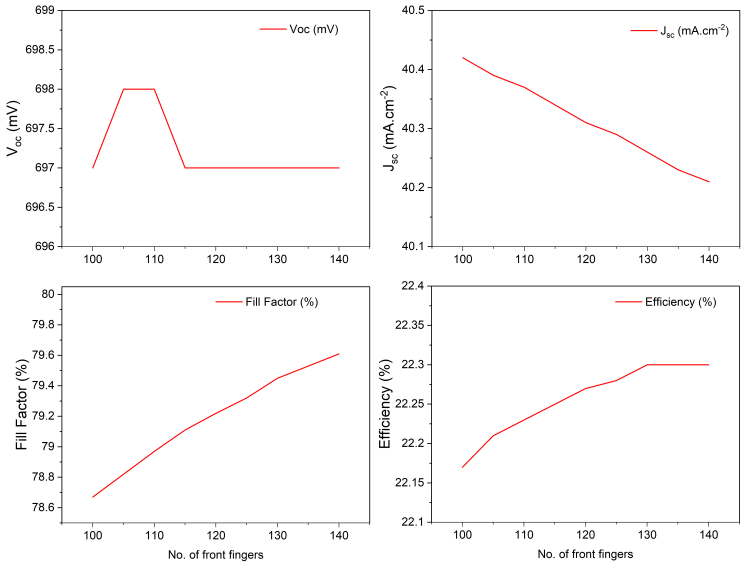


Figure B.4: Results of the external parameters as a function of the number of fingers at the front, obtained with simulations using Gridler 2.5PRO on solar cells shown in Figure B.2 : (a) open-circuit voltage, V_{oc} (V), (b) short-circuit current density, J_{sc} (mA.cm^{-2}), (c) fill factor, FF (%) and (d) conversion efficiency, η (%).

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Curriculum Vitæ

Aditya CHAUDHARY

Aditya Chaudhary studied Power Engineering at National Power Training Institute, New Delhi, India and graduated in 2014. Afterwards, he completed the Master of Science programme in Electrical Sustainable Energy at Delft University of Technology, Delft, Netherlands in the year 2017. The master thesis work involved development of four-terminal mechanically stacked a-SiO_x/c-Si solar cells and was carried out under supervision of Dr. R.A.C.M.M. van Swaaijin the research group Photovoltaic Materials and Devices headed by Prof.dr. Miro Zeman. Since January 2018, he has been working at ISC Konstanz, Konstanz, Germany, as a PhD researcher. The topic of his work is metallisation of n^+ polysilicon/SiO_x passivated contacts.

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2010–2014	NPTI (Bachelors of Technology) Power Engineering
2015-2017	Delft University of Technology (Masters of Science) Electrical Sustainable Energy *Thesis:* Development of four-terminal mechanically-stacked solar cells utilising hydrogenated amorphous silicon oxide (a-SiO_x:H) and crystalline silicon cells *Supervisor:* Dr. R.A.C.M.M. van Swaaij
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List of Publications

Journal Papers

1. **A. Chaudhary**, J. Hoß, J. Lossen, F. Huster, R. Kopecek, R. van Swaaij, and M. Zeman, Influence of polysilicon thickness on properties of screen printed silver paste metallized silicon oxide/polysilicon passivated contacts, physica status solidi (a) (2021): 2100243.

2. T. Fellmeth, F. Feldmann, B. Steinhauser, H. Nagel, S. Mack, M. Hermle, F. Torregrosa, A. Ingenito, F. Haug, A. Morisset, F. Buchholz, **A. Chaudhary**, T. Desrues, F. Haase, B. Min, R. Peibst, L. Tous, "A Round Robin - HighLiting on the Passivating Contact Technology". Epj Photovoltaics (2021), 12, p12

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Conference contributions

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