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31.3 A 0.14mm² 16MHz CMOS RC Frequency Reference with a 1-Point Trimmed Inaccuracy of ±400ppm from −45°C to 85°C

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Recently, rapid strides have been made in improving the accuracy of RC-based frequency references [1-3]. Inaccuracies better than ±500ppm from -45°C to 85°C have been achieved, but typically at the expense of a costly and time-consuming 2-point trim to compensate for RC spread and temperature dependence. This paper describes a 16MHz RC-based frequency reference that achieves ±400ppm inaccuracy over the industrial temperature range with a single room-temperature (RT) trim. The prototype draws 88μA from a 1.8V supply and occupies 0.14mm², which represents a 2× improvement in both power and area compared to the state of the art [2].

The proposed frequency reference is built around a frequency-locked loop (FLL), which locks the frequency of a digitally controlled oscillator (DCO) to the temperature-compensated phase shift of an RC filter. In previous work, a Wien bridge (WB) bandpass RC filter was used, and its temperature dependency was corrected with the help of a Wheatstone bridge (WhB) temperature sensor (Fig. 31.3.1, top) [2]. Both the WhB and the WB were read out by dedicated high-resolution ADCs, resulting in large chip area and high power dissipation. In this work, a single ADC is combined with a reconfigurable RC front-end and readout to save both chip area and power. The ADC is operated in a time-multiplexed manner, and switches between two modes: a temperature-sensing mode and a phase-sensing mode. After trimming and polynomial correction, the resulting digital values are applied to a digital loop filter, whose output drives the DCO (Fig. 31.3.1, bottom).

As shown in Fig. 31.3.1 (bottom), the WhB temperature sensor consists of three resistors: two p-poly resistors ($R_{n1,2}$ = 64kΩ, TC~-240ppm/°C) and one silicided diffusion resistor (R_p = 90kΩ, TC~3000ppm/°C). As in [4], a fixed 4-bit trim is applied to the R_p branches to compensate for process spread. To reduce area and minimize the number of components that contribute to spread, the RC filter is realized by combining a single MIM capacitor (C_{lpf} = 5pF) with the R_n branches of the WhB. The result is a lowpass filter (LPF), whose phase shift is determined by a single RC time constant. Compared to WBs, whose phase response is determined by two separate RC time constants, the use of an LPF is a promising way to achieve better inaccuracy after a 1-point trim. Since the outputs of the WhB sensor and the phase-shift of the LPF vary in a similar manner over the target temperature range (-45°C to 85°C), good accuracy can be achieved with a 4th-order temperature-compensating polynomial. Furthermore, since the p-poly resistors are shared, their spread affects both the LPF and the WhB in a correlated manner, which reduces the spread of the temperature-compensated phase-shift of the LPF.

The reconfigurable ADC is based on a continuous-time 2nd-order ΔΣM, as shown in Fig. 31.3.2. In the temperature sensing mode, ϕ_{ch_lpf} is disabled, and the ΔΣM employs a 1-bit resistive DAC made from p-poly resistors (like the R_n branches) to force the average input current of the integrator to zero. As in [4], a return-to-CM switching scheme is employed, which reduces the supply current drawn by the DAC, thus increasing the modulator's energy efficiency and maximizing its temperature-sensing sensitivity. The 1/*f* noise and offset of the 1st integrator are suppressed by chopping it at the sampling frequency (f_s = 500kHz). In the phase-sensing mode, ϕ_{ch_whb} is frozen, and the phase DAC drives the LPF with a 500kHz square wave (ϕ_{drive}). A chopper, controlled by ϕ_{ch_lpf}, then demodulates the LPF phase shift to DC using the phase references $\phi_{0,1}$ (-45°±5.625° w.r.t to ϕ_{drive}) selected by the bitstream (Fig. 31.3.3 top). It also mitigates the 1st integrator's offset and 1/*f* noise by up-modulating them to 500kHz. As in [4], an area-efficient switched-capacitor 2nd integrator is used.

As shown in Fig. 31.3.2, the DCO is implemented using a 3-stage inverter-based ring oscillator. To suppress its spread over PVT, the inverters are loaded by RC lowpass filters, such that the free-running frequency is around the designed 16MHz at the typical corner. To ensure a sufficiently wide DCO tuning range as well as sufficient resolution, a coarse-fine architecture is utilized: a 4-bit coarse capacitive DAC provides a tuning range of ±40%, while a ±10% range of the fine 1-bit ΔΣ DAC is provided by a MOS-varactor [3]. To suppress the ΔΣ DAC's quantization noise, a 3-stage RC lowpass filter is employed.

To suppress their quantization-noise, the bitstream outputs of both sensing modes are decimated by a cascaded integrator–comb filter with a decimation factor of 1024. Each sensing mode consists of 5 decimation cycles for proper settling. As shown in Fig. 31.3.3 (bottom), a 4th-order polynomial maps the WhB output (μ_{whb}) to the LPF output and corrects its temperature dependence before the next cycle. The compensated output is then driven to zero by the FLL's digital integrator, locking the output of the DCO (f_{dco}) to the desired temperature-independent frequency. Due to the time-multiplexing scheme, the integrator's update rate is ~49Hz, which is fast enough to compensate for ambient temperature variations [5].

The prototype was fabricated in a standard 0.18μm CMOS process and packaged in ceramic DIL (Fig. 31.3.7). It has an active area of 0.14mm² and draws 88μA from a 1.8V voltage supply (LPF/WhB unit, ΔΣM, DCO, and the biasing circuit). Figure 31.3.4 (left) shows the PSD of the bitstream output of the ΔΣM in the WhB and LPF sensing modes. Using an external 16MHz reference clock, the performance of both modes was characterized over temperature. As expected, the temperature dependence of the LPF phase-shift is quite low (~-240ppm/°C), and its non-linearity is similar to that of the WhB output (Fig. 31.3.4, right). As a result, most of the frequency error can be removed by applying a 1-point offset trim to the outputs of both the WhB and LPF at room temperature. Since the WhB and the LPF are implemented on the same die, this trim is quite robust to ambient temperature variations [2].

After a 1-point trim, open-loop measurements show that the estimated frequency error due to the LPF alone is about ±520ppm (Fig. 31.3.5, top left), while the error due to the WhB alone is about ±470ppm (Fig. 31.3.5, top right). Since the p-poly resistors are shared by both bridges, these errors are somewhat correlated, which reduces the error after the loop is closed. 18 chips were characterized from −45°C to 85°C with the frequency-locked loop closed. After an individual 1-point trim at 25°C and a fixed 4th-order polynomial nonlinearity correction, the proposed frequency reference achieves an inaccuracy of ±400ppm, as shown in Fig. 31.3.5, bottom left, which corresponds to a residual TC of 5.2ppm/°C (box method). By applying a 2-point trim at -25°C and 75°C and a fixed 5th-order polynomial non-linearity correction, the inaccuracy can be improved to ±200ppm. The RMS period jitter of the DCO alone is 10.3ps, while the closed-loop result is 10.2ps. The Allan Deviation of the DCO alone is around 90ppm, which improves to 0.35ppm in the closed-loop configuration (Fig. 31.3.5, bottom right).

Figure 31.3.6 summarizes the performance of the proposed RC frequency reference and compares it to other high-accuracy designs that achieve <10ppm/°C residual TC. Compared to [2], the proposed frequency reference achieves comparable accuracy after a 1-point trim at room temperature, as well as better energy and area-efficiency. This makes it highly compatible with IoT and wireline applications that require good accuracy and a high level of integration.

Acknowledgments:
The authors would like to thank Z. Chang for his help with the measurements.

References:

[1] Ç. Gürleyük et al., "A CMOS Dual-RC Frequency Reference with ±200-ppm Inaccuracy from -45°C to 85°C", *IEEE JSSC*, vol. 53, no. 12, pp. 3386-3395, Dec. 2018.
[2] Ç. Gürleyük et al., "A 16MHz CMOS RC Frequency Reference with ±400ppm Inaccuracy from -45°C to 85°C After Digital Linear Temperature Compensation," *ISSCC*, pp. 64-65, Feb. 2020.
[3] A. Khashaba et al., "A 34μW 32MHz RC Oscillator with ±530ppm Inaccuracy from -40°C to 85°C and 80ppm/V Supply Sensitivity Enabled by Pulse-Density Modulated Resistors," *ISSCC*, pp. 66-67, Feb. 2020.
[4] S. Pan and K. A. A. Makinwa, "A Wheatstone Bridge Temperature Sensor with a Resolution FoM of 20fJK²", *ISSCC*, pp. 186-187, Feb. 2019.
[5] S. Zaliasl et al., "A 3 ppm 1.5 × 0.8 mm ² 1.0 μA 32.768 kHz MEMS-Based Oscillator," *IEEE JSSC*, vol. 50, no. 1, pp. 291-302, Jan. 2015.
[6] G. Zhang et al., "A 3.2ppm/°C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting Technique", *IEEE Symp. VLSI Circuits*, pp. C126-C127, 2017.

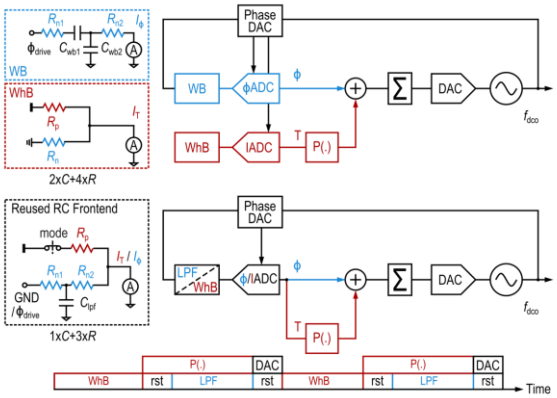

Figure 31.3.1: Simplified (single-ended) block diagram of a conventional dual-channel frequency reference (top); the proposed frequency reference with the time-multiplexing scheme (bottom).

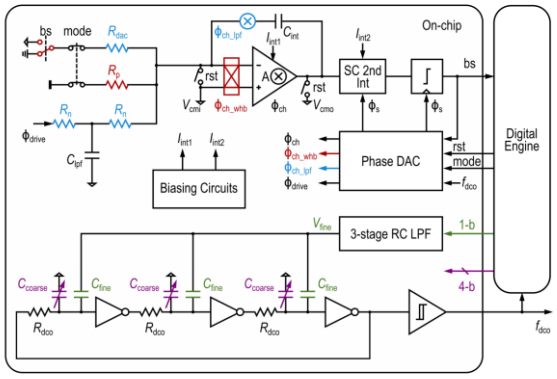

Figure 31.3.2: Simplified (single-ended) circuit diagram of the proposed frequency reference.

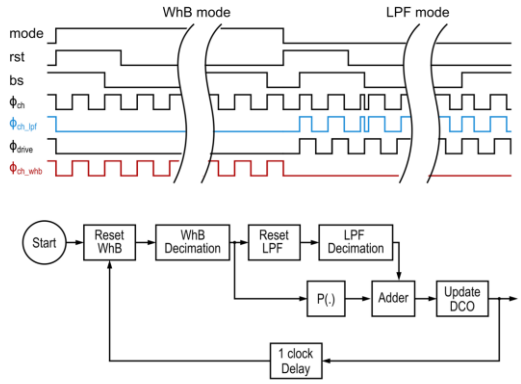

Figure 31.3.3: Timing diagram of Phase DAC (top) and Flow Chart of the Digital Engine (bottom).

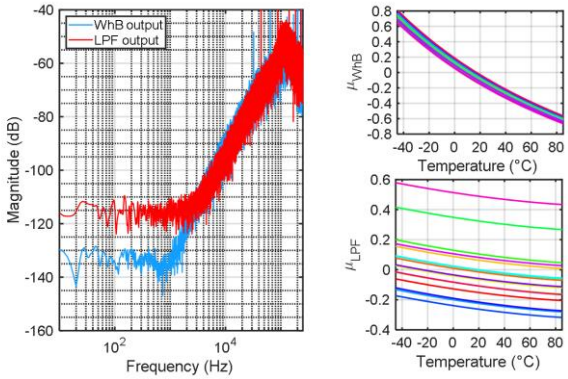

Figure 31.3.4: Measured PSD of the ΔΣM in WhB and LPF modes (left); measured bitstream averages μ_{LPF} (top right) and μ_{WhB} (bottom right) over temperature.

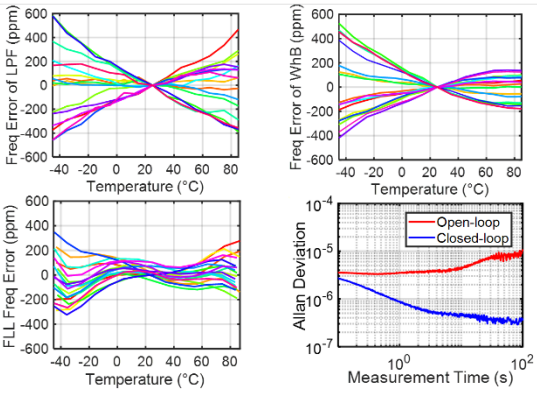

Figure 31.3.5: Estimated residual frequency error due to measured μ_{LPF} (top left) and μ_{WhB} (top right), measured frequency error after a 1-point trim and 4th systematic non-linearity correction (bottom left), and Allan Deviation (bottom right) in closed-loop and open-loop configurations.

	This Work	Gurleyuk [2] ISSCC'20		Khashaba [3] ISSCC'20	Gurleyuk [1] JSSC'18	Zhang [6] JSSC'18
Process (nm)	**180**	180		65	180	180
Area (mm^2)	**0.14**	0.3		0.18	1.65	0.17
Frequency (MHz)	**16**	16		32	7	24
Norm. Inaccuracy (ppm)	**±400**	±400	±100	±530	±170	±215
# of Trimming Points	**1+Batch (4th order)**	2	2+Batch (6th order)	2	2+Batch (4th order)	3
Temperature Range (°C)	**-45 to 85**	-45 to 85		-45 to 85	-45 to 85	-40 to 150
Supply Range (V)	**1.6 to 2.0**	1.6 to 2.0		1.1 to 3.3	1.7 to 2.0	1.8 to 5.0
Supply Sensitivity (%/V)	**0.2**	0.12		0.008*	0.18	0.01
# of Samples	**18**	20		6	8	1
Allan Deviation (ppm)	**0.35**	0.32		2.5	0.33	-
Power (μW)	**158.4**	400		34	750	200

* with on-chip LDO.

Figure 31.3.6: Performance summary and comparison with the state of the art.

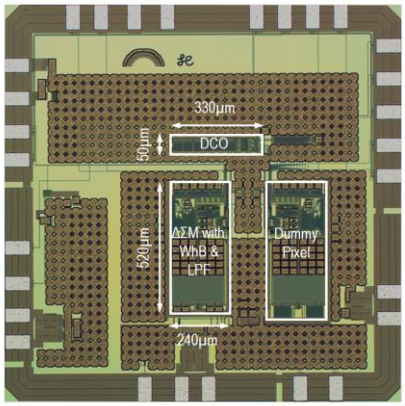

Figure 31.3.7: Die micrograph of the fabricated chip.