A Dynamically Reconfigurable Recursive Switched-Capacitor DC-DC Converter with Adaptive Load Ability Enhancement

By

Qi Lu

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Author

Qi Lu

Student Number

5376939

Thesis Committee Members

Dr. Ir. Nick van der Meijs
Dr. Sijun Du

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Abstract

Multiple voltage conversion ratio (VCR) recursive switched-capacitor (SC) DC-DC converters, based on a number of basic 2:1 converters, are widely used for on-chip power supplies due to their flexible VCRs for higher energy efficiency. However, conventional multi-VCR SC converters usually have one or more 2:1 converters unused for some VCRs, which results in lower power density and chip area wastage. This paper presents a new recursive DC-DC converter system, which is able to dynamically reconfigure the connection of all on-chip 2:1 converter cells so that the unused converters in conventional designs can be re-used in this new architecture for increasing the load-driving capacity, power density and power efficiency.

To validate the design, a 4-bit-input 15-ratio system was designed and fabricated in a 180-nm BCD process, which can support a maximum load current of 0.71 mA and achieve a peak power efficiency of 93.1% with 105.3 μA/mm^2 chip power density from a 2 V input power supply. The measurement results show that the load-driving capacity can become 6.826×, 2.236× and 2.175× larger than the conventional topology when the VCR is 1/2, 1/4 and 3/4, respectively. In addition, the power efficiency under these specific VCRs can also be improved considerably.

1 Introduction

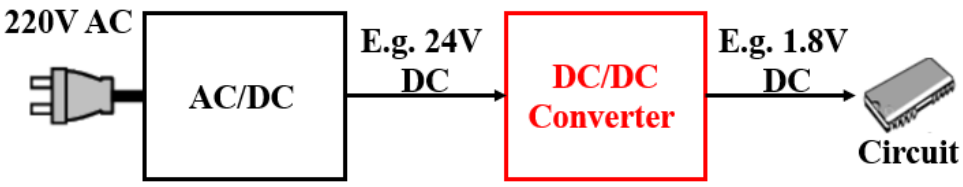

Figure 1: DC-DC

In recent society, electrical devices have become an indispensable part of people's daily life. All electrical devices need DC power supply to work. The usual mains power is 220 V AC which cannot be used directly for devices. AC/DC converters are usually used to convert it into a high voltage DC power supply (E.g. 24 V), but this DC voltage still cannot be used for electrical devices because it will exceed the safety voltage limitation of electrical appliances and break them down. At this time, a DC/DC converter is necessarily to be used to convert the high DC voltage into a low DC voltage (E.g. 1.8 V), which is suitable for electrical devices' work.

1.1 DC-DC converter

DC/DC converter is a voltage converter that converts an input voltage and efficiently outputs a fixed voltage. DC/DC converters are divided into three categories: step-up DC/DC converters, step-down DC/DC converters, and buck-boost DC/DC converters. Commonly used types of DC-DC converter are low-dropout regulator, inductor-based buck/boost converter and switched-capacitor converter, which will be introduced separately as below.

1.1.1 Low-dropout regulator (LDO regulator)

A low-dropout regulator (LDO regulator) is a DC linear voltage regulator (Which can only be used in step-down applications) that can regulate the output voltage even when the supply voltage is very close to the output voltage. Its main components are a controllable

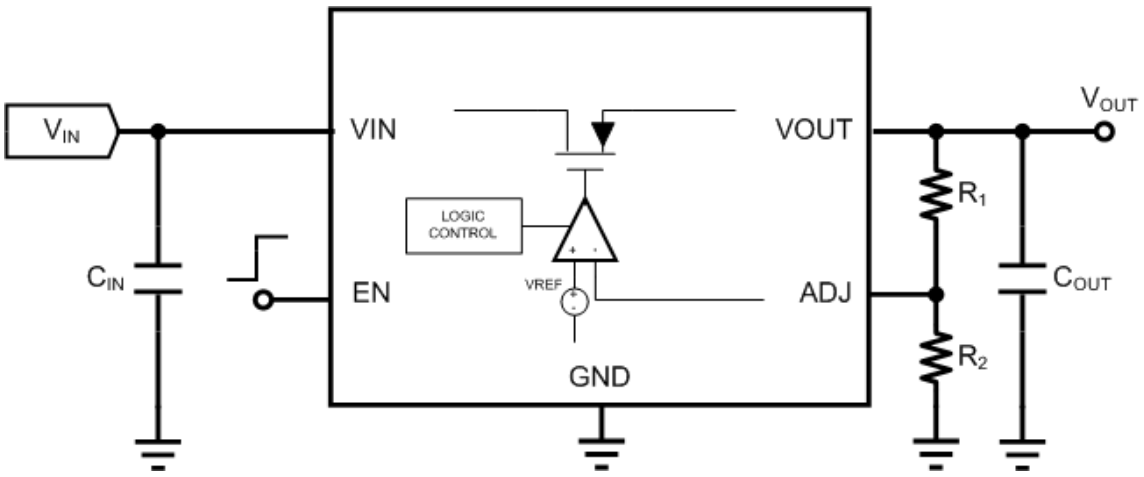

Figure 2: Low-dropout regulator (LDO regulator)

power MOSFET and a differential amplifier (error amplifier). One input of the differential amplifier monitors the fraction of the output V_{out} determined by the resistor ratio of R_1 and R_2. The second input to the differential amplifier is from a stable voltage reference V_{ref} (bandgap reference). The working principle is: The sampled output V_{out} will be compared with the reference voltage V_{ref} in the error amplifier, the difference between these two voltages is amplified to control the voltage drop V_{DS} of the power MOSFET, thereby stabilizing the output voltage. When the output voltage V_{out} decreases, and the difference between the reference voltage V_{ref} and the sampling voltage V_{out} increases, the drive current output by the error amplifier increases, and the voltage drop V_{DS} of the power MOSFET decreases, thereby increasing the output voltage, vice versa. The output voltage will be finally stabilized as a constant value determined as Eq.(1).

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} \tag{1}$$

The energy efficiency of LDO can be calculated as $\eta = V_{out}/V_{in}$, it can be found that when the voltage difference between V_{in} and V_{out} is large, the energy efficiency will be very low, which is unacceptable in the power converter system.

1.1.2 Inductor-based Buck/Boost DC-DC converter

In order to achieve high efficiency power conversion, a popular energy storage element-inductor is used in DC-DC converter design, that is, an inductor-based buck/boost converter. This part will only introduce the principle of a buck converter working in continuous mode as shown in Fig.3.

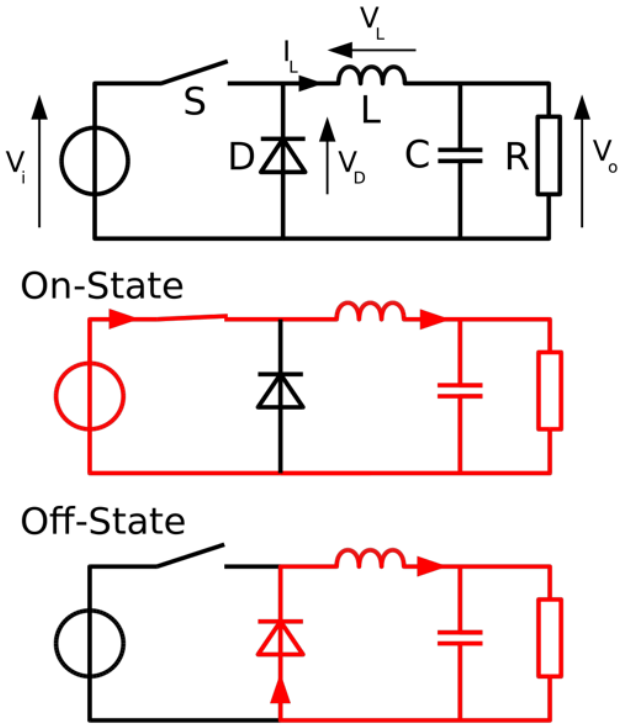

Figure 3: Buck converter

Buck converters operate in continuous mode if the current through the inductor I_L never falls to zero during a whole period T. When the switch is closed (On-state), the voltage across the inductor is $V_L = V_{in} - V_{out}$. The current through the inductor I_L rises linearly (in approximation, so long as the voltage drop is almost constant). As the diode is reverse-biased now, no current flows through it; When the switch is opened (Off-state), the diode is forward-biased. The voltage across the inductor is $V_L = -V_{out}$ (neglecting diode drop). Current I_L decreases. The energy stored in inductor L is $E_L = 0.5LI_L^2$. It can be seen that the energy stored in inductor L increases during on-time as I_L increases and then

decreases during the off-state. L is used to transfer energy from the input to the output of the converter. In the steady state, the energy stored in the inductor L at the end of a operation period T is equal to that at the beginning of the period. That means the current $I_L(0) = I_L(T)$. Based on this, the output voltage can be determined as Eq.(3):

$$V_{out} = DV_{in} \tag{2}$$

Where D is the duty cycle of the period (On-state time $T_{on} = DT$, Off-state time $T_{off} = (1-D)T$).

The inductor-based buck converter can achieve over 90% energy efficiency and drive a very large load current, which is preferred over a long time in DC-DC converter design. However, with the development of integrated circuits, people's requirements for the miniaturization of electronic equipment are increasing day by day, and fully integrated power conversion systems have been favored by designers because of their smaller area, lower IR drops and Ld_i/d_t drops in the package. In this case, the performance exhibited by the inductor in fully on-chip integration is not satisfactory due to: 1) On-chip inductive converters require high-Q inductor for good efficiency, necessitating special masks and increasing manufacturing costs [5]. 2) Integrating the inductor will introduce large inductor's parasitic resistance, parasitic capacitance between the inductor and the silicon substrate, and also the skin effect in the windings [6], [7], [2]. 3) Since inductor-based converter requires complex control systems, when supplying low power loads, the load power scaling is challenging, which limits the power efficiency.

1.1.3 Switched-capacitor DC-DC converter

Capacitor, as another energy storage element, is introduced to the fully integrated DC-DC converter design to overcome the disadvantage of inductor integration. The working principle of the most widely used topology 2:1 Dickson step-down SC converter will be explained briefly here.

Switched-capacitor DC-DC converter usually works in 2 interleaved phases: charging phase $\phi 1$ and discharging $\phi 2$. With the 50% duty cycle operation shown in Fig.4, during

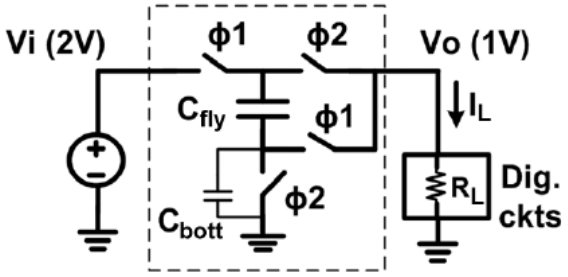

Figure 4: Dickson 2:1 step-down converter [1].

the charging phase $\phi 1$, the flying capacitor C_{fly} is connected between the input V_{in} and the output V_{out} ($V_{C_{fly}} = V_{in} - V_{out}$). The charge drawn from V_{in} will charge this capacitor up and flow to the output. In the discharging phase $\phi 2$, C_{fly} is connected between output V_{out} and ground V_{SS} ($V_{C_{fly}} + V_{SS} = V_{out}$), and thus the charge previously stored on the flying capacitor is transferred to the output. The overall output voltage will be $V_{out} = 0.5V_{in}$, realizing the 2:1 voltage step-down function. (The detailed analysis of the 2:1 SC converter will be given in the section.3.1.1)

Capacitor-based DC-DC converter has shown better performance (low parasitic factors and easy power scaling) and it has been proved that this kind of DC-DC converters are able to achieve better power conversion efficiencies (almost 100% ideally) than inductive converters in fully integrated design [8], [9]. Hence, switched-capacitor (SC) power converters have successfully emerged as the best candidate to become the next generation of fully integrated on-chip power converter.

However, traditional SC converter topologies (with fixed voltage conversion ratio) are only efficient at discrete ratios of input to output voltages which will constrict efficient dynamic voltage scaling (DVS) to a small voltage range [10]. For example, in the SoC system shown in Fig.5, many modules require different supply voltages. If only a fixed voltage conversion ratio SC converter (E.g. VCR=5/2, the output voltage is 1.32 V) is used to power all modules, only the MEM-2 module (1.2 V) has the best conversion efficiency, and the efficiency of MEM-1 and Processor will decrease dramatically. To optimize the overall efficiency of the power management system, several converters with different VCRs need to be used in this situation, resulting in design complexity and control

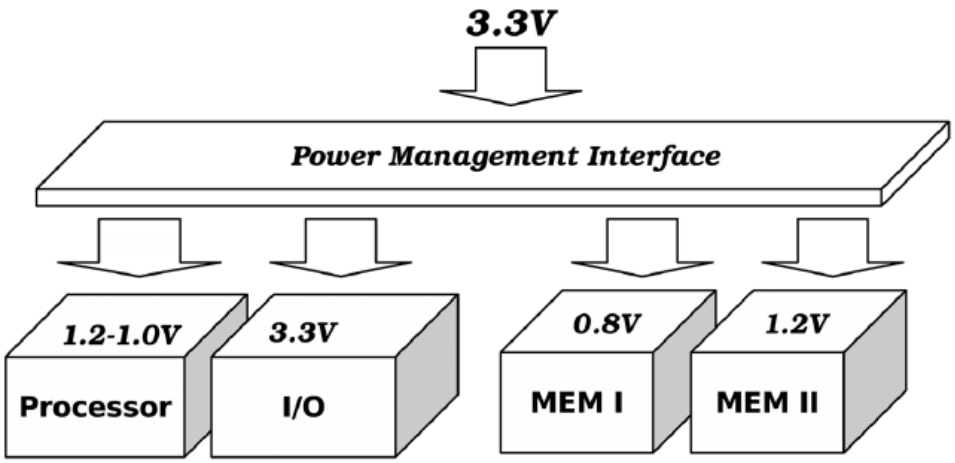

Figure 5: SoC power management [2].

logic complexity. Also, in a real case, the battery will degrade slowly, with a fixed-VCR converter, the output voltage might not be able to reach the required voltage after a period of time. So designing a circuit that can offer multiple voltage conversion ratios is necessary.

One way to realize that is by combining traditional fixed-VCR topologies into one circuit (E.g. Combining 4:1 topology and 3:1 topology to offer 2 VCRs by sharing flying capacitors and power switches). However, this will result in increased system complexity, power consumption, and extra switching elements [5]. In recent years, some pioneering multi-VCR topologies based on multiple cascaded 2:1 converters have been invented. These types of multi-VCR topology have a simple circuit structure and could provide high efficiency over a wide output voltage range, with a very high output voltage resolution. 2 constructive designs will be introduced in the next section ”state of the art”.

1.2 State of the art of Multi-VCR designs

1.2.1 Successive approximation SC converter

In 2013, Suyoung Bang in [4] proposed a Successive approximation (SAR) SC DC-DC converter that allows for fine output voltage control to enable effective load and line regulation in ultra-low power applications. Fig.6 explains the conceptual operation of

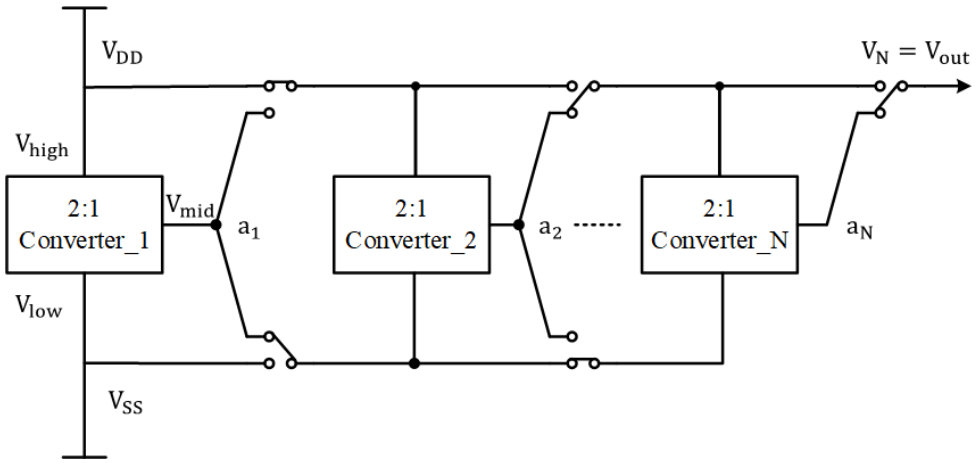

Figure 6: Successive approximation SC [3].

this converter. The central idea is to cascade multiple 2:1 SC stages using configuration switches to obtain a fine-grain output voltage (V_{out}). Each SC stage takes two inputs (V_{high}, V_{low}) and produces an output $V_{mid} = (V_{high} + V_{low})/2$. The ($V_{high}$, V_{low}) inputs of a stage are connected through configuration switches to either (V_{high}, V_{mid}) or (V_{mid}, V_{low}) of the previous stage. And the voltage conversion ratio V_{out}/V_{in} under no load could be determined as Eq.(3) below:

$$\frac{V_{out}}{V_{in}} = \frac{A+1}{2^N} \tag{3}$$

Where A is a N-bit binary control signal and $A = \{a_1, a_2, ..., a_N\}$.

In a 3-stage SAR example with VCR=5/8, the battery voltage $V_{DD} = 2\,\text{V}$ is converted to $V_{out} = V_{DD}(100_2 + 1)/2^3 = 1.25\,\text{V}$ with configuration control $A = \{a_1, a_2, a_3\} = 100_2$. $a_1 = 1$ means the mid-voltage of the first 2:1 stage $V_{mid,1}$ is connected to the low-voltage of the second 2:1 stage $V_{low,2}$, $V_{low,2} = V_{mid,1} = (V_{DD} + V_{SS})/2 = 1\,\text{V}$, and the high-voltage of the second stage $V_{high,2}$ is connected to the battery voltage, $V_{high,2} = V_{DD} = 2\,\text{V}$. So now the mid-voltage of the second 2:1 stage becomes to $V_{mid,2} = (V_{high,2} + V_{low,2})/2 = 1.5\,\text{V}$. For $a_2 = 0$, the mid-voltage of the second 2:1 stage $V_{mid,2}$ is connected to the high-voltage of the third 2:1 stage $V_{high,3}$, $V_{high,3} = V_{mid,2} = 1.5\,\text{V}$, and the low-voltage of the third stage $V_{low,3}$ is now connected to low-voltage of the second 2:1 stage $V_{low,2}$, $V_{low,3} = V_{low,2} = V_{mid,1} = 1\,\text{V}$. So now the mid-voltage of the third stage is $V_{mid,3} = (V_{high,3} + V_{low,3})/2 =$

1.25 V. In this case, the third stage is the last stage, so $a_3 = a_N = 0$ means the output node is connected to the mid-voltage of the third stage, then $V_{out} = V_{mid,3} = 1.25\,\text{V}$. Similarly, when VCR=6/8, the battery voltage $V_{DD} = 2\,\text{V}$ can also be converted to $V_{out} = V_{DD}(101_2 + 1)/2^3 = 1.5\,\text{V}$ with configuration control $A = \{a_1, a_2, a_3\} = 101_2$, therefore providing a 250 mV output voltage step (no load condition).

Hence, the key benefit of the successive approximation (SAR) SC converter is generating $(2^N - 1)$ voltage conversion ratios through one simple circuit structure and having a very fine V_{out} resolution over a wide output voltage range while maintaining similar efficiency (65%-70%) [3]. The output voltage resolution is $V_{DD}/2^N$. (N is the cascaded 2:1 stage number). However, the SAR SC converter will suffer from the cascaded losses due to the linear cascading of stages, limiting overall power efficiency.

1.2.2 Recursive SC converter

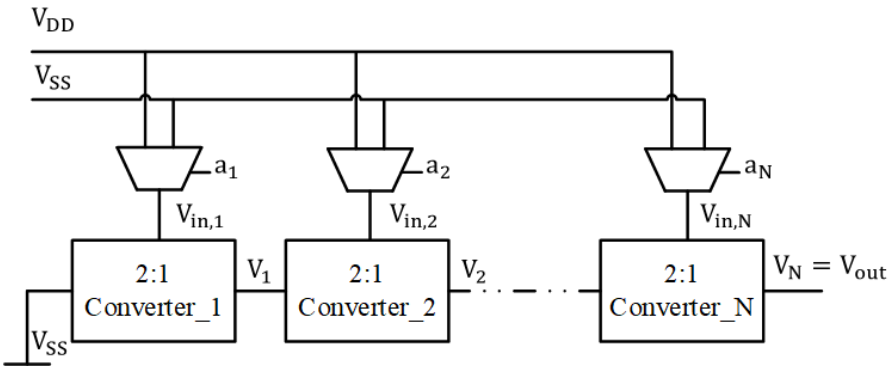

Figure 7: Recursive SC [4]

To improve the cascaded losses, in 2014 Loai G. Salem of [4] introduced a recursive switched capacitor (RSC) DC-DC converter topology that achieves high efficiency across a wide output voltage range by also providing $(2^N - 1)$ conversion ratios using N 2:1 SC cells with minimal hardware overhead as shown in Fig.7. In this binary recursive SC converter, each 2:1 SC converter stage receives one input from the previous stage's output, and the other from a power supply rail, either V_{DD} or V_{SS} (The most important difference between this design and the SAR SC converter). Since each 2:1 converter has 1/2 voltage

gain from input to output, changing supply voltage at a stage far away from the output has an exponentially smaller impact than ones near the output, resulting in binary ratio tuning [11]. The VCR can be obtained as Eq.(4).

$$\frac{V_{out}}{V_{in}} = \frac{A}{2^N} \tag{4}$$

Where A is also a N-bit binary control signal but the order of the bit is now inversed as $A = \{a_N, ..., a_2, a_1\}$ here.

Also taking a 3-stage RSC example with VCR=5/8, the battery voltage keeps the same as $V_{DD} = 2\,\text{V}$. It will be converted to an output voltage $V_{out} = V_{DD}(101_2)/2^3 = 1.25\,\text{V}$ with configuration control $A = \{a_3, a_2, a_1\} = 101_2$. Compared with the SAR SC converter, the control of this RSC topology is much more simple. When the control signal $a_1 = 1$, the input voltage of the first 2:1 stage $V_{in,1}$ will be selected as V_{DD} in the MUX, so the output voltage of the first stage will be $V_1 = (V_{in,1} + V_{SS})/2 = 1\,\text{V}$. For $a_2 = 0$, the input of the second 2:1 stage $V_{in,2}$ will be selected as ground V_{SS}, then the output of the second voltage is $V_2 = (V_{in,2} + V_1)/2 = 0.5\,\text{V}$. The third 2:1 stage is the last stage, $a_3 = a_N = 1$ means the input voltage $V_{in,3}$ is V_{DD} now, therefore the output voltage becomes $V_{out} = V_3 = (V_{in,3} + V_2)/2 = 1.25\,\text{V}$, realizing the 5/8 voltage conversion ratio.

When evaluating the efficiency performance of the converter system, the charge flowing through each flying capacitor needs to be known. Here taking a 4-stage SAR and RSC SC converter with VCR=11/16 as an example to analyze the charge distribution in each 2:1 converter stage.

In Fig.8(a) the SAR SC converter, the last stage converter_4's flying capacitor $C_{fly,4}$ loads half of the output charge $q_{out}/2$ on the third stage converter_3's output, therefore $C_{fly,3}$ will load $q_{out}/4$. Then the charge loaded on the output of the second stage will be the sum of $C_{fly,4}$ and $C_{fly,3}$, so $C_{fly,2}$ will load $3q_{out}/8$. Similarly, the first stage $C_{fly,1}$ will load $5q_{out}/16$.

In contrast, the RSC converter employs the configuration shown in Fig.8(b), where the one input voltage of these 4 2:1 converter stages is directly connected to the battery voltage V_{DD} or the ground V_{SS}. Therefore, the charge distribution is fixed in this topology, the loaded charge on $C_{fly,1}$ to $C_{fly,4}$ will be $q_{out}/16$, $q_{out}/8$, $q_{out}/4$ and $q_{out}/2$,respectively.

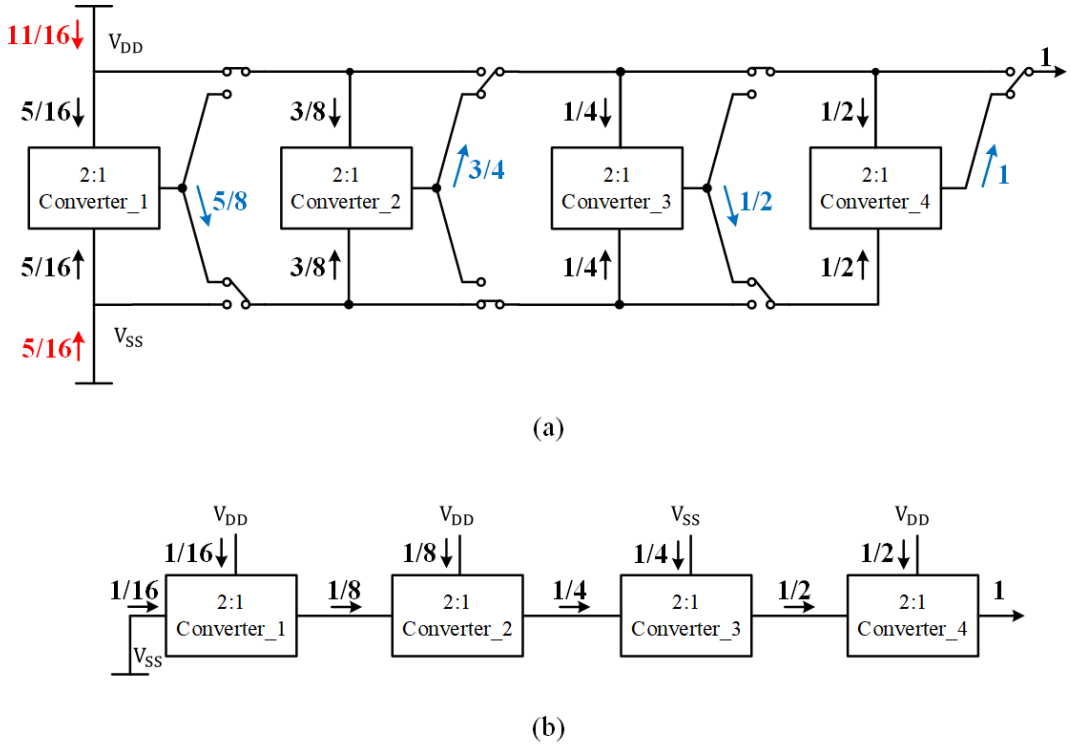

Figure 8: Charge distribution in 4-stage (a) SAR and (b) RSC SC converter

For the N-stage RSC converter, each flying capacitor $C_{fly,i}$ in each stage is loaded with a charge q_i that is divided by a binary weight of the total output charge, q_{out}, such that $q_i = q_{out}/2^N$, where i is the stage order in the cascaded system.

The important intrinsic power loss that will significantly affect the power efficiency is due to the charge sharing loss of all flying capacitors, which is proportional to the charge flowing through that capacitor. According to the analysis of charge distribution before, by maximizing the number of connections to the power supply V_{DD} and V_{SS}, the RSC topology minimizes the total charge (much smaller than that of SAR SC converter) transferred through the flying capacitors, and thus minimizes the cascaded losses, resulting in an 85% peak efficiency and greater than 70% power efficiency over a wide output voltage range.

1.3 Research Questions

The aforementioned Multi-VCR topologies can be employed in the modern System-on-Chips (SoC) and Internet-of-Things (IoT) devices to solve multi-power supply requirements and the battery degradation problem, then extend the battery lifetime. However, these 2 multi-VCR converter topologies based on 2:1 converter all share a common problem: in some specific voltage conversion ratios, the 2:1 converter cells in the circuit are not fully utilized. As a result, load-driving ability, power density, and power efficiency are limited. Taking the recursive SC converter topology and the commonly used VCR=1/2 condition as an example, only the N-th converter cell operates whereas the remaining $(N-1)$ converters are not in use. To address this problem, this paper proposes a novel topology to make full use of every on-chip 2:1 converter in different VCRs. The connection of all on-chip 2:1 converters can be dynamically reconfigured, which means the unused converters in conventional RSC designs can be re-used and no converter cell is wasted. The proposed converter has been designed and fabricated in a 180-nm BCD process. The measurement results show the dramatically increased load-driving capability and improved power conversion efficiency under certain VCRs.

1.4 Thesis Outline

This article is organized as follows:

Chapter 2 gives the operation principle of the proposed system, the energy loss mechanism and the power transfer efficiency.

Chapter 3 aims to gradually present the detailed implementation of building blocks and highlights the theoretical analysis results of single 2:1 converter and the total RSC converter system.

Chapter 4 provides the measurement results for the implemented design with emphasis on the energy efficiency and load-driving capacity. Also the performance of this design compared with state of the art multi-VCR SC converters is also presented in this section.

Chapter 5 illustrates the conclusions and gives some valuable ideas of this design to get further improved in the future.

2 Proposed Topology

2.1 Operation Principle

Table 1: Reconfigurable VCR number of different cascaded stages

Cascaded Number (N)	VCR number	Reconfigurable VCR Number
1	1	0
2	3	1
3	7	1
4	15	3
...	...	...
N	$2^N - 1$	$2^{int(N/2)} - 1$

* int means round down.

This proposed topology aims to reconfigure the cascaded recursive converter topology into a paralleled converter circuit to make full use of every single 2:1 converter stage. That means the more cascaded converter stages there are, the more VCR can be dynamically reconfigured. The relationship between the cascaded stage number and the reconfigurable VCR number is presented in Table 1. For N cascaded stages, the reconfigurable VCR number could be generalized as Eq.(5) shown below.

$$RVN = 2^{int(N/2)} - 1 \tag{5}$$

Taken a four-stage cascaded recursive SC converter as an example, according to Table 1, three VCRs can be dynamically reconfigured, which are VCR=1/2, 1/4 and 3/ 4 respectively. In these 3 specific VCRs in conventional RSC converters, only the last one stage

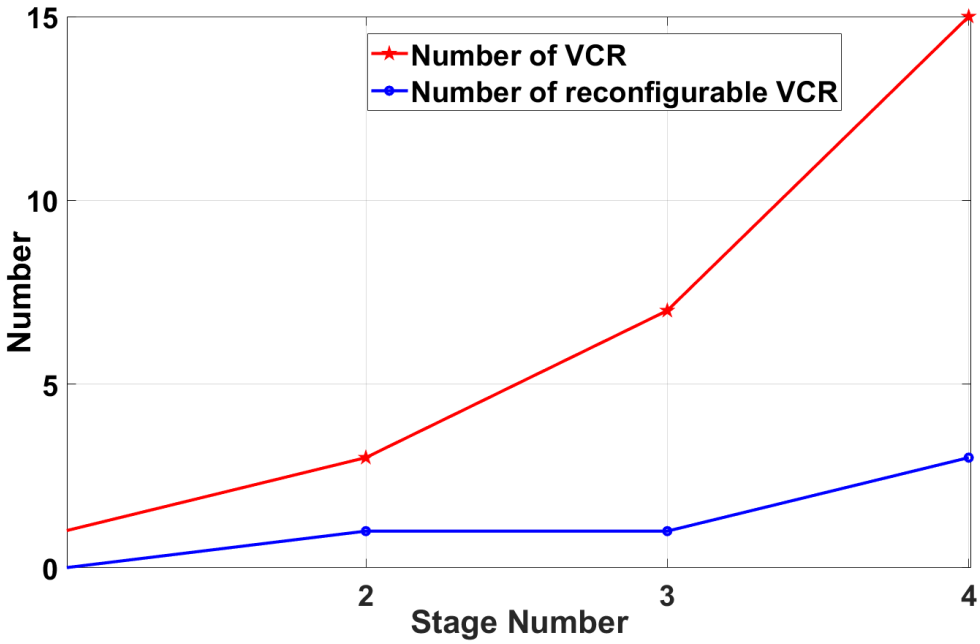

Figure 9: Reconfigurable VCR numbers

(VCR=1/2) or the last two stages (VCR=1/4 or 3/4) will be used, whereas the other converter cells are idle. Fig.10 shows the reconfiguration process of the proposed system at these three VCRs, with the unused converter cells colored in gray. When VCR=1/2, this proposed converter will reconfigure the 4-stage-series-connected converter system into a 4-stage-parallel-connected converter system, so that the previously unused converters can be fully used and the load-driving capacity will therefore be enhanced by at least 4 times. Similarly, when VCR=1/4 or 3/4, the topology will also switch the series-connected system into a new parallel-connected system and the load-driving capacity can be increased by at least 2 times. However, the real enhancement factor calculation is much more complicated. Because the unused converters affect the effective output impedance although they are not outputting any power. Theoretically, if the unused converters are connected in parallel for VCR=1/4, 1/2 and 3/4 cases, the load-driving capacity should be enhanced by 2.125×, 5.3125× and 2.125×, respectively. The detailed analysis will be given in section 3.2.

In order to validate the proposed design, a 4-bit 15-VCR converter system consisting

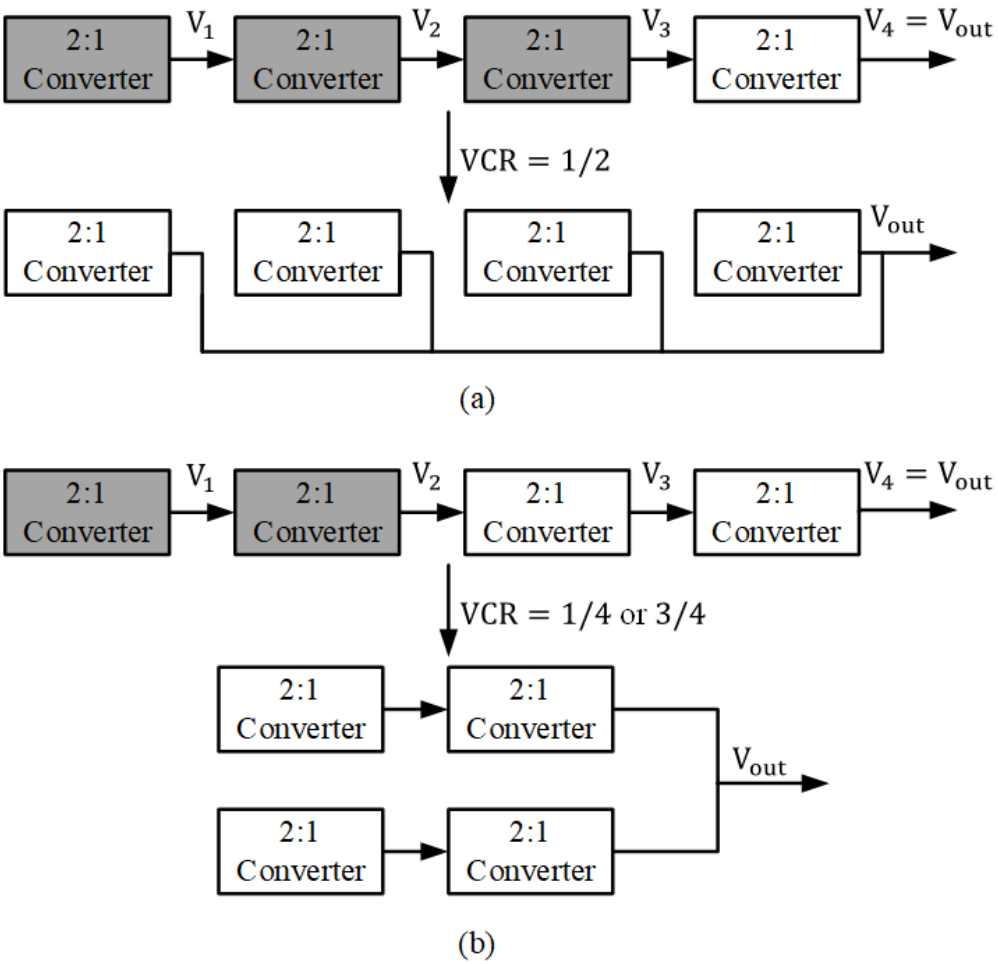

Figure 10: Proposed dynamic reconfiguration scheme for (a) VCR = 1/2 and (b) VCR = 1/4 or 3/4.

of four 2:1 converter cells is designed. The top-level system architecture is shown in Fig.11. The proposed system contains five main blocks: a 4-level series 2:1 converter system, a converter mode control block (VCR reconfiguration), a circuit reconfiguration control block, an output switch control block and a CLK control block. The voltage conversion ratio of the system is controlled by an external 4-bit binary global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$. In these cases, the circuit reconfiguration control block produces a MUX control signal $\{SW_3, SW_2, SW_1\}$, to make the unused converter cells forming new sub-modules. Then the converter mode control block generates a new VCR control signal

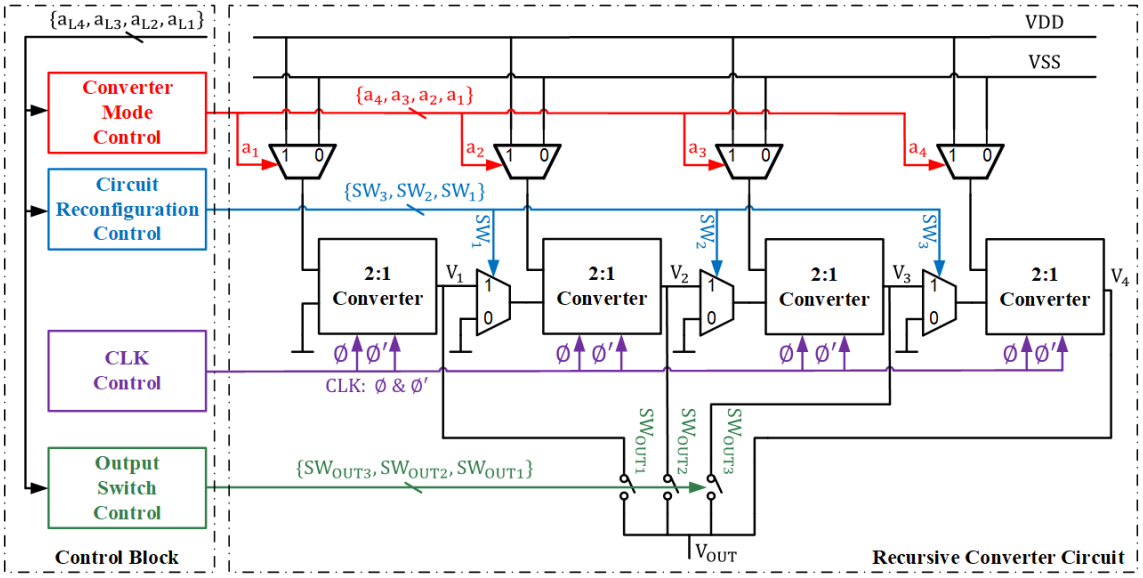

Figure 11: Proposed system architecture.

$\{a_4, a_3, a_2, a_1\}$ to control the conversion ratio of the new sub-modules. These processes could guarantee all sub-modules to have the same desired VCRs, so that they can be re-configured in parallel. The outputs of all 2:1 converters are connected to the total output V_{out} through a 3-bit controllable selecting signal $\{SW_{out3}, SW_{out2}, SW_{out1}\}$, so as to increase the total output current at specific VCRs, thus improving the system's load-driving capacity.

2.2 Power Loss

The main components of the SC converter design are capacitors and power switches. Both of them suffer from non-idealities that cause loss of energy during the normal CLK operation. In this design, the total power loss P_{loss} consists of the switching loss $P_{Switching}$, the conduction loss $P_{Conduction}$ and the power consumption of the CLK generation block P_{CLK}, respectively.

2.2.1 Switching Loss

This section investigates the switching loss $P_{switching}$, the dominating part of whole

power loss. The main contribution of the switching loss are parasitic capacitor charge sharing loss $P_{bot-cap}$ and gate-driving loss P_{driver}.

$$P_{Switching} = P_{bott,cap} + P_{driver} \tag{6}$$

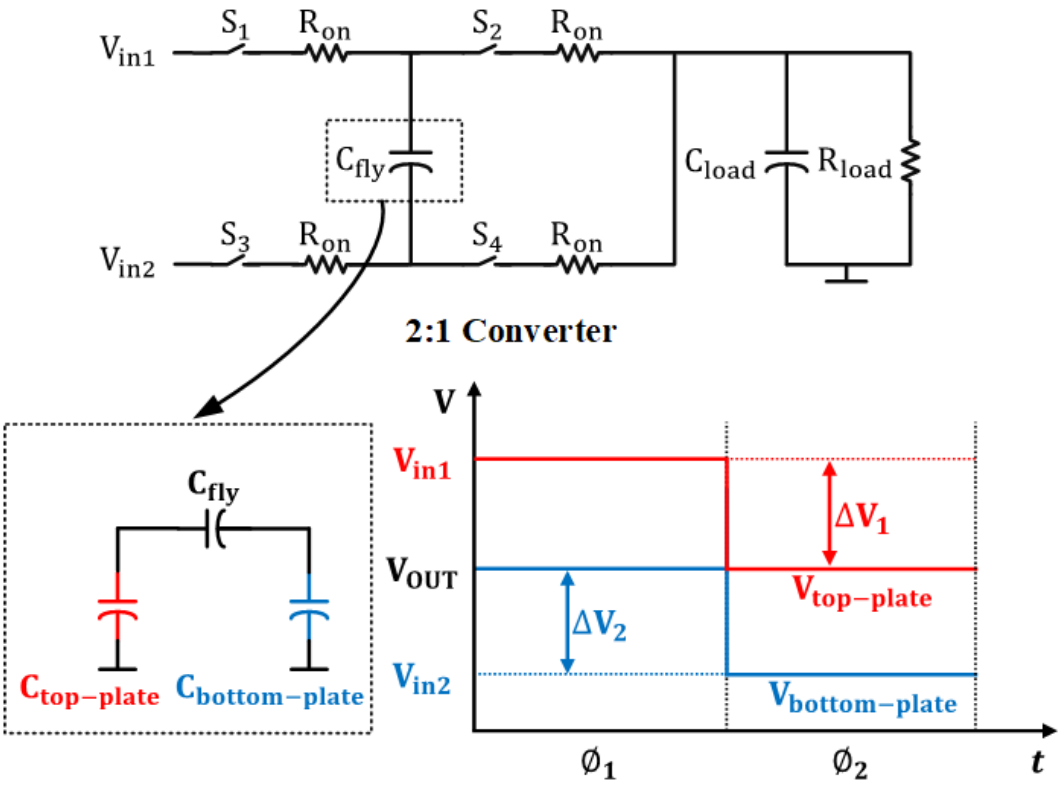

Figure 12: Parasitic Capacitance.

In the fully integrated circuit design, the flying capacitors suffer from parasitic capacitors from their terminals to ground. The most widely used capacitor type-MIM (Metal-Insulator-Metal) capacitor creates parasitic capacitors $C_{top-plate}$ and $C_{bottom-plate}$ between each metal layer away from the substrate, colored in red and blue respectively in Fig.12 [12]. During the whole operation, the voltage change of $V_{top-plate}$ and $V_{bottom-plate}$ are presented in Fig.12. Power loss happens when charging and discharging these two parasitic capacitors. In the steady-state, the top plate capacitor $C_{top-plate}$ and the bottom plate capacitor $C_{bottom-plate}$ will experience approximately equal voltage swings which means $\Delta V = \Delta V_1 = \Delta V_2$. Therefore, it's reasonable to group both losses caused by these

two parasitic capacitors into one parasitic capacitor switching loss $P_{bot-cap}$ [1], which is given by:

$$P_{bot-cap} = M_{bot} f_s C_{bot} \Delta V^2 \tag{7}$$

Where M_{bot} is a constant determined by the RSC cascade stage number ($M_{bot} = N$ for a N-stage RSC system) and the general capacitance $C_{bot} = C_{top-plate} + C_{bottom-plate}$. Because normally in MIM capacitor, the bottom plate parasitic capacitor $C_{bottom-plate}$ are much bigger than the top plate parasitic capacitor $C_{top-plate}$, so this part of switching loss is also called the bottom-plate loss.

Another part of the switching loss comes from the gate driver. Under certain circumstances, the SC converter design might requires large power switches to optimize the characteristic of the output impedance. The CLK generated from the oscillator might not drive the power switches directly. Each power switch needs a tapered buffer to amplify the CLK's driving ability and each tapered buffer consumes huge power. The power loss is also caused by the gate capacitor charging and discharging loss. For a single power switch, the power loss can be determined as Eq.(8):

$$P_{gate-cap} = f_s (C_{SW} + C_{buffer}) V_{SW}^2 \tag{8}$$

Where C_{buffer} is the sum of the gate parasitic capacitance of each buffer stage, and C_{SW} is the gate parasitic capacitance of the power switch. Then V_{SW} is the voltage swing of these gate parasitic capacitance during the CLK operation which is simply equal to the CLK voltage swing V_{dd}.

$$\begin{aligned} P_{driver} &= M_{driver} P_{gate-cap} \\ &= M_{driver} f_s (C_{SW} + C_{buffer}) V_{dd}^2 \end{aligned} \tag{9}$$

Eq.(9) expresses the total power loss for amplifying the drive ability, which is the sum of each pair of the power switch and its gate driver of the whole converter system. Assuming all 4 power switches inside a 2:1 converter are identical, for a N-cascaded-stage converter system in this topology, the M_{driver} will be a constant $4N$. And this part of power loss is the most pivotal limitation of the system's power efficiency.

2.2.2 Conduction Loss

The conduction loss is also an important part of the total power loss. The total conduction loss $P_{Conduction}$ contains intrinsic conduction loss $P_{R_{out}}$ and extrinsic conduction loss P_{switch}.

$$P_{Conduction} = P_{R_{out}} + P_{switch} \tag{10}$$

$$P_{R_{out}} = I_{out}^2 R_{out} = P_{C_{fly}} + P_{R_{SW}} \tag{11}$$

$P_{C_{fly}}$ and $P_{R_{SW}}$ contributes to the intrinsic conduction loss $P_{R_{out}}$. They are caused by the equivalent series resistance (R_{ESR}) of the flying capacitor, and the finite conductance of the power switches respectively of one single 2:1 converter stage [1]. These two kinds of loss are both set by the stage output current I_{out}, and can be modeled by the equivalent output resistance R_{out} in Fig.14. The analysis will be specified in the "output impedance" part in the next section, since this part only focuses on the extrinsic conduction loss P_{switch} due to the reconfiguration MOSFET switches of the control blocks.

In this design, the reconfiguration function of the system is realized by multiple MOSFET switches operating in the linear region, named the reconfiguration switch here. Since the gate control voltage of these switches do not change during operation, it is not necessary to consider the dynamic power consumption. So the conduction loss of this part is the sum of the static power consumption of each MOSFET switch in Eq.(12).

$$P_{switch} = \sum_{i=1}^{M_{switch}} I_i^2 R_i = M_{switch} I_{ON}^2 R_{ON} \tag{12}$$

Where M_{switch} is a constant which is related to the system cascaded stage number N and equal to $(5N-2)$ in this design. R_i is the ON-state resistance of the reconfiguration switch and I_i is the current flowing through R_i. If assuming the reconfiguration switches have the same characteristic, the equation can be further simplified.

$$R_{ON} = \frac{L_{ON}}{\mu C_{ox} W_{ON} (V_{GS} - V_{th})} \tag{13}$$

The ON-state resistance of the i-th reconfiguration switch working in linear region can be expressed as Eq.(13). In this expression, the gate-oxide capacitance density C_{ox}, carrier mobility μ and the threshold voltage V_{th} are determined by the process and always keep fixed which means the ON-state resistance is proportional to the length and inversely proportional to the width. Therefore, it is only necessary to ensure that the minimum length $L_{ON} = L_{min}$ of the process is selected, and then increasing the width W_{ON} as large as possible can minimize the on-resistance. But this is a trade-off with chip area, larger area also introduces more parasitic capacitance and parasitic resistance, which has an impact on system performance.

In order for the converter to achieve the highest overall efficiency at a given power density, we must minimize the total loss, which is set by the combination of the previously discussed loss components:

$$\begin{aligned} P_{loss} &= (P_{bot-cap} + P_{driver}) + (P_{R_{out}} + P_{switch}) \\ &= (Nf_s C_{bot} \Delta V^2 + 4Nf_s (C_{SW} + C_{buffer}) V_{dd}^2) \\ &\quad + (\sum_{i=1}^{N} \frac{1}{4f_s C_{fly,i}} I_{out,i}^2 + \frac{1}{2} \sum_{i=1}^{N} \sum_{j=1}^{4} I_{out,i}^2 R_{SW,ij} \\ &\quad + (5N-2) I_{ON}^2 R_{ON}) \end{aligned} \tag{14}$$

2.3 Power Efficiency

With previous analysis, it can be found that the power loss is related to the component property, the parasitic effect and the CLK switching frequency. Once the components, devices and setup are chosen, the total power loss would approximately keep as a constant. The general expression of the power efficiency is shown below as Eq.(15):

$$eff = \frac{P_{out}}{P_{in} + P_{loss}} \tag{15}$$

In this topology, the input power P_{in} is equal to the output power P_{out} in theory. After reconfiguring the converter system, the input power P_{in} and the output power P_{out} would be increased by the same factor, which is dependent on VCR; but the power loss P_{loss} doesn't change too much as long as f_s is not changed. That indicates the power loss would have relatively lower impairment to Eq.(15), which means the power efficiency can be improved through the reconfiguration method in this design.

3 Circuit Implementation and Analysis

3.1 2:1 SC Converter

3.1.1 Concept of the 2:1 SC Converter

In this subsection, the 2 : 1 switched-capacitor power converter unit is depicted in Fig.13 which consists of a flying capacitor C_{fly} and four power switches with ON-state resistances R_{on}. The output consists of a decoupling capacitor C_{load} in parallel with the load resistor R_{load} [13]. Typically, the switched-capacitor dc-dc converter operates in 2 phases with 50% duty cycle (Could be slightly less than 50%, but the duty cycle of 2 phases should keep the same), and the flying capacitor is switched between the charging phase 1 and the discharging phase 2 [1].

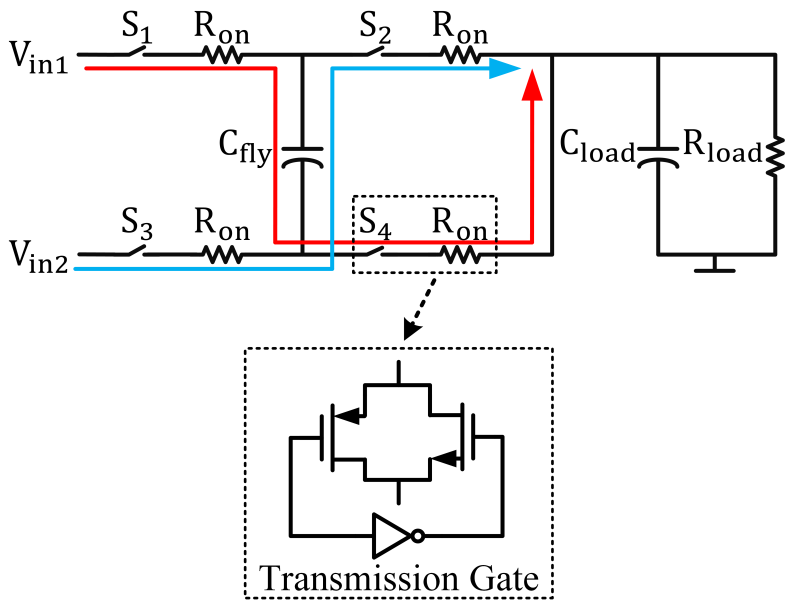

Figure 13: One 2:1 converter cell.

During the charging phase 1 shown as the red line in Fig.13, the flying capacitor is in series between the input V_{in1} and the output V_{out} (switches S_1 and S_4 are ON). The charge from the input goes through C_{fly} to charges this capacitor up to $V_C = (V_{in} - V_{out})$ and flows to the output [13].

$$V_{in1} = V_C + V_{out} \tag{16}$$

During the discharging phase 2 shown as the blue line in Fig.13, the flying capacitor is in series between another input V_{in2} the output V_{out} (switches S_2 and S_3 are ON). The charge stored on C_{fly} in the previous phase is now transferred to the output. The V_{out} becomes the sum of the input V_{in2} and capacitor voltage V_C .

$$V_{out} = V_C + V_{in2} \tag{17}$$

By combining Eq.(16) and Eq.(17), the output voltage V_{out} in steady state can be obtained as below:

$$V_{out} = \frac{1}{2}(V_{in1} + V_{in2}) \tag{18}$$

Since the 2 inputs of converter cell do not maintain the polarity during operations in this topology, transmission gates with NMOS and PMOS switches, as shown in Fig.13, are employed in this design to handle the different voltage polarities across the switches.

3.1.2 The Average Model

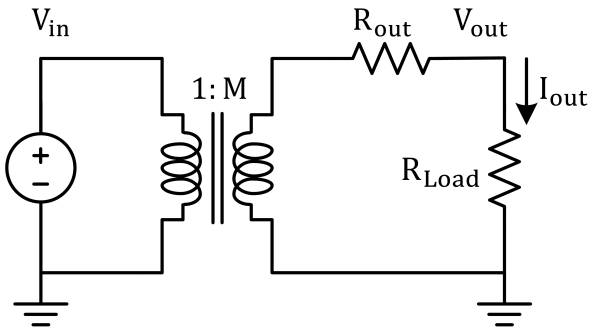

Figure 14: Average Model

The equivalent circuit of an Switched-capacitor converter can be expressed by a cascade connection of an ideal fixed-conversion-ratio stage with an internal resistance R_{out} as shown in Fig.14. In Eq.(19), the fixed-conversion-ratio M is determined by the circuit

configuration. It is equal to the input and output voltage ratio V_{out}/V_{in} at no load condition. The R_{out}, namely the output impedance, directly reflects the efficiency of the converter, incorporates both the conduction loss and the charge sharing loss, then determines the characteristics of the SC converter [10], [14]. Therefore, it is important to obtain the output impedance R_{out} analytically.

$$V_{out} = MV_{in} - R_{out}I_{load} \tag{19}$$

3.1.3 Analysis of Output Impedance

As the switching frequency f_s changes, the 2:1 converter will work in 2 asymptotic operating regions: the fast switching limit (FSL) and the slow switching limit (SSL) [15], [16]. By evaluating the dissipated power loss of these two operating regions when providing $I_{load} \neq 0$, the equivalent output impedance R_{out} can be found. So it's important to analyse the charge distribution during the whole operation firstly.

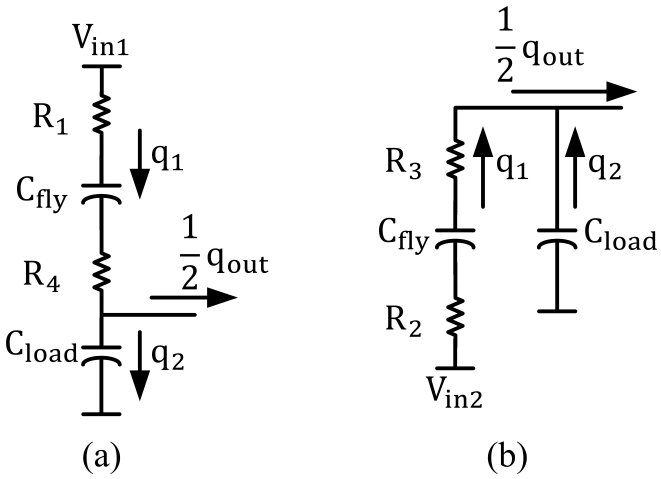

Figure 15: (a) Charge Flow of Phase 1, (b) Charge Flow of Phase 2.

Due to the same phase time, the charge flowing to the output in phase 1 and phase 2 will be the same, which is equal to $0.5q_{out}$. The charge flowing through flying capacitor C_{fly} and the load capacitor C_{load} is q_1 and q_2 respectively. In the charging phase 1 plotted in Fig.15(a), the input V_{in1} charges these two capacitors and also contributes some charge

to the output. So the relationship is shown as Eq.(20).

$$q_{in} = q_1 = \frac{1}{2} q_{out} + q_2 \tag{20}$$

Note that, in steady state, the charge flowing through each of the capacitors must be of equal magnitude but opposite in both clock phase. That means in discharging phase 2 shown in Fig.15(b), both of these two capacitors in this topology C_{fly} and C_{load} will contribute charge to the output. The relationship becomes as Eq.(21).

$$\frac{1}{2} q_{in} = q_1 + q_2 \tag{21}$$

In this way the charge stored and released in the flying capcitor can be easily obtained as Eq.(22).

$$q_1 = \frac{1}{2} q_{out} = q_{in} \tag{22}$$

Firstly considering the fast switching limit (FSL), which means the system is working in a very high switching frequency f_s which will make the phase time much smaller than the time constant τ of this topology. In this mode, the flying capacitors only have a little time to be charged and discharged which means the capacitors voltage can be modeled as constant, so does the current. The circuit energy loss is related only to the conduction loss when the charge flows through the ON-state resistance of the power switches [15].

$$\phi_1 = \phi_2 = \frac{1}{2} T = \frac{1}{2} \frac{1}{f_s} \ll \tau \tag{23}$$

$$\begin{aligned} \tau &= R_{eff} C_{eff} \\ &= (R_1 + R_4) C_{fly} \\ or &= (R_2 + R_3) C_{fly} \end{aligned} \tag{24}$$

The energy consumption of each equivalent resistor can be represented as Eq.(25). In this topology, during two switching phases the charge flows through these 4 ON-resistance of 4 power switches is the same which is equal to $q_1 = 0.5 q_{out}$, the total energy loss $E_{T,FSL}$

caused by the conduction loss is calculated as the sum of each resistor energy as Eq.(26).

$$E_{FSL} = I_i^2 R_i T_i = R_i \frac{q_i^2}{T_i} \tag{25}$$

$$\begin{aligned} E_{T,FSL} &= \sum_{i=1}^{n} E_{FSL} \\ &= \sum_{i=1}^{4} R_i \frac{q_i^2}{T_i} \\ &= \frac{q_{out}^2}{2T}(R_1 + R_2 + R_3 + R_4) \end{aligned} \tag{26}$$

$$\begin{aligned} P_{R_{SW}} &= \frac{E_{T,FSL}}{T} \\ &= \frac{q_{out}^2}{2T^2}(R_1 + R_2 + R_3 + R_4) \\ &= \frac{1}{2}(R_1 + R_2 + R_3 + R_4) I_{out}^2 \\ &= R_{FSL} I_{out}^2 \end{aligned} \tag{27}$$

The time period T_i is equal to half cycle and the relationship between charge and current is $q_i = I_i T_i$, then the equivalent output resistance of FSL mode can be obtained. If the ON-state resistance of each power switch is the same which is equal to R_{on}, the expression R_{FSL} can be simplified further more as Eq.(28) and it's obvious that it is independent of switching frequency f_s and flying capacitor C_{fly}.

$$R_{FSL} = 1/2(R_1 + R_2 + R_3 + R_4) = 2R_{on} \tag{28}$$

The slow switching limit (SSL) is just the opposite situation with fast switching limit (FSL). In this mode, the phase time is much larger than time constant so that the capacitor could have enough time to be charged and discharged. In steady state, the current flowing through the capacitor will become to zero, the energy loss when charging and discharging a capacitor is not related to ON-state resistance of the power switch R_{on} any more [15]. Assuming charging a capacitor from a initial voltage V_0 to V_1, the voltage expression of the capacitor V_C can be defined as Eq.(29).

$$V_C(t) = V_0 + (V_1 - V_0)(1 - e^{\frac{-t}{R_{ESR}C}}) \tag{29}$$

$$I(t) = C\frac{dV_C(t)}{dt} = (V_1 - V_0)\frac{1}{R_{ESR}}e^{\frac{-t}{R_{ESR}C}} \tag{30}$$

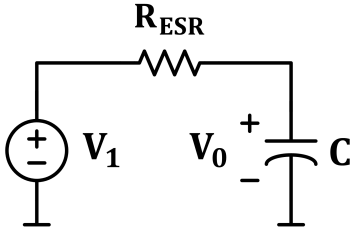

Figure 16: Equivalent series resistance of the capacitor.

Practical capacitor used in electric circuits is not ideal component with only capacitance. However, they can be treated to a very good approximation, as being an ideal capacitor in series with a resistance and this resistance is defined as the equivalent series resistance R_{ESR} [17]. The power loss P_{cap} during charging and discharging period happens due to the conduction loss of the equivalent series resistance R_{ESR} which can be calculated as Eq.(31) [18], [19].

$$P_{Cap} = I^2(t)R = (V_1 - V_0)^2\frac{1}{R_{ESR}}e^{\frac{-2t}{R_{ESR}C}} \tag{31}$$

$$E_{Cap} = \int_0^\infty Pdt = \frac{1}{2}C(V_1 - V_0)^2 = \frac{1}{2}C\Delta V^2 \tag{32}$$

As we explained before, the charge flowing through the capacitor in two phases will be same magnitude but opposite direction. And the charge flowing through the capacitor q_i results in the voltage change of the capacitor ΔV as $q_i = C_i\Delta V$. If substituting the relationship equation between q_i and ΔV to the expression of $E_{C_{fly}}$, the energy loss during a half-cycle $E_{C_{fly},\phi}$ can be simplified as Eq.(33).

$$E_{Cap,\phi} = \frac{q_i^2}{2C_i} \tag{33}$$

At this time, the energy loss of each capacitor during 2 phases can be expressed as Eq.(34). Because there is only one flying capacitor in this 2:1 converter topology, so the total energy loss $E_{T,SSL}$ can be calculated as Eq.(35).

$$E_{SSL} = E_{Cap,\phi 1} + E_{Cap,\phi 2} = \frac{q_i^2}{C_i} \tag{34}$$

$$E_{T,SSL} = \sum_{i=1}^{n} E_{SSL} = \sum_{i=1}^{1} \frac{q_i^2}{C_i} = \frac{q_{out}^2}{4C_{fly}} \tag{35}$$

$$P_{C_{fly}} = \frac{E_{T,SSL}}{T} = \frac{1}{4f_s C_{fly}} I_{out}^2 = R_{SSL} I_{out}^2 \tag{36}$$

By using the same method, the equivalent output impedance of SSL mode can be calculated as R_{SSL} in Eq.(37), which depends on the switching frequency f_s and fly capacitance C_{fly}, but is independent of ON-state switch resistance R_{on}.

$$R_{SSL} = \frac{1}{4f_s C_{fly}} \tag{37}$$

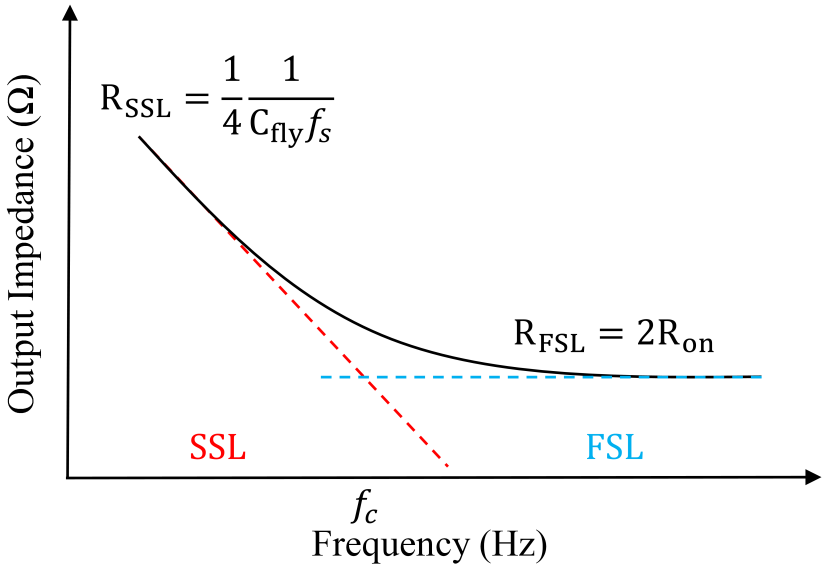

Figure 17: Output Impedance vs Switching Frequency f_s.

The equivalent output impedance R_{out} can be plotted against the switching frequency f_s which is shown in Fig.17. By making $R_{SSL} = R_{FSL}$, the corner frequency f_c can be found in Eq.(38) which reveals the relationship between the switch frequency f_s and output impedance R_{out}. To make the output impedance minimized, the switching frequency in FSL region is always preferred.

$$f_c = \frac{1}{8C_{fly}R_{on}} \tag{38}$$

Because the wire resistance can be minimized through an optimal layout, so the main design parameter in the 2 : 1 SC converter is the ON-state resistance R_{on} of the power switches. The ON-state resistance R_{on} and the switching frequency f_s can be chosen as a trade-off between power density and power transfer efficiency. The ON-state resistance R_{on} is inversely proportional to transistor area, thereby influencing the power density. And the gate-source and drain-source capacitance C_{gs}, C_{ds} (which are proportional to transistor area) and switching frequency f_s are related to switching losses, thereby influencing the power efficiency [13].

3.2 Total System Analysis

The original binary recursive SC converter is based on multi-stage 2:1 converter cascaded. Each flying capacitor C_i in the 2:1 converter cell has at least one input node connected to V_{DD} or V_{SS}. So each converter will load half of its output charge $q_C = 0.5q_{out}$ on the input from previous converter cell and the power supply V_{DD} or V_{SS}. For an N-stage cascaded recursive converter, each converter stage is loaded with a output charge $q_{out,i}$ that is divided by a binary weight of the total output charge q_{out} which is $q_{out,i} = q_{out}/(2^{N-i})$ [4]. By using the same analysis method from previous section, the SSL mode R_{SSL} and the FSL mode R_{FSL} of a N stage RSC system could be summarized as Eq.(39) and Eq.(40), respectively.

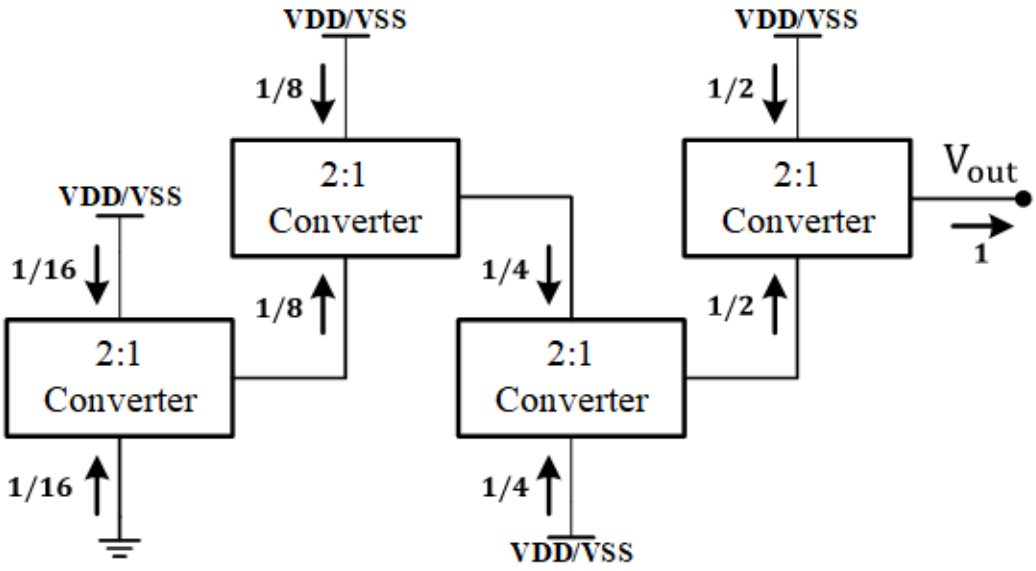

Figure 18: Charge distribution of the original recursive SC

$$R_{SSL} = \sum_{i=1}^{N}\sum_{j=1}^{4}\left(\frac{1}{2^{N-i+1}}\right)^2\frac{1}{f_s C_i} \tag{39}$$

$$R_{FSL} = \sum_{i=1}^{N}\sum_{j=1}^{4}\frac{1}{2}\left(\frac{1}{2^{N-i}}\right)^2 R_{i,j} \tag{40}$$

In the N=4 original RSC system, the $R_{SSL,ori}$ and $R_{FSL,ori}$ can be calculated as Eq.(41) and Eq.(42) below:

$$R_{SSL,ori} = \frac{1}{4}\frac{1}{f_s C_4} + \frac{1}{16}\frac{1}{f_s C_3} + \frac{1}{64}\frac{1}{f_s C_2} + \frac{1}{256}\frac{1}{f_s C_1} = \frac{85}{256}\frac{1}{f_s C} \tag{41}$$

$$R_{FSL,ori} = \frac{1}{64}2R_1 + \frac{1}{16}2R_2 + \frac{1}{4}2R_3 + \frac{1}{1}2R_4 = 2.65625R_{on} \tag{42}$$

It is worth noting that for the original binary RSC converter system, as long as the number of recursion depth N is determined, the charge distribution of each stage will be fixed as Fig.18. That means, no matter how the voltage conversion ratio changes, the equivalent output impedance will theoretically keep the same which is presented in Table. 2.

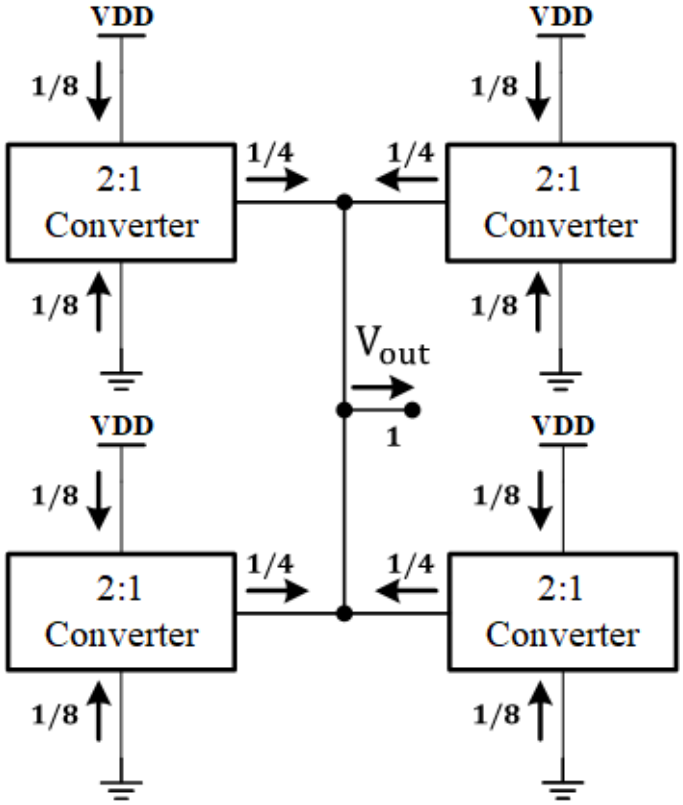

Figure 19: Charge distribution of this reconfigurable recursive SC at VCR=1/2

While for the proposed design in this paper, by reconfiguring the circuit structure un-

der some specific VCRs, the originally fixed charge distribution is now changed. Fig.19 shows the new charge distribution at VCR=1/2 when recursion depth N=4. Through the identical equivalent impedance analysis method, the $R_{SSL,2:1}$ and $R_{FSL,2:1}$ of the reconfigured circuit can be calculated, as Eq.(43) and Eq.(44) shown in Table. 2.

$$R_{SSL,2:1} = \frac{1}{64}\frac{1}{f_s C_4} + \frac{1}{64}\frac{1}{f_s C_3} + \frac{1}{64}\frac{1}{f_s C_2} + \frac{1}{64}\frac{1}{f_s C_1} = \frac{16}{256}\frac{1}{f_s C} \tag{43}$$

$$R_{FSL,2:1} = \frac{1}{16}2R_1 + \frac{1}{16}2R_2 + \frac{1}{16}2R_3 + \frac{1}{16}2R_4 = 0.5R_{on} \tag{44}$$

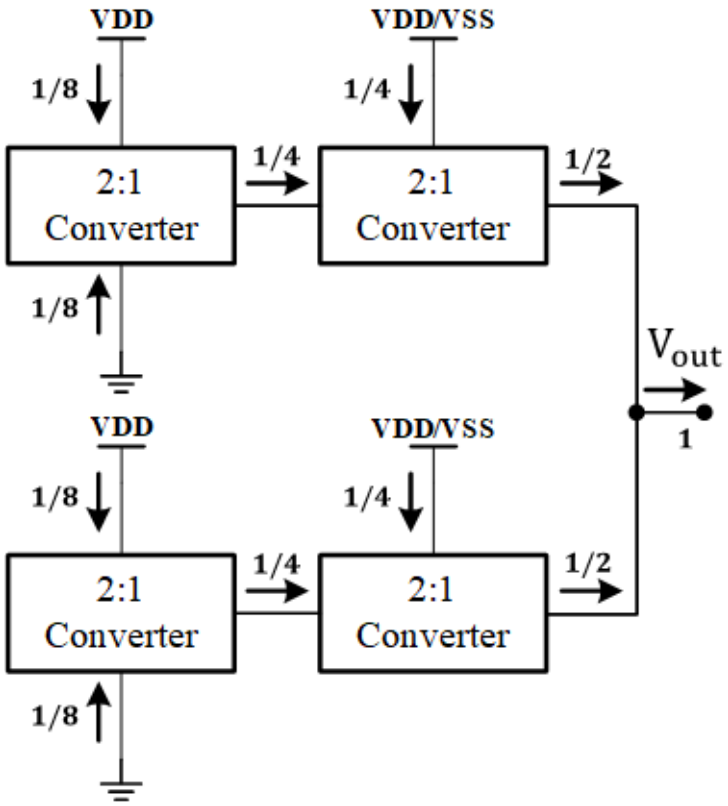

Figure 20: Charge distribution of this reconfigurable recursive SC at VCR=1/4 or 3/4

Fig.20 presents the charge distribution at VCR=1/4 or 3/4 when recursion depth N=4. By using the same analysis method, the $R_{SSL,4:1/3}$ and $R_{FSL,4:1/3}$ of the reconfigured circuit can be calculated, as Eq.(45) and Eq.(46).

$$R_{SSL,4:1/3} = \frac{1}{64}\frac{1}{f_s C_1} + \frac{1}{16}\frac{1}{f_s C_2} + \frac{1}{64}\frac{1}{f_s C_3} + \frac{1}{16}\frac{1}{f_s C_4} = \frac{40}{256}\frac{1}{f_s C} \tag{45}$$

$$R_{FSL,4:1/3} = \frac{1}{16}2R_1 + \frac{1}{4}2R_2 + \frac{1}{16}2R_3 + \frac{1}{4}2R_4 = 1.25R_{on} \tag{46}$$

Table 2: R_{out} of total system

	VCR	R_{SSL}	R_{FSL}	$M_{Enhance}$
Original Recursive	$\frac{1\sim15}{16}$	$\frac{85}{256 f_s C}$	$2.65625R_{on}$	none
Proposed Design	$\frac{1}{2}$	$\frac{16}{256 f_s C}$	$0.5R_{on}$	5.3125
	$\frac{1}{4}$ or $\frac{3}{4}$	$\frac{40}{256 f_s C}$	$1.25R_{on}$	2.125
	others	$\frac{85}{256 f_s C}$	$2.65625R_{on}$	1

Where $M_{Enhance}$ is the enhancement factor, which refers to the ratio of the equivalent output resistance between the original RSC system and this reconfigurable one. $M_{Enhance}$ directly reflects the enhancement of the load drive capacity under these 3 VCRs. Theoretically, for VCR=1/2, the load drive capacity is improved to 5.3125×, whereas for VCR=1/4 or 3/4, a 2.125× increment is realized.

3.3 Logic Control Blocks

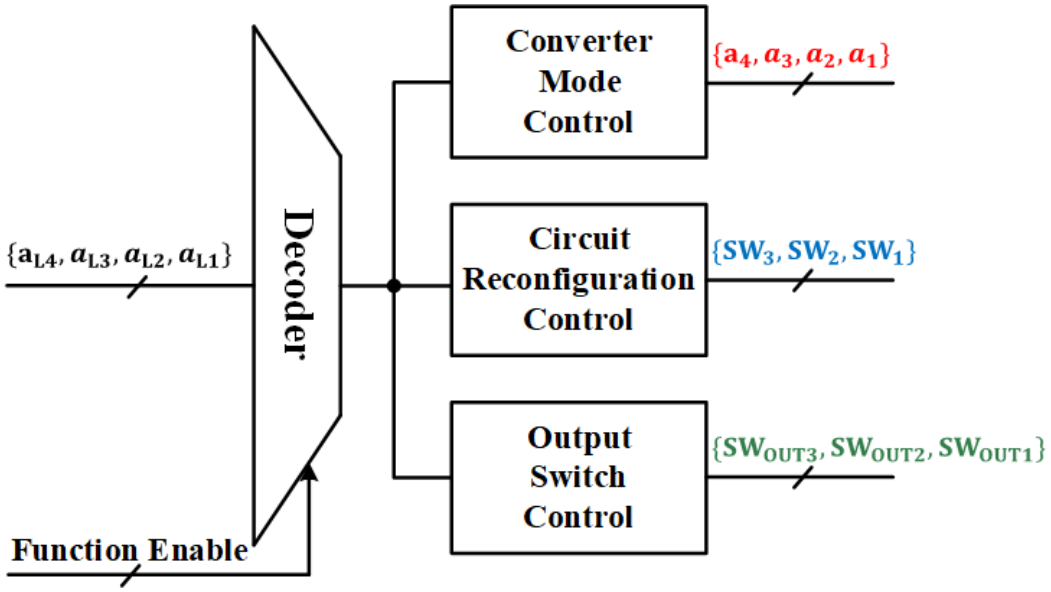

Figure 21: Logic control diagram

The logic control blocks include the Converter Mode Control, the Circuit Reconfiguration Control and the Output Switch Control blocks, as shown in Fig.21. The output control signals of these three blocks are generated from the 4-bit global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$. This 4-bit global input gives the desired VCR for the proposed system. The three logic control blocks translate this 4-bit VCR signal into different configuration signals to determine what the actual VCR should be for each 2:1 converter cell, the parallel-series connections and which converter cells are connected to the global output V_{out}, respectively.

Table 3 shows the signal translation of each logic control block for different voltage conversion ratios. In this 15-VCR 4-stage converter architecture, under 3 specific VCRs (draws in red) this proposed system can be dynamically reconfigured to improve the performance.

Table 3: digital control block logic

Voltage Conversion Ratio(VCR)	Global Input Signal	Converter Mode Signal	Circuit Reconfiguration Signal	Output Switch Signal
1/16	0001	0001	111	000
1/8	0010	0010	111	000
3/16	0011	0011	111	000
1/4	**0100**	**0101**	**101**	**010**
5/16	0101	0101	111	000
3/8	0110	0110	111	000
7/16	0111	0111	111	000
1/2	**1000**	**1111**	**000**	**111**
9/16	1001	1111	000	111
5/8	1010	1111	000	111
11/16	1011	1111	000	111
3/4	**1100**	**1111**	**101**	**010**
13/16	1101	1111	000	111
7/8	1110	1111	000	111
15/16	1111	1111	000	111

The simulated waveform of the global 4-bit input signals, some key control signals and the output voltage are shown in Fig.22. At the first time period, the global input signal is $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\} = 4'b1010$ (VCR=10/16, $Vout = 1.25\,\mathrm{V}$), the output switching signal is $\{SW_{out3}, SW_{out2}, SW_{out1}\} = 3'b000$, meaning only the 4-th 2:1 converter is connected to the global output and all the converter cells are connected in series. Then the global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$ turns to $4'b0100$ (VCR=1/4, $Vout = 0.5\,\mathrm{V}$), $\{SW_{out3}, SW_{out2}, SW_{out1}\}$ switches into $3'b010$ indicating that the system is split into two sub-modules (each submodule has a 2-cascaded converter) and the output of the 2-nd and

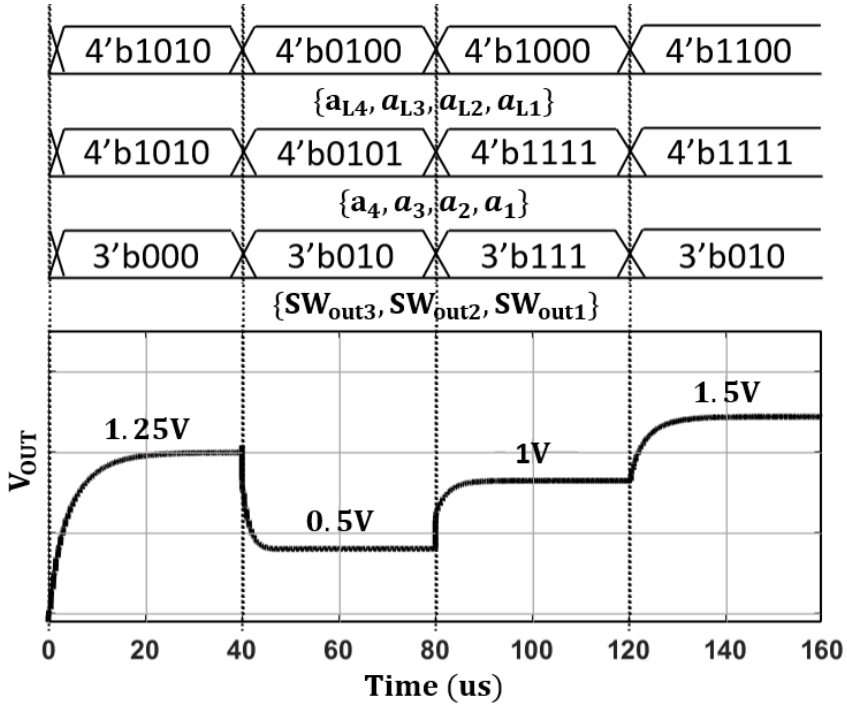

Figure 22: Output voltage waveform

4-th converter cells V_2 and V_4 are connected to the global output. Finally the converter mode control signal $\{a_4, a_3, a_2, a_1\}$ will be equal to $4'b0101$ to make sure the two new sub-modules could realize VCR=1/4. The load-driving capacity will be therefore enhanced by 2.125× theoretically. The system should now operate as the reconfiguration shown in Fig.10 (b).

Then, $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$ becomes $4'b1000$ (VCR=1/2, $Vout = 1\,\text{V}$). The converter mode control block will create a new input control signal $\{a_4, a_3, a_2, a_1\} = 4'b1111$ so that each individual converter achieves the VCR=1/2. And $\{SW_{out}3, SW_{out}2, SW_{out}1\}$ changes into $3'b111$ which means all reconfiguration switches are used now. As a result, the proposed design makes full use of each 2:1 converters to increase the load-driving capacity by 5.3125×. This is the case shown in Fig.10 (a).

3.4 CLK Control Block

Fig.23 presents the CLK control block which includes a pulse signal generator, CLK selector (MUX) and a non-overlapping CLK generator.

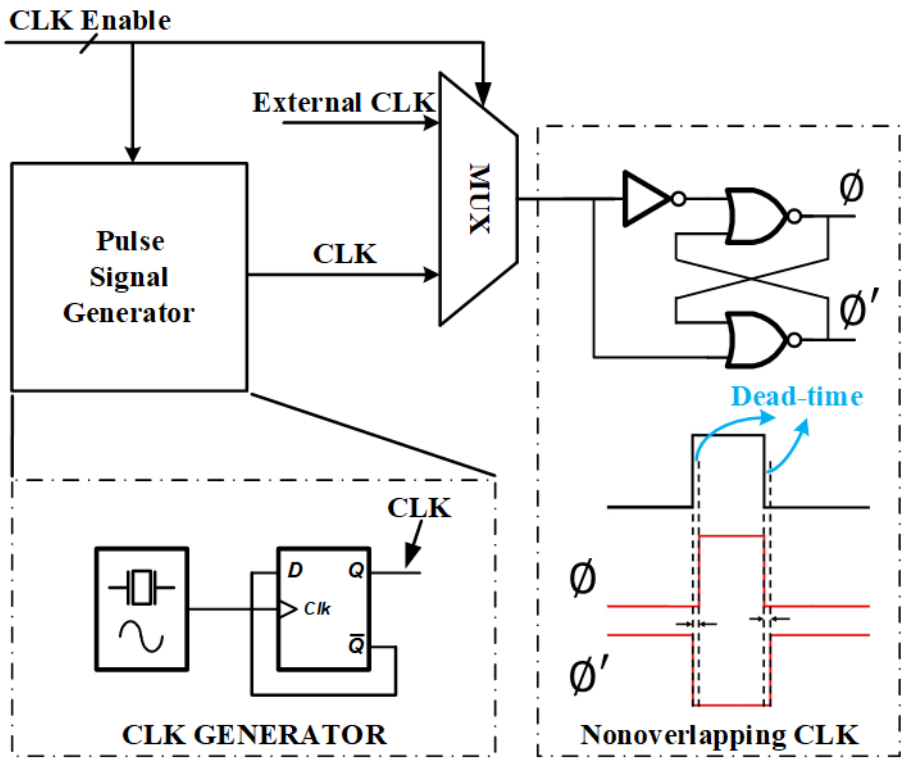

Figure 23: CLK control block.

3.4.1 CLK Generator

The pulse signal generator contains a ring oscillator and a D flip-flop. After the ring oscillator generates a sine-wave with a suitable frequency f_s, the D flip-flop will shape it into a square wave with a duty cycle of 50%. Also, the D flip-flop only consumes very little energy which is good for energy efficiency. In addition to the internal CLK formed by pulse generator, this block also has an external CLK. These two CLKs can be selected by a 1-bit CLK Enable signal at the MUX.

3.4.2 Non-overlapping CLK Generation Circuit

In normal switched-capacitor power converter, the system has to work in two 180° shifted CLK phases. Due to the delay of the device or the parasitic effect, these 2 CLK phases might have a time period overlapped which results in the conduction of all power switches. In this case, a low impedance path from the power supply to the ground will be created and massive energy will be lost.

The non-overlapping clock generation circuit presented in Fig. 23 can handle this problem effectively. In the non-overlapping circuit, the selected CLK will be translated into a pair of interleaved signals ϕ and ϕ' with sufficient dead-time to control the operation of the entire system. This can avoid simultaneous conduction of power transistors during switching transitions, removing the shoot-through current of power transistors and the short circuit power loss in the converter.

3.4.3 Gate Driver

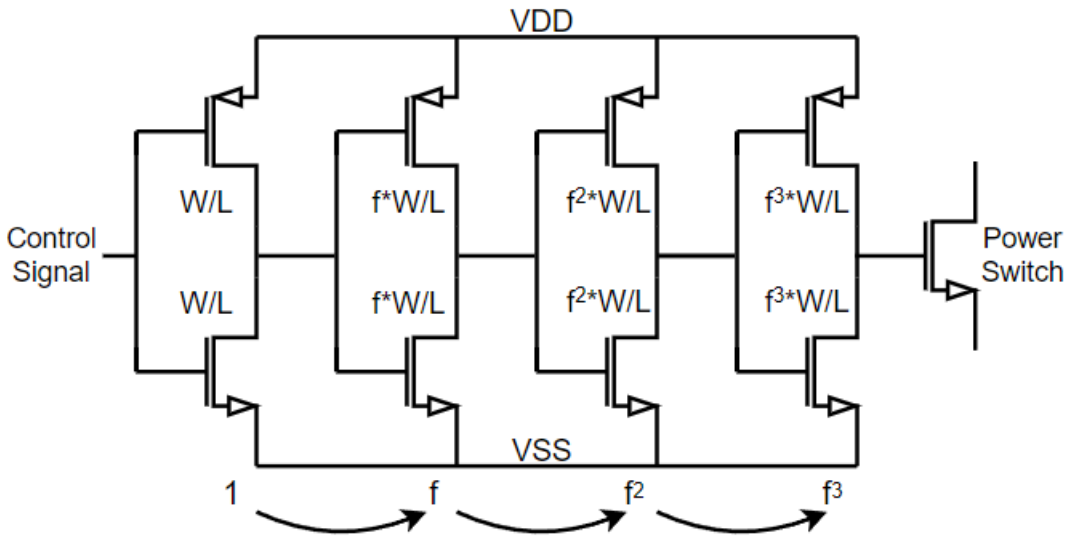

Figure 24: Gate Driver

Typically, the control signals generated from non-overlapping CLK generation circuit cannot drive large power switches in an efficient manner. Hence, the gate driver depicted in Fig. 24 are necessary for each power switches in the system. The gate driver consists of several tapered buffers, which are used to exponentially increase the load-driving capability of the control signal so that it can drive the gates of the large power switches. The tapering factor for each buffering inverter is given by the equation below:

$$f = \sqrt[n]{\frac{size_{power}}{size_{unit}}} \tag{47}$$

Where, n is the number of driver stages, $size_{power}$ is the size of power device and the $size_{unit}$ is the size of the first stage unit.

4 Measurement Results

4.1 Environment Setup

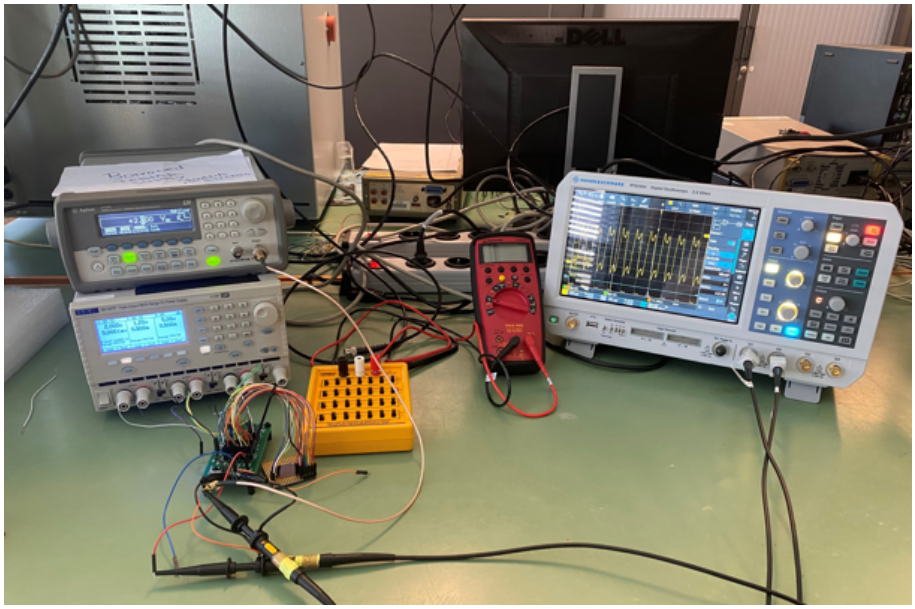

Figure 25: Measurement room

All measurements of this chip were carried out in the measurement room LB.690 in the building of the Faculty of Electrical Engineering, Mathematics and Computer Science at Delft University of Technology. Because this design is a fully on-chip integrated circuit design, there is no need for any external electrical components to participate. All the instruments used in the measurement consist of a pulse signal generator, a DC voltage source, a oscilloscope and a resistor box.

The pulse signal generator could generate a sine wave signal with a frequency of 1 MHz and a duty cycle of 50%, which is used to control the power switches inside the converter cells to perform interleaved-phase operation. The DC voltage source is responsible for generating two supply voltage rails, which are input voltage $V_{in} = V_{DD} = 2\,\mathrm{V}$, and ground voltage $V_{SS} = 0\,\mathrm{V}$. An oscilloscope is used to observe the voltage and current of each node. Finally, the resistor box can be assumed to be a load of the circuit, which can achieve a very wide resistance range, from $0.1\,\Omega$ to $100\,\mathrm{M}\Omega$, with a resolution of $0.1\,\Omega$.

4.2 Chip package

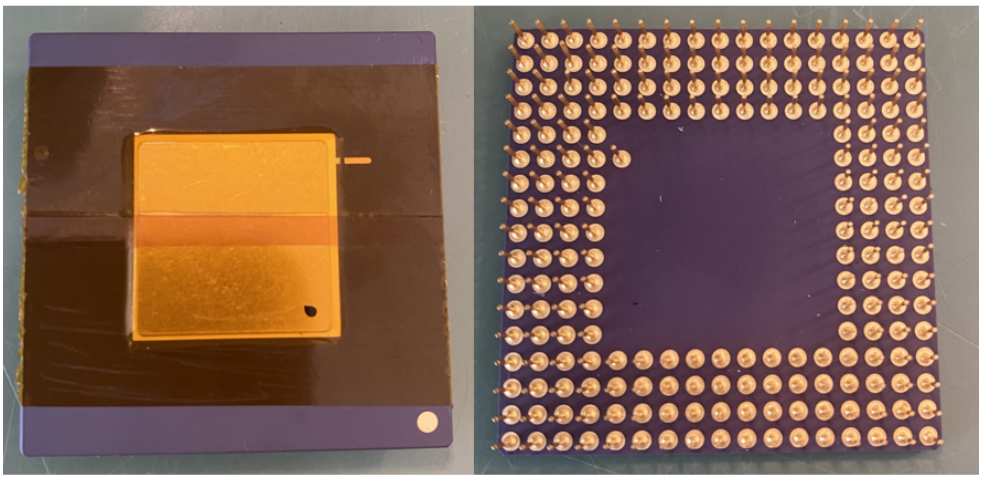

Figure 26: chip photograph

Fig.26 shows the entire chip of this tape-out. This chip has been already packaged and cut. The overall area is about $2.56\,\mathrm{cm}^2$ ($1.6\,\mathrm{cm} \times 1.6\,\mathrm{cm}$) and the chip contains 210 pins in total. The reason for why there are hundreds of pins is that there are 5 designs integrated on the same chip in this tape out.

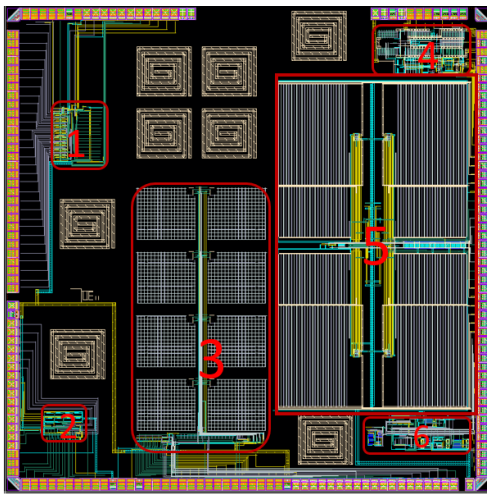

Figure 27: Chip layout

Fig.27 shows the layout of this chip. The entire layout area is around 25 mm^2 (5 mm $\times$ 5 mm), and the largest design NO.5 is this design. This design has 21 pads, including 2 power supply pads, 5 output voltage observation pads, 6 digital control signal input pads and 8 capacitor top and bottom plate voltage signal observation pads. In the chip socket shown in Fig.28, the corresponding pins region is within the red square on the right side of the figure. (More package information will be given in appendix (A.2).)

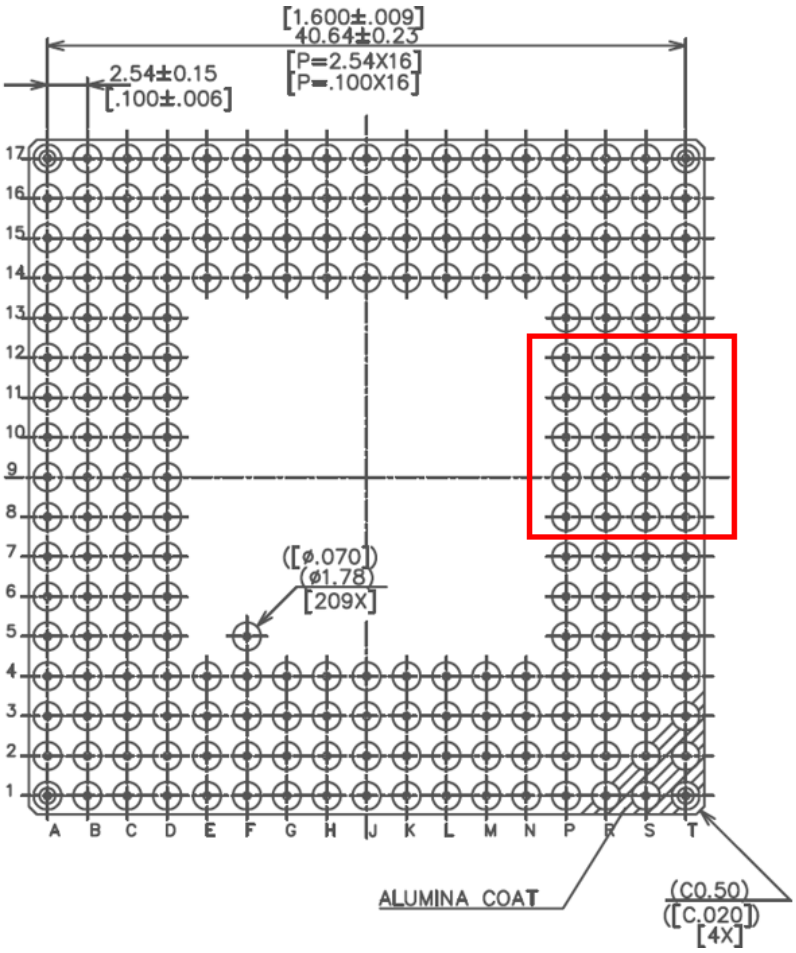

Figure 28: Chip pins

4.3 Chip die graph

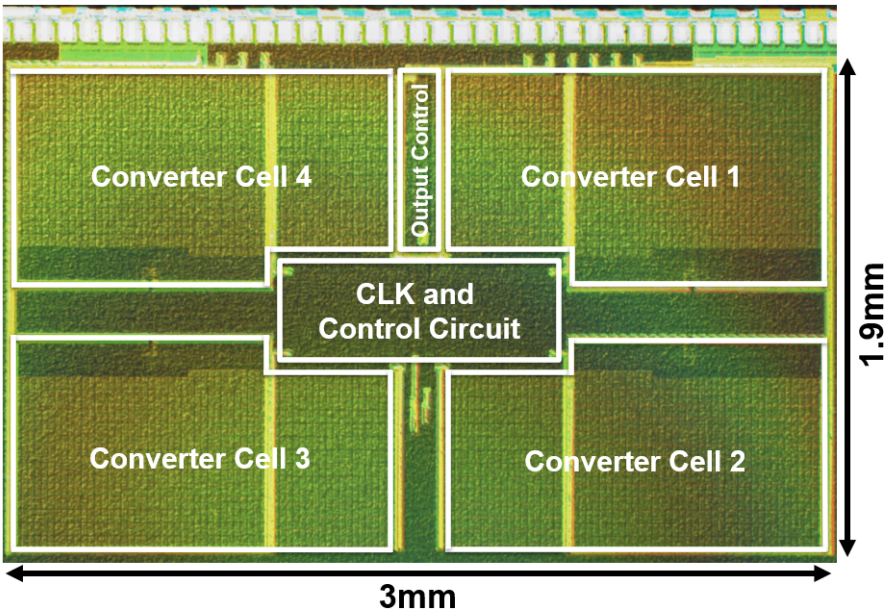

Figure 29: Chip Micrograph

The Fig.29 shows the micrograph of the design circuit. The proposed system has been fabricated in a 180-nm BCD process, occupying 5.7 mm^2 active chip area (1.9 mm $\times$ 3 mm). The proposed system has been made fully on-chip integrated, and On-chip MIM capacitors are used for flying capacitors which are 4 nF in total (1 nF in each converter cell). The maximum load-driving current is 0.71 mA and the power density of this converter system under a peak efficiency of 93.1% is 105.3 $\mu A/mm^2$.

4.4 Efficiency vs output voltage V_{out}

The Fig.30 illustrates the efficiency versus output voltage. Since the figures for the proposed design and conventional design are the same for the VCRs not needing reconfiguration, this figure only focuses on the reconfigurable VCRs, which are 1/4, 1/2 and 3/4. In VCR=1/4 region, when the output voltage is 0.48 V, the load current of proposed work and the conventional RSC are 0.1 mA and 0.04 mA, respectively. Then, in VCR=1/2 region, when the output voltage becomes to 0.97 V, the load current of these two design

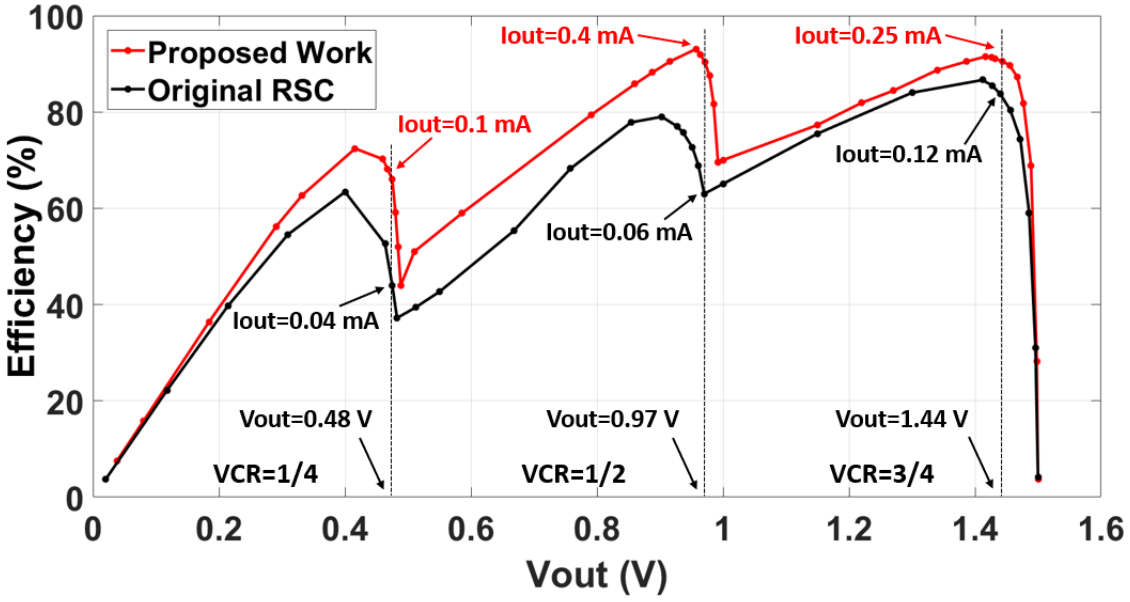

Figure 30: Efficiency vs V_{out}

becomes to 0.4 mA and 0.06 mA, respectively. While for VCR=3/4, the load current changes into 0.25 mA and 0.12 mA for these two circuit when output voltage turns into 1.44 V. From the curve, it can be easily found that when the output voltage is the same, the load current of the this work is much larger than that of the conventional RSC under these 3 VCRs, because the idle converter cells are fully used through reconfiguration in this work. Besides, for these three VCRs, the power conversion efficiency of the proposed design has been comprehensively improved over the entire output voltage range. This is because the input and output power has been significantly improved while the energy loss of the entire system remains unchanged; as a result, the impact of non-ideal energy loss on efficiency becomes smaller in this case.

4.5 Efficiency and V_{out} vs load current I_{out}

The $Efficiency - I_{out}$ and V_{out}-I_{out} figures under VCR = 1/4, 1/2 and 3/4 are plotted in the Fig.31, 32 and 33, respectively. Here we define the valid output should be larger than 95% of desired output voltage. In Fig.31, VCR = 1/4, when the efficiency reaches peak value and output voltage is drawn down to 0.475 V near 95% of preferred output voltage

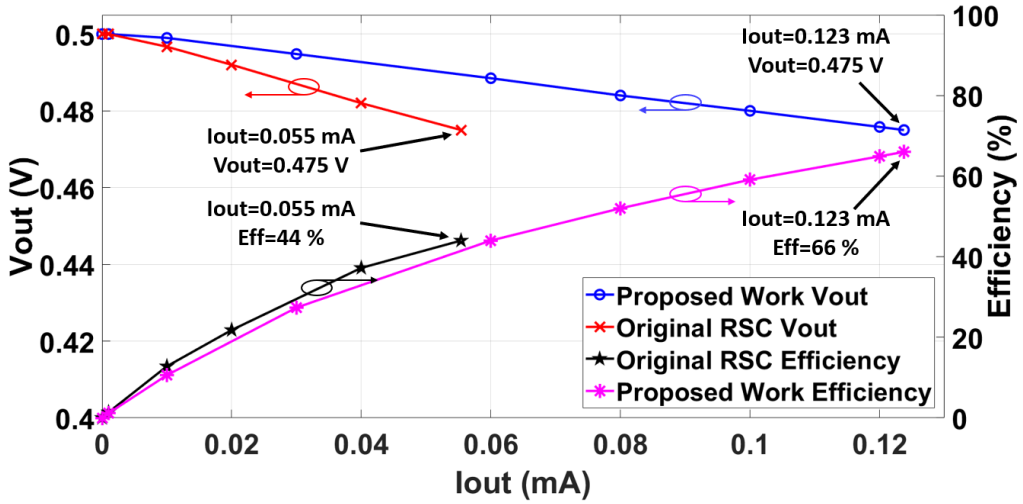

Figure 31: Efficiency and V_{out} vs I_{out} at VCR=1/4

(0.5 V), the load current of proposed and conventional RSC converters are 123 μA and 55 μA, respectively. It can be seen that the load-driving capacity becomes almost 2.236× larger with the proposed design in this case. Furthermore, the peak efficiency of proposed work is 66%, much higher than 44% of the conventional RSC.

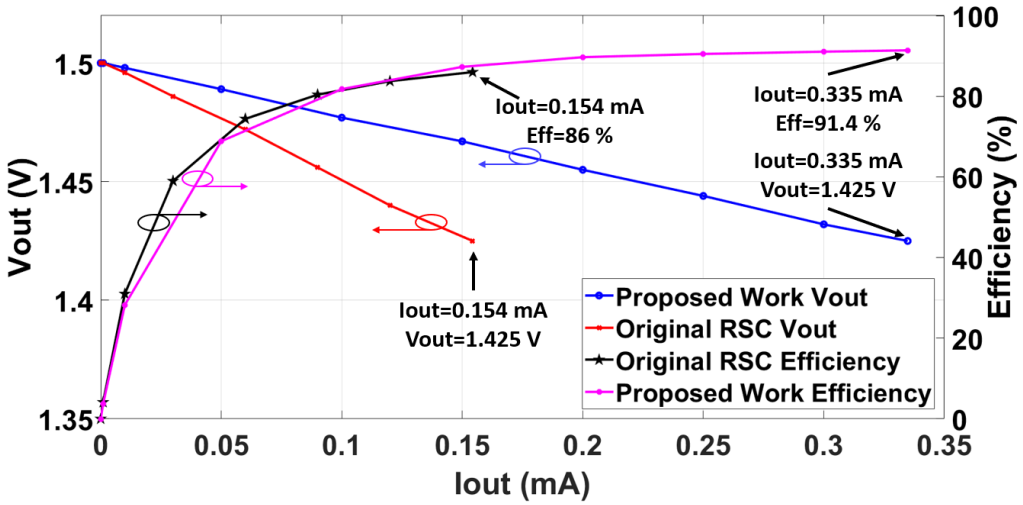

Figure 32: Efficiency and V_{out} vs I_{out} at VCR=3/4

The VCR = 3/4 has the similar condition like previous VCR, which is shown in the Fig.32. When the efficiency reaches peak value and output voltage drops to 1.425 V

near 95% of preferred output voltage (1.5 V), the maximum load current is 335 μA and 154 μA for this work and the conventional RSC. In this case, the measured load-driving enhancement becomes to 2.175×. The peak power efficiency is also improved a lot, from 86% of the conventional RSC to current 91.4%.

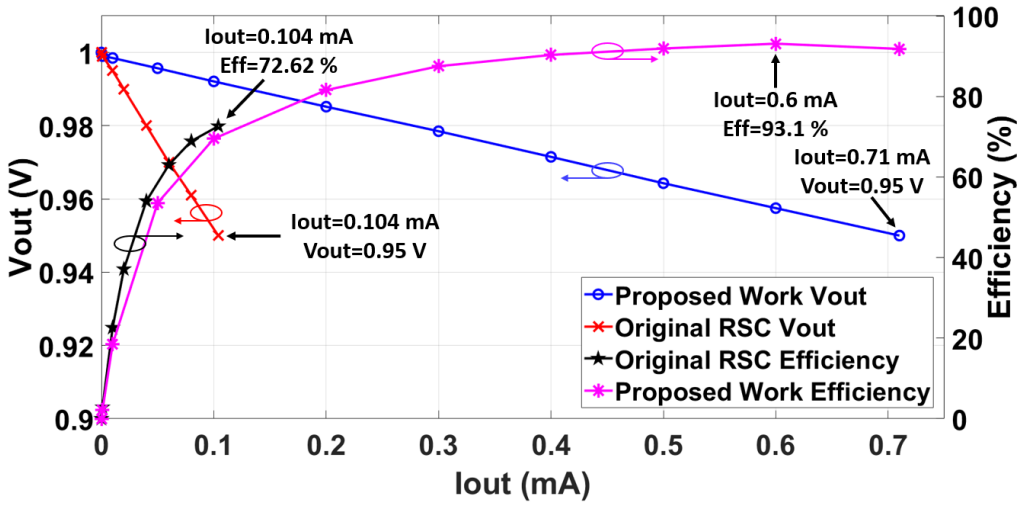

Figure 33: Efficiency and V_{out} vs I_{out} at VCR=1/2

The Fig.33 gives the results when VCR=1/2. When the efficiency achieves the peak value, the proposed work can attain 93.1% peak efficiency under $I_{out} = 600\,\mu$A and the original RSC can only have 72.62% peak efficiency under $I_{out} = 104\,\mu$A. In addition, when output voltage deteriorates to 950 mV (95% of preferred output voltage, 1 V), the load current of the proposed work is 710 μA, which is larger than 104 μA when using the original RSC. It can be seen that the load-driving capacity under VCR = 1/2 is improved by around 6.826× thanks to the 4 converter cells reconfigured to be connected in parallel.

4.6 Output impedance

According to the average model Eq.(19), the load-driving capacity can be reflected by the equivalent output impedance R_{out} of the entire circuit. Based on the measurement results of V_{out} vs I_{out} in the previous paragraph, the equivalent output impedance under these 3 VCRs can be calculated and shown in Table 4. For the conventional RSC circuit,

Table 4: Measurement of overall output impedance R_{out}

	VCR	Conventional RSC	Proposed RSC	Theoretical Factor	Measured Factor
R_{out}	2:1	485Ω	71.05Ω	5.3125	6.826
	4:1	451Ω	201.7Ω	2.125	2.236
	4:3	486Ω	223.45Ω	2.125	2.175

the output impedance of VCR=1/2, 1/4 and 3/4 is 485 Ω, 451 Ω and 486 Ω, respectively. While in the proposed design, the output impedance becomes much more smaller of these 3 VCRs, Which is 71.05 Ω, 201.7 Ω and 223.45 Ω now. The factor, referring to the ratio of the equivalent output impedance between conventional and proposed RSC converter, indicates the enhancement of the load-driving capacity. It can be found that for VCR=1/4 and 3/4, the measured factors 2.236 and 2.175 are slightly larger than the theoretical factor 2.125, but they are still close. While for VCR=1/2, the measured factor 6.826 is much larger than 5.3125. The reasons for these variation are explained as: First, in the total equivalent output impedance analysis, the ON-resistance of all switches used for reconfiguration function must also be taken into account and will dramatically influence the overall impedance. In addition, in the layout design, the wire resistance and the parasitic capacitor introduced between different metal layers will also have a great impact on the final equivalent output impedance.

4.7 State of the art comparison

Table 5 gives the comparison of key performance between this work and conventional designs. One improvement of the proposed design is dynamically reconfigurable connection of all 2:1 converter cells according to the desired VCR; while the conventional RSC designs were fixed topology using four 2:1 converter cells in series, which results in lower load-driving capacity and unused on-chip area.

In addition, in all fully on-chip integrated designs, proposed work realized a peak efficiency of 93.1%, which is among the highest, second only to 95% of [11]. At the same time, compared with the design [4], which is also based on the recursive SC topology, the peak efficiency gets improved by around 8%. Further more, compared to high efficiency design [11], this work has a larger load-driving capacity of 0.71 mA than 0.49 mA of [11], showing higher power density.

Table 5: State of the art comparison

Design	This Work	2019 [20]	2018 [21]	2016 [11]	2015 [22]	2014 [4]	2013 [3]
Technology	180 nm	250 nm	130 nm	180 nm	250 nm	250 nm	180 nm
Topology	Reconfigurable Recursive	Asymmetrical Shunt	Fixed	Rational	Gear Train+ Charge Feedback	Recursive	Successive-approximation
Number of Ratios	15	187	3	79	24	15	117
Circuit Dynamical Configuration	Yes	No	No	No	No	No	No
Maximum Converter Reuse Times	4	1	1	1	1	1	1
Input Voltage	2 V	3.3 V	1.2 - 2.3 V	2 V	2.5 - 5 V	2.5 V	3.4 - 4.3 V
Output Voltage	0.12 - 1.8 V	0.4 - 2.8V	0.9 V	0.13 - 1.87 V	0.2 - 2 V	0.1 - 2.18 V	0.9 - 1.5 V
Max. Load Current	0.71 mA	10 mA	0.49 mA	N/A	60 mA	2 mA	0.3 mA
Capacitor Type	MIM On-Chip	MIM On-Chip	MOS On-Chip	MIM On-Chip	SMD Off-Chip	MIM On-Chip	MIM+MOS On-Chip
Peak Efficiency (η_{peak})	93.1%	87%	80.4%	95%	95.5%	85%	72%
Power Density @ η_{peak} ($\mu A/mm^2$)	105.3	1120.4	3550	71.4	2881.8 (Off-chip caps)	430.6	5.9
Chip Area (mm^2)	5.7	7.14	0.138	3.36	3.47	4.645	1.69

5 Conclusion

5.1 Summary of Main Contributions

This paper proposes a dynamically reconfigurable recursive switched-capacitor DC-DC converter with adaptive load ability enhancement. The presented topology can make full use of each 2:1 converter of a multi-VCR system by dynamically reconfiguring the connection of all the 2:1 converter cells. The reconfigurable VCR number can be determined as $(2^{int(N/2)}-1)$ for N cascaded recursive converter system. Through this method, the load-driving capacity under specific VCRs can be significantly enhanced; in addition, the power transfer efficiency can also be further improved.

A fully-integrated dynamically reconfigurable 4-stage recursive SC converter was designed and fabricated in a 180-nm BCD process to experimentally validate the enhanced load-driving ability and power efficiency. The measurement results show that the maximum load-driving current is around 0.71 mA and the power density of this converter system under a peak efficiency of 93.1% is $105.3\,\mu A/mm^2$. In addition, the proposed circuit has an energy efficiency greater than 80% over a wide output range. Most importantly, the load-driving capacity under some VCRs is significantly increased by up to $6.826\times$ compared to the conventional RSC topology.

5.2 Future Work

5.2.1 Parameter Sizing

In this proposed circuit architecture, 4 converter cells are designed to be the same in order to verify the idea of multiplying the load drive capacity by times. For the specific VCRs that can be dynamically reconfigured, the energy efficiency and the load-driving capacity are good enough. But for other VCRs, from Eq.(41) and Eq.(42), the output impedance is too large and will dramatically limit their peak efficiency and load-driving capacity. To optimize this, each 2:1 converter cell needs to be designed individually, optimizing the ratio between the capacitance of all flying capacitors and the ON-resistance (conductance) of all power switches, rather than using the same parameters.

$$R_{SSL} = \frac{1}{256}\frac{1}{f_s C_1} + \frac{1}{64}\frac{1}{f_s C_2} + \frac{1}{16}\frac{1}{f_s C_3} + \frac{1}{4}\frac{1}{f_s C_4} \tag{48}$$

$$\begin{aligned} R_{FSL} &= 2\left(\frac{1}{64}R_1 + \frac{1}{16}R_2 + \frac{1}{4}R_3 + \frac{1}{1}R_4\right) \\ &= 2\left(\frac{1}{64}\frac{1}{G_1} + \frac{1}{16}\frac{1}{G_2} + \frac{1}{4}\frac{1}{G_3} + \frac{1}{1}\frac{1}{G_4}\right) \end{aligned} \tag{49}$$

The R_{SSL} and R_{FSL} of the recursive SC converter are Eq.(48) and Eq.(49), respectively. If the total capacitance C_{tot} and total conductance G_{tot} are fixed here, by using Lagrange multiplier, the best capacitance solution for the minimal SSL mode impedance R_{SSL} can be obtained as Eq.(50):

$$C_i = \frac{2^{i-1}}{2^N - 1} C_{tot} \tag{50}$$

Where N is the cascaded stage number and i is the order of 2:1 converter cell.

Then, the best conductance of power switch in each stage for the minimal FSL mode impedance R_{FSL} can also be determined as Eq.(51) shown below. (The detailed calculation is given in (A.1) in appendix.)

$$G_i = \frac{2^{i-1}}{2^N - 1} G_{tot} \tag{51}$$

5.2.2 Hybrid SC

There are some other methods to further improve the loss mechanism. An inductor can be introduced between the SC stage and the load capacitor. This method uses LC resonance to achieve lossless energy transfer through resonant operation ,thereby reducing the charge sharing loss. In Fig.34, it can be found that in FSL mode, the R_{out} of hybrid and RSC converter are almost the same, but hybrid SC converter requires much lower switching frequency. This will result in smaller gate-driving loss in the control circuit therefore higher energy efficiency can be realized.

However, the frequency of the LC resonant oscillation cannot be accurately predicted, so an additional current zero-crossing detection circuit will be required. And this approach cannot achieve fully on-chip integration.

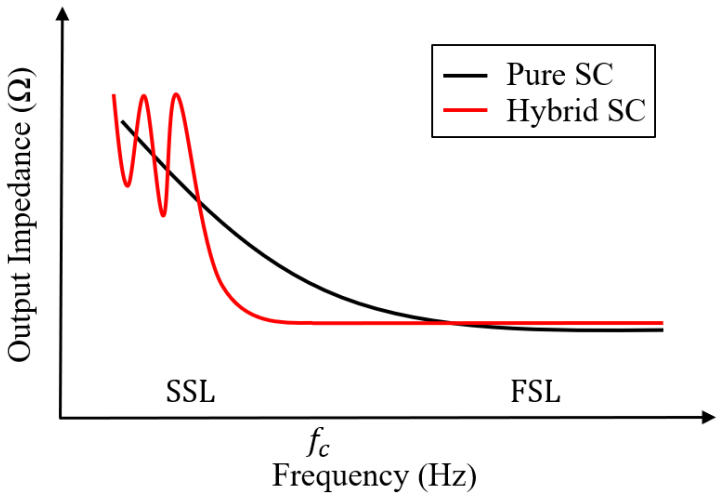

Figure 34: hybrid SC

5.2.3 Soft Charging Technique

Another strategy to optimize the intrinsic loss is to use multi-phase soft charging technique to reduce the voltage step between flying capacitor and the load capacitor by splitting the entire flying cap into multiple capacitors, thereby reducing charge sharing loss. This method can significantly reduce the loss, but cannot reduce it as well as the previous way. It can be realized fully on-chip but requires additional power switches and flying capacitors, resulting in system complexity and more driving loss. Different techniques can be selected according to specific needs.

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A Appendix

A.1 Parameter Sizing

Using Lagrange multiplier to get minimal value L_{min} of $L = \frac{1}{256}\frac{1}{C_1} + \frac{1}{64}\frac{1}{C_2} + \frac{1}{16}\frac{1}{C_3} + \frac{1}{4}\frac{1}{C_4}$:

$$L_{min} = \frac{1}{256}\frac{1}{C_1} + \frac{1}{64}\frac{1}{C_2} + \frac{1}{16}\frac{1}{C_3} + \frac{1}{4}\frac{1}{C_4} + \lambda(C_{tot} - C_1 - C_2 - C_3 - C_4) \tag{52}$$

$$\frac{\partial L}{\partial C_i} = \begin{cases} \frac{1}{4}\frac{1}{C_4^2} = -\lambda \\ \frac{1}{16}\frac{1}{C_3^2} = -\lambda \\ \frac{1}{64}\frac{1}{C_2^2} = -\lambda \\ \frac{1}{256}\frac{1}{C_1^2} = -\lambda \end{cases} \tag{53}$$

$$\frac{1}{4}\frac{1}{C_4^2} = \frac{1}{16}\frac{1}{C_3^2} = \frac{1}{64}\frac{1}{C_2^2} = \frac{1}{256}\frac{1}{C_1^2} \tag{54}$$

$$\begin{cases} C_4 = 8C_1 \\ C_3 = 4C_1 \\ C_2 = 2C_1 \\ C_1 = C_1 \end{cases} \tag{55}$$

$$\begin{cases} C_4 = \frac{8}{15}C_{tot} \\ C_3 = \frac{4}{15}C_{tot} \\ C_2 = \frac{2}{15}C_{tot} \\ C_1 = \frac{1}{15}C_{tot} \end{cases} \tag{56}$$

So the ratio of capacitance can be found as below; the derivation of conductance is the same.

$$C_i = \frac{2^{i-1}}{2^N - 1}C_{tot} \tag{57}$$

A.2 Chip information

A.2.1 Chip front side

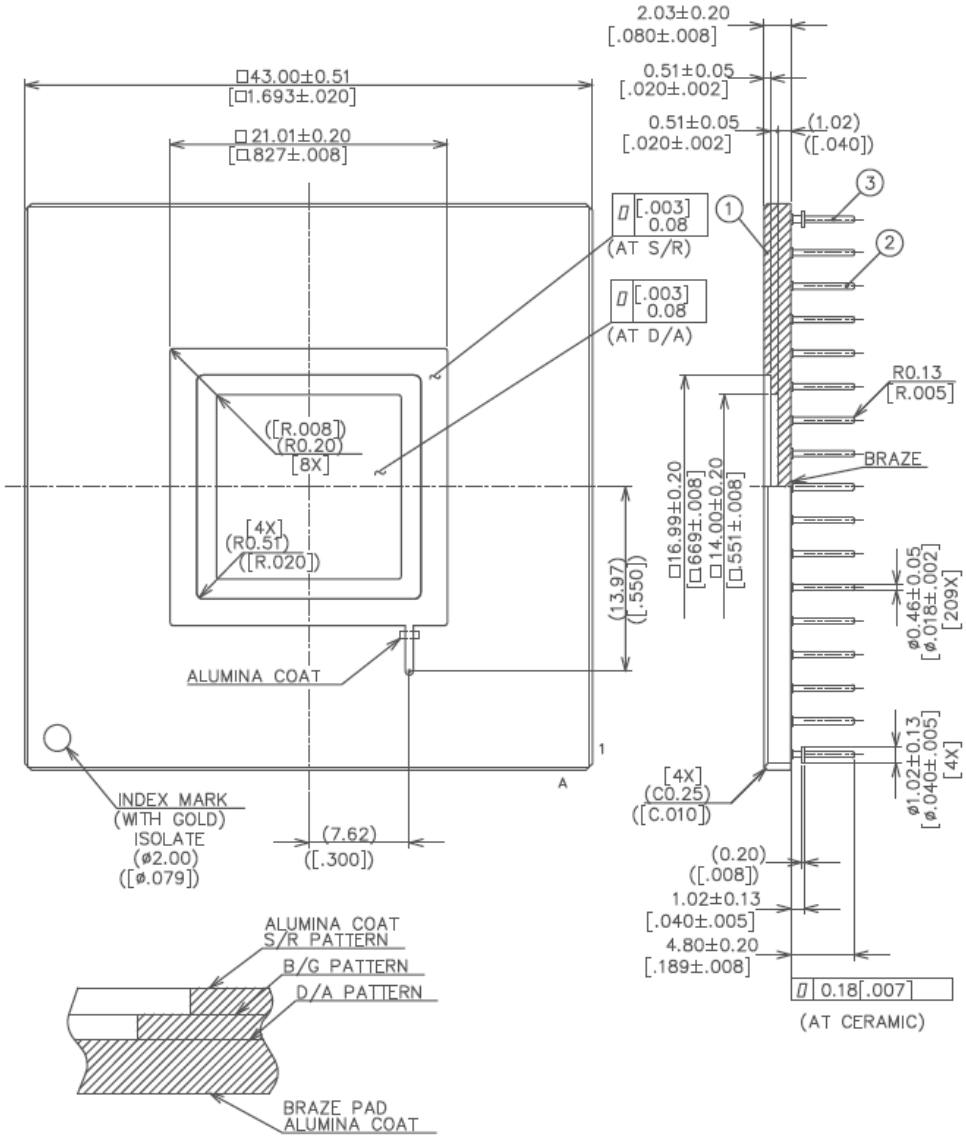

Figure 35: Chip front side

A.2.2 Chip pins table

CONNECTION TABLE

PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN
1	P4	31	H4	60	A2	90	A13	120	G14	150	N15	180	T10	D/A	N/C
2	P3	32	H3	61	A3	91	B12	121	G15	151	P16	181	S9	S/R	N/C
3	R2	33	G1	62	B5	92	A14	122	F17	152	N14	182	P9		
4	T1	34	G2	63	D6	93	C12	123	G16	153	R16	183	R9		
5	P2	35	F1	64	C6	94	D12	124	G17	154	P15	184	T9		
6	N4	36	G3	65	A4	95	A15	125	H14	155	S16	185	T8		
7	N3	37	G4	66	B6	96	B13	126	H15	156	R15	186	S8		
8	S1	38	E1	67	A5	97	A16	127	H16	157	P14	187	P8		
9	R1	39	F2	68	D7	98	C13	128	H17	158	R14	188	R8		
10	N2	40	D1	69	C7	99	B14	129	J16	159	S15	189	T7		
11	M4	41	F3	70	A6	100	D13	130	J14	160	T17	190	S7		
12	M3	42	F4	71	B7	101	B15	131	J15	161	S14	191	T6		
13	P1		F5	72	A7	102	C14	132	J17	162	P13	192	R7		
14	M2	43	C1	73	D8	103	B16	133	K17	163	R13	193	P7		
15	N1	44	E2	74	C8	104	C15	134	K16	164	T16	194	T5		
16	L4	45	B1	75	B8	105	D14	135	K14	165	T15	195	S6		
17	L3	46	E3	76	A8	106	D15	136	K15	166	S13	196	T4		
18	M1	47	D2	77	B9	107	C16	137	L17	167	P12	197	R6		
19	L2	48	E4	78	D9	108	A17	138	L16	168	R12	198	P6		
20	L1	49	C2	79	C9	109	D16	139	M17	169	T14	199	T3		
21	K4	50	D3	80	A9	110	E14	140	L15	170	S12	200	S5		
22	K3	51	B2	81	A10	111	E15	141	L14	171	T13	201	T2		
23	K2	52	C3	82	B10	112	B17	142	N17	172	P11	202	R5		
24	K1	53	D4	83	D10	113	C17	143	M16	173	R11	203	S4		
25	J2	54	C4	84	C10	114	E16	144	P17	174	T12	204	P5		
26	J4	55	B3	85	A11	115	F14	145	M15	175	S11	205	S3		
27	J3	56	A1	86	B11	116	F15	146	M14	176	T11	206	R4		
28	J1	57	B4	87	A12	117	D17	147	R17	177	P10	207	S2		
29	H1	58	D5	88	C11	118	F16	148	N16	178	R10	208	R3		
30	H2	59	C5	89	D11	119	E17	149	S17	179	S10				

Figure 36: Chip pins table

A.3 List of publications

Q Lu, S Li, S Du, “A dynamically reconfigurable recursive switched-capacitor dc-dc converter with adaptive load ability enhancement,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022. (Under review)