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RESEARCH ARTICLE

Quadratic Boost DC–DC Converters Capable of Being Extended to Improved Topologies

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ABSTRACT Luo converters represent the most extensive family of non-isolated DC-DC converters, yet achieving high voltage gain in these topologies often compromises simplicity. This study introduces a novel family of quadratic boost converters that address this challenge by combining six key features: 1) continuous input current, 2) reduced component count, 3) optimized voltage/current stress on semiconductors, 4) higher voltage gain than conventional designs, 5) high efficiency across a wide duty-cycle range, and 6) topological extensibility comparable to Luo converters. The proposed topologies are analyzed in both ideal and non-ideal operating modes, with derived expressions for voltage gain and efficiency sensitivity. Design requirements are detailed for continuous conduction mode (CCM), complemented by small-signal analysis and compensator design for the primary family members. Experimental results validate the theoretical models, demonstrating the converters' performance and robustness. Additionally, voltage gain tests for extended topologies confirm their adherence to theoretical predictions. The proposed family offers a streamlined, high-performance alternative to existing Luo converters, with potential applications in high-gain, non-isolated power conversion systems.

INDEX TERMS Boost converter, family converters, high-gain converters, non-isolated converters, quadratic boost converters.

I. INTRODUCTION

DC-DC converters are broadly classified into isolated and non-isolated topologies. Isolated converters utilize high-frequency transformers to achieve higher voltage gain [1] and provide essential galvanic isolation for sensitive loads. However, these transformers introduce several drawbacks, including leakage inductance, residual currents, and elevated voltage stress on switching devices [2]. Furthermore, their discontinuous input current increases the current stress on input filter capacitors, necessitating bulky, high-capacitance components that raise system cost and volume [3]. The transformers themselves also contribute to increased converter size and weight, making non-isolated topologies preferable for many applications. Among conventional non-isolated DC-DC converters, the boost converter stands out for its ability to elevate input voltage across all duty cycle ranges. However, its voltage gain progression is slow (0% duty cycle: Gain = 1, 50% duty cycle: Gain = 2, 80% duty cycle: Gain = 4). Critically, efficiency plummets sharply at duty cycles beyond 80%, severely limiting practical voltage gain [4]. This inherent constraint underscores the need for improved topologies capable of delivering higher gain without compromising efficiency [5]. Luo family converters are other non-isolated classic DC-DC converters. This family proposes many topologies with various features. The basic topologies in this family provide a higher voltage gain than the boost topology. Notably, this achievement is not significant. Additionally, a significant voltage gain increase is achieved in the complex member of this family. However, the component's number increase is more significant than the voltage gain increase. In other words, the voltage gain density in these converters is poor and unacceptable.

Recent advancements in non-isolated DC-DC converters have sought to address the inherent limitations of

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conventional boost topologies, particularly in achieving high voltage gain without compromising efficiency or practicality. However, existing solutions exhibit critical trade-offs that hinder their widespread adoption. While [6] successfully doubles the voltage gain of a standard boost converter, it sacrifices the common ground between the input source and load—a crucial requirement for many applications (Gain Enhancement at the Cost of Functionality). Cascaded and hybrid topologies, such as cascaded buck-boost configurations ([7], [23]) achieve higher gain but suffer from discontinuous input current, elevated voltage/current stress on semiconductors, and the need for multiple switch types, increasing control complexity. Converters in [8], [10], and [17] provide higher gain but introduce excessive input current ripple, necessitating larger filters. Conversely, [9] combines boost and Cuk topologies but achieves lower gain due to duty-cycle limitations (increased ripple and efficiency loss). The designs in [16] and [20] employ numerous passive/active components yet deliver only marginal gain improvements. Similarly, [18]'s quadratic buck-boost topology imposes prohibitively high voltage/current stress on switches, offsetting its gain advantage (excessive component count with limited benefits). Modifications like [14] and [19] fail to mitigate excessive voltage stress on critical components. Although [22] improves upon [19], it retains this fundamental drawback (unresolved voltage stress issues). The Cuk-based approach in [11] maintains continuous current but lacks significant gain enhancement. Meanwhile, [21] reduces capacitor stress and uses a single switch, but its gain improvement remains unsatisfactory (partial solutions with compromises). Prior efforts either: i) increase gain but introduce ripple, stress, or grounding issues; ii) reduce stress but fail to improve gain meaningfully; or iii) add complexity without proportional performance benefits. This underscores the demand for a converter that simultaneously delivers i) high voltage gain (beyond conventional boost limits); ii) continuous input current (minimizing filter requirements); iii) low component stress (enhancing reliability); iv) common-ground operation (ensuring practicality); v) minimal passive components (reducing cost/size). All the converters discussed in [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], and [23] are quadratic DC-DC topologies that do not utilize the voltage lift technique. In contrast, the topologies introduced in [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], and [41] combine boost or quadratic boost topologies with voltage lift structures, also known as voltage multiplier cells (VMCs). These VMCs enhance the converter's voltage gain through the parallel and series connection of capacitors. The topologies presented in [24], [25], [26], [27], and [28] combine boost topologies with VMCs, resulting in a higher voltage gain compared to standard boost converters. However, the voltage gain achieved is not substantial. The topologies proposed in [29] and [30] utilize a simple voltage lift structure alongside a cascaded boost topology, leading to a slightly higher voltage gain than that of quadratic boost topologies. References [31], [32], [33], [34], and [35] feature a voltage-doubling structure applied to the quadratic boost topology, effectively providing twice the voltage gain of the quadratic boost topology itself. It's important to note that these topologies cannot achieve a tenfold voltage gain when the duty cycle is under 50 percent. In [36], [37], [38], and [39], the quadratic boost topology is employed with an enhanced VMC, allowing for a tenfold voltage gain when the duty cycle reaches 50 percent. Compared to earlier topologies, this implementation has seen success; however, the achieved voltage gain still falls short for many applications. Finally, the topologies in [40] and [41] represent improved designs capable of delivering a voltage gain exceeding ten times at a 50 percent duty cycle. Nevertheless, this enhancement is still not deemed significant. The presented topology in [42] uses the stucture of the super lift Luo converter for two times. However, the provided voltage gain is not high and desired. The proposed topology in [43] has achieved a high voltage gain. However, the common ground of the load and input source has been lost and can be provided.

In this study, a family of non-isolated quadratic boost topologies is introduced as same as the Luo converters family, which introduces some main topologies and extracts improved extensions according to the main structures. The main converters of this family have a continuous input current and distribute it between two inductors, ensuring that the inductors' current stresses and their conduction loss are decreased. The semiconductors are in good condition concerning their desired voltage and current stresses. Notably, such an advantage is improving in the extracted extension of the main structures. The increased voltage gain in the extensions of the main topology makes this family capable of being used in a variety of applications.

This study is organized as follows:

- Section II discusses the operational details.
- Section III studies the non-ideal mode.
- Section IV is about small signal analysis and compensator design.
- Section V discusses the other members of this family.
- Section VI presents the suitable applications of the proposed topologies.
- Section VII compares the proposed family members with each other.
- Section VIII compares the proposed topologies with the recently suggested converters.
- Section IX reports the possibility of the use of other classic topologies in this family.
- Section X reports the experimental results.
- Section XI belongs to the conclusion.

II. OPERATIONAL DETAILS

The main topologies of the proposed family are named the first and second proposed DC-DC converters, depicted in Fig. 1. Both topologies consist of 2 switches, 2 diodes,

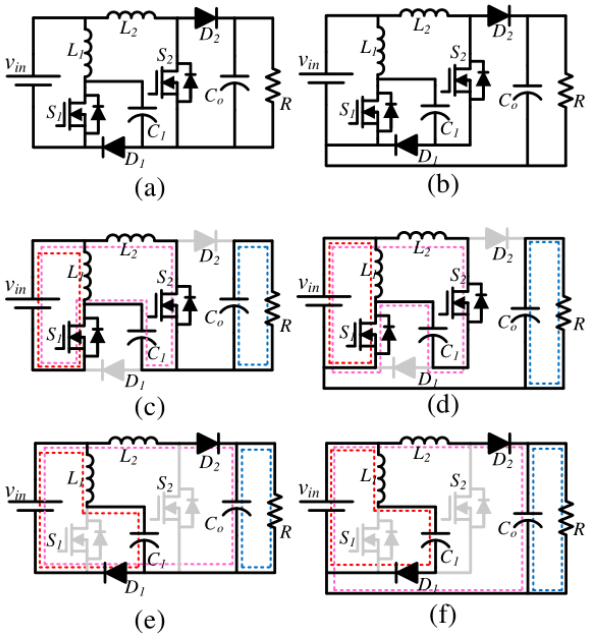

FIGURE 1. (a), (c), (e) The first proposed converter and (b),(d), (f) the second proposed converter.

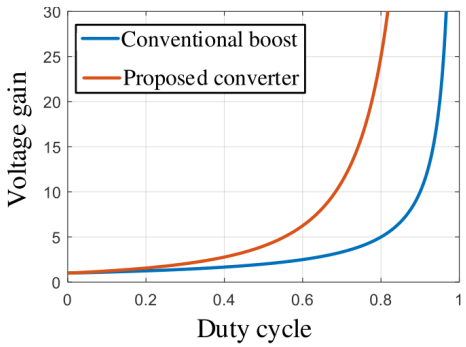

FIGURE 2. Ideal voltage gain comparing of the proposed topologies and the conventional boost converter.

2 inductors, and 2 capacitors with a continuous input current. As shown in Fig. 1, the sum of the currents in the inductors serves as the input current of the converters, thereby reducing the current stress on the inductors. In other words, this method is better than crossing the same value of the input current through a single inductor, which leads to a lower conduction loss. The first topology lacks the common ground between the load and input source, a deficiency addressed in the second suggested topology. The analysis assumptions for this converter's functioning include ideal component behaviour, continuous conduction mode (CCM), and steady-state operation.

Two operating modes can be discussed for both the main topologies according to the activation and inactivation of the semiconductors. The first operating mode of both the topologies starts with the activation of the switches. In this mode, the diodes are OFF, and positive voltages are applied to the inductors to magnetize them. Additionally, the crossing currents through the capacitors discharge them. The equivalent circuit of the first and second proposed converters have been illustrated in Figs. 1 (c) and (d), respectively.

When the switches are turned off, the second operation mode begins. Figs. 1(e) and 1(f) show the equivalent circuits of the second operating mode for the first and second proposed topologies, respectively. The inductors release their stored energy due to their negative voltage, while the capacitors' currents flow from their positive terminal and charge them. Additionally, the diodes are activated by the direction of the inductors' current. To define the function parameters of these converters, the voltage equations of inductors and the current equations of capacitors are described for the first and second proposed topologies as follows.

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - v_{c1}) \\ L_2\dfrac{di_{L2}}{dt} = D(V_{in} + v_{c1}) + (1-D)(V_{in} - v_o) \\ c_1\dfrac{dv_{c1}}{dt} = D(-i_{L2}) + (1-D)(i_{L1}) \\ c_o\dfrac{dv_{co}}{dt} = D(-I_o) + (1-D)(i_{L2} - I_o) \end{cases} \tag{1}$$

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = D(V_{in}) + (1-D)(V_{in} - v_{c1}) \\ L_2\dfrac{di_{L2}}{dt} = D(V_{in} + v_{c1}) + (1-D)(V_{in} - v_o) \\ c_1\dfrac{dv_{c1}}{dt} = D(-i_{L2}) + (1-D)(i_{L1}) \\ c_o\dfrac{dv_{co}}{dt} = D(-I_o) + (1-D)(i_{L2} - I_o) \end{cases} \tag{2}$$

According to the presented figure, the presented topologies have a negligible difference in their topology. In other words, the lost common ground of the load and input source in the first proposed topology is solved simply in the second proposed topology with a simple change in the connections. Notably, this connection change did not have any influence on the operating equations of the proposed topologies, and the corresponding relations in both equations are the same.

In the steady state, inductors behave like a short circuit, while capacitors behave like an open circuit. This means that the average voltage across the inductor and the average current through the capacitor are both zero. Therefore, the average current through the inductors and the average voltage across the capacitors can be expressed as the following equations for the first and second proposed topologies respectively:

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D} \\ V_{Co} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \quad \begin{cases} I_{L1} = \dfrac{D}{(1-D)^2} I_o \\ I_{L2} = \dfrac{I_o}{1-D} \end{cases} \tag{3}$$

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D} \\ V_{Co} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \quad \begin{cases} I_{L1} = \dfrac{D}{(1-D)^2} I_o \\ I_{L2} = \dfrac{I_o}{1-D} \end{cases} \tag{4}$$

Based on the extracted relations, both topologies have the same voltage gain, corresponding capacitor voltages, and corresponding inductor currents. Fig. 2 shows the voltage gain of the proposed topologies compared to the conventional boost converter. As shown, the proposed topologies provide a higher voltage gain than the conventional one for all duty cycle percentages.

In the next step, calculating the inductor's average current and the capacitors' average voltage allows to determine the voltage/current stresses on the semiconductors of the first and second proposed topologies as follows, respectively.

$$\begin{cases} I_{S1} = \dfrac{D}{(1-D)^2} I_o \\ I_{S2} = \dfrac{D}{1-D} I_o \\ I_{D1} = \dfrac{I_o}{1-D} \\ I_{D2} = I_o \end{cases} \quad \begin{cases} V_{S1} = \dfrac{V_{in}}{1-D} \\ V_{D1} = \dfrac{V_{in}}{1-D} \\ V_{S2} = \dfrac{V_{in}}{(1-D)^2} \\ V_{D2} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{5}$$

$$\begin{cases} I_{S1} = \dfrac{D}{(1-D)^2} I_o \\ I_{S2} = \dfrac{D}{1-D} I_o \\ I_{D1} = \dfrac{D}{1-D} I_o \\ I_{D2} = I_o \end{cases} \quad \begin{cases} V_{S1} = \dfrac{V_{in}}{1-D} \\ V_{D1} = \dfrac{V_{in}}{1-D} \\ V_{S2} = \dfrac{V_{in}}{(1-D)^2} \\ V_{D2} = \dfrac{2-D}{(1-D)^2} V_{in} \end{cases} \tag{6}$$

Comparing the corresponding stresses shows that the current stress of the first diode in the first proposed topology is higher than in the second proposed topology. On the other hand, all the corresponding voltage stresses are the same except the second diode voltage stress, which has a higher value in the second proposed topology. To define the acceptability of the extracted stresses, they must be compared with a base value. In the step-up converters, the highest current value is the input current, and the highest voltage value is the output voltage. In this study, the input current and the output voltage are as follows:

$$I_{in} = \frac{I_o}{(1-D)^2}, V_o = \frac{V_{in}}{(1-D)^2} \tag{7}$$

Comparing the presented current stress of the semiconductors with the input current shows that all the current stresses are less than the input current in both proposed topologies. Therefore, the current stresses are in an acceptable condition. In the case of the voltage stresses, the highest voltage stress in the first proposed topology is the same as the output voltage. However, in the second proposed topology, the highest voltage stress exceeds the output voltage value. Notably, this challenge can be solved in the possible extensions of these converters.

The simplified format of the inductors' current ripple and capacitors' voltage ripple are as follows for both the first and second proposed topologies, respectively:

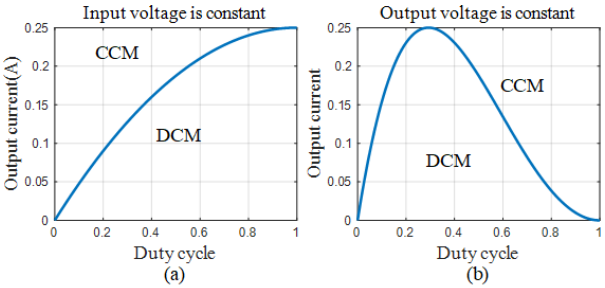

FIGURE 3. Operation region of the first and second proposed converters in CCM AND DCM, while: (a) the output voltage is constant and (b) the input voltage is constant.

$$\begin{cases} \Delta i_{L1} = \dfrac{DV_{in}}{L_1 f_s} \\ \Delta i_{L2} = \dfrac{D(2-D)V_{in}}{(1-D)L_2 f_s} \end{cases} \quad \begin{cases} \Delta v_{C1} = \dfrac{DI_o}{(1-D)C_1 f_s} \\ \Delta v_o = \dfrac{DI_o}{C_o f_s} \end{cases} \tag{8}$$

$$\begin{cases} \Delta i_{L1} = \dfrac{DV_{in}}{L_1 f_s} \\ \Delta i_{L2} = \dfrac{D(2-D)V_{in}}{(1-D)L_2 f_s} \end{cases} \quad \begin{cases} \Delta v_{C1} = \dfrac{DI_o}{(1-D)C_1 f_s} \\ \Delta v_o = \dfrac{DI_o}{C_o f_s} \end{cases} \tag{9}$$

The operation of the converter in CCM depends on the ripple of the inductor's current and the average output current. The minimum inductor values required for proper converter operation are as follows:

$$L_1 > \frac{(1-D)^4 R}{2f_s}, L_2 > \frac{D(2-D)(1-D)^2 R}{2f_s} \tag{10}$$

$$L_1 > \frac{(1-D)^4 R}{2f_s}, L_2 > \frac{D(2-D)(1-D)^2 R}{2f_s} \tag{11}$$

The second effective factor is the average value of the output current of the inductors. The average value of the inductors varies with the average value of the output current and the duty cycle percentage. Fig. 3 illustrates the operating region of the converters in both CCM and DCM, based on the average output current and duty cycle for the first and second proposed topologies. This figure is valid for both converters. These curves have been extracted according to the presented equations as follows:

$$I_o = \frac{V_{in}}{2f_s L_2} D(2-D) = \frac{V_o}{2f_s L_2} D(2-D)(1-D)^2 \tag{12}$$

All the points below the curves belong to the discontinuous conduction mode (DCM), and all the points above the curves belong to the continuous conduction mode (CCM).

III. NON-IDEAL MODE

The voltage gain calculated in the second section may not accurately reflect the converter's actual voltage gain behaviour for all duty cycle percentages in real-world scenarios. Therefore, it is important to take into account the

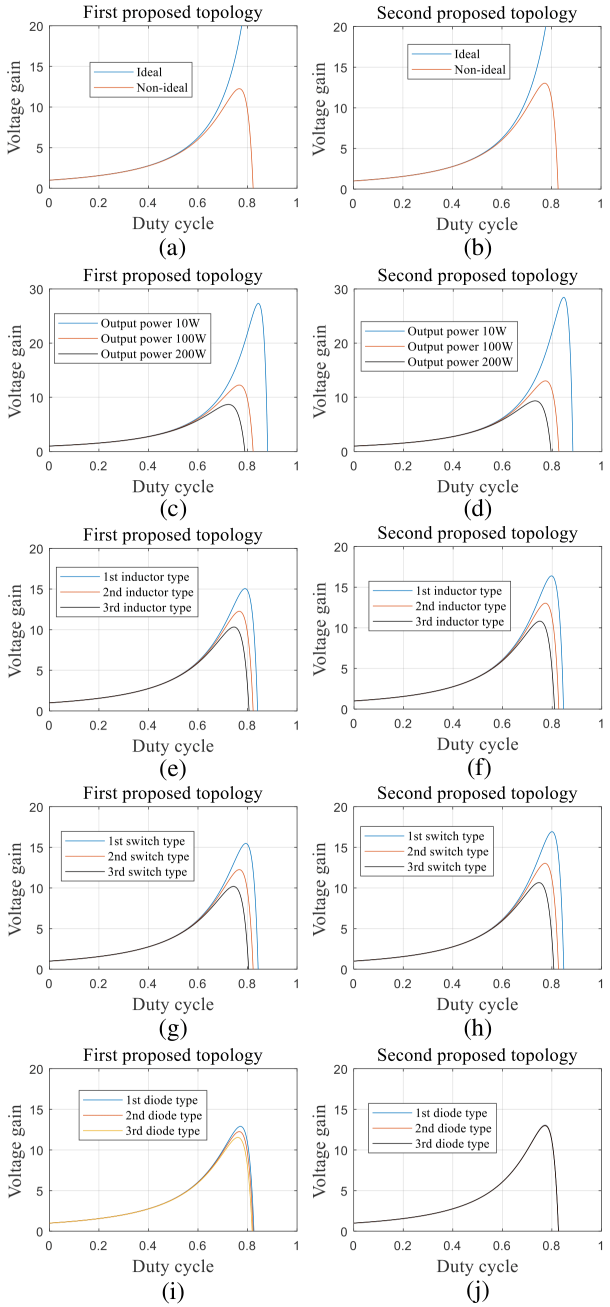

FIGURE 4. (a) and (b) Ideal and non-ideal voltage gain comparing in a fixed output power, (c) and (d) non-ideal voltage gain behaviour for various output powers, (e) and (f) various inductors, (g) and (h) various switches, (i) and (j) various diodes.

parasitic resistance of inductors, switches, and diodes. If we overlook the equivalent series resistance of capacitors, the converters' non-ideal voltage gain will be as follows:

$$\begin{cases} \dfrac{v_o}{V_{in}} = \dfrac{1}{(1-D)^2}\left(1 - \dfrac{r_L}{R}\left(\dfrac{D^2-D+1}{(1-D)^4}\right) - \right. \\ \left. \dfrac{r_S}{R}\left(\dfrac{D+D^2-D^3}{(1-D)^4}\right) - \dfrac{r_D}{R}\left(\dfrac{2-2D+D^2}{(1-D)^3}\right)\right) \end{cases} \tag{13}$$

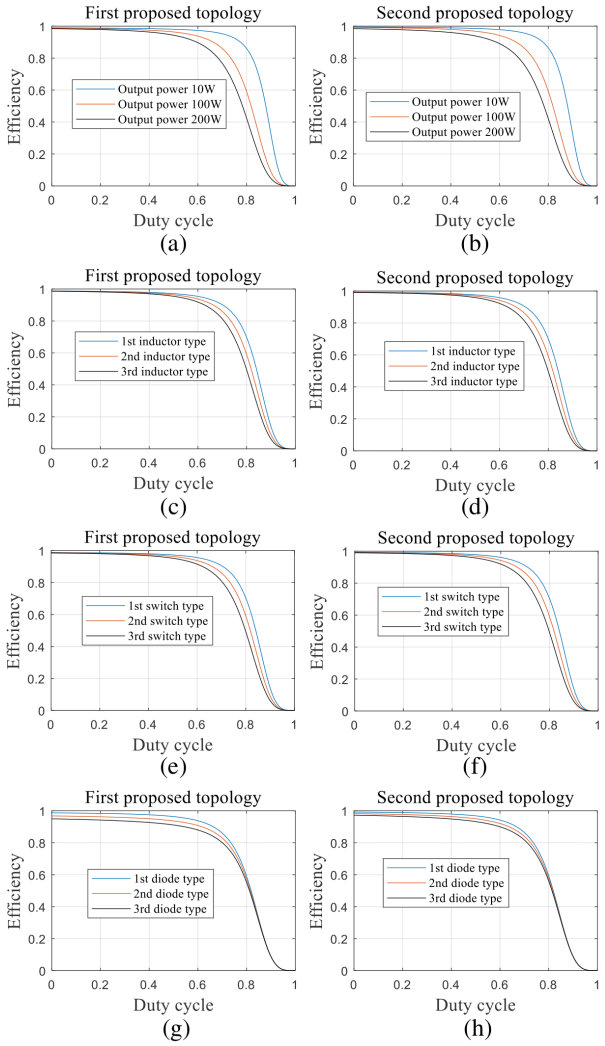

FIGURE 5. (a) and (b) Efficiency behaviour for various output powers, (c) and (d) various inductors, (e) and (f) various switches, (g) and (h) various diodes.

$$\begin{cases} \dfrac{v_o}{V_{in}} = \dfrac{1}{(1-D)^2}\left(1 - \dfrac{r_L}{R}\left(\dfrac{D^2-D+1}{(1-D)^4}\right) - \right. \\ \left. \dfrac{r_S}{R}\left(\dfrac{D+D^2-D^3}{(1-D)^4}\right) - \dfrac{r_D}{R}\left(\dfrac{1-D+D^2}{(1-D)^3}\right)\right) \end{cases} \tag{14}$$

In these equations, r_L, r_S, r_D, and R are the parasitic resistance of the inductor, switch, diode and load. Also, V_o and V_{in} refer to the output and input voltages. Based on the given relationships, the negative values indicate the parasitic effects of the circuit components. Figs. 4(a)-(b) illustrate the voltage gain under both ideal and non-ideal conditions. The figures show that voltage gain values vary inconsistently across all duty cycle percentages. The extent of this inconsistency depends on the output power and the quality of the circuit components. Figs. 4(c)-(j) demonstrate how the voltage gain behaves as different parameters change. These figures show that changing the type of diode has the least impact on voltage gain behaviour.

Efficiency is another essential factor to consider in the non-ideal mode, which is formed by considering the components'

conduction losses and neglecting the frequency losses.

$$\begin{cases} P_L = \dfrac{2-2D+D^2}{(1-D)^4}\dfrac{r_L}{R}P_o \\ P_S = \dfrac{D(2-2D+D^2)}{(1-D)^4}\dfrac{r_s}{R}P_o \\ P_D = \dfrac{2-D}{1-D}v_{DF}I_o \\ \eta = \dfrac{P_o}{P_o+P_L+P_{SC}+P_D} \end{cases} \tag{15}$$

$$\begin{cases} P_L = \dfrac{2-2D+D^2}{(1-D)^4}\dfrac{r_L}{R}P_o \\ P_S = \dfrac{D(2-2D+D^2)}{(1-D)^4}\dfrac{r_s}{R}P_o \\ P_D = \dfrac{1}{1-D}v_{DF}I_o \\ \eta = \dfrac{P_o}{P_o+P_L+P_{SC}+P_D} \end{cases} \tag{16}$$

In these equations, P_L is the conduction loss of the inductors, P_S is the conduction loss of the switches, P_D is the conduction loss of the diodes, and η is the efficiency. These relations define the duty cycle percentage, component quality, and the effect of the output power on the efficiency. In Fig. 5, the efficiency due to changes in output power and component quality can be seen. According to this figure, the output power changes primarily influence efficiency behaviour. It is important to note that the second proposed topology presents lower diode conduction loss due to its structure compared to the first one. In other words, the second inductor current does not cross through the first diode in the second proposed topology. Consequently, its current stress decreases. Considering the highest output power, 50 percent duty cycle, and employing the accessible high qualify components, the extracted efficiency according to the mentioned equations is 91 percent.

IV. SMALL SIGNAL ANALYSIS

A small signal analysis is used to determine the proposed topologies' dynamic behaviour. In this study, the state variables are the current in the inductors and the voltage across the capacitors. The equations for the voltage across the inductors and the current through the capacitors can be used to construct the state space matrices for both the proposed topologies as follows:

$$A = \begin{bmatrix} 0 & 0 & -\frac{1-D}{L_1} & 0 \\ 0 & 0 & \frac{D}{L_2} & -\frac{1-D}{L_2} \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ 0 & \frac{1-D}{C_o} & 0 & \frac{-1}{RC_o} \end{bmatrix} x + \begin{bmatrix} \frac{V_{c1}}{L_1} \\ \frac{V_{c1}+V_o}{L_2} \\ -\frac{I_{L1}+I_{L2}}{C_1} \\ -\frac{I_{L2}}{C_o} \end{bmatrix},$$

$$C^T = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$$

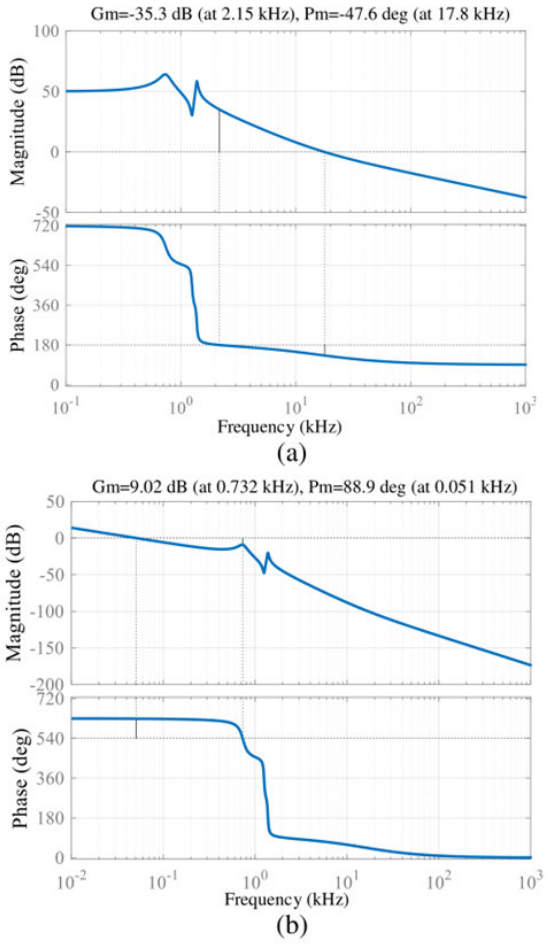

FIGURE 6. Bode diagrams of (a) before compensating, (b) after compensating.

The proposed circuit configurations were analyzed using matrices and the sisotool in MATLAB. The resulting Bode diagrams are shown in Fig. 6(a) for both the proposed converters. It's important to note that these configurations produce discontinuous output current, which makes them non-minimum phase converters. This characteristic is reflected in the negative phase and gain margins as depicted in Fig. 6(a). Subsequently, a compensator was designed using MATLAB sisotool and applied to the matrices. The new Bode diagram, displayed in Fig. 6(b), exhibits positive phase and gain margins.

V. OTHER MEMBERS OF THIS FAMILY

The first and second proposed converters are used to extract the improved topologies, which form the family converter. Figure 8 presents the improved formats. The third proposed topology is the multi-output format of the first proposed converter. The second part of the first proposed topology is in a form that its repeating increases the number of outputs. The rest of the figures in Figure 8 indicate the improved format of the second proposed topology. According to this figure, employing the diode-capacitor and diode inductor-capacitor

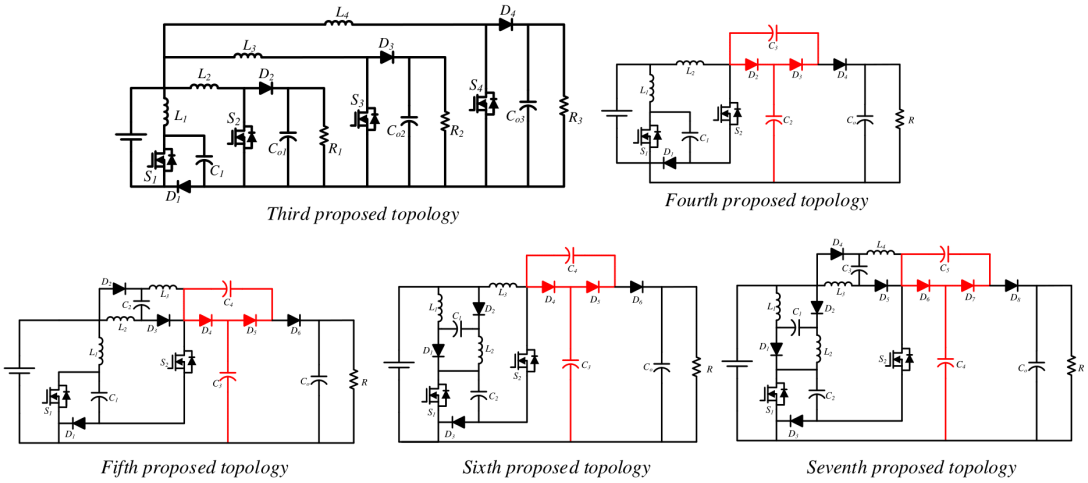

FIGURE 7. The third to seventh proposed topologies.

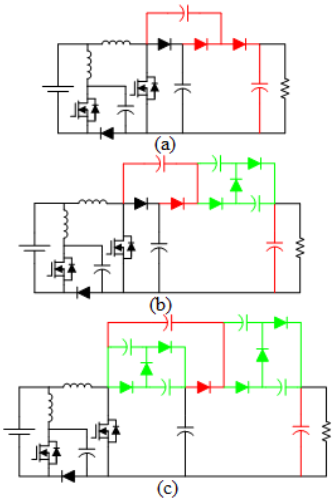

FIGURE 8. The family members: (a) eighth, (b) ninth, (c) tenth extensions.

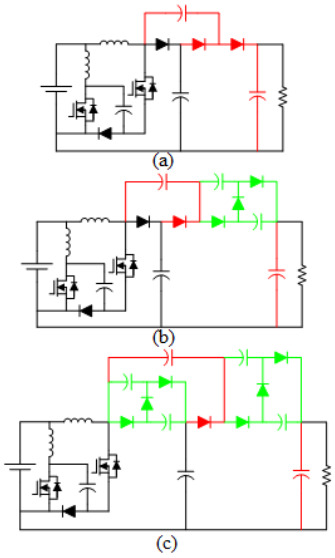

FIGURE 9. The family members: (a) fourth, (b) eleventh, (c) twelfth extensions.

voltage multiplier cells in the proposed topology leads to high voltage providing. The provided voltage gain by the presented topologies in Figures 9(a)-(d) is as follows:

$$\begin{cases} \dfrac{V_o}{V_{in}} = \dfrac{3-D}{(1-D)^2} \\ \dfrac{V_o}{V_{in}} = \dfrac{7-3D}{(1-D)^2} \\ \dfrac{V_o}{V_{in}} = \dfrac{4}{(1-D)^2} \\ \dfrac{V_o}{V_{in}} = \dfrac{10-2D}{(1-D)^2} \end{cases} \tag{17}$$

A 50% duty cycle results in a voltage gain of 10, 22, 16, and 36 times. The input current continuity and input-output common ground are also provided.

Possible extensions of the proposed topologies are not limited to the third to seventh extensions. In other words, the presented extensions can be a base topology for other improved topologies. The presented extensions in Fig. 8, show the combination of the first proposed topologies with diode-capacitor structures. The produced voltage gain by these extensions are as follows for the eighth to the tenth extensions:

$$\begin{cases} G_{8th} = \dfrac{2}{(1-D)^2} \\ G_{9th} = \dfrac{3}{(1-D)^2} \\ G_{10th} = \dfrac{4}{(1-D)^2} \end{cases} \tag{18}$$

Besides the voltage gain increase compared with the first proposed topology, the highest voltage stress of the semiconductors is less than the output voltage. In the eighth

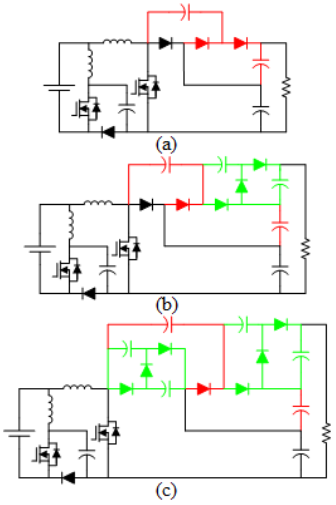

FIGURE 10. The family members: (a) thirteenth, (b) fourteenth, (c) fifteenth extensions.

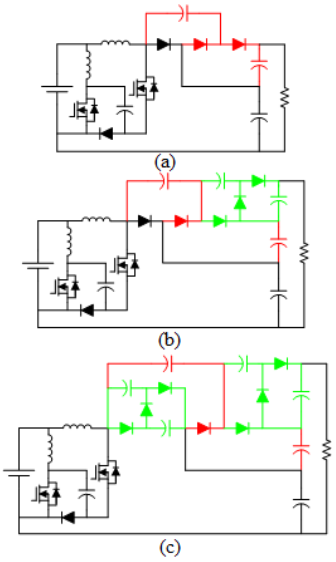

FIGURE 11. The family members: (a) sixteenth, (b) seventeenth, (c) eighteenth extensions.

extension, the highest switch and diode voltage stresses are as follows:

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2} \\ V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{19}$$

It can be understood that the highest voltage stresses are half of the output voltage. In the ninth extension, the highest switch and diode voltage stresses are as follows:

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2} \\ V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{20}$$

According to the extracted values, the highest voltage stresses are one-third of the output voltage in the ninth

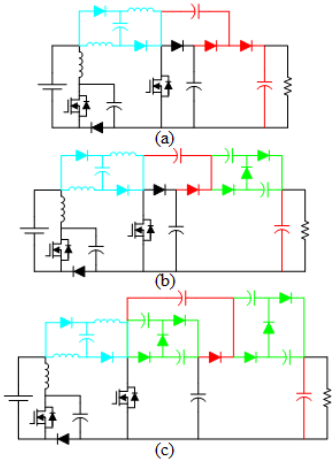

FIGURE 12. The family members: (a) fifth, (b) nineteenth, (c) twentieth extensions.

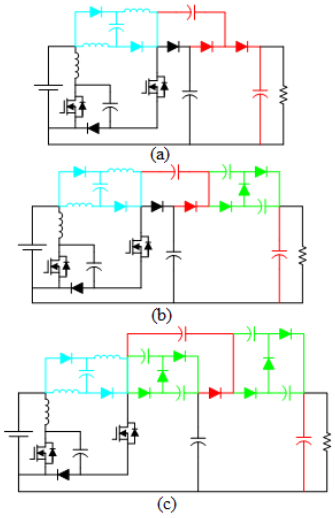

FIGURE 13. The family members: (a) twenty-first, (b) twenty-second, (c) twenty-third extensions.

extension. The highest switch and diode voltage stresses are as follows in the tenth extension:

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2} \\ V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{21}$$

Based on these values, the highest voltage stresses are one-fourth of the output voltage in the tenth extension. The eleventh and twelfth extensions are based on the second proposed topology and are based on the fourth extension. The extracted voltage gain of these extensions (presented in Fig. 9) is as follows:

$$\begin{cases} G_{4th} = \dfrac{3-D}{(1-D)^2} \\ G_{11th} = \dfrac{5-2D}{(1-D)^2} \\ G_{12th} = \dfrac{7-3D}{(1-D)^2} \end{cases} \tag{22}$$

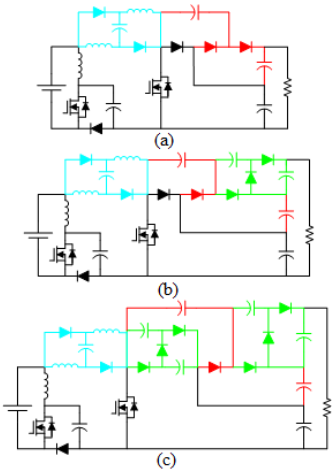

FIGURE 14. The family members: (a) twenty-fourth, (b) twenty-fifth, (c) twenty-sixth extensions.

Comparing these relations with the extracted voltage gains of eighth to tenth extensions shows that the presented extensions in Fig.9 provide a higher voltage gain. Notably, the voltage stress challenge of the semiconductors in the second proposed topology is also solved. Additionally, the highest switch and diode voltage stresses in the fourth, eleventh, and twelfth extensions are as follows, respectively.

$$\begin{cases} Vo_{4th} = \dfrac{3-D}{(1-D)^2} V_{in} \\ Vo_{11th} = \dfrac{5-2D}{(1-D)^2} V_{in} \\ Vo_{12th} = \dfrac{7-3D}{(1-D)^2} V_{in} \end{cases} \tag{23}$$

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2} V_{in} \end{cases} \tag{24}$$

According to the presented equation, the highest voltage stress of the semiconductors is less than the output voltage.

It is good to note that the presented extensions in the previous figures apply their output voltage to a single capacitor at the output terminal. Consequently, the voltage stress of the output capacitors is the same as the output voltage. In order to solve this challenge, the presented extensions in Figs. 10 and 11 are introduced. In these topologies, the stack connection of the capacitors from various parts forms the output terminal of the converters. Moreover, the output terminal capacitors perform a double role in these extensions. The voltage gain of the thirteenth to fifteenth extensions (presented in Fig. 10) is as follows:

$$\begin{cases} G_{13th} = \dfrac{2}{(1-D)^2} \\ G_{14th} = \dfrac{3}{(1-D)^2} \\ G_{15th} = \dfrac{4}{(1-D)^2} \end{cases} \tag{25}$$

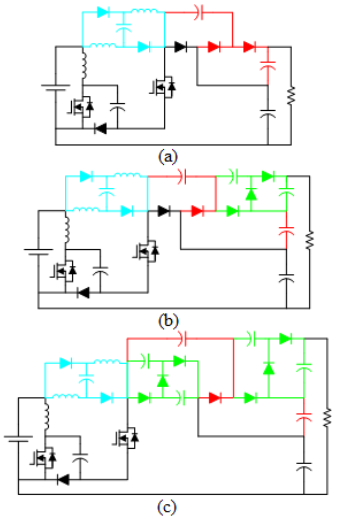

FIGURE 15. The family members: (a) twenty-seventh, (b) twenty-eighth, (c) twenty-ninth extensions.

The highest voltage stress of the switch and diode in these extensions is as follows:

$$\begin{cases} Vo_{13th} = \dfrac{2}{(1-D)^2} V_{in} \\ Vo_{14th} = \dfrac{3}{(1-D)^2} V_{in} \\ Vo_{15th} = \dfrac{4}{(1-D)^2} V_{in} \end{cases} \tag{26}$$

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{V_{in}}{(1-D)^2} \end{cases} \tag{27}$$

It can be understood that the voltage stress challenge of the semiconductors has been solved. The voltage gain of the sixteenth to eighteenth extensions (presented in Fig.11) are as follows:

$$\begin{cases} G_{16th} = \dfrac{3-D}{(1-D)^2} \\ G_{17th} = \dfrac{5-2D}{(1-D)^2} \\ G_{18th} = \dfrac{7-3D}{(1-D)^2} \end{cases} \tag{28}$$

The highest voltage stress of the switches and diodes are as follows for the sixteenth to eighteenth extensions:

$$\begin{cases} Vo_{16th} = \dfrac{3-D}{(1-D)^2} V_{in} \\ Vo_{17th} = \dfrac{5-2D}{(1-D)^2} V_{in} \\ Vo_{18th} = \dfrac{7-3D}{(1-D)^2} V_{in} \end{cases} \tag{29}$$

$$\begin{cases} V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{V_{in}}{(1-D)^2}, V_{Dmax} = \dfrac{2-D}{(1-D)^2}V_{in} \end{cases} \tag{30}$$

The presented extensions in Fig.12 are according to the fifth proposed topology. The fifth, nineteenth, and twentieth extensions have been presented in Fig.12. The extracted voltage gain of these extensions are as follows, respectively.

$$\begin{cases} G_{5th} = \dfrac{2(3-D)}{(1-D)^2} \\ G_{19th} = \dfrac{3(3-D)}{(1-D)^2} \\ G_{20th} = \dfrac{4(3-D)}{(1-D)^2} \end{cases} \tag{31}$$

The highest voltage stress of the switch and diodes are as follows:

$$\begin{cases} Vo_{5th} = \dfrac{2(3-D)}{(1-D)^2}V_{in} \\ Vo_{19th} = \dfrac{3(3-D)}{(1-D)^2}V_{in} \\ Vo_{20th} = \dfrac{4(3-D)}{(1-D)^2}V_{in} \end{cases} \tag{32}$$

$$\begin{cases} V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \end{cases} \tag{33}$$

It can be understood that the voltage gain has increased properly, and the challenge of the semiconductors' voltage stresses has been solved. Additionally, as same as the first proposed topology, the common ground of the load and input source is absent. This challenge has been solved in the presented extensions of Fig.13. The twenty-first to twenty-third extensions have solved the absence of the common ground between load and input source. The extracted voltage gain from these topologies are as follows, respectively.

$$\begin{cases} G_{21st} = \dfrac{7-3D}{(1-D)^2} \\ G_{22nd} = \dfrac{10-4D}{(1-D)^2} \\ G_{23rd} = \dfrac{13-5D}{(1-D)^2} \end{cases} \tag{34}$$

The highest voltage stress of the switch and diode are follows:

$$\begin{cases} Vo_{21st} = \dfrac{7-3D}{(1-D)^2}V_{in} \\ Vo_{22nd} = \dfrac{10-4D}{(1-D)^2}V_{in} \\ Vo_{23rd} = \dfrac{13-5D}{(1-D)^2}V_{in} \end{cases} \tag{35}$$

$$\begin{cases} V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \end{cases} \tag{36}$$

It can be understood that the challenge of the semiconductors' voltage stresses has been solved.

The presented extensions in Figs. 14 and 15 solve the challenge of output terminal capacitors' voltage stress. The provided voltage gain and the semiconductors' highest voltage stress of the corresponding topologies in Fig. 14 are as follows:

$$\begin{cases} G_{24th} = \dfrac{2(3-D)}{(1-D)^2} \\ G_{25th} = \dfrac{3(3-D)}{(1-D)^2} \\ G_{26th} = \dfrac{4(3-D)}{(1-D)^2} \end{cases} \tag{37}$$

$$\begin{cases} Vo_{24th} = \dfrac{2(3-D)}{(1-D)^2}V_{in} \\ Vo_{25th} = \dfrac{3(3-D)}{(1-D)^2}V_{in} \\ Vo_{26th} = \dfrac{4(3-D)}{(1-D)^2}V_{in} \end{cases} \tag{38}$$

$$\begin{cases} V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{3-D}{(1-D)^2}V_{in} \end{cases} \tag{39}$$

The provided voltage gain and the semiconductors' highest voltage stress of the corresponding topologies in Fig. 15 are as follows:

$$\begin{cases} G_{27th} = \dfrac{7-3D}{(1-D)^2} \\ G_{28th} = \dfrac{10-4D}{(1-D)^2} \\ G_{29th} = \dfrac{13-5D}{(1-D)^2} \end{cases} \tag{40}$$

$$\begin{cases} Vo_{27th} = \dfrac{7-3D}{(1-D)^2}V_{in} \\ Vo_{28th} = \dfrac{10-4D}{(1-D)^2}V_{in} \\ Vo_{29th} = \dfrac{13-5D}{(1-D)^2}V_{in} \end{cases} \tag{41}$$

$$\begin{cases} V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{3-D}{(1-D)^2}V_{in}, V_{Dmax} = \dfrac{4-2D}{(1-D)^2}V_{in} \end{cases} \tag{42}$$

The presented extensions in Figs. 16 to 19 have used the same idea in the illustrated extensions in Figs. 12 to 15. However, the presented topologies in Figs. 16 to 19 use an inductor-diode-based voltage multiplier cell instead of the

inductor. The extracted voltage gain and maximum voltage stress of the semiconductors in Fig. 16 are as follows:

$$\begin{cases} G_{30th} = \dfrac{2(1+2D-D^2)}{(1-D)^2} \\ G_{31st} = \dfrac{3(1+2D-D^2)}{(1-D)^2} \\ G_{32nd} = \dfrac{4(1+2D-D^2)}{(1-D)^2} \end{cases} \tag{43}$$

$$\begin{cases} Vo_{30th} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ Vo_{31st} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ Vo_{32nd} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \end{cases} \tag{44}$$

$$\begin{cases} V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \end{cases} \tag{45}$$

The voltage gain and voltage stress of the semiconductors in the presented topologies of Fig. 17 are as follows:

$$\begin{cases} G_{33rd} = \dfrac{3+3D-2D^2}{(1-D)^2} \\ G_{34th} = \dfrac{5+4D-3D^2}{(1-D)^2} \\ G_{35th} = \dfrac{7+5D-4D^2}{(1-D)^2} \end{cases} \tag{46}$$

$$\begin{cases} Vo_{33rd} = \dfrac{3+3D-2D^2}{(1-D)^2} V_{in} \\ Vo_{34th} = \dfrac{5+4D-3D^2}{(1-D)^2} V_{in} \\ Vo_{35th} = \dfrac{7+5D-4D^2}{(1-D)^2} V_{in} \end{cases} \tag{47}$$

$$\begin{cases} V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \end{cases} \tag{48}$$

The presented topologies in Fig. 18 provide their voltage gain and highest voltage stress of the semiconductors as follows:

$$\begin{cases} G_{36th} = \dfrac{2(1+2D-D^2)}{(1-D)^2} \\ G_{37th} = \dfrac{3(1+2D-D^2)}{(1-D)^2} \\ G_{38th} = \dfrac{4(1+2D-D^2)}{(1-D)^2} \end{cases} \tag{49}$$

$$\begin{cases} Vo_{36th} = \dfrac{2(1+2D-D^2)}{(1-D)^2} V_{in} \\ Vo_{37th} = \dfrac{3(1+2D-D^2)}{(1-D)^2} V_{in} \\ Vo_{38th} = \dfrac{4(1+2D-D^2)}{(1-D)^2} V_{in} \end{cases} \tag{50}$$

$$\begin{cases} V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in} \end{cases} \tag{51}$$

The presented topologies in Fig. 19 provide their voltage gain and highest voltage stress of the semiconductors as follows:

$$\begin{cases} G_{39th} = \dfrac{3+3D-2D^2}{(1-D)^2} \\ G_{40th} = \dfrac{5+4D-3D^2}{(1-D)^2} \\ G_{41st} = \dfrac{7+5D-4D^2}{(1-D)^2} \end{cases} \tag{52}$$

$$\begin{cases} Vo_{39th} = \dfrac{3+3D-2D^2}{(1-D)^2} V_{in} \\ Vo_{40th} = \dfrac{5+4D-3D^2}{(1-D)^2} V_{in} \\ Vo_{41st} = \dfrac{7+5D-4D^2}{(1-D)^2} V_{in} \end{cases} \tag{53}$$

$$\begin{cases} V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \\ V_{Smax} = \dfrac{1+2D-D^2}{(1-D)^2} V_{in}, V_{Dmax} = \dfrac{2+D-D^2}{(1-D)^2} V_{in} \end{cases} \tag{54}$$

The presented topologies in Figs. 20 to 23 employ two inductor-capacitor-diode-based VMCs instead of the inductors in the first and second proposed topologies. The extracted voltage gain and the highest voltage stress of the switch and diodes in the topologies of Fig. 20 are as follows:

$$\begin{cases} G_{42nd} = \dfrac{8}{(1-D)^2} \\ G_{43rd} = \dfrac{12}{(1-D)^2} \\ G_{44th} = \dfrac{16}{(1-D)^2} \end{cases} \tag{55}$$

$$\begin{cases} Vo_{42nd} = \dfrac{8}{(1-D)^2} V_{in} \\ Vo_{43rd} = \dfrac{12}{(1-D)^2} V_{in} \\ Vo_{44th} = \dfrac{16}{(1-D)^2} V_{in} \end{cases} \tag{56}$$

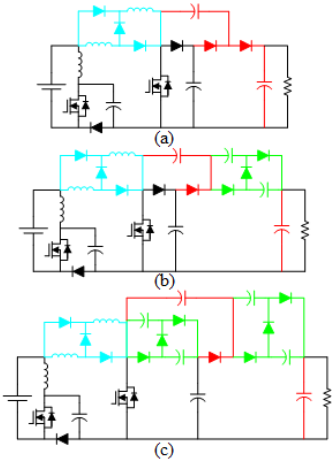

FIGURE 16. The family members: (a) thirtieth, (b) thirty-first, (c) thirty-second extensions.

$$\begin{cases} V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \end{cases} \tag{57}$$

The presented topologies in Fig. 21 provide the voltage gain and the highest voltage stress of the semiconductors as follows:

$$\begin{cases} G_{7th} = \dfrac{10-2D}{(1-D)^2} \\ G_{45th} = \dfrac{16-4D}{(1-D)^2} \\ G_{46th} = \dfrac{22-6D}{(1-D)^2} \end{cases} \tag{58}$$

$$\begin{cases} Vo_{7th} = \dfrac{10-2D}{(1-D)^2}V_{in} \\ Vo_{45th} = \dfrac{16-4D}{(1-D)^2}V_{in} \\ Vo_{46th} = \dfrac{22-6D}{(1-D)^2}V_{in} \end{cases} \tag{59}$$

$$\begin{cases} V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \end{cases} \tag{60}$$

The presented topologies in Fig. 22 provide the voltage gain and the highest voltage stress of the semiconductors as follows:

$$\begin{cases} G_{47th} = \dfrac{8}{(1-D)^2} \\ G_{48th} = \dfrac{12}{(1-D)^2} \\ G_{49th} = \dfrac{16}{(1-D)^2} \end{cases} \tag{61}$$

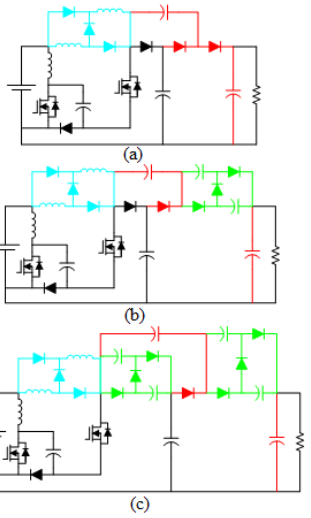

FIGURE 17. The family members: (a) thirty-third, (b) thirty-fourth, (c) thirty-fifth extensions.

$$\begin{cases} Vo_{47th} = \dfrac{8}{(1-D)^2}V_{in} \\ Vo_{48th} = \dfrac{12}{(1-D)^2}V_{in} \\ Vo_{49th} = \dfrac{16}{(1-D)^2}V_{in} \end{cases} \tag{62}$$

$$\begin{cases} V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{4}{(1-D)^2}V_{in} \end{cases} \tag{63}$$

The voltage gain and the highest voltage stress of the semiconductors in the topologies of Fig. 23 are as follows:

$$\begin{cases} G_{50th} = \dfrac{10-2D}{(1-D)^2} \\ G_{51st} = \dfrac{16-4D}{(1-D)^2} \\ G_{52nd} = \dfrac{22-6D}{(1-D)^2} \end{cases} \tag{64}$$

$$\begin{cases} Vo_{50th} = \dfrac{10-2D}{(1-D)^2}V_{in} \\ Vo_{51st} = \dfrac{16-4D}{(1-D)^2}V_{in} \\ Vo_{52nd} = \dfrac{22-6D}{(1-D)^2}V_{in} \end{cases} \tag{65}$$

$$\begin{cases} V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \\ V_{Smax} = \dfrac{4}{(1-D)^2}V_{in},\ V_{Dmax} = \dfrac{6-2D}{(1-D)^2}V_{in} \end{cases} \tag{66}$$

The presented topologies in Figs. 24 to 27 use two inductor-diode-based VMCs instead of the inductors in the first and second proposed topologies. The voltage gain and

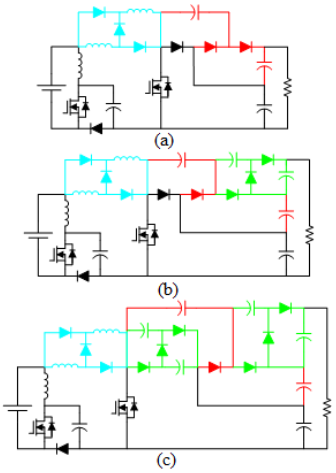

FIGURE 18. The family members: (a) thirty-sixth, (b) thirty-seventh, (c) thirty-eighth extensions.

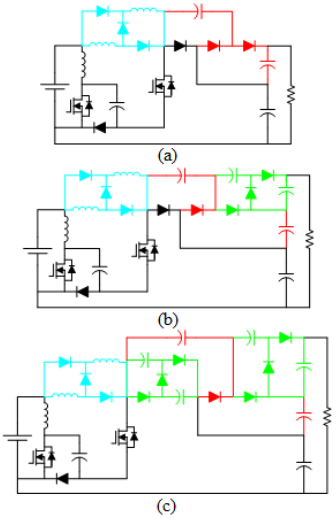

FIGURE 19. The family members: (a) thirty-ninth, (b) fortieth, (c) forty-first extensions.

the highest voltage stress of the semiconductors in the topologies of Fig. 24 are as follows:

$$\begin{cases} G_{53rd} = 2\left(\dfrac{1+D}{1-D}\right)^2 \\ G_{54th} = 3\left(\dfrac{1+D}{1-D}\right)^2 \\ G_{55th} = 4\left(\dfrac{1+D}{1-D}\right)^2 \end{cases} \tag{67}$$

$$\begin{cases} Vo_{53rd} = 2\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ Vo_{54th} = 3\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ Vo_{55th} = 4\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \end{cases} \tag{68}$$

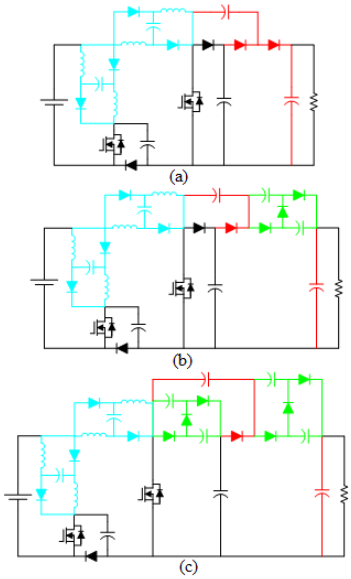

FIGURE 20. The family members: (a) forty-second, (b) forty-third, (c) forty-fourth extensions.

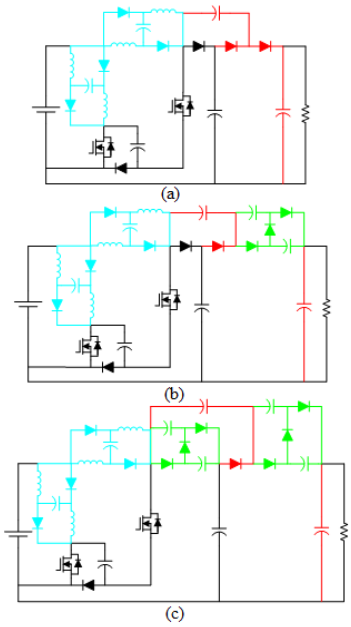

FIGURE 21. The family members: (a) seventh, (b) forty-fifth, (c) forty-sixth extensions.

$$\begin{cases} V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \end{cases} \tag{69}$$

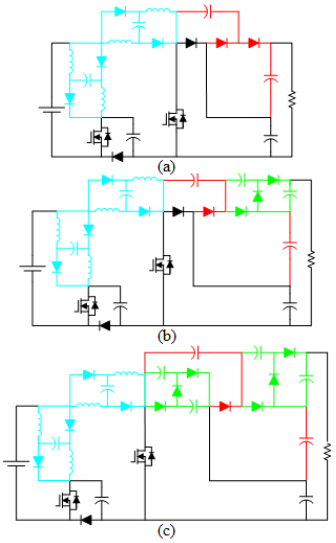

FIGURE 22. The family members: (a) forty-seventh, (b) forty-eighth, (c) forty-ninth extensions.

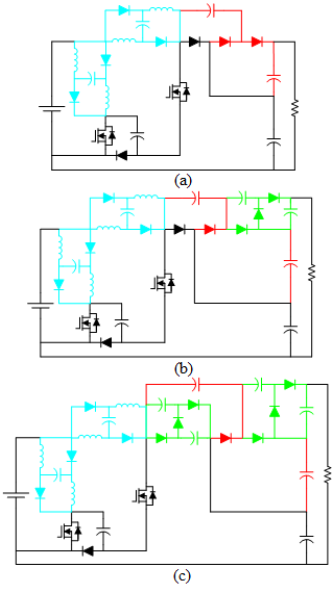

FIGURE 23. The family members: (a) fiftieth, (b) fifty-first, (c) fifty-second extensions.

The voltage gain and the highest voltage stress of the semiconductors in the topologies of Fig. 25 are as follows:

$$\begin{cases} G_{56th} = \dfrac{(1+D)(3+D)}{(1-D)^2} \\ G_{57th} = \dfrac{(1+D)(5+D)}{(1-D)^2} \\ G_{58th} = \dfrac{(1+D)(7+D)}{(1-D)^2} \end{cases} \tag{70}$$

$$\begin{cases} Vo_{56th} = \dfrac{(1+D)(3+D)}{(1-D)^2} V_{in} \\ Vo_{57th} = \dfrac{(1+D)(5+D)}{(1-D)^2} V_{in} \\ Vo_{58th} = \dfrac{(1+D)(7+D)}{(1-D)^2} V_{in} \end{cases} \tag{71}$$

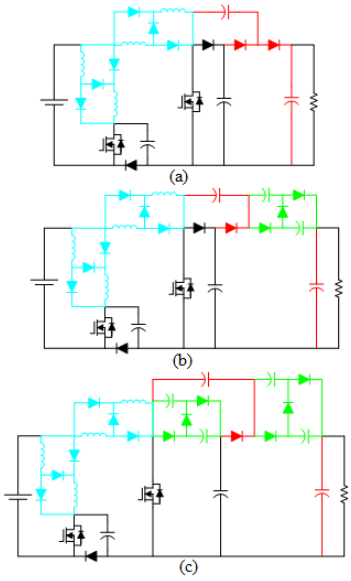

FIGURE 24. The family members: (a) fifty-third, (b) fifty-fourth, (c) fifty-fifth extensions.

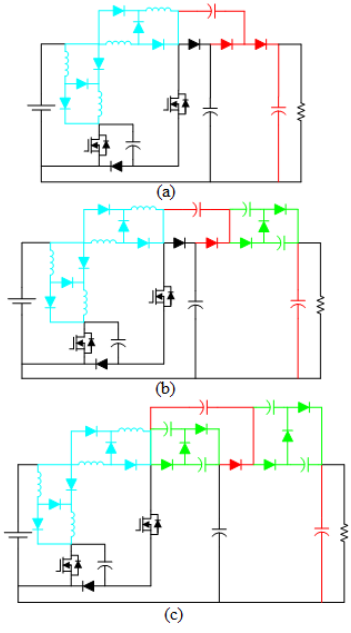

FIGURE 25. The family members: (a) fifty-sixth, (b) fifty-seventh, (c) fifty-eighth extensions.

$$\begin{cases} V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in},\ V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in},\ V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in},\ V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \end{cases} \tag{72}$$

The voltage gain and the highest voltage stress of the semiconductors in the topologies of Fig. 26 are

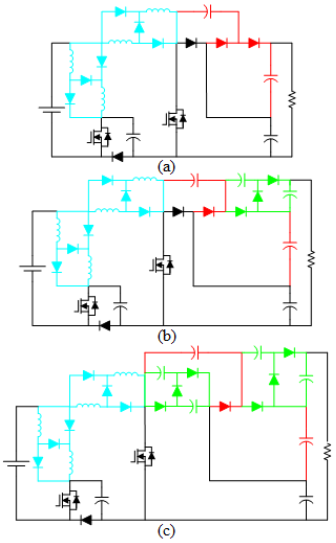

FIGURE 26. The family members: (a) fifty-ninth, (b) sixtieth, (c) sixty-first extensions.

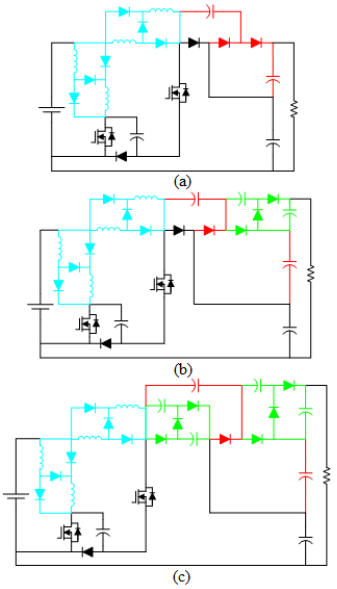

FIGURE 27. The family members: (a) sixty-second, (b) sixty-third, (c) sixty-fourth extensions.

as follows:

$$\begin{cases} G_{59th} = 2\left(\dfrac{1+D}{1-D}\right)^2 \\ G_{60th} = 3\left(\dfrac{1+D}{1-D}\right)^2 \\ G_{61st} = 4\left(\dfrac{1+D}{1-D}\right)^2 \end{cases} \tag{73}$$

$$\begin{cases} Vo_{59th} = 2\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ Vo_{60th} = 3\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ Vo_{61st} = 4\left(\dfrac{1+D}{1-D}\right)^2 V_{in} \end{cases} \tag{74}$$

$$\begin{cases} V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in} \end{cases} \tag{75}$$

The voltage gain and the highest voltage stress of the semiconductors in the topologies of Fig. 27 are as follows:

$$\begin{cases} G_{62nd} = \dfrac{(1+D)(3+D)}{(1-D)^2} \\ G_{63rd} = \dfrac{(1+D)(5+D)}{(1-D)^2} \\ G_{64th} = \dfrac{(1+D)(7+D)}{(1-D)^2} \end{cases} \tag{76}$$

$$\begin{cases} Vo_{62nd} = \dfrac{(1+D)(3+D)}{(1-D)^2} V_{in} \\ Vo_{63rd} = \dfrac{(1+D)(5+D)}{(1-D)^2} V_{in} \\ Vo_{64th} = \dfrac{(1+D)(7+D)}{(1-D)^2} V_{in} \end{cases} \tag{77}$$

$$\begin{cases} V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \\ V_{Smax} = \left(\dfrac{1+D}{1-D}\right)^2 V_{in}, V_{Dmax} = \dfrac{2(1+D)}{(1-D)^2} V_{in} \end{cases} \tag{78}$$

According to the 64 discussed topologies, the employed diode-capacitor structures increase the voltage gain of the main topologies and decrease the voltage stress of the semiconductors. Notably, the diode-capacitor structures with a stacked form solved the dramatic voltage stress challenge of the output terminal capacitors. This achievement was gotten in the presented topologies of Figs. 10, 11, 14, 15, 18, 19, 22, 23, 26, 27. Moreover, the output terminal capacitors in the mentioned diode-capacitor structures have a double performance. In other words, these capacitors perform another role in the various levels of the converter. Employing inductor-based VMCs instead of the inductors in the main topologies brings two achievements. The first achievement is their voltage lift effect in the voltage gain, which increases the voltage gain more than before. The second achievement is decreasing the conduction loss of the inductors. Notably, in one of the operating modes, the inductors of these VMCs become parallel with each other. Consequently, the input current is divided into more paths. Additionally, the crossing current through the inductors will be more less than the input current, which is the highest current of the converter. Such a

feature leads to a conduction loss, which is one-fourth of the state of crossing the input current through an inductor or a single path.

VI. APPLICATION

The DC-DC converter can support various applications. In this study, a huge number of topologies have been proposed. Notably, depending on the family members' voltage gain capability, various applications can be suggested. The first and second proposed topologies can be used in the series connection of the photovoltaic panels as a solar power optimizer. The input current's continuity and step-up behavior make them suitable for photovoltaic applications. The fourth to sixty-fourth extensions are suitable for HID lamps. This kind of lamp requires a high input voltage and a low input current. However, the voltage of the batteries in all kinds of cars is limited. Consequently, the battery voltage of the car can not satisfy these lamps alone. This condition makes the field ready to employ high-gain DC-DC converters. Notably, the mentioned extensions can provide a wide range of high-output voltages. Therefore, they can satisfy the requirements of all kinds of HID lamps. The other application that requires a high voltage is water electrolyzing to generate hydrogen. Hydrogen can be used in a fuel cell to generate electrical energy or can be used as a clean fuel, which results in water as the outcome of the combustion. Notably, the water can be electrolyzed with a 10 V DC voltage. But, applying this voltage to electrodes is a low-efficiency procedure. In this condition, the population of the bubbles around the electrodes is high and reduces the rate of hydrogen generation. Notably, this procedure can be improved by applying a pulsed high voltage, whose average is around 10 V. Additionally, such a pulsed high voltage can be easily provided by the 19th to 64th extensions from a low DC voltage source, which is very accessible. The provided high DC voltage by the mentioned converters can be applied to a pulsed converter to create the mentioned pulsed output voltage. The other application that needs a high voltage with a low and negligible current is the Partial discharge (PD) tests. During the PD test of a dielectric or extracting the tg(δ) characteristic of the dielectric, a high AC voltage with a frequency variety of 0.0001 Hz to 1000 Hz must be applied to the dielectric in a determined procedure. It is good to note that the mentioned AC voltage providing is not a simple issue. In other words, providing a high voltage with a low or high frequency is challenging. An answer to this challenge is using 42nd to 64th extensions to provide a high DC voltage from the accessible DC low voltage sources. Then, apply this voltage to an inverter to provide an AC voltage with the desired frequency. The symbolic presentation of the mentioned applications has been presented in Figs. 28 to 30.

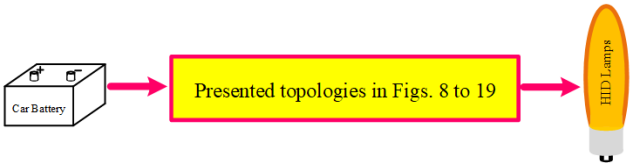

FIGURE 28. Employing the proposed topologies in HID lamps.

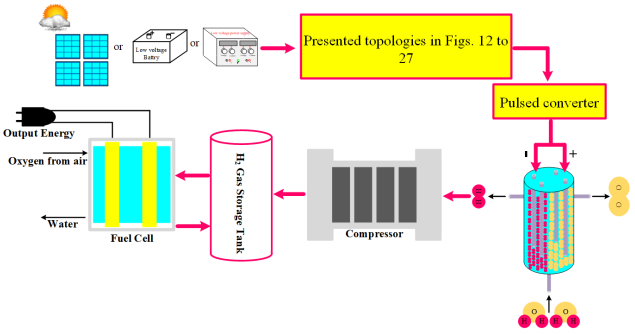

FIGURE 29. Employing the proposed topologies in water electrolyzing and green hydrogen.

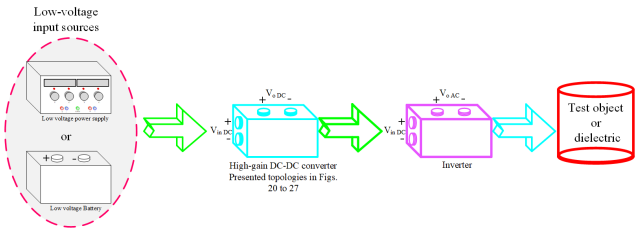

FIGURE 30. Employing the proposed topologies in the partial discharge (PD) test of dielectric.

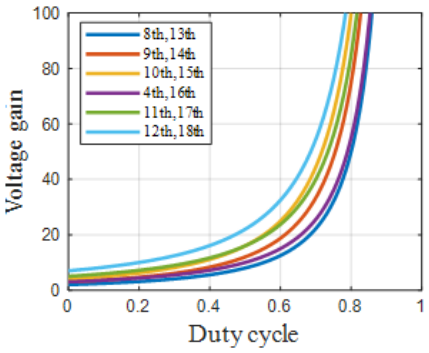

FIGURE 31. The voltage gain comparison of the presented topologies in Figs. 8 to 11.

VII. COMPARISON OF THE FAMILY MEMBERS WITH EACH OTHER

In this section, the proposed topologies and their extensions are compared with each other. The first factor, which can be discussed about the proposed topologies, is their voltage gain. Fig.31 presents the voltage gain comparison of the presented topologies in Figs. 8 to 11. According to this figure, the provided voltage gain by the 12th and 18th extensions has the highest value in this group. Fig.32 presents the voltage gain comparison of the presented topologies in Figs. 12 to 15. Based on the presented curves in this figure, the 23rd and 29th extensions provide the highest voltage gain in this group.

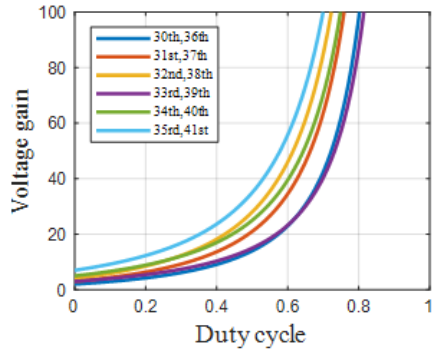

FIGURE 32. The voltage gain comparison of the presented topologies in Figs. 12 to 15.

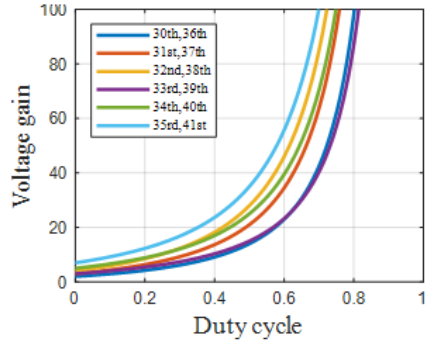

FIGURE 33. The voltage gain comparison of the presented topologies in Figs. 16 to 19.

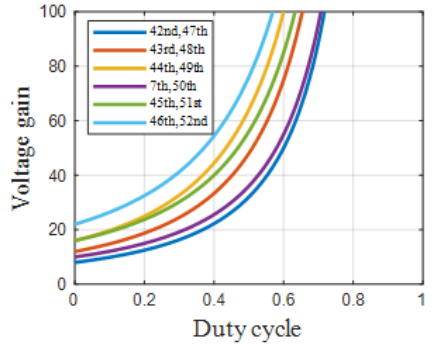

FIGURE 34. The voltage gain comparison of the presented topologies in Figs. 20 to 23.

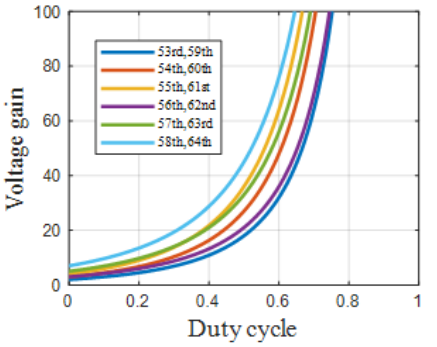

FIGURE 35. The voltage gain comparison of the presented topologies in Figs. 24 to 27.

TABLE 1. Components number.

Topologies	Inductor	Capacitor	Switch	Diode	$\frac{V_o}{V_{in}}$
1st Proposed	2	2	2	2	$\frac{1}{(1-D)^2}$
2nd Proposed	2	2	2	2	$\frac{1}{(1-D)^2}$
[6]	1	3	1	3	$\frac{2}{1-D}$
[7]	2	2	2	2	$\left(\frac{D}{1-D}\right)^2$
[8]	2	2	2	2	$\frac{D(2-D)}{(1-D)^2}$
[9]	3	3	1	3	$\frac{D}{(1-D)^2}$
[10]	2	2	1	3	$\frac{1}{(1-D)^2}$
[11]	3	4	1	2	$\frac{2D}{1-D}$
[12]	2	2	2	2	$\frac{D}{(1-D)^2}$
[13]	3	3	1	3	$\frac{D}{(1-D)^2}$
[14]	2	2	2	2	$\frac{1}{(1-D)^2}$
[15]	2	2	1	3	$\frac{D(2-D)}{(1-D)^2}$
[16]	3	4	2	3	$\frac{2D}{(1-D)^2}$
[17]	2	2	1	3	$\frac{1}{(1-D)^2}$
[18]	3	3	2	2	$\left(\frac{D}{1-D}\right)^2$
[19]	2	2	1	3	$\frac{2}{1-D}$
[20]	2	3	2	3	$\frac{2D}{(1-D)^2}$
[21]	2	3	1	2	$\frac{1+D}{1-D}$
[22]	2	3	1	2	$\frac{1}{1-2D}$
[23]	2	2	2	2	$\left(\frac{D}{1-D}\right)^2$

Fig.33 presents the voltage gain comparison of the presented topologies in Figs. 16 to 19. It can be understood that the provided voltage gain by the 35th and 41st topologies is the highest in this group. Fig.34 presents the voltage gain comparison of the presented topologies in Figs. 20 to 23. According to this figure, the extracted voltage gain from the 46th and 52nd topologies is the highest. Fig.35 presents the voltage gain comparison of the presented topologies in Figs. 24 to 27. According to this figure, the provided voltage gain of the 58th and 64th topologies is the highest in this group. Fig.36 presents the voltage gain comparison of the 12th, 18th, 23rd, 29th, 35th, 41st, 46th, 52nd, 58th, and 64th topologies. According to this figure, the 46th and 52nd extensions have the highest voltage gain among the other family members. To see the capability of the 46th and 52nd extensions, their voltage gain density according to each component type number and all component numbers have been presented in Fig.37. According to Fig. 37(a), the voltage gain density over the inductors' number is between 50 to 19 at the low percentages of the duty cycle. Additionally, according to Fig. 37(b), the voltage gain density over the capacitors' number is between 2.2 and 7.6, while the duty cycle percentage is less than 50 percent. Fig. 37(c) presents

TABLE 2. Voltage gain, the highest switch and diode voltage stress.

Topologies	$\frac{V_o}{v_{in}}$	V_{Smax}	V_{Dmax}
52nd extension	$\frac{22-6D}{(1-D)^2}$	$\frac{4}{(1-D)^2}V_{in}$	$\frac{6-2D}{(1-D)^2}V_{in}$
[24]	$\frac{4}{1-D}$	$\frac{2}{1-D}V_{in}$	$\frac{2}{1-D}V_{in}$
[25]	$\frac{4}{1-D}$	$\frac{2}{1-D}V_{in}$	$\frac{2}{1-D}V_{in}$
[26]	$\frac{(1+D)^2}{1-D}$	$\frac{1+D}{1-D}V_{in}$	$\frac{1+D}{1-D}V_{in}$
[27]	$\frac{2+D}{1-D}$	$\frac{2}{1-D}V_{in}$	$\frac{2}{1-D}V_{in}$
[28]	$\frac{2+D}{1-D}$	$\frac{1}{1-D}V_{in}$	$\frac{1}{1-D}V_{in}$
[29]	$\frac{2-D}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[30]	$\frac{1+D}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[31]	$\frac{2}{(1-D)^2}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[32]	$\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[33]	$\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[34]	$\frac{2}{(1-D)^2}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[35]	$\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[36]	$\frac{3-D}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{2-D}{(1-D)^2}V_{in}$
[37]	$\frac{3-D}{(1-D)^2}$	$\frac{1}{(1-D)^2}V_{in}$	$\frac{1}{(1-D)^2}V_{in}$
[38]	$\frac{3-D}{(1-D)^2}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[39]	$\frac{3-D}{(1-D)^2}$	$\frac{3-D}{(1-D)^2}V_{in}$	$\frac{3-D}{(1-D)^2}V_{in}$
[40]	$\frac{2(2-D)}{(1-D)^2}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[41]	$\frac{2(2-D)}{(1-D)^2}$	$\frac{2-D}{(1-D)^2}V_{in}$	$\frac{2-D}{(1-D)^2}V_{in}$

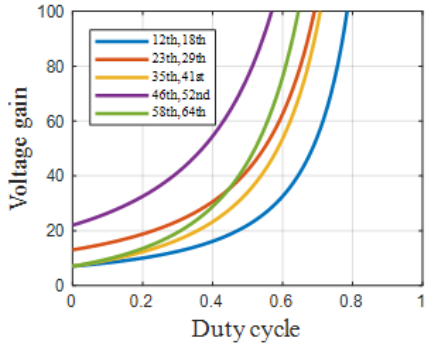

FIGURE 36. The voltage gain comparison of the best converters of Figs. 8 to 27.

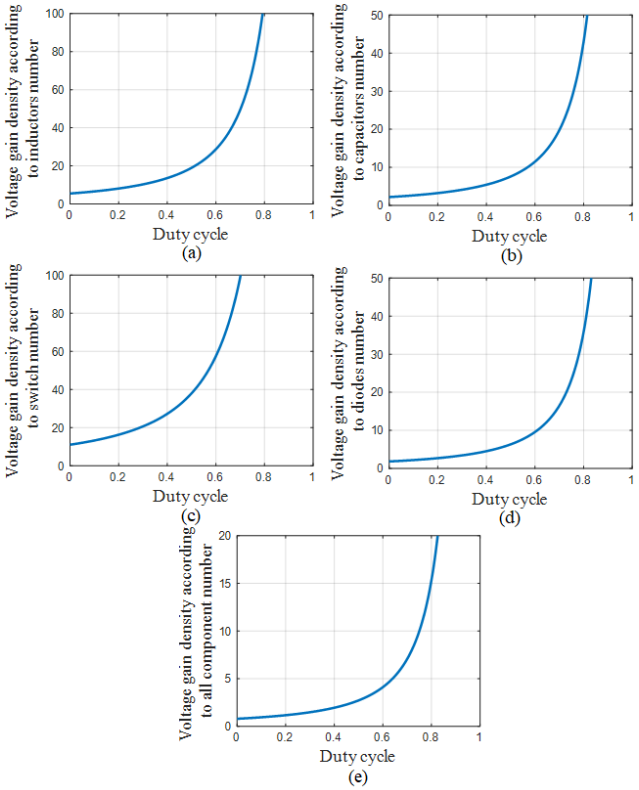

FIGURE 37. Voltage gain density of 52nd extension according to the: (a) inductors number, (b) capacitors number, (c) switch number, (d) diodes number, (e) whole components number.

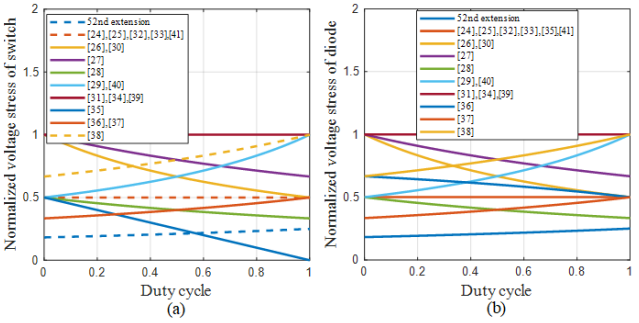

FIGURE 38. Comparison of the: (a) normalized voltage stress of the switch among [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] and 52nd extension, (b) normalized voltage stress of the diode among [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] and 52nd extension.

the voltage gain density over the switch numbers. Based on this figure, the voltage gain density over the switch number is 11 to 38, while the duty cycle percentage is less than 50 percent. Fig. 37(d) presents the voltage gain density over the diode number. It can be understood that the extracted values are between 1.8 to 6.33 while the duty cycle is less than 50 percent. Fig.37(e) presents the voltage gain density over the number of whole components. According to this figure, this density is between 0.78 and 2.7, while the duty cycle is less than 50 percent. All these results show the superiority of the converters' design in providing voltage gain.

VIII. COMPARISON WITH RECENTLY SUGGESTED CONVERTERS

In the first step of the comparison, the first and second proposed topologies are compared with the presented topologies in [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17],

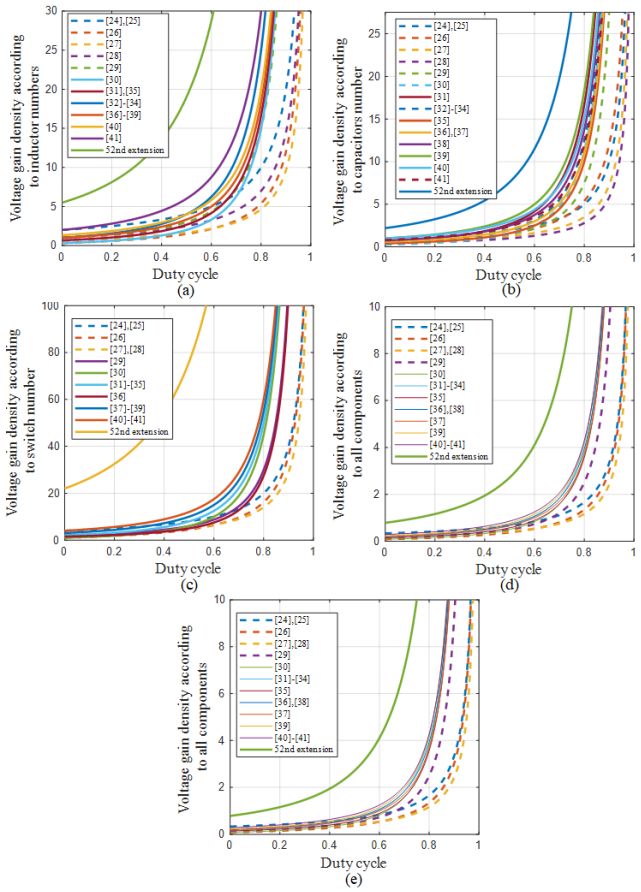

FIGURE 39. Voltage gain density comparison of the 52nd extension and [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] according to: (a) inductors number, (b) capacitors number, (c) switch number, (d) diodes number, (e) whole components number.

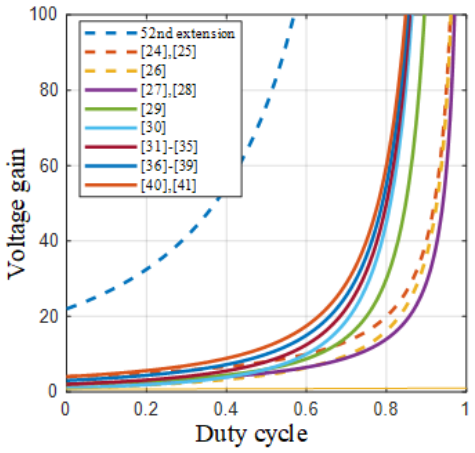

FIGURE 40. Voltage gain comparison of the 52nd extension and [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41].

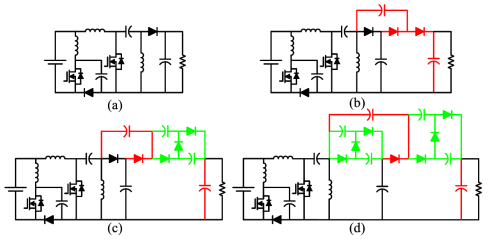

FIGURE 41. First group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

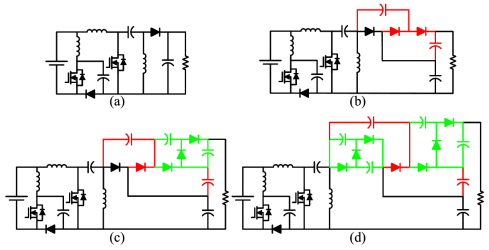

FIGURE 42. Second group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

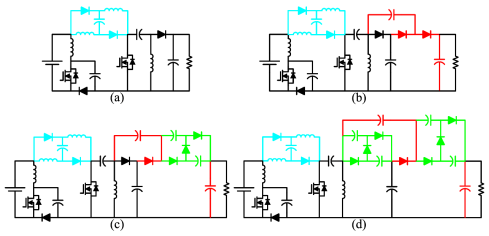

FIGURE 43. Third group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

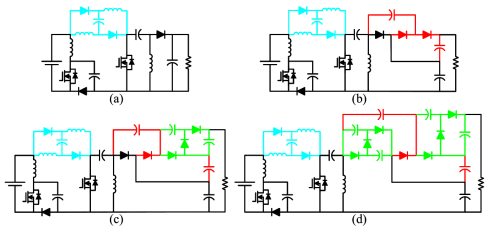

FIGURE 44. Fourth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

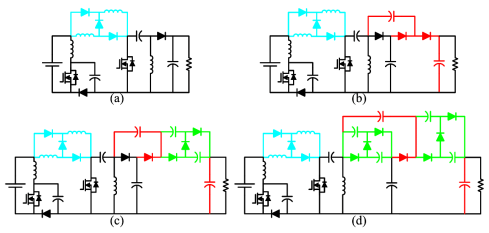

FIGURE 45. Fifth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

[18], [19], [20], [21], [22], and [23]. Table 1 compares the first and second proposed topologies concerning their components number and the voltage gain value. According to this table, the voltage gain of the first and second proposed topologies is more than [6], [7], [8], [9], [11], [12], [13], [15], [16],

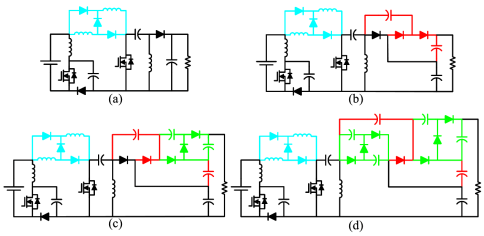

FIGURE 46. Sixth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

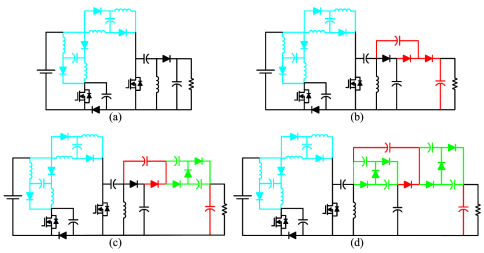

FIGURE 47. Seventh group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

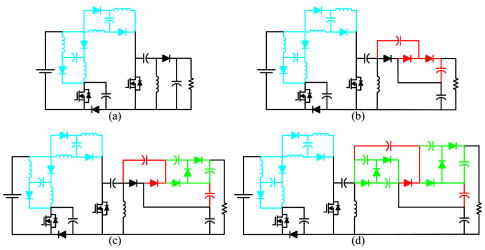

FIGURE 48. Eighth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

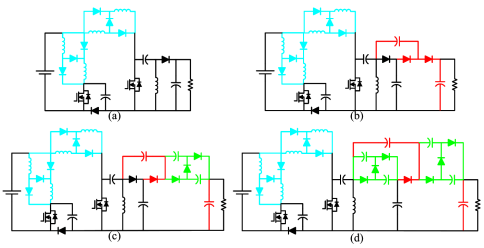

FIGURE 49. Ninth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

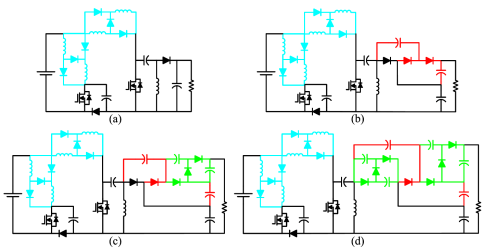

FIGURE 50. Tenth group of SEPIC-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

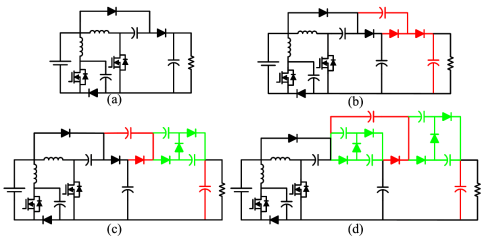

FIGURE 51. First group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

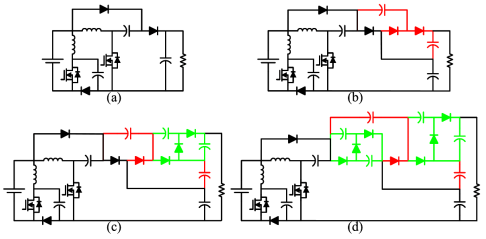

FIGURE 52. Second group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

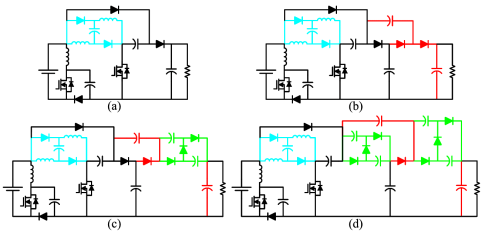

FIGURE 53. Third group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

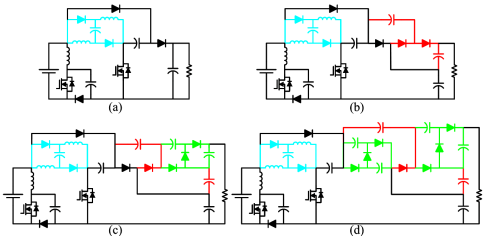

FIGURE 54. Fourth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

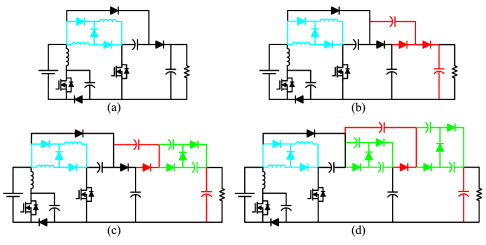

FIGURE 55. Fifth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

[18], [19], [20], [21], [22], [23], and the same as [10], [14], and [17]. Additionally, the component number of the first and second proposed topologies is less than in [9], [11], [13], [16], [18], [20], and [22].

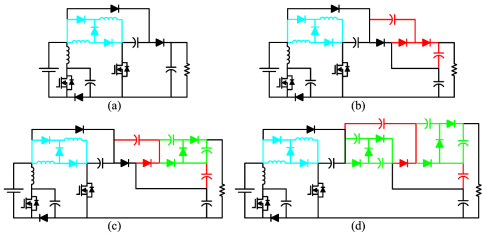

FIGURE 56. Sixth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

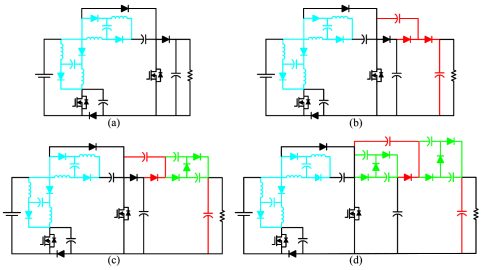

FIGURE 57. Seventh group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

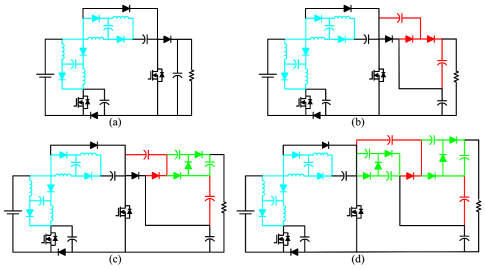

FIGURE 58. Eighth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

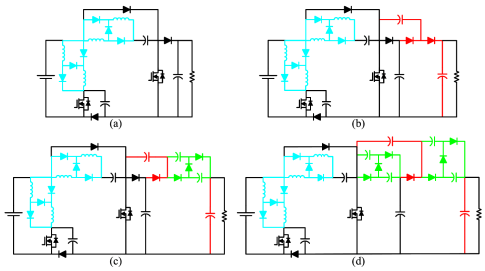

FIGURE 59. Ninth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

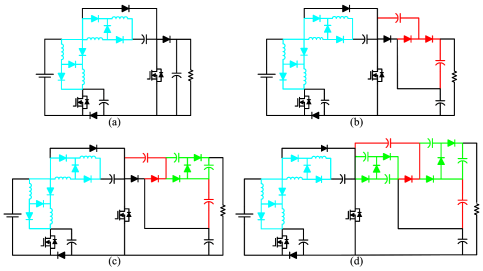

FIGURE 60. Tenth group of super lft Luo-based improved topologies: (a) first member, (b) second member, (c) third member, (d) fourth member.

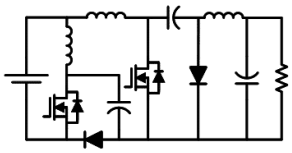

FIGURE 61. Cuk-based proposed topology.

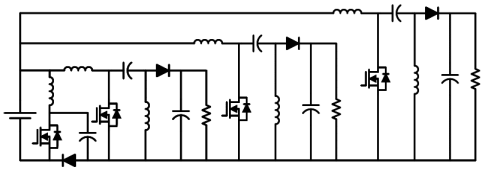

FIGURE 62. SEPIC-based multi output topology.

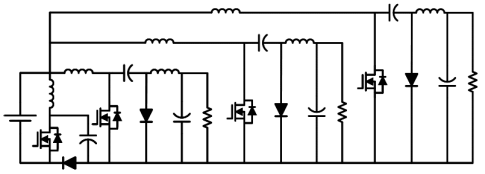

FIGURE 63. Cuk-based multi output topology.

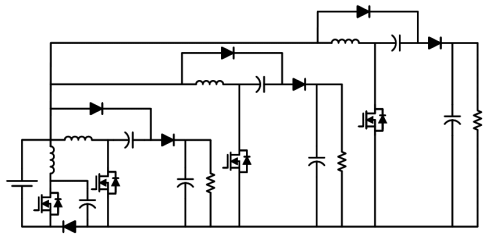

FIGURE 64. Super lift Luo-based multi output topology.

Table 2 presents the voltage gain, highest switch voltage stress, and highest diode voltage stress of the presented topologies in [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], and [41], besides the 52nd extension of this family. Notably, the 52nd extension has been selected as the best member of the proposed structures in this study. According to this table, the highest voltage stress of the switch and diodes are less than the output voltage in the corresponding converter in the 52nd extension, [24], [25], [26], [27], [28], [29], [30], [32], [33], [35], [36], [37], [38], [40], [41]. According to the expressed information in this table, in Fig. 38 the normalized voltage stress of the switch and diodes have been presented. Notably, these stresses have been normalized by the corresponding converter's output voltage. According to this figure, the provided normalized switch and diode voltage stress in the 52nd extension in this study are the least one, which shows

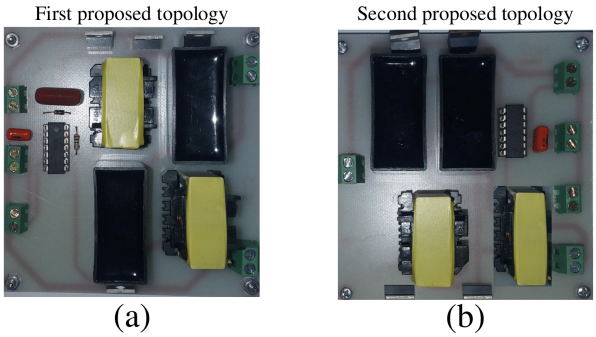

FIGURE 65. The prototypes: (a) the first proposed topology, (b) the second proposed topology.

TABLE 3. Design considerations.

V_{in}	f_s	I_o	Δi_L	ΔV_c	D
20 V	50kHz	1 A	30%	5%	50%

TABLE 4. Components current/voltage stresses of the first proposed topology according to the theoretical relations.

I_{L1}	I_{L2}	V_{C1}	V_o
$2A$	$2A$	$40V$	$80V$
I_{S1}	I_{S2}	I_{D1}	I_{D2}
$2A$	$1A$	$2A$	$1A$
V_{S1}	V_{S2}	V_{D1}	V_{D2}
$40V$	$80V$	$40V$	$80V$

that the highest voltage stresses are less than the output voltage with the highest difference.

In order to show the superiority of the 52nd extension in this family compared with [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] which are improved quadratic boost topologies, the voltage gain density of the converters according to the inductors, capacitors, switches, diodes, and all components' number have been presented in Fig.39. According to this figure, the voltage gain density of the 52nd extension is higher than [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41]. This achievement shows that the high voltage gain of the 52nd extension is not only due to its component number and it also has superiority in its design. It is good to note that the voltage gain comparison of the 52nd extensions and topologies of [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], and [41] has been presented in Fig.40. According to this figure, the provided voltage gain by the 52nd extension is higher than the rest with a far difference.

IX. EMPLOYING THE PRESENTED METHOD WITH OTHER CLASSIC CONVERTERS

In this section, the presented method in the previous sections is employed to provide other topologies. In Figs. 41 to 50 acombination of the boost topology at the first level with a SEPIC converter at the second level has been presented.

TABLE 5. Components current/voltage stresses of the first proposed topology according to the theoretical relations.

I_{L1}	I_{L2}	V_{C1}	V_o
$2A$	$2A$	$40V$	$80V$
I_{S1}	I_{S2}	I_{D1}	I_{D2}
$2A$	$1A$	$1A$	$1A$
V_{S1}	V_{S2}	V_{D1}	V_{D2}
$40V$	$80V$	$40V$	$120V$

TABLE 6. Components types.

Inductors	Capacitors	Switch	Diode
E-E core	MKT	IRF540 A	FES8GT

TABLE 7. Components value.

L_1	L_2	C_1	C_o
$334\mu H$	$500\mu H$	$10\mu F$	$2.5\mu F$

All these figures shows the presented method in section V with the boost and SEPIC topologies. It is good to note that the SEPIC topology is similar to the boost topology with a lower voltage gain. In bothe the SEPIC and boost converters, the input current is continuous and the output current is discontinuous. Additionally, the switch is low-sided with a simple drive circuit. These similarities in these topologies makes it possible to use the SEPIC topology at the second level as same as the boost topology. Notably, the super lift Luo converter has the mentioned common points with the boost topology. Consecuently, it can be used at the second level as same as the SEPIC topology. Figs. 51 to 60 show the employ of the super lift Lou converter in the presented procedure in section V. It is important to say that a converter like Cuk topology which its output terminal form is not the same as the boost topology can be used in this method. Fig. 61 presents the employ of the Cuk converter in the mentioned method. One of the extracted extensions of two boost topologies was the multi output structure. In Figs. 62 to 64 the multi output form of the SEPIC, Cuk, and super lift Luo-based converters have been presented. All these topologies proves this claim that the presented method in section V is not only fo two boost topologies and a other classic topologies can have a role in this method.

X. EXPERIMENTAL RESULTS

Table 3 provides the necessary details for obtaining experimental results, such as the types of semiconductors used, inductor and capacitor values, input voltage, switching frequency, output current, inductor current ripple, capacitor voltage ripple, and duty cycle percentage. Based on the values in Table 3, the average current of the inductors, average voltage of the capacitors, and voltage/current stresses of the semiconductors are determined and listed in Tables 4 and 5 for the first and second converters, respectively.

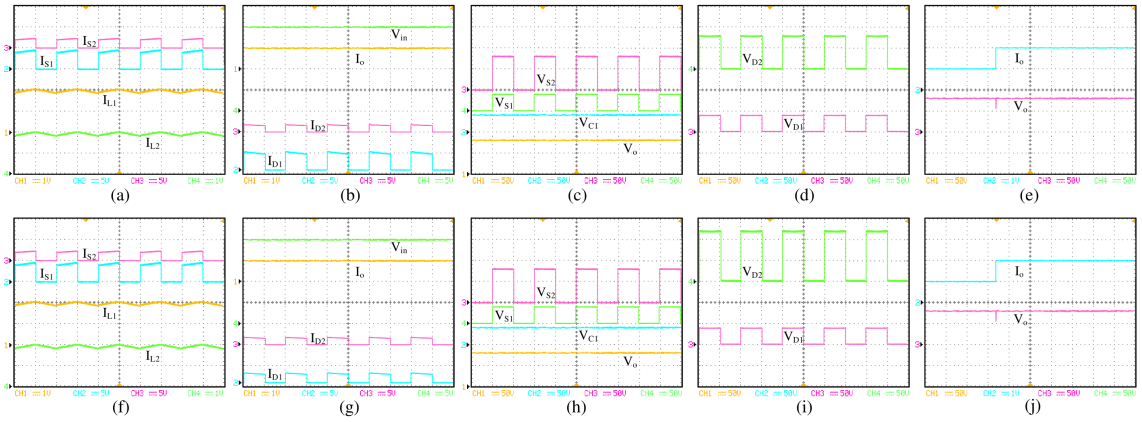

FIGURE 66. The experimental results and dynamic response: (a)-(e) for the first proposed topologies and (f)-(j) for the second proposed topologies.

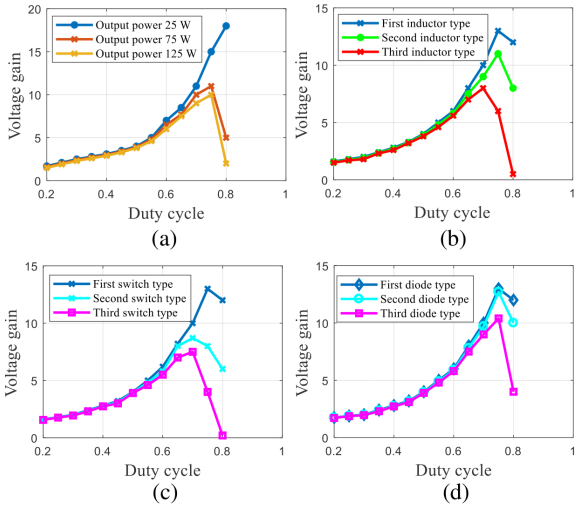

FIGURE 67. Voltage gain sensitivity analysis according to the experimental results for (a) output power changing, (b) inductors quality changing, (c) switches quality changing, (d) diodes quality changing.

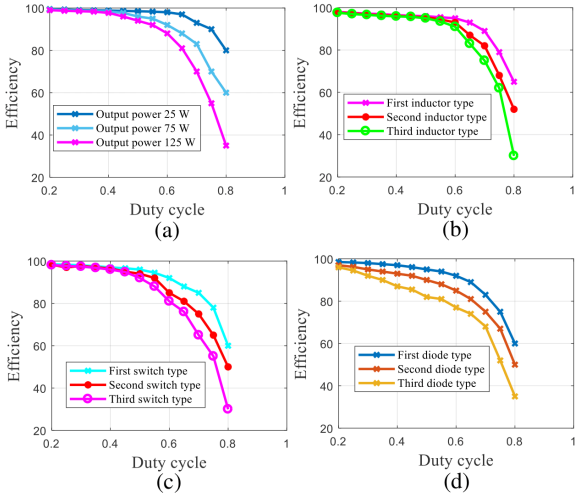

FIGURE 68. Efficiency sensitivity analysis according to the experimental results for (a) output power changing, (b) inductors quality changing, (c) switches quality changing, (d) diodes quality changing.

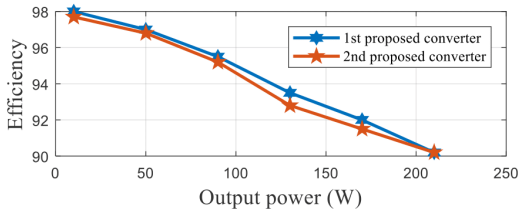

FIGURE 69. Efficiency of the first and second proposed topologies according to the output power changing, extracted from the experimental results.

The component types are shown in Table 6 based on the mentioned assumptions.

The figures in Fig. 65 show the prototypes of the first and second proposed topologies. In Fig. 66, the experimental results of the first and second proposed topologies, showing waveforms and values consistent with the assumptions and validating the relations in the second section. Table 7 contains the values of the inductors and capacitors. In the case of the control strategy, voltage mode control has been employed. In this case, the output voltage is compared to a reference voltage, and the error is processed by a compensator (PI/PID) to generate a control signal for the PWM modulator.

In addition, Figs. 67 and 68 show the sensitivity analysis results for the voltage gain and efficiency of the first proposed topology, which align with the plots in the third section. This confirms the accuracy of the reported relationships for the non-ideal mode. Fig. 69 illustrates the efficiency of the first and second proposed topologies as the output power changes at a fixed duty cycle and input voltage. This presentation shows that both converters can maintain an efficiency of over 90 % across a wide range of output power.

The presented voltage waveforms in Figs. 70 to 74 belongs to the voltage gain test of the expressed extensions. In all these plots, the input voltage is 10 V and the duty cycle is

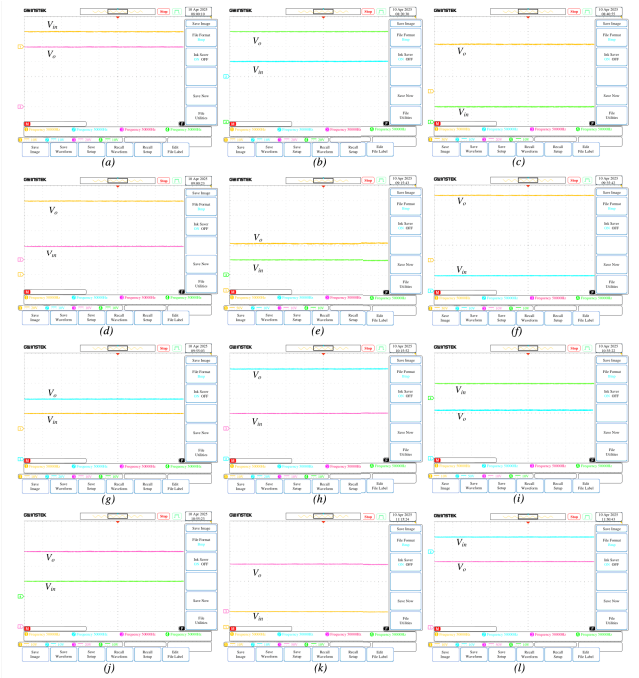

FIGURE 70. The voltage gain test of: (a) eighth, (b) ninth, (c) tenth, (d) fourth, (e) eleventh, (f) twelfth, (g) thirteenth, (h) fourteenth, (i) fifteenth, (j) sixteenth, (k) seventeenth, (l) eighteenth extensions.

FIGURE 71. The voltage gain test of: (a) fifth, (b) nineteenth, (c) twentieth, (d) twenty-first, (e) twenty-second, (f) twenty-third, (g) twenty-fourth, (h) twenty-fifth, (i) twenty-sixth, (j) twenty-seventh, (k) twenty-eighth, (l) twenty-ninth extensions.

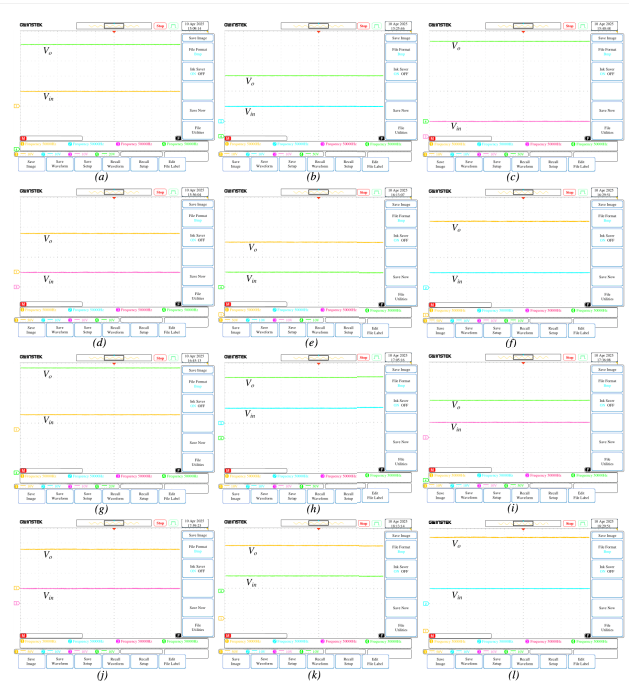

FIGURE 72. The voltage gain test of: (a) thirtieth, (b) thirty-first, (c) thirty-second, (d) thirty-third, (e) thirty-fourth, (f) thirty-fifth, (g) thirty-sixth, (h) thirty-seventh, (i) thirty-eighth, (j) thirty-ninth, (k) fortieth, (l) forty-first extensions.

FIGURE 73. The voltage gain test of: (a) forty-second, (b) forty-third, (c) forty-fourth, (d) seventh, (e) forty-fifth, (f) forty-sixth, (g) forty-seventh, (h) forty-eighth, (i) forty-ninth, (j) fiftieth, (k) fifty-first, (l) fifty-second extensions.

50 percent. The low value of the input voltage is due to the components and cost limitations. All these waveforms show that the expressed voltage gain tests are compatible with the theoretical values of the voltage gains in the fifth section.

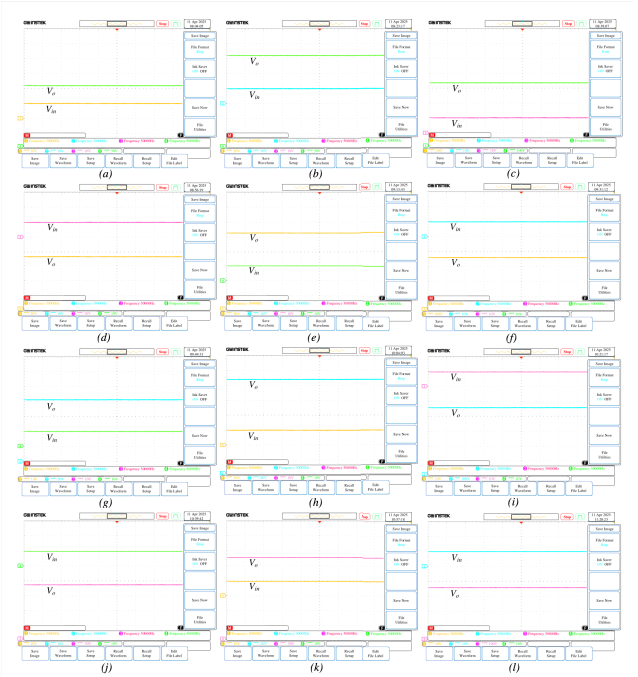

FIGURE 74. The voltage gain test of: (a) fifty-third, (b) fifty-fourth, (c) fifty-fifth, (d) fifty-sixth, (e) fifty-seventh, (f) fifty-eighth, (g) fifty-ninth, (h) sixtieth, (i) sixty-first, (j) sixty-second, (k) sixty-third, (l) sixty-fourth extensions.

XI. CONCLUSION

In this study, a family of quadratic DC-DC converters was proposed. The main advantages of the boost topology were present in the proposed topologies. Moreover, the voltage stress challenge of the semiconductors and output terminal capacitors was solved. Furthermore, the wide variety of converters in this family was capable of answering the various applications. Additionally, the highly improved family members of the proposed structures can be employed in water electrolyzing and hydrogen generation. The proposed topologies were compared with the recently suggested topologies, and their superiority was concluded. Finally, the experimental results were discussed their compatibility with the theoretical relations validated the expressed theoretical relations. Consequently, the proposed topologies can be used in various applications and solve their challenges. Notably, in this study only one form of the connection of two boost topologies was discussed and the presented family was introduced based on the mentioned main topology. However, dicussing about the family member of the other connections of two boost topologies was not discussed in this study and requires more researches and try, which is planed for the future study.

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