An Ultra-Linear LNA for Base stations

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An Ultra-Linear LNA for Base stations

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Abstract

In the commercial basestation market of today, LNAs are implemented using GaAs pHEMT technology. The popularity of GaAs pHEMT technology is based on its excellent low noise and high linearity properties. In this project, an LNA for basestation applications is designed using SiGe technology, which can provide low noise performance, but requires more work to achieve a competitive linearity when comparing with GaAs pHEMT technology. The main motivation of a LNA implementation in SiGe are the lower cost, higher integration possibilities than GaAs. As such, in this master project an ultra-linear LNA has been designed in QUBiC4Xi technology for base station applications in the 1710-1980 MHz band.

The requirement for a base station LNA are low noise, high gain, and high linearity. To achieve these goals simultaneously, a 2-stage topology is used where the first stage is optimized for low-noise and high-gain operation, whereas the second stage aims for high linearity and a high 1dB compression point using negative feedback. The first stage is using a cascode topology, which provides high gain and excellent reverse isolation. Its noise figure has been optimized by proper biasing and noise matching.

The output stage is implemented using a differential structure, to enhance linearity and output power handling. The techniques used to improve the linearity of the output stage include overall feedback, Implicit IM3 cancellation, 2^{nd} harmonic termination at the output, and out-of-band matching at its output. The out-of-band matching technique has been also evaluated separately for its linearity potential using a simplified Gummel Poon model to understand the impact of individual transistor parasitic (C_{je}, τ_f, C_{jc}) on linearity.

Since the targeted LNA input and output are single-ended, balun have been used in the interstage connection and at output convert from single-ended to differential. The 1 dB compression point of the output stage, which is typically limited by the maximum voltage swing of the transistor technology is in its configuration enhanced by applying impedance transformation in the output balun.

All of the yielded the conclusion that a transformer coupled 2 stage LNA one of the most promising circuit options, fulfilling (at least in simulation) all project specifications. These targeted specification are, low-noise figure (F<0.65dB), high gain (>30dB) high compression (P1dB>24 dBm) and high linearity (OIP3 > 40 dBm) up to the 1dB compression point.

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Chapter 1

Introduction

In wireless communication industry, cellular communication is a fast growing segment [1]. The cellular systems are one of the most successful application of the wireless communication. Two main building blocks of a cellular system are the cellular phone and the base station. Both these blocks use a same receiver architecture, but differ in their required performance in terms of sensitivity, linearity and power consumption. The base station should provide large area of coverage while sharing the same site with many transmitters.

One of the most important functional blocks of a base station receiver is the low noise amplifier. An LNA senses the weak input signal from the antenna and amplifies it. The surrounding filters reject out-of-band signals, since in practical situations many service providers are accommodated on the same base station to reduce cost [2]. The basic requirements of an LNA are low noise, high gain, low return loss(IRL), high linearity and output return loss(ORL). Multiple technologies are available for implementation of an LNA, such as GaAs, SiGe, and etc. An integrated solution using one single technology is desired to lower system and test costs. The main focus of this project is to implement an ultra-linear LNA for base station using SiGe technology.

1-1 Receiver architecture

Figure 1-1 shows the full receiver architecture of a typical base station [3]. In this figure the cavity filter is the first component, which filters out-of-band interference generated by the base station transmitters. The losses of the filter should be low, since it directly impacts the noise performance. The LNA is the first active block of the receiver chain, which determines the coverage and tolerance of the base station receiver. The RF signal received from the filter is low in intensity, which is amplified by an LNA and fed to the mixer or RF filter. Designing a tower top LNA for macro cells base station is the goal of this project.

A co-axial cable is used for connecting to the top of the base station to the receiver at the bottom(see Figure 1-2). The typical length of this co-axial cable is around 20 m, which results approximately 10 dB losses. To compensate the losses in the coaxial cable an additional ground level amplifier is used. The ground level amplifier provides high linearity at moderate noise level. The image rejection filter, filters out the noise in the image band before it reaches the down converting mixer stage in base station receiver. The intermediate filter removes any frequency component other than the desired intermediate frequency IF component. The filter may have low pass or band pass response depending on the IF frequency.

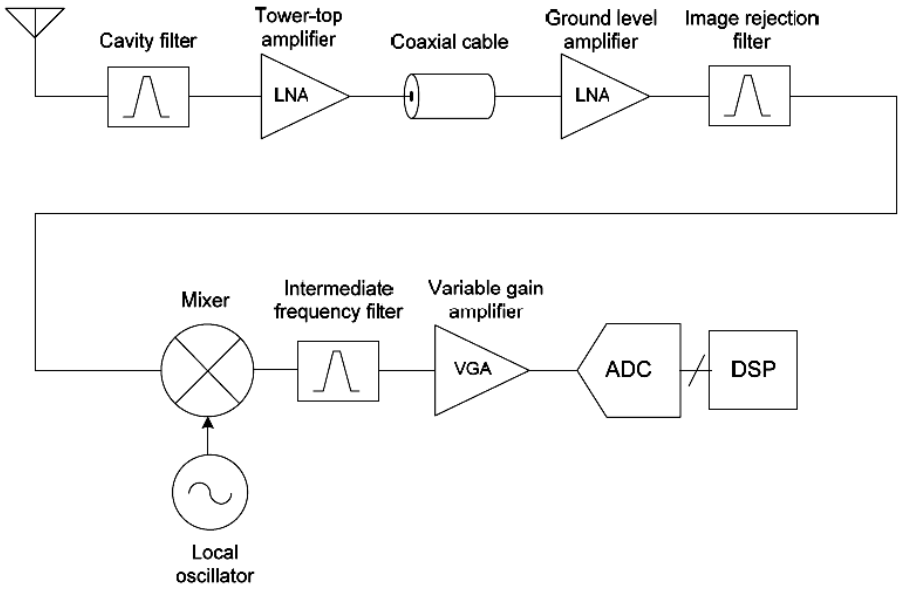

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Figure 1-1: Receiver Architecture

1-2 Requirements for base station LNA

The main requirement of a macro cell base station are low noise, high gain, high linearity and high compression point. The physical placement of the LNA and other components of the receiver are shown in Figure 1-2.

1) Since the coverage area of the base station needs to be as high as possible, the receiver must be able to detect and resolve weak signals coming over a large distance. Consequently, the receiver needs to have good sensitivity. The sensitivity performance of a receiver is specified using noise figure. The noise figure (NF) of the first block dominates the NF of the entire receiver. Hence, typically noise figure requirement for base station receiver is sub-1dB [4].

2) As shown in Figure 1-2, usually the LNA is kept very close to the antenna for conditioning the signal before transferring it to a ground unit over a cable [5]. The signal transfer over the long cable, results in a few dB attenuation. Due to this attenuation in the cable, the gain requirement of the base station LNA is high.

3) The multiple transceiver present in a typical base station interfere with each other. Consequently, the LNA in these receivers should have high linearity to reduce the effect of out-of-band and in-band interference.

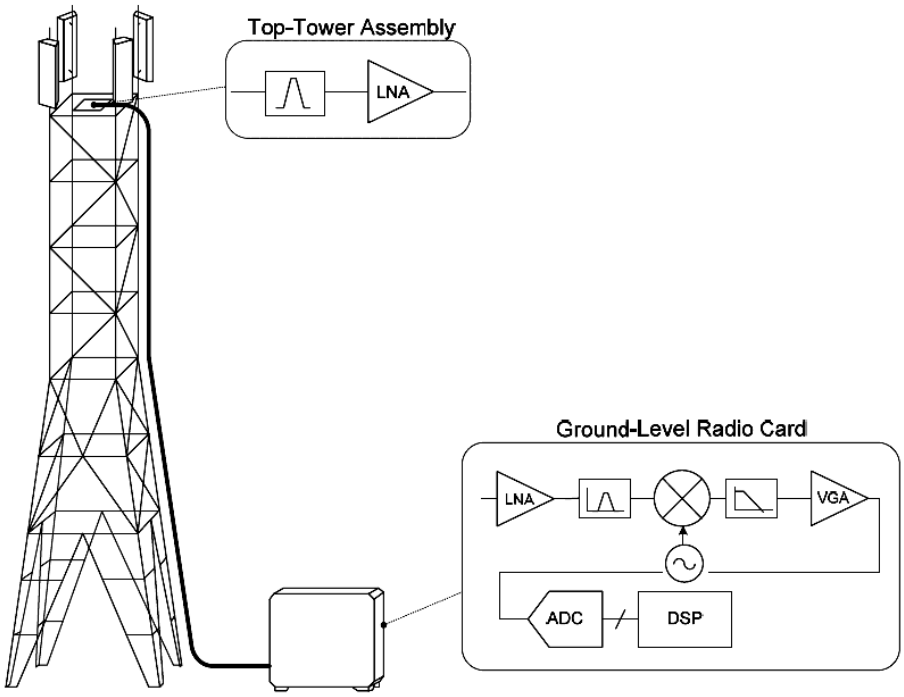

Figure 1-2: Base Station

1-3 Technologies for LNA

To achieve all the LNA requirements, different technologies are used. The present generation wireless systems are implemented based on considerations such as low cost, high performance, high integration and short time to market [6]. For high performance application, III-V process technologies such as InP and GaAs are available. III-V semiconductor technologies provide HEMT and HBT devices, that use a heterojunction mode of operation [7]. The heterojunction is formed by using different bandgap materials e.g GaAs, InP, SiGe. The device fabrication and properties are altered to get good performance at high frequency.

Table 1-1 compares the performance of HBT and HEMT [7]. HEMT devices provide superior electron mobility and velocity compared to HBT. For high-frequency application technologies such as GaAs HEMT, GaAs MESFET and SiGe HBT are often used. Table 1-2 compares different technologies with respect to noise figure and cost [2]. From both tables it can seen that by using GaAs pHEMT the lowest noise figure can be achieved, but the process technology is about 200 more times costlier than Silicon.

Table 1-1: Comparison table of different fabrication technique [7]

Merit Parameter	HEMT	HBT	conclusion
f_t	M	H	HBT has highest speed
f_{max}	H	L	HEMT is highest frequency
Noise figure	L	H	HEMT is best for LNA
$IP3/P_{dc}$	M	H	HBT is best at low frequency

Table 1-2: Comparison table of different technology w.r.t noise and cost [2]

Technology	Noise rating	Epitaxy cost/mm^2
InP pHEMT	Very good	$10
GaAs pHEMT	Very good	$2
GaAs HBT	Good	$2
Si CMOS	Fair	$0.01

1-4 Motivation and objectives

A low noise figure can be achieved by using optimum design technology and cooling arrangements. However, some of these techniques are not feasible for a base station receiver. For instance, by using helium cooling a low noise figure can be achieved but its maintenance is too expensive to be practically feasible [2]. The other way to achieve low noise is to use more exotic fabrication process and material.

To achieve high linearity the device needs to operate at higher f_t. In GaAs pHEMT, the noise is low for a wide range of bias, which helps to achieve low noise and high linearity simultaneously. In SiGe, the noise figure is strongly dependent on the base and collector shot noise. Thus, the minimum noise figure after its sweet spot will increase with current. Hence, this limits a good trade-off between the minimum noise figure and linearity. Table 1-3 shows the performance comparison of different, commercially available LNAs for base station applications.

Table 1-3: Commercially available highly linear LNA for base station

Product	**MGA-13316** [8]	**MMl20242H** [9]	**SKY65040-360LF** [10]	**BGU7063** [11]
Technology	GaAs pHEMT	GaAs pHEMT	GaAs pHEMT	SiGe
frf [GHz]	2.5	1.95	1.95	1.98
NF [dB]	0.76	0.59	0.65	0.9
S_{21} [dB]	34.3	34	17.5	35
OIP3 [dBm]	41.8	39.5	34.5	36
OP1 [dBm]	23.5	24	16	22.5
mA@V	160@5	160@5	150@5.5	230@5

* It can be seen that most of the LNA use GaAs pHEMT technology. LNAs designed using GaAs technology provide low noise and high linearity which is in accordance with point discussed in earlier. GaAs is a costly technology, since the material used are expensive. Also the unit cost is higher due to smaller size of wafer and low production speed.

* The SiGe technology provides reasonable performance for linearity and noise figure but it has advantages such as low cost, high yield and higher integrity than GaAs.

* The BGU7063 uses SiGe technology for base station LNA. The disadvantage of this product is the use of separate technologies to achieve low noise (QUBiC4Xi) and high linearity, 1dB compression point (QUBiC4X).

* This project aims to use only one technology namely 0.25μm SiGe BiCMOS QUBiC4Xi. This technology can provide low noise and high speed. However due to the Johnson power limit, as the f_t increases BV_{CEO} of the device decreases [12]. This can also be seen from the Table 1-4 [5]. The QUBiC4Xi technology has higher f_t so, the BV_{CEO} is reduced compared to QUBiC4X. This reduction in BV_{CEO} becomes a challenge in achieving higher 1-dB compression point.

Table 1-4: Comparison of two different 0.25 μm SiGe BICMOS processes

	QUBiC4X		**QUBiC4Xi**		**Unit**
	LVNPN	HVNPN	LVNPN	HVNPN	
β	400	320	2000	7000	
f_t	130	60	216	80	GHz
f_{max}	180	120	177	162	GHz
NF_{min}	0.60	-	0.35	-	dB
BV_{CEO}	1.8	3.3	1.4	2.5	V
BV_{cbo}	6	13	5.2	12	V

It will be investigated if this higher speed can be utilized to enhance the loop gain and as such improve the achievable linearity. However, with the restriction of using a single technology it

becomes more challenging to achieve low noise, high linearity, and high compression point simultaneously. In summary the main objectives of this project are:
* Investigate the linearity of QUBiC4Xi technology.
* To propose an architecture which would enhance linearity.
* To present a systematic design approach to achieve high linearity, low noise, high gain and high compression point.

1-5 Specifications

The noise figure requirement of the receiver, can be derived from its sensitivity equation represented as [13],

$$S_{in}dBm = NF(dB) + kTB_{RF}(dBm) + E_b/N_0 - PG(dB) \tag{1-1}$$

where kTB_{RF} is the thermal noise power at room temperature, E_b/N_0 is 7 dB [14] and PG is the processing gain, which is equal to 24 dB [14] for a BER= 0.001. For a basestation application, a sensitivity level of -121 dBm, a data rate of 12.2 kbps and a bandwidth of 3.84 MHz are typical numbers [15]. The thermal noise power over the bandwidth of 3.84 MHz is -108.13 dBm. By substituting these values in Eq. (1-1), it can be concluded that the NF requirement for the full receiver is around 4 dB. However, if the losses of the duplexer, and the total receiver are considered then the noise figure of LNA should be below sub-1 dB [4].

In an FDD system, there is simultaneous transmission and reception of signals. A duplexer is used to isolate the transmitting and receiving signals. As the base station shares the same site with other transmitter and receivers operating on different standards, e.g. GSM800 and DCS1900, the interference due to these transmitter is +16 dBm and isolation provided by the duplexer is around +30 dB. The leakage of transmitting signal is still around -14 dBm. The thermal noise power at 27 $\circ C$ is around -109 dBm, which is 6 dB higher than the sensitivity level. So the IIP3 requirement for a complete receiver is -6 dBm [4]. The IIP3 requirement for LNA is around +10 dBm for all the gains level. The gain specified for this project is 30 dB. Therefore, the OIP3 requirement is +40 dBm [4].

The input compression point required for a wide range base station receiver is -13 dBm. To meet the receiver requirement of compression point, the LNA needs to have higher compression point. The typical output compression point required for LNA is greater than 20 dBm for a gain of 20 dB [4].

Table 1-5 provides the specification that need to be achieved for this project.

Table 1-5: Specification for ultra linear LNA

Parameter	Value
Technology	$0.25\mu m^2$ BiCMOS QUBiC4Xi
Frequency Band [GHz]	1.710-1.980
Noise figure [dB]	0.6
OIP3 [dBm]	>40
OP1 [dBm]	24

1-6 Thesis organization

In chapter 2, a two stage approach is introduced to achieve all the requirements of base station LNA simultaneously. The specification required for individual stage are derived using Friis noise figure and cascade linearity system equation. To achieve the requirements of this project, negative feedback is proposed. Two different types of feedback are discussed, the overall feedback and local feedback. The use of negative feedback may cause instability problems, so frequency compensation technique such as phantom zero are also presented. Finally, the overall architecture used for implementation of the 2 stage LNA is explained.

In chapter 3, the device characteristics of the technology to be used in this project are discussed. Before applying any linearity improvement technique, the dominant non-linearities in a transistor are identified. After the dominant non-linearities are known, linearity improvement techniques such as implicit IM3 cancellation, out-of-band cancellation, and the use of 2^{nd}-harmonic termination are elaborated to reduce the non-linearities. At last the out-of-band cancellation technique is used on an ideal Gummel Poon model, to demonstrate the potential linearity improvement. The design considerations required to achieve high output compression are given.

In chapter 4, the input stage is designed to achieve high gain, low noise and low return loss. The technique used to achieve low noise and impedance match simultaneously is explained. To complete the 2 stage LNA, two differential output stages are discussed namely CE and cascode stage based. All the linearity techniques discussed in chapter 3 are applied to achieve high linearity and high compression point in the output stage. The input stage and the two differential output stages are combined to form the complete 2 stage LNA design. The performance of the complete 2 stage LNA is demonstrated.

In chapter 5, the physical layout of the schematic finalized in the chapter 4 is presented. The extraction of the layout is done using Assura and Momentum to include all parasitic. The post layout simulation results are shown. A comparison of this work with state-of-the-art is provided.

Chapter 2

Low noise amplifier

2-1 Introduction

Basic requirements for wide range base station LNA are low noise, low return loss, high gain, high linearity, and high compression point. The LNA is noise and impedance matched to achieve low noise and low return losses. In order to achieve high gain at high frequency an amplifier choice needs to be made. The high linearity requirements are satisfied by operating the device at higher f_t and using special linearity improvement techniques. In this chapter, the approach used to achieve linearity and noise simultaneously in SiGe technology is discussed. The related specification required for design approach is derived using Friis and linearity of cascade system equation. To achieve these requirements the negative feedback is used. The frequency compensation technique is discussed to improve the stability of the 2 stage system. Finally the implementation of the two stage system along with differential amplifier and transformer are discussed.

In Section 2-2, two stage approach used to to meet the LNA requirement is discussed, followed by in this section the equation and specification related to each stage is explained. In next Section 2-3, distortion reduction due to negative feedback and stability analysis is discussed. In last Section 2-4, the two stage design used for implementation is shown.

2-2 Two stage approach

To achieve simultaneously low noise, high gain, high output power and, high linearity using a single stage is very difficult, due to the conflicting operating conditions of the active device . One solution to achieve these requirements is to choose a two stage approach [5]. In the two stage approach first stage targets low noise and high gain, second stage aims for high linearity and

high output power. The biasing of both stages can be optimized independently for lower noise, linearity and output power.

The block diagram of the two stage approach is as shown in Figure 2-1. The input stage provides high gain to suppress the noise of the second stage. The high gain of the input stage also makes the linearity requirement of the output stage high. In order to improve the linearity and operational bandwidth of the output stage overall feedback can be considered. However, this may lead to stability concerns which will be discussed later. First we focus on the requirements of the individual circuit blocks in such a configuration.

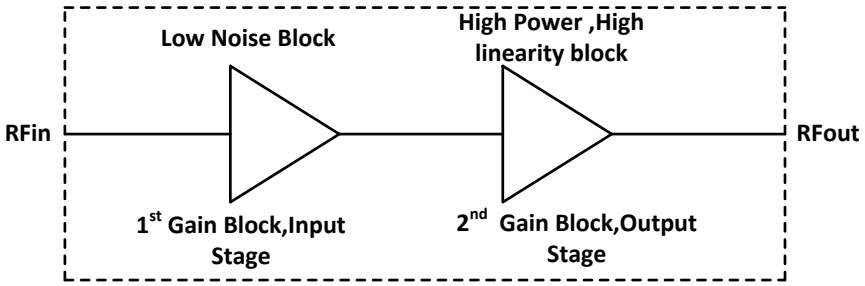

Figure 2-1: Two stage approach

Noise in cascade system

In order to calculate the noise figure of two-stage LNA, let us consider an example as shown in Figure 2-2, where G_{a1}, G_{a2} and F_1, F_2 are gain, noise figure of stage A and B, respectively. The overall noise figure of the system can be represented as [16],

$$F = F_1 + \frac{F_2 - 1}{G_{a1}} \tag{2-1}$$

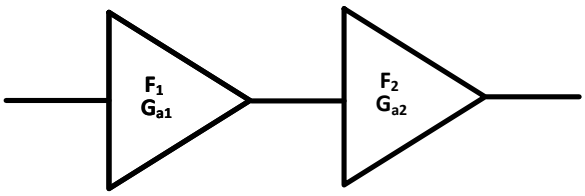

Figure 2-2: Noise figure of cascade system

From Eq. (2-1), it can be concluded that with a high-gain at first stage, noise of the subsequent stages can be suppressed, but the noise figure of the first stage dominate that of the LNA.

Cascaded non linear system

In order to calculate the linearity of the 2-stage LNA, all the non-linearity need to be referred back to the input or the output. Let us consider a two non-linear cascade amplifier, where the non-linear output of stage A and B are given by,

$$\begin{aligned} y(t) &= a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \\ z(t) &= a_1 y(t) + a_2 y^2(t) + a_3 y^3(t) \end{aligned} \tag{2-2}$$

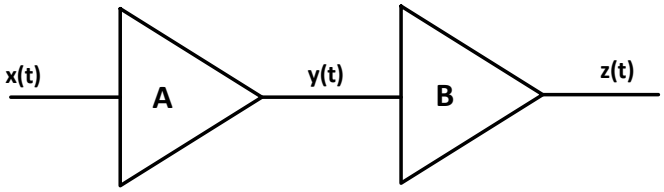

Figure 2-3: Cascaded blocks

By rearranging the third order non linearity and fundamental responses, the linearity of cascaded system $IIP3_{cas}$ is written as in Eq. (2-3) [17]. The equation is approximated to Eq. (2-4), where $IIP3_A$ and $IIP3_B$ represent the input third order intercept point of stages A and B, respectively. From Eq. (2-4), it can be concluded that if the gain of the first stage (a_1) is high, the linearity of the stage B becomes important and tends to limit the linearity of the system.

$$IIP3_{cas} = \sqrt{\frac{3}{4}\left[\frac{a_1 b_1}{a_1^3 b_3 + 2a_1 a_2 b_2 + a_3 b_1}\right]} \tag{2-3}$$

$$IIP3_{cas}^2 = \left[\frac{1}{IIP3_a^2 + \frac{a_1^2}{IIP3_B^2} + \frac{3a_2 b_2}{2b_1}}\right]^{-1} \tag{2-4}$$

Specification of two stages

A two stage approach is used in this project. Design parameters such as gain, noise figure and linearity are derived for individual stages. The noise figure of the full system is dependent on the first stage. The minimum possible noise from the transistor is 0.35 dB [5], so the noise figure of the first stage is assumed to be around 0.5 dB. The additional 0.1 dB is assumed to include the noise added by the interconnect and other passive elements used for simultaneous input and noise match. A gain of 20 dB is considered for the first stage to suppress the noise of second stage. Now the bottle neck for high linearity is the output stage due to the high gain of first stage. The linearity of about 42 dBm is assumed for second stage. The noise figure can be calculated using Friis formula given by Eq. (2-1) and linearity by using Eq. (2-4) .

Table 2-1: Specification for two stage

Parameter	Input stage	Output stage	Overall LNA
Gain [dB]	20	10	30
Noise figure [dB]	0.5	5.6	0.6
IIP3 [dBm]	12	32	>10
OIP3 [dBm]	32	42	>40

2-3 Negative feedback

Negative feedback is the most commonly used method for distortion reduction. The negative feedback improves the transfer function characteristics and also provides the optimum impedance matching condition. Along with these advantages feedback also makes circuit less sensitive to process and temperature variations and makes the transfer function more linear [17].

Overall feedback

The commonly used negative feedback is overall feedback. Applying overall feedback is challenging at high frequencies, the reasons are firstly at high frequencies the achievable gain is less and using feedback reduces the gain even further. In order to achieve high gain multiple cascade stages are to be used, which may lead to an unstable design. Secondly, circuits for high frequency applications operate close to f_t, leading to large phase shifts, which may also lead to unstable design. Thirdly, in high frequency design, gain has a band pass characteristics in order to reduce interference from baseband and second harmonic. To apply feedback for these characteristics is difficult.

With advancements in process technology the device f_t has increased which makes the use of feedback feasible. High f_t also helps to achieve high loop gain at high frequency.

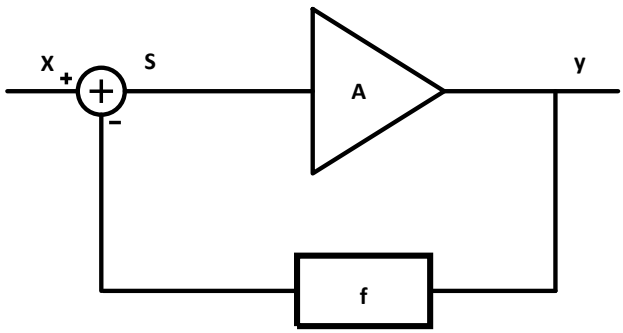

Figure 2-4: Overall negative feedback

The feedback implementation is as shown in Figure 2-4, where A is the basic amplifier and f is the feedback element, where f is usually a passive element. Both the amplifier and the feedback element are considered to be nonlinear. The non-linear transfer function of the amplifier can be written as,

$$y(t) = a_1 s(t) + a_2 s^2(t) + a_3 s^3(t) \tag{2-5}$$

The output of a feedback system as shown in figure can be written as,

$$s(t) = x(t) - fy(t) \tag{2-6}$$

By substituting Eq. (2-6) in Eq. (2-5), we get

$$y(t) = a_1[x(t) - fy(t)] + a_2[x(t) - fy(t)]^2 + a_3[x(t) - fy(t)]^3 \tag{2-7}$$

By solving above equation,

$$y(t) = n_1 x(t) + n_2 x^2(t) + n_3 x^3(t) \tag{2-8}$$

where n_1=$\frac{a_1}{(1+a_1 f)}$; n_2=$\frac{a_2}{(1+a_1 f^3)}$; n_3=$\frac{a_3(1+a_1 f)-2a_2^2 f}{(1+a_1 f^3)}$. For the feedback amplifier IMD2 and IMD3, can be represented as,

$$IM2_{FB} = \frac{n_2}{n_1}A = \frac{a_2}{a_1(1+a_1 f_2)^2}A = \frac{IM2_{AMP}}{(1+a_1 f)^2} \tag{2-9}$$

$$IM3_{FB} = \frac{3}{4}\frac{n_3}{n_1}A^2 = \frac{3}{4}\frac{a_3}{a_1(1+a_1 f_2)^3}A^2 = \frac{IM3_{AMP}}{(1+a_1 f)^3} \tag{2-10}$$

From the Eq. (2-9) and Eq. (2-10) , 2^{nd} order intermodulation are reduced by factor square of the loop gain $(1+af)^2$ and third order is reduced by cube of loop gain $(1+af)^3$. So larger the loop gain, lower will be the distortion. The larger loop gain can be achieved by using multiple active stage in cascade. But this is limited by stability considerations [17]. While cascading, the least linear block needs to be placed at the start of the receiver chain and most linear block are placed at end of the receiver. Another way to improve the distortion performance is to include the loop gain by using large transconductance which, however incur a lot of power. The linearity not only depends on the loop gain $(a_1.f)$ but also on the magnitude of non-linearity (a_2, a_3). These non-linearities must be reduced, which can be accomplished by employing current mode of coupling between the stages. The limitation of overall feedback is, that the feedback elements also introduce non-linearities. The large loop gain can linearize the amplifier, but cannot reduce the non-linearities caused due to feedback element.

2-3-1 Local feedback

The local feedback is another form of negative feedback which is shown in Figure 2-5. The impedance Z_1 provides series feedback. By using local feedback, transconductance reduces, output and input impedances increase. The increase in input and output impedance helps in matching. In local feedback when input voltage V_i increases, the current increases and voltage drop

across the local feedback resistor increases, in-turn reducing the input voltage, thus achieving negative feedback. Local feedback helps in reduction of the distortion, as the transfer function becomes more linear.

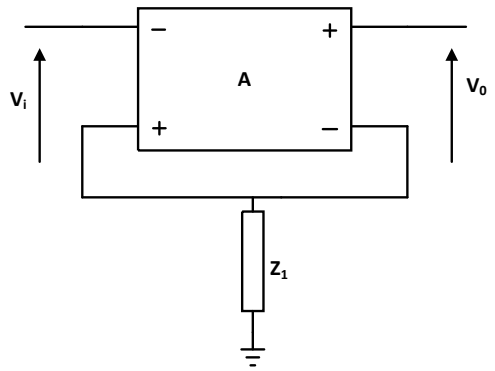

Figure 2-5: Local feedback

Assume if the gain of the amplifier is A, and g_m its transconductance, then the second and third harmonic distortion with local feedback are given by [18],

$$HD_2 = \frac{A}{4V_t(g_m Z_1)^2} \tag{2-11}$$

$$HD_3 = \frac{A^2}{12V_t^2(g_m Z_1)^3} \tag{2-12}$$

where $V_t = \frac{kT}{q}$. The harmonic distortion can be reduced by increasing the g_m or Z_1 .

2-3-2 Stability

The stability is an important consideration for an amplifier. It can be determined using the S-parameters, the matching network and termination [19]. This system will become unstable if either input or output sees a negative impedance i.e $|\gamma_{in}|$>1 or $|\gamma_{out}|$>1 for unilateral device. The stability of a system can be determined by stern stability factor,

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} \tag{2-13}$$

where $\Delta = s_{11}s_{22} - s_{12}s_{21}$. For a system to be unconditionally stable the necessary condition is $K > 1$ and $\Delta < 1$ for a particular combination for source and load impedance. In a feedback

system, for a certain combination of feedback network, source and load impedance, system might become unstable.

Another way of analyzing stability is by pole-zero analysis. An amplifier with a low-pass response (one dominant pole) will never show instability behavior. If an amplifier has two dominant poles, where each pole provides a phase shift of -90^0, the phase shift will exceed -180^0 at high frequencies. And if the loop gain is larger than unity, then the system will oscillate. In high frequency circuit design, frequency response is usually bandpass. If the system is unstable, frequency compensation needs to be applied to make it stable.

Frequency compensation

One of the most important considerations for designing a feedback system is to how to apply frequency compensation technique to improve stability. Frequency compensation essential modifies the system polynomial by moving poles in the s-plane. It can be done either changing the starting point of the loop poles or changing the shape of the root locus [20]. The compensation techniques used for changing the loop poles are pole splitting, pole zero cancellation, resistive broad-banding. The process of changing the root locus is done by using phantom zero technique.

The most attractive technique to improve stability at high frequencies is phantom zero. Phantom zero is visible in loop but not in the systems transfer function [20]. The shape of the root locus is altered by the phantom zero, which is shown in Figure 2-6. The phantom zero is usually added at the band edge, the element used to introduce phantom zero is apparent at high frequency. The noise and distortion performance are only effected at the band edge, where it is introduced. The phantom zero can be provided at three places in circuit: input, output, feedback network.

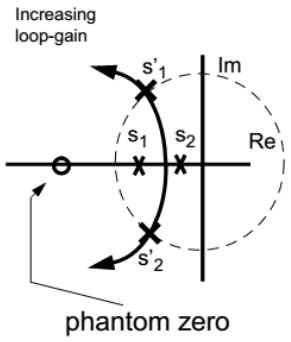

Figure 2-6: Root locus after applying phantom zero

For example, let us consider a dual feedback configuration shown in Figure 2-7. First feedback is overall feedback which provided by the impedance Z_1 and second feedback is local feedback through impedance Z_2. This configuration has both voltage and current feedback. This dual

feedback helps in improvement of linearity. If the impedance Z_1 is resistive, then in order to realize a phantom zero, a capacitor is usually placed in parallel with Z_1.

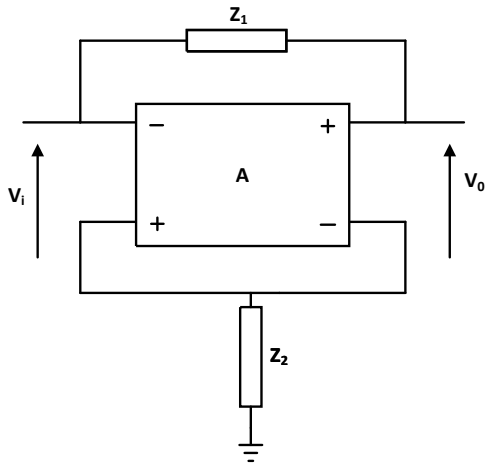

Figure 2-7: Dual loop feedback amplifier

2-4 Two stage design

The block diagram of the choice of architecture is shown in Figure 2-8. From the earlier discussion, first stage needs to be designed for low noise and high gain. The low noise figure is achieved by using a technology device, which inherently has low noise and additionally by providing a noise match. The gain requirement of the first stage is very high. The most common gain stage used is CE stage, but at high frequencies, its gain is limited by base to collector capacitance. This problem is solved by using a cascade of CE-CB stage. The amplifier used in combination of common emitter and common base is referred to as cascode amplifier. A negative local feedback is used for first stage to improve linearity and input impedance of the device, which helps it to match it to 50 Ω. A capacitive shunt negative feedback is used for input and noise match.

The main objective of the second stage is to improve linearity and compression point. The differential structure is used for output stage, which helps to control the odd and even harmonic orthogonal. This helps to control the impedance at the baseband, second harmonic and fundamental to improve linearity. The linearity is improved by using techniques such as implicit IM3 cancellation, overall feedback, out-of-band cancellation, 2^{nd} harmonic terminations. As the second stage is differential and first stage is single-ended a balun is used for conversion from single-ended to differential. At the output another balun is used for conversion from differential to single-ended. The balun used at output helps output matching and impedance transformation. The use of differential structure provides double the power compared to single-stage. Along with differential structure and impedance transformation high output compression point is attained.

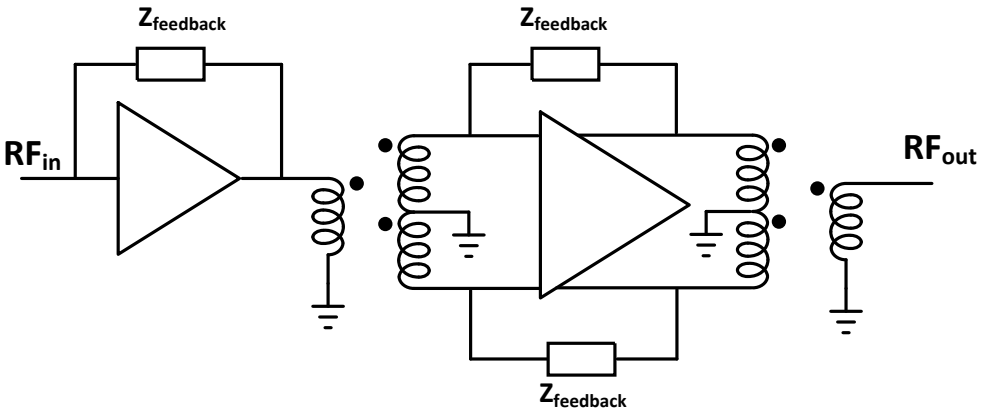

Figure 2-8: Two stage design

We tried to explore the effect of negative feedback in this project. An attempt has been made during the project to apply overall feedback on the complete LNA, although at the end has not been applied for stability reasons. As discussed, feedback was applied for individual stages. The overall noise performance degrades, due to the losses in the feedback elements.

The important blocks of the output stage are the differential amplifier and the balun. A basic understanding of differential structure for improvement in linearity is discussed. The balun at the output limits the performance of the LNA, the losses in this balun should be reduced. The parameters affecting, and the techniques need to be used to optimize for low losses, is discussed.

2-4-1 Differential output stage

Differential amplifiers are one among the high performing circuits. The antenna is single ended and the output from the LNA can either be differential or single-ended. In this project both the input and output are single-ended. To use a differential amplifier, a balun/transformer needs to be used for conversion from single ended input to differential or vice versa. The basic bipolar differential circuit is as shown in Figure 2-9. The V_{out} is the differential collector of the collector voltage, which can be represented as [18],

$$V_{out} = I_{EE} R_L \frac{\beta}{1+\beta} tanh(\frac{V_i}{V_t}) \tag{2-14}$$

where I_{EE} is bias current, β is current gain of BJT, V_i is the input to differential pair, R_L is the load impedance. From the equation, it can be found that the voltage is an odd function of input voltage V_i, no even harmonics are present at the output. The voltage at the common emitter node of differential stage can be represented as [18],

$$V_E = \frac{V_i}{2} - V_t ln \frac{\beta}{1+\beta} \frac{I_{EE}}{I_s} + V_t ln(1 + exp(\frac{V_i}{V_t})) \tag{2-15}$$

The voltage V_E is an even function of input voltage. If both the $\frac{V_i}{2}$ and $\frac{-V_i}{2}$ are interchanged, then also V_E voltage changes exactly in identical manner. Thus, it can be said that there are no odd harmonics present at this node. The tail node is AC ground, when the circuit is linearized. This helps to reduce the non-linearities caused by even harmonics. The overall distortion performance of system can be improved.

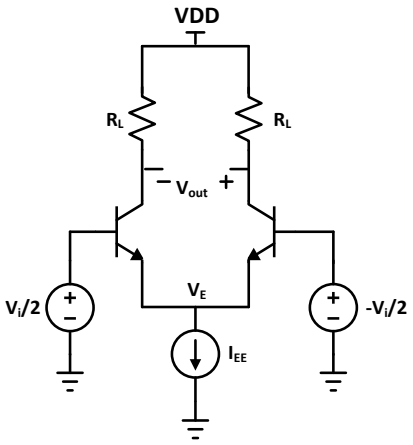

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Figure 2-9: Basic Common emitter Differential pair

In a differential pair, equal and opposite AC voltage and currents flows in two differential branches. If the layout is symmetrical then the two branches have equal coupling with the reference system. The introduced AC current in the reference system from one branch is counteracted by the equal and opposite from the other branch.

In layout, at high frequency metal interconnect connecting to ground plane has a finite impedance. The noise generated by the signal returning from ground, across the finite impedance to ground is referred to as ground bounce. Due to ground bounce both the differential branch will be effected equally. But due to the counteract nature of the differential branches, the common mode signal will get canceled.

2-4-2 Transformer

A transformer transfers power from the primary to the secondary coil using mutual coupling. The power transfer should happen with low loss. The impedance is transformed between the coils depending on the turns ratio. If an alternating current i_p flows in primary it induces a current in secondary i_s. In the ideal transformer the current and voltage transformation between the winding is expressed in terms of turns ratio n as [21],

$$n = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_P}{L_S}} \tag{2-16}$$

where (v_p, v_s), (i_p, i_s) are voltages and currents in primary and secondary coils respectively. L_p, L_s are the self inductance of primary and secondary coils, respectively. The energy with which power is transferred between the coils depends on magnetic coupling which is given by Eq. (2-17), where M is mutual inductance.

$$k_m = \frac{M}{\sqrt{L_P L_S}} \tag{2-17}$$

The quality of the transformer is evaluated by the maximum available gain. It can be expressed in terms of quality factor and mutual coupling of the primary and secondary coils. The maximum gain is limited by mutual resistive coupling with silicon substrate and also quality factor of the primary and secondary coils [22]. For maximum power transfer the efficiency should be high. The efficiency can be defined as the ratio of power delivered to load to input power. The maximum gain is expressed in terms of S-parameters as [22],

$$G_{max} = |\frac{s_{21}}{s_{12}}|(k - \sqrt{k^2 - 1}) \tag{2-18}$$

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|} \tag{2-19}$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21} \tag{2-20}$$

The alternative expression for max gain is,

$$G_{max} = 1 + 2(x - \sqrt{x^2 + x}) \tag{2-21}$$

$$x = \frac{Re(z_{11})Re(z_{22}) - [Re(z_{12})]^2}{[Re(z_{12})]^2 + [Re(z_{12})]^2} \tag{2-22}$$

where z_{ij}(i,j=1,2) are impedance matrix of transformer. The mutual reactive (k_{Im}) and mutual resistive (k_{Re}) coupling factor is represented by [22],

$$k_{Im} = \sqrt{\frac{[Im(z_{12}]^2}{Im(z_{11})Im(Z_{22})}}$$

$$k_{Re} = \sqrt{\frac{[Re(z_{12}]^2}{Re(z_{11})Re(Z_{22})}} \tag{2-23}$$

The k_{Im} is mutual reactive coupling factor, equal to mutual magnetic coupling factor at low frequency but deviates at high frequency due to capacitance between the primary and secondary. The k_{Re} is the mutual resistive coupling factor at high frequency and zero at low frequency due to the coupling between the inductor is dominant. The x in the Eq. (2-22) can also be written in terms of k_{Re}, k_{Im}, $Q_P = \frac{j\omega L_P}{R_P}$,$Q_S = \frac{j\omega L_S}{R_S}$ as [22],

$$x = \frac{1 - k_{Re}^2}{k_{Im}^2 Q_P Q_S + k_{Re}^2} \tag{2-24}$$

In order to obtain higher G_{max}, the x should be lowered by increasing Q_p, Q_s, k_{Re} and k_{Im}. The losses in transformer can be reduced by maximizing for mutual coupling and optimizing for coupling factor. The use of differential pair and transformer, helps to achieve two requirement, one is high linearity and other is high compression point.

2-5 Conclusion

In this chapter, the two stage approach which is used to achieve all the requirements simultaneously for wide range LNA is discussed. The specification requirements for individual stages such as gain, noise figure, and linearity were derived. Negative feedback is used for multiple purposes such as for linearity improvements, noise and impedance match. The use of negative feedback may lead to stability issues, so the frequency compensation technique used to improve stability is discussed. The final architecture used for implementation of 2 stage LNA and its component are explained.

Chapter 3

Linearity enhancement techniques

3-1 Introduction

In a two stage approach, the output stage has to provide high linearity and high compression point. In this chapter, the techniques used to improve linearity and compression point are discussed. Initially, the device characteristics such as DC characteristics, small signal model, and figure of merit are shown. The dominant non-linearities present in the bipolar transistor are identified and the techniques to mitigate them are discussed. These linearity improvement techniques are applied on an "ideal" Gummel Poon transistor representation to better understand their individual impact on the overall linearity. (Note that the Gummel-Poon model allows a much more straightforward simplification of the transistor than the more accurate Mextram model description). Another important requirement of this project is the output 1 dB compression point , which is limited by the technology. A circuit technique to improve the 1 dB compression point is also discussed. For all the simulation in this chapter Cadence Spectre and ADS were used.

In Section 3-2 the device characteristics are discussed. In next Section 3-3, the reference circuit and the dominant non-linearities in a transistor are presented. The technique to improve linearity are discussed in Section 3-4. The limitation of technology and technique to improve compression point is discussed in Section 3-5. In last Section 3-6, the out-of-band linearization technique is applied on the ideal Gummel Poon model to see the impact of each parasitic on linearity.

3-2 Device characteristics

The technology used for this project is 0.25 μm SiGe BiCMOS QUBiC4Xi. In this section, the DC characteristics, small signal model, and figure of merit used to characterize the transistor are discussed.

3-2-1 DC characteristics

In QUBiC4Xi technology, different SiGe bipolar transistors are available. In this project two transistors namely BNY and BNA are used. The output characteristics of BNY and BNA are shown in Figure 3-1 and Figure 3-2, respectively. The collector current I_C is plotted for different value of base to emitter voltage V_{BE} and by varying emitter to collector voltage V_{CE} from 0-5 V. These plots gives information regarding the maximum breakdown voltage BV_{CEO}. This determines the maximum output swing available for these transistors. This property becomes important while considering to achieve high compression point (output power). The BV_{CEO} of BNY and BNA transistors are approximately 1.5 V and 2.5 V, respectively. The transistor BNA HV has high BV_{CEO}, hence it is used for high output delivering stages.

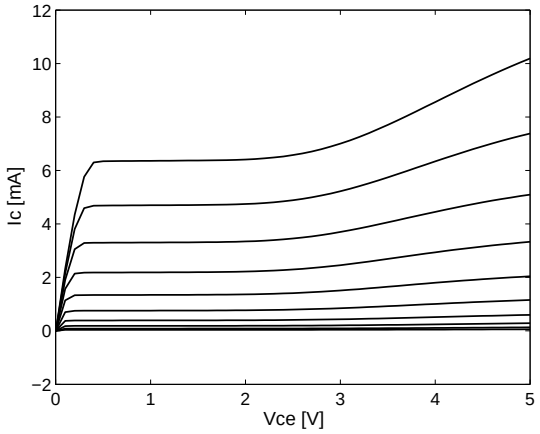

Figure 3-1: I_C vs. V_{CE} characteristic for constant values of V_{BE}, for size 0.3 μm x 1 μm x 1 QUBiC4Xi SiGe BNY BJT

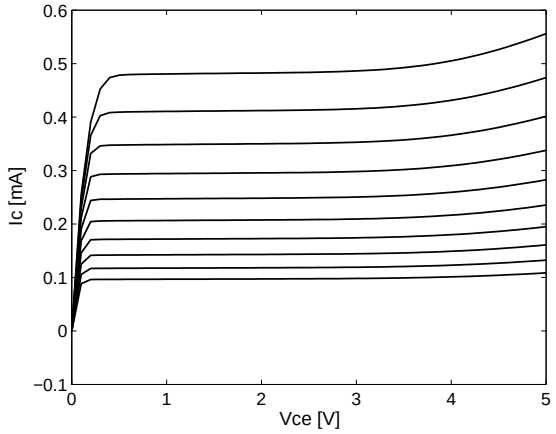

Figure 3-2: I_C vs V_{CE} characteristic for constant values of V_{BE}, for size 0.4 μm x 1 μm x 1 QUBiC4Xi SiGe BNA BJT

3-2-2 Small signal model

Figure 3-3 shows the small signal model of the BJT [23]. The r_b, r_E, r_c are the base, emitter, collector resistances respectively, which are inversely proportional to device scale [16]. The resistor values r_E and r_c are low, due to heavy doping of the emitter and buried layer of the collector. But due to low doping of the base, r_b is considerably large. Each terminal base, emitter and collector has a finite capacitance C_{be}, C_{ce} and C_{bc}, respectively. The r_E and r_c are small hence, often omitted along with C_{bc} and C_{be} [23]. The simplified model, which is used for analysis is shown in Figure 3-4. The small signal model parameters r_π, c_π, g_m, r_b are dependent on the biasing of transistor. These parameters affect the figure of merit for the transistors. The cut off frequency (f_t) and maximum oscillation frequency (f_{max}) are figure of merit generally used for characterizing transistors at high frequency [24].

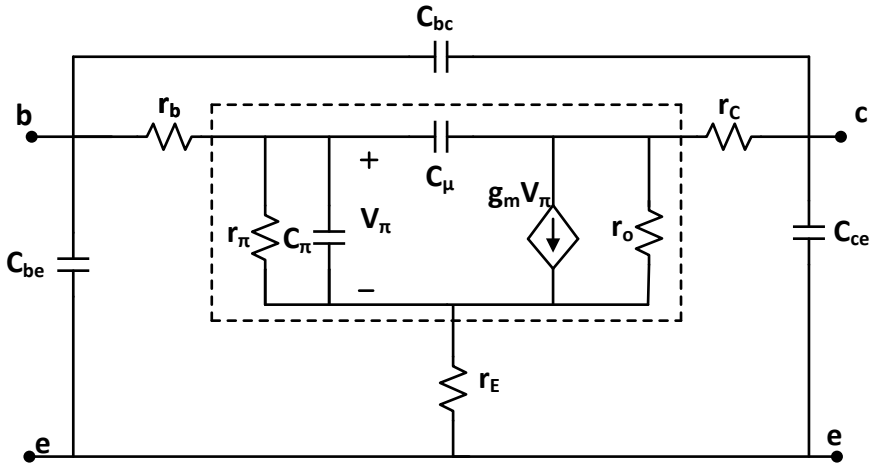

Figure 3-3: Small signal model of BJT

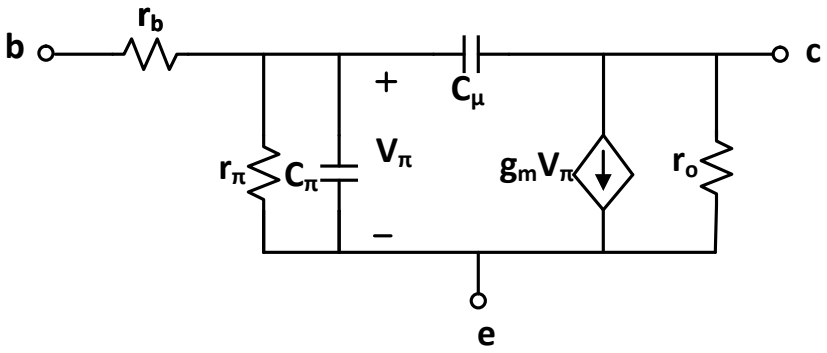

Figure 3-4: Simplified small signal model of BJT

Cut off frequency

"The cut-off or transition frequency f_t is the frequency for which the magnitude of the AC current gain drops to unity for transistor in common emitter configuration with an AC-shorted collector" [24]. The f_t of transistor is dependent on transconductance g_m and capacitance C_π of BJT as given by Eq. (3-1). The capacitance C_π is dependent on two capacitances: junction capacitor C_{je} and diffusion capacitor C_d. The junction capacitor is voltage dependent, whereas diffusion capacitor and g_m are collector current dependent. The g_m increases faster as compared to diffusion capacitance, hence the f_t increases. At higher current levels f_t rolls off due to current crowding and kirk effects [23].

$$f_t = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{3-1}$$

Maximum oscillation frequency

Maximum oscillator frequency f_{max} is defined as "The frequency where the magnitude of the power gain of a transistor becoming unity" [24]. Maximum oscillation frequency is expressed as in Eq. (3-2). It provides additional information regarding the base resistance. The base resistance gives information of speed and noise of the transistor. The f_t and f_{max} of transistors BNY and BNA are shown in Figure 3-5 and Figure 3-6, respectively.

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_b C_\pi}} \tag{3-2}$$

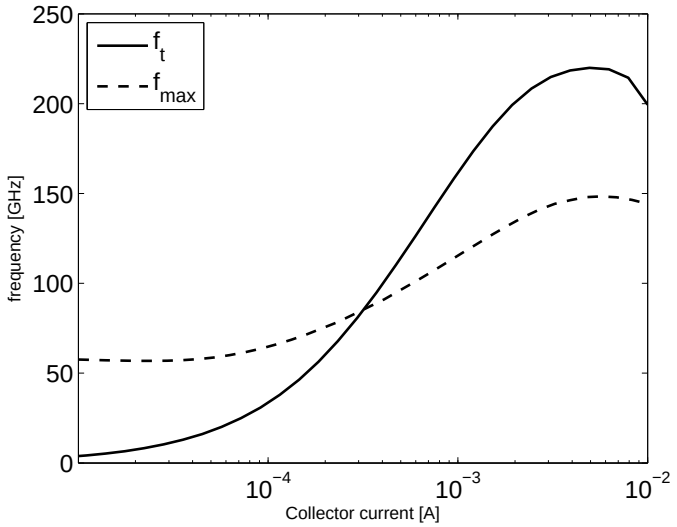

Figure 3-5: f_t and f_{max} is simulated for I_C vs. V_{CE} of 0 V, for size:0.3 μm x 1 μm x 1 QUBiC4Xi SiGe BNY BJT

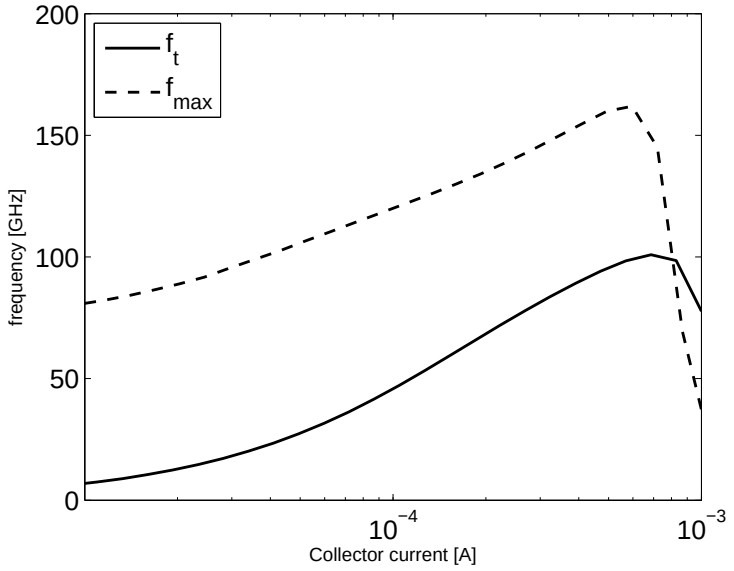

Figure 3-6: f_t and f_{max} is simulated for I_C vs V_{CE} of 0 V, for size:0.4 μm x 1 μm x 1 QUBiC4Xi SiGe BNA BJT

3-3 Dominant non-linearities

From the previous section the DC characteristic, figure of merit of the transistor are known. Before using these transistor at high frequencies. circuit design, it is required to identify dominant sources of non-linearities. The transistors linearity depends on the interaction between the transistor and the surrounding circuitry, such as loading impedance and harmonic termination. Consequently, a reference circuit is required for distortion characterization of a device.

Reference circuit for distortion characterization

To analyze the non-linearity of a real transistor a reference circuit is used. High frequency systems are often terminated by 50 Ω impedance at the input and the output, which influences the fundamental matching conditions. When considering harmonic and baseband terminations the reference circuit needs to be designed carefully. Since any change in the impedance at baseband and second harmonic frequencies, will effect the linearity of the amplifier. Figure 3-7 shows the simple reference circuit used for determining the linearity performance of the device. The circuit comprises of two negative feedback loops provided through R_1 and R_2. By proper selection of values of R_1 and R_2, the input and the output can be matched to 50 Ω. The transistor size used for this experimentation is 0.4 μm x 20.7 μm x 1 QUBiC4Xi BNA transistor. The linearity check for this circuit was done with two tone (ω_1, ω_2) simulation at -30 dBm tone power each.

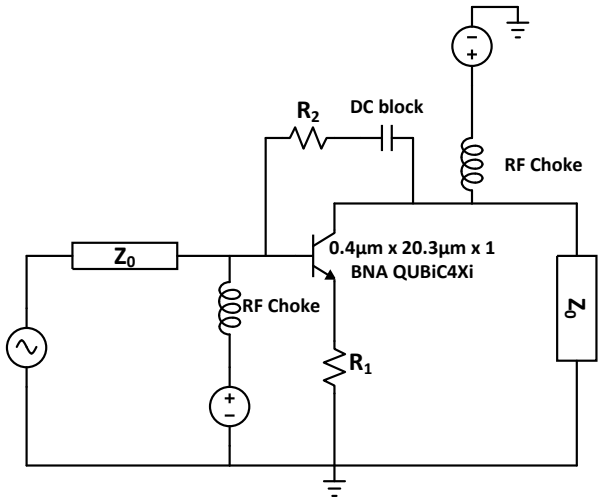

Figure 3-7: Reference circuit for distortion characterization

Regions of non linearity

For the circuit shown in Figure 3-7, contour of OIP3 is plotted. To obtain the contour plot, Mextram Spectre model was used to derive the model parameters for BJT in Agilent ADS. Using this model, OIP3 simulations are done in Agilent ADS. Contour plot of OIP3 is obtained from the resulting simulated data using MATLAB. Figure 3-8 shows constant OIP3 in dBm on $I_C(V_{CE})$ plane at 1.84 GHz for the device size 0.4 μm x 20.7 μm x 1 QUBiC4Xi SiGe. From the contour, three dominant regions can be identified.

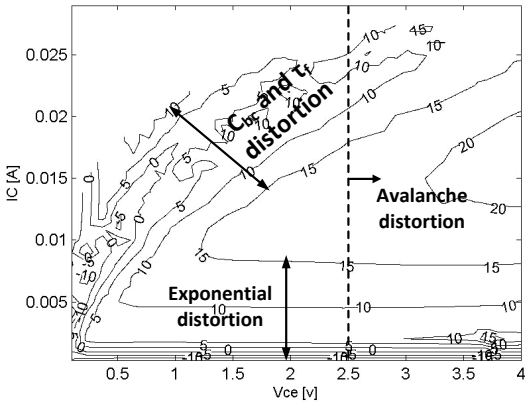

Figure 3-8: OIP3-contours in dBm on the $I_C(V_{CE})$ plane at 1.84 GHz of the 0.4μm x 20.7μm x 1 QUBiC4Xi SiGe BNA transistor

1) Exponential distortion: At low current levels ($I_C < I_C@f_{tpeak}$), linearity is independent of collector to emitter voltage V_{CE}, but only varies with collector current, which can be seen in Figure 3-8. This is due to the exponential dependency of collector current I_C, base current I_B, and diffusion capacitance C_{be} on base to emitter voltage V_{be} ($I_C \approx I_s e^{\frac{qV_{be}}{kt}}$) [17]. The output linearity is set by the DC bias current. The technique used to reduce the non-linearity due to exponential behavior are implicit IM3 cancellation/local feedback and out-of-band IM3 cancellation, which is discussed in Section 3-4-1 and in Section 3-4-2 respectively.

2) Base-collector/nonlinear transit time: At higher current levels, the exponential distortion becomes less prominent. The non-linearities increase due to the non-linear feedback effect of base to collector capacitance C_{jc}, forward transit time τ_f. Both these effects lead to base charge modulation by the collector voltage and current swing. This is dominant at lower V_{CE} and at higher current levels. The non-linear effect of capacitance C_{jc} and τ_f impacts the OIP3. As the V_{CE} increases till the reverse breakdown voltage, the reverse biased CB junction capacitance decreases, which makes it more linear due to this linearity improves at high V_{CE}. The technique used to reduce effect of feedback capacitor is called unilateralization/neutralization. A transformer is used in feedback to nullify base to collector capacitor [25]. The cascode of CE- CB stage is used to reduce the feedback from output to input, which is another most commonly used technique.

3) Avalanche effect: Although not fully visible in Figure 3-8, at very high V_{CE}, (i.e beyond the breakdown voltage) avalanche effect occurs and results in nonlinear current feedback from base to collector. Due to this non linear feedback, linearity may improve or degrade depending on the phase of the distortion. The operation of transistor in this region should be avoided.

3-4 Techniques to improve linearity

The dominant non-linearities in bipolar junction transistor were identified in previous section. The techniques used to reduce these non-linearities are discussed in this section. The techniques are as follows: 1)Implicit IM3 cancellation
2)Out-of-band linearization
3)2^{nd} harmonic short

3-4-1 Implicit IM3 cancellation

At high frequency, implicit IM3 cancellation (local feedback) is applied to improve linearity. In order to analyze implicit IM3 cancellation technique, a non linear model has been used, which is shown in Figure 3-9 [26], where Z_b is the base impedance which include R_s and r_b, Z_e is the emitter impedance which includes r_e and degeneration impedance, C_{je} is the base emitter capacitance, C_b is base charging capacitor, I_b is base current and I_c is collector current. The IM3 product at third harmonic frequency is given by Eq. (3-3) [26].

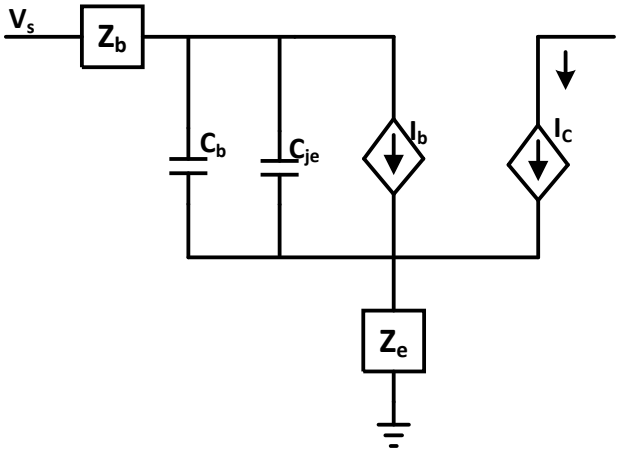

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Figure 3-9: Common emitter transconductance stage model

$$
\begin{aligned}
|IM3| &= |\frac{3}{4}\frac{A_3(s_a, s_a, -s_b)}{A_1(2s_a - s_b)}||V_s^2| \\
&\approx |\frac{A_1}{I_Q}|^3|\frac{V_T}{4}[1 + sC_{je}Z(s)] \\
\mathbf{x}\{-1 &+ \frac{A_1(\Delta s}{g_m}[1 + \Delta sC_{je}Z(\Delta s)] \\
+\frac{A_1(2s)}{2g_m}&[1 + 2sC_{je}Z(2s)]\}||V_s|^2
\end{aligned}
\tag{3-3}
$$

where V_s is the power of the voltage source, A_n is the volterra series co-efficient, which is written as,

$$A_1(s) = \frac{g_m}{sC_{je}Z(s) + s\tau g_m Z(s) + \frac{g_m Z(s)}{\beta} + 1 + g_m Z_e(s)} \tag{3-4}$$

From the above equation $|IM3|$ depends on magnitude of ,

$$[1 + sC_{je}Z_b(s) + sC_{je}Z_e(s)] \tag{3-5}$$

From Eq. (3-3) IM3 also depends on cube of the small signal transconductance, i.e bias current I_Q. By increasing the biasing current the linearity can be improved until a certain limit. By using an inductive degeneration as shown in Figure 3-10, the sC_{je} along with Z_e becomes negative "-1" and cancel "1" term in Eq. (3-5). With a proper selection of degeneration inductor L_e, transconductance g_m and size of the transistor A_e implicit IM3 cancellation can be achieved.

The optimum choice of the base resistance, simultaneous impedance and noise match can be achieved. The two disadvantages of using a degeneration inductor is that, one it reduces gain and second that it is often not compatible for low noise operation.

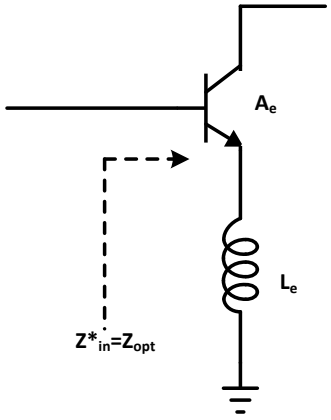


Figure 3-10: Inductive degenerative implicit IM3 cancellation [27]

3-4-2 Out of band linearization

Out of band IM3 distortion cancellation has the advantage over the other IM3 improvement technique, that it does not compromise for fundamental gain and noise match nor the DC power. It provides orthogonality between the gain, noise and impedance match vs the linearity optimization [17]. This is due to the fact that the linearization completely depends on the even order termination. The third order non-linearities are generated by:

1) direct mixing through the 3^{rd} order non-linearity the device
2) indirect mixing of fundamental and 2^{nd} order distortion product with 2^{nd} order non-linearity, yielding again IM3 products

By controlling the termination of the 2^{nd} order non-linearities, indirect mixing can be controlled such that it provides a IM3 distortion signal with an equal amplitude but with an opposite phase compared to IM3 signal resulting from direct third-order non-linearities. This process is shown in Figure 3-11.

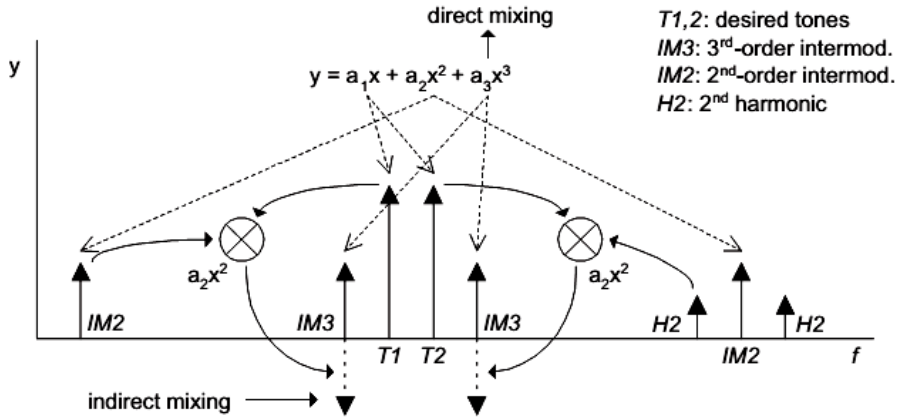


Figure 3-11: Out of band IM3 cancellation [17]

The large signal circuit used for investigation of linearity improvement for CE stage using out-of-band linearization is shown in Figure 3-12 [17]. The exponential distortion is considered to be the dominant source of the non-linearity. The effect of base to collector capacitance is also considered for derivation, since the distortion cancellation depends on all the circuit parasitics. The IIP3 for CE stage can be expressed as [17],

$$IIP3 = \frac{1}{6R|H_{1b}(s)|^3|D(s)||\varepsilon(\Delta s, 2s)|} \tag{3-6}$$

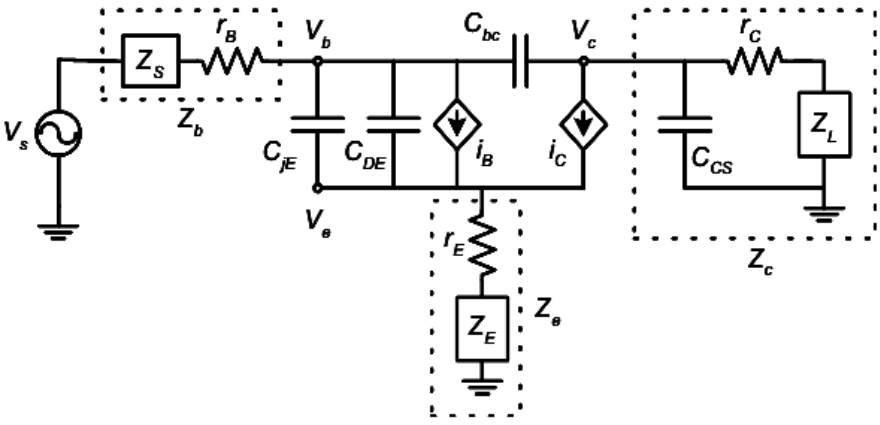


Figure 3-12: Large signal model for CE stage [17]

For Eq. (3-6), three different terms can be identified. Firstly, $H_{1b(s)}$ is transfer function of the

input voltage source V_s to the internal base emitter voltage, which is expressed as,

$$H_{1b}(s) = \frac{1 + sC_{bc}Z_c}{1 + g_m(\frac{Z_b}{\beta_f} + Z_e) + s[C_\pi(Z_b + Z_e) + C_{bc}(Z_b + Z_e + g_m\overline{Z})] + s^2C_\pi C_{bc}\overline{Z}} \tag{3-7}$$

where $\overline{Z} = Z_bZ_e + Z_bZ_c + Z_eZ_c, Z_b$ and $Z_{ed}(s)$ are the impedance seen from the base, collector and emitter node of the transistors respectively, at the corresponding frequency s.

Secondly, $D(s)$ represents the third order non-linearity term from base-emitter junction to collector node which is written as,

$$D(s) = \frac{1}{g_m}.\frac{1 + s[C_{jE}(Z_b + Z_e) + C_{bc}Z_b] + s^2C_{bc}\tau Z_b}{1 - sC_{bc}(r_e + Z_e) - s^2C_\pi C_{bc}r_eZ_e} \tag{3-8}$$

Thirdly, $\varepsilon(\Delta s, 2s)$ represents influence of the second order non-linearities on the IM3 distortion. It is expressed as,

$$\varepsilon(\Delta s, 2s) = \frac{g_{m,3}}{3}[2F(\Delta s) + F(2s)] \tag{3-9}$$

The factor $\varepsilon(\Delta s, 2s)$, determines the out-of-band impedance impact on the linearity of the full circuit. If two terms in Eq. (3-9) ($F(\Delta s)$ and $F(2s)$) are reduces to zero, then term $\varepsilon(\Delta s, 2s)$ will reduce, improving the linearity. The F(s) can be represented as,

$$F(s) = \frac{1 - 2g_m(\frac{Z_b}{\beta_F} + Z_e) + s[C_h(Z_b + Z_e)] + C_{bc}(Z_b + Z_c - 2g_m\overline{Z}) + s^2C_{bc}C_h\overline{Z}}{1 + g_m(\frac{Z_b}{\beta_F} + Z_e) + s[C_\pi(Z_b + Z_e)] + C_{bc}(Z_b + Z_c + g_m\overline{Z}) + s^2C_{bc}C_\pi\overline{Z}} \tag{3-10}$$

A first order approximation of Eq. (3-10) is assumed to analyze a practical IM3-cancellation technique for CE-stage. For simplicity, $Z_c(\Delta s) = Z(2s) \approx 0$ and $\Delta s \approx 0$ is considered to give a simplified equation represented as [17],

$$F(\Delta s) = \frac{1 - 2g_m(\frac{Z_b}{\beta_F} + Z_e)}{1 + g_m(\frac{Z_b}{\beta_F} + Z_e)} \tag{3-11}$$

$$F(2s) = \frac{1 - 2g_m(\frac{Z_b}{\beta_F} + Z_e) + 2s[(C_{je} - 2\tau g_m)(Z_b + Z_e)] + C_{bc}Z_b(1 - 2g_mZ_e)}{1 + g_m(\frac{Z_b}{\beta_F} + Z_e) + 2s[(C_{je} - \tau g_m)(Z_b + Z_e)] + C_{bc}Z_b(1 + g_mZ_e)} \tag{3-12}$$

From the Eq. (3-11) and Eq. (3-12), $F(\Delta s)$ and $F(2s)$ are functions of impedance termination at Z_b, Z_e, emitter area A_e and $g_m = \frac{I_C}{v_t}$. Therefore, two types of impedance termination for out-of-band matching can be used at base and emitter.

Base tuning

The impedance termination for base tuning at emitter and base terminal of CE stage at frequencies Δs and $2s$ can be selected as,

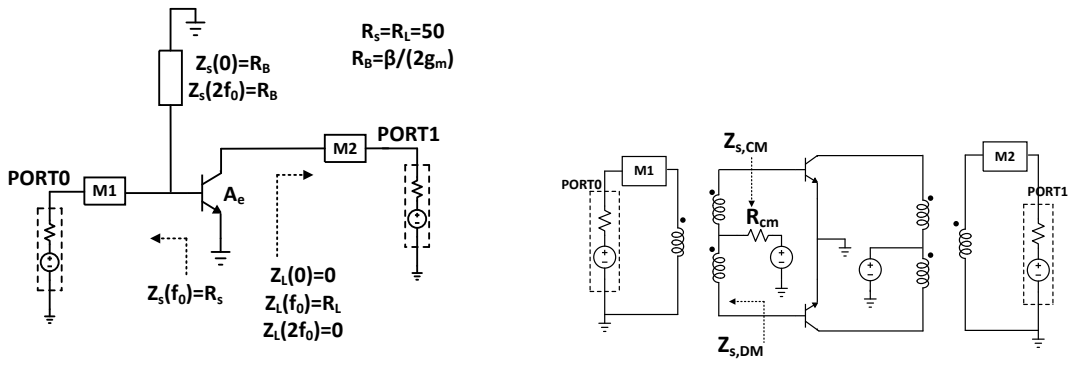
$$\begin{aligned} Z_b(\Delta s) &= \frac{\beta}{2g_m} \qquad Z_e(\Delta s) = 0 \\ Z_b(2s) &= \frac{\beta}{2g_m} \qquad Z_e(2s) = 0 \end{aligned} \tag{3-13}$$

Substituting Eq. (3-13) in Eq. (3-11) and Eq. (3-12), yields

$$|2F(\Delta s) + F(2s)| = \frac{2s\beta(C_{je} - 2\tau g_m) + C_{bc}\beta}{\frac{3g_m}{2} + 2s\beta(C_{je} - 2\tau g_m) + C_{bc}\beta} \tag{3-14}$$

Figure 3-13 shows the circuit for out-of-band matching base tuning. The implementation of out-of-band matching, independent of fundamental termination is difficult in single-ended configuration. The differential topology provides orthogonality between even order (common mode) and odd order (Differential mode) frequencies. This basic concepts of out-of-band tuning for single ended CE stage can be extended to differential CE stage. The correct termination depends on control even-order harmonics. At the input transformer, the even order (common mode) are developed across $Z_{S,CM}$, while is the same way odd-order is generated across $Z_{S,DM}$. The condition to satisfy IM3 requirement for common mode is given by [17].

$$Z_{S,CM} = R_{CM} = \frac{\beta_f}{4g_{m,d3}} = \frac{\beta_f \tau_f}{2(C_{je} + C_{bc})} \tag{3-15}$$



(a) Single stage [28] **(b)** Differential stage [17]

Figure 3-13: Impedance termination for out-of-band base tuning for single stage and differential stage

Emitter tuning

The Figure 3-14 shows the schematic for emitter tuning. The out-of-band impedance termination at frequency Δs and $2s$ are selected as,

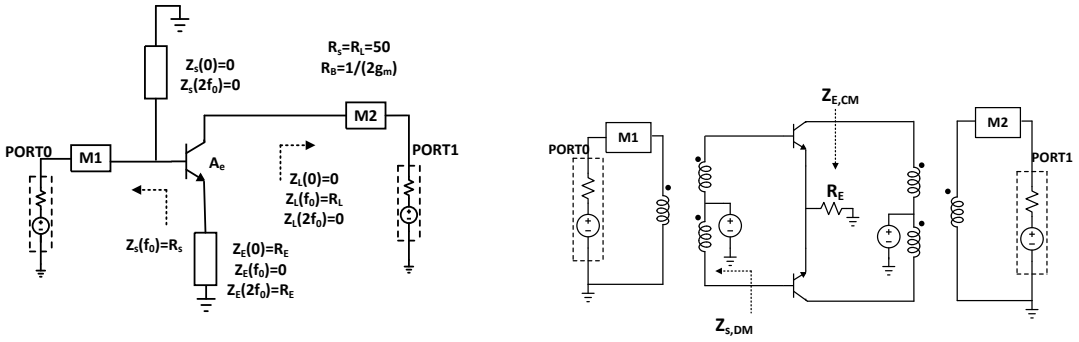
$$\begin{aligned} Z_b(\Delta s) &= 0 \qquad Z_e(\Delta s) = \frac{1}{2g_m} \\ Z_b(2s) &= 0 \qquad Z_e(2s) = \frac{1}{2g_m} \end{aligned} \tag{3-16}$$

Substituting Eq. (3-16) in Eq. (3-11) and Eq. (3-12), yields

$$|2F(\Delta s) + F(2s)| = \frac{2s(C_{je} - 2\tau g_m) + 2C_{bc}g_m}{\frac{3g_m}{2} + 2s(C_{je} - 2\tau g_m) + 2C_{bc}g_m} \tag{3-17}$$

The advantage of differential topology already discussed holds good in out-of-band emitter tuning also. The requirement for IM3 cancellation on common mode impedance is,

$$Z_{E,CM} = R_E = \frac{1}{4g_m} = \frac{V_T}{2I_{EE}} \tag{3-18}$$



(a) Single stage [28] **(b)** Differential stage [17]

Figure 3-14: Impedance termination for out-of-band emitter tuning for single stage and differential stage

3-4-3 2^{nd} harmonic short

One of the reasons for generation of third order and fifth order distortion at high currents is due to indirect mixing of odd and even order distortion with even order non-linearities. The 2^{nd} order and baseband generated non-linearities by the transistor can be reduced by the use of

even harmonic shorts. The harmonic short is provided by tuning source and load impedance at baseband $Z_S(\Delta\omega)$ and $Z_L(\Delta\omega)$, where $\Delta\omega = |\omega_1 - \omega_2|$ and at second harmonic $Z_S(2\omega)$ and $Z_L(2\omega)$, where $2\omega = 2\omega_1, 2\omega_2$. The harmonic short is provided at input and output by using a series LC resonator as shown in Figure 3-15 [29].

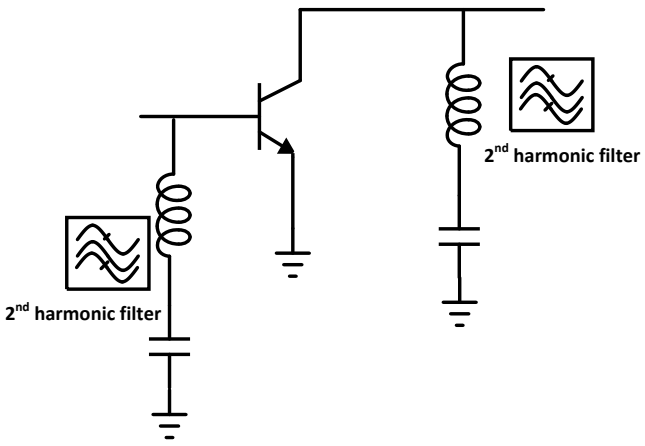


Figure 3-15: A 2^{nd} harmonic termination is provided at input and output by series resonator [29]

The harmonic termination should not impact the performance of an amplifier at fundamental frequency. For matching at fundamental frequency an additional matching circuit would be required. It is difficult to achieve 2^{nd} harmonic short independent of fundamental matching [29]. This problem can be solved by using a differential structure as shown in Figure 3-16.

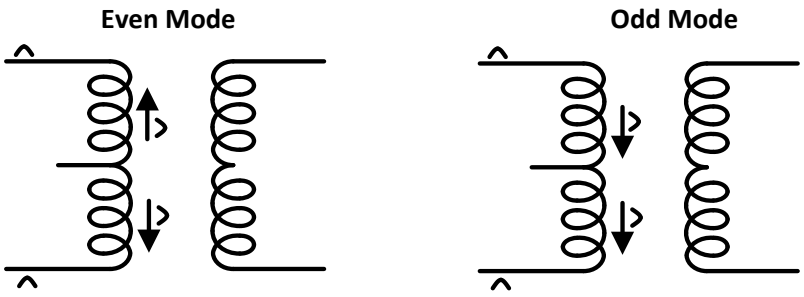


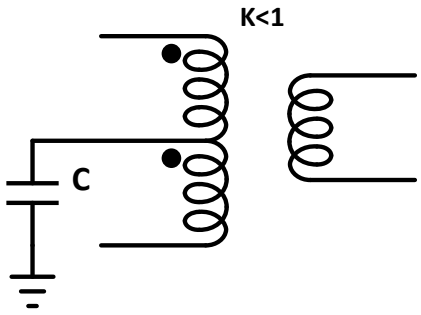
Figure 3-16: Even and odd mode operation [29]

In differential structure with center tap, even and odd mode of operation can be decoupled. For

ideal transformer it can be seen in Figure 3-16, that even mode (common mode) cancels out, showing a short for second harmonic and baseband. For odd mode (differential mode) the two signal do not cancel, showing desired operation for fundamental frequency. This helps to set the impedance for fundamental and second harmonic independently.

In practical transformer, the coupling factor k is less than 1. Due to reduction in the coupling factor and capacitive coupling between the primary and the secondary coils, the impedance at the center tap (second harmonic) is not a perfect short. In differential mode of operation this will result in loss of the signal. By using the finite impedance of the coil, a resonant L,C can be provided at center tap. The resultant configuration is as shown in Figure 3-17. The value of the capacitor depends on inductance of the coil, which is given by [29],

$$C = \frac{2}{\omega^2 L_p} \tag{3-19}$$



.

Figure 3-17: Resonating out parasitic inductance

3-5 OP1dB consideration

The compression point is a standard for specifying the output power of an amplifier. The total output power delivered by an amplifier is defined by Eq. (3-20), where V_{out} is the amplitude of the output signal and R_L is the load impedance. From Eq. (3-20), output power can be increased either by increasing the output swing or reducing output impedance. The output swing is limited by transistor's BV_{CEO}, which is $\approx$2.5 V for the technology used for this project.

When the output impedance is matched to 50 Ω, for this combination of output swing and output impedance maximum achievable output power is 18 dBm. The load impedance needs to be reduced to achieve high compression point. An impedance transformation from high to low can be done using a transformer. The impedance transformation is equal to turns ratio squared. It is

represented in Eq. (3-21), where n is turns ratio, R_p and R_s are impedance connected at primary and secondary, respectively. The load impedance required to achieve +24 dBm of OP1dB is ≈12 Ω for a output swing of 2.5 V. The maximum achievable output compression point will be limited by the losses of the transformer.

$$P_{out} = V_{out}^2 / 2R_L \tag{3-20}$$

$$n = \sqrt{\frac{R_p}{R_s}} \tag{3-21}$$

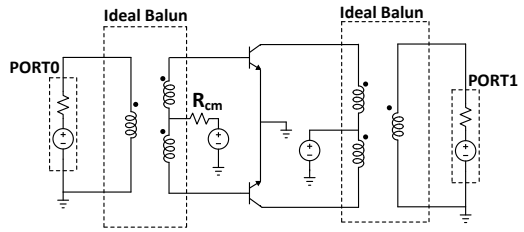
3-6 Simulation results

In this section, ideal Gummel Poon model is used for simulation study. The simulation are done to support the previous discussion on linearity enhancement techniques. Some of the model parameters are changed to find the impact of each individual parasitic on the linearity. The parameters whose values are changed are C_{je}, τ_f, C_{jc}. The two key IM3 compensation techniques studied are out-of-band base tuning and emitter tuning, along with overall negative feedback.

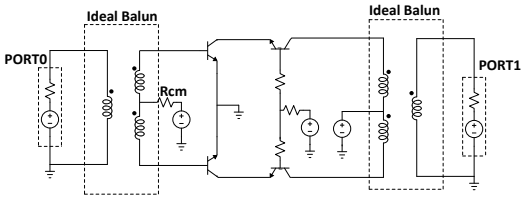
3-6-1 Base tuning

The simulation for out-of-band matching base tuning is performed on differential pairs, such as CE and cascode configuration. The overall negative feedback is applied to analyze the effect of feedback on an out of band matching. Hence, differential circuits are simulated with and without feedback. The out-of-band base tuning discussed in Section 3-4-2 for CE stage is extended for analysis of a differential cascode as well. The schematics used for analysis out-of-band base tuning are shown in Figure 3-18.

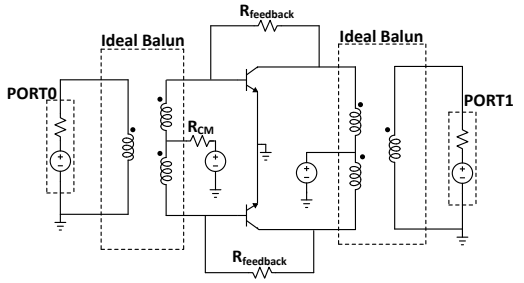
In order to convert single ended input to differential output and vice-versa, an ideal balun is used at both input and output. The ideal output balun, provide a perfect even harmonic short and as such reduces the non-linearities at the second and baseband frequencies. At the input the resistive based out-of-band matching for base tuning is used, for this purpose a resistor R_{cm} is used at the centertap of input balun as shown in Figure 3-18.



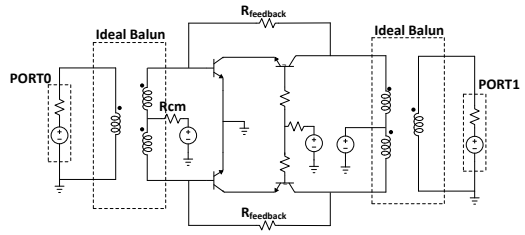
(a) Differential CE stage



(b) Differential cascode stage



(c) Differential CE stage with feedback



(d) Differential cascode stage with feedback

Figure 3-18: Schematic circuits for differential configuration with out-of-band matching for base tuning

From Section 3-4-2, out-of-band base tuning including all the parasitic is expressed as,

$$|2F(\Delta s)+F(2s)| = \frac{2s\beta(C_{je}-2\tau g_m)+C_{bc}\beta}{\frac{3g_m}{2}+4s\beta(C_{je}-2\tau g_m)+C_{bc}\beta} \tag{3-22}$$

A step by step analysis is done to see the effect of individual transistor parasitics on linearity. First analysis is done with ideal Gummel Poon model (no capacitance, no delay). In the next step parasitic base to emitter capacitance C_{je}, transit time τ_f are included and at last effect due to base to collector capacitance C_{jc} is also monitored.

Ideal Gummel Poon model

The capacitive parasitic of the bipolar model are considered to be zero shown in Table 3-1. As all the parasitics are assumed to be zero, the Eq. (3-22) can be approximated to zero. Hence, the only source of distortion is the exponential distortion.

Table 3-1: Parameters used in ideal Gummel Poon model

Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0 F
τ_f	Ideal transit time	0 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0 F
β	Forward gain	100

The contour plots are plotted using MATLAB, where the simulation data is extracted from Agilent ADS. The contour of constant OIP3 in dBm for input tone power of -30 dBm is shown in Figure 3-19. This figure shows the variation of linearity due to the center tap resistance R_{cm} and collector current for all the circuit configurations in Figure 3-18.

From these results, it can be concluded that linearity improves with increase in collector current. The OIP3 contours of the differential CE (see Figure 3-19(a)) and cascode stage (see Figure 3-19(b)), yields more or less the same maximum achievable OIP3. Any visible changes in contour plots are due to the difference in output loading condition of differential CE and differential cascode stages. The OIP3 contour plots of the differential CE (see Figure 3-19(c)) and differential cascode (see Figure 3-19(d)) stage including feedback, shows improvement in maximum achievable OIP3. As such it can be concluded that exponential distortion can be reduced by out-of-band cancellation method and by using a combination of out-of-band cancellation and overall feedback, yielding even higher linearity levels.

C_{je} and τ_f

In this following analysis, the effect of out-of-band matching base tuning when the parasitic capacitance (C_{je}) and transit time (τ_f) are non-zero, is investigated. Table 3-2 shows the values used for Gummel Poon model.

Table 3-2: Parameters used for simplified Gummel Poon model

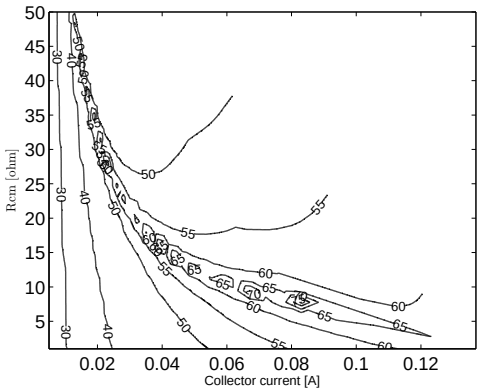
Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0.04 pF
τ_f	Ideal transit time	10 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0 F
β	Forward gain	100

The input impedance C_π is expressed as,

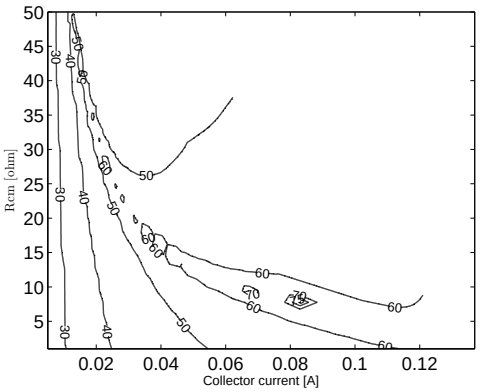
$$C_\pi = C_b + C_{je} \tag{3-23}$$

where C_b is the base-charging capacitance.

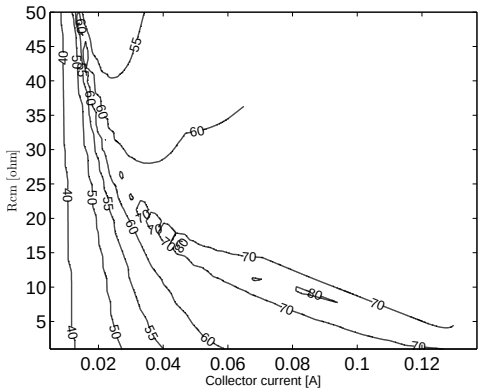
$$C_b = \tau_f g_m \tag{3-24}$$



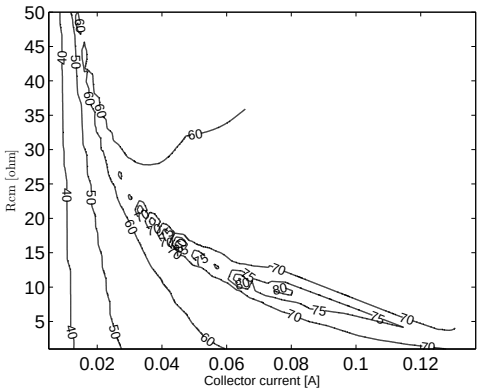
(a) OIP3 contour for differential CE stage with out-of-band base tuning



(b) OIP3 contour for differential cascode stage with out-of-band base tuning



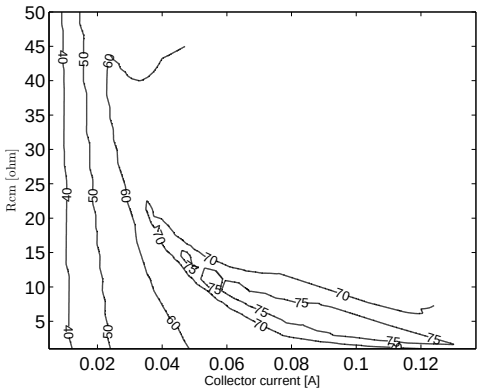
(c) OIP3 contour for differential CE with feedback stage with out-of-band base tuning



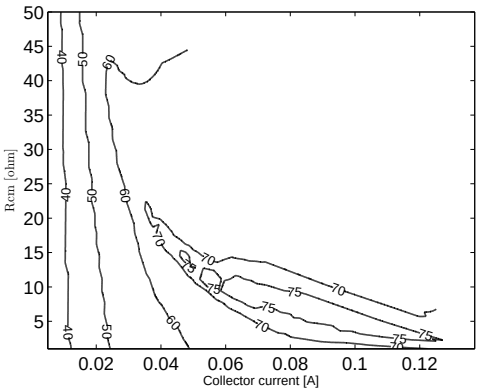
(d) OIP3 contour for differential cascode with feedback stage with out-of-band base tuning

Figure 3-19: Contour out-of-band matching for base tuning, for ideal Gummel Poon model

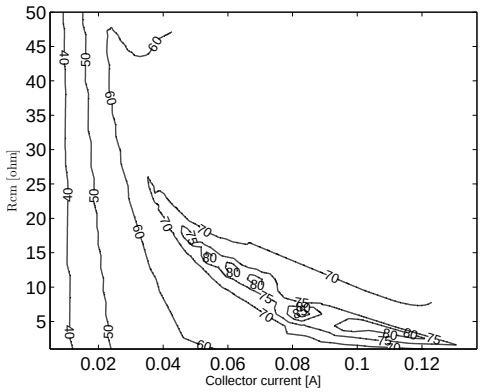
The base diffusion capacitance is proportional to g_m and τ_f [18], hence the transistor linearity depends also on transconductance. The τ_f and β are constant for a transistor, whereas parasitic capacitance C_{je} is constant for a particular size of transistor. Thus, for a given transistor size only g_m can be changed. The contour of constant OIP3 in dBm for input tone power of -30 dBm is shown in Figure 3-20 for all the circuits in Figure 3-18, respectively. The Figure 3-20 shows OIP3 contour by varying collector current and center tap resistor R_{cm}. At a particular current level, when $I_C = C_b V_t / 2\tau_f$, the non-linearities due to C_b gets canceled [30] and for a proper combination of C_{je}, τ_f and g_m a high OIP3 is achieved, which can be seen from Eq. (3-22) and Figure 3-20.



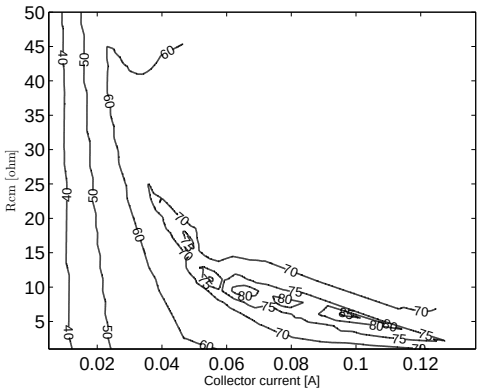
(a) OIP3 contour for differential CE stage with out-of-band base tuning



(b) OIP3 contour for differential cascode stage with out-of-band base tuning



(c) OIP3 contour for differential CE with feedback stage with out-of-band base tuning



(d) OIP3 contour for differential cascode with feedback stage with out-of-band base tuning

Figure 3-20: Contour out-of-band matching for base tuning, for ideal Gummel Poon model with C_{je} and τ_f

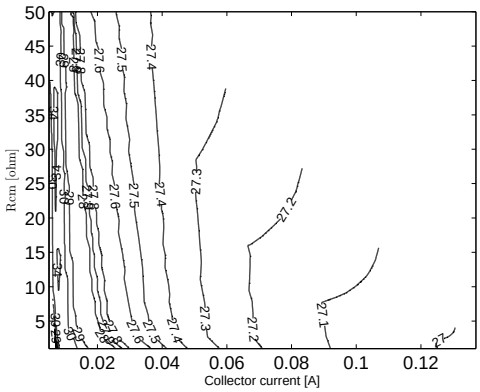
Base to collector capacitance

In this simulation, all the parasitics contributing for non-linearities are considered. Table 3-3 shows the values of parasitics used.

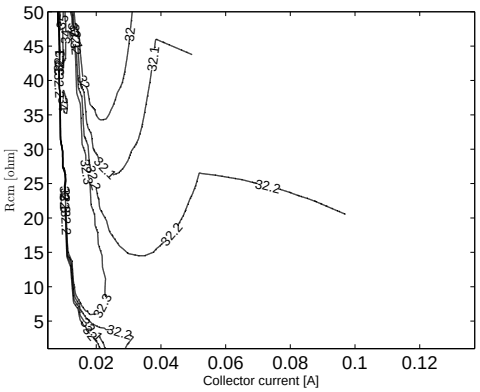
Table 3-3: Parameter used for simplified Gummel Poon model

Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0.04 pF
τ_f	Ideal transit time	10 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0.5 fF
β	Forward gain	100

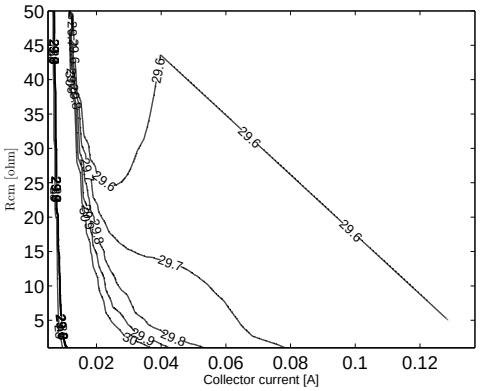
Due to C_{jc}, there is non-linear feedback from collector to base of transistor, therefore the transfer



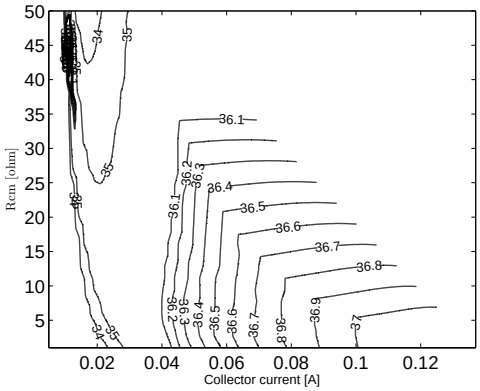
(a) OIP3 contour for differential CE stage with out-of-band base tuning



(b) OIP3 contour for differential cascode stage with out-of-band base tuning



(c) OIP3 contour for differential CE with feedback stage with out-of-band base tuning



(d) OIP3 contour for differential cascode with feedback stage with out-of-band base tuning

Figure 3-21: Contour out-of-band matching for base tuning, for ideal Gummel Poon model with C_{je}, τ_f and C_{jc}

function of transistor has become more nonlinear. The non-linearities introduced by C_{jc} depends on collector to base voltage and collector current.

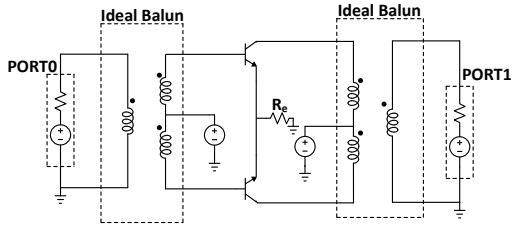
The contour of OIP3 in dBm for input tone power of -30 dBm is shown in Figure 3-21 for all the circuits in Figure 3-18, correspondingly. The figure shows OIP3 contour by varying collector current and centertap resistor R_{cm}. In earlier case, in ideal Gummel Poon and with parasitic C_{je} and τ_f the maximum achievable OIP3 was higher. But now due to the introduction of parasitic capacitance C_{jc} reduced OIP3 to lower levels. The resistor R_{cm} does not help anymore in controlling the second order indirect mixing to improve linearity.

By applying feedback to differential CE stage, the achievable OIP3 (see Figure 3-21(c)) has increased compared to differential CE without feedback. In differential cascode case the effect

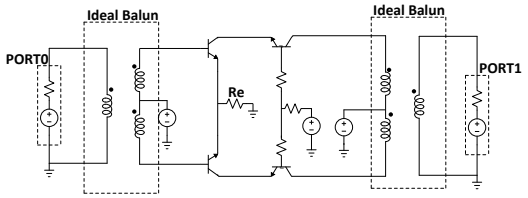
of capacitor C_{jc} of common emitter stage is reduced. Hence, achievable OIP3 in the case of differential cascode(see Figure 3-21(b)) is higher. Further, by applying feedback the linearity is improved for even high currents(see Figure 3-21(d)).

3-6-2 Emitter tuning

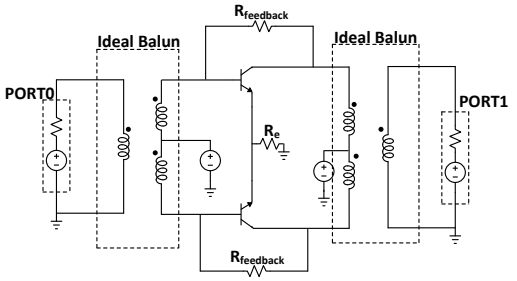
In the following simulation, out-of-band emitter tuning has been followed applied in similar manner as out-of-band base tuning. Four different pair circuits are simulated, i.e the differential CE and differential cascode with and without feedback. The schematic of all the four circuits are shown in 3-22. An ideal balun is used at input and output to provide perfect even harmonic short. The resistive based out-of-band matching emitter tuning is done with a resistor R_e at the virtual ground in differential configuration. From Section 3-4-2 it is clear that out-of-band emitter tuning



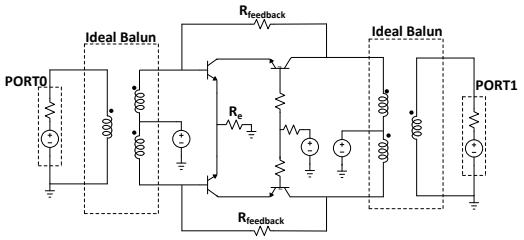
(a) Differential CE stage



(b) Differential cascode stage



(c) Differential CE stage with feedback



(d) Differential cascode stage with feedback

Figure 3-22: Schematic circuits for differential configuration with out-of-band matching for emitter tuning

with all the parasitic can be represented as,

$$|2F(\Delta s)+F(2s)| = \frac{2s(C_{je}-2\tau g_m)+2C_{bc}g_m}{\frac{3g_m}{2}+2s(C_{je}-2\tau g_m)+2C_{bc}g_m} \tag{3-25}$$

Ideal Gummel Poon model

The value of parasitic for the bipolar model are considered to be zero as in Table 3-4. The only source of non-linearity is due to exponential distortion.

Table 3-4: Parameters used for simplified Gummel Poon model

Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0 F
τ_f	Ideal transit time	0 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0 F
β	Forward gain	100

As the parasitics are assumed to be zero, the Eq. (3-25) can be approximated to zero. The contour of OIP3 in dBm for input tone power of -30 dBm is shown in Figure 3-23. This figure shows the variation of OIP3 due to resistance R_e and collector current for all the circuit configuration in Figure 3-22, correspondingly. The linearity improves with increase in collector current. It can be seen from the Figure 3-23(a) (b), that exponential distortion is reduced by out-of-band emitter tuning. By combing both out-of-band cancellation and feedback, the linearity can be improved to even higher levels (see Figure 3-23(c)(d)). Note that the impedance levels needed for emitter compensation at higher current levels can be quite low.

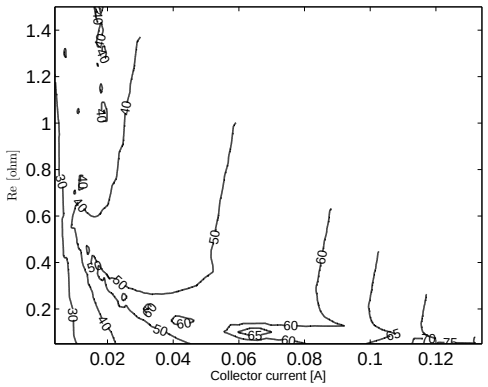
C_{je} and τ_f

In this simulation, the effect of out-of-band emitter tuning when the depletion-capacitance (C_{je}) and base transit time (τ_f) present are investigated. The Table 3-5 shows the value used for Gummel Poon model.

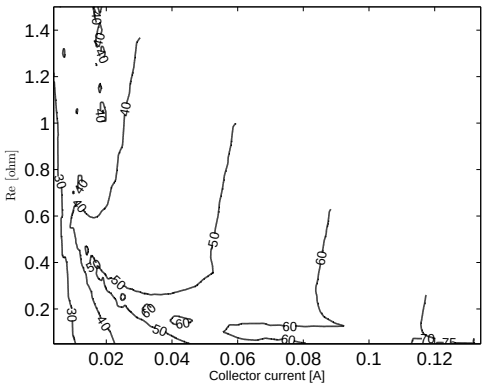
Table 3-5: Parameters used for simplified Gummel Poon model

Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0.04 pF
τ_f	Ideal transit time	10 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0 F
β	Forward gain	100

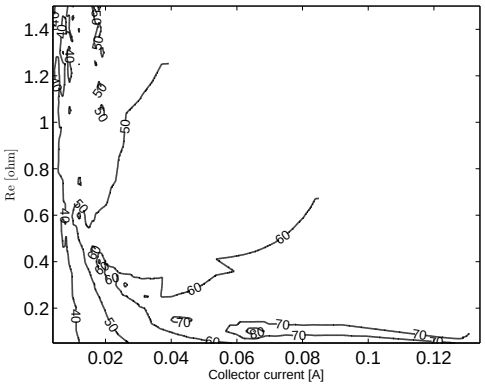
As discussed in Section 3-6-1, base diffusion capacitance is proportional to g_m and τ_f [18] and only variable quantity for a transistor is g_m. The contour of constant OIP3 in dBm for input tone power of -30 dBm is shown in Figure 3-24 for all the circuits in Figure 3-22. These figures shows OIP3 contour by varying g_m and center tap resistor R_e. For a proper combination of C_{je}, τ_f and g_m, the IM3 products reduces, to improve linearity. So high OIP3 can be achieved, this can be seen in Figure 3-24.



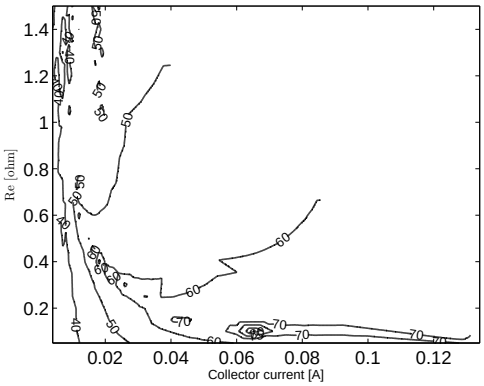
(a) OIP3 contour for differential CE stage with out-of-band emitter tuning



(b) OIP3 contour for differential cascode with out-of-band emitter tuning



(c) OIP3 contour for differential CE stage with feedback and out-of-band emitter tuning



(d) OIP3 contour for cascode stage with feedback and out-of-band emitter tuning

Figure 3-23: Contour out-of-band matching for emitter tuning, for ideal Gummel Poon model

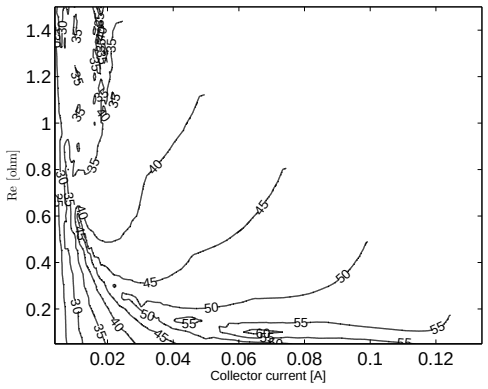
Base to collector capacitance

The parasitic contributing to non-linearities are considered as in Table 3-6.

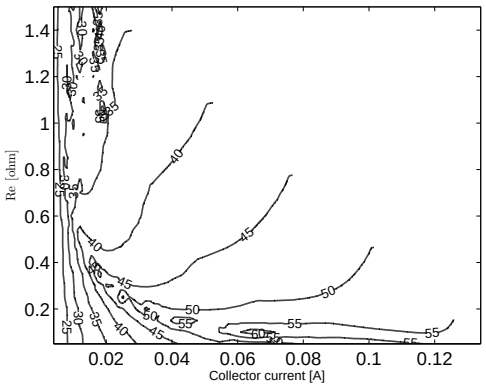
Table 3-6: Parameters used for simplified Gummel Poon model

Parameter	Description	Value
C_{je}	Base-emitter zero bias depletion capacitor	0.04 pF
τ_f	Ideal transit time	10 ps
C_{jc}	Base-collector zero-bias depletion capacitance	0.5 fF
β	Forward gain	100

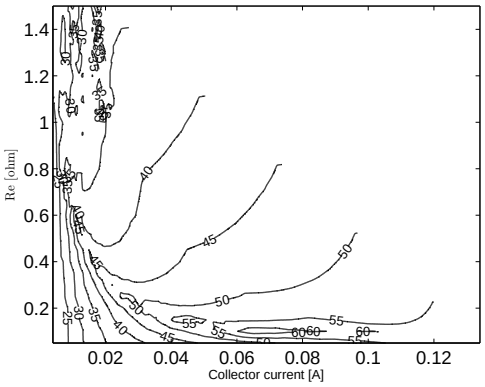
The OIP3 contours in dBm for input tone power of -30 dBm are shown in Figure 3-25 for all the



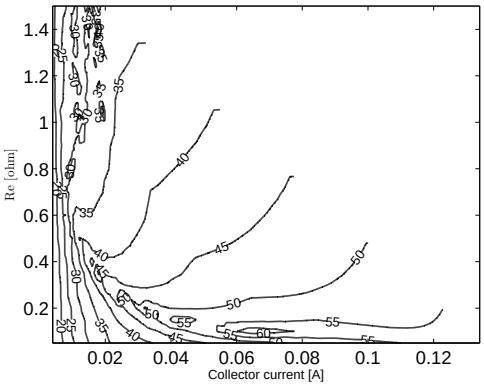
(a) OIP3 contour for differential CE stage with out-of-band emitter tuning



(b) OIP3 contour for differential cascode with out-of-band emitter tuning



(c) OIP3 contour for differential CE stage with feedback and out-of-band emitter tuning

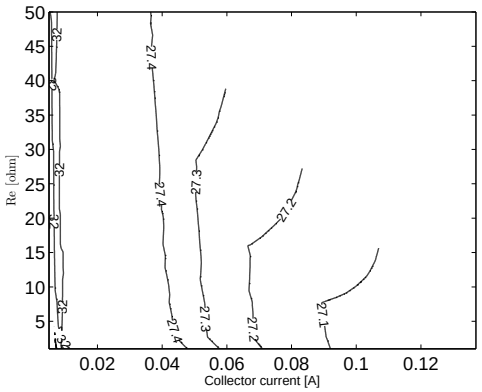


(d) OIP3 contour for cascode stage with feedback and out-of-band emitter tuning

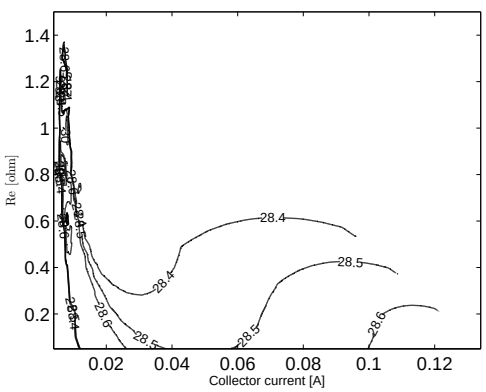
Figure 3-24: Contour out-of-band matching for emitter tuning, for ideal Gummel Poon model with C_{je} and τ_f

circuits of Figure 3-22. The figure shows OIP3 contour for a varying collector current and center tap resistor R_e. Due to the introduction of capacitance C_{jc} the OIP3 reduced to very low levels. The resistor R_e does no longer help in controlling the second order indirect mixing to improve linearity.

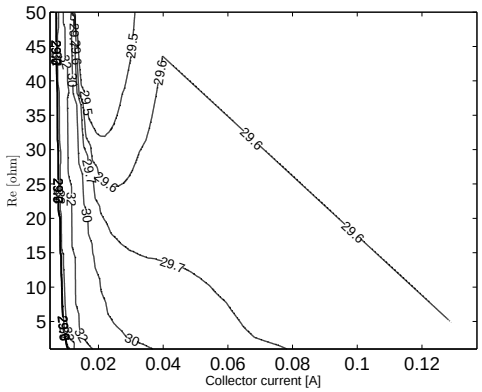
By applying feedback to differential CE stage, the achievable OIP3 (see Figure 3-25(c)) has increased compared to differential CE without feedback. In cascode case the effect of capacitor C_{jc} of common emitter stage is reduced. So achievable OIP3 in the case of differential cascode(see Figure 3-25(b)) has increased and also by applying feedback the linearity is has improved even for high currents(see Figure 3-25(d)).



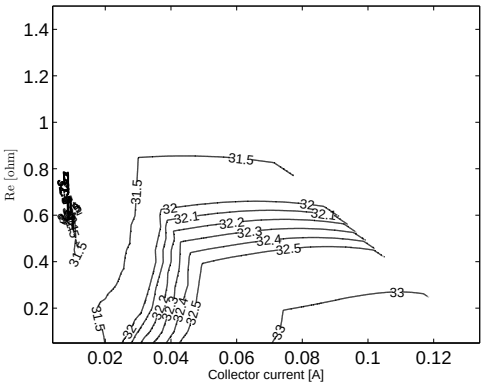
(a) OIP3 contour for differential CE stage with out-of-band emitter tuning



(b) OIP3 contour for differential cascode with out-of-band emitter tuning



(c) OIP3 contour for cascode stage with out-of-band emitter tuning



(d) OIP3 contour for differential CE stage with feedback and out-of-band emitter tuning

Figure 3-25: Contour out-of-band matching for emitter tuning, for ideal Gummel Poon model with C_{je}, τ_f and C_{jc}

3-6-3 Discussion

Table 3-7 and Table 3-8 shows the performance of out-of-band matching for improvement of linearity. The primary goal of these experiment was to determine the effect of each parasitic on linearity. From the tables it can be seen, that the major degradation on the linearity is due to C_{jc} capacitor. The effect of the feedback on out-of band matching can also be observed. From the table, it can be concluded that the base tuning provides higher linearity compared to the emitter tuning. In our experiment, the highest linearity is achieved when using the out-of-band base tuning for a differential cascode and differential CE stage with feedback when no base-collector capacitance is present.

Table 3-7: Performance for out of band base tuning for all the configurations using Gummel Poon model

	Base tuning					
	Ideal model		C_{je} and τ_f		C_{je},τ_f and C_{jc}	
	OIP3 [dBm]	Current [mA]	OIP3 [dBm]	Current [mA]	OIP3 [dBm]	Current [mA]
Diff. CE	60	70	70	70	27	70
Diff. CE with feedback	70	70	80	70	29	70
Diff. Cascode	60	70	70	70	32	70
Diff. Cascode with feedback	70	70	80	70	36	70

Table 3-8: Performance for out of band emitter tuning for all the configurations using Gummel Poon model

	Emitter tuning					
	Ideal model		C_{je} and τ_f		C_{je},τ_f and C_{jc}	
	OIP3 [dBm]	Current [mA]	OIP3 [dBm]	Current [mA]	OIP3 [dBm]	Current [mA]
Diff. CE	60	70	55	70	27	70
Diff. CE with feedback	70	70	60	70	29	70
Diff. Cascode	60	70	55	70	28.5	70
Diff. Cascode with feedback	70	70	60	70	32.5	70

3-7 Conclusion

In this chapter, the dominant sources of IM3 distortion were identified. Next, the techniques that can be used to reduce the impact of these non-linearities are discussed. The limitation and the techniques that will be used for achieving a high output compression point has been discussed. It shows that a use of a differential topology allows better control of the even order distortion component. As such a more orthogonal design procedure for improving the linearity can be used. In addition the use of differential topology proves beneficial topology for the linearity enhancement. This technique has been applied to a practical circuit using a Gummel Poon model

for the active device. From the results, it can be concluded that the base collector capacitance is the major constrain in achieving high linearity

Chapter 4

A two stage low noise and highly linear LNA

4-1 Introduction

In a two stage design, the input stage should have low noise, high gain, and low return loss while the output stage should have high linearity and high compression point. In this chapter the implementation details of both the input and output stages designed in this work are presented. The linearity and compression point enhancement techniques discussed in chapter 3 are employed and the schematic level simulation results are presented.

The design and implementations of the input stage is discussed in Section 4-2. In next Section 4-3, two differential implementation of the output stage using linearity enhancement technique are presented. In last Section 4-4, both the input stage and the output stage are combined to form a complete two stage LNA .

4-2 Input stage

As discussed in Chapter 2, the input stage of the LNA is targeted for high gain, low noise and linearity requirements. The high gain is achieved by using a cascade of CE-CB stage, which is normally referred as cascode. This also improves reverse isolation. A low noise figure is achieved by selecting proper transistor biasing and noise matching. The linearity is improved to some extent by using inductive degeneration. The other important requirement is low return loss, because the duplexer filter preceding the LNA is sensitive to load matching. The filter between antenna and LNA is designed as high frequency device with a load termination of 50 Ω. If the load termination deviates from 50 Ω, the filter may have losses and show ripple effect

in passband and stopband [31]. Hence, the LNA needs to be impedance matched to 50 Ω. To have low noise figure and low return loss, the input stage of 2 stage LNA should be noise and impedance matched simultaneously. The matching is usually done using passive elements, as they are less noisy compared to active elements. The passive elements matches impedance only over a band of frequency.

4-2-1 Input impedance and noise matching

The dominant noise sources in bipolar transistor are shot noise related to current of i_b, i_c and thermal noise of r_b, r_E and, r_C. In a cascode, the first stage (CE stage) dominates the overall noise performance. The noise added by CB stage in cascode is small compared to common emitter stage [32]. The minimum noise figure for common emitter stage of NPN transistor can be written as [33],

$$NF_{min} = 1 + \frac{1}{\beta}\sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + (\frac{f}{f_T})^2} \tag{4-1}$$

The above equation shows that the low noise figure can be achieved by using a device with high cut-off frequency f_t, high current gain β, and large area device to reduce the base resistance r_b. The minimum noise achievable in QUBiC4Xi technology is 0.3 dB @ 2 GHz. The Figure 4-1 shows the noise performance of minimum sized BNY transistor. The current gain (β) of this technology is 2000, which basically eliminates the base shot noise i_b. The f_t of the device is 194 GHz which also helps to achieve a low noise figure. The input stage is implemented using BNY HV transistor in 0.25 μm BiCMOS SiGe QUBiC4Xi technology.

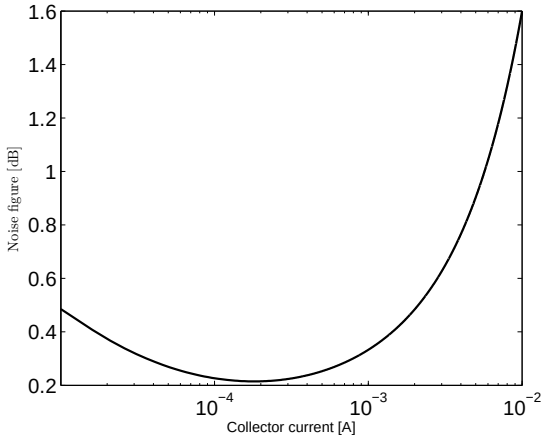


Figure 4-1: Noise figure @ 2 GHz simulated versus I_C, for size:0.3 μm x 1 μm x 1 QUBiC4Xi SiGe BNY BJT

The input stage is noise and impedance matched to achieve low return loss and noise figure. The input impedance and related S_{opt} of the minimum sized transistor are high. Hence, multiple

parallel device are used to reduce the input impedance of the first stage. The most common method used to match both noise and input simultaneously is to use inductor at both emitter and base of CE stage [34]. The series resistive loss of both inductors will limit the noise performance of LNA. A degeneration inductor at emitter serves two purposes, it increases the input impedance and improves linearity, hence it is a must use. The disadvantage of using a degenerative inductor is it degrades the NF. To replace an inductor at base, a shunt capacitive feedback along with degenerative inductor is used for impedance and noise matching simultaneously [32].

The schematic of the input stage is shown in Figure 4-2, where C_f is shunt feedback capacitor, C_{zero} capacitor is used to improve the stability of the CB stage in cascode, R_{stab} is used to improve the stability of first stage at low frequencies. The C_{zero} is also required, because without this capacitor, the CB-stage does not work as a CB-stage. The base of the CB-stage should be connected low-ohmic to ground, which is done by the C_{zero}. A balun is used at the output of the first stage to convert from single-ended to differential in order to feed the differential output stage. The input matching (Z_{in}) is controlled by the shunt feedback capacitor, the inductor L_e and to some extent the loading impedance Z_L.

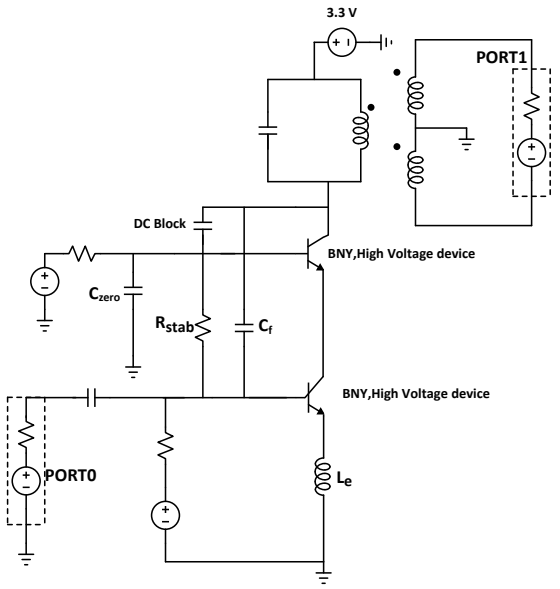


Figure 4-2: Input stage

The technique followed for input and noise matching (shown in Figure 4-3) are as follows,

* For a minimum sized transistor, (size:0.4 μm x 10.3 μm x 2), the input impedance is 14.4-j402.5 and Z_{opt} is 388+j340.25. By increasing the emitter area by 8 to 9 times the S_{opt} is placed on unit circle of the Smith chart. While increasing the size of the device, the current density is kept constant for minimum noise figure.

* From the Smith chart it can be seen that, the input impedance is capacitive. An inductive impedance can be used at the emitter terminal to increase the input impedance. The input impedance is given by,

$$Z_{in} = \frac{-j}{\omega C_\pi} + j\omega Le + \frac{g_m L_e}{C_\pi} \tag{4-2}$$

The real part of input impedance must be made equal to,

$$\frac{g_m L_e}{C_\pi} = R_s \tag{4-3}$$

$$L_e = \frac{R_s C_\pi}{g_m} = \frac{R_s}{\omega_T} \tag{4-4}$$

where $\omega_T = 2 * \pi * f_t$ is the operating frequency of the device, R_s is the source impedance. The value of inductance used for input matching is 0.35 nH. By use of degeneration inductor gets Z_{opt} a bit closer to 50 Ω.

* From the Smith chart, the input impedance is way off from 50 Ω, so an additional network is needed to achieve input match. An additional shunt capacitor is used for input matching. The shunt capacitor and load impedance do not impact the noise performance.

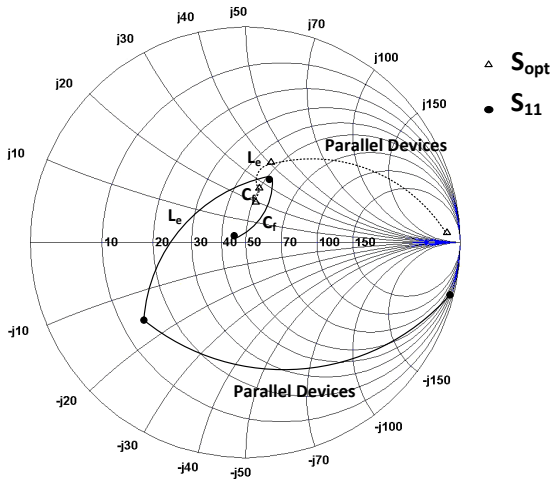
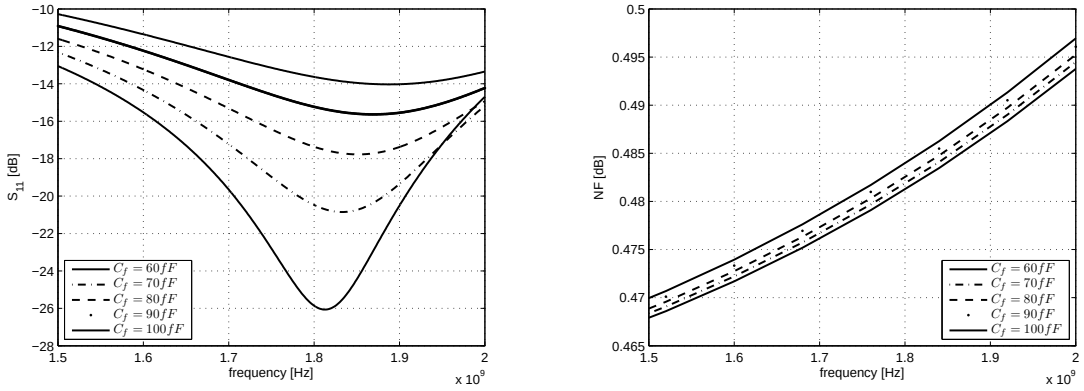


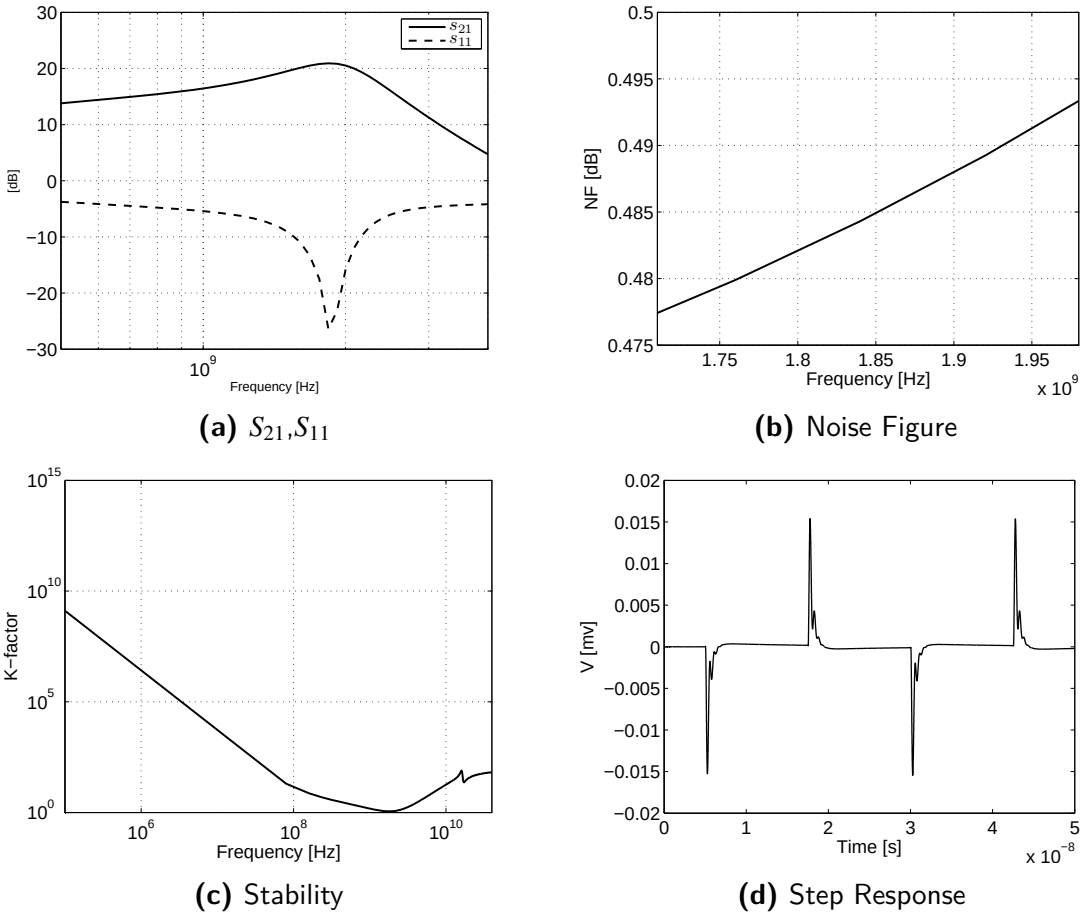
Figure 4-3: Input matching and noise matching

Figure 4-4 shows, the change in input matching (S_{11}) and noise figure due to the shunt feedback C_f. A C_f of 60 fF provides a good input matching in the desired frequency range (see Figure 4-4(a)). The shunt feedback does not have much impact on the NF (see Figure 4-4(b)). Thus, the shunt feedback helps in input matching without affecting the noise figure. As discussed in chapter 3, the degenerative inductor improves linearity.



(a) S_{11} **(b)** Noise Figure

Figure 4-4: The variation of S_{11} and noise figure by C_f

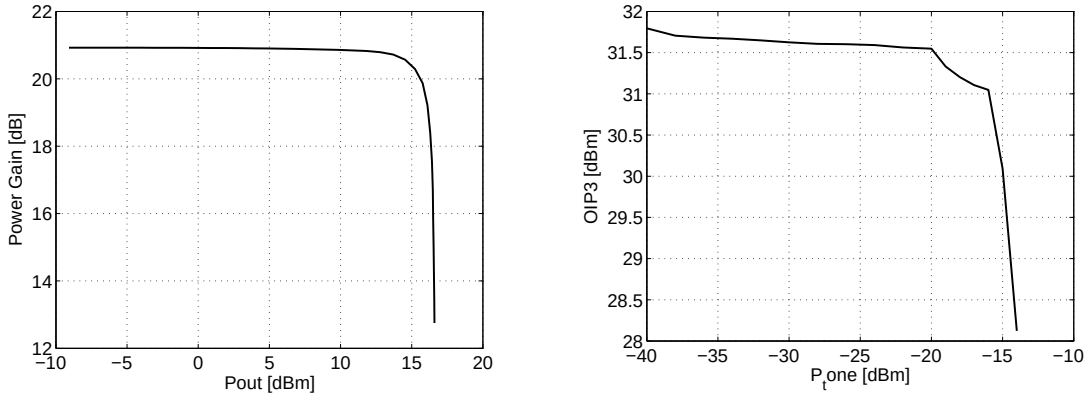


(a) S_{21},S_{11} **(b)** Noise Figure

(c) Stability **(d)** Step Response

Figure 4-5: Simulation results of input stage

The simulation results after applying the simultaneous noise and impedance matching are shown in Figure 4-5. The target specification for gain: s_{21} of 20 dB, s_{11} of -20 dB, NF of 0.49 dB are achieved in desired range of frequency. The stability factor k is larger than 1 for a wide frequency range from DC up to 40 GHz. The step response analysis is also done to demonstrate the stability, from the step response one can say the system is critically damped. The output compression point was simulated for 1 tone @ 1.84 GHz. Figure 4-6(a) shows the output power as a function of power gain. The output compression achieved is 15 dBm. For the OIP3, a 2 tone test simulation with beat frequency of 10 MHz is performed. From Figure 4-12(b), the maximum achievable OIP3 is 31 dBm up to an input tone power -15 dBm.



(a) Power Gain Vs P_{out} **(b)** OIP3 Vs P_{tone}

Figure 4-6: Compression point and linearity performance of the input stage

4-3 Output stage

The main target of the output stage are high linearity and a high output compression point. The differential configuration helps in controlling the fundamental and second harmonic impedance independently. Hence, a differential push-pull topology is used for the implementation of the output stage to achieve high linearity. A center-tapped transformer is used for impedance transformation, which helps in achieving high 1 dB compression point. It also helps in conversion from single ended to differential and vice-versa. These transformers are useful in implementing the input and output matching.

The primary coil of the balun is single ended, where as the secondary coil is differential with a center tap. In an ideal case, the center tap is connected to ground, the common mode signal in differential configuration only experience the impedance connected to the center tap of balun. As the center tap is connected to ground, impedance seen is a short. In a practical implementation balun are imperfect, since the coupling factor is less than 1 (K<1). The common mode signal now sees a finite inductance, which is not a short. To overcome this problem a capacitor is connected at the center tap of the balun to tune out the inductance of the secondary coil by series

resonance. The non-ideal coupling will also impact the differential operation as such requiring a parallel capacitance to enhance the power transfer in the desired frequency band.

The setup for common mode is shown in Figure 4-7. The capacitor C_2 is connected to the center tap of the balun, capacitor C_1 is used to tuned to enhance the energy transfer at the operating frequency. The capacitor C_2 is used to remove the imbalance in the impedance at second harmonic. By changing the center tap capacitor C_2, the impedance offered to common mode component changes as shown in Figure 4-8. As the value of capacitor C_2 is increased, a series resonance is enforced moving the effective impedance towards a perfect short.

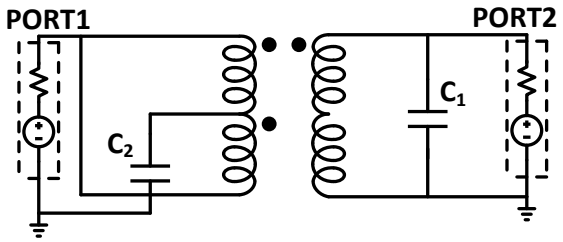


Figure 4-7: Common mode test

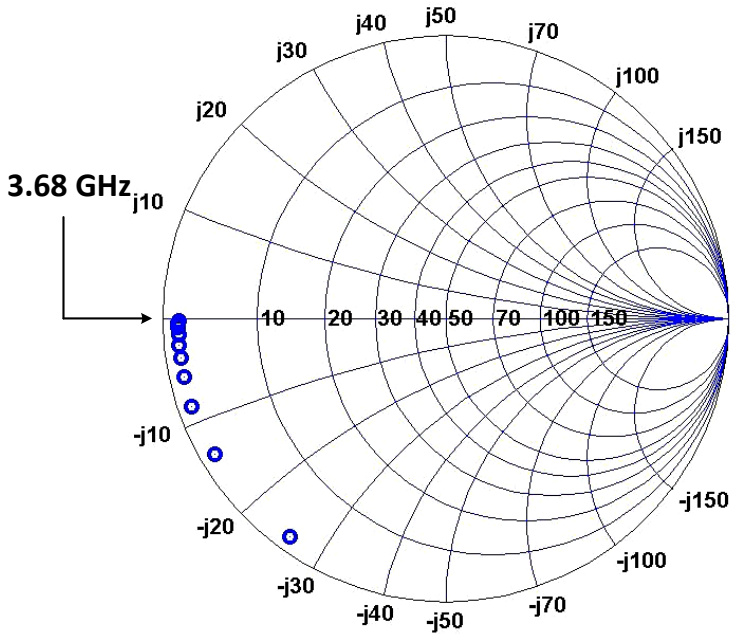


Figure 4-8: Impedance at 2^{nd} harmonic due to centertap capacitor C_2

The output stage is biased at higher current levels, to achieve high linearity and OP1dB compression point. Here a BNA transistor is used since it allows a maximum output voltage swing of 2.5 V. The use of cascode increases the effective output impedance and the gain. It was also expected that the cascode would provide better linearity since the non-linear feedback through the C_{jc} capacitance is reduces in this configuration. In addition resistive shunt feedback is used to improve linearity. Two output stages are discussed differential cascode stage and differential CE stage. In both the architectures, the common mode at input and output balun is almost set to a perfect short using a centertap capacitor.

4-3-1 Differential cascode stage

The linearity enhancement technique used in this architecture are implicit IM3 cancellation technique, overall feedback and the application of a 2^{nd} harmonic short. The schematic of the inductively degenerated differential cascode with overall shunt resistive feedback is shown in Figure 4-9. An inductive degeneration is provided through L_e for implicit IM3 cancellation, the overall feedback is achieved by $R_{feedback}$ and the frequency compensation is done by capacitor C_{ph}. Two baluns are used, one at the input and one at the output. The second harmonic short is provided at the centertap of balun at both input and output using $C_{centertap1}$ and $C_{centertap2}$ respectively, C_{zero} is used to provide stability for cascode configuration. By using a balun, the impedance level is adjusted, to achieve a high compression point. The differential cascode is expected to be beneficial in achieving high linearity. The out-of-band linearization technique was applied on the differential cascode, but there was no linearity improvement.

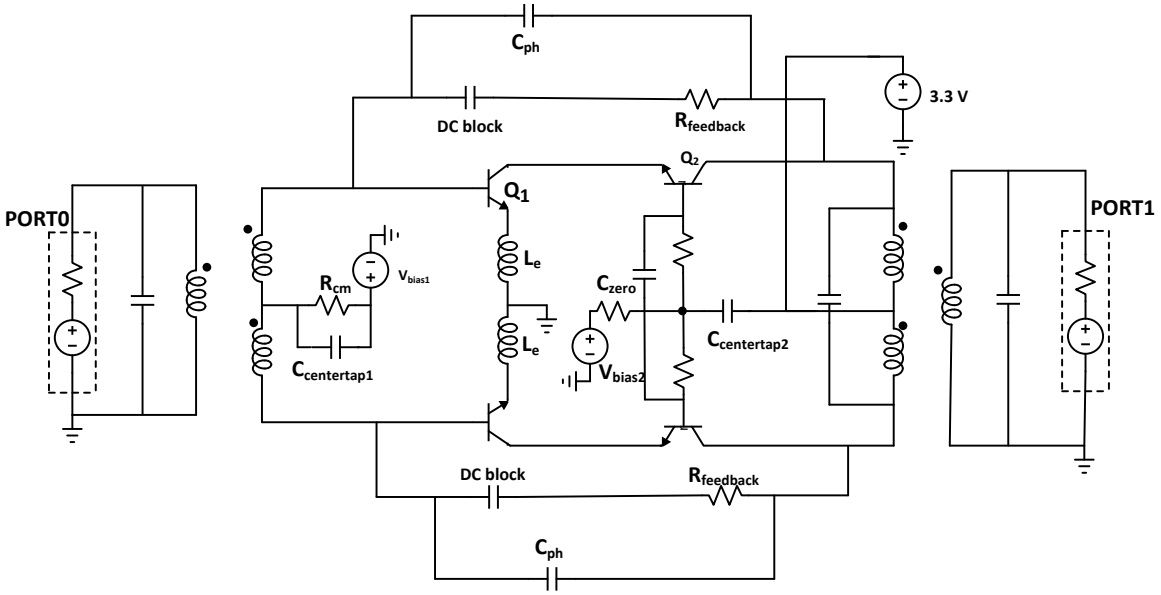
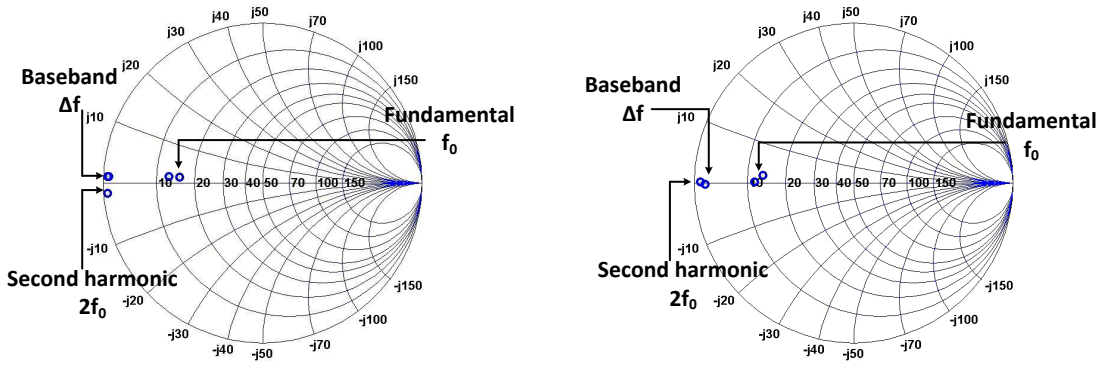


Figure 4-9: Differential Cascode stage

The cascode provides a high loop gain and also provides good isolation from output to input. The reason for achieving high gain at high frequency is, the reduced Miller effect $C_{\mu 1}$. The disadvantage of using cascode is it requires a high supply to bias $Q1$ and $Q2$ sufficiently. The RF signal is provided at the base of the CE stage. These stages act as transconductance, converting the voltage input to current output. The unity current gain of the common base stage delivers the output current to the load.

At lower current, when exponential distortion is considered to be dominant, the nonlinearities will be introduced by CE stages, whereas CB stage behaves almost linearly. The CB stage of cascode the base to collector capacitor C_{jc} is shunted between the output and ground, and does not act as a nonlinear feedback element. The linearity improvement by using degenerative inductance. In the cascode configuration, the voltage gain of the CE stage is low as the input impedance of the CB is low$(1/g_{m2})$. As voltage gain of CE stage is low, the voltage variation across the feedback base collector capacitor C_{jc} is low ,thus improving the linearity. In cascode, CB stage is the output stage. To deliver higher output power, collector to emitter voltage V_{CE} across CB stage is maintained at ≈2.5 V.

The impedance seen by the base of transistor Q_1 and collector of transistor Q_2 towards the input balun and the output balun at baseband, second harmonic and fundamental frequencies are shown in Figure 4-10. At the input and the output balun, the impedance seen at baseband and second harmonic frequencies is a perfect short. The $C_{centertap1}$ and $C_{centertap2}$ at center tap of both input and output balun, respectively help provide a short. The impedance at fundamental frequency at input balun is $\approx 13\ \Omega$. It can be seen that the impedance at fundamental frequency is $\approx 10-12\ \Omega$ for output balun, which helps to meet the output compression point requirement. The mismatch in the fundamental frequency at both input and output, is due to unbalanced capacitive loading between the primary and secondary coils.



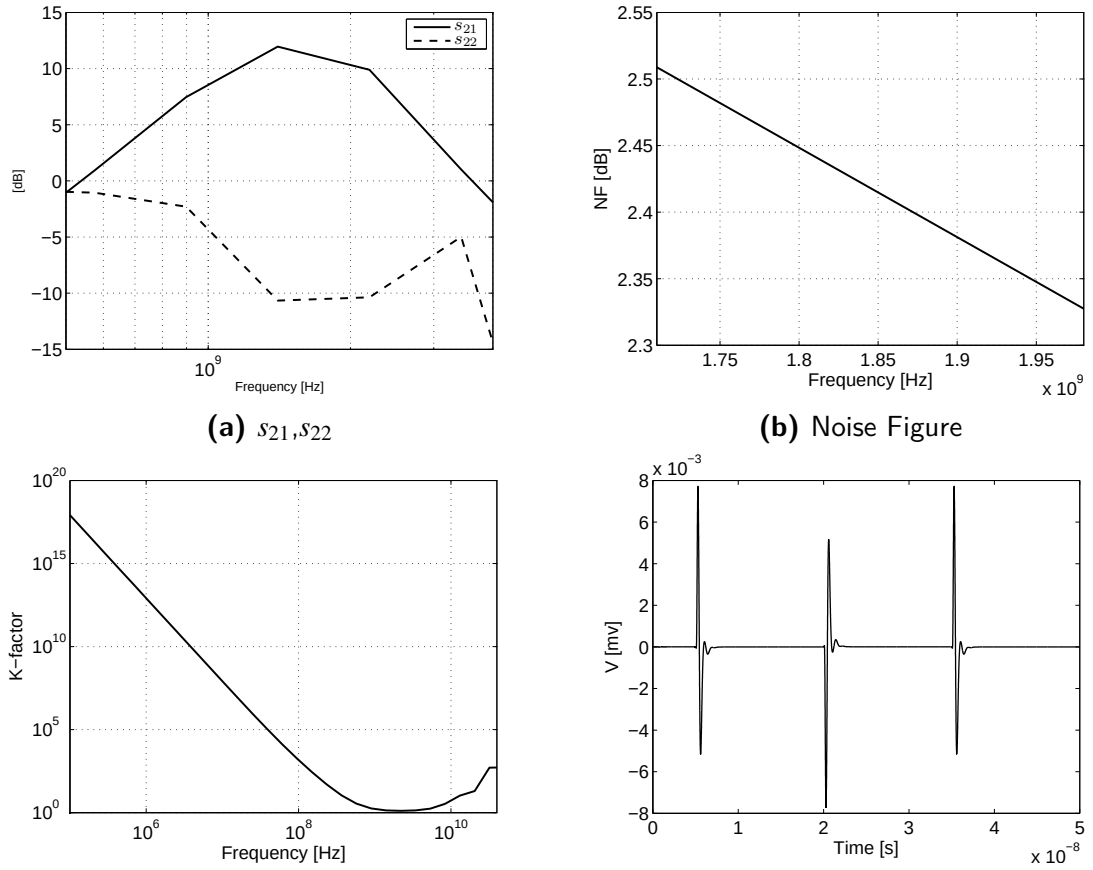
(a) Impedance at input balun **(b)** Impedance at output balun

Figure 4-10: Impedance at baseband, fundamental and second harmonic

The balun used at input and output has turns ratio of 3:2. The turns ratio is 1.5, which helps in impedance transformation and output matching. The swing provided by the output stage CB

of cascode is 2.5 V and the load seen by the transistor is ≈10-12 Ω. For this combination, the output compression point is 24 dBm.

The value of inductance used for improvement of linearity is L_e of 0.35 nH, and collector current of 80 mA in each branch of differential pair and emitter length A_e of both the CE and CB stages are chosen to be same, the size of transistor is 0.4 μm x 20.7 μm x 24. The supply voltage used for biasing cascode is 3.3 V, it is provided at the center tap of the output balun. The biasing for the transistor Q_1 is provided at the center tap of input balun. The size of transistor is chosen to carry high current and to operate at high f_t to get maximum gain, high linearity and high compression point. The feedback resistor $R_{feedback}$ is selected to provide a gain of 10 dB. The centertap capacitance $C_{centertap1}$ and $C_{centertap2}$ are tuned as shown in section 4-3 to achieve second harmonic short.



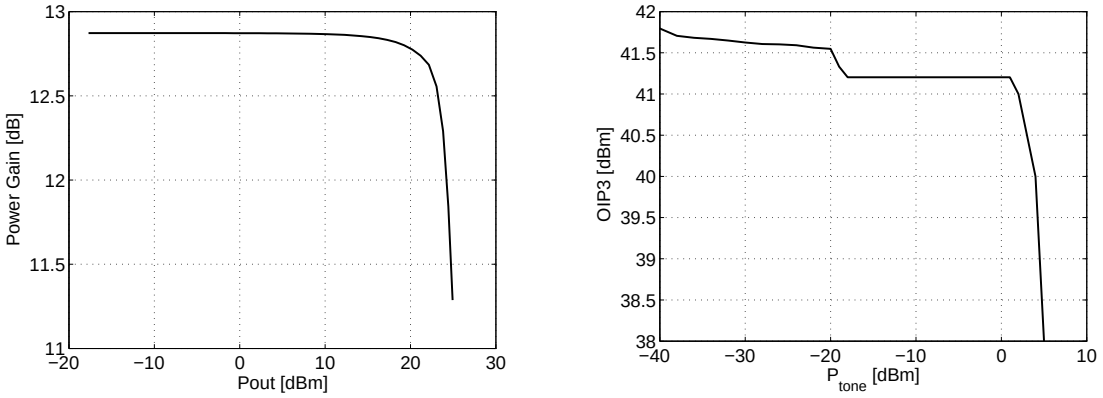
(a) s_{21},s_{22} **(b)** Noise Figure

(c) Stability factor **(d)** Step Response

Figure 4-11: Simulation results of differential cascode stage

The simulation results of differential cascode are shown in Figure 4-11. The gain S_{21} of 10 dB and S_{22} of -10 dB are achieved in desired range of frequency. The noise figure of the output stage is 2.5 dB, which is well below the specification derived for the output stage. The stability factor,

k is greater than 1 for a wide range of frequency from DC to 40 GHz. The step response analysis is also done to show the stability and it can be inferred that the system is critically damped. The output compression point was simulated for 1 tone @ 1.84 GHz. Figure 4-12(a) shows the output power vs the power gain, the output compression achieved is 24 dBm. For the OIP3 test, a 2 tone simulation with beat frequency of 10 MHz is done. From Figure 4-12(b) , the maximum achievable OIP3 is 41 dBm up to input power tone of 4 dBm.



(a) Power Gain vs. P_{out} **(b)** OIP3 vs. P_{tone}

Figure 4-12: Compression Point and Linearity performance of differential cascode

4-3-2 Differential CE stage

The linearity improvement technique used for differential CE stage architectures are implicit IM3 cancellation, overall feedback, 2^{nd} harmonic short, out-of-band matching base tuning. The inductive degeneration, differential CE with overall shunt resistive feedback is as shown in Figure 4-13. The inductive degeneration is given through L_e, the overall feedback is given by $R_{feedback}$. Baluns are used at input and output nodes. The second harmonic short is provided through centertap of the balun at both input and output using $C_{centertap1}$ and $C_{centertap2}$, respectively. The centertap resistance R_{cm} is used for out-of-band matching base tuning at the base terminal.

The gain needed by the output stage is around 10 dB, which can be provided by the CE stage. But at high frequencies the loop gain of CE stage is limited by the base to collector capacitor. The gain of the CE stage with degeneration inductor can be approximated by,

$$A_v = \frac{g_m Z_L @ (1.84GHz)}{1 + g_m Z_E @ (1.84GHZ)} \tag{4-5}$$

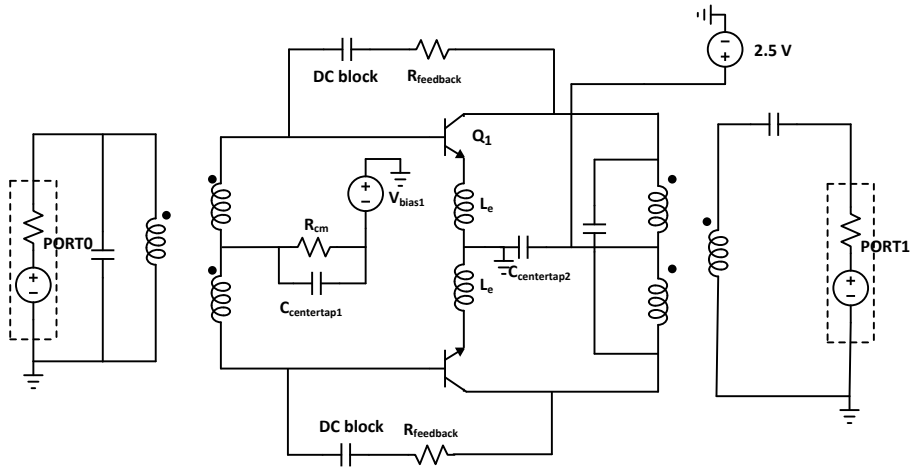


Figure 4-13: Differential CE stage

From the Eq. (4-5), increasing the value of Z_E to improve the linearity, will limit the gain of the differential CE stage. A trade-off is considered between the linearity and gain. One of the techniques which does not compromise for gain is out-of-band matching as discussed in section 3-4-2. It was earlier concluded in Chapter 3 that for differential structure out-of-band base tuning is more effective than emitter tuning. Out-of-band matching base tuning is provided at the centertap of the input balun through resistor R_{cm}.

The variation in OIP3, by changing the value of centertap resistance R_{cm} is shown in Figure 4-14. From this simulation, out-of-band cancellation occurs at R_{cm} 38 Ω . The maximum OIP3 achieved is 46 dBm.

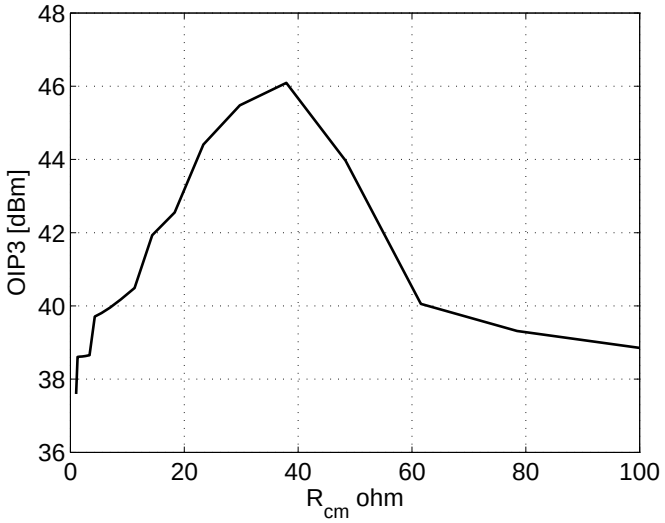
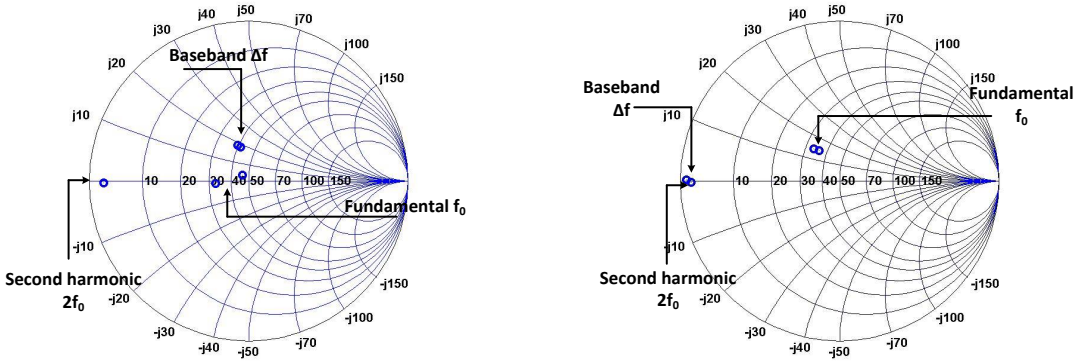


Figure 4-14: OIP3 variation



(a) Impedance at input balun **(b)** Impedance at output balun

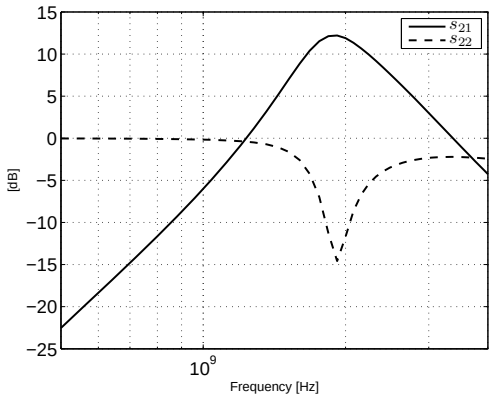
Figure 4-15: Impedance at baseband, fundamental and second harmonic

The impedance seen by the transistor Q_1 towards the input and the output balun at baseband, second harmonic and fundamental frequencies are shown in Figure 4-15. At the input balun the impedance at baseband is around 40 Ω, which is provided by the centertap resistor R_{cm}. The 2^{nd} harmonic termination is provided at both input and output for improved linearity. The second harmonic short is provided by capacitor $C_{centertap1}$ and $C_{centertap1}$ at centertap of the input and output balun, respectively. At the output balun, impedance seen by baseband and second harmonic is close to perfect short. The impedance at fundamental frequency shows some mismatch, which is due to unbalanced capacitive loading between the single-end driver primary and differential operated secondary coil. At fundamental frequency, the impedance is around 35 Ω.

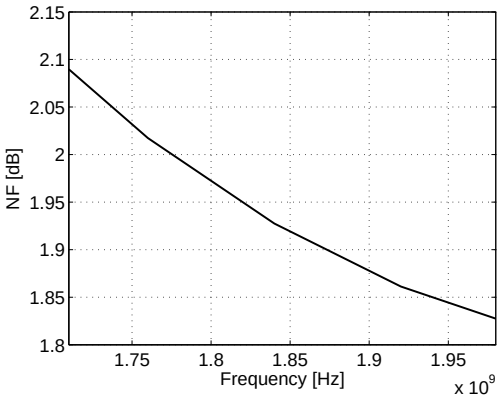
The value of inductance used for improvement of linearity is L_e of 0.5 nH, and collector current of 60 mA in each branch of differential pair and emitter length A_e of the CE, the size of transistor is 0.4 μm x 20.7 μm x 24. The supply voltage used for biasing is 2.5 V, it is provided at the center tap of the output balun. The biasing for the transistor Q_1 is provided at the center tap of input balun.

The simulation results of differential CE stage is shown in Figure 4-16. The gain s_{21} of 10 dB and s_{22} of -10 dB is achieved in desired range of frequency. The noise figure of the output stage is 2.5 dB, which is well below the specification derived for output stage. The stability factor, k>1 for a wide range of frequency from low frequency to 40 GHz. The step response analysis is also done to show the stability, it can be said the system is critically damped.

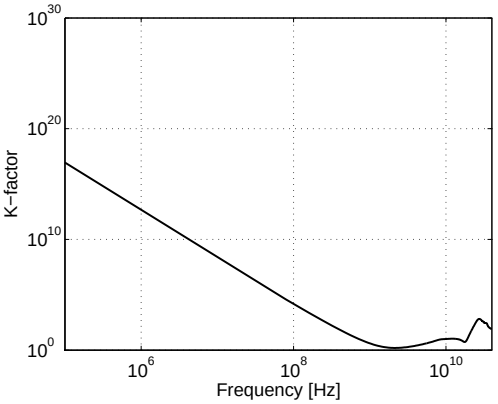
The output compression point was simulated for 1 tone @ 1.84 GHz. Figure 4-17(a) shows the output power vs. the power gain, the output compression achieved is 21 dBm. For an OIP3 test a 2 tone simulation with beat frequency of 10 MHz is done. From Figure 4-17(b), the maximum achievable OIP3 is 45.5 dBm till input power tone of -4 dBm.



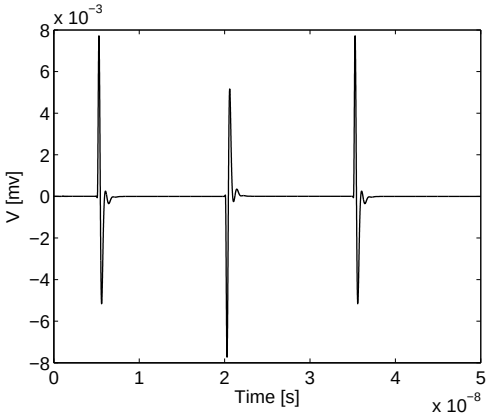
(a) s_{21},s_{22}



(b) Noise Figure

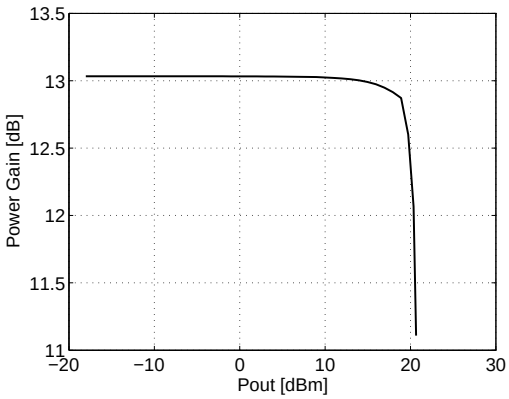


(c) Stability

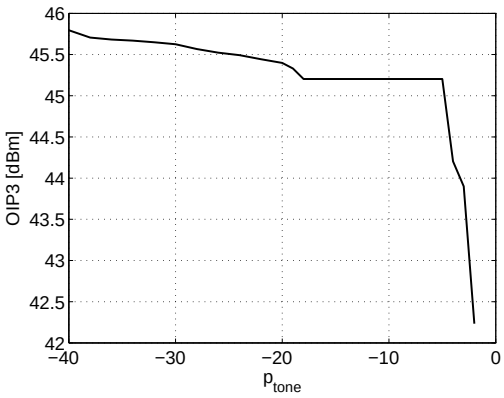


(d) Step Response

Figure 4-16: Simulation results of differential CE stage



(a) Power Gain vs. P_{out}



(b) OIP3 vs. P_{tone}

Figure 4-17: Compression Point and Linearity performance of differential cascode

4-4 First and second stage combined

The input stage discussed in section 4-2 and output stages discussed in section 4-3 are combined to form a 2 stage LNA. Two combinations of the combined circuits are discussed, one with a differential cascode output stage and the other one with the differential CE output stage.

4-4-1 LNA with differential cascode output stage

The schematic of the LNA with differential cascode output stage is shown in Figure 4-18. The use of degeneration increases the input and output impedance. In a cascode stage, CE stage acts as a degeneration for CB stage. The CE stage operates as a small-signal resistance equal to r_o. So use of cascode also increases the output impedance. The input impedance of the output stage is lower as multiple devices are in parallel to carry high current. For maximum power transfer, interstage matching has to done between the first stage and second stage. For inter stage matching a balun with turns ratio 3:2 is used. As the turns ratio is 1.5, the impedance from the first stage is down converted to establish a interstage matching. The connecting balun acts as even order filter. The even harmonics generated from the first stage are filtered. This helps in improving the linearity and compression point.

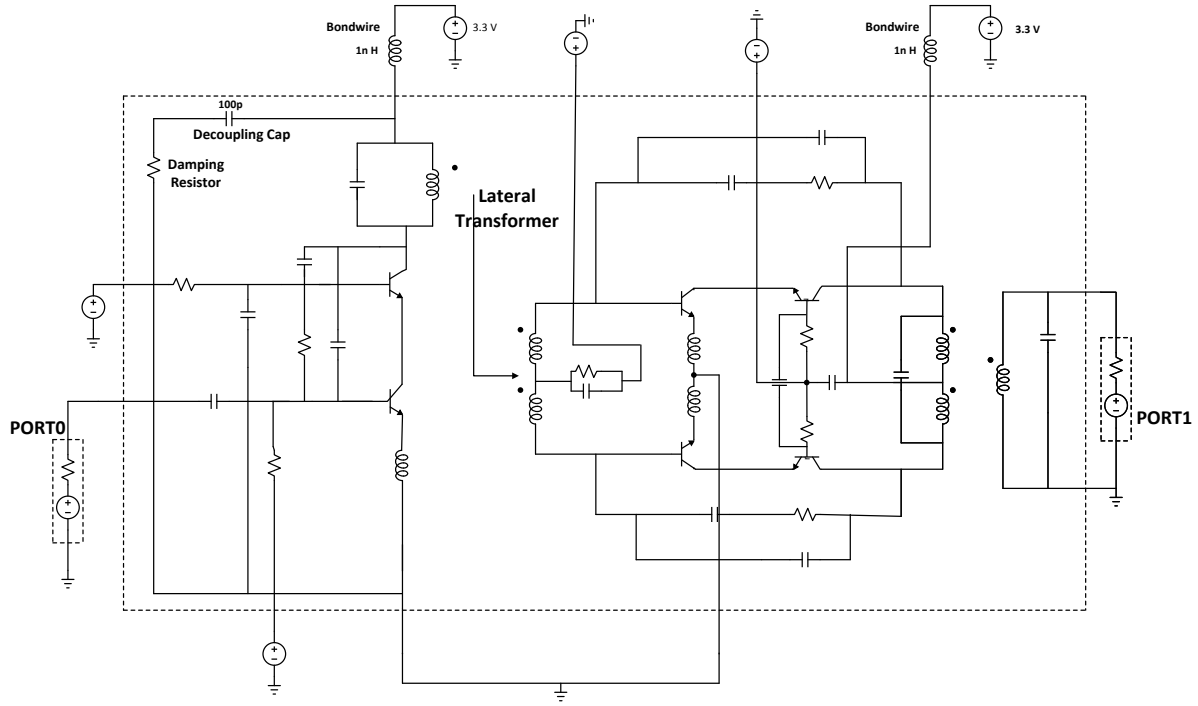
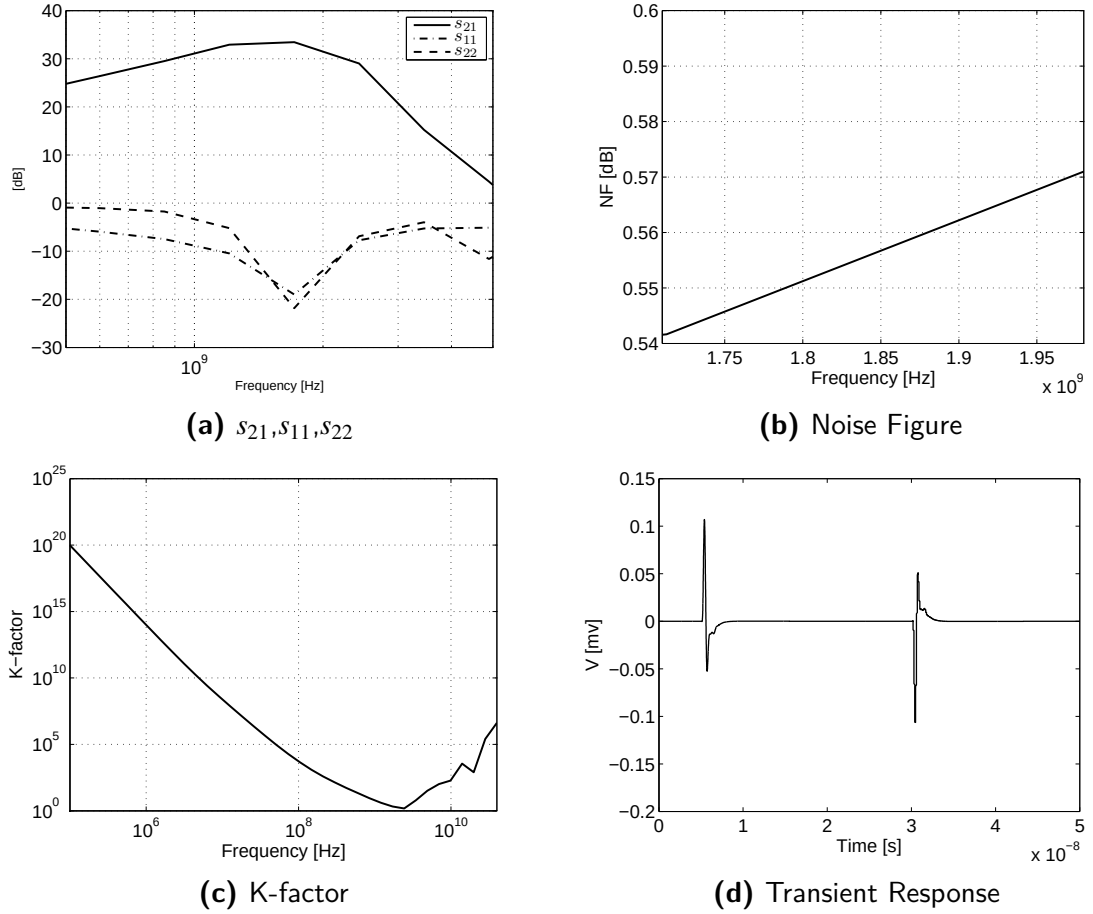


Figure 4-18: LNA with differential Cascode stage

The circuit is designed to include the effect of the supply line impedance. To reduce the effect of

supply impedance decoupling is used, which includes capacitors and a damping resistors. The decoupling capacitor is used to provide a low resistance path to the ground. The damping resistor is used to damp the coupling of decoupling capacitor with the supply impedance to make it free of resonant peaks, that might disturb the operation of LNA. The decoupling circuit is used only for the input stage and not been used for at output stage, due to its differential nature of operation.



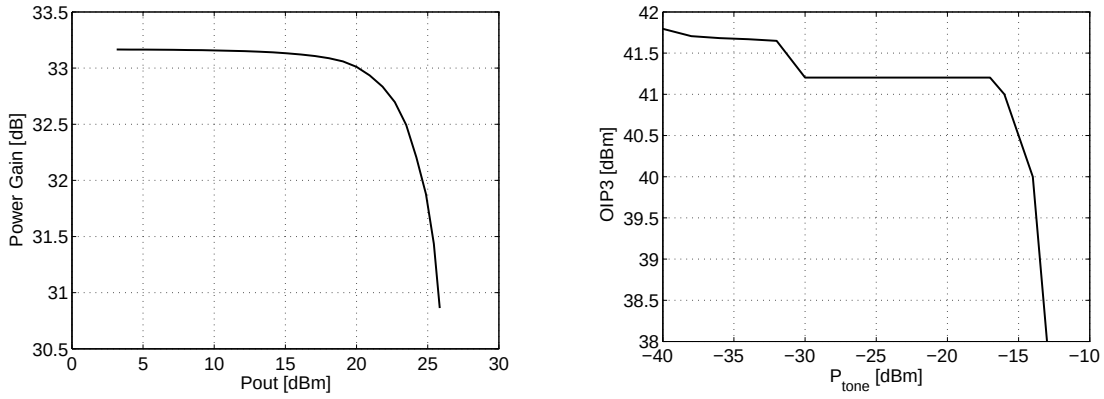
(a) s_{21},s_{11},s_{22} **(b)** Noise Figure

(c) K-factor **(d)** Transient Response

Figure 4-19: Simulation results of LNA with differential cascode stage

The simulation results of overall LNA featuring a differential cascode output stage is as shown in Figure 4-19. The gain is S_{21} of 32 dB, while as S_{11} of -20 dB and S_{22} of -20 dB is achieved in desired range of frequency. The overall noise figure of the LNA is 0.56 dB. The stability factor, k proves to be larger than 1, from DC to 40 GHz. The step response analysis is also done to show the stability, it can be said the system is critically damped.

The output compression point was simulated for 1 tone @1.84 GHz. Figure 4-20(a) shows the power gain vs. output power, the output compression achieved is 24 dBm. For OIP3 testing a 2 tone simulation with beat frequency of 10 MHz is performed. From Figure 4-20(b) , the maximum achievable OIP3 is +41 dBm till input power tone of -14 dBm.



(a) Power Gain vs. P_{out} **(b)** OIP3 vs. P_{tone}

Figure 4-20: Compression Point and Linearity performance of LNA with differential cascode

In order to understand the effect of process and mismatch variations on the linearity (OIP3) a Monte Carlo simulation is done. The studying the impact of process variation helps us to analyze the variation on the expects performance parameters. The Monte Carlo simulation is done for N=500 points. The results of the Monte Carlo simulation are shown in Figure 4-21, where x-axis represents OIP3 in dBm and y-axis represents the number of test points. From the simulation results, the mean is around OIP3 is 40.7 dBm, which is equal to original specification. The range of variation of OIP3 is 41.5 dBm to 39.5 dBm respectively.

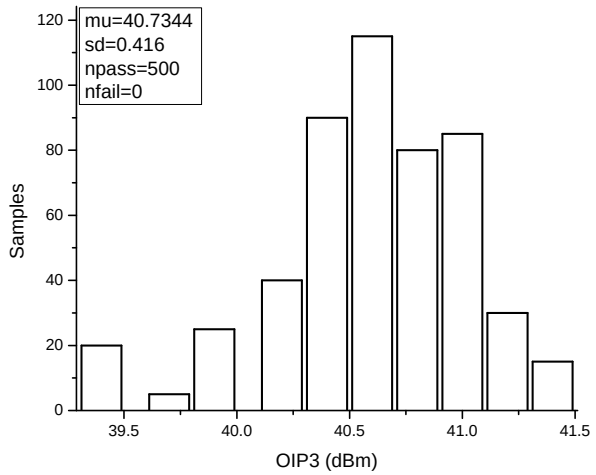


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Figure 4-21: Monte Carlo simulation of schematic for LNA with differential cascode stage

4-4-2 LNA with differential CE stage output stage

The implementation of the LNA with differential CE output stage is shown in Figure 4-22. As in the case of LNA with differential cascode, a balun with 3:2 turns ratio is used for interstage matching. The decoupling circuit is added to decouple the circuit core from supply impedance.

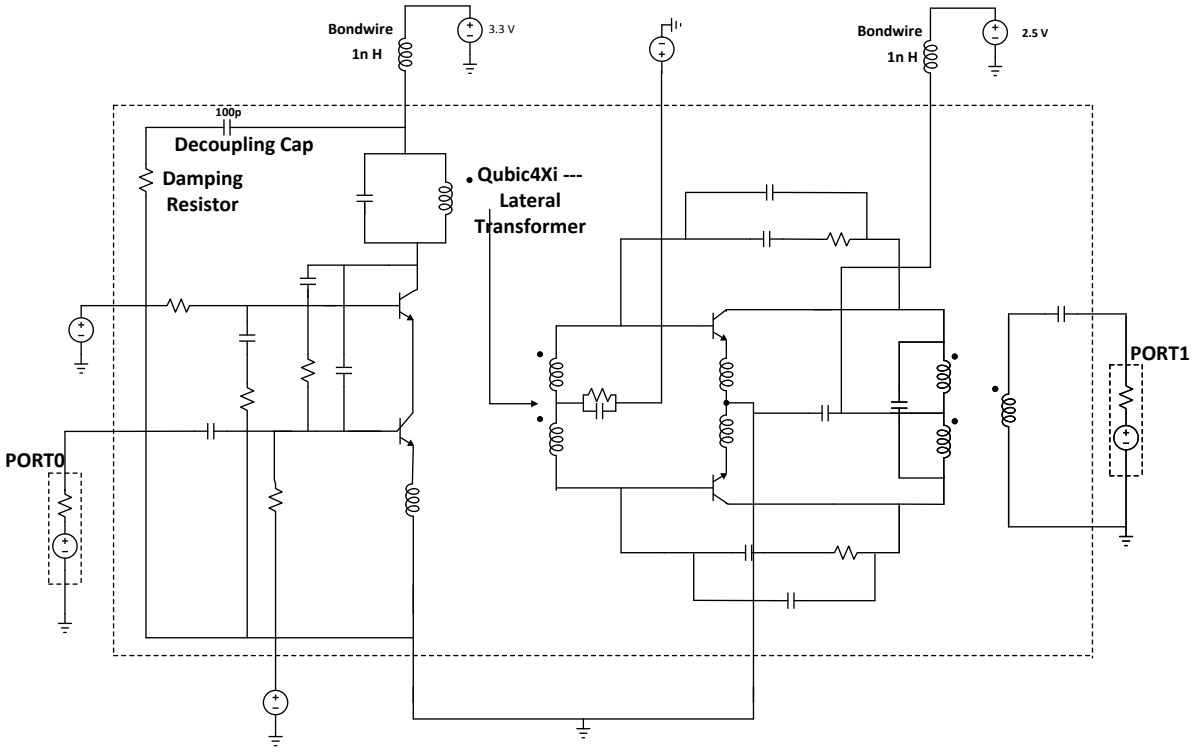
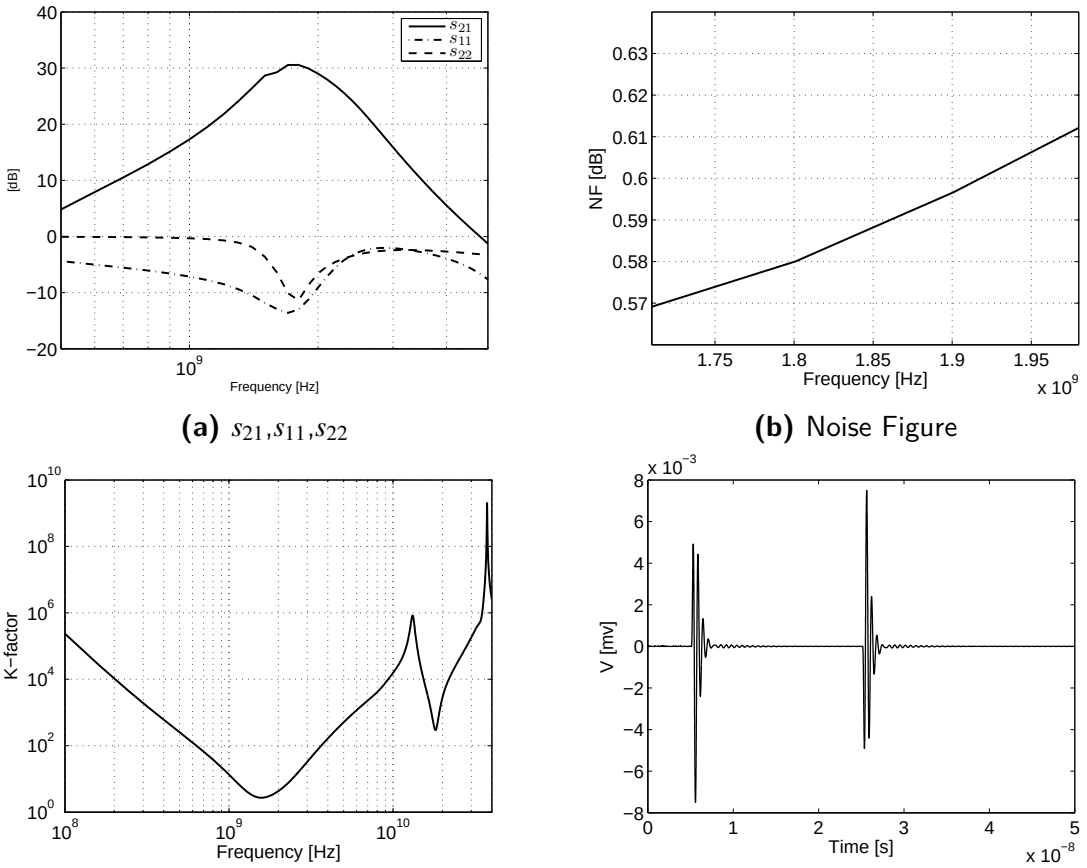


Figure 4-22: LNA with differential CE stage

The simulation results of the LNA with differential CE stage is shown in Figure 4-23. The gain S_{21} of 30 dB, S_{11} of -15 dB and S_{22} of -10 dB is achieved in desired range of frequency. The overall noise figure of the system is 0.59 dB. The stability factor, k>1 for a wide range of frequency from low frequency to 40 GHz. The step response analysis is also done to show the stability, it can be said the system is critically damped.

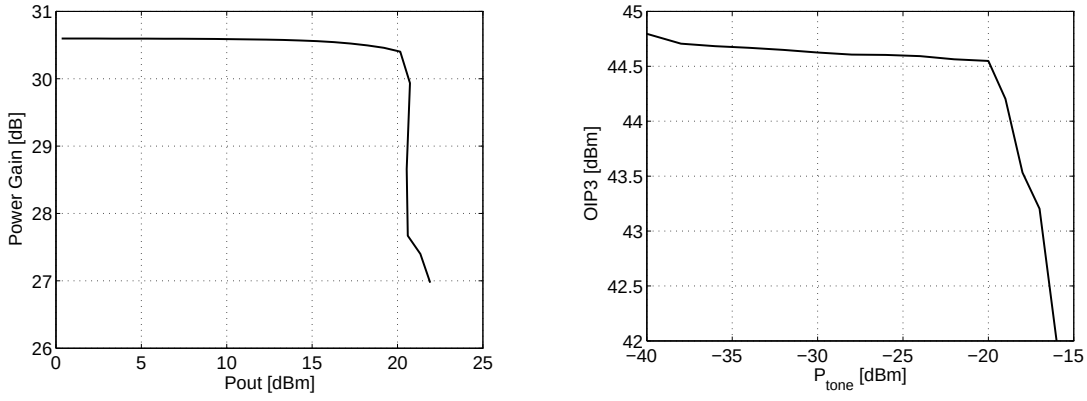
The output compression point was simulated for 1 tone @ 1.84 GHz. Figure 4-24(a) shows the power gain vs. output power, the output compression achieved is 21 dBm. For an OIP3 test a 2-tone simulation with a beat frequency of 10 MHz is performed. From Figure 4-24(b) , it can be concluded the maximum achievable OIP3 is +44 dBm up till an input power tone of -17 dBm.



(a) s_{21},s_{11},s_{22} **(b)** Noise Figure

(c) Stability **(d)** Step Response

Figure 4-23: Simulation results of LNA with differential CE stage



(a) Power Gain vs. P_{out} **(b)** OIP3 vs. P_{tone}

Figure 4-24: Compression Point and Linearity performance of LNA with differential CE stage

In this case, Monte Carlo simulation is done as well for both process and mismatch variation. The results are as shown in Figure 4-25. The simulation was done for N=500 points. From the simulation results, it can seen that the linearity is very sensitive to the mismatch variation. The standard deviation is greater than 1, means its variation is greater than 3σ, this fails SOA (safe area of operation). SOA is one of the important consideration for high power device, as it determines the manufacturability and reliability. The range of variation in from OIP3 is 47.5 dBm to 39 dBm respectively. The sensitivity in OIP3 is higher due to its initially higher value, which depends on a IM3 sweet spot.

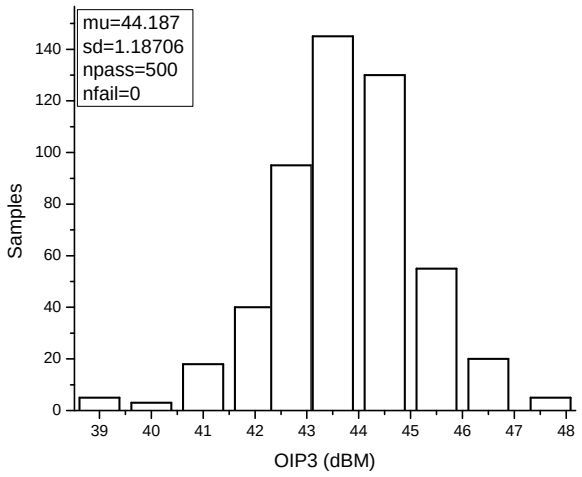


Figure 4-25: Monte Carlo simulation of schematic for LNA with differential CE stage

4-5 Conclusions

In this chapter, the input stage was impedance and noise matched to achieve low IRL and noise figure. The specifications for the input stage are satisfied as shown by simulation results. Next, the output stage was designed to achieve high linearity and high compression. Two output stage configurations have been considered, namely a differential cascode configuration and differential CE stage configuration. The use of a differential CE stage configuration seems to result in the highest linearity potential. This is a bit different than the linearity results obtained in Chapter 3. It should be stressed however, that within this Chapter, use has been made of the full Mextram which closely describes the underlying QUBIC technology. In contrast, in Chapter 3 use was made of the much simpler Gummel-Poon model using some approximating parameters. The reason for this choice was that a Gummel-Poon model can be easily simplified, such that the individual distortion contributions in the circuit can be quantified. After the discussion of both input and output stages using the complete models, the stages were combined to form a 2-stage LNA. Monte Carlo simulations were done to analyze the influence of the process and

device mismatch variations. This analysis indicated that, the cascode seems to be less affected by component spread than the CE output stage, but that the CE stage seems to have the capability to provide the highest linearity. Simulations indicate that this is due to interactions due to the seconder terminations at the output and the feedback circuitry.

Chapter 5

Physical layout and post-layout results

5-1 Introduction

In this chapter, the LNA layout and post-layout simulation are discussed. The tools used for the layout and post-layout simulation are virtuoso layout editor, Assura (post layout parasitic extraction) and ADS Momentum for simulating the interconnect and balun.

5-2 Schematic

The schematic used for generation of the layout is shown in Figure 5-1. Initial post layout iterations were performed based upon the expected performance, few changes have been made in LNA design described in Chapter 4. During the initial post layout simulation the interconnect related to connecting the capacitor C_{zero} to the ground in first stage impacted the stability performance. This interconnect behaved as finite inductance, which appears as negative resistance for CE stage that can causes instability [35]. A a remedy resistor R_{stab} is connected in series with the grounding capacitor C_{zero}. This R_{stab} de-Q's the resonance response of capacitor and interconnect inductance to improve stability. However, although R_{stab} improves stability it degrades the noise performance.

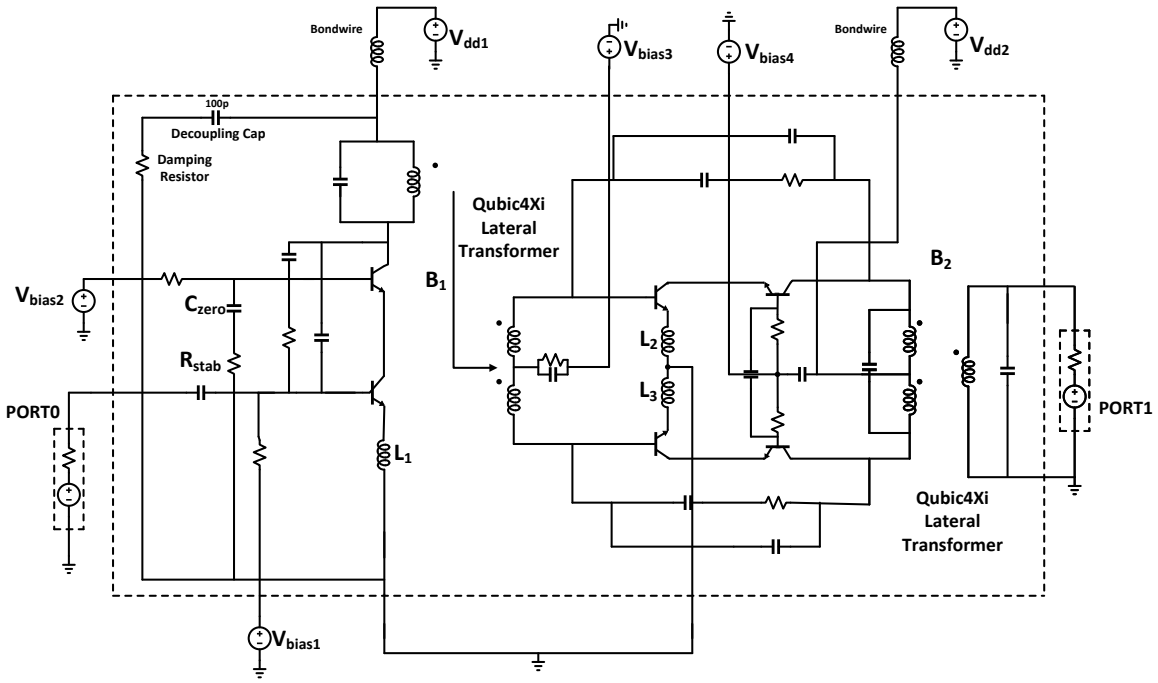


Figure 5-1: Final schematic of the overall LNA with differential cascode output stage

5-3 Metal stack

The metal stack available in QUBiC4Xi is shown in Figure 5-2. The substrate is high resistive, which is very favorable for RF circuit design. The high resistive substrate will not have any significant effect on the magnetic field flowing in the top metal layer [36]. The technology provides 5 metal layer stack. The top metal is thickest metal layer, which is used for designing on-chip passives. This layer is also used for routing of critical interconnects.

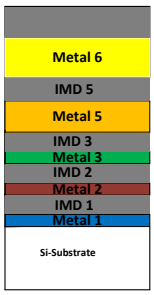


Figure 5-2: Metal stack

5-4 Inductor and balun

In the implementation of the 2 stage LNA, three inductors and two baluns are used. One inductor is used for inductive degeneration of the first stage L_1 and the two other inductors L_2 and L_3 are used for degeneration at output stage. Balun B_1 is used for magnetic coupling of the first and second stage. The second balun B_2 is used for conversion of the differential output stage to single-ended load at the output. Table 5-1 shows dimensions and values of the inductors used in layout implementation. The layout of the inductor used is shown in Figure 5-3.

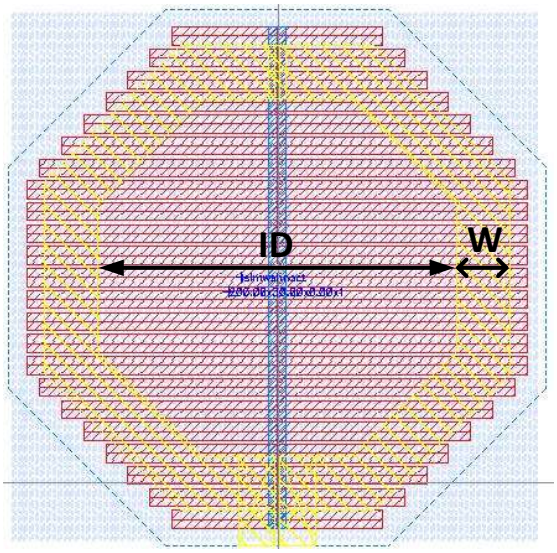


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Figure 5-3: Inductor layout used for various inductor in LNA

Table 5-1: Dimension and values of inductance used in layout

	ID [μm]	W [μm]	inductance [nH]
L_1	180	30	0.350
L_2	120	30	0.240
L_3	120	30	0.240

The balun B_2 at the output needs to be designed for low losses, since its losses limit the output compression of the LNA. In order to limit the losses the coupling factor k_m should be high. In practice achievable values for the coupling factor are within the range of $0.75 < k_m < 0.9$. The main factors affecting the magnetic coupling are width and spacing of metal and thickness of substrate [37]. The parameters such as thickness of substrate and minimum spacing between the metal are fixed by the technology. The other factor, would be to improve the quality factor of both primary and secondary. In order to improve quality factor the width of the metal is increased. The

losses are also reduced by optimizing for the inner diameter. To reduces the effect of substrate coupling shielding is provided. The shield is floating, which increase the resonant frequency. The increase in resonant frequency is due to the fact that conductive path between signal and ground conductor is doubled [38]. The parameters set for both the input and output balun is in Table 5-1 and the layout is shown in Figure 5-4.

Table 5-2: Dimension and values of inductance of coils in balun used in layout

	ID [μm]	W [μm]	Primary inductance [nH]	Secondary inductance [nH]
B_1	230	22	3.8	2.83
B_2	170	22	2.15	1.61

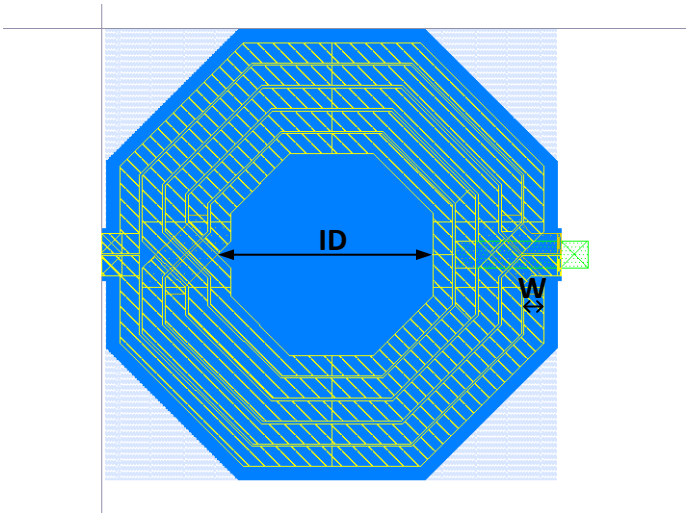
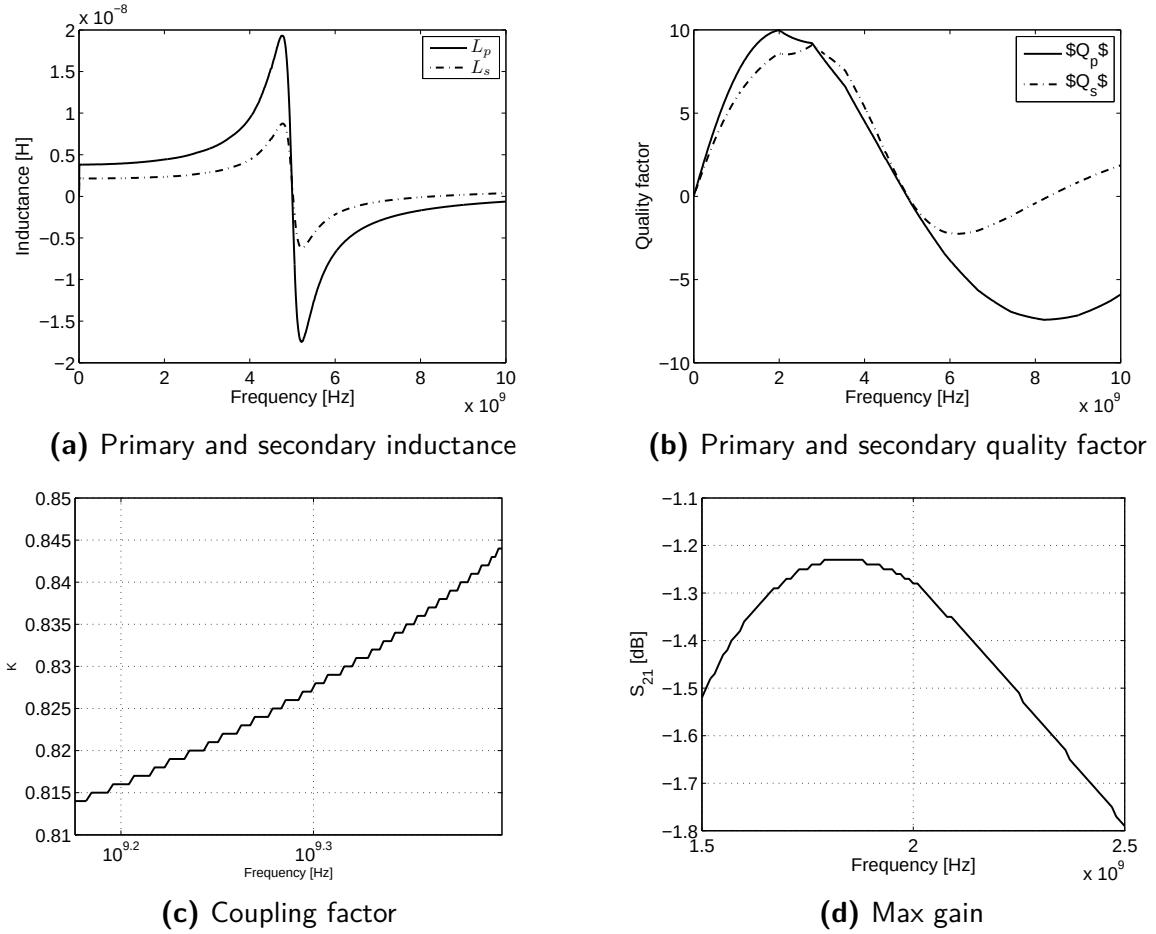


Figure 5-4: Balun Layout

The performance of the output balun is shown in Figure 5-5. The inductance of both primary and secondary are 3.8 nH and 2.15 nH respectively. The quality factor achieved for both primary and secondary are 10 and 8.5 respectively. The coupling factor is 0.871. The primary and the secondary windings of the balun are tuned with a capacitor to reduce the losses. The loss at 1.84 GHz is about -1.2 dB.



(a) Primary and secondary inductance

(b) Primary and secondary quality factor

(c) Coupling factor

(d) Max gain

Figure 5-5: Performance of output balun

5-5 Layout considerations

The LNA is designed for high-output power application, so electromigration consideration becomes very important. Electromigration is the displacement of metal atoms of the conductor due to the current flowing through it. Due to electromigration voids, hillocks, and extrusion on metal are formed [39]. It may result in open circuit conditions when voids on the metal lines are big or short circuit condition if the extrusions are long enough such that it forms a connection with adjacent metal layer. To avoid these problem electromigration rules are followed for each metal layer. The EM rule for Metal6, Metal5, Metal3, Metal2 are 20.6 mA/μm, 11.5 mA/μm, 5.3 mA/μm for 100 $^{\circ}C$ temperature, respectively. The power supply for output stage is provided at the center tap of the balun, the metal used for center tap is Metal3. The bias current of the output stage is high due to the linearity and compression point requirement. However, the current handling capability of the Metal 3 is low, hence Metal3 and Metal2 are used in parallel to satisfy the EM rules.

The primary mechanism of injection of substrate noise is due to coupling of junction capacitance to the substrate, impact ionization, power and ground fluctuations. The injected noise propagates along the substrate, may reach the sensitive circuit. To avoid coupling of the noise with the sensitive circuit a guard ring is used. The guard ring consists of contacts to substrate. These guard ring are connected to ground path acting as a low resistant path to remove the noise.

Deep trench isolation (DTI) is a process of etching a pattern in substrate before transistors are laid. Usually a deep trench isolation layer is used to isolate the transistor and decrease the capacitance to ground. Deep trench layer is used around the transistor, and underneath all the passive elements (i.e,inductor, capacitor, resistor). Figure 5-6 shows the application of DTI layer and guard ring around the transistors.

During the plasma etching, the charges are stored on the floating metal layer, when connected this event may destroy the nitride layer of MIM capacitor, whose dielectric thickness is less or destroy the transistor device. Protection diodes are used to prevent antenna problems. The antenna protection diode reduces the voltage across the oxide below the tunneling threshold [39].

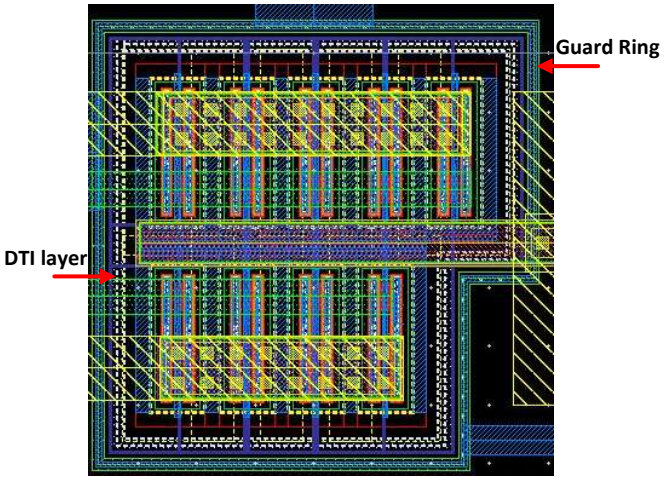


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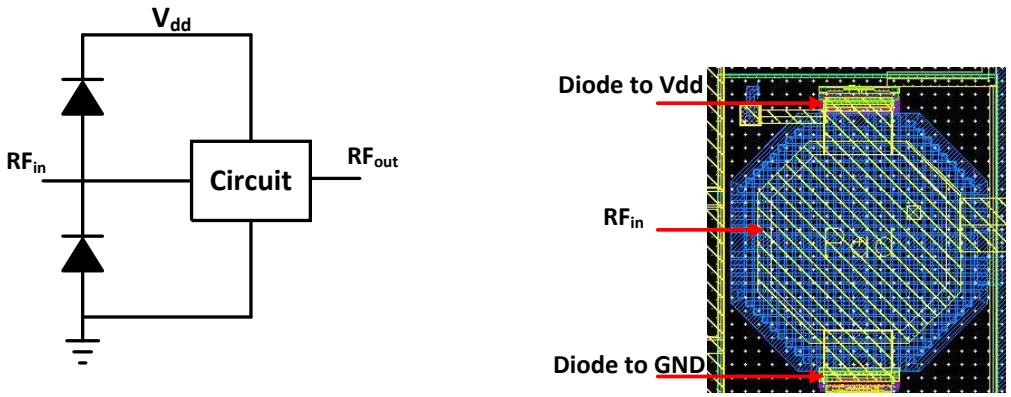
Figure 5-6: Guard ring and DTI layer for transistor

A high ESD pulse, resulting in high current should not affect the devices on the chip. ESD protection is provided at the input by connecting the diodes as in Figure 5-7. At the output ESD protection is not provided, since the connecting balun (i.e, inductor) does not allow sudden change in the current due to an ESD event.



(a) ESD protection diode in schematic **(b)** ESD protection diode in layout

Figure 5-7: ESD protection

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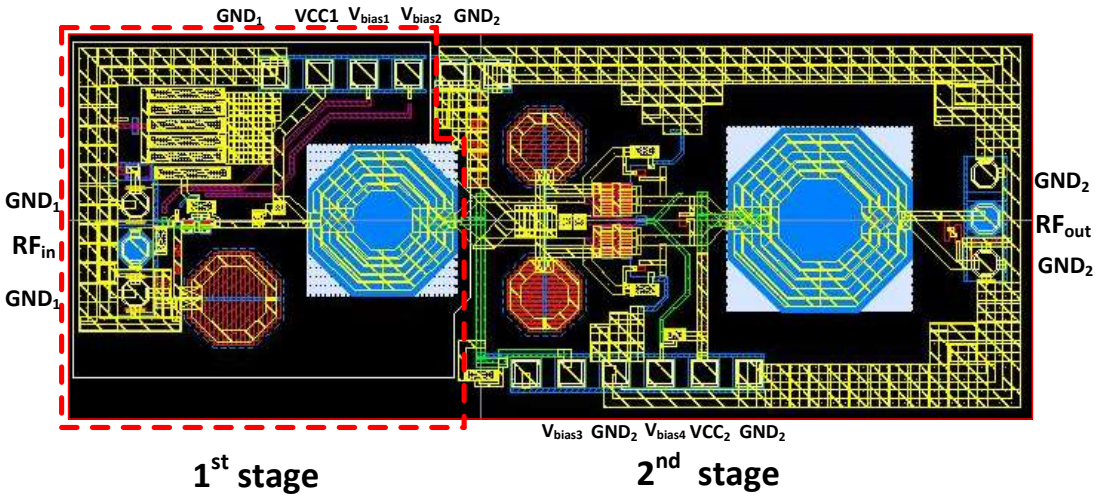


Figure 5-8: Final layout

The floorplanning of the 2 stage LNA is shown in Figure 5-8. The noise requirements are critical for the first stage. The transistors are kept close to RF_{in} pad, to avoid long interconnect. The long interconnect would degrade the noise performance. The transistors are connected overlapping each other to reduce the interconnect losses. The output stage is built symmetrically to get high linearity. Both the input and output stages operate at different current levels. Thus, separate ground are used GND1 and GND2 for input and output stages respectively.

5-5-1 Momentum simulation

In order to determine the overall performance of the interconnect, inductor and balun, a momentum simulation of the top metal layer is done. The layout used for Momentum simulation is shown in Figure 5-9. The Momentum simulation is done for three metal layers Metal6, Metal5 and Metal3. In the figure, yellow color with different shading represents Metal6, Metal5 and the one in green is Metal3. The quality factor and effective inductance of the inductor and balun will change as it couples with surroundings. This will impact the performance of the circuit. The Momentum simulation helps to include these RLC effects simultaneously. Due to the high-current operation, any voltage drop across the ground plane would reduce the gain and compression point. In order to reduce the inductance and resistive losses the ground plane is built using stack of three metal layers: Metal6, Metal5, Metal3 in parallel.

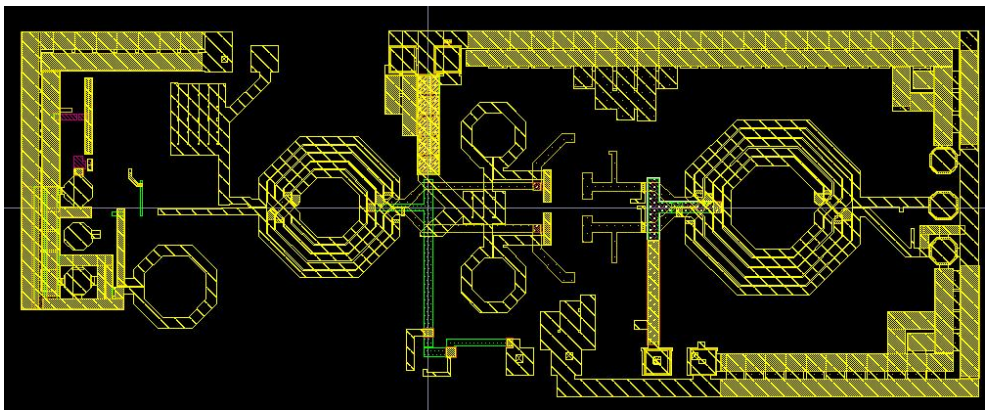


Figure 5-9: Momentum view of top metal layer

5-6 Post layout simulation results

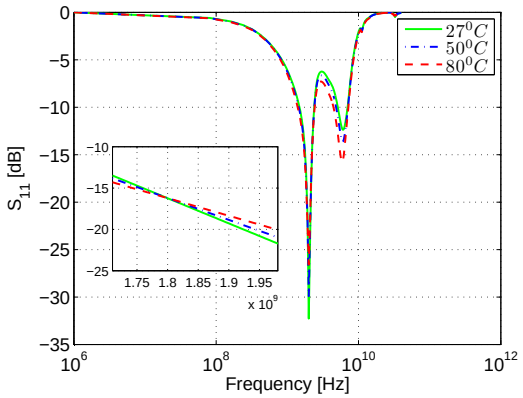
The post layout simulation results are derived from:- transistor and interconnect are RC extracted using Assura and the inductor, balun and interconnect are RLC extracted using Momentum. The simulation are done to evaluate effect all the PVT variations. The simulations are repeated to check RF performance of the circuit including layout effects at 27 $^{\circ}C$, 50 $^{\circ}C$, 80 $^{\circ}C$. Since PTAT biasing is not included, bias voltage at each temperature will change as shown in Table 5-3. Secondly, simulation results due to the effect of bias and supply voltage variation on the OIP3 are shown. Finally, process and mismatch variation done using Monte Carlo simulation for the LNA including layout effects.

Table 5-3: Biasing for different temperatures

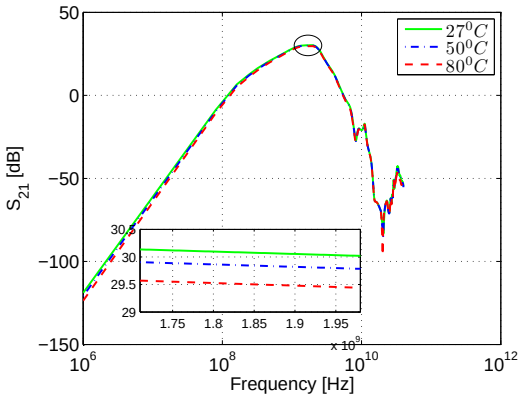
Temperature [$^{\circ}C$]	V_{dd} [V]	V_{bias1} [V]	V_{bias2} [V]
27	3.3	0.790	0.800
50	3.3	0.775	0.780
80	3.3	0.765	0.750

s-parameter

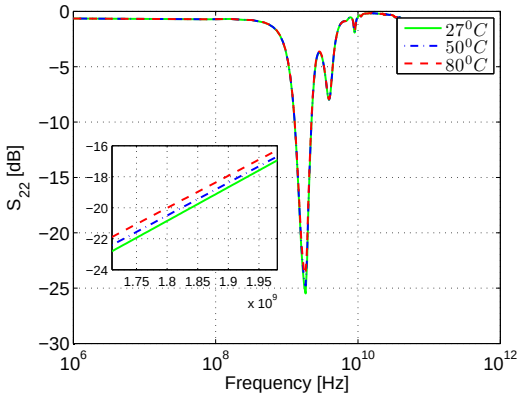
The s-parameter simulation results at different temperatures are shown in Figure 5-10. The parameters are plotted from DC to 40 GHz. The input(S_{11}) and output return loss (S_{22}) are close to -18 dB and -20 dB respectively. The gain S_{21} is as targeted 30 dB. From the figure it can be seen that gain and return losses are not affected by the temperature variations.



(a) S_{11}



(b) S_{21}



(c) S_{22}

Figure 5-10: S-parameter

Noise figure

The noise figure for different temperatures is shown in Figure 5-11. At 27 $^{\circ}C$, the noise figure is 0.65 dB. The noise performance degrades as the temperature increases.

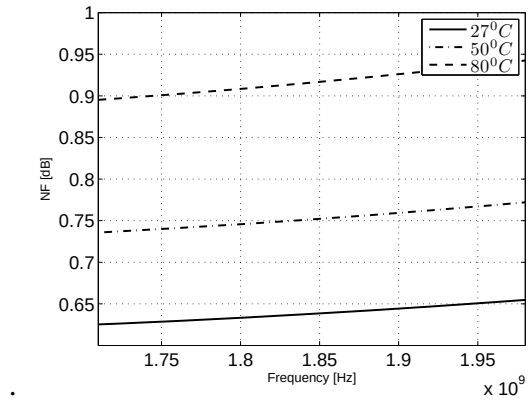
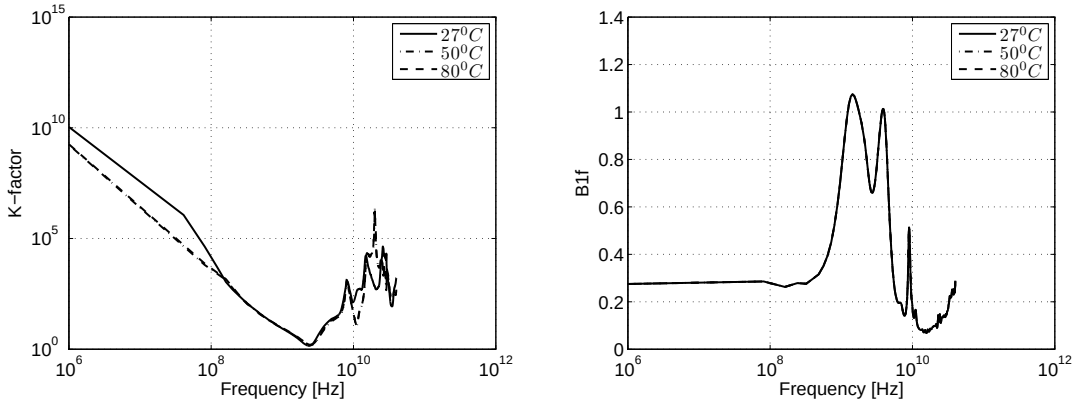


Figure 5-11: Noise figure at different temperature

Stability

The stability performance of the 2 stage LNA is as shown in Figure 5-12. It can be seen inferred that the system is unconditionally stable for a large range of frequencies.



(a) K-factor **(b)** B1f

Figure 5-12: Stability analysis

OP1dB

The OP1dB is simulated for frequency range from 1.71 GHz and 1.98 GHz. The compression point variation due to temperature is shown in Figure 5-13. At nominal temperature 27 $^{\circ}C$, the

achieved output compression point is 24 dBm. The maximum variation due to temperature is around 0.5 dB over the temperature.

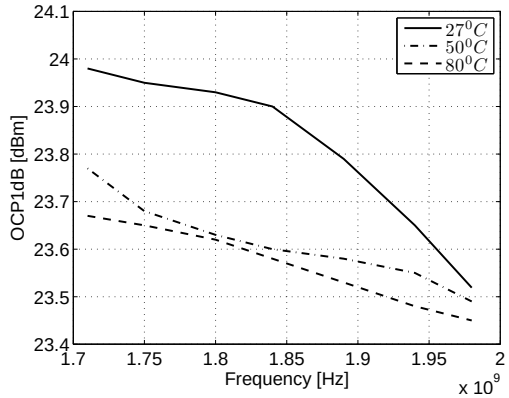
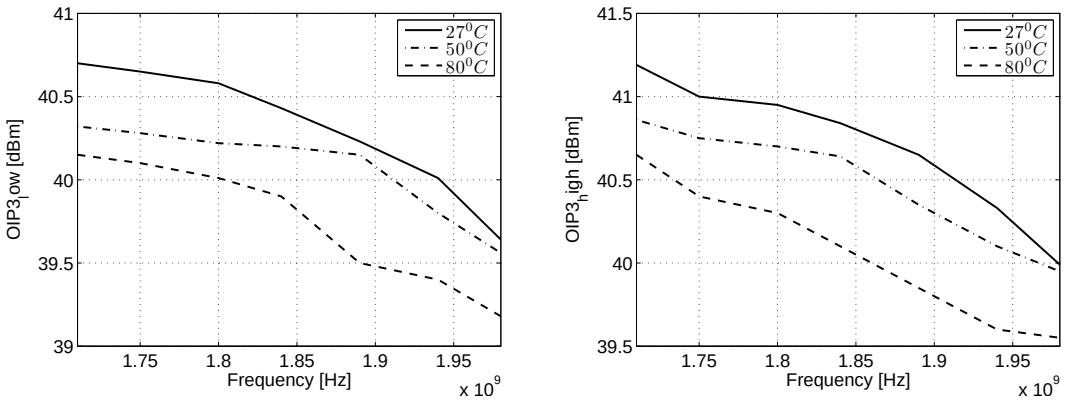


Figure 5-13: Output compression point for different temperatures

OIP3

The variation of OIP3 for different temperatures is shown in Figure 5-14. For linearity performance a 2 tone simulation is done over the frequency range from 1.71 GHz to 1.98 GHz. The center frequency is varied from 1.71 GHz to 1.98 GHz, with a tone spacing of 10 MHz and input power for each tone -20 dBm. The OIP3 results are shown for both IM3 intermodulation products, lower and upper sideband. Figure 5-15 shows the OIP3 versus input tone power, from this figure it can be concluded that OIP3 is almost constant till 1 dB compression point.



(a) $OIP3_{low}$ **(b)** $OIP3_{high}$

Figure 5-14: OIP3 for both sidebands

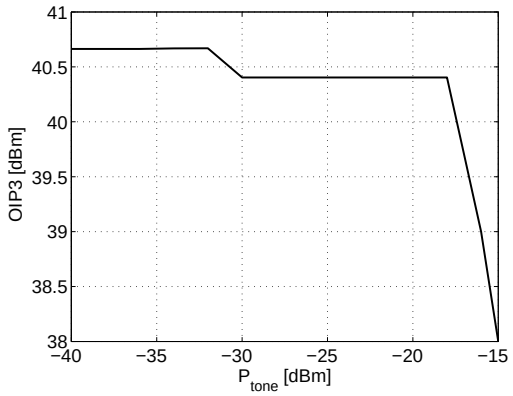
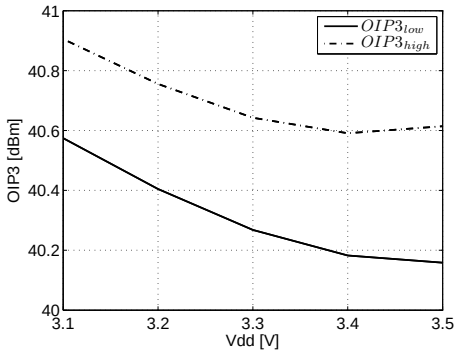


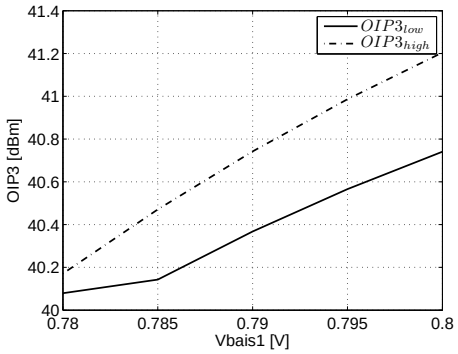
Figure 5-15: OIP3 vs input tone power @ 1.84 GHz

Supply and bias variation

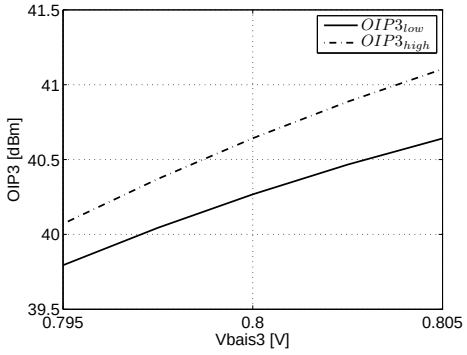
In order to evaluate the effect of supply and bias voltage on the linearity, a simulation for varying supply voltage and bias voltage is done. The simulation results are shown in Figure 5-16.



(a) OIP3 variation V_{dd} @ 1.84 GHz



(b) OIP3 variation V_{bias3} @ 1.84 GHz



(c) OIP3 variation V_{bias1} @ 1.84 GHz

Figure 5-16: Plot of OIP3 due to supply and bias variation @ 1.84 GHz

The supply V_{dd} is varied round 3.3 V and two bias voltage V_{bias3} and V_{bias1} around 0.79 V and 0.8 V respectively. The variation in voltages does not have much impact on the linearity.

Process and mismatch variation

A Monte Carlo simulation is performed to verify the impact of process and mismatch variation. The simulation was done at 27 $^{\circ}C$, for input tone power of -20 dBm at center frequency of 1.84 GHz and beat frequency of 10 MHz for N = 100 runs. The histogram of OIP3 is shown in Figure 5-17.

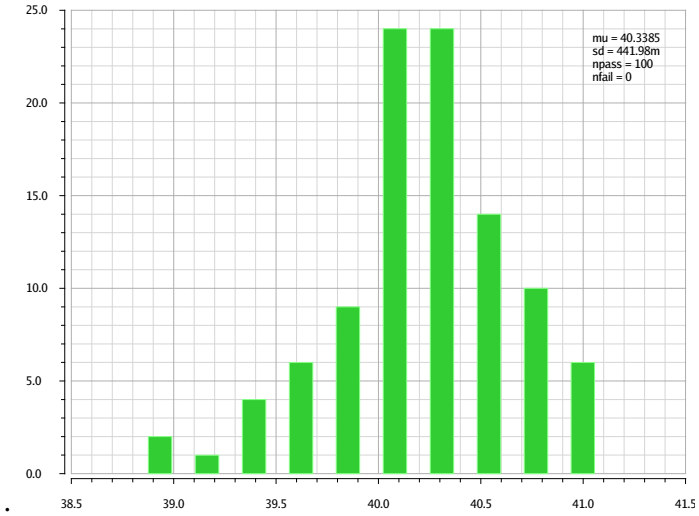


Figure 5-17: Histogram of OIP3

5-7 Comparison and conclusion

Table 5-4, compares the simulated results form post-layout parasitic extraction of this work with the state-of-the-art in the literature. Two designs with different input stages—a cascade and a cascode of two CE stages—and same output stage are presented in [5]. However, in that paper the input and the output stages are implemented using different technologies 0.25 μm SiGe QUBiC4Xi and QUBiC4X. In contrast, this work implements both the stages in a single technology, thereby enabling higher degree of integration and reduced system costs with a better performance. The noise figure of 0.65 dB, high linearity of 40 dBm, and output high compression point of 24 dBm are achieved. Increased dissipated power results from the higher OP1db compression point achieved. This shows the effectiveness of proposed techniques to enhance linearity and compression point. This allows the use of low cost ultra linear LNA for base station applications.

Table 5-4: Comparison with state-of-the-art

Parameter	**This Work**	**[5]** cascode	**[5]** Two stage
S_{21} [dB]	30	37	37
S_{11} [dB]	-18	-20	-20
S_{22} [dB]	-20	-20	-20
Noise figure [dB]	0.65	0.7	0.6
Stability	Unconditionally	Unconditionally	Unconditionally
OIP3 [dBm]	>40	40	38
IIP3 [dBm]	10	3	1
OP1dB [dBm]	24	22	23
Pdiss [W]	0.820	0.75	0.65
Technology	0.25 μm SiGe QUBiC4Xi	0.25 μm SiGe QUBiC4Xi and QUBiC4X	0.25 μm SiGe QUBiC4Xi and QUBiC4X

Chapter 6

Conclusions and future work

6-1 Conclusion

The main aim of this project was to investigate and to propose an architecture which is capable to achieve simultaneously high gain, low noise, high linearity, and high compression point using QUBiC4Xi 0.25 μm SiGe BiCMOS technology. As such, an ultra-linear LNA for base station was designed, following a two stage approach. In this two-stage design, the first stage was optimized to achieve high gain and low noise, whereas the output stage was targeted to achieve high linearity and high compression.

A cascode/CE-CB stage was used for the first stage, which achieves high gain (20 dB) and good reverse isolation. The input return loss is -18 dB, which was achieved by matching using a degenerative inductor, a shunt-feedback capacitor. By optimum biasing and noise matching, a noise figure of 0.5 dB for the first stage was obtained. The linearity requirement for first stage was satisfied using implicit IM3 cancellation.

Two differential output-stages implementations were investigated namely, a differential cascode and a differential CE stage. The advantage of using a differential structure is that the fundamental and the second harmonics can be controlled orthogonally, which helps in improving the linearity. Before applying any linearity improvement technique the dominant non-linearities of the transistor were analyzed. Techniques used to improve linearity in this report are: implicit IM3, overall negative feedback, 2^{nd} harmonic termination at the output and out-of-band linearization at the input of the output stage. The implicit IM3 cancellation was done using degeneration inductor. The out-of-band cancellation was implemented as base tuning in the differential output stage. The external load is single-ended, so a balun is used at the output differential stage to convert to single-ended. A LC series resonant circuit was provided at the center tap of the transformer output balun to provide a 2^{nd} harmonic trap. The maximum linearity (OIP3) achieved for the differential cascode and differential CE output stage are 41 dBm and 46 dBm, receptively. The

output compression point of 24 dBm was achieved using output balun transformer as matching element.

The differential output stage was combined with the single-ended input stage to form a 2-stage LNA. The 2-stage LNA using differential cascode based output stage showed less variation due to process spread, than differential CE as output stage, however the later configuration seems to have the potential to achieve even higher linearity levels. The single-ended input stage and differential output-stage were coupled using a balun. The balun facilitated in the interstage matching maximum power transfer. As final step physical layout of 2-stage LNA with differential cascode output stage was designed. The layout parasitic were extracted using Assura and Momentum. The related post layout simulation results provided insight in performance spread for different temperature, supply and process variation. All target specification were achieved in simulation: low noise figure (0.65 dB), high gain (30 dB), high output compression (24 dBm) and high linearity OIP3 (40 dBm) up to the 1dB compression point.

6-2 Future work

Balun design

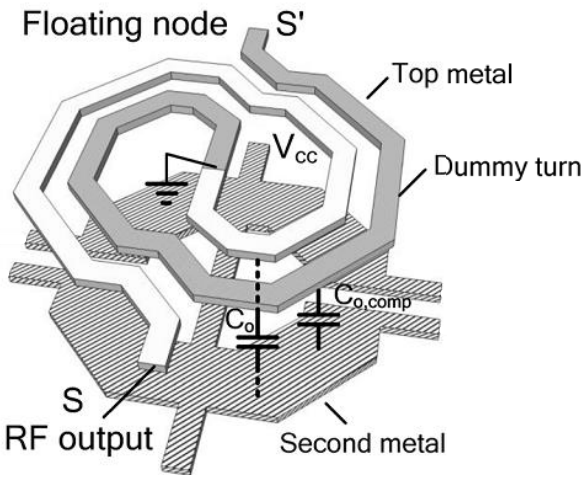


Figure 6-1: Laterally compensated balun [40]

The disadvantage of using differential topology for the output stage is that it's quite difficult to achieve fully symmetrical operation. In all practical baluns there is parasitic capacitance between the primary and the secondary coils of balun. The effect of this parasitic capacitance increases when multiple windings are used. During the conversion from single-ended to differential or vice versa using a balun, one terminal of the single ended side of the balun is connected to load

and other to AC ground. As such capacitive loading is unbalanced. Therefore there is also an impedance unbalance seen by the output transistor. It is rather difficult in practice to use an extra lumped capacitor in the output balun to compensate for these effects. In fact, to compensate for the mismatch in transformers, the most optimum approach seems to be an additional dummy turn shown in Figure 6-1. Note that in this structure the voltage swing seen at the RF output to S is duplicated along the length of the winding. As such, the parasitic capacitance C_o, between the winding is effectively compensated by capacitance $C_{o,comp}$ between the dummy turn and the second metal [40].

Cross coupled design

From the experiments in Chapter 3, one major reason linearity constraint at higher bias currents is the non-linear base-to-collector capacitor C_{jc}, which acts like a nonlinear feedback. One technique to reduce the impact of this capacitor would be to use bridge neutralization. The differential CE stage cross coupled capacitor is shown in Figure 6-2. In this figure the two cross-coupled capacitances are provided by diode connected transistors Q_{1c} and Q_{2c}. These two diodes are connected in anti-phase, which eliminate the feedback effect of C_{jc}. This structure can yield good reverse isolation and help improve stability for the differential operation. Simulations indicate that this approach can enhance the linearity by at least 3-dB (When the linearity is base-collector limited). Higher linearity levels seems to be feasible, but this requires still more investigation, since there seems to be an interaction with linear (resistive) feedback elements.

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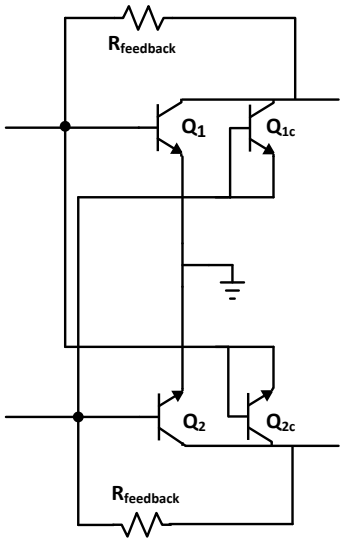


Figure 6-2: Cross coupled differential stage

Appendix A

Appendix A

A-1 Single-ended output stage

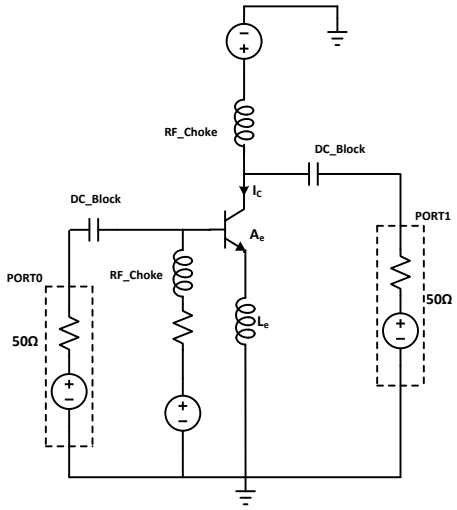
In this appendix, the implicit IM3 cancellation and overall feedback are applied to single stage amplifier, to investigate the linearity of QUBiC4Xi technology.

A-1-1 An inductively degenerated CE stage

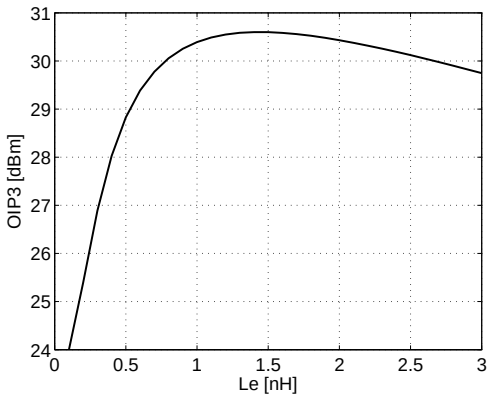
An inductive degenerative CE is shown in Figure A-1 (a), where *Le* is the degenerative inductor, A_e is emitter area and I_C collector current. As discussed in section 3-3 the implicit IM3 depends on the value the of the degeneration inductor and bias current. The Figure A-1 (b) shows the variation of OIP3 versus the degeneration inductor L_e. Final simulated OIP3 may be different but, this plot provides a direction for optimization of the design. From figure it can be seen that linearity improves for increasing L_e. At lower current levels the exponential distortion dominates.

Design example

When the approximate values of collector current and degenerative inductance are known, these values can be used for further optimizing of the design. From the specification, the gain required for second stage is 10 dB. The gain of the degenerative CE can be calculated from Eq. (A-1), but at high frequency the Miller effect needs to be considered. The Miller capacitor along with C_π provides a low impedance at the input for high frequencies, so the gain reduces at high frequency.



(a) Inductively degenerated CE stage



(b) OIP3 vs. L_e @ 1.84 GHz of the size:0.4 μm x 20.7 μm x 25 QUBiC4Xi SiGe BNA transistor

Figure A-1

The transconductance required to achieve high gain depends on the collector current ($g_m = \frac{I_C}{V_T}$). For sustaining high collector current the emitter length needs to be chosen to be larger. A transistor size of 0.4 μm x 20.7 μm x 25 is considered for design. For this size of device C_{je} value is 5.824 pF. The optimum value of inductor required to improve the linearity is given by Eq. (A-2). By substituting the value of C_{je} and operating frequency of 1.84 GHz, the value of the inductor required is 1.4 nH. The value of load impedance required to achieve the required gain is calculated. The biasing network are optimized for out of band IM3 cancellation to improve the linearity further. The supply voltage used is 2.5 V and collector current is 51 mA. The OIP3 versus input power tone is as shown in Figure A-2. The results obtained by this architecture is given by the table A-1.

$$A_v = \frac{-g_m * Z_L@1.84G}{1 + g_m * Z_e} \tag{A-1}$$

$$L_{e,opt} = \frac{50}{C_{je}\omega_t^2} \tag{A-2}$$

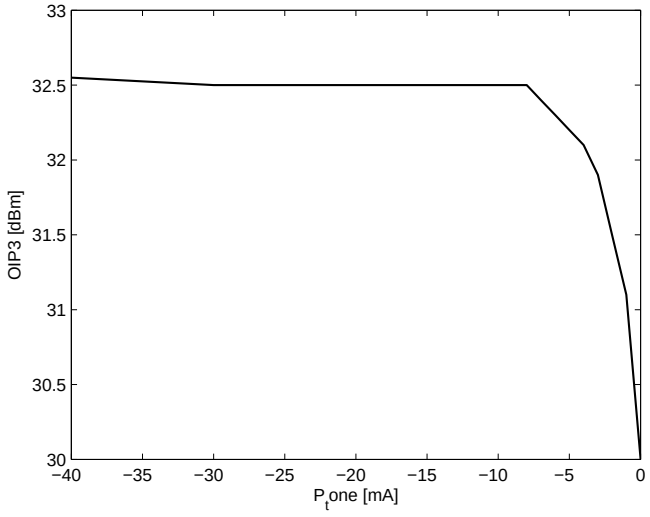


Figure A-2: OIP3 Vs Input Power

Table A-1: Design matrix achieved for an inductively degenerated CE stage

Parameter	Value
Gain S_{21}@1.84G Hz [dB]	10
OCP1 [dBm]	18.53
ICP1 [dBm]	8.53
OIP3 [dBm]	32.5
Stability	unconditionally stable

The gain requirement can be easily achieved with the CE stage, but it is limited for its OIP3. The main limiting factor for inductive degenerated CE stage in achieving high linearity is base-collector capacitance and base-charge modulation. A cascode stage can be used to reduce the feedback of base collector capacitor.

A-1-2 An inductively degenerated cascode

The configuration of an inductive degenerative cascode is shown in Figure A-3, where $Q1$ is CE stage, $Q2$ is CB stage, Le is degenerative inductor, A_e is the emitter area and, I_C collector current. Figure A-4 at lower current levels the linearity is improved using to implicit IM3 cancellation through degeneration inductor.

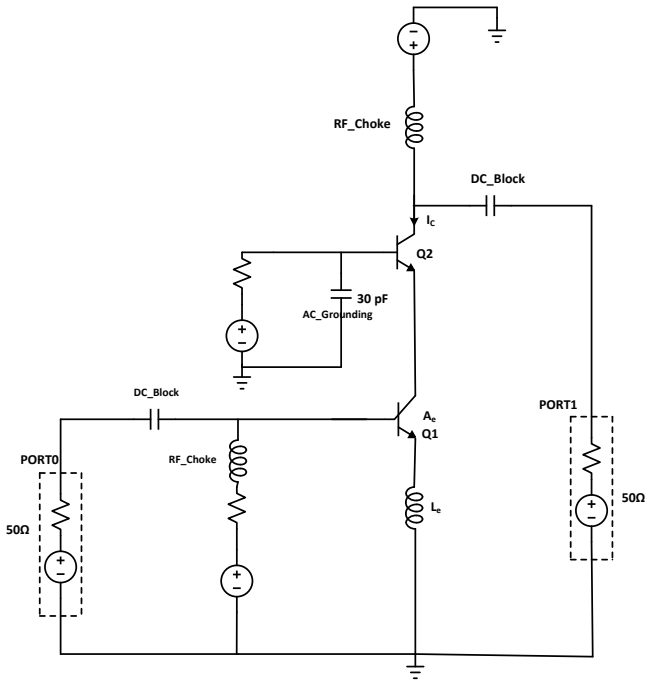


Figure A-3: Cascode inductive degeneration

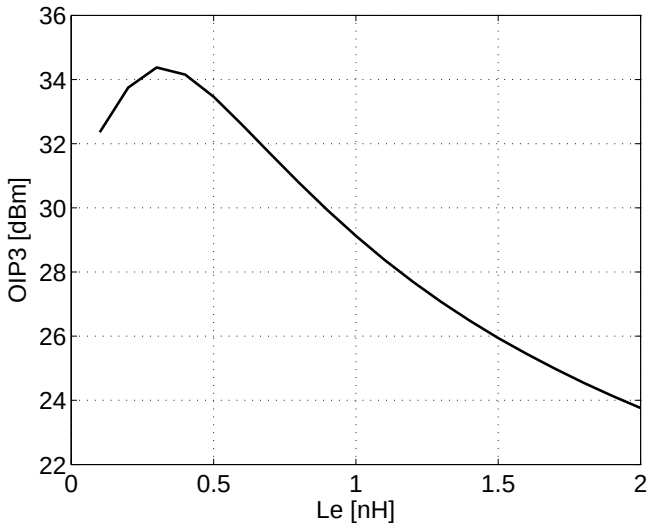


Figure A-4: OIP3 vs. L_e @ 1.84 GHz of the size:0.4 μm x 20.7 μm x 25 QUBiC4Xi SiGe BNA transistor

Design example

From Figure A-4 the optimum value for degenerative inductor is obtained. The supply voltage required for the biasing of cascode stage is 3.3 V. The collector to base voltage V_{CB} is kept low to reduce the non-linearities introduced by base to collector capacitor of CE stage (≈10 mV). The OIP3 versus the input power tone is plotted as shown in Figure A-5. The achieved specification from inductive degenerated cascode is as given by table A-2.

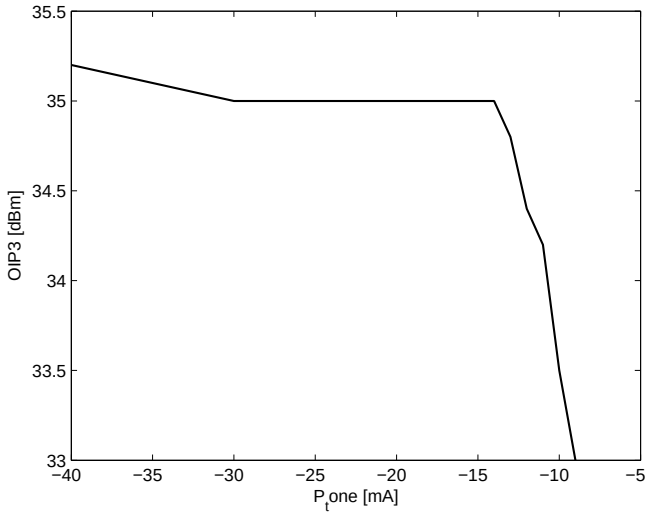


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Figure A-5: OIP3 Vs Input Power

Table A-2: Design Matrix of an inductively degenerated cascode

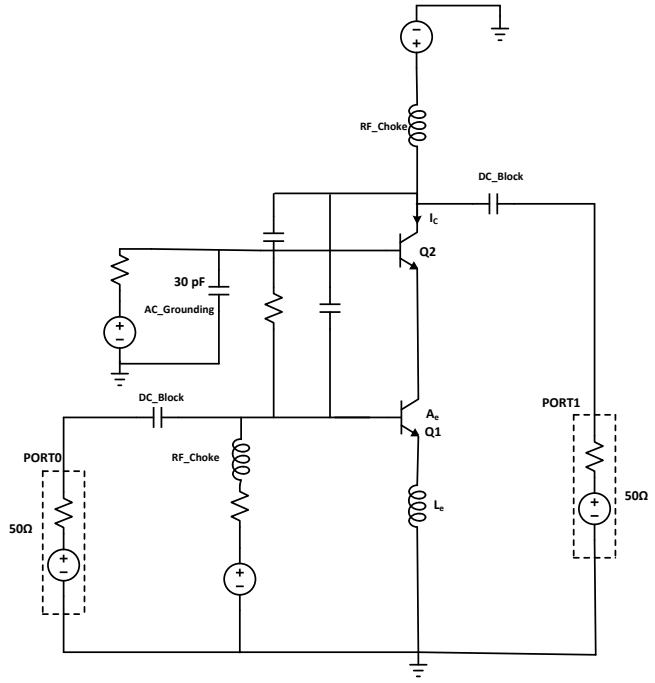
Parameter	Value
Gain S_{21}@1.84G Hz [dB]	22
OCP1 [dBm]	19.5
ICP1 [dBm]	-2.5
OIP3 [dBm]	35
Stability	unconditionally stable

From the design, it can be concluded that the even after using a cascode configuration required specification of linearity (OIP3)are not achieved. The advantage of using cascode is high loop gain. The gain achieved from cascode is 22 dB which is high when compared to the specification of the output stage. This high gain can be reduced by using a negative feedback. An inductive degenerative feedback cascode with feedback is discussed in next section.

A-1-3 An inductive degenerated cascode with feedback

An inductive degenerated cascode with feedback is shown in Figure A-6. The feedback is applied through resistor $R_{feedback}$. Due to overall feedback the linearity is improved, which is shown in

Figure A-7.



.

Figure A-6: An inductive degenerated cascode with feedback

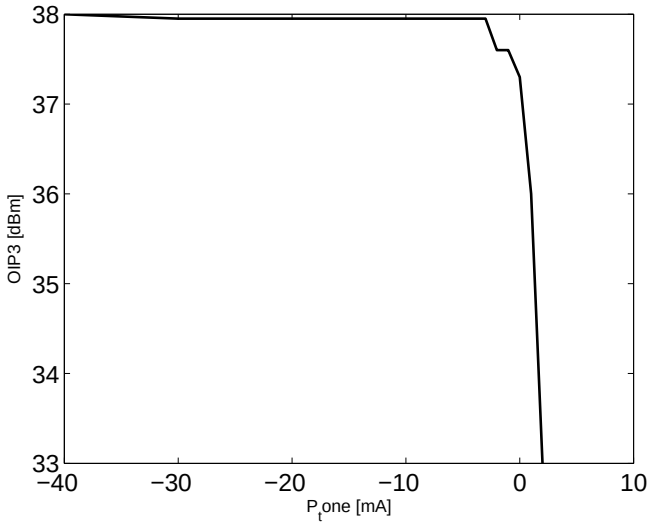


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Figure A-7: OIP3 Vs Input Power

It can be concluded that, an inductive degenerated cascode with feedback provides high linearity compared to inductive degenerated cascode and CE stage. The open gain provided by the cascode

is reduced by using feedback to achieve high linearity. The design matrix achieved by using inductive degenerated cascode with feedback is shown Table A-3.

Parameter	Value
Gain S_{21}@1.84G Hz [dB]	10
OCP1 [dBm]	21
ICP1 [dBm]	11
OIP3 [dBm]	38
Stability	unconditionally stable

Table A-3: Design Matrix of an inductive degenerated cascode with feedback

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Glossary

List of Acronyms

IRL	Low return loss
ORL	Output return loss
LNA	Low noise amplifier
HEMT	High electron mobility transistor
HBT	Heterjunction bipolar transistor
GaAs	Gallium arsenide
InP	Indium phosphide
SiGe	Silicon germanium
BJT	Bipolar junction transistor
NF	Noise figure
IF	Intermediate frequency
pHEMT	Pseudomorphic High electron mobility transistor
MESFET	MetalâĂŞsemiconductor field effect transistor
IM3	3rd order intermodulation component
IIP3	Input third order intercept
OIP3	Output third order intercept

FDD	Frequency division duplex
GSM	Global system for mobile communications
CE	Common emitter
CB	Common base
HV	High voltage
NF	Noise figure
IF	Intermediate frequency
DCS	Digital Cellular System
ESD	Electrostatic discharge
DTI	Deep trench isolation
ADS	Advanced Design System