Surface-Passivated High-Resistivity Silicon Substrates for RFICs

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***Abstract*—Surface passivation of high-resistivity silicon (HRS) by amorphous silicon thin-film deposition is demonstrated as a novel technique for establishing HRS as a microwave substrate. Metal–oxide–silicon (MOS) capacitor measurements are used to characterize the silicon surface properties. An increase of the quality factor (Q) of a 10-nH spiral inductor by 40% to $Q = 15$ and a 6.5-dB lower attenuation of a coplanar wave guide (CPW) at 17 GHz indicate the beneficial effect of the surface passivation for radio frequency (RF) and microwave applications. Regarding CPW attenuation, a nonpassivated 3000-$\Omega \cdot$ cm substrate is equivalent to a 70-$\Omega \cdot$ cm passivated substrate. Surface-passivated HRS, having minimum losses, a high permittivity, and a high thermal conductivity, qualifies as a close-to-ideal radio frequency and microwave substrate.**

***Index Terms*—Attenuation, conductivity, coplanar waveguides, dielectric losses, eddy currents, excimer lasers, high-frequency (HF) measurements, HF receivers, HF transmitters, inductors, integrated circuit doping, losses, lossless circuits, loss measurement, magnetic fields, microwave circuits, microwave technology, monolithic microwave integrated circuits (MMICs), mobile communication, Q factor, scattering parameters, semiconductor device fabrication, semiconductor materials, silicon, transmission lines.**

I. Introduction

HIGH-RESISTIVITY SILICON (HRS) has long been viewed as an ideal substrate for radio frequency integrated circuits (RFICs) [1]–[5], but surface effects tend to overshadow the potentially low RF loss levels in HRS [6]–[9]. Charges within the insulating SiO_2 layer and at the SiO_2/Si interface lead to accumulation or inversion layers at the silicon surface, contributing to an increased attenuation of integrated transmission lines [6]–[11], a reduced quality factor (Q) of on-chip spiral inductors [12], and a leakage path between integrated devices [6]. Furthermore, the surface-channel losses can be bias-dependent, leading to difficulties in parameter control [7]. The impact of a parasitic surface channel is consequently more pronounced in coplanar wave guide (CPW) structures, in which the electric field is more concentrated at the wafer surface, [6]–[9], [11] than in microstrip structures [7], [10], or spiral inductors [12]. In view of the recent attention to the application of HRS substrates in RFIC processes [13], elimination of surface channels on HRS is highly desirable. The conventional surface channel stopper is not very applicable since the additional doping at the surface will lead to even higher losses [14]. Solutions will come from techniques that will transform the silicon surface region underneath the passive components into a highly damaged but still semiconducting material, having a very high trap density in the bandgap and possibly an increased bandgap. Conceptually, either a thin film having such properties can be deposited at the silicon surface or the silicon surface can be damaged by a high-dose implantation of, e.g., argon (Ar-I/I) prior to the interconnect formation in an IC fabrication process. Surface passivation by polysilicon thin-film deposition [10] and by amorphization through Ar-I/I [11], [12] have recently been proposed and demonstrated. The reliability and stability in subsequent hot-processing steps, which are crucial criteria in manufacturing, however, have not been addressed to date.

In this letter, a new HRS surface passivation technique, using an amorphous silicon thin-film deposition, is presented. The effectiveness of the new technique is demonstrated by a considerable improvement in CPW attenuation and inductor-Q. Process temperature stability is demonstrated for the first time and shown to be superior to the mentioned passivation technique by Ar-I/I.

II. Fabrication and Characterization

Float-zone HRS p-type wafers with nominally 3000-$\Omega \cdot$cm resistivity were used to fabricate metal–oxide–semiconductor capacitors (MOS-caps) and CPWs for characterization of the HRS surface region. Half of the wafer received a 30-nm thermally grown SiO_2 layer, through which a 10^{15} cm^{-2} Ar dose was implanted. That Ar dose is close to the critical dose for amorphization by Ar-I/I. A 300-nm-thick surface layer of silicon was amorphized by the Ar-I/I [verified by transmitting electron microcope (TEM)]. On the other half of the wafer, a 300-nm amorphous silicon (α-Si) layer was formed by plasma-enhanced chemical vapor deposition (PECVD, 350 °C for 3.5 h) directly on the HRS. Note that both techniques will require an additional photolithographic mask in an IC process. Next, a 500-nm-thick SiO_2 layer was deposited over the entire wafer by PECVD at 350 °C for 1.2 min. Finally, a 4-μm-thick metallization was added to form MOS-caps with a radius of 1 mm, having the second contact at the wafer backside. That backside contact was formed at the end of the process by using excimer laser annealing in order not to expose the wafer frontside initially to any additional thermal budget [15]. Also, 10-nH spiral inductors and CPWs (signal line width $= 50$ μm signal–ground spacing

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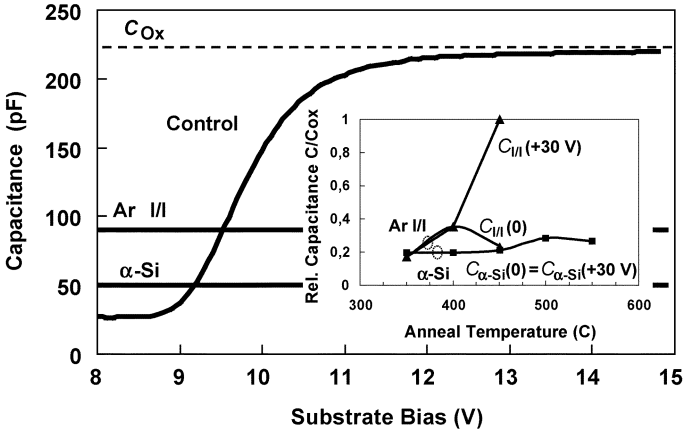

Fig. 1. *C–V* characteristics of MOS capacitors on a 3000-$\Omega \cdot$ cm silicon wafer without (control) and with surface passivation either by Ar implantation (Ar-I/I) or by amorphous silicon deposition (α-Si), measured at 100 kHz after a 400- °C, 30-min anneal. The oxide capacitance ($C_{\rm Ox}$) is indicated as a reference. The inset shows the relative change in capacitance at biases of 0 (inversion regime) and 30 V (accumulation regime), indicating that with the Ar-I/I passivation the bias-dependence of the capacitance reappeared at 450 °C, while with α-Si passivation, the capacitance remained constant even at 550 °C. Note that the data shown in the inset are not de-embedded, thus, having somewhat lower $C/C_{\rm Ox}$ values.

$= 25\ \mu$m) were fabricated. The test structures were then measured and subsequently annealed in nitrogen N$(_2)$ ambient at 400 °C, 450 °C, 500 °C, and 550 °C, for 30 min with remeasurement after each interval. The MOS-caps were measured at frequencies ranging from 1 kHz to 1 MHz for dc biases between 0 and +30 V by using an HP-4284 LCR meter. Inductors and CPWs were characterized through *S*-parameter measurements up to 30 GHz by using an HP-8110 network analyzer.

III. Results and Discussion

The capacitance–voltage (*C–V*) characteristics of a MOS-cap without any surface passivation (control) and with an Ar-I/I or an α-Si thin-film deposition at 100 kHz after a 400 °C, 30 min anneal are shown in Fig. 1. The considerable impedance of the HRS substrate was subtracted from the measured data by applying a special de-embedding technique [16]. It is obvious from Fig. 1 that the Control showed a typical high-frequency MOS-cap characteristics at 100 kHz, indicating the buildup of a depletion region in inversion regime (substrate bias <9 V), while with the Ar-I/I and the α-Si there was no bias dependence and the capacitances were far lower than the oxide capacitance ($C_{\rm Ox}$; Fig. 1). For the measurement frequencies $\ll$100 kHz a clear low-frequency characteristic was found for the control (not shown). The surface-passivated MOS-caps still did not show any bias dependence, but the capacitance value did increase with lowering of the frequency; for the Ar-I/I device, a value equal to $C_{\rm Ox}$ was reached at the minimum test frequency of 1 kHz (not shown). This indicated that apparently no depletion region was building up in the highly damaged silicon surface region and that the majority carriers could only accumulate directly at the surface at very low test frequencies. Both types of surface passivation were stable up to an anneal temperature of 400 °C (inset Fig. 1). At 450 °C, the high-frequency MOS-cap *C–V* characteristics reappeared for the Ar-I/I case. The α-Si device remained

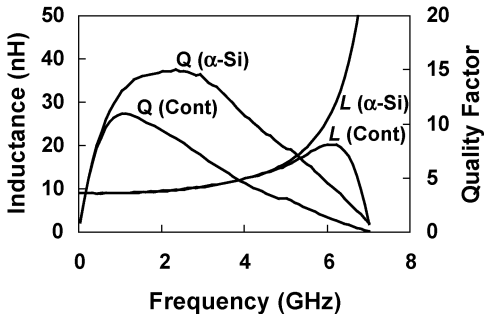

Fig. 2. Inductance and quality factor (Q) of a 10-nH inductor versus frequency on a 3000-$\Omega \cdot$cm substrate without (control) and with (α-Si) surface passivation.

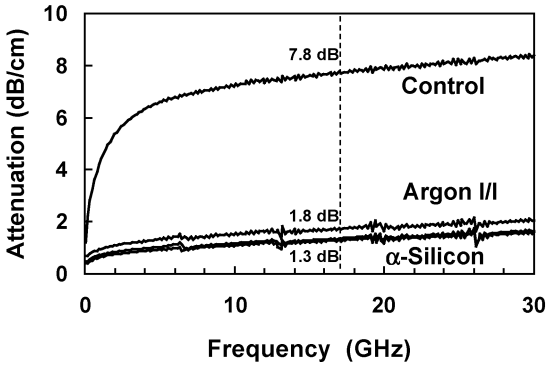

Fig. 3. Attenuation of coplanar wave guides versus frequency on a 3000-$\Omega \cdot$cm substrate without (control) and with (α-Si; Ar-I/I) surface passivation.

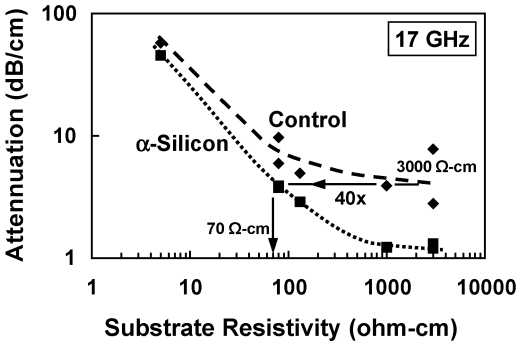

Fig. 4. Attenuation of coplanar wave guides at 17 GHz as a function the substrate resistivity and without (Control) and with (α-Si) surface passivation (data from two experimental runs). It is indicated that the 3000-$\Omega \cdot$ cm silicon Control exhibits an attenuation that is equivalent to a surface-passivated substrate having 70-$\Omega \cdot$ cm resistivity.

bias-independent up to the maximum annealing temperature of 550 °C. Higher anneal temperatures could not be evaluated because of melting of the Al contacts near 600 °C.

The fact that the α-Si passivation was successful in preventing the formation of a conductive channel at the silicon surface led to a substantial increase in inductor-Q by $\sim$40% (Fig. 2). For the CPWs, the effect of surface passivation was even more pronounced (Fig. 3). The application of the Ar-I/I led to a 6.0-dB lower attenuation at 17 GHz, while another 0.5-dB reduction was achieved with using the α-Si passivation layer. Fig. 4 shows the attenuation losses of CPWs built on silicon substrates and having resistivities in the range of 5–3000 $\Omega \cdot$cm with and without α-Si passivation at 17 GHz. It is indicated that

a 3000-$\Omega \cdot$cm substrate without any surface passivation exhibits a CPW attenuation that is equivalent to that of a 70-$\Omega \cdot$ cm passivated substrate. Besides, the data spread was much smaller with the surface passivation compared to the untreated HRS.

IV. Conclusion

Surface-passivated HRS, having minimum losses, a high permittivity, and a high thermal conductivity, qualifies as a close-to-ideal RF and microwave substrate. Passivation can be achieved through amorphization of the silicon surface in order to prohibit the buildup of a conductive surface channel. Amorphization through the deposition of a thin amorphous silicon film is superior to amorphization by argon implantation in terms of loss reduction and stability in post annealing. The demonstrated stability of the surface passivation after an annealing temperature up to 550 °C is more than sufficient to make high-resistivity silicon passivation by amorphous silicon deposition applicable to RFIC process technology prior to the backend processing.

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