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Loss evaluation of GaN GIT in a high frequency boost converter in different operation modes

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Summary

In this paper, losses in a 600V Gallium Nitride (GaN) Gate Injection Transistor (GIT) were evaluated in different operation modes of a boost converter. Analytical loss model of GaN GIT, in which circuit and package parasitics are accounted for, was developed to assist the evaluation. Losses in GIT were assessed in a boost converter using the model and the results showed that: in Continuous Conduction Mode (CCM) and Boundary Conduction Mode (BCM), turn-on loss, mainly originated from discharging of transistor output capacitance, dominates in GIT; in Boundary Conduction Mode with Valley Switching (BCM-VS), where transistor is switched on with reduced voltage and zero current, turn-on loss can be greatly reduced. In BCM-VS, where turn-off current is higher than CCM and BCM, turn-off loss dominates as C_{gd} is large and the ratio between C_{ds} and C_{gd} is small in low voltage range. Experiments were performed to validate the loss model at both 100kHz and 1MHz as well as to prove and demonstrate the loss analysis.

1. Introduction

High frequency power conversion is an ongoing trend in power electronics. To achieve high frequency operation while maintaining high efficiency, suitable switching devices are required. GaN power semiconductors, resulting from their material properties, have faster switching speed than Silicon (Si) counterparts and are recognized as one of the good candidates to replace Si devices [1][2]. Up to date, performances of different types of GaN HEMTs were evaluated, and the results showed that GaN HEMTs are promising for high frequency applications under soft turn-on conditions [3][4].

In this paper, losses in a new type of GaN transistor, GaN GIT from Panasonic, are evaluated in a boost converter. Analytical loss model of GIT is developed as a tool to predict transistor losses when it is operated in different modes i.e. different switching conditions. Experimental measurements are conducted to validate the model and to prove the analysis.

2. Loss modeling and analysis of GaN GIT in a boost converter

2.1 Analytical loss modeling of GaN GIT in a boost converter

To evaluate performances of GaN GIT, loss modeling of the device is needed. Loss models of GaN HEMTs had been well developed, whereas loss modeling of GaN GIT, to our knowledge, has not been performed. In this paper, losses in GaN GIT is modeled and analyzed in a boost converter. Unlike the approach recommended by Panasonic, GIT is drove with no auxiliary circuit in gate loop in this paper [5].

2.1.1 Loss modeling approach

An equivalent circuit of a GaN GIT based boost converter that includes circuit and package parasitic inductances (drain inductance L_d, gate inductance L_g and common source inductance between gate loop and switching loop L_s) as well as parasitic capacitances (parasitic capacitances of the transistor: C_{gd}, C_{gs} and C_{ds}) that has been proved to have major effects on transistor switching characteristics in a diode-clamped, inductive load switching circuits [3][6][7] is shown in Fig 1. It should be noted that L_d consists of inductance of transistor package at drain terminal L_{d-GIT} and inductance of PCB at drain side L_{d-PCB}, and so does L_g and L_s. Inductance in the rest part of commutation loop (lumped as L_D) and mutual inductances between different leads of GIT ($M_{gs,}$ M_{gd}, M_{ds}) are also included. Nonlinear properties of C_{gd} and C_{ds} in GIT and C_D in the freewheeling diode are accounted for. Reverse recovery effect of the freewheeling diode is not considered as it is avoided in some operation modes (e.g. BCM and BCM-VS) and, in the mode (e.g. CCM) where the effect is critical, Silicon Carbide (SiC) diode that has no reverse recovery charge, will be used.

2.1.2 Loss modeling of GaN GIT in a boost converter in CCM

Switching transients of GaN GIT are divided into different stages and sub-stages, as characterized

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for switching behaviors of both GaN HEMTs and Si MOSFET [3][4][6][7]. Values of parasitic elements are modeled differently according to the conditions such as v_{ds} variation range, current direction in GaN GIT package leads, etc. in each single stage or substage.

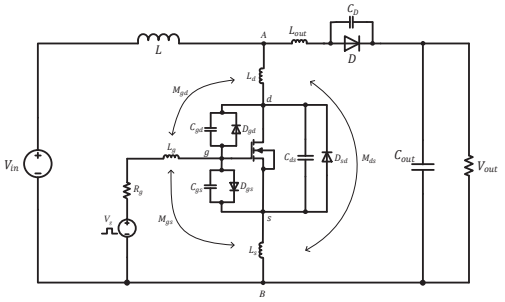

Fig.1 GaN GIT based boost converter with circuit and package parasitics

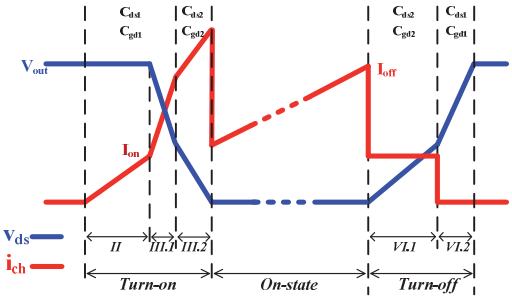

Fig. 2 GaN GIT switching waveform

$$C_{ds1} = C_{ds(V_{out})},\ C_{gd1} = C_{gd(V_{out})},\ C_{D2} = C_{D(V_{out})}$$

$$C_{ds2} = \frac{C_{ds(V_{out})} + C_{ds(R_{ds-on}I_{on})}}{2},\ C_{gd2} = \frac{C_{gd(V_{out})} + C_{gd(R_{ds-on}I_{on})}}{2}$$

$$C_{D1} = \frac{C_{D(V_{out})} + C_{D(0)}}{2}$$

A. Turn-on transient

Stage I Turn-on delay

When gate voltage V_g is initiated, the resulting gate current in the gate loop starts to charge the input capacitance C_{gs} and C_{gd}. As C_{gs} is usually much larger than C_{gd} when v_{ds} is high, it is assumed that only C_{gs} is charged in this stage [3][6]. Before transistor threshold voltage V_{th} is reached, status of power stage doesn't change, and therefore no power loss is generated in GaN GIT. At the end of this stage, V_{gs} equals V_{th}.

Stage II Channel current rise

Once V_{th} is reached, channel of the GIT becomes conductive, GIT operates in saturation region as as $v_{ds} > v_{gs} - V_{th}$. Therefore, maximum current the channel can conduct is determined by v_{gs}. Due to time-changing current that flows in the commutation loop, voltage drop on parasitic inductances will be induced, affecting v_{ds} and losses in the transistor.

$$i_{ch-ir}(t) = i_{L_d}(t) - i_{C_{ds}}(t) - i_{C_{dg}}(t) \quad (1)$$

$$i_{ch-ir}(t) = g_{fs}(v_{gs}(t) - V_{th}) \quad (2)$$

By solving the equations from both gate loop and commutation loop, values of transistor channel current and voltage on the transistor i.e. instant power loss in GaN GIT can be obtained, though the expressions are quite complex. In this paper, channel current is considered as equal to drain terminal current $i_{L_d}(t)$ in this stage; variation of $v_{ds}$is accounted for by adding loss of discharging GaN GIT output capacitance. At the end of this stage, transistor channel takes over the whole load current I_{on} and voltage on GIT is $V_{ds\,(t_{ir})}$. Switching loss in this stage is modeled as:

$$P_{ir} = f_{sw}\int_0^{t_{ir}} v_{ds}(t) i_{Ld}(t)dt + \frac{C_{ds1}+C_{gd1}}{2}\left(V_{out}^2 - V_{ds(t_{ir})}^2\right)f_{sw} \quad (3)$$

Where t_{ir} denotes current rise time and f_{sw} is the operation frequency of the converter.

Stage III Voltage fall

After GaN GIT has taken over I_{on} , the freewheeling diode stops conducting and blocks output voltage V_{out}. Voltage on transistor starts to fall, C_{ds} and C_{gd} get discharged through transistor channel. As GIT is still working in saturation region, the current through GIT channel is still controlled by v_{gs}. As indicated from datasheet of GIT, values of C_{gd} and C_{ds} are almost constant when v_{ds} is greater than 255 V. Below 255 V, however, both capacitances values vary with v_{ds} , andC_{gd} varies dramatically. To more accurately model loss, this stage is divided into two substages according to the value of v_{ds}.

Substage III.1 High voltage range

As drain current is constant (I_{on}), $M_{gd}$and M_{ds} are modelled as zero. Rearranging equations for *Stage II* with modifications on values of channel current and mutual inductances, expressions of channel current $i_{ch-vf1}(t)$ and drain source voltage $v_{ds-vf1(t)}$ can be obtained. This stage ends when v_{ds} drops from $V_{ds(t_{ir})}$ to 255 V by the time t_{vf1}. Loss in this stage is modelled as

$$P_{vf1} = f_{sw}\int_0^{t_{vf1}} v_{ds-vf1(t)} i_{ch-vf1}(t)dt \quad (4)$$

Substage III.2 Low voltage range

In low v_{ds} range, nonlinearity of parasitic capacitances should be accounted for. The relationships between capacitance values and v_{ds} can be modeled through curve fitting to find polynomial expressions of C_{gd} and C_{ds} as functions of v_{ds}. Although this approach could result in accurate calculation of loss, as C_{gd} and C_{ds} are coupled with the time changing v_{ds}, it usually ends up with complex equations and

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therefore calls for simplifications [4]. In this work, average values of C_{gd} and C_{ds} are used to account for nonlinearity of the capacitances.

After a fall time of t_{vf2}, v_{ds} decrease to $R_{ds-on}I_{on}$ and this stage ends. Expressions of channel current $i_{ch-vf2}(t)$ and voltage $v_{ds-vf2}(t)$ can be obtained by substituting values of C_{gd} and C_{ds} with C_{gd2} and C_{ds2}, replacing i_{L_d} with I_{on} and, as drain current is constant, setting M_{gd}, M_{ds} to zero in equations in previous stage. Loss in GIT in this substage:

$$P_{vf2} = f_{sw}\int_0^{t_{vf2}} v_{ds-vf2}(t)i_{ch-vf2}(t)dt \quad (5)$$

Parasitic capacitance of the freewheeling diode will be charged during transistor voltage fall and the corresponding current will flow through transistor channel. The displacement-current induced loss is accounted for by:

$$P_{C_D-dis} = \frac{Q_{V_{out}}V_{out}}{2}f_{sw} \quad (6)$$

$Q_{V_{out}}$ is the charge needed to build potential across the diode up to V_{out} and value of $Q_{V_{out}}$ can be obtained from diode datasheet. After v_{ds} drops to $R_{ds-on}I_{on}$, v_{gs} continues to increase and, as gate–source characteristics is modeled as a capacitor in parallel with a diode (forward voltage V_{gsD}, on–state resistance R_{gsD}), final value of v_{gs} is determined by:

$$V_{gson} = V_{gsD} + \frac{V_g - V_{gsD}}{R_{gon}+R_{gsD}}R_{gsD} \quad (7)$$

Because of the large transconductance g_{fs} of the transistor, the gate–source diode illustrated in Fig. 1, will not conduct during switching transient until the channel current reaches about 40A. And thus, the effect of gate–source diode on turn-on loss is not considered in this paper.

B. Turn-off transient

Stage V Turn-off delay

When V_g starts decreasing, C_{gs} and C_{gd} are discharged and turn-off transient starts. As v_{gs} will firstly drop to V_{gsD} under the influence of gate–source diode and then falls without the effects of the diode, two substages exist.

Substage V.1 Gate–source diode in on-state

In this substage, gate source voltage drops from V_{gson} to V_{gsD} by the time t_{offd1}.

$$i_{gs}(t) = C_{gs}\frac{dv_{gs}(t)}{dt} + \frac{V_g - V_{gsD}}{R_{gsD}} \quad (8)$$

Substage V.2 Gate–source diode in off-state

After the gate–source diode stops conducting, v_{gs} drops from V_{gsD} to turn-off plateau voltage V_{gs-vr}, with a time duration of t_{offd2}.

As channel current and drain source voltage of GaN GIT remains the same as when transistor is in on-state, this stage can be regarded as an extension of transistor on-state. Power loss in GaN GIT during this stage is estimated as:

$$P_{offdelay} = R_{ds-on}I_{off}^2(t_{offd1} + t_{offd2})f_{sw} \quad (9)$$

Stage VI Voltage rise

Theoretically, after the delay stage, transistor will not enter into saturation region until $v_{ds} > v_{gs} - V_{th}$. Given the fact that GaN GIT has a large g_{fs}, transition time from ohmic region to saturation is neglected [6]. During voltage rise, load current I_{off} splits into four parts: $i_{C_{gd}}$ that charges C_{gd}, which equals the gate current; $i_{C_{ds}}$ that charges C_{ds}, i_{C_D} that charges C_D and i_{ch} that flows through transistor channel. It is assumed that v_{gs} stays constant at V_{gs-vr} in this stage:

$$I_{off} = I_{C_{dg}} + I_{C_{ds}} + I_{ch} + I_{C_D} \quad (10)$$

$$I_{C_{dg}} = C_{gd3}\frac{dv_{dg}(t)}{dt} = \frac{V_{gs-vr}}{R_{goff}} \quad (11)$$

$$I_{ch} = g_{fs}(V_{gs-vr} - V_{gs-th}) \quad (12)$$

V_{gs-vr} is determined by applying values of C_{gd} and C_{ds} when drain source voltage is $R_{ds-on}I_{on}$:

$$C_{ds3} = C_{ds(R_{ds-on}I_{on})},\ C_{gd3} = C_{gd(R_{ds-on}I_{on})}$$

As discussed in *Stage III*, values of parasitic capacitors in GaN GIT show different characteristics below and above 255 V of v_{ds}. To account for this effect, this stage is separated into two substages as well.

Substage VI.1 Low voltage range

In low voltage range, averaged capacitance values are used:

$$v_{ds-vr1}(t) = \frac{V_{gs-vr}}{R_{goff}C_{gd2}}t \quad (13)$$

$$I_{ch-vr1} = \begin{cases} I_{off} - \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds2}+C_{D2}}{C_{gd2}}\right), & I_{off} > \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds2}+C_{D2}}{C_{gd2}}\right) \\ 0, & I_{off} \le \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds2}+C_{D2}}{C_{gd2}}\right) \end{cases} \quad (14)$$

This stage ends when v_{ds} reaches 255 V. Loss generated in GIT in this substage is calculated as:

$$P_{vr1} = f_{sw}\int_0^{t_{vr1}} v_{ds-vr1}(t)I_{ch-vr1}dt \quad (15)$$

t_{vr1} stands for the time needed in this substage.

Substage VI.2 High voltage range

In high voltage range, $v_{ds-vr2}(t)$ varies different with time than its counterpart in low voltage range and the value of channel current I_{ch-vr2} is also not the same as I_{ch-vr1}. Expressions of I_{ch-vr2} and $v_{ds-vr2}(t)$ can be obtained by substituting C_{gd2}, C_{ds2} and C_{D2}, in (13) and (14) with C_{gd1}, C_{ds1} and C_{D1} respectively. After a time of t_{vr2}, v_{ds} reaches V_{out}. Loss occurred in GaN GIT during this stage can be expressed as:

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$$P_{vr2} = f_{sw}\int_0^{t_{vr2}} v_{ds-vr2}(t) I_{ch-vr2} dt \quad (16)$$

Stage VII Drain current fall

After v_{ds} increased up to V_{out}, diode begins to conduct, load current commutes from transistor to diode. Analytical loss modeling approach of GaN GIT in this stage is the same as the modeling of corresponding stage of GaN HEMT in [3]. It should be noted that during drain current fall, considering the current directions in this stage, coupling coefficients are different from the values in turn-on transient.

C. Conduction loss

Apart from the switching losses, there is also conduction loss, which is generated during GaN GIT on stage

$$P_{cond} = I_{rms-on}^2 R_{ds-on} \quad (17)$$

In case of reverse conduction, loss can be estimated as

$$P_{cond-rev} = f_{sw}\int_0^{t_{rev}} v_{ds-rev}(t) i_{Ld-rev}(t) dt \quad (18)$$

Where v_{ds-rev} and i_{Ld-rev} are voltage on and current though the transistor, respectively. And t_{rev} is the duration of reverse conduction.

2.2 Operation modes in a boost converter

Apart from the commonly seen operation modes of a boost converter, CCM, DCM and BCM, a mode of so-called BCM-VS, which is commonly used in PFC boost converters, also exists [9]-[11]. As explained in detail in [3], in BCM-VS, transistor will be switched on at reduced voltages with Zero current (ZCS) and therefore turn-on loss can be minimized.

Different switching conditions for GIT are enabled by operating the GIT based boost converter in different modes: in CCM, turn-on process is hard switching; in BCM, ZCS turn-on can be achieved, the effect of turn-on current on turn-on loss is excluded; in BCM-VS, ZCS turn-on can be maintained while the voltage across the switch is at a low value (or even zero).

2.3 Loss analysis of GaN GIT in different operation modes

2.3.1 Loss breakdown and analysis

Utilizing the developed model, losses in GaN GIT were analysed in three different operation modes at 1MHz, with an output voltage of 400V and a power of 300W with the specifications detailed in Table III in a boost converter. As illustrated in Fig. 3: in CCM, turn-on loss dominates (99.4%), while turn-off loss is zero; in BCM, where turn-on loss is caused only by discharging transistor output capacitance, turn-on loss still dominates (73.2%), turn-off loss contributes 25.8% to total loss; in BCM-VS I (V_{out}<2V_{in}), where GIT will be switched on with ZCS at 120V and turned off with similar current as BCM, turn-on loss is greatly reduced while turn-off dominates (70.5%); in BCM-VS II (V_{out}>2V_{in}), where GIT is to be switched on with ZCS and negligible voltage, turn-off loss is up to 94.4% of total loss; conduction losses are low in all modes resulting from the low on-state resistance of less than 0.1Ω.

Table I. Specifications and losses in the boost converter in different modes

Mode	v_{in}(V)	I_{on}(A)	I_{off}(A)	Loss (W)
CCM	200	1.35	1.65	12.33
BCM	200	0	3	10.98
BCM-VS I	260	0	3.2	4.66
BCM-VS II	120	0	6.6	10.76

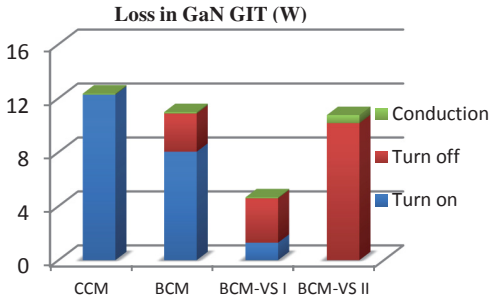

Fig. 3 Loss breakdown of GIT in different modes

The results of loss breakdown indicate that: in CCM and BCM, turn-on loss dominates in GaN resulting from the discharging of the large output capacitance of the transistor; in BCM-VS I and BCM-VS II, where transistor is to be switched on at reduced voltage and switched off with higher current, turn-off loss dominates. The high turn-off loss is due to the facts that C_{gd} is large and the ratio between C_{ds} and C_{gd} is small in low voltage range in GIT, which will end up with long voltage rise time and large channel current. Turn off loss, as implied in equations 13 and 14, can be reduced by paralleling external capacitors to GaN GIT, reducing gate resistance R_{g-off} or enforcing negative v_{gs}.

2.3.2 Effects of parasitic inductances on switching loss

Effects of parasitic inductances on switching loss of GaN GIT depend greatly on operation modes the transistor is working in. In BCM, BCM-VS I

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and BCM-VS II, where GaN GIT is switched on with ZCS, parasitic inductances has no effects on turn-on loss. As implied by (14), loss will be generated in substage *VI.1* if there's current in GIT channel. As the ratio between C_{ds} and C_{gd} increases up to a value of 70 after V_{ds} exceeds 255V, no channel current will be present unless the turn-off current is larger than 49.3A in substage *VI.2*. And therefore, turn-off loss is not influenced by parasitic inductances.

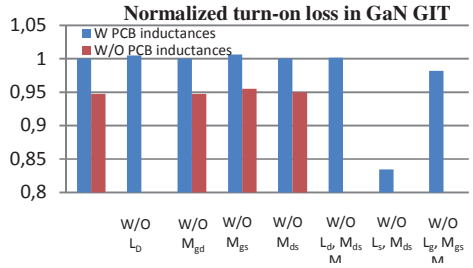

Fig.4 Effects of parasitic inductances in CCM on turn-on loss

The effects of different parasitic inductances on turn-on loss in CCM are demonstrated in Fig. 4. L_s has the largest influence on turn-on loss in CCM because it behaves as a negative feedback between gate loop and switching loop and thus slows down switching transients. L_D , $L_d$and M_{ds} lower turn-on loss by reducing the value of v_{ds}. During turn-on, the presence of L_g increases turn-on loss, which differs from the conclusion that L_g affects only delay times but not loss in [6]. Coupling effect between gate and source (M_{gs}) helps to reduce effective inductances in common source and gate, and decrease turn-on loss thereof. Apart from L_g, the rest parasitic inductances have limited effects on turn-on loss.

The effects of mutual inductances on turn-on loss are further illustrated by considering only package inductances i.e. setting values of L_{d-PCB} , L_{s-PCB} , and L_{g-PCB} to zero. The influences of mutual inductances are enhanced although still limited. For instance, when PCB inductances present, existence of M_{gs} and M_{ds} would reduce 0.64% and 0.08% of turn-on loss, respectively, while when there's no PCB inductances on drain, source and gate exist, the values grows to 7.84% and 2.59%, respectively.

3. Experimental results

A 300W boost converter prototype is built to perform loss model validation and assess losses in GaN GIT in different operation modes. Losses in GIT are measured thermally. The effects of diode on transistor temperature may be excluded by proper layout i.e. putting the diode physically away from the transistor; while the effect of driver on transistor temperature can be omitted as losses in the driver was negligible given the low driving voltage of 4V and the fact that GIT requires only 8 nC to be fully on. Experimental verifications were performed and confirmed that both diode and driver have negligible contribution to temperature increase of GIT. A lookup table that calibrates relationship between loss and temperature increase in GIT was made by injecting different values of DC current into GIT when it is kept in on-state. With help of the look-up table. losses in GIT are quantified.

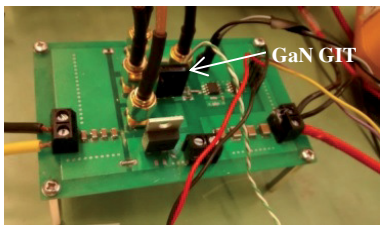

Fig.5 Converter prototype employing GaN GIT

3.1 Loss model validation

The loss model was validated experimentally in CCM at 100 kHz. The validations were performed using the prototype shown in Fig.5 with the specifications detailed in Table II. Circuit and package parasitic inductances were calculated by PEEC (Partial Element Equivalent Circuit) tool and values of parasitic capacitances of the transistor were extracted from transistor datasheet. SiC Schottky diode was used to eliminate boost diode's reverse recovery current. As indicated in Fig. 6, the modelled loss agreed well with measurement results.

Table II. Values of parasitic elements

Parasitics		Values	Parasitics		Values
L_d	L_{d-PCB}	1.40nH	L_s	L_{s-PCB}	1.97nH
	L_{d-GIT}	1.73nH		L_{s-GIT}	1.81nH
L_g	L_{g-PCB}	2.64nH	C_{gd1}		1.1pF
	L_{g-GIT}	1.81nH	C_{gd2}		22.1pF
M_{gs}		0.29nH	C_{gd3}		43pF
M_{gd}		0.54nH	C_{ds1}		70pF
M_{ds}		0.54nH	C_{ds2}		145pF
L_D		9.87nH	C_{ds3}		220pF
C_{gs}		270pF	C_{D1}		27pF
Q_{out}		5nC	C_{D2}		12pF

Table III. Specifications of converter test points

P_{out}(W)	v_{out}(V)	I_{on}(A)	I_{off}(A)
20	100	0.35	0.44
45	150	0.51	0.65
75	200	0.70	0.88

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120	250	0.87	1.09
170	300	1.04	1.31
230	350	1.20	1.52
300	400	1.40	1.70

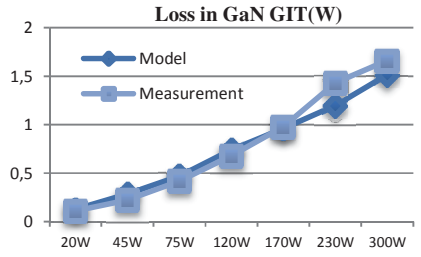

Fig. 6 Measured and calculated (modeled) loss in GaN GIT

3.2 Loss evaluation of GIT at 1 MHz in different operation modes

In CCM, GaN GIT is hard switched in both turn-on and turn-off with low currents, measured loss is 11.9W. In BCM, the transistor is switched on with ZCS and off with higher current than CCM, loss is measured as 11W. In BCM-VS I and BCM-VS II, ZCS turn-on are maintained while turn-on voltages are reduced and turn-off currents are larger than BCM, losses in GaN GIT are measured as 4.5W and 9.8W, respectively. Measurement results agree well with the analysis in Section 3.2.1, although there are deviations in values. The measured and calculated loss of GaN GIT at 1MHz also proved that the model can predict loss in GaN GIT with satisfactory accuracy. Deviations originate mainly from measurement errors and inaccurate modeling of capacitance during turn-off.

4. Conclusions

In this paper, loss model of a 600V GaN GIT was developed. Losses in GIT were then evaluated in a boost converter in three different operation modes-CCM, BCM and BCM-VS utilizing the loss model. It is shown that in CCM and BCM, turn-on loss dominates originating from discharging of the large output capacitance. In BCM-VS, where GIT is switched on with lowered voltage, turn on loss can be greatly reduced. It was revealed that the ratio of C_{ds}/C_{gd}, which affect turn-off loss, is low in GaN GIT in low v_{ds} range (below 255V) and therefore, in BCM (with high current) and in BCM-VS, where turn-off current is much larger than CCM, turn-off loss dominates. Given these facts, losses in BCM-VS can be reduced by improving driving circuit (e.g. adding auxiliary circuits) or paralleling external capacitors to drain-source of GIT. As with CCM and BCM (with low current), reduction of the parasitic capacitance e.g. die shrinking is needed to decrease the loss. Conduction is low in all modes resulting from the low on-state resistance of GaN GIT. Experiments were performed to validate the loss mode and to prove the analysis.

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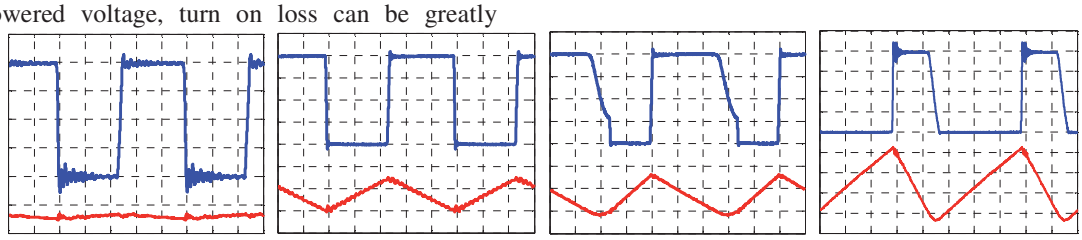

(a) (b) (c) (d)

Fig. 7 Measurement results: (a) CCM; (b) BCM; (c) BCM-VS I (V_{out}<2V_{in}); (d) BCM-VS II (V_{out}>2V_{in})
(V_{ds}: 200V/Div; i_L: 2A/Div; time: 200ns/Div

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