TU Delft

FM modulator and demodulator design

As part of a wireless FM Tranceiver

By

Jasper van Vliet
Gilbert Hardeman

in partial fulfillment of the requirements for the degree of

Bachelor of Science
In Electrical Engineering

Supervisors:
dr. M. Alavi,
dr. M. Babaie,
ing. M. Pelk

21 July 2019

DELFT UNIVERSITY OF TECHNOLOGY

FACULTY OF ELECTRICAL ENGINEERING, MATHEMATICS
AND COMPUTER SCIENCE

ELECTRICAL ENGINEERING PROGRAMME

Abstract

This report details the design and implementation of subsystems within a wireless FM transceiver. All the subsystems will be developed and integrated into a working FM transceiver. The subsystems discussed in this report are the modulator and demodulator. The modulator, on the transmitter side, varies the carrier wave frequency, based on the input audio signal. The demodulator, on the receiver side, can detect these variations and retrieve the audio signal.

The modulator is implemented using a voltage controlled oscillator, which is based on the Colpitts oscillator. The input audio signal controls the oscillation frequency by modulating varicaps. The demodulator consists of mixer, amplifier and a slope detector. The amplifier is not discussed in this thesis. The mixer uses a local oscillator to shift the RF input signal to an intermediate frequency. This thesis proposes a mixer integrated into a local oscillator, using only one transistor. The detector is based on a slope detector, which differentiates the FM signal and converts it into an AM signal. The differentiator is implemented using a bandpass filter. The audio signal is retrieved from the AM signal using an envelope detector.

The work will be concluded with a display of the complete FM transceiver circuit.

Preface and acknowledgements

The past 8 weeks have surely been a fitting end to a challenging but very rewarding education. After years of training we enjoyed the increased freedom we had during this project. Defining the requirements ourselves, finding solutions. We think the field of electronic design requires exceptional engineering ingenuity, this experience will surely benefit us during the rest of our careers.

That being said, the project was also designed to confront us with a lot of advanced theoretical concepts. For this we want to thank our our project proposer dr. S.M. Alavi in particular. Furthermore, we want to thank dr. S.M. Alavi, ing. M. Pelk and dr. M. Babaie for their insightfull comments during our, sometimes hours long, weekely meetings. Perhaps the greatest help during this project was the open door policy of dr. S.M. Alavi and ing. M. Pelk. They were always happy to help, and we think we might have learned the most in our visits to them. For this we want to state our utmost gratitude.

We look forward to the final phase that follows now. The remaining time until the defence, we will spend in the lab, validating the design.

We hope you enjoy reading about our journey as much as we did experiencing it.

Jasper van Vliet
Gilbert Hardeman
Delft, June 2019

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1 Introduction

Over the last decades wireless technologies have become ubiquitous. The revolution was started by exceptional intellectual people such as James Clerk Maxwell, Heinrich Hertz, Guglielmo Marconi and more. There was a rapid developments of these technologies during WWI and WWII. As a result, the radio was brought to the public.
Technological advances have brought us to a world where everyone has a device in their pocket that is able to connect to multiple satellites. The ever-increasing demand for higher data-rates, the push towards the Internet of Things (IoT) and more people getting access to technology, will continue to drive growth in the wireless technology sector. The goal of this bachelor project is to build an FM transmitter and receiver from *only* discrete components. This basic wireless system makes use of the fundamental ideas applied in modern wireless systems.

1.1 A standard wireless system

The frequencies of the signals coming from the information source are generally not suitable for wireless transmission. To cope with this, the information is modulated onto a carrier wave. After the information is modulated, the transmitter will amplify the signal to get the required power at the antenna. The antenna transmits the signal through the wireless signal.
When the signal reaches the receiver, it will be attenuated, so the first step is to amplify the signal again. Since the received signal is in the order of μV, it is of particular importance to add as little noise as possible in this amplifier. After amplification, the signal is demodulated to obtain the original information signal. Depending on the power of the information signal and the required input of modulator there could be more amplification needed between the information source and modulator. Similarly, depending on the required output signal and the output of the demodulator, there could be amplification needed after the demodulator.

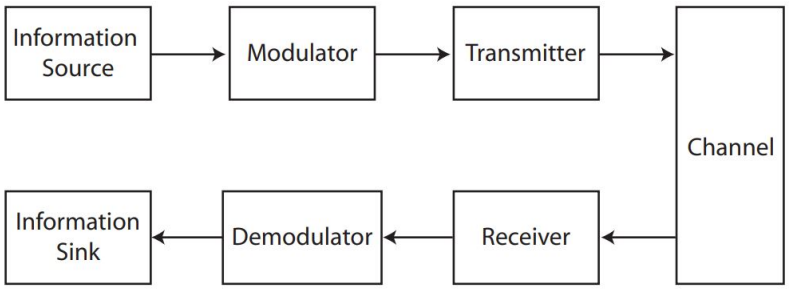


Figure 1.1: A standard wireless communication system

1.2 Project goal and division

Where the capabilities and specific implementations of wireless technologies has evolved over time, the basic building blocks of a wireless communication system have largely stayed the same. To acquire a deeper understanding of these basic building blocks, an Electrical Engineering Bachelor Graduation Project was set up. The goal of the project is to go through the complete design of a FM transceiver, hereby gaining fundamental knowledge on the design of wireless systems.
The goal of this project is reached by using only discrete components such as capacitors, inductors, resistors and transistors. This project also contributes to the knowledge of modern wireless systems, since modern modulation techniques have some resemblance with AM, FM or both modulation types. Frequency modulation specifically, is closely related to frequency shift keying (FSK), which is used in modern protocols

such as Bluetooth. FM technology is also applied in frequency modulated continuous wave (FMCW) radar.

The division of a communication system into basic building blocks lends itself naturally to a group-project in which the group is divided into subgroups, where each subgroup is responsible for a part of the overall design. The six students of this project are divided into groups of two. The proposed system and its division is shown in Fig. 1.2.
One team is responsible for the design of the first and last amplification stage of the whole transceiver, indicated by yellow. A second team is responsible for the amplifier stages just before transmission and directly after receiving the signal, indicated by blue. The final team is responsible for the modulation and demodulation of the signal. The modulation and demodulation are the topics of this thesis.
This thesis will cover the design and validation of these circuits assisted by simulation and measurement results. The design and simulation of the system will be done using Keysight Advanced Design System 2019 (ADS). This is a widely used software package in RF electronics.
The main goal for this project is to have a working system, because of the limited time for this project, often the simplest solution for a problem will be chosen. At the moment, thesis delivery, the project is at the stage of testing the subsystems that are made per subgroup. The following nine days until the thesis defence will be spend integrating the components into the final system.

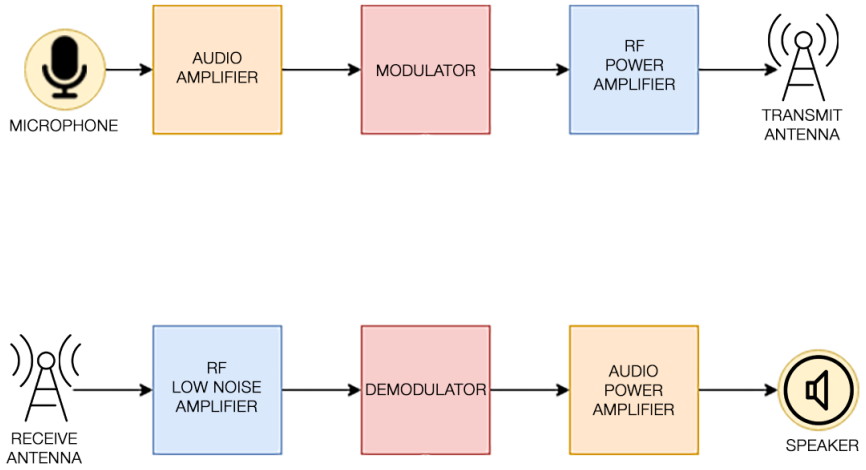


Figure 1.2: Overview of the proposed system

1.3 State-of-the-art analysis

The world is entering an era where billions of objects can sense, communicate and share information through networks [1]. The IoT devices used for tracking and monitoring are small chips with minimal processing capabilities. Typically GSM, GPRS, LTE, ZigBee, WiFi and Mesh Network are used for communication while RFID, NFC, GNSS and BLE are employed for tracking [2]. Research is going into building transceivers that can function with multiple of these protocols [3].

As the number of devices grows, so does the demand for bandwidth. Thus research is going into modulation techniques that are efficient in their use of bandwidth. Modulation techniques based on frequency-shift keying (FSK) are widely used in wireless communication [4]. Bluetooth makes use of a modified version of FSK, namely gaussian frequency shift keying (GFSK). GFSK passes the baseband signal through a gaussian filter before the signal is modulated, resulting in smoother transitions.

To benefit from the scaling of digital circuits, wireless transceivers are increasingly digital. These can outperform state-of-the art traditional transceivers [5]. Implementing traditional RF circuits in increasingly

more advanced CMOS would make its performance increasingly worse [6].

The circuits that implement the modern modulation schemes have some critical building blocks. A recurring, enabling building block is the Phased Locked Loop (PLL). This block creates a signal that is in phase with the input signal. The PLL can obtain the information of the frequency and the phase of the input signal precisely. So it can be used to track and lock an input signal for synchronising the frequency and phase of an output signal with the input signal [7].

1.4 Thesis synopsis

The introduction explains the relevance of the project and states the goals. In chapter 2 the requirements are stated and motivated. In chapter 3, the modulator will be elaborated on. It starts with a high level functional description of the modulator. After that, there will be a section about the oscillator, vital for the design of the modulator. Next is the extension of the oscillator into a voltage controlled oscillator. With elaboration on the design choices, simulation results and the measurement setup. Next, chapter 4, is about the demodulator. It comprises the mixer, detector, and an explanation of a superheterodyne receiver. The introduction of the chapter is a high level description of the function and discussion of possible implementations. This followed by the design process and simulation results, as well as the discussion of the measurement setup. Finally, chapter 5 contains the conclusions. The conclusion will reflect on the achieved specifications and show the complete FM transceiver circuit.

2 Program of Requirements

As explained in the introduction, the main goal of this bachelor end project is to develop a working wireless communication system. This chapter will first state the requirements of the overall system. The described system requirements are used to specify requirements for the various subblocks. In this report we focus on the modulator and demodulator, because of that, more specific requirements for those subblocks are included. The requirements of the subblocks are made in close communication with the group members that design the interfacing subblocks.

2.1 Overall system requirements

The overall system requirements divided into mandatory requirements and trade-off requirements.

The mandatory requirements are as follows:

- the system must work at a distance of at least 5 meters between transmitter and receiver
- The system must make use of FM
- The system must have a tuneable operating range
- The system must use 12 V as its DC source

The trade-off requirements are as follows:

- The modulated signal should have a bandwidth of 75 kHz
- The system should work with audio signals in the range of 20 Hz-20 kHz
- The system should have equal output signal level in the operating range of 88 MHz-108 MHz

Using FM is a requirement defined by the supervisor. The required 5 meter distance between transmitter and receiver, is a key performance indicator, set by the supervisor. The tunable operating range extends the useability of the system, and it adds a technical challenge. The 12 V source is chosen because group members that design amplifiers need this. As we will all use the same DC source, we need to design our blocks for 12 V as well. The requirement of the variable operating range in the range of 88 MHz-108 MHz, is in line with FM broadcast standards throughout the world. Similarly, the bandwidth of 75 kHz is in line with FM broadcast standards. The audio range of 20 Hz-20kHz, is based on the human hearing range.

2.2 Requirements modulator

- Unwanted frequency component should be at least 20dB weaker than the wanted frequency component
- The output voltage swing must exceed 5 V
- The output signal level should not vary by more then 3 V, over the whole tuning range of 88 MHz-108 MHz

Furthermore, all the overall system requirements apply directly to the modulator. The modulator defines the modulation technique, controls the bandwidth and operating range.

2.3 Requirements demodulator

For this thesis the demodulator has two critical blocks. Namely a mixer, and a detector.

- The mixer's output must not be weaker than its input, coming from the LNA
- The detector's output must have an output swing of at least 20 mV

2.4 Practical considerations

A practical requirements is that the selected components should have a physical length of at least 1.5mm, to be able to be soldered by hand. The design must be put onto a pcb, since a breadboard would have too much parasitic effects.

3 Modulator

A modulator varies the characteristics of a carrier wave based on an information signal. These variations can be detected on the receiver side, to retrieve the information signal. The reason for using modulation is that information signals are generally not suitable for wireless transmission. An important reason is that the required antenna length is inversely proportional to the frequency of the electromagnetic wave. "For efficient radiation, the antenna needs to be longer than one-tenth of a wavelength" [8]. In this thesis the information signals are audio signals with frequencies in the range of 20 Hz-20 kHz. In Eq. 3.1 the wavelength of a 1 kHz signal is determined to be 300 km, resulting in an antenna length of 30 km. This is impractical, and thus, the need to modulate the information signal onto a higher frequency carrier wave.

$$\lambda = \frac{c}{f_c} = \frac{3 \cdot 10^8 \text{ m/s}}{1 \cdot 10^3 \text{ Hz}} = 300 \text{ km} \tag{3.1}$$

Another important reason is that multiple frequency bands can be used to increase the capacity of the transmission medium. The transmitters can modulate their information signals onto different carrier wave frequencies. This allows multiple sources to transmit a signal in the same medium without interfering with each other.
There are different types of modulation. In amplitude modulation (AM), the modulator varies the amplitude of the carrier wave. In frequency modulation (FM), the modulator varies the frequency of the carrier wave. In digital modulation techniques, the (analog) carrier signal is modulated by a discrete signal which represents a bit-pattern. An example of such modulation technique is FSK, in which a finite number of frequencies are used to represent a number of bits.
In this thesis, the FM modulation technique is used. FM modulated signals are better resistive to noise compared to AM modulated signals, as long as the noise is below a certain threshold. The signal to noise ratio at the output is not affected by amplitude noise, as is with AM modulated signals.

3.1 Functional analysis

For frequency modulation, the instantaneous frequency of the carrier wave is varied based on the amplitude of the input signal. The amplitude of the output of the FM modulator should remain constant. The desired transfer of the modulator is shown in Fig. 3.1. With no input signal the carrier will not be modulated. In the graph, f_{max} and f_{min} correspond to the carrier frequency plus, minus the maximum instantaneous frequency deviation respectively. The slope of the indicated line is the sensitivity of the modulator. This sensitivity needs to be as constant as possible over the whole desired frequency range. The sensitivity is expressed in Hz/V.

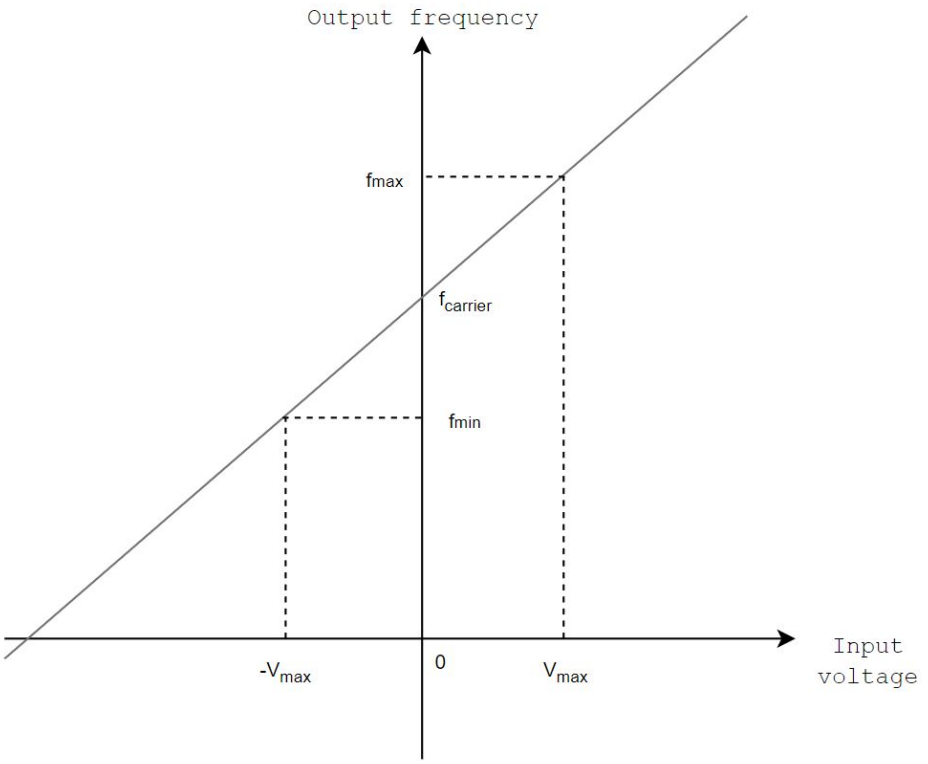


Figure 3.1: FM modulator charactaristic

A simple way to implement a FM modulator is using a voltage controlled oscillator (VCO). A VCO is an oscillator that has components that can change its instantaneous frequency based on an input signal. The variation of the component result in a variation of the oscillation frequency of the VCO. In modern technologies more advanced architectures are used. As an example, a phased-locked loop can be employed for as an FM modulator. The PLL can produce more stable oscillations, compared to just a VCO. The PLL however also has a VCO as a building block. Given the limited time to develop the system, a VCO was chosen to implement the FM Modulator.

3.2 Oscillator analysis

As mentioned in the previous section, the modulator will be implemented using a VCO. The first step towards that, is to develop an oscillator.

An oscillator is a circuit that produces a periodic waveform, using only a DC source and no external input. The oscillation frequency is determined by a resonator. In this project, only LC tank circuit resonators are considered. A parallel LC circuit has a frequency dependant impedance given by Eq. 3.2. For one specific frequency, the effective impedances of the inductor and capacitor are equal but opposite. This will cause the impedance of the LC circuit to go to infinity. This frequency is called the resonance frequency and is given by Eq. 3.3.

$$\frac{1}{j\omega C} \parallel j\omega L = j \cdot \frac{1}{\frac{1}{\omega L} - \omega C} \tag{3.2}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.3}$$

The physical explanation for his phenomenon is that at resonance, the capacitor and inductor are exchanging energy. Hereby drawing no current from an external source. However in a realistic LC network

there are paracitic resistances from the components, causing the oscillation amplitude to decay. To sustain the oscillation, the dissipated energy needs to be compensated for. This can be done using a feedback amplifier.
The feedback amplifier will add a fraction of the output signal back to the input. This function is illustrated in the block scheme of Fig. 3.2. In this block scheme, H(s) represents the filtering that the LC tank implements and the triangular gain block represents the regenerative feedback.

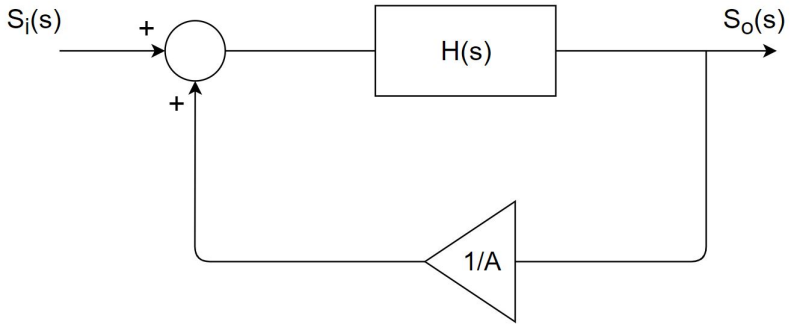


Figure 3.2: Blockscheme of a feedback oscillator

The transfer function of the block scheme is shown in Eq. 3.4. To sustain an oscillation, there are two conditions called the 'Barkhausen criteria'. The first condition of the Barkhausen criteria is that at the desired frequency, the loop gain is equal to one. This means that the losses of the filter are exactly compensated with the provided gain. This condition is shown in Eq. 3.5. The second condition of the Barkhausen criteria is that the total phase shift from input to output is zero, or a multiple of 360 degrees. This means that there is positive feedback. This condition is shown in Eq. 3.6.

$$\frac{S_i}{S_o}(s) = \frac{AH(s)}{A + H(s)} \tag{3.4}$$

$$\left| \frac{AH(s)}{A + H(s)} \right| = 1 \tag{3.5}$$

$$\angle \left\{ \frac{AH(s)}{A + H(s)} \right\} = k \cdot 360° \quad k \in \mathbf{Z} \tag{3.6}$$

The feedback of a fraction of the output can be implemented in different ways. When restricting ourselves to using as few components as possible, there are two possible LC oscillator circuits. The Colpitts oscillator implements the feedback by a capacitive divider. Alternatively, the Hartley oscillator, implements the feedback using a inductive divider. Both these methods implement a purely positive feedback from input to output, satisfying Eq. 3.6. The resulting circuits, disregarding biasing, are shown in Fig. 3.3.

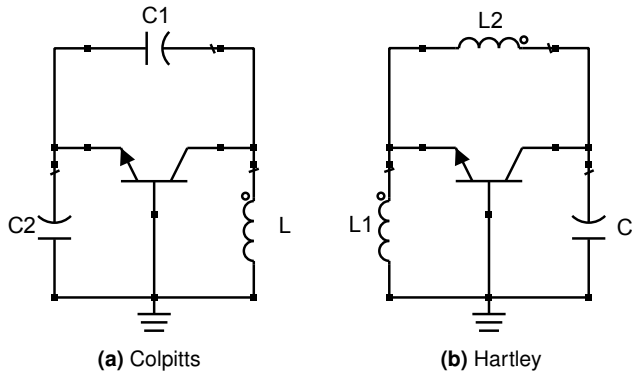


Figure 3.3: Fundamentals Colpitts and Hartley oscillator

For the modulator design, the Colpitts oscillator is chosen, because it has a number of practical advantages. First of all, capacitors are cheaper than inductors. When using inductors care should be taken not to get unwanted coupled inductors, so using capacitors facilitates the design process. Capacitors also generally have a lower series resistance. In figure3.4, a Colpitts oscillator design including biasing for the transistor is shown.

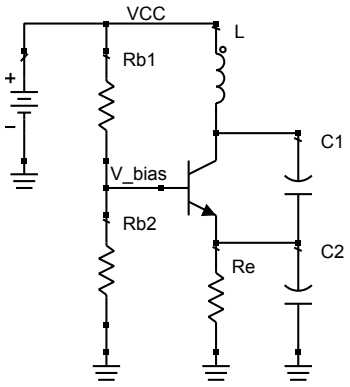


Figure 3.4: Colpitts oscillator including biasing resistors

These oscillator circuits can be build using different types of transistors. The transistors used in this project are bipolar junction transistors (BJT). The advantages of a BJT compared to a field effect transistor (FET) is that the BJT has a higher intrinsic gain. Another advantage is that the BJT does not have a high capacitive input impedance at the base. FET's have the advantage of using low power, however power usage is not the focus of this project. In modern technology, FET transistors have cost benefits, related to integrating transistors on a chip. In this project, only discrete components are used, so the FET is not an option. For the modulator, we chose to use the BFU550A transistor made by NXP. The unity gain frequency (F_t) of this transistor is 11 GHz. This is more than sufficient given our operating frequency of around 100 MHz.

Biasing of the oscillator

The oscillator has no external input. To create the AC output it makes use of the present thermal noise. This noise has a flat spectrum and thus contains all frequencies. The oscillator then amplifies one of the frequencies to create the output. This raises the condition that the oscillator should have enough small signal gain, to start building up the output signal.
The start-up conditions for Colpitts oscillator, as derived in Razavi [9], relate the series resistance of the inductor to the transconductance, capacitor and inductor values, see Eq. 3.7. When the quality factor of the inductor is sufficiently high (Q$\geq$3), the series resistance can be converted to a parallel resistance (R_p),

using the relation shown in Eq. 3.8. The resonant frequency is now determined by the inductor and the capacitors in series, shown in Eq. 3.9. Substituting equation 3.9 and the relation of Eq. 3.8 into equation 3.7, the startup conditions for the oscillator can be stated as Eq. 3.10. These start-up conditions are the disadvantage of simple three-point oscillators. More complex circuits, can have lower requirements on the parallel resistance and transconductance.

$$R_S = \frac{g_m}{C_1 C_2 \omega^2} \tag{3.7}$$

$$\frac{L_1\omega}{R_S} \approx \frac{R_p}{L_1\omega} \tag{3.8}$$

$$\omega_{osc} = \frac{1}{\sqrt{L_1 \frac{C_1 C_2}{C_1+C_2}}} \tag{3.9}$$

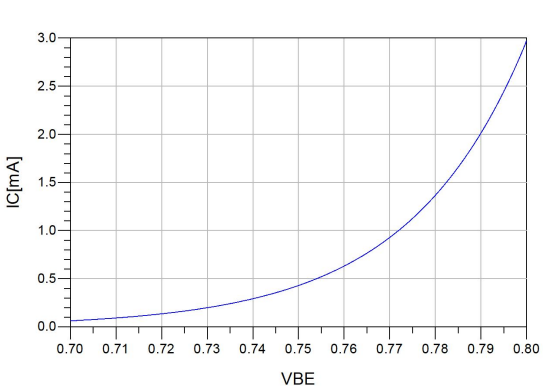
$$g_m R_p \geq \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2 \tag{3.10}$$

As the startup conditions depend on the transconductance, choosing the transconductance is discussed next. The small signal transconductance (g_m) is the derivative of the collector current, with respect to the base emitter voltage. The collector current as a function of the base emitter voltage is shown in Eq. 3.11. The leakage current is disregarded and V_T is the thermal voltage of approximately 25 mV. Equation 3.12 shows that increasing I_C, will increase the transconductance. Figure 3.5 shows the simulated current characteristic. In the real oscillator circuit, the DC base voltage is hold constant, and collector current is set by a resistor, between emitter and ground, it acts as current source. This is resistor R_e in Fig. 3.4. The collector current can be calculated using Eq. 3.13. To determine the bias voltage on the base the simulation of Fig. 3.6 was done. The collector of the transistor will be connected to the output of the oscillator. Because of this, the collector voltage will oscillate. The breakdown voltage of the transistor is around 12 V. To get maximum possible swing on the output the base voltage should be in the middle between where the active region starts, and the breakdown voltage. The base voltage is set by the voltage divider of R_{b1} and R_{b2} in Fig. 3.4

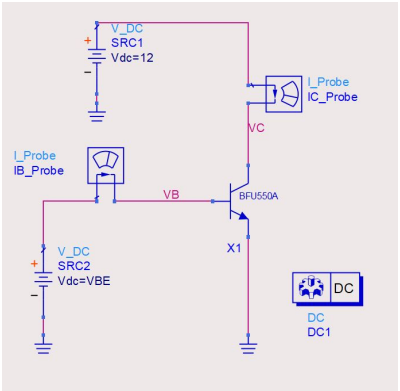
$$I_C = I_0 e^{V_{BE}/V_T} \tag{3.11}$$

$$g_m = \frac{dI_C}{dV_{BE}} = \frac{I_C}{V_T} \tag{3.12}$$

$$I_C = \frac{V_{bias} - V_{BE}}{R_E} \tag{3.13}$$

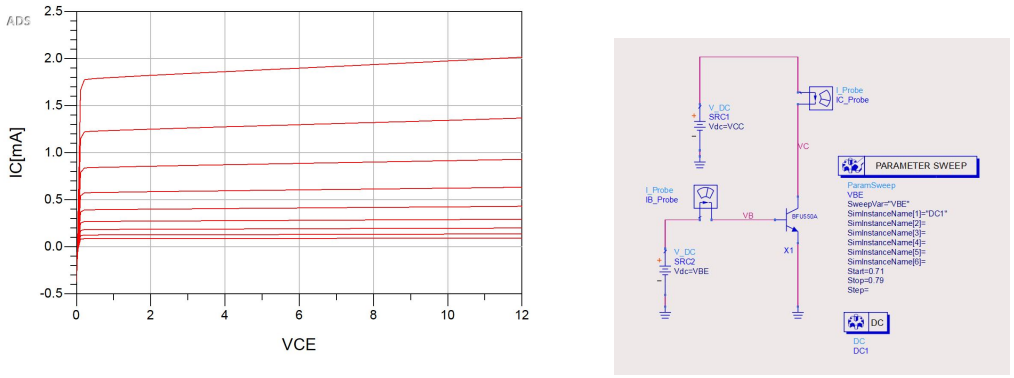


(a) Simulation result



(b) Circuit used

Figure 3.5: Simulated current charactaristic as function of V_{BE}



(a) Simulation result **(b)** Circuit used

Figure 3.6: Simulated current as a function of V_{CE}, using different values of V_{BE}

To find the steady state behaviour of the oscillator we need to consider the large signal transconductance (G_m). Once the oscillator starts building up the output, V_{BE} will become a growing sinusoidal signal. V_{BE} will be equal to the voltage between capacitor C1 and C2, since the base of the transistor is an AC ground. The collector current as a function of a sinusoidal V_{BE} is shown in Eq. 3.14.

$$I_C = I_0 e^{\frac{V_{BE} \cdot cos(\omega t)}{V_T}} \tag{3.14}$$

$$\frac{G_m}{g_m} = \frac{2V_T}{V_1} \tag{3.15}$$

Finding the transconductance now involves solving a bessel function of the first kind, this is out of the scope of this thesis. It can be shown that the large signal transconductance decreases when the variation of V_{BE} increases [10]. This is shown in Eq. 3.15, V_1 refers to the amplitude of the AC signal. This relation is illustrated in Fig. 3.7. As the oscillation builds up, the G_m, and thus, the loopgain drops, until the loopgain is unity. At unity the oscillation stabilises. The g_m is set by the biasing. From this, we can conclude that the final oscillation amplitude, depends on the biasing.

The found relations are used as guidelines, the final biasing is chosen based on simulations.

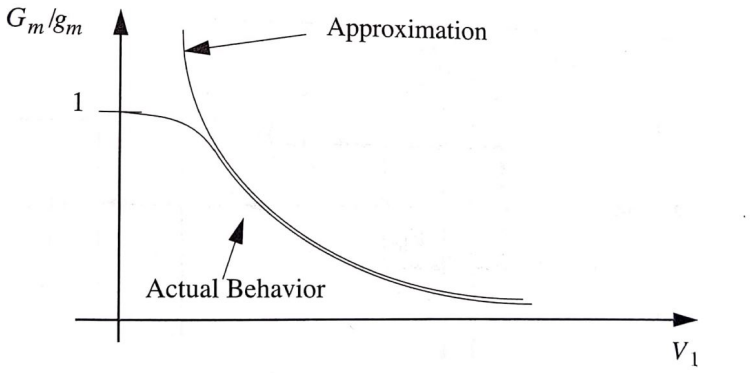


Figure 3.7: G_m/g_m versus V_1 [11, p. 607]

Determining feedback ratio

Figure 3.8 shows the functional model of the Colpitts oscillator. The R is a combination of the parasitic parallel resistor of the inductor, and the load resistor. The load is connected parallel to the tank circuit.

The feedback is equal to $\frac{C_1}{C_1+C_2}$. The higher the feedback, the higher the loopgain. As described earlier, for the system to start oscillating, there needs to be a minimum amount of loopgain. This is the start-up condition, stated in Eq. 3.16. To find the values of C_1 and C_2 that minimize the startup conditions we take the derivative, as shown in Eq. 3.18. Equating to zero and solving results in the optimal ratio of C_1 and C_2 given by Eq. 3.19

$$g_m R \geq \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2 \tag{3.16}$$

$$f(x) = 1/x + x + 2 \text{ with } x = C_2/C_1 \tag{3.17}$$

$$\frac{df(x)}{dx} = -\frac{1}{x^2} + 1 \tag{3.18}$$

$$\frac{C_1}{C_2} = 1 \tag{3.19}$$

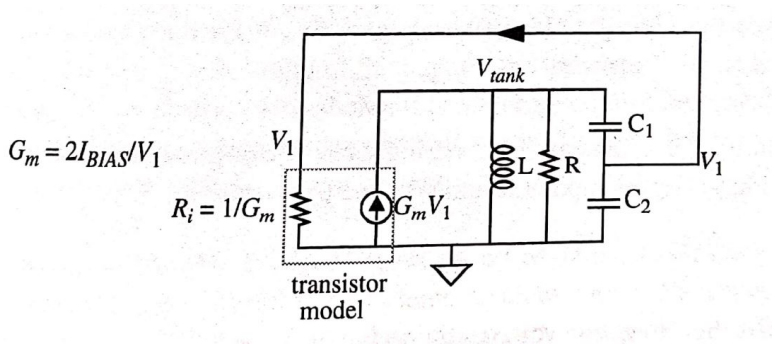


Figure 3.8: functional model of the Colpitts oscillator [11, p. 621]

Another factor to consider is the resistor between base and emitor of the transistor. In Fig. 3.8 this is resistor R_i. In the colpitts oscillator R_i is in parallel with C_2. R_i can be reflected back to the output, and thus, has an influence on the loopgain. Treating the capacitive divider as an ideal impedance transformer, valid when in-circuit Q is large. R_i reflected to the output results in Eq. 3.20 [11, p. 622].

$$R_{reflected} = R_i \cdot \left(\frac{C_1 + C_2}{C_1}\right)^2 \tag{3.20}$$

So to make the output less dependent on the R_i, C_2 should be increased. In practice, we found that C_2 should be around 20 times bigger then C_1 .

3.3 Design

The previous section describes the reason for choosing the collpitts oscillator. This section explains how the Colpitts oscillator is extended to the final modulator design.
The first requirement of the modulator is the operational frequency, which has to be variable from 88 MHz to 108 MHz. This means the frequency of the Colpitts oscillator has to be variable. There are no requirements for how this should be done, so lets discuss some options.

The frequency of the oscillator is determined by the inductance and the capacitance value, as can be seen in Equation 3.21. This means that a variable inductor or a variable capacitor can be used to fulfill the operational frequency requirement.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.21}$$

A type of variable inductor is the tunable inductor. Tunable inductors use moving parts to change their inductance. For this frequency range the inductance should be around one-hundred nanohenry. If the selected inductance would be chosen too large, the capacitance would be too small. There is a limit to the minimum capacitance value of the varactors that are available which is a few picofarad. Also the physical size of the capacitance components would get too small to solder by hand, which is a requirement for this project.
Tunable inductors down to tens of nanohenry exist and are large enough to solder so they could be an option. However because they are relatively small, tuning them requires a tool which is inconvenient for regular use.
For variable capacitors that have their capacitance changed by mechanical motion, two types can be distinguished. Trimmer capacitors, which are usually used for one time internal adjustment, and tuning capacitors that are intentionally designed to repeatedly tune an oscillator circuit. The last one would be a valid option to use.
There also exist voltage controlled capacitors known as the varicap diode or varactor diode. This type of variable capacitor exploits the voltage dependent capacitance of a reverse biased pn junction [12]. These varicap diodes can thus, under reversed bias be used as a voltage controlled variable capacitor. In the final design of the VCO we chose to use varicaps. The frequency and the capacitance in Equation 3.21 does not have an linear relation ship, since a doubling of the capacitance would only result in a decrease of 30 % of the frequency. This would mean that with such a tunable inductor or trimmer capacitor, the tuning accuracy would be higher at the lower frequencies than at the higher frequencies. For a linear voltage-frequency relation, the capacitance must have a quadratic relation to voltage, to compensate the square root in the denominator (Eq. 3.21). The varactor is a good candidate to achieve this, since its capacitance has roughly a quadratic voltage relation (see Fig. A.1a in the Appendix). As a result, the BB201 varactor has an almost linear frequency voltage relation and a trimmer capacitor (represented by $C_{\text{fitted linear line}}$ in Fig. 3.9) is not linear at all, as explained earlier.[1] To not have distortion the frequency should have a linear relation with the input voltage, so the varactor is chosen as the variable capacitor. For clarity, an increased input voltage on the varactor, will decrease the capacitance, and this will increase the oscillation frequency.

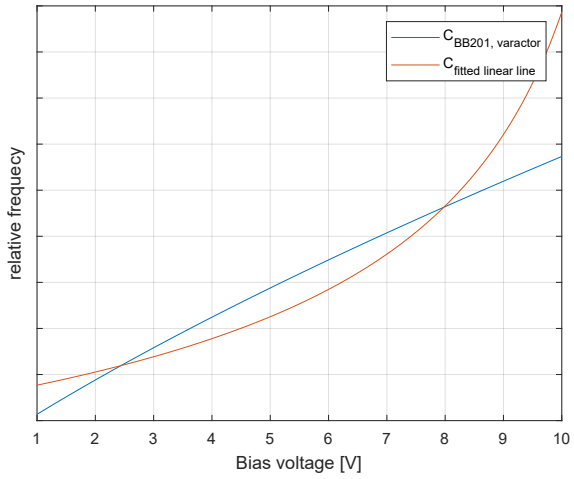


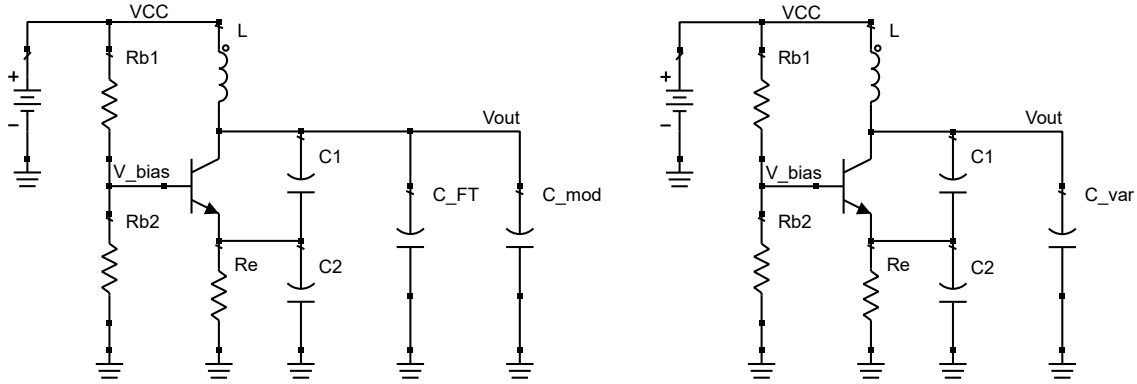
Figure 3.9: Caption

Initial design

In the previous section, it is discovered that the varicap diode is a good choice to vary the frequency of the modulator. Additionally, a varactor is used to modulate the audio signal onto the carrier signal. This is actually for the same reason since for both linear frequency voltage relations are preferred. In this section

[1] In Fig. A.1, the $C_{\text{fitted linear line}}$ is chosen in a way the capacitance is comparable to that of the varactor. See section A.1 for further explanation and section B.1 for the Matlab files.

the design steps of the modulator are described. In the next section the final design of the modulator is discussed.
For the modulator design, the Colpitts oscillator design depicted in Fig. 3.4 must be extended with a variable capacitor for modulating the input signal and a variable capacitor for the frequency tuning. This is (in the ADS simulator) initially done with ideal capacitors (for which the capacitance is varied), to verify the tank circuits oscillation frequency. The ADS circuit can be seen in Figure 3.10a, where C_{FT} represents the variable frequency tuning capacitor and C_{mod} the variable capacitor for modulating the input signal.
These two capacitors, that represent varactors, can be combined since they are in parallel, the result is Figure 3.10b.



(a) Initial modulator design with ideal variable capacitors

(b) Initial modulator design with variable capacitors combined

Figure 3.10: Fundamentals Colpitts and Hartley oscillator

A more practical design

In the initial design there is no load resistance present. This is however necessary to determine the output in the simulation. Also the input source is nowhere to be seen. The input source should be connected to the varicap with some DC offset, to set the right capacitance value. The peak to peak swing of the input signal determines how much the capacitance changes and thus determines the bandwidth of the modulator. The DC bias determines the operating frequency.
The ideal input voltage source (V_{in}) has an output impedance of zero ohm. This creates a direct path to ground for the oscillator. To block this, a relative high resistance ('block_RF') is placed in series with the input source. In the real design this resistor helps to block the RF signal from the previous amplification stage. For the DC bias of the varicap, a voltage divider is used. To block this DC signal from the rest of the circuit two decouple capacitors are used. $C_{decouple1}$ is used to protect the rest of the oscillator circuit from this DC bias, $C_{decouple2}$ is used to decouple the DC bias from the input source. This decouple capacitor also prevents any DC from the input from going into the circuit. A thirth decouple capacitor is used to decouple the output from the circuit. The practical design described above can be seen in Figure 3.11.

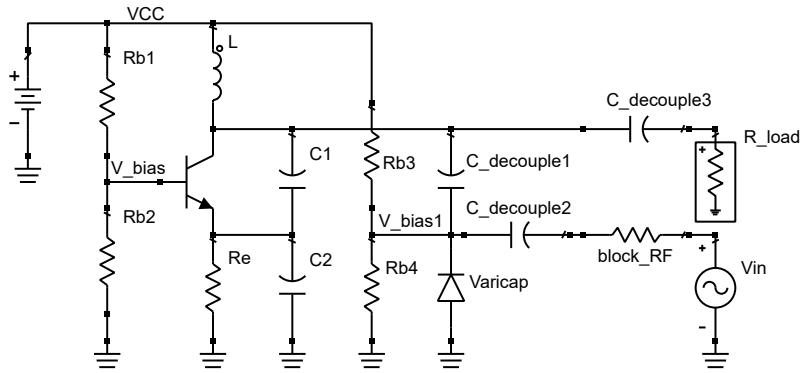


Figure 3.11: First proposed practical design - Modulator

Tank circuit

In the last section a practical modulator circuit is presented. In this section some capacitance and inductance values are explored for the tank circuit of the modulator design.

The inductance value is chosen first, because there is only one inductor in the modulator design. The initial choice is made by making a table in which the capacitance is calculated for different inductance values using Eq. 3.22, which is a rewritten version of Eq. 3.21. This is done for the required frequency range which gives a capacitance range for the varactor. A few lines of this table is displayed in Table 3.1.

$$C = \frac{1}{\omega^2 L} \tag{3.22}$$

The inductance value is chosen based on the $\Delta C_{\text{varactor}}$ and the minimum capacitance value at the highest operational frequency. This is mostly based on the available varactors since the varicaps have a limited capacitance range for the bias that is available.

An inductor with an inductance of 100 nH for the inductance of the tank circuit of the Colpitts oscillator. This allowed the ΔC to be low enough to choose the BB135 UHF variable capacitance diode from NXP [13]. This varicap is chosen for its capacitance ratio and low diode capacitance.
The series resistance of the inductor [14] is calculated with the quality factor read from the data sheet graph using a rewritten version of Eq. 3.23, where ω_0 is the frequency in rad per seconds. This results in a series resistance of about one ohm for the operating frequency range.

$$Q = \frac{L\omega_0}{R_s} \tag{3.23}$$

Table 3.1: Capacitance range needed for varactor for given inductance

Inductance [nH]	$C_{f=88\,MHz}$ [pF]	$C_{f=108\,MHz}$ [pF]	$\Delta C_{\text{varactor}}$ [pF]
18	182	121	61
47	69.6	46.2	23.4
82	39.9	26.5	13.4
100	32.7	21.7	11.0
180	18.2	12.1	6.1

Modulation bandwidth

As seen in the requirements, the modulation bandwidth is chosen to be 75 kHz, which is half of the standard maximum frequency deviation of the carrier wave allowed for FM stereo broadcasting. For this frequency

deviation the capacitance deviation can be calculated using Eq. 3.24. The result for three carrier frequencies is displayed in Table 3.2.[2]

$$\Delta C = \left| \left(\frac{1}{(2\pi \cdot (f_c - 0.5 f_{dev}))^2 \cdot L} - \frac{1}{(2\pi \cdot (f_c + 0.5 f_{dev}))^2 \cdot L} \right) \right| \tag{3.24}$$

As can be seen in Table 3.2, the capacitance deviations are in the order of tens of femtofarad. The voltage swing needed to get these small capacitance deviations at a the specific operating frequency varies between 12.9 mV and 83.0 mV for the BB135 varactor[3], which is already a varicap diode with a small capacitance. The ratio between the voltage swing needed for the outermost frequencies poses a problem, since the bandwidth is proportional to the input voltage swing. Ideally this ratio should be one, so the bandwidth of the modulator doesn't change with varying the operational frequency. In the next section a solution to this problem is presented.

Table 3.2: Capacitance deviation for a BW of 75 kHz at different carrier frequencies

	$f_c = 88\,MHz$	$f_c = 98\,MHz$	$f_c = 108\,MHz$
$\Delta C_{varicap}$ [fF]	55.8	40.4	30.2

Second varactor diode

In the previous section is discovered that the one varicap that is used for modulation, as well as the operational frequency range, has it's limitations in terms of a stable bandwidth. In this section a separate varactor for changing the operational frequency and one for the modulation is implemented into the modulator design.
In this new design a second varicap with biasing resistors is added and provided with a decoupling capacitor, this can be seen in Fig. 3.12.

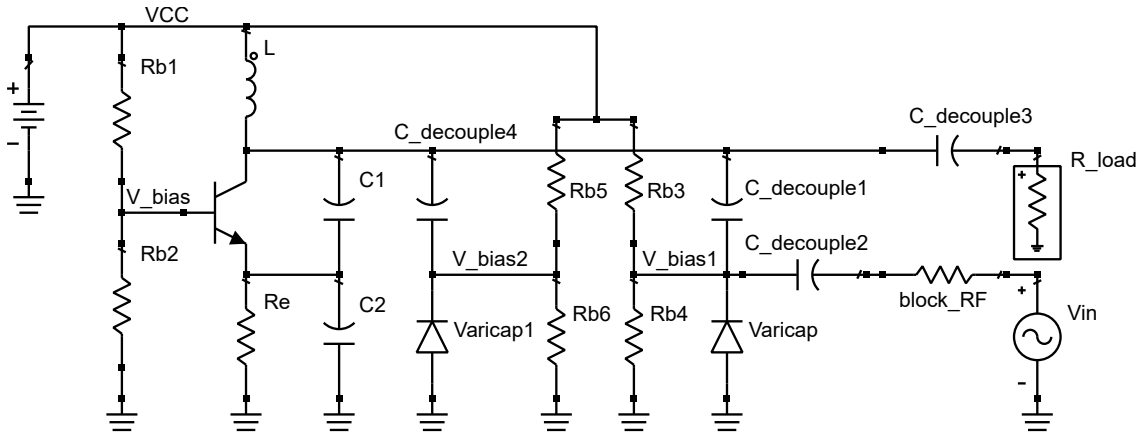


Figure 3.12: Modulator design with two varicaps

During simulation the output swing was maximised to increase the efficiency of the modulator. However the large voltage swing caused the varicap diodes to be in forward bias for some period of an oscillation cycle. This unwanted effect is solved by using another set of varactors (Fig. 3.13). Placing these varactors in the opposite direction prevents the varactors from going into forward bias. This diode configuration needs two additional resistors (R_1 and R_2) to provide DC ground for the two top varicaps.

[2] For the calculations, the inductance value is assumed to be 100 nH, as is described in the 'Tank circuit' section
[3] Calculations can be found in the appendix, see section B.2

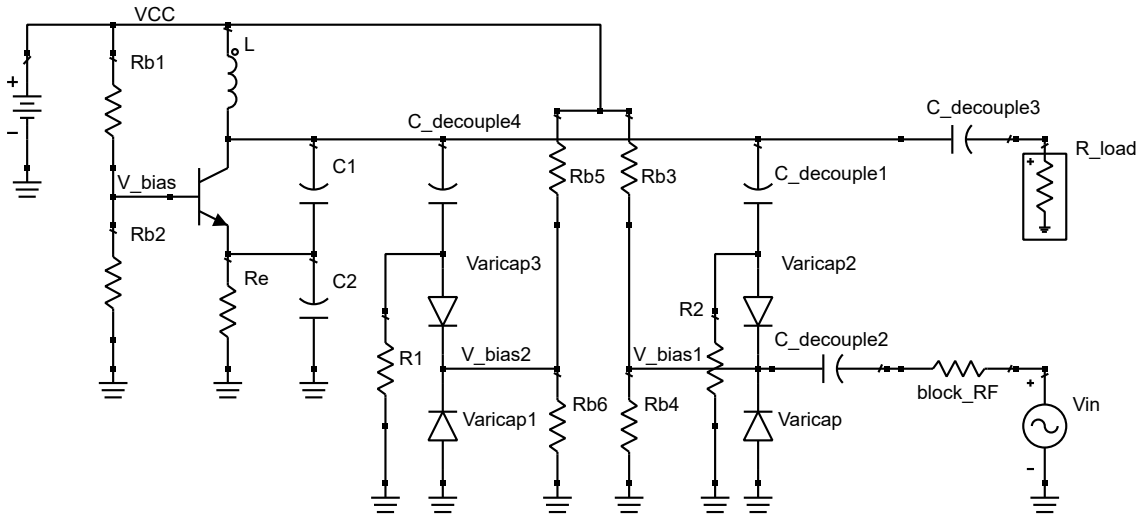


Figure 3.13: Modulator design with double diodes to prevent forward bias

Final modulator design

At this stage, the design of the modulator is coming to its end. In this section the design will be finished and component values will be determined.
The final design of the modulator is very much related to the design shown in Fig. 3.13. Additional components to this design are two capacitors that provide an ac-ground for the bipolar junction transistor base and the DC input line. For the transistor base this is important because if the bias voltage is not constant extra frequency components are introduced in the output. Between the varactors and their bias resistors the resistors R_4 and R_5 are added. These prevent an RF ground through R_{b4} and R_{b6} when the bias voltage for the varicaps is low. In figure 3.14 the final design of the modulator can be seen. A detailed version with component values and simulation components can be found in the appendix, section A.2.

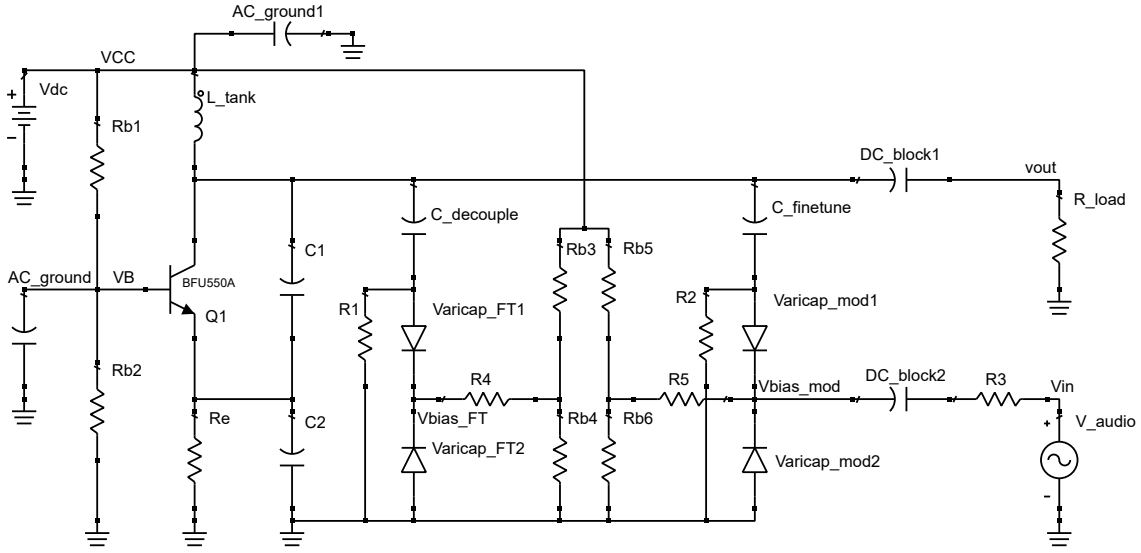


Figure 3.14: Final design schematic of the modulator

To make an estimate of the component values, some formula's are derived from the new circuit (Fig. 3.14). As described in the subsection 'Tank circuit', the inductance of the tank circuit is initially chosen at 100 nH. The capacitance of the tank circuit can be split in three main parallel connected equivalent capacitances.

First, the capacitance of the initial Colpitts oscillator without varactors (Eq. 3.25). Second, the equivalent capacitance of the frequency tuning varicap diodes and decoupling capacitor (Eq. 3.26). Last, the equivalent capacitance of the varicap diodes used for modulation in series with a capacitor to fine-tune the final bandwidth of the modulator (Eq. 3.27).

$$C_{12'} = \frac{(C_1 + C_{BJT}) \cdot C_2}{(C_1 + C_{BJT}) + C_2} \tag{3.25}$$

$$C_{var\_FT} = \left(\frac{1}{C_{decouple}} + \frac{1}{C_{varicap\_FT1}} + \frac{1}{C_{varicap\_FT2}} \right)^{-1} \tag{3.26}$$

$$C_{var\_mod} = \left(\frac{1}{C_{finetune}} + \frac{1}{C_{varicap\_mod1}} + \frac{1}{C_{varicap\_mod2}} \right)^{-1} \tag{3.27}$$

When is assumed that the varicaps are exactly equal, Eq. 3.26 and Eq. 3.27 can be rewritten to Eq. 3.28 and Eq. 3.29:

$$C_{var\_FT} = \frac{C_{decouple} \cdot 0.5 \cdot C_{varicap\_FT}}{C_{decouple} + 0.5 \cdot C_{varicap\_FT}} \tag{3.28}$$

$$C_{var\_mod} = \frac{C_{finetune} \cdot 0.5 \cdot C_{varicap\_mod}}{C_{finetune} + 0.5 \cdot C_{varicap\_mod}} \tag{3.29}$$

The total tank capacitance can than be written as:

$$C_{tank} = C_{12'} + C_{var\_FT} + C_{var\_mod} \tag{3.30}$$

Determining the three parallel capacitance values is an optimisation process. First, the frequency tuning capacitance (C_{var_FT}) is approximated by determining a proper bias range to meet the $\Delta C_{varactor}$ requirement, which is discussed in the 'Tank circuit' section. After that some approximate values for $C_{12'}$ and C_{var_mod} are calculated and the value of C_{var_FT} is adjusted. To ease the design process, some Matlab files where created which automated the calculation process and to provide graphs of the capacitance vs voltage and frequency for visual insight. These Matlab files can be found in the appendix, section B.3.
For the frequency tuning varicap diodes, the BB201 Low-voltage variable capacitance double diode is chosen [15]. This one is chosen for it's capacitance range and relative low capacitance value at ten volt. For the modulating varactors a varactor with very low capacitance is needed. The BB135 UHF variable capacitance diode [13] is chosen for its low capacitance value of around 4.5 pF at ten volt and the relative low series resistance of 0.75 Ω.
Finally the C_1 capacitance value is adjusted for a proper feedback and to adjust the capacitance towards the capacitance needed for the operational frequency as is listed in Table 3.1.

3.4 Simulation results

In this section the simulation results of the final modulator design will described and displayed. These contain the bandwidth, operational frequency, input impedance

The exact ADS schematic with which these are made can be found in the appendix, section A.2.

Bandwidth

The most important simulation results are the ones that show that the modulator is able to modulate an input signal. To verify this harmonic balance simulations have been done in ADS.
As can be seen in Figure 3.15 the bandwidth of the modulated signal does meet the bandwidth requirement of 75 kHz for an input signal of 0.5 V amplitude. This is for an carrier frequency of around 88 MHz (displayed as F_high and F_low). The output of the modulator at this carrier frequency is 8.25 V peak to peak. This is calculated by the equations that are visible in the figure[4].

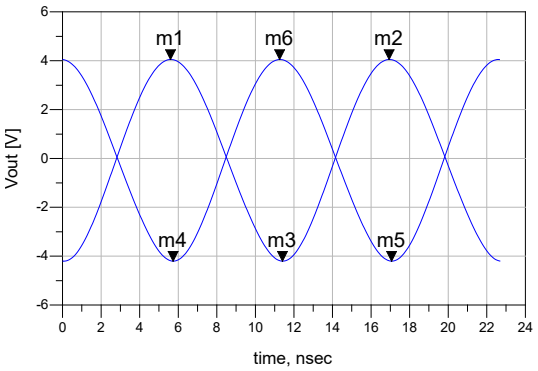
[4] indep(m_) is the time of the markers 'm'

Bandwidth - modulator @ 0.5V ampl. inp.

time	Bandwidth_kHz
<invalid>sec	75.238

Frequencies at +0.5V and -0.5V input voltage

time	F_high	F_low	F_high_pp	F_low_pp
<invalid>sec	88.2860	88.2108	8.2516	8.2539



Eqn Bandwidth_kHz = (F_high-F_low)*1e3
Eqn F_high=1/((indep(m5)-indep(m4))*1e6)
Eqn F_low=1/((indep(m2)-indep(m1))*1e6)
Eqn F_high_pp = m6 - m5
Eqn F_low_pp = m2 - m3

m1 time=5.597nsec ts(HB.vout)=4.048 VvarF=3.250 Peak	m3 time=11.41nsec ts(HB.vout)=-4.205 VvarF=3.250 Valley	m5 time=17.06nsec ts(HB.vout)=-4.204 VvarF=4.250 Valley
m2 time=16.93nsec ts(HB.vout)=4.048 VvarF=3.250 Peak	m4 time=5.734nsec ts(HB.vout)=-4.204 VvarF=4.250 Valley	m6 time=11.26nsec ts(HB.vout)=4.047 VvarF=4.250 Peak

Figure 3.15: HB simulation for the bandwidth at a carrier frequency of about 88 MHz

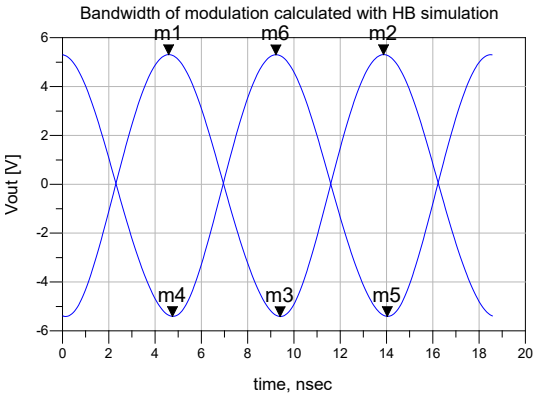
In Figure 3.16 it can be observed that the bandwidth of the modulated signal at a carrier frequency of 108 MHz is a about 100 kHz. This is somewhat higher than the 75 kHz, but does not introduce problems directly. The signal can be demodulated by the demodulator for a higher bandwidth than 75 kHz. Also the bandwidth can be reduced by reducing the input amplitude, which is a relative simple modification.
The amplitude of the output signal (10.7 V) at this operating frequency comes close to the supply voltage of 12 V, which is a good sign since this means the modulator is used to it's full potential. Also the amplitude change across the bandwidth is only 8 mV which is negligible, which is good since the amplitude of a FM should be constant.

Bandwidth - modulator @ 0.5V ampl. inp.

time	Bandwidth_kHz
<invalid>sec	101.989

Frequencies at +0.5V and -0.5V input voltage

time	F_high	F_low	F_high_pp	F_low_pp
<invalid>sec	107.7897	107.6877	10.7101	10.7180



Eqn Bandwidth_kHz = (F_high-F_low)*1e3
Eqn F_high=1/((indep(m5)-indep(m4))*1e6)
Eqn F_low=1/((indep(m2)-indep(m1))*1e6)
Eqn F_high_pp = m6 - m5
Eqn F_low_pp = m2 - m3

m1 time=4.585nsec ts(HB.vout)=5.306 VvarF=7.050 Peak	m3 time=9.402nsec ts(HB.vout)=-5.412 VvarF=7.050 Valley	m5 time=14.03nsec ts(HB.vout)=-5.408 VvarF=8.050 Valley
m2 time=13.87nsec ts(HB.vout)=5.306 VvarF=7.050 Peak	m4 time=4.755nsec ts(HB.vout)=-5.408 VvarF=8.050 Valley	m6 time=9.219nsec ts(HB.vout)=5.302 VvarF=8.050 Peak

Figure 3.16: HB simulation for the bandwidth at a carrier frequency of about 108 MHz

Operational frequency

In the previous section it has already been observed that the modulator can work at the required operational frequencies. In this section the operational frequency is verified in a short transient simulation. The input signal, which can be seen in the left graph in Fig. 3.17, is applied to the input of the modulator for a realistic simulation. The simulation time is set to 100 µs which is two periods of a 20 kHz signal.
As can be seen in the frequency analysis graph on the right of Fig. 3.17, the operational frequencies of the

transient simulation support those seen in the harmonic balance simulation. These operational frequencies have been achieved with a bias voltage of 3.75 V and 7.55 V for respectively 88 MHz and 108 MHz.

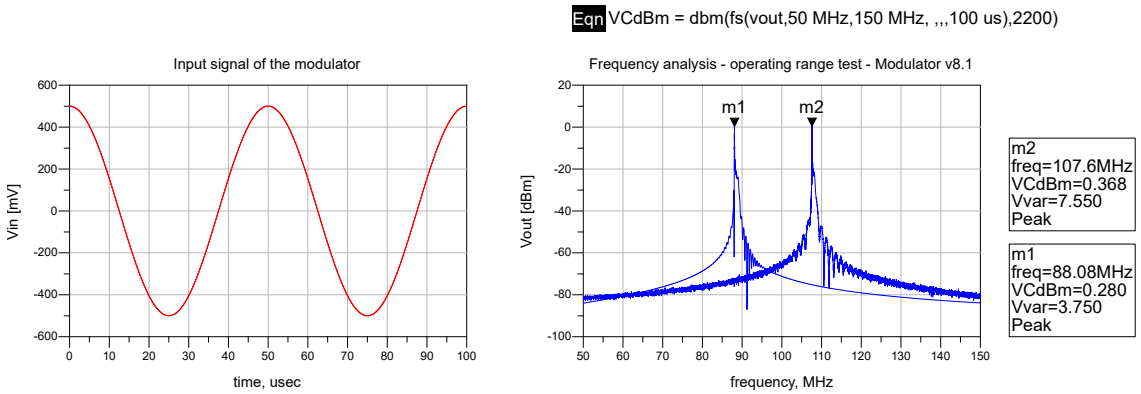


Figure 3.17: Frequency analysis with a transient simulation

Finally a plot is made that shows the harmonics of the operational frequencies shown in the previous graphs. As can be seen in Fig. 3.18 the first harmonics of the operational frequencies, indicated by marker m_1 and m_6, are more than 30 dB lower. The harmonics after are even more suppressed.

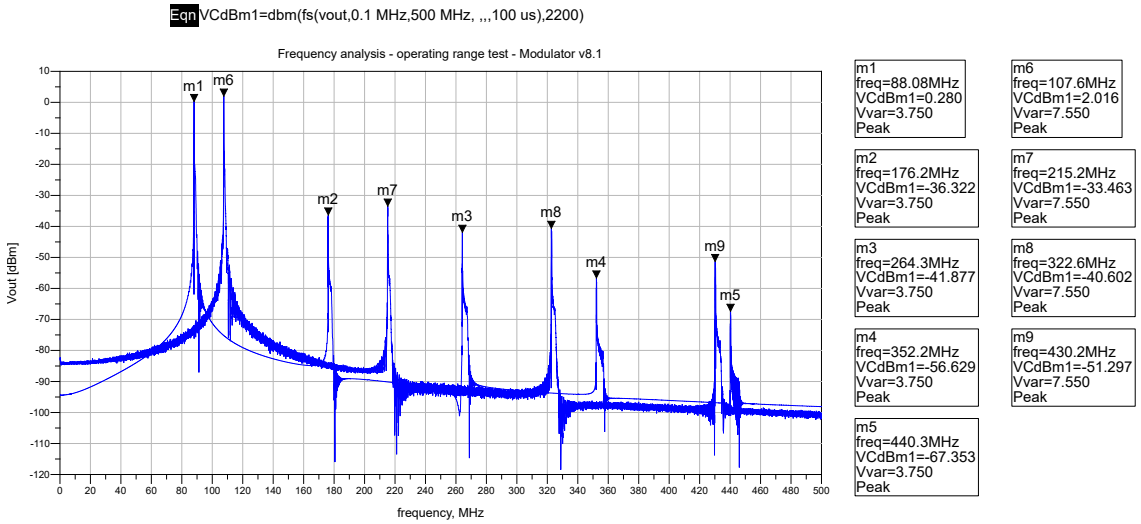


Figure 3.18: Fundamental oscillation frequencies and their harmonics

Input impedance

The input impedance of the modulator is mostly resistive, for the lower frequencies the complex impedance plays a role and the impedance goes up as can be seen in Figure 3.19. For frequencies beyond 100 Hz the input impedance is about 69 kΩ. At 20 Hz the input impedance is roughly 450 kΩ. This is however not a problem, since a buffer is used between the audio amplifier and the modulator [16].

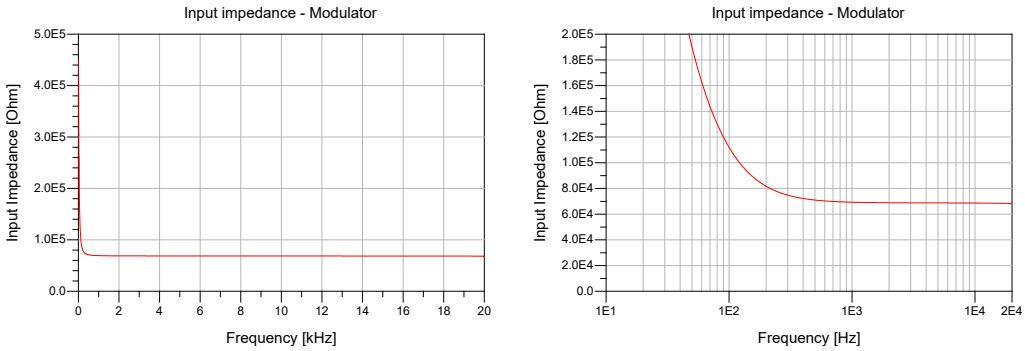


Figure 3.19: Input Impedance of the modulator

Design validation

For the modulator to work correctly and reliably, the voltages and the currents should not exceed the values that components can handle consistently. The most critical component is the BFU550A transistor that is used. It has a maximum sustained V_{CE} of 12 V and a I_C rating of 15 mA [17].
In Fig. 3.20 it can be seen that the output voltage and the collector current stay within the limits of the transistor. The blue line shows the harmonic balance simulation for a carrier frequency of 108 MHz and the red line for 88 MHz.

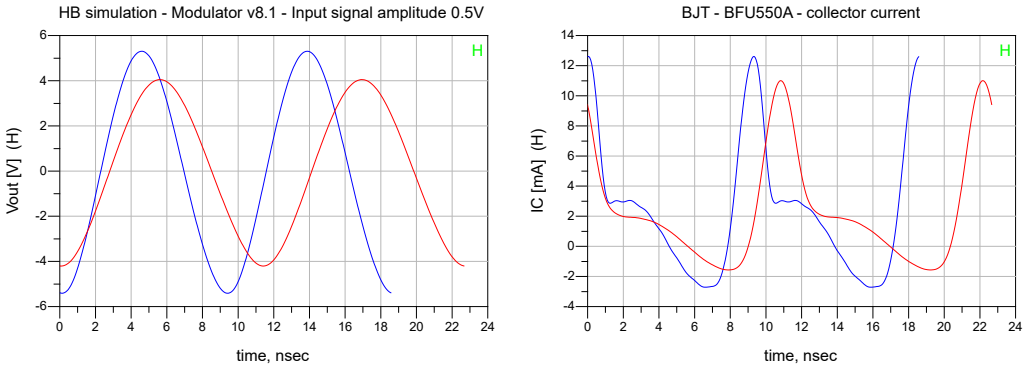


Figure 3.20: Output voltages of the modulator at the edges of the operational frequency

The harmonic balance simulation does have a proper output, which means that the startup conditions of the oscillator are met. The startup conditions in should however be verified in transient simulation, which is shown in Fig. 3.21.

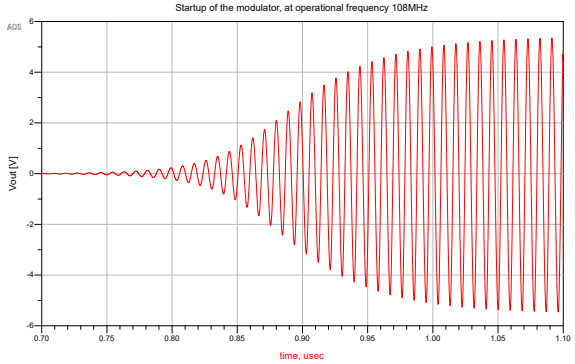


Figure 3.21: Startup of the modulator at 108 MHz

3.5 Measurement setup

The measurement setup of the modulator consists of a DC-source, a signal generator that can produce test tones between 20 Hz and 20 kHz with an amplitude of at least 0.5 V and a frequency analyser or oscilloscope.
At the moment of writing this thesis, no measurement results are available. This section will describe how the measurement will be done.
The DC-source will be connected to the top side of the pcb shown in Fig. 3.22. The input signal should be connected to the light blue resistor on the far right of the pcb. The output signal can be measured between the large brown ceramic capacitor and the top most, large 2.2 kOhm resistor.
When the DC-source is switched on, an output carrier frequency should be visible at the oscilloscope.

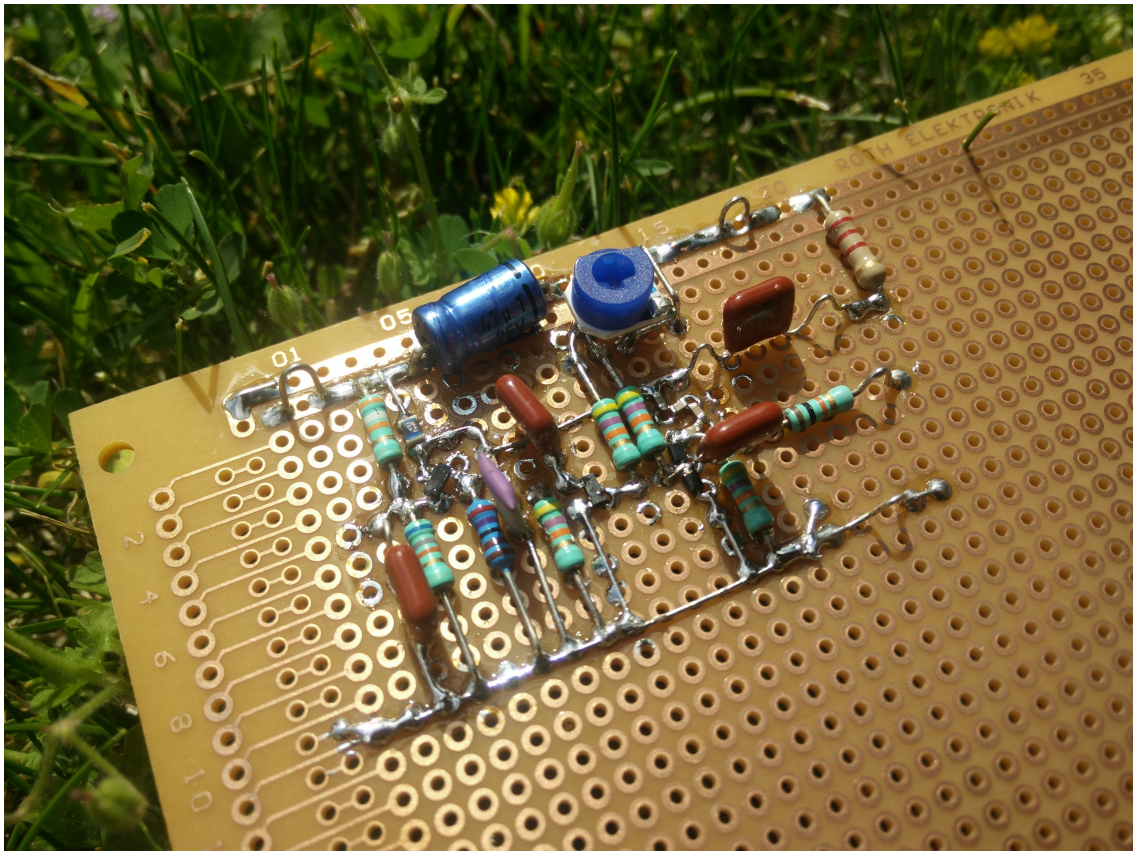


Figure 3.22: Modulator soldered on a pcb

3.6 Measurements

Modulator measurement results are discussed in subsection 4.1.4.

4 Demodulator

This chapter elaborates on the different parts designed for the demodulator. A typical superheterodyne receiver is shown in Fig. 4.1. In the receiver a mixer is used to shift the received signal around a fixed intermediate frequency(IF). This structure is used in almost all modern receivers. The advantage of this structure is that all the successive circuits can be optimized for the IF. The mixer will be discussed in section 4.1. After the mixer there will be more amplification needed to get the required swing at the input of the detector. The IF amplifiers are discussed in the thesis of groupmates Ivor and Victor. The detector will detect the information out of the FM signal, discussed in section 4.2.

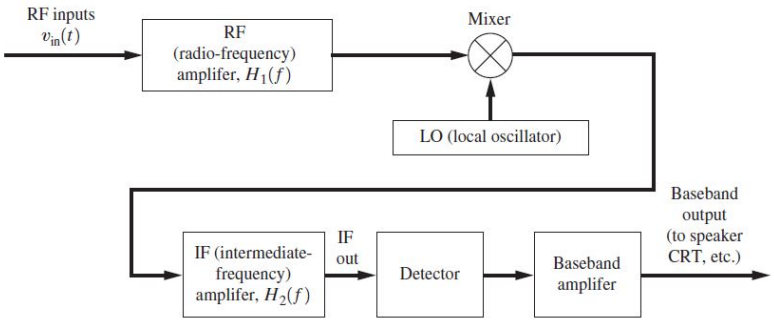


Figure 4.1: Superheterodyne receiver [8]

4.1 Mixer

The function of the mixer is to shift the RF signal onto a lower intermediate frequency (IF). As mentioned, by shifting the signal to a lower frequency, the following circuits can be optimized for that specific frequency. Another advantage is that the following circuits will have less parasitic effects. This last reason motivated us to choose the relatively low IF of 4 MHz. The mixer makes use of a tunable local oscillator. By tuning the local oscillator, any signal in the range of 88 MHz to 108 MHz can be mixed at the IF.

Frequency shifting is a non-linear operation, so any mixer makes use of a non-linear device [18]. The mixer in this project is integrated into an oscillator. This way, only one transistor is used to have an oscillator, and mixer. The mixing operation is implemented by putting the RF signal on the base of the transistor. The voltage on the base-emiter diode is the sum of the input signal, and the already present oscillator signal. Disregarding leakage current, the diode equation is shown in Eq. 4.1. Substituting Eq. 4.2 and writing out the taylors expansion results in Eq. 4.3. The quadratic term is of interest, because it contains a component at the difference frequency, as is shown in Eq. 4.4. With the correct ω_{LO}, this difference frequency is equal to the IF. As is shown there are also other unwanted frequencies created. Therefore, the stages after the mixer should have bandpass filters on the IF.

$$I_D = I_0 e^{V_D/V_T} \tag{4.1}$$

$$V_D = V_{LO} + V_{RF} \tag{4.2}$$

$$I_D = I_0 e^{\frac{V_{LO}+V_{RF}}{V_T}} = I_0 \sum_{n=0}^{\infty} \frac{(\frac{V_{LO}+V_{RF}}{V_T})^n}{n!} \tag{4.3}$$

$$= \alpha_0 + \alpha_1 (V_{RF} + V_{LO}) + \alpha_2 (V_{RF} + V_{LO})^2 + \alpha_3 (V_{RF} + V_{LO})^3 + \dots$$

$$\begin{aligned}(V_{RF} + V_{LO})^2 &= (V_{RF} \cos(\omega_{RF} t) + V_{LO} \cos(\omega_{LO} t))^2 \\ &= \left(V_{RF}^2 (1 + \cos(2\omega_{RF} t)) + V_{LO}^2 (1 + \cos(2\omega_{LO} t))\right. \\ &\quad \left. + 2V_{RF} V_{LO} [\cos(\omega_{RF} - \omega_{LO}) t + \cos(\omega_{RF} + \omega_{LO}) t]\right)\end{aligned} \tag{4.4}$$

4.1.1 Design

In the previous sections is described that the mixer is a modified oscillator. Since a Colpitts oscillator is already designed for the modulator and the operational frequencies lay very close together, the design is very much alike. In the chapter of the modulator a practical design of the modulator is proposed (Fig. 3.11). For the modulator this single varicap design was not yet good enough to fulfil the requirement (modulation and frequency tuning). For the mixer however, one varactor is enough to meet the frequency tuning requirement of the demodulator. Before the design is presented, the operational frequency of the LO has to be chosen. This is explained next.

As explained and derived in the previous section, the mixer creates a difference frequency that is called the IF. There are two cases for the oscillator frequency, either the local oscillator frequency is higher than the input RF signal, or lower than the input RF signal. In both cases the difference between the two frequencies is the IF frequency. For the design of the mixer, the local oscillator frequency (f_{LO}) is chosen to be lower than the input frequency f_{RF}. The reason is that when the f_{LO} is lower than the f_{RF}, the image frequencies (f_{im}) that are shifted to the IF frequency are below rather than above the f_{LO} frequency. The benefit this is that the LO can operate at a lower frequency, which means less parasitic effects. An illustration of mixing is given in Fig. 4.2.

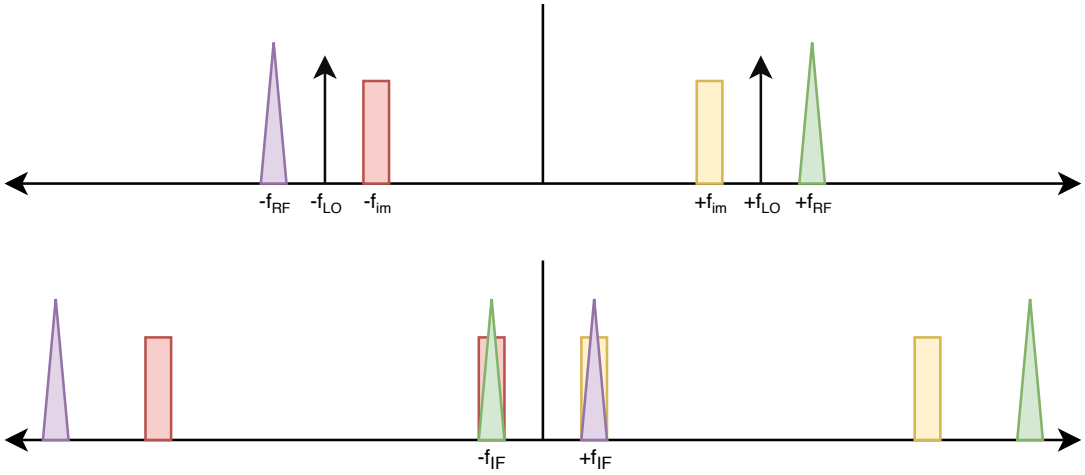


Figure 4.2: Illustration of image frequencies that are mixed with the RF signal at the IF frequency

How much the RF signal is distorted by the image frequencies depend on the signal levels. Since the requirement for the distance between the TX and RX is at least 5 m, the RF signal level is expected to be strong enough to have an acceptable output. However if this isn't the case (i.e. the receiver is close to an other strong signal source), the operating frequency can be chosen between approximately 88 MHz

and 96 MHz. For this frequency range the image frequencies lay below 88 MHz and are filtered out by the preceding LNA stage [19], as is described and displayed in the introduction (Fig. 1.2).

final design

As explained, the design of the mixer is largely based on the previous Colpitts oscillator first seen in Fig. 3.4. This oscillator consists of a series LC-tank which is fed by a transistor to sustain itself. The operational frequency can be varied by changing the capacitance of the varicap diode connected parallel to the other capacitances of the LC-tank.
The RF signal is introduced into the circuit by applying it to the base of the transistor. This causes the amplitude of the oscillator to vary based on the input RF signal and thus creates different frequency components, as showed in Eq. 4.3 in the previous section.
The amplitude of the difference frequency component is mostly determined by the amplitude of the input signal, but this mixer design can potentially provide some gain. However since the mixer doesn't need to provide gain, the initial minimum gain is set to one.

For the design of the mixer, the same dual varactor setup as in the final design of the modulator is used. This is also for the same reason as in the modulator circuit: to prevent the varicap diode from going into forward bias. The final design of the mixer can be seen in Fig. 4.3. In this design the Colpitts oscillator can be recognised by the inductor at the collector of the transistor, L_{tank} and the two capacitors C_1 and C_2. The choice for the varactor is again the BB201 Low-voltage variable capacitance double diode from NXP. This three pin package is represented by Varicap1 and Varicap2 in the circuit seen in Fig. 4.3.
To optimise the integration of the mixer into the complete design a few extra components are added. The function of the components of the oscillator (R_1, R_2, R_{b1} - R_{b4}, Q_1, L_{tank}, C_1, C_2, $C_{decouple}$ and the varicaps is already described in chapter 3.
The capacitor at the input, $C_{decouple1}$, is used to decouple the input from the DC bias of the transistor. The capacitors C_{s1} and C_{s2} should provide a ground for LO so it can't propagate into the previous or next stage respectively. Choosing the correct value for these capacitors is however an optimisation problem, since C_{s1} should not provide a ground for the input signal and C_{s2} should not provide a ground for the IF. Finally, the High Frequency choke blocks the RF signals from the DC supply line.

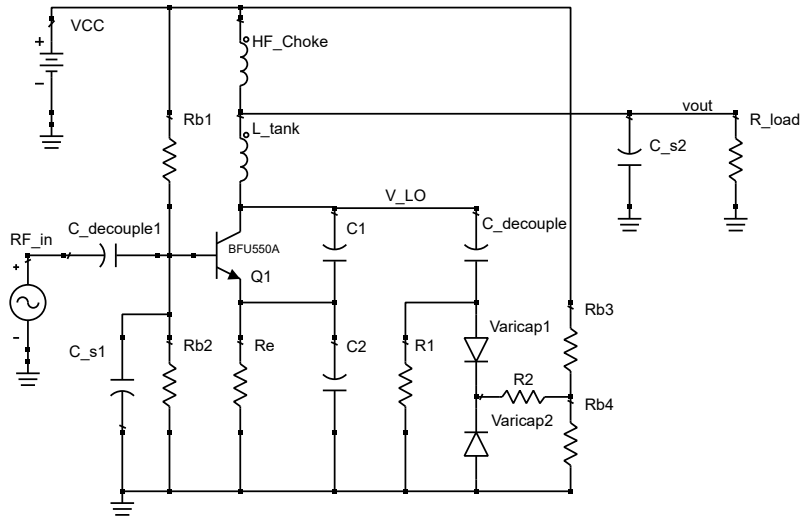


Figure 4.3: Final mixer design

A varicap analysis is done to verify if the BB201 varicap is a good choice. The capacitance value needed for three carrier frequencies (88, 98 & 108 MHz) is approximated using Eq. 4.5[1]. With ideal

[1]The derivation of this formula can be found in the appendix, section A.3

capacitors (instead of varactors), a more exact capacitance value for an IF of 4 MHz is determined by trail and error in the simulator. The calculated values and more exact capacitance values are listed in Table 4.1.

With these determined values, the bias voltage of the BB201 varicap diode is determined with the help of a Matlab script[2]. As can be seen in Fig. 4.4, the bias voltages are well within the possible DC bias voltage that can be provided. So it can be concluded that the BB201 varactor is a valid choice for the mixer design.

$$C_{var} = \frac{1}{(2\pi f)^2 \cdot L} - \frac{(C_1 + C_{BJT}) \cdot C_2}{(C_1 + C_{BJT}) + C_2} \tag{4.5}$$

Table 4.1: Capacitance values

	$f_{88\,MHz}$	$f_{98\,MHz}$	$f_{108\,MHz}$
calculated [pF]	25.7	18.5	13.2
simulated [pF]	27.2	19.3	13.7

For all the components surrounding the Colpitts oscillator, the ADS simulator is used to fine tune the values to a point where the gain of the mixer was highest. This is done for the three mentioned carrier frequencies since the gain can rise for once carrier frequency while dropping for another. With the final values, a gain between ten and twenty is reached across the operating frequency. This will be showed in the following section.

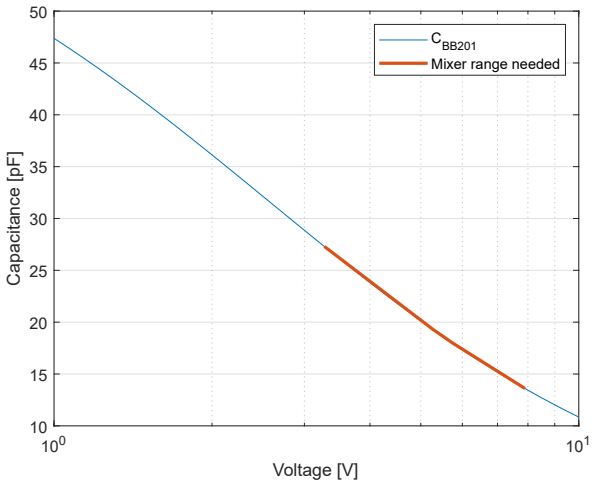


Figure 4.4: Capacitance and bias voltage range needed for the mixer circuit

4.1.2 Simulation results

In this section the simulation results of the final mixer design will be reviewed. First the transient simulation results for three carrier frequencies will be discussed. After that the Harmonic balance simulations will be compared to the transient results and the gain of the mixer will be discussed.

For the transient simulation a simulation time of 500 µs is chosen. With the $fs()$ function, a frequency plot can be made from the time signal. The start and stop time are 100 µs and 500 µs respectively. For the window type, Blackman-Harris is chosen and for the time-to-frequency transform, the Fast Fourier transform. The other settings are left on default.

[2]The Matlab script can be found in the appendix, section A.3.

In figure 4.5 the local oscillator operates at approximately 94 MHz[3]. This is for a DC-bias voltage of 5.262 V on the varicap. It can be observed that the LO peak (m_3), is the highest, which is expected since the LO signal is the strongest. The input signal is relatively weak at 100 µV and creates the peak m_4. The IF frequency is marked by m_1 and is clearly higher than the RF signal. This will be confirmed in the harmonic balance which is discussed next.

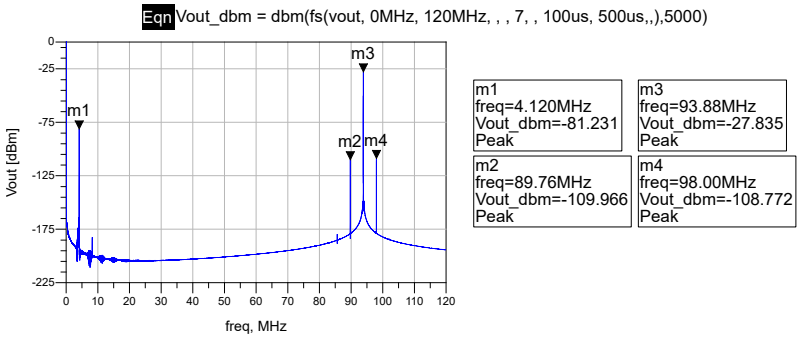


Figure 4.5: Transient simulation of the mixer, f_{RF} = 98 MHz, $f_{LO} \approx$ 94 MHz

The harmonic balance simulations are done on the same frequencies as the transient simulations. In figure 4.6 can be seen that the gain of the mixer at this operating range is almost 20. This is larger the gain of one, which was stated as a minimum in the requirements. When the operating frequency is 88 MHz, the gain of the mixer drops to about ten, which can be seen in Fig. A.7 in the appendix. This is still a gain that is higher than is minimum required.
Also the collector current (I_C) and collector emitter voltage (V_{CE}) of the BJT 550A are plotted. This is to check if the values are within the allowed ranges. This is the case since V_{CE} is allowed to be 12 V and I_C to be 15 mA.

Harmonics - Mixer

harmindex	freq	mag(Vin)	mag(vout)
0	0.000000 Hz	0.00000	12.00000
1	4.00018 MHz	0.00000	0.00196
2	8.00037 MHz	0.00000	7.32674E-8
3	89.9996 MHz	0.00000	0.00002
4	93.9998 MHz	0.00000	0.13647
5	98.0000 MHz	0.00010	0.00002
6	102.000 MHz	0.00000	5.49396E-7
7	183.999 MHz	0.00000	1.95598E-7
8	188.000 MHz	0.00000	0.00042
9	192.000 MHz	0.00000	2.97347E-7

Gain of the mixer

harmindex	Mixer_GAIN
<invalid>	19.579

Eqn F_IFmag=mag(mix(vout, {-1,1}))
Eqn F_IFmag_IN=mag(mix(Vin, {0,1}))
Eqn Mixer_GAIN=F_IFmag/F_IFmag_IN

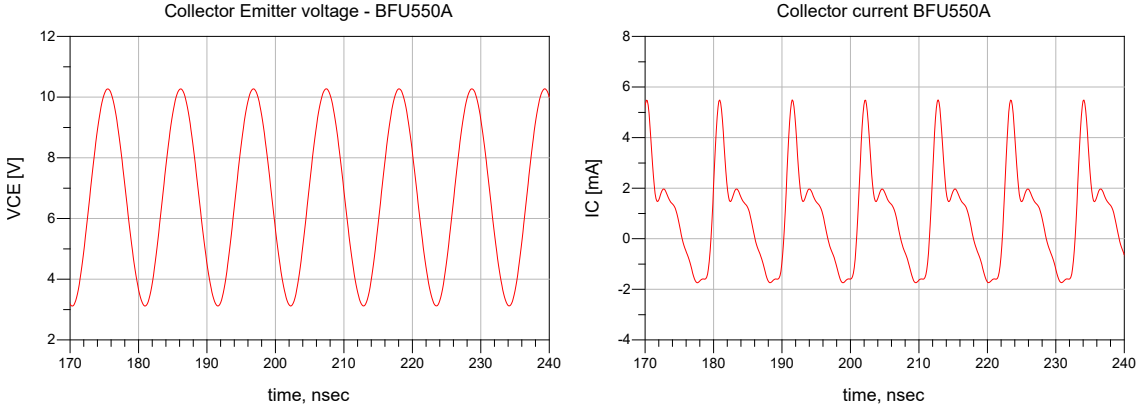


Figure 4.6: Harmonic balance simulation - gain of the mixer at f_{RF} = 98 MHz

[3]In the appendix are more of these figures, they both display another LO frequency and one of them contains additional graphs in which the peaks can be seen in more detail.

Lastly the input impedance of the mixer is simulated over the whole operating range. As can be seen in Fig. 4.7, the input impedance lays between about 5.65 Ω and 4.65 Ω. This is a bit low for the LNA, and if nothing would be done, the LNA amplification would decrease. To solve this a buffer stage is added to the LNA design as can be read in [19].

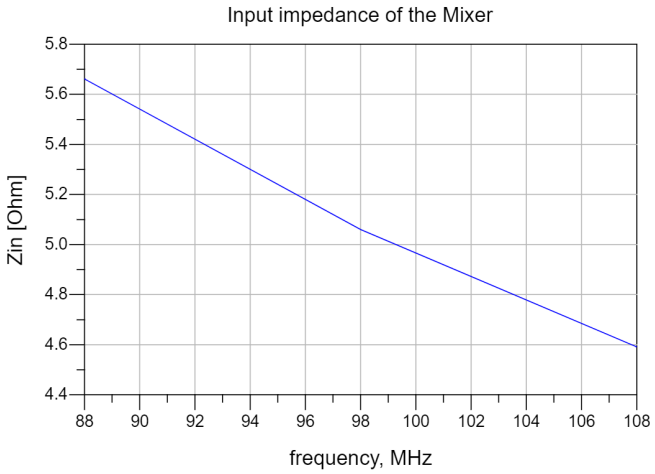


Figure 4.7: Input impedance of the mixer

4.1.3 Measurement setup

The measurement setup for the mixer consists of a DC-source, a signal generator that can generate an RF frequency signal of at least 100 uV and a oscilloscope to display the output.

4.1.4 Measurements

After the submission of this thesis, the circuits of the mixer and modulator have been measured. Unfortunately, the measurements did't show any oscillations. To go back a few steps, a Colpitts oscillator circuit was made and measured. Some results where achieved with this circuit (see Fig. 4.8), but in the available time we where not able to adapt it to a working modulator or mixer.
Two additional figures of the mixer and modulator are provided that show the final state of the mixer and modulator circuits (see Fig. 4.9, Fig. 4.10).

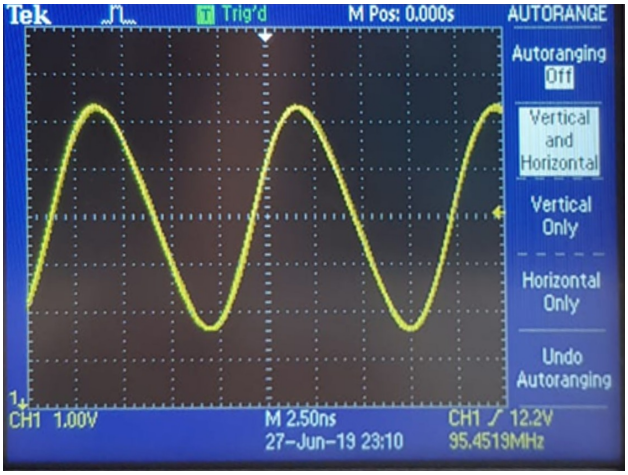


Figure 4.8: Measurement of an oscillator

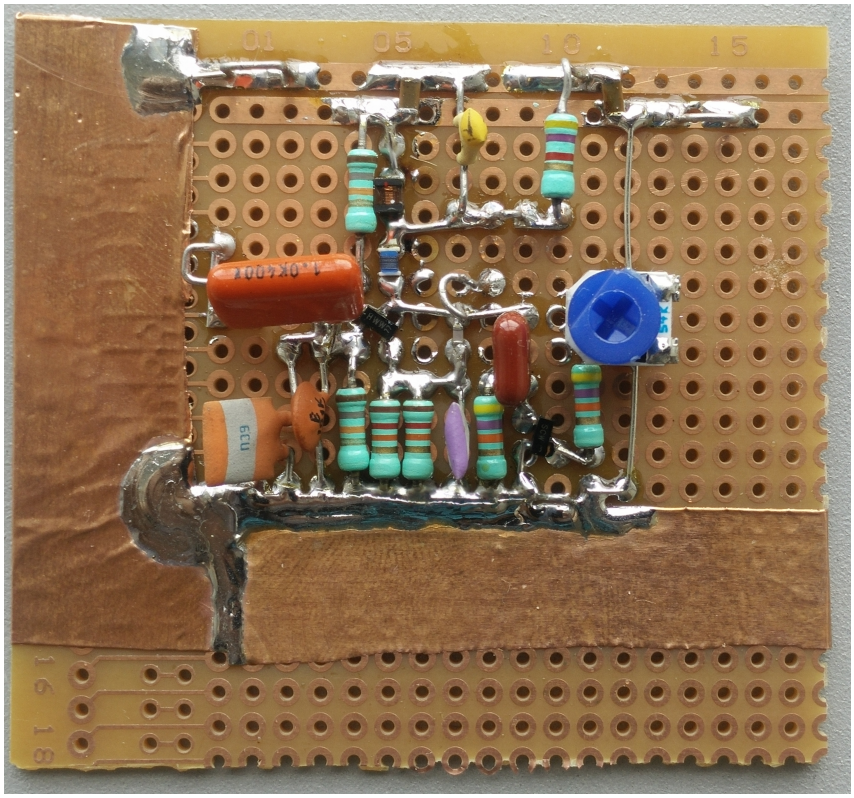


Figure 4.9: Display of final mixer circuit

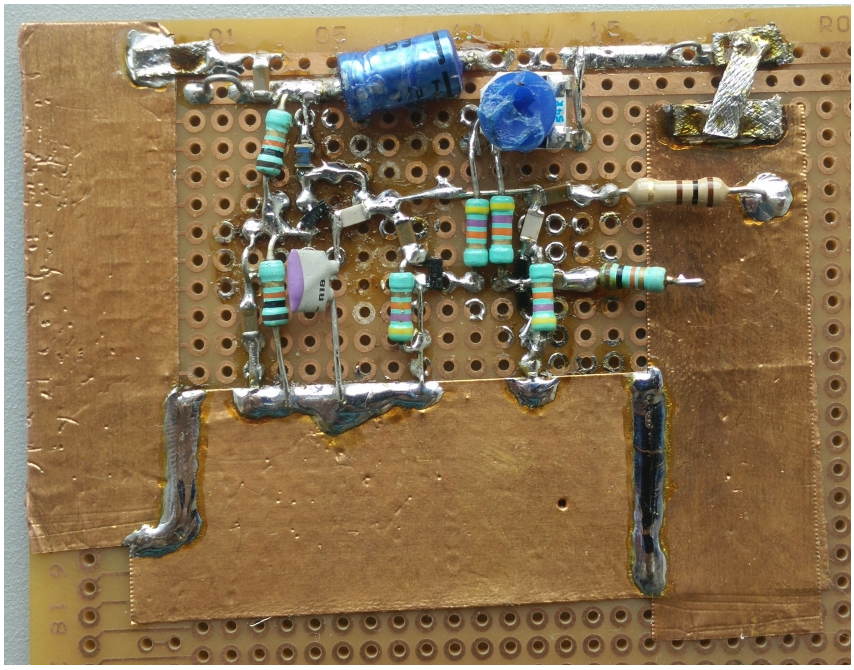


Figure 4.10: Display of final modulator circuit, with ground-plane

4.2 Detector

Ideally an FM detector has an output directly proportional to the frequency of the input. As the information of the input signal is in the carrier frequency, the desired output amplitude is directly proportional to the frequency of the input. This desired transfer is illustrated in Fig. 4.11. Remembering the differentiation property of the Laplace transform of Eq. 4.6; a linear frequency versus time characteristic corresponds to a differentiator in the time domain. The goal is to build a circuit that approximates the ideal differentiatior in the bandwidth of the signal. The bandwidth is specified in the program of requirements as 75kHz

$$\mathcal{L}\left(f'\right) = sF(s) - f(0) \tag{4.6}$$

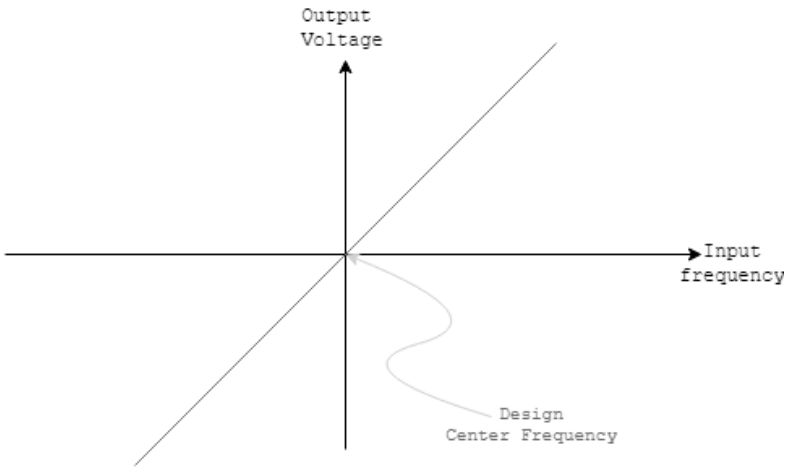


Figure 4.11: Ideal detector transfer

There are different kind of FM detectors, but those which are in the scope of this project function as a frequency to amplitude converter, driving a conventional AM envelope detector. A block scheme of such a system is shown in Fig. 4.12. The function of the left block is to convert the FM signal into an AM signal. It does this by differentiating the FM signal shown in Eq. 4.8, the σ accounts for attenuation. However this signal will be AM modulated around the design center frequency. The envelope detector converts the AM signal into the information signal shown in Eq. 4.9.

$$V_1(t) = A\cos\left[\omega_o t + \theta(t)\right] \tag{4.7}$$

$$V_2(t) = -\sigma A\left[\omega_o + \frac{d\theta}{dt}\right]\sin\left[\omega_o t + \theta(t)\right] \tag{4.8}$$

$$V_3(t) = \sigma A\omega_o + \sigma A\frac{d\theta}{dt} \tag{4.9}$$

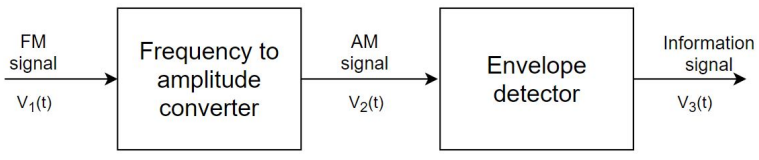
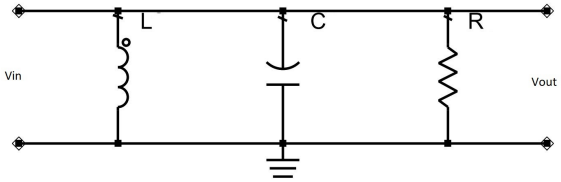
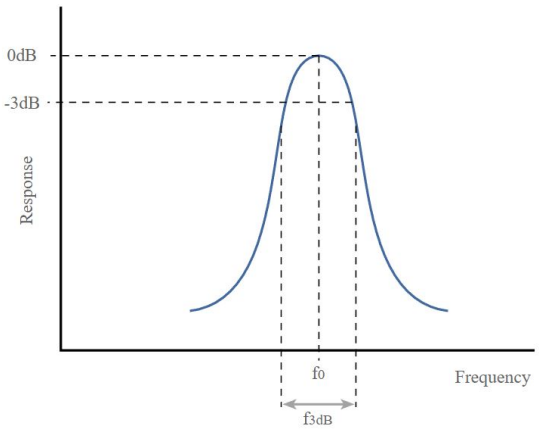


Figure 4.12: Block scheme of common FM detectors

The simplest way of implementing the frequency to amplitude converter is by means of a bandpass filter. The bandpass filter has a approximately linear region in its transition band. This region can be used as a differentiatior in the time domain. A picture of a simple RLC bandpass circuit is shown in Fig. 4.13a. A typical transfer is shown in Fig. 4.13b, the region around the -3dB frequency could be used as a differentiatior.

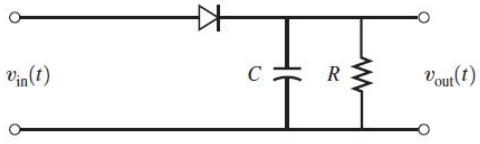


(a) Simple bandpass filter

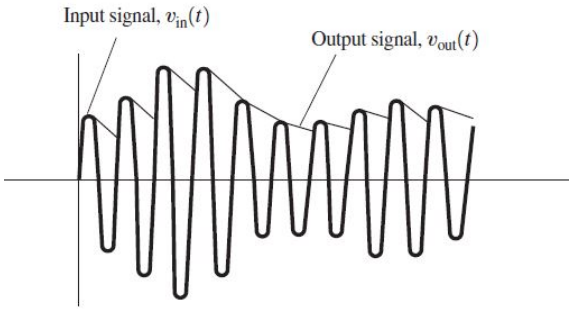


(b) Response of an RLC circuit [20]

After the bandpass circuit, the signal is still AM modulated around the IF frequency. To retrieve the information signal, an envelope detector is used. A standard envelope detector is shown in Fig. 4.14a. When the voltage at node vin is above zero, the diode current will charge the capacitor. When the voltage at vin is below zero, the capacitor will discharge through the resistor. The result is the waveform of Fig. 4.14b. The RC time constant should be chosen such that the output signal is able to follow the envelope of the input signal.



(a) Diode envelope detector [8]



(b) Diode envelope detector waveform [8]

Integrating the diode detector into the bandpass filter results in the circuit of Fig. 4.15. This circuit is called the slope detector.

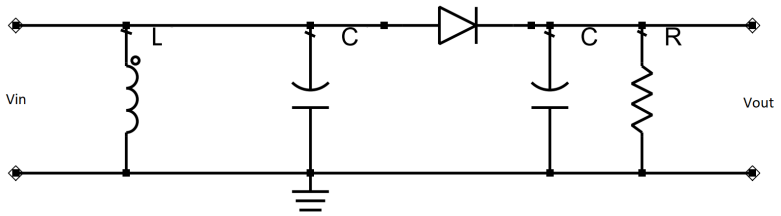


Figure 4.15: Slope detector

When discrete components were still the norm, a widely used FM detector was the Foster-Seeley discriminator. The Foster-Seeley discriminator is shown in Fig. 4.16. The circuit left of the radio frequency choke(RFC) functions as a tuned-transformer, so like with the slope detector, it has a bandpass characteristic. The right part shows two stacked envelope detectors. The Foster-Seeley discriminator differentiates the input signal by first splitting the input into two signals that are out of phase. These signals are then added to obtain the differential. The two out of phase signals are created using a loosely coupled center tapped transformer. The center tap fed back, through a capacitor, to the primary coil. The signal on coil L1 will be out of phase with the signal on the coil L2. The center tap is connected through a radio frequency choke (RFC), to the middle point of the two envelope detectors. Hereby providing a reference. The two out of phase signals are summed to get the final output.

The summing of two signals that are equally, but oppositely shifted in phase, has two advantages. Firstly, the amplitude of the output will be higher. Secondly, the distortion in the transfer will also be equal and opposite. So by summing the signals, the distortion will be limited. The transfer is illustrated in Fig. 4.16.

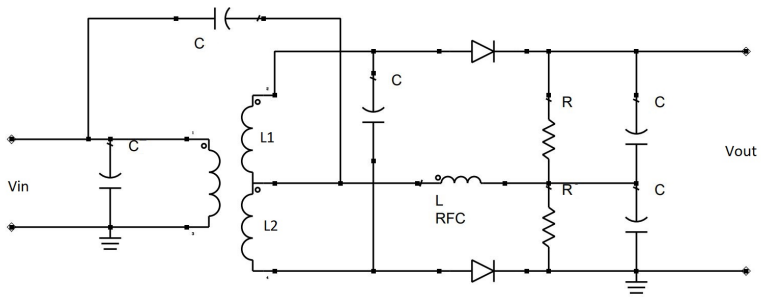


Figure 4.16: Foster-Seeley discriminator

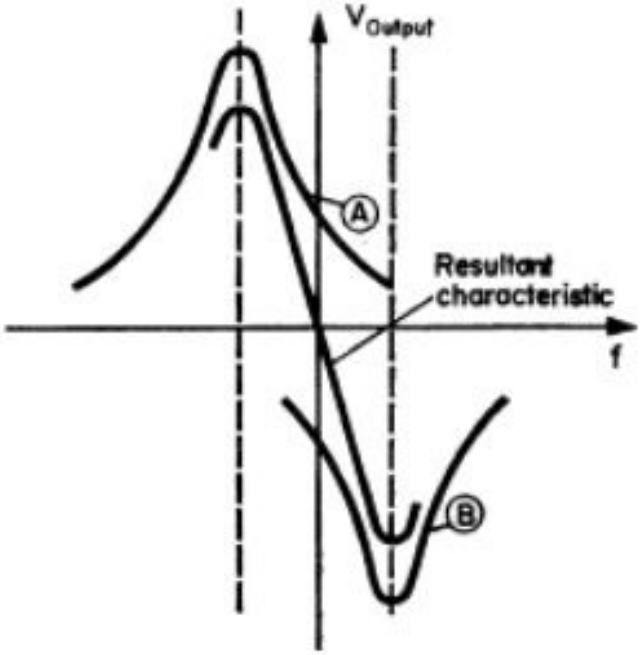


Figure 4.17: Foster-Seeley charactaristic [21]

In the final design we choose to not use the Foster-Seeley discriminator. The most important reason is the complexity of the design. Furthermore, transformers are expensive, and not suitable to be integrated on a chip. Because of this, modern technologies avoid transformers as much as possible. And thus, the transformers are no longer widely available on the market. In modern detectors they make use of the phased locked loop. This is out of the scope of this project. Concluding, given the limited time, the slope detector is implemented in the final design.

4.2.1 Design slope detector

As mentioned before, the demodulator is a circuit that has an output directly proportional to the frequency of the input. This should hold in a 75 kHz bandwidth. The steepness of the transfer should be maximised, since this directly translates into the swing of the output signal.

Two passive circuits are considered to implement the differentiator:

1. RC highpass filter
2. RLC bandpass filter

The regions of interest are in the transition band. Both of these topologies have regions with the desired transfer. The advantage of the RC filter is that it has less components, thus it is simpler. Moreover, the steepness can easily be improved by adding another identical stage. The bandpass filter has the advantage that it filters out high frequency signals. Considering the noise grows with the bandwidth; the bandwidth of the filter should be as small as possible. Moreover, the mixer and IF amplifier also create unwanted frequency components. This consideration made us choose the RLC bandpass filter.

The characteristic of an RLC circuit is shown in Fig. 4.18. The operation of the bandpass filter relies on that at resonance, the inductor and capacitor will exchange energy. As a result the inductor and capacitor will draw zero current and energy from the supply. All the current coming from the supply will then be forced through the parallel resistor. The maximum transfer of the filter will consequently be at the resonance frequency. At lower frequencies the indicators impedance will lower and this will lower the

filter's transfer. For higher frequencies the capacitor's impedance will lower and this will lower the filter's transfer.

The damping of a resonator can be described by the Q factor. The higher the Q factor, the lower the damping. The cause of damping is the dissipation of power in the resistive components. The resistive components consist of the parallel resistor, and the parasitic resistances of the inductor and capacitor. The Q factor is defined in as in Eq. 4.10, with ω being the angular frequency at which the stored energy and power loss are measured. The maximum energy stored is calculated as in Eq. 4.11. The maximum energy stored will be equal to the maximum amount of energy that can be stored in a capacitor. Because when the capacitor is fully charged, the inductor will have no potential energy. Substituting Eq. 4.11 and Eq. 4.12 into Eq. 4.13 gives a symbolic expression for Q, that depends on ω. Substituting Eq. 4.14 gives us the final expression for Q, on the resonance frequency.

$$Q(\omega) = \omega \cdot \frac{\text{maximum energy stored}}{\text{power loss}} \tag{4.10}$$

$$\text{maximum energy stored} = CV_{Crms}^2 \tag{4.11}$$

$$P_{dissipated} = \frac{V_{Rrms}^2}{R} \tag{4.12}$$

$$Q(\omega) = \omega \cdot \frac{CV_{Crms}^2}{\frac{V_{Rrms}^2}{R}} \tag{4.13}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.14}$$

$$Q(\omega_o) = R\sqrt{\frac{C}{L}} \tag{4.15}$$

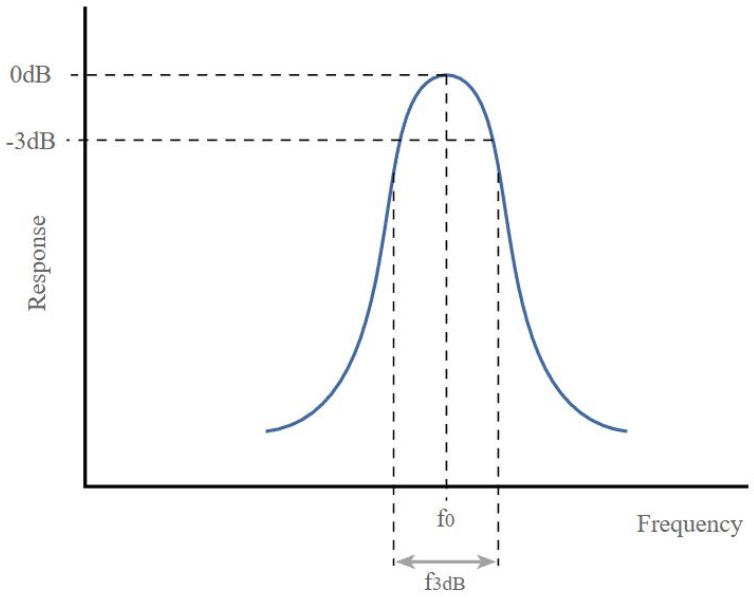


Figure 4.18: Response of an LC circuit [20]

Increasing the Q factor results in steepening the slope of the filter in the transitions band. As mentioned before, the steeper the incline of the filter, the higher the amplitude of the output of the detector. Eq. 4.15 shows that decreasing L, and increasing C, will increase the Q factor of the bandpass filter. The goal is

thus, to find the maximum capacitor and the minimum inductor value. With the IF being at 4 MHz, the resonance frequency of the bandpass circuit will be between 4 MHz and 5 MHz. At this frequency air core inductors are available that have a Q factor of above 50. The Q factor of an inductor can be translated into parasitic series resistance using Eq. 4.16.

$$R_s = \frac{\omega L}{Q} = \frac{2\pi \cdot 4\text{e}6 \cdot 130\text{e-}9}{50} = 63.35\text{m}\Omega \tag{4.16}$$

(4.17)

Available air core inductor values range from 2 nH up to 500 nH. Regarding capacitors the choice is wider. A capacitor of 10 nF was selected. This capacitor has a series resistance of less than 1 mOhm. Based on this capacitor, an inductor of 130 nH was selected. The parallel resistor of the bandpass filter is selected based on the envelope detector, this will be discussed later. The datasheets can be found in the Appendix.The resulting circuit is shown in Fig. 4.19. The preceding stage of this circuit is a buffer. The estimated voltage swing and output resistance of the buffer will be 1 V and 25 Ohm respectively.

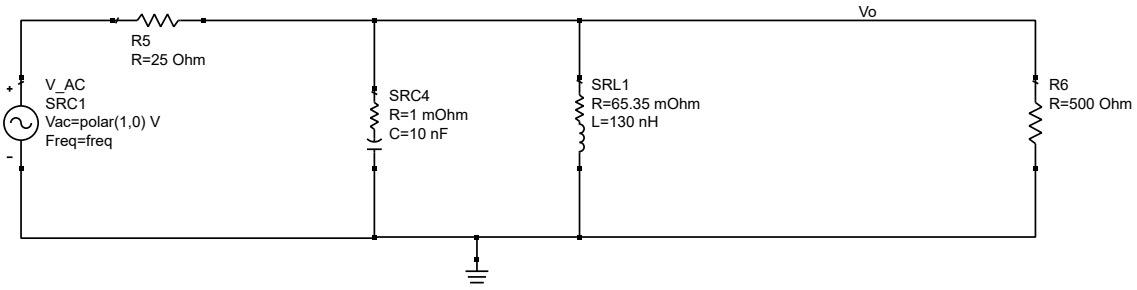
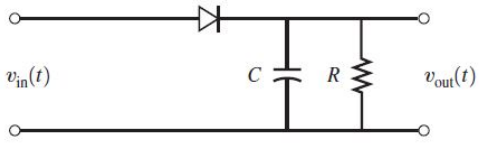
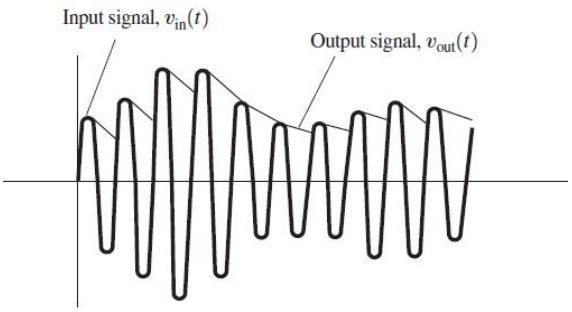


Figure 4.19: Bandpass circuit

With this circuit the signal is still AM modulated around the IF frequency. To detect the the information signal, an envelope detector is used. A standard envelope detector is again shown in Fig. 4.20a. When the voltage at node vin is above zero, the diode current will charge the capacitor. When the voltage at vin is below zero, the capacitor will discharge through the resistor. The result is the waveform of Fig. 4.20b. The RC time constant should be chosen such that the output signal is able to follow the envelope of the input signal.



(a) Diode envelope detector [8]



(b) Diode envelope detector waveform [8]

Adding the envelope results in the complete FM detector shown in Fig. 4.21. The diode in this circuit is a schottky diode. Schottky diodes have the advantage of a low forward voltage drop. Keeping in mind the maximum audio frequency of 20 kHz. The cutoff frequency is chosen at 31.8 kHz, as shown in Eq. 4.18. The final design of the detector, including the envelope detector, is shown in Fig. 4.21.

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 500 \cdot 10\text{e-}9} = 31.8 \text{ kHz} \tag{4.18}$$

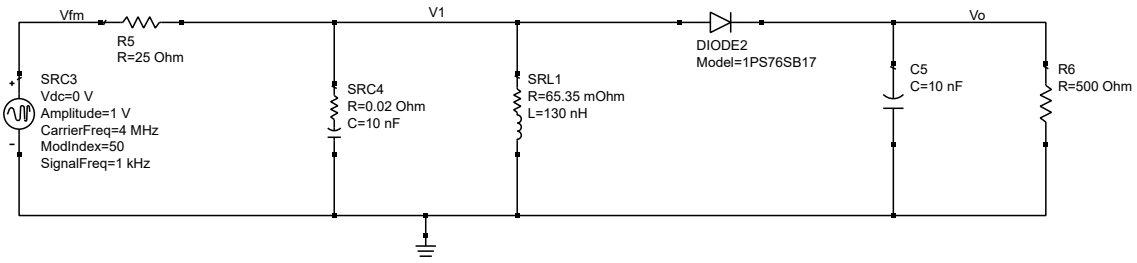
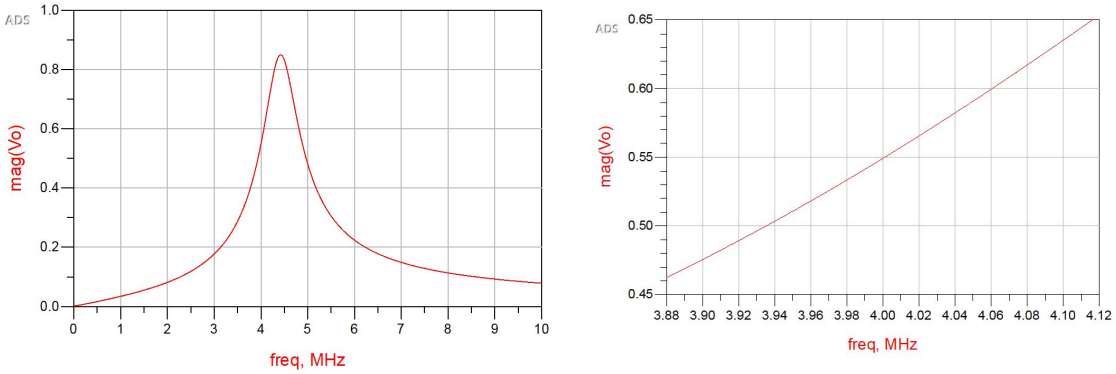


Figure 4.21: Detector circuit

4.2.2 Simulation results

To test the bandpass characteristic of the circuit of Fig. 4.19 an frequency sweep was done. The results are shown in Fig. 4.22a. In Fig. 4.22b the region of interest is shown. The input impedance shows also a bandpass characteristic, around the IF this is around 70 Ohm



(a) Transfer bandpass circuit **(b)** Region of interest bandpass filter

Figure 4.22: Simulation bandpass circuit

To simulate the whole circuit we made use of the 'VtSFF' block in ADS. The function of that block is shown in Fig. 4.23. This is a time-domain source. The modulation index is defined as in Eq. 4.19. However the modulator in this project changes the frequency of its output, based only on the amplitude of the input. So the output of the modulator resulting from an 1 kHz sine at the input, will have the same frequency deviation as an output resulting from a 20 kHz sine at the input. The difference is that the instantaneous frequency changes are more rapid in time. Analysing Eq. 4.19 and keeping in mind that the frequency deviation will remain constant. This must mean that the modulation index is dependant of the frequency of the input signal.

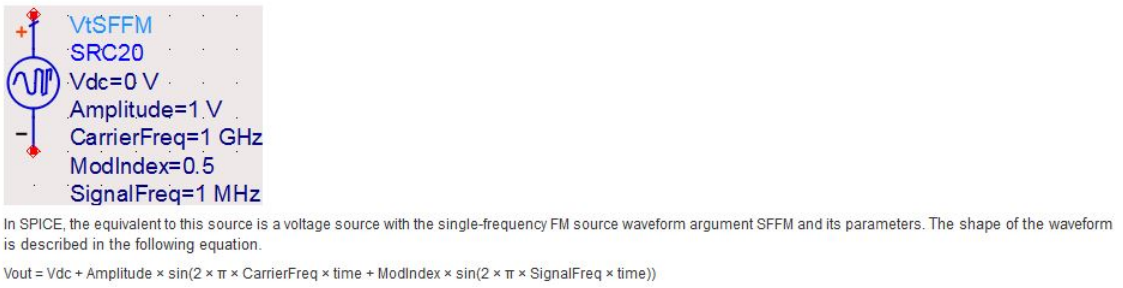


Figure 4.23: Description ADS of FM block

In Fig. 4.21 a 1 kHz tone modulation was used. The Modindex is calculated in Eq. 4.20. For a 20 kHz signal, the Modindex is calculated in Eq. 4.21. During the development of the modulator the bandwidth of the modulated signal proved to reach up to 100 kHz. For that reason the maximum frequency deviation in Eq. 4.20 and Eq. 4.21 is taken equal to 50 kHz. The transient simulation results for a 1 kHz and a 20 kHz modulation signal are shown in Fig. 4.24.

$$Modindex = \beta_f = \frac{\Delta F}{f_m} \tag{4.19}$$

$$\beta_{1\,kHz} = \frac{50kHz}{1\,kHz} = 50 \tag{4.20}$$

$$\beta_{1\,kHz} = \frac{50kHz}{20\,kHz} = 2.5 \tag{4.21}$$

The transient simulation results for a 1 kHz and a 20 kHz modulation signal are shown in Fig. 4.24

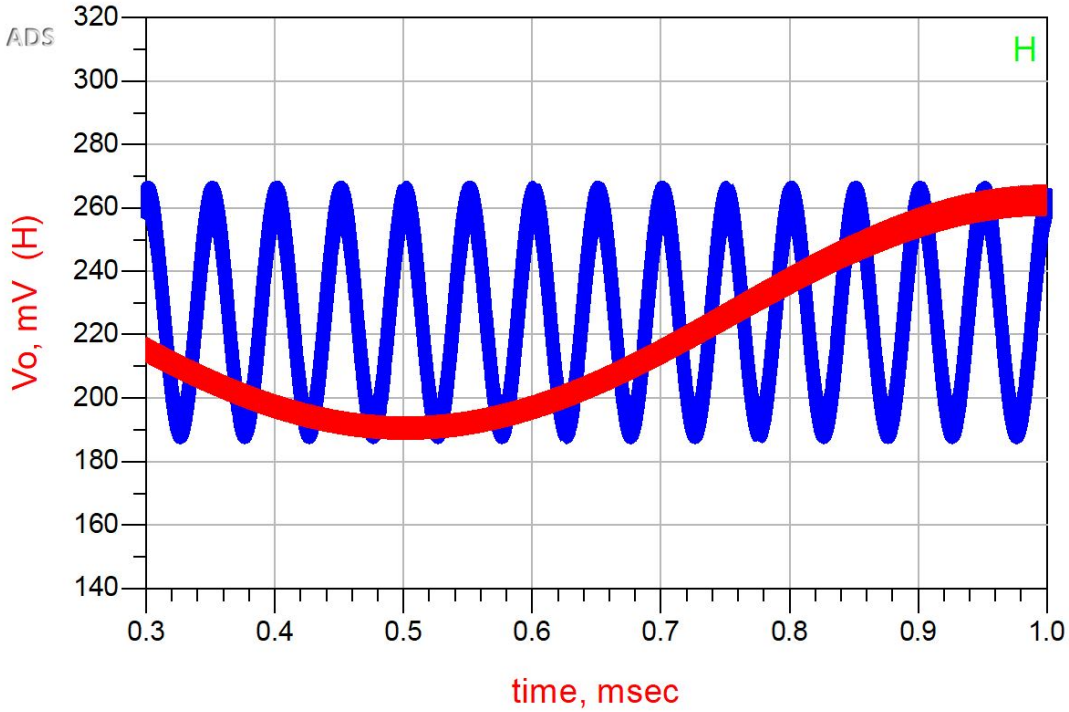
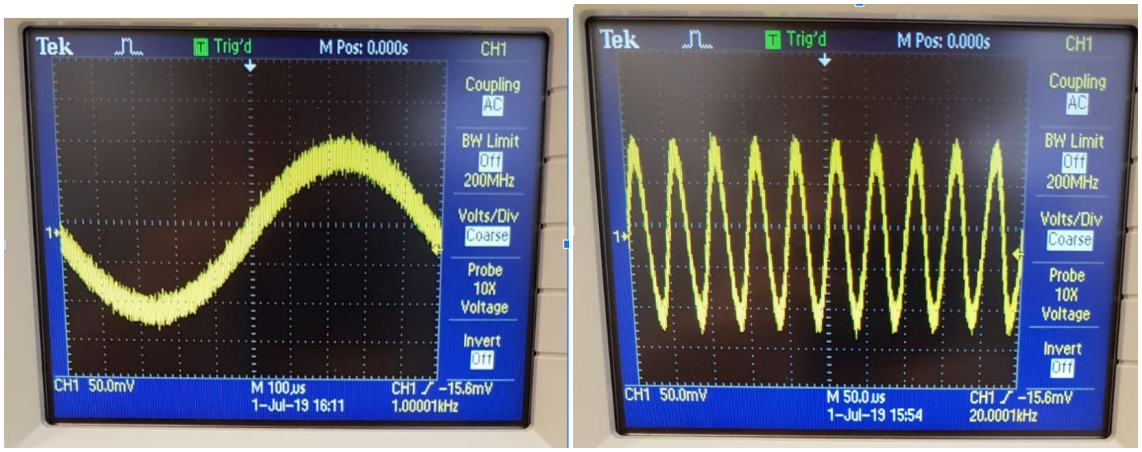


Figure 4.24: Transient simulation detector for a 1 kHz, and a 20 kHz information signal

4.2.3 Measurements

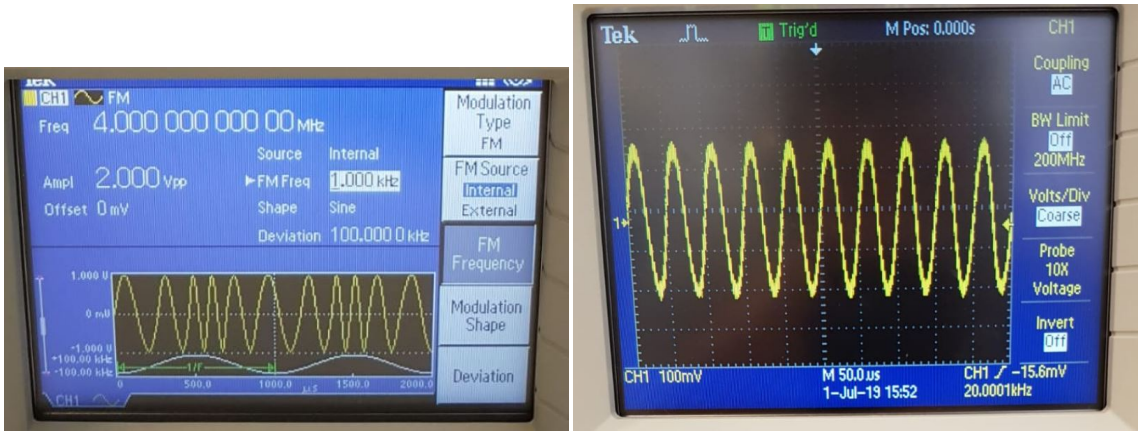
The circuit can be tested similarly as it is simulated. The ADS component shown in Fig. 4.23 is based on a realistic function generator. The circuit will thus be tested with a function generator, that has the option of FM modulation. Like in the simulation the circuit will be tested with a fixed carrier frequency of 4 MHz. The carrier will be modulated with different frequencies or even a frequency sweep in the range of 20 Hz-20 Khz, to test the detector output.

The results of the measurements are shown in Fig. 4.25. The function generator, acting as an FM source, is shown in Fig. 4.26a. Increasing the deviation frequency of the FM signal, results in better performance, as shown in Fig. 4.26b. The final circuit used for the measurements is shown in Fig. 4.27, of which the schematic is found in Fig. 4.21.



(a) Using FM frequency of 1kHz **(b)** Using FM frequency of 20kHz

Figure 4.25: Detector output for modulating signals of different frequencies



(a) Signal generator as an FM source **(b)** Using a deviation of 200kHz

Figure 4.26

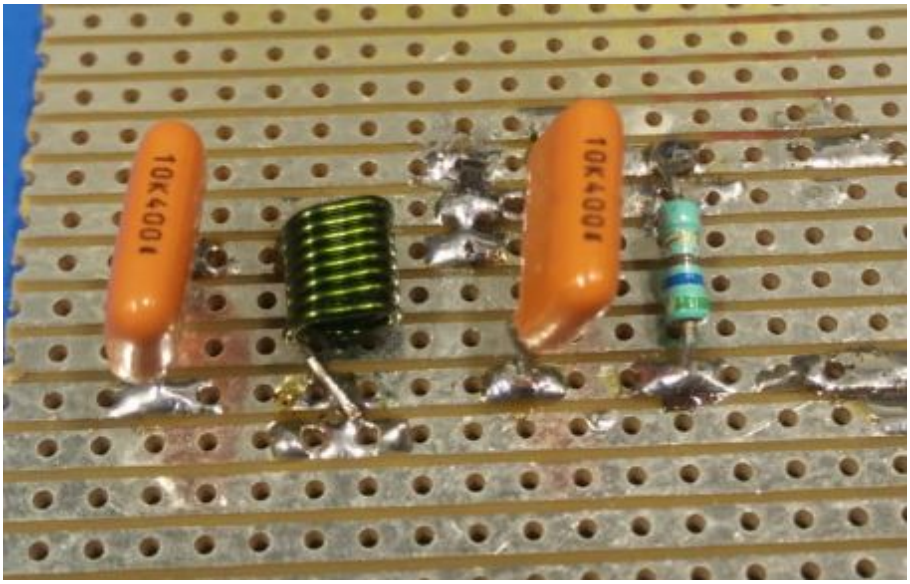


Figure 4.27: Final detector circuit

5 Discussion and conclusion

The conclusion will discuss what requirements were satisfied. After that we will display the complete circuit of the FM transceiver. The mandatory requirements were used as a starting point, on which the complete design was based. The system is using FM as its modulation technique. The tunable operating range is implemented and validated. And the system is designed around the 12 V DC source. The most important performance indicator was that the system should work with a minimum distance of 5 meters between transmitter and receiver. Since the different subblocks are not yet integrated into a working transceiver, this can not be assessed yet.

Furthermore, we had trade-off requirements. The trade-off requirements were mostly related to specified bandwidth or frequency of operation. During the design some concessions were made, in order to get a working end result.

In the simulation results of the modulator section we've seen that the peak to peak output voltage varies between 8.25 V and 10.71 V for the operating frequency. From this we can conclude that the maximum variation of the output signal is less than 2.5 V. This means that the requirement of the output signal level is satisfactory.

Also as can be seen in the simulations of the modulator that the bandwidth is 75 kHz at a carrier frequency of 88 MHz and 102 kHz for a carrier frequency of 108 MHz. The last one is above the 75 kHz specified by the requirements. This however not a big problem since this can be easily compensated for by adjusting the input voltage level.

The requirement for voltage swing of the modulator is partially met. The voltage swing of at least 5 V is met for less than the entire operating range since the voltage swing is 'only' just above 4 V for an operating frequency of 88 MHz.

The final design of the mixer has a gain of 10. The original requirement was only that it should not weaken the signal. The detector needed to have a voltage swing of at least 20 mV. In simulation an output of 35 mV was achieved. However these simulations are based on assumptions of the input signal.

The final transmitter is is shown in Fig. 5.1. The final receiver is shown in Fig. 5.2.

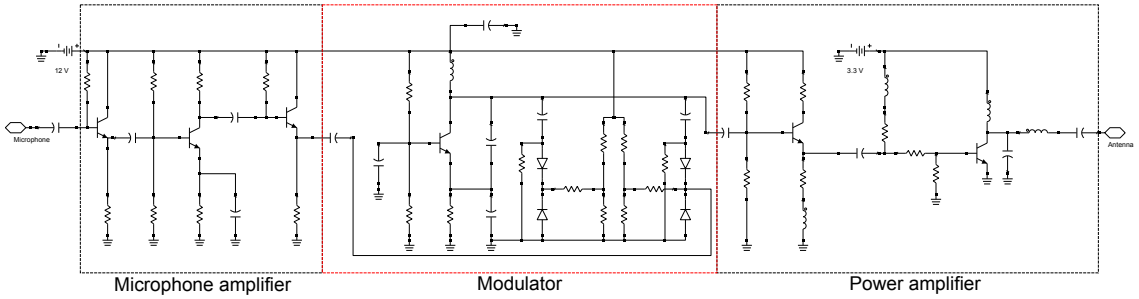


Figure 5.1: Transmitter

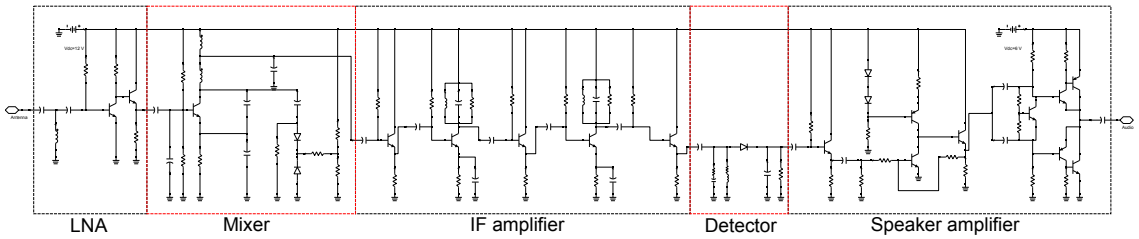


Figure 5.2: Receiver

5.1 Future work

During the design we ran into multiple disadvantages of the chosen intermediate frequency in the detector. As is explained in section 4.1, the IF of 4MHz results in a image frequency which is inside the required tuning range. As a result, the image frequencies can never be filtered before the mixer, since the information signal could also appear at the possible image frequencies.

The IF was chosen mainly to be able to use the low complexity slope detector. A slope detector designed for a IF around 10MHz would need component values that are not practically available. for future work the recommendation is thus, to use a different detector, so that a higher IF can be used.

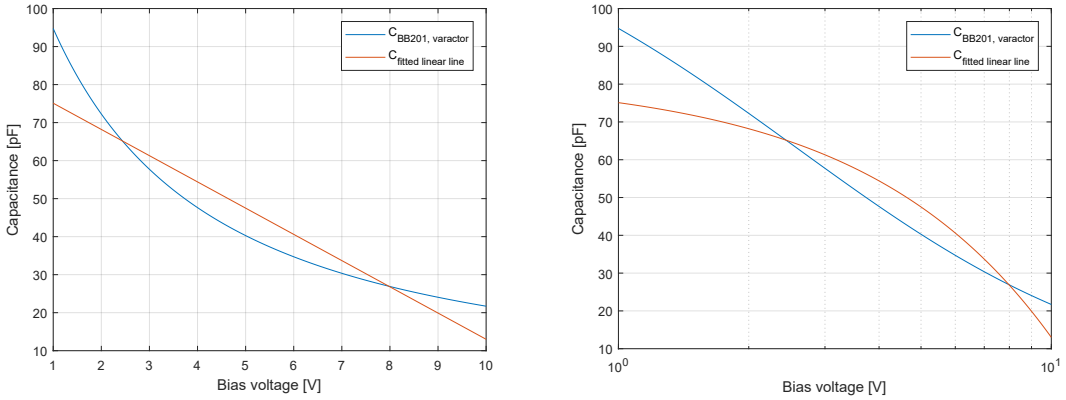
The mixer was integrated into a local oscillator, to reduce complexity. However this resulted into conflicting requirements for the capacitor at the base of the transistor, further explained in section 4.1. The capacitor should provide an AC ground for the oscillator, and it should not influence the RF input. Since the RF frequency is variable, and always close to the oscillator frequency, a trade-off had to be made. The recommendation for future work is thus, to split the oscillator and mixer, so that they can be optimized independently.

Appendices

A Additional figures & calculations

A.1 Modulator - design process

The following two figures show the capacitance voltage graphs of a BB201 varactor (blue line). There is also a orange line in the graphs. This linear line is created with the Matlab plot fitting tool.
These graphs make clear that with linear axes, the varactor line is curved, but on a logarithmic scale it is by approximation linear for this interval. In section 3.3 is argumented that because of this the frequency voltage characteristic of the modulator is (close to being) linear compared to exponential as can be seen in Fig. A.2. The Matlab code which has created these files can be found in section B.1



(a) linear axes **(b)** X-axis logarithmic

Figure A.1: Real varactor, capacitance vs voltage plot & linear fitted line

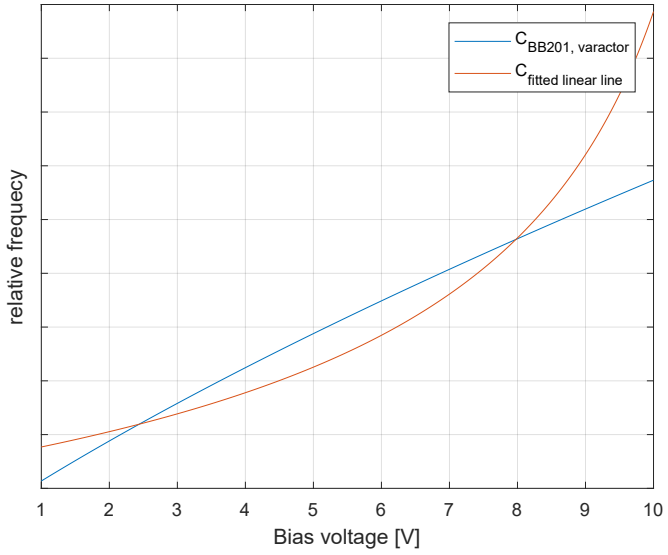


Figure A.2: Frequency voltage relation for a varactor and a linear varicable capacitor

A.2 Modulator - final design

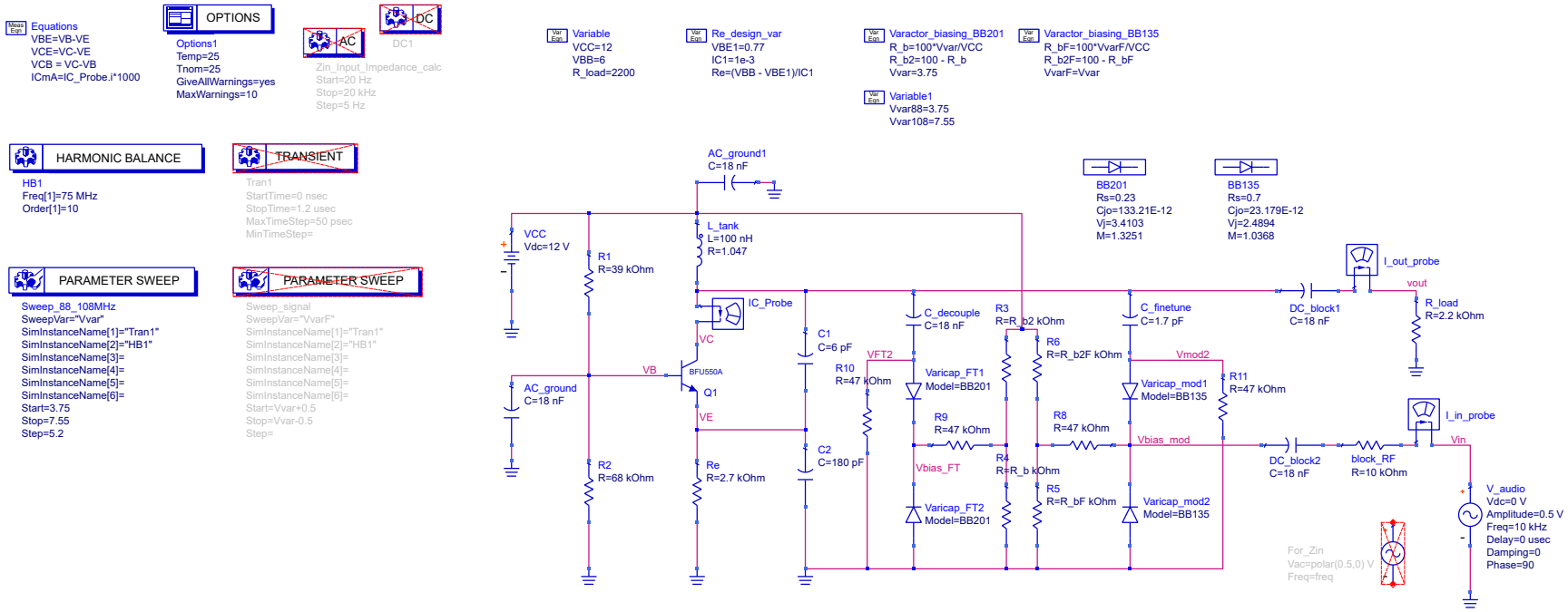


Figure A.3: Final modulator design in ADS simulator

A.3 Mixer - final design

Derivation of Eq. 4.5 from subsection 4.1.1, with the help of Eq. A.5 and Eq. A.6:

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{A.1}$$

$$C_{eq}(f) = \frac{1}{(2\pi f)^2 \cdot L} \tag{A.2}$$

$$C_{var}(f) = C_{eq}(f) - C_{12'} \tag{A.3}$$

$$= \frac{1}{(2\pi f)^2 \cdot L} - \frac{(C_1 + C_{BJT}) \cdot C_2}{(C_1 + C_{BJT}) + C_2} \tag{A.4}$$

Approximate equivalent capacitance of the mixer circuit:

$$C_{12'} = \frac{(C_1 + C_{BJT}) \cdot C_2}{(C_1 + C_{BJT}) + C_2} \tag{A.5}$$

$$C_{eq} = C_{12'} + C_{var} \tag{A.6}$$

Final mixer design in ADS simulator:

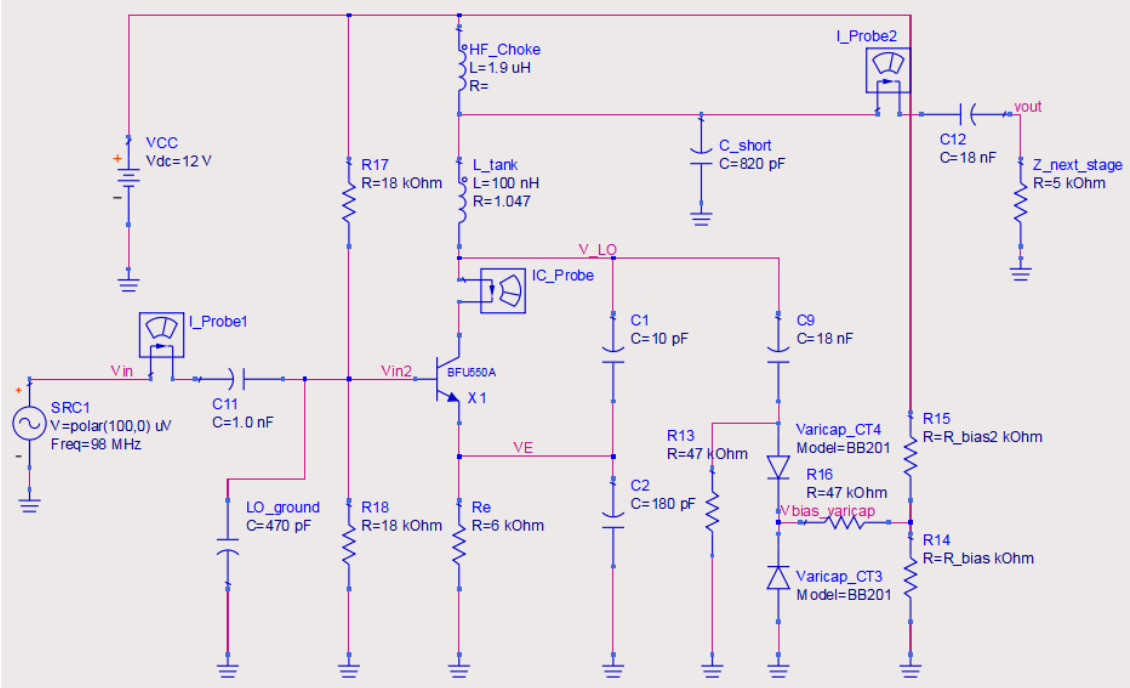


Figure A.4: Final mixer design in ADS simulator

A.4 Mixer - simulation results

In this section additional figures with simulation results can be seen.

These figures are the same as Fig. 4.5 in subsection 4.1.2, but for different f_{RF}. The first is at an f_{RF} of 88 MHz, the second at an $_{RF}$ of 108 MHz, but this one has some additional graphs that show the IF and RF peaks in more detail.

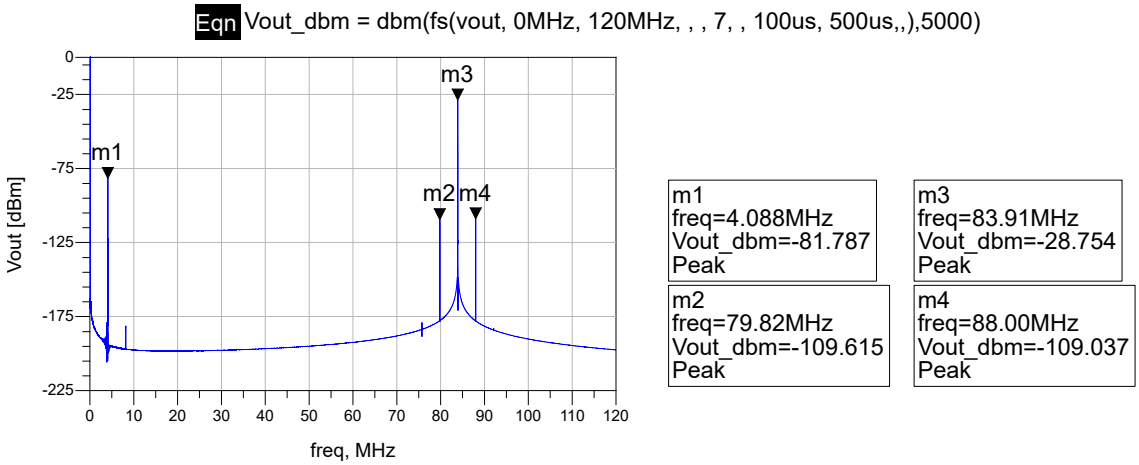


Figure A.5: Transient simulation of the mixer, f_{RF} = 88 MHz, $f_{LO} \approx$ 84 MHz

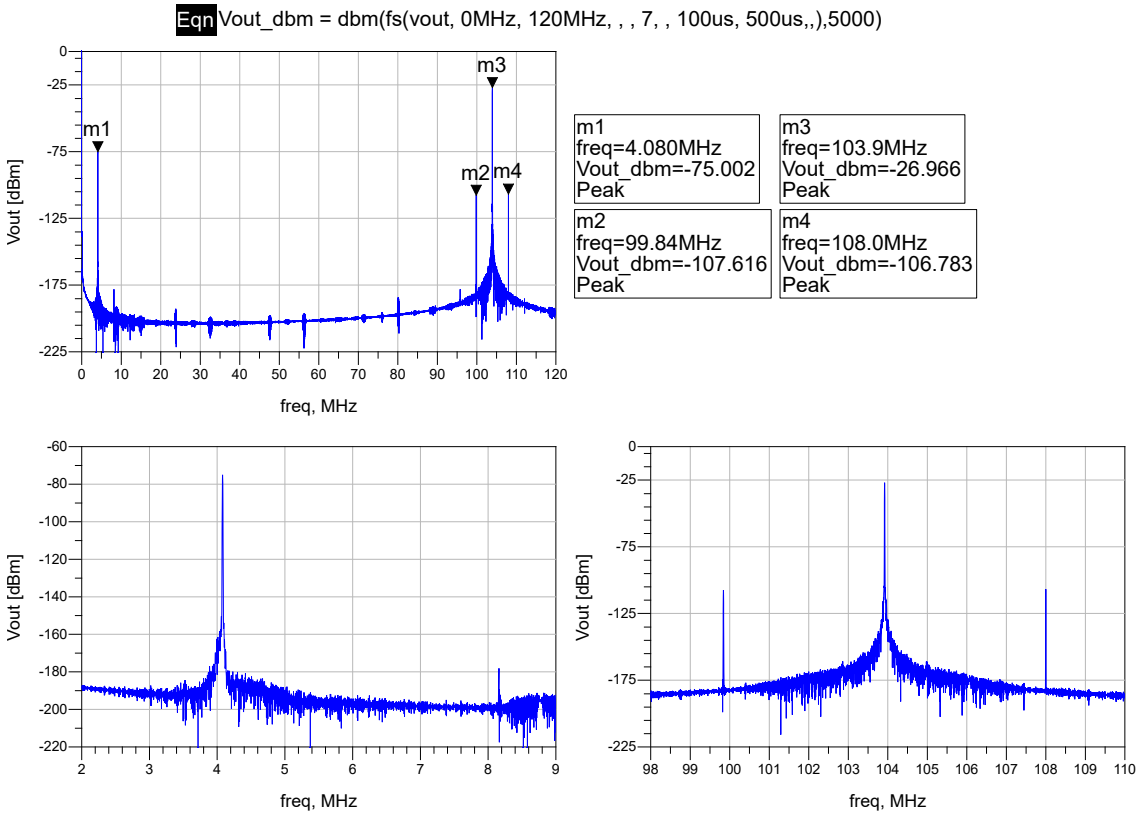


Figure A.6: Transient simulation of the mixer, f_{RF} = 108 MHz, $f_{LO} \approx$ 104 MHz, with more detailed graphs

The following figures are the same as Fig. 4.6, which is displayed in subsection 4.1.2, but these figures are at another frequency.

Harmonics - Mixer

harmindex	freq	mag(Vin)	mag(vout)
0	0.000000 Hz	0.00000	12.00000
1	4.00050 MHz	0.00000	0.00095
2	8.00099 MHz	0.00000	5.84429E-9
3	79.9990 MHz	0.00000	0.00001
4	83.9995 MHz	0.00000	0.12667
5	88.0000 MHz	0.00010	0.00001
6	92.0005 MHz	0.00000	3.39628E-8
7	163.999 MHz	0.00000	1.29292E-7
8	167.999 MHz	0.00000	0.00041
9	172.000 MHz	0.00000	2.86043E-7

Gain of the mixer

harmindex	Mixer_GAIN
<invalid>	9.513

Eqn F_IFmag=mag(mix(vout, {-1,1}))
Eqn F_IFmag_IN=mag(mix(Vin, {0,1}))
Eqn Mixer_GAIN=F_IFmag/F_IFmag_IN

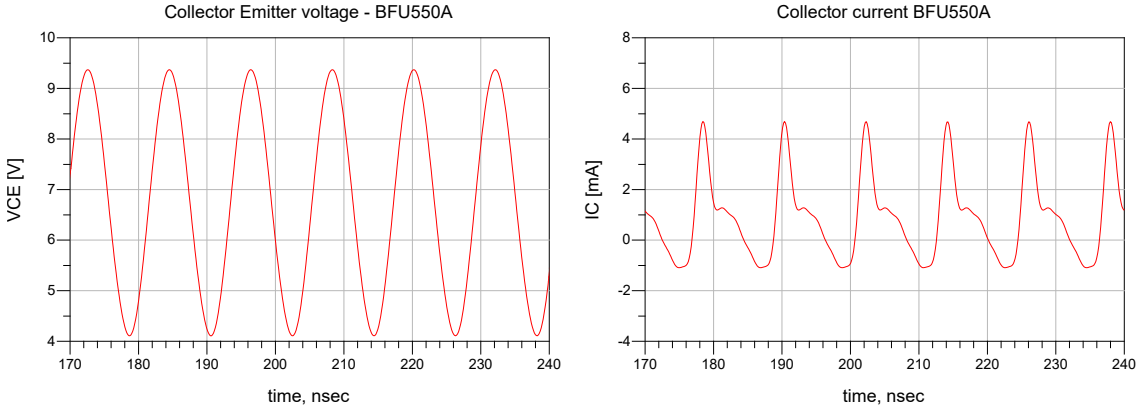


Figure A.7: Harmonic balance simulation - gain of the mixer at f_{RF} = 88 MHz

Harmonics - Mixer

harmindex	freq	mag(Vin)	mag(vout)
0	0.000000 Hz	0.00000	12.00000
1	4.00054 MHz	0.00000	0.00220
2	8.00108 MHz	0.00000	1.55919E-6
3	99.9989 MHz	0.00000	0.00002
4	103.999 MHz	0.00000	0.14415
5	108.000 MHz	0.00010	0.00001
6	112.001 MHz	0.00000	3.86284E-6
7	203.998 MHz	0.00000	2.25482E-7
8	207.999 MHz	0.00000	0.00041
9	211.999 MHz	0.00000	1.92335E-7

Gain of the mixer

harmindex	Mixer_GAIN
<invalid>	22.005

Eqn F_IFmag=mag(mix(vout, {-1,1}))
Eqn F_IFmag_IN=mag(mix(Vin, {0,1}))
Eqn Mixer_GAIN=F_IFmag/F_IFmag_IN

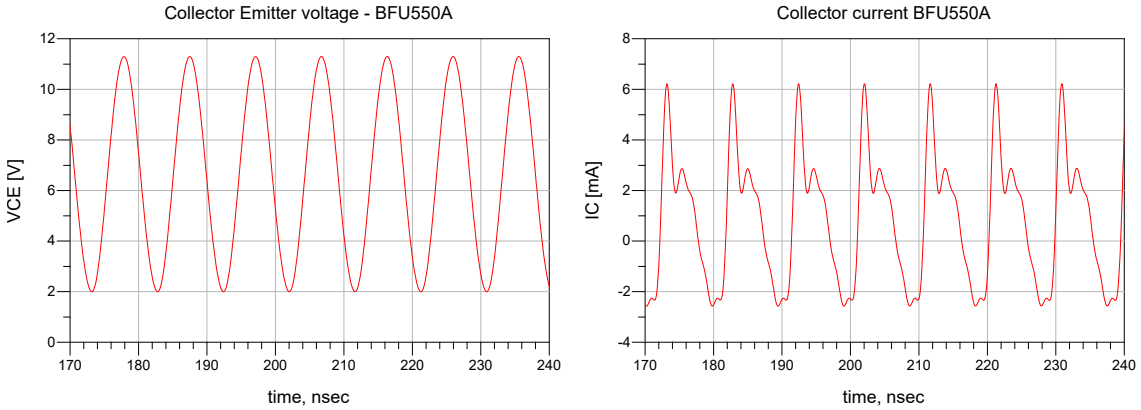


Figure A.8: Harmonic balance simulation - gain of the mixer at f_{RF} = 108 MHz

B Matlab files

B.1 Modulator - design process

This Matlab function is used to explore the differences of using a linear variable capacitor device such as a trimmer capacitor vs a non-linear varicap diode. As is shown by the plots, the varicap diode has an exponential voltage to capacitance relation and because of this the transfer in the voltage frequency plot is almost linear.

```
%Made by Jasper van Vliet
%Date: 14-06-2019
%
%Investigation linearity improvements varactor vs linear device

%%
Vin = [1:0.01:10];

for i=1:length(Vin)
    y(i) = -6.9*Vin(i)+82; %linearly fitted line of BB201 capacitance
    C(i) = BB201_Vin(Vin(i));
    f_varactor(i)=1/((C(i))^(0.5));
    f_linear(i) = 1/((y(i))^(0.5));
end
%Some plots
figure(1)
plot(Vin,f_varactor); hold on
plot(Vin,f_linear);
figure(2)
plot(Vin,C); hold on
plot(Vin,y);
figure(3);
semilogx(Vin,f_varactor); hold on
semilogx(Vin,f_linear);
figure(4)
semilogx(Vin,C); hold on
semilogx(Vin,y);

%% Make plots for thesis
close all

figure(1)
plot(Vin,C); hold on
plot(Vin,y);
ylabel('Capacitance [pF]'); xlabel('Bias voltage [V]');
%title('Capacitance vs Voltage relation, varactor vs linear');
grid on;
legend('C_{BB201, varactor}','C_{fitted linear line}')
%set(gcf, 'Position',  [100, 100, 400, 300]) %position x,y, size, x,y

figure(2)
semilogx(Vin,C); hold on
semilogx(Vin,y);
ylabel('Capacitance [pF]'); xlabel('Bias voltage [V]');
%title('Capacitance vs Voltage relation, X-axis logarithmic');
```

```
grid on;
legend('C_{BB201, varactor}','C_{fitted linear line}')
%set(gcf, 'Position',  [550, 100, 400, 300])

figure(3)
plot(Vin,f_varactor); hold on
plot(Vin,f_linear);
set(gca,'YTickLabel',{'','','','','','','','','','',''});
ylabel('relative frequecy'); xlabel('Bias voltage [V]');
%title('Frequency vs voltage');
grid on;
legend('C_{BB201, varactor}','C_{fitted linear line}')
%set(gcf, 'Position',  [1000, 100, 400, 300])
```

Listing B.1: Comparison between a varicap diode vs a linear capacitance device, for the use as variable capacitor in the modulator circuit

B.2 Modulation bandwidth

This Matlab function is used in the early design stages of the modulator. This Matlab function is used to calculate the input peak to peak voltage needed for a bandwidth of 75 kHz for the outer operational frequencies (88 MHz and 108 MHz). The results lead us to the conclusion that the single varactor design had to be improved.[1]

```
%Made by Jasper van Vliet
%Date: 16-06-2019
% Small script to calculate voltage deviation of BB135 varactor
%at realistic bias voltage levels for this varactor (for in thesis)
%% Plotting BB135 capacitance vs voltage
clear all; close all;

Vin = [0.1:0.01:28]; %real bias range is around 1 to 11v realistically
for i=1:length(Vin)
    C135(i) = BB135_Vin(Vin(i));
end
semilogx(Vin,C135) %Capacitance values BB135 plotted

%% Calculating Voltage deviation for
C_108_fF = 30.2e-3; %value needed in pF
C_88_fF = 55.8e-3;

%capacitance at realistic bias voltage levels for the
% operational frequency range:
bias = 10; %DC bias: 10V
C_deviation_needed = 11; %11pF deviation needed for 88 to 108 MHz
C_10v_bias = BB135_Vin(bias); %capacitance at 10v bias -> C at 108MHz
C_low_bias = C_10v_bias + C_deviation_needed; %C, 88MHz (higer C lower f)

%capacitance values needed for 108 and 88MHz with proper other
%capacitances in the circuit.
C108 = C_10v_bias;
C88 = C_low_bias;

%calculate voltage deviation for 75kHz bandwidth:
V_dev_88 = BB135_Cin(C88) - BB135_Cin(C88 + C_88_fF);
```

[1] This file was created for the thesis to illustrate the design process. The original calculations where done on paper.

```
V_dev_108 = BB135_Cin(C108) - BB135_Cin(C108 + C_108_fF);
```

Listing B.2: Matlab file used for determining the right varactor for the modulator design

B.3 Modulator - final design

The function listed below plots the total tank capacitance, bias voltage vs frequency and frequency vs bias voltage. A fitted line is made with for the frequency vs bias voltage graph with the basic fitting tool of Matlab. With this formula, the bias voltage needed to get a certain carrier frequency can be calculated.

```
%Made by Jasper van Vliet
%Date: 30-05-2019

% Final C analysis & calculation, colpitt v7 design.
% Determine bias voltage to use in design, without trail and error methode
clear all; close all;
%%
% note: Ceq_tot function contains hardcoded values from the design!
V_bias = [1:0.05:10];
C1_feedback = 6;            %C1 feedback capacitor value
Ceq = zeros(length(V_bias),1);
for i=1:length(V_bias)
    Ceq(i) = Ceq_tot(V_bias(i),C1_feedback);
end

%% Make graph total capacitance vs bias voltage applied to tuning varactor
figure(1);
semilogx(V_bias, Ceq);
hold on;
ylabel('Capacitance [pF]'); xlabel('Bias voltage [V], log scale');
title('Total tank capacitance of the Collpit Oscillator');
grid on

%%
L=100e-9; %Inductor is 100nH
frequency = zeros(length(Ceq),1);
for i=1:length(Ceq)
    frequency(i) = 1/(2*pi*(L*Ceq(i)*10^(-12))^0.5);
end
figure(2);
plot(V_bias, frequency);
ylabel('Frequency [Hz]'); xlabel('Bias voltage [V]');
hold on
figure(3);
plot(frequency, V_bias);
xlabel('Frequency [Hz]'); ylabel('Bias voltage [V]');
hold on
%% Fitted line from above graph (fig. 3) to determine Bias voltages
% x = frequency
% y = Bias voltage

%y = p1*x^4 + p2*x^3 + p3*x^2 + p4*x + p5 ;

%Coefficients:
  p1 = 1.1969e-32;p2 = -2.6488e-24;p3 = 7.5706e-16;p4 = 1.7862e-08;p5 =
    -3.3817;

  x = 88e6;
```

```
  Vb_88MHz = p1*x^4 + p2*x^3 + p3*x^2 + p4*x + p5 ;
  x = 108e6;
  Vb_108MHz = p1*x^4 + p2*x^3 + p3*x^2 + p4*x + p5 ;

  Vb_88MHz
  Vb_108MHz
```

Listing B.3: Matlab file which is used for the final analysis of the modulator design

This Matlab file is created to check if the varactor capacitance function with a voltage input parameter created the same plot as in the datasheets of the varactors. Also the function with a capacitance input parameter where checked because these where made without knowing if they would work.

```
%Made by Jasper van Vliet
%Date: 30-05-2019
% This Matlab file is created to check if the Varicap_Vin and Cin
% functions work as intended and to check visuals with the datasheet.
%
% Capacitance values calculated from Vin functions, then put back into
% Cin functions to check if produces same Vin again.

%% BB135,201,207 function verification
clear all
close all
V_in = [1:0.01:10];
for i = 1:length(V_in)
    C135(i) = BB135_Vin(V_in(i));
    C201(i) = BB201_Vin(V_in(i));
    C207(i) = BB207_Vin(V_in(i));
end

figure(135)
semilogx(V_in, C135);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB135 varicap function plotted'); grid on; hold on;
figure(201)
semilogx(V_in, C201);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB201 varicap function plotted'); grid on; hold on
figure(207)
semilogx(V_in, C207);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB207 varicap function plotted'); grid on; hold on

%% Now test Cin functions and use these values also for plotting
%-> should be the same curves as before
for j = 1:length(C135)
    V135(j) = BB135_Cin(C135(j));
    V201(j) = BB201_Cin(C201(j));
    V207(j) = BB207_Cin(C207(j));
end
figure(135)
semilogx(V135, C135); legend('data1','data2')
figure(201)
semilogx(V201, C201); legend('data1','data2')
figure(207)
semilogx(V207, C207); legend('data1','data2')
```

Listing B.4: Matlab file to check validity of created functions

This function is made to investigate if a certain varicap is able to meet the bandwidth requirements for the final modulator design. The first two options (BB201, BB207) did not, however the BB135 varicap did. There are no plots in this file since the results are stored in the variables. This was sufficient enough to determine if a varactor was up to the task.

```
%By: Jasper van Vliet
%Date: 30-05-2019
%Description: looking for varicap with certain range for FM 75kHz sweep
%consistency for different bias voltages
%Turns out that BB201 & BB207 are no good candidate but
%BB135 in series with a capacitor is.

%% ####____####____####____####____####____####____####____####____####
clear all; close all;
%% Calculate some delta C values for given delta V values
Vin = [0,1,2,3,4,5,6,7,8,9];
for i = 1:length(Vin)
    Cdelta(i) = BB201_Vin(Vin(i)) - BB201_Vin(Vin(i)+1);
end

%% Create Matrix with capacitance:
% Test multiple BB201 varicaps in series to achieve proper capacitace
% Result, so many in serie needed, not a good solution.

Vpp = 1; %peak to peak voltage
Vin = [0,1,2,3,4,5,6,7,8,9];    %bias voltages
CC = [14,13.5,13,12.5];         %capacitance values [pF] to try out
Cdelta_BB201 = zeros(length(CC)+1,length(Vin)+1); %pre-allocate
Cdelta_BB201(2:length(CC)+1,1)=CC'; %First column: CC reference values
Cdelta_BB201(1,2:length(Vin)+1)=Vin+0.5; %First row: Vbias ref values
for j = 1:length(CC)            %Create matrix
    C = CC(j);
    for i = 1:length(Vin)
        a = BB201_Vin(Vin(i));
        b = BB201_Vin(Vin(i)+Vpp);
        C1 = (1/a + 1/a + 1/a + 1/a)^-1; %Testing multiple BB201 in series
        C2 = (1/b+1/b+1/b+1/b)^-1; %Testing multiple BB201 in series
        A = Series_C(C1,C);
        B = Series_C(C2,C);
        Cdelta_BB201(j+1,i+1) = A-B;
    end
end
Cdelta_BB201           % Display results

%% Realistical only one varicap (not multiple in parallel)
% BB207 investigatio:
% rerun the value table Cdelta.

%%
% --- BB201 & BB207 in series with CC ---

% TARGET VALUES: 0.05568 - 0.03013 [pF] for 75kHz sweep on 88 - 108MHz

% BB201 & BB207 results:
% BB207 niet geschikt, geen range
% BB201 volledige 0.5-9.5V range nodig. Niet handig. BB135 investigation

% BB201 shows not enough tuning capacitance to keep the limited frequency
```

```
% sweep of 75kHz

%Pre-defined values
Vpp = 1;                    %peak to peak voltage of input audio signal
Vin = [0,1,2,3,4,5,6,7,8,9];%Bias voltages
CC = [4.0,3.5,3.4,3.3,3.2,3.1,3.0,2.9,2.8,2.7,2.6,2.5,2.0];%C_series [pF]
Cdelta_BB201 = zeros(length(CC)+1,length(Vin)+1); %pre-allocate matrix
Cdelta_BB207 = Cdelta_BB201;                      %pre-allocate matrix
Ceq1_BB201 =zeros(length(Vin),1); Ceq2_BB201=Ceq1_BB201; %pre-allocate
Ceq1_BB207 =zeros(length(Vin),1); Ceq2_BB207=Ceq1_BB207; %pre-allocate
Cdelta_BB201(2:length(CC)+1,1)=CC';    %first column are the capacitances
Cdelta_BB201(1,2:length(Vin)+1)=Vin+0.5;%first row are the voltages
Cdelta_BB207(2:length(CC)+1,1)=CC';    %first column are the capacitances
Cdelta_BB207(1,2:length(Vin)+1)=Vin+0.5;%first row are the voltages

%Precalculate BB201 and BB207 package capacitances (two diode in series)
for i = 1:length(Vin)
    C1 = BB201_Vin(Vin(i));
    C2 = BB201_Vin(Vin(i)+Vpp);
    Ceq1_BB201(i) = Series_C(C1,C1); %C_effective @ Vin = x [V]
    Ceq2_BB201(i) = Series_C(C2,C2); %C_effective @ Vin = x+1 [V]
    C7 = BB207_Vin(Vin(i));
    C8 = BB207_Vin(Vin(i)+Vpp);
    Ceq1_BB207(i) = Series_C(C7,C7); %C_effective @ Vin = x [V]
    Ceq2_BB207(i) = Series_C(C8,C8); %C_effective @ Vin = x+1 [V]
end

% Calculate BB201 & BB207 in series with a capacitance
for j = 1:length(CC)
    C = CC(j);                          % series capacitance
    for i = 1:length(Vin)
        A1 = Series_C(Ceq1_BB201(i),C); % equivalent capacitance
        B1 = Series_C(Ceq2_BB201(i),C); % equivalent capacitance
        A7 = Series_C(Ceq1_BB207(i),C); % equivalent capacitance
        B7 = Series_C(Ceq2_BB207(i),C); % equivalent capacitance
        Cdelta_BB201(j+1,i+1) = A1-B1;  % difference in cap. @ bias level
        Cdelta_BB207(j+1,i+1) = A7-B7;  % difference in cap. @ bias level
    end
end
%Display results:
Cdelta_BB201
Cdelta_BB207

%% Add info for BB135
%Pre-defined values
Vpp = 1;                        %peak to peak voltage
Vin = [0,1,2,3,4,5,6,7,8,9];    %Bias voltages
CC = [1:0.1:2];                 %series capacitance pF
Cdelta_BB135 = zeros(length(CC)+1,length(Vin)+1); %create matrix size
Ceq1_BB135 =zeros(length(Vin),1); Ceq2_BB135=Ceq1_BB135;
Cdelta_BB135(2:length(CC)+1,1)=CC';     %first column are the capacitances
Cdelta_BB135(1,2:length(Vin)+1)=Vin+0.5;%first row are the voltages


%Precalculate
for i = 1:length(Vin)
    C3 = BB135_Vin(Vin(i));
    C5 = BB135_Vin(Vin(i)+Vpp);
```

```
    Ceq1_BB135(i) = Series_C(C3,C3); %C_effective @ Vin = x [V]
    Ceq2_BB135(i) = Series_C(C5,C5); %C_effective @ Vin = x+1 [V]
end

% Calculate BB135in series with a capacitance
for j = 1:length(CC)
    C = CC(j);                          % series capacitance
    for i = 1:length(Vin)
        A3 = Series_C(Ceq1_BB135(i),C); % equivalent capacitance
        B3 = Series_C(Ceq2_BB135(i),C); % equivalent capacitance
        Cdelta_BB135(j+1,i+1) = A3-B3;  % difference in cap. @ bias level
    end
end
%Display results:
Cdelta_BB135
```

Listing B.5: Caption test

The following two functions are made to investigate and visualise the capacitance of two varactors in series with a capacitance. This is used in the process of meeting the bandwidth requirement for the whole operating range.

```
%Made by Jasper van Vliet
%Date: 29-05-2019
% Plots values read from varicap graph and function to compare them.
% Also determine capacitance function for a series capacitance added

close all
clear all
%%

%points from datasheet
%values read from graph in BB201 varicap (may not be very accurate but are
%used to see if function is plotted correct)
C(:,1)=[1,2,3,4,5,6,7,8,9,10]; %voltage [V]
C(:,2)=[98,75,60,48,40,34,29,26,23,21]; %capacitance [pF]
cap = C(:,2);
volt = C(:,1);

%% Plot BB201 function Capacitance vs Voltage with Voltage on log scale

Rs = 0.23;
Cj0 = 133.21e-12;
Vj = 3.4103;
M = 1.3251;

V_in = [1:0.002:10];

for i = 1:length(V_in)
    Cj(i) = (Cj0/(1+V_in(i)/Vj)^M)*10^12; %*10^12 -> convert to pF
end

figure;
semilogx(V_in, Cj);
hold on;
semilogx(volt,cap);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB201 varicap function & datasheet points plotted');
grid on

```

```
%% Plot CC contected BB201 capacitance (result: half of single capacitance)
for i = 1:length(Cj)
    C1(i) = Cj(i)*Cj(i) / (Cj(i)+Cj(i)); %
end

semilogx(V_in, C1);


%% Plot capacitance for series of serie-capacitances with BB201

CC = [100,50,20,10,5];
figure;
semilogx(V_in, C1); %original (no series C)
hold on
% for j = 1:length(CC)
%     C = CC(j);
%     for i = 1:length(Cj)
%         Ceq(i) = C1(i)*C / (C1(i)+C); %
%     end
%     semilogx(V_in, Ceq);
% end

ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB201 capacitance (CC conected) with series capacitance');
grid on
legend('C_{series} = \infty',...
    ['C_{series} = ' num2str(CC(1))],['C_{series} = ' num2str(CC(2))],...
    ['C_{series} = ' num2str(CC(3))],['C_{series} = ' num2str(CC(4))],...
  ['C_{series} = ' num2str(CC(5))])
```

Listing B.6: Caption test

```
%Made by Jasper van Vliet
%Date: 29-05-2019
% Plots values read from varicap graph and function to compare them.
% Also determine capacitance function for a series capacitance added

clear all; close all;
%%
%points from datasheet
%values read from graph in BB201 varicap
C(:,1)=[1,2,3,4,5,6,7,8,9,10]; %voltage [V]
C(:,2)=[82,63,51,43.5,37,33.5,29,26,24.5,23]; %capacitance [pF]
cap = C(:,2);
volt = C(:,1);

%%

Rs = 0.3;
Cj0 = 122.50e-12;
Vj = 1.4881;
M = 0.81153;

V_in = [1:0.1:10];

for i = 1:length(V_in)
    Cj(i) = (Cj0/(1+V_in(i)/Vj)^M)*10^12; %*10^12 -> convert to pF
end

```

```
figure;
semilogx(V_in, Cj);
hold on;
semilogx(volt,cap);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB207 varicap function & datasheet points plotted');
grid on

%%
for i = 1:length(Cj)
    C1(i) = Cj(i)*Cj(i) / (Cj(i)+Cj(i)); %
end

semilogx(V_in, C1);


%%
close all;
figure;
semilogx(V_in, Cj);
hold on;
semilogx(volt,cap);
ylabel('Capacitance [pF]'); xlabel('Voltage [V], log scale');
title('BB207 varicap function & datasheet points plotted');
grid on

CC = [5,10,20,50,100,200,500];
for j = 1:length(CC)
    C = CC(j);
    for i = 1:length(Cj)
        Ceq(i) = C1(i)*C / (C1(i)+C); %
    end
    semilogx(V_in, Ceq);
end
```

Listing B.7: Caption test

B.4 Mixer matlab files

This function is used to check if a varactor is suitable as varactor in the mixer design. To visualise this, a plot is made that shows which part of the varactor capacitance range is used for the operational frequency range of the mixer.

```
%Made by Jasper van Vliet
%Date: 03-06-2019
%
% Varactor capacitances needed for Mixer design v1.5
% check if varactor can handle range needed

%%
clear all; close all;
%%
%Capacitance values determined from simulation after initial guess by
%calculation:
Cvar_need =     [27.3 19.28 18 13.6];
freq_related =  [84   94    96 104];

%get voltage values for Cvar_need values
```

```
for i=1:length(Cvar_need)
    Vvar_need(i) = BB201_Cin(2*Cvar_need(i));
end


%% calculate plotting stuff BB201 varicap
% (from Varicap_function_BB201.m file)
Rs = 0.23;
Cj0 = 133.21e-12;
Vj = 3.4103;
M = 1.3251;

V_in = [1:0.002:10];

for i = 1:length(V_in)
    Cj(i) = (Cj0/(1+V_in(i)/Vj)^M)*10^12; %*10^12 -> convert to pF
end

% calc CC contected diode capacitance (result: half of single capacitance)
for i = 1:length(Cj)
    C1(i) = Cj(i)*Cj(i) / (Cj(i)+Cj(i)); %equivalent to 0.5*Cj(i)
end

%% plotting

figure(1);
semilogx(V_in, C1); %BB201
hold on;
semilogx(Vvar_need, Cvar_need,'LineWidth',2); %capacitance needed
ylabel('Capacitance [pF]'); xlabel('Voltage [V]');
% No title for use in thesis.
%title('Variable capacitance range mixer & BB201 function plotted');
grid on
legend('C_{BB201}','Mixer range needed')
Vvar_need %just output the values on screen
```

Listing B.8: Caption test

B.5 Capacitance functions

In this section the Matlab code of all the functions is found. Most of them are short functions that implement parameters from varicaps to calculate the capacitance for a given voltage or calculate the voltage for a given capacitance. There are also a few equivalent capacitance functions which are made just for convenience.

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB135 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB135.prm
%
% single diode in package

function V = BB135_Cin(C_in)
    if (C_in > 23.18 || C_in < 1.6155)
        error('Keep values between 1.616pF and 23.179pF please')
    end

    %Rs = 0.7; not used
    Cj0 = 23.179e-12;
```

```
    Vj = 2.4894;
    M = 1.0368;

    Cj = C_in*10^(-12); %convert from picofarad to farad

    V = Vj*((Cj0/Cj)^(1/M) -1);
end
```

Listing B.9: BB135_Cin.m - calculates bias voltage for given capacitance

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB201 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB201.prm
%
%KEEP IN MIND: This function calculates only values for a SINGLE reverse
%biased diode, there are however two of such in a BB201 package in series.

function V = BB201_Cin(C_in)
    if (C_in > 133 || C_in < 21.7)
        error('Keep values between 21.7pF and 133pF please') %linear piece
    end

    %Rs = 0.23; not used
    Cj0 = 133.21e-12;
    Vj = 3.4103;
    M = 1.3251;

    Cj = C_in*10^(-12); %convert from picofarad to farad

    V = Vj*((Cj0/Cj)^(1/M) -1);
end
```

Listing B.10: BB201_Cin.m - calculates bias voltage for given capacitance

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB207 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB207.prm
%
%KEEP IN MIND: This function calculates only values for a single reverse
%biased diode, there are however two of such in a BB207 package in series.

function V = BB207_Cin(C_in)
    if (C_in > 122.5 || C_in < 23.3)
        error('Keep values between 21.7pF and 133pF please')
    end

    %Rs = 0.3; not used
    Cj0 = 122.50e-12;
    Vj = 1.4881;
    M = 0.81153;

    Cj = C_in*10^(-12); %convert from picofarad to farad

    V = Vj*((Cj0/Cj)^(1/M) -1);
end
```

Listing B.11: BB207_Cin.m - calculates bias voltage for given capacitance

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB135 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB135.prm
%
% single diode in package

function Cj = BB135_Vin(V_in)
    if (V_in > 30 || V_in < 0)
        error('Keep values between 0V and 30V please')
    end

    %Rs = 0.7; not used
    Cj0 = 23.179e-12;
    Vj = 2.4894;
    M = 1.0368;

    A = (Cj0/(1+V_in/Vj)^M);

    Cj = A*10^12; %return value in picofarad
end
```

Listing B.12: BB135_Vin.m - calculates varicap diode capacitance (single diode) for given voltage

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB201 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB201.prm
%
%KEEP IN MIND: This function calculates only values for a single reverse
%biased diode, there are however two of such in a BB201 package in series.

function Cj = BB201_Vin(V_in)
    if (V_in > 10 || V_in < 0)
        error('Keep values between 0V and 10V please')
    end

    %Rs = 0.23; not used
    Cj0 = 133.21e-12;
    Vj = 3.4103;
    M = 1.3251;

    A = (Cj0/(1+V_in/Vj)^M);

    Cj = A*10^12; %return value in picofarad
end
```

Listing B.13: BB201_Vin.m - calculates varicap diode capacitance (single diode) for given voltage

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%source values NXP BB207 parameters:
% https://www.nxp.com/downloads/en/spice-model/BB207.prm
%
%KEEP IN MIND: This function calculates only values for a single reverse
%biased diode, there are however two of such in a BB207 package in series.

function Cj = BB207_Vin(V_in)
    if (V_in > 10 || V_in < 0)
```

```
        error('Keep values between 0V and 10V please')
    end

    %Rs = 0.3; not used
    Cj0 = 122.50e-12;
    Vj = 1.4881;
    M = 0.81153;

    A = (Cj0/(1+V_in/Vj)^M);

    Cj = A*10^12; %return value in picofarad
end
```

Listing B.14: BB207_Vin.m - calculates varicap diode capacitance (single diode) for given voltage

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%
% Function that calculates, C_equivalent for:
% Dual BB135 arrangement with series capacitor

function C_eq = BB135_Ceq_tot(V_bias, C_series)
    C_BB135 =   BB135_Vin(V_bias);
    Ceq1 =      Series_C(C_BB135,C_BB135);
    C_eq =      Series_C(Ceq1, C_series);
end
```

Listing B.15: BB135_Ceq_tot.m - calculates equivalent capacitance of two BB135 varactors and a thirth capacitance in series

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%
% C equivalent calculator for:
% Dual BB201 arrangement with series capacitor (=single BB201 device)

function C_eq = BB201_Ceq_tot(V_bias, C_series)
    C_BB201 =   BB201_Vin(V_bias);
    Ceq1 =      Series_C(C_BB201,C_BB201);
    C_eq =      Series_C(Ceq1, C_series);
end
```

Listing B.16: BB201_Ceq_tot.m - calculates equivalent capacitance of two BB135 varactors and a thirth capacitance in series

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%
% C equivalent calculator for:
% Dual varicap arrangement with series capacitor
% - ADS modulator design v7

function C_eq = Ceq_tot(V_bias, C1)
    %Hardcoded values from the design:
    C_BJT = 0.72;
    %C1 =    6; %changed to variable for checking stuff
    C2 =    200;
    C_decouble_BB201 =  20e3; %20nF
    C_series_BB135 =     1.7; %1.7pF
```

```
    C_eq =  Series_C((C1 + C_BJT), C2) + ...
            BB201_Ceq_tot(V_bias, C_decouble_BB201) + ...
            BB135_Ceq_tot(V_bias, C_series_BB135);
end
```

Listing B.17: Ceq_tot.m - is used to calculate the total equivalent capacitance of the Modulator tank circuit

```
%Made by Jasper van Vliet
%Date: 30-05-2019
%simple series capacitance function

function Ceq = Series_C(C1,C2)
    Ceq = C1*C2/(C1+C2);
end
```

Listing B.18: Series_C.m - calculates the equivalent capacitance of two capacitors in series

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