# Liquid crystal wavefront corrector on silicon

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## ABSTRACT

A reflective-type liquid crystal (LC) wavefront corrector with modal addressing is described. The corrector's backplane has an array of pixel electrodes interconnected by a network of discrete resistors. The resistive network serves to form the local voltage profile that controls the phase distribution generated in the liquid crystal layer. This design is realized in a bipolar silicon technology. Preliminary numerical analysis is presented; technology and experimental results are discussed.

**Keywords:** wavefront correctors, phase modulators, liquid crystal optics

## 1. INTRODUCTION

Liquid crystal (LC) phase modulators are used as an alternative to traditionally used deformable mirrors for wavefront correction in adaptive optics[1,2]. The advantages of the LC technology are low control voltages, low power consumption, large dynamic range, absence of moving parts and low cost of materials. In addition, it profits from the basis of a powerful LC industry, the products of which are widely used in everyday life. Another major technology that can be applied for manufacturing LC modulators, is silicon integrated circuit (IC) manufacturing technology. Reflective Liquid Crystals on Silicon (LCoS) phase modulators with 1920x1200 pixels already exist[3], where each pixel is addressed individually with in total 2.2M pixels per frame being addressed. At the same time, for instance, for ophthalmic applications[4] it is enough to provide compensation of a limited number of low-order wavefront aberrations, such as defocus, astigmatism, coma, spherical aberration etc.

Modal-type correctors, such as deformable mirrors with continuous faceplate, provide spatially continuous phase modulation and reasonable approximation to low-order aberrations using a relatively small number of actuators (several tens). A similar approach can be realized using liquid crystal optics. Implementation of a liquid crystal modal wavefront corrector (LC-MWC) was described in [5,6]. The operation of this device is based on the change of the birefringence of a thin LC layer under the application of an electric field. Continuous voltage distribution formed across the corrector's aperture generates continuous phase response in the LC layer. A resistive layer with very high sheet resistance (~1 MΩ/square) serves as a distributed voltage divider, which ensures a smooth voltage variation across the aperture. This approach was realized using glass-based technology, and two series of 37-channel devices with 30-mm and 70-mm aperture were produced. The technology can be extended to produce devices with apertures up to 10 cm and hundreds of actuators. Nevertheless, in its present state it is quite demanding and hardly suitable for serial production.

Another option is offered by silicon technology, which allows the formation of the required configuration of actuators on the surface of a chip using standard IC manufacturing processes. Another attractive feature of this approach is that on-chip implementation of the multiplexed control enables the further scaling of this technology to a very large number of actuators. However, direct implementation of the LC-MWC with continuous resistive layer cannot be accomplished in the framework of standard bipolar and CMOS processes, mainly because these processes do not involve technologies suitable for making layers with sheet resistances as high as is required for the CE. Thus, additional technological steps should be incorporated, which, in turn, would increase the processing costs. In this paper we present an indirect implementation of this approach, which we call a *hybrid* approach.

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## 2. BASIC PRINCIPLES AND PRELIMINARY ANALYSIS

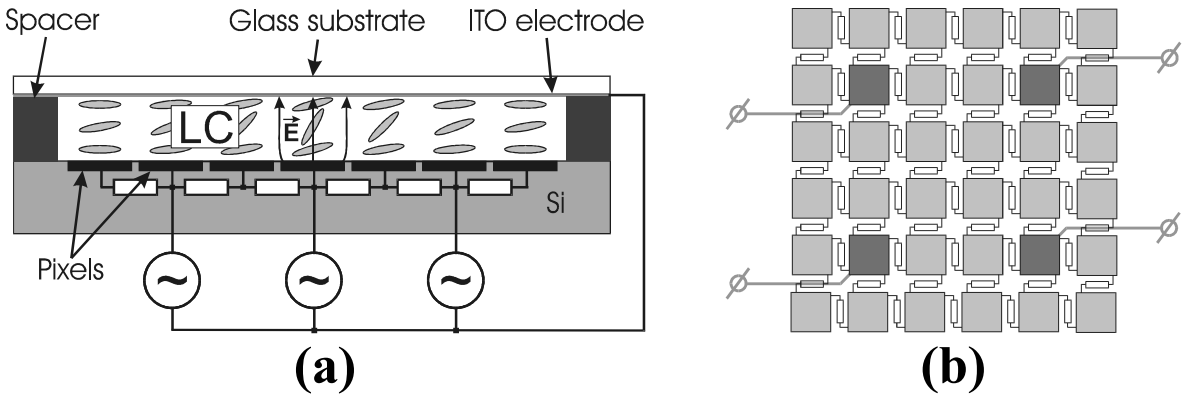


Fig. 1. Cross-section (a) and structure of pixels (b) of the hybrid LC wavefront corrector.

A schematic of the device is shown in Fig. 1a. A thin LC layer is sandwiched between two substrates, a glass substrate and a silicon substrate; the latter has a reflective array of pixels on top of it. Spacers placed between the substrates at the periphery provide a homogeneous thickness of the LC layer. Special alignment coatings generate initial planar alignment of the LC molecules. A transparent conductive indium-tin oxide (ITO) coating covers the glass substrate.

The device is driven by AC voltages applied between the pixels and the ITO electrode. The local phase response of the LC layer, $\Delta\Phi$, depends on the *rms* value of the voltage applied to electrodes, $U_{rms}$, following the electro-optical response characteristic of the LC $\Delta\Phi = \Delta\Phi(U_{rms})$.

The hybrid approach is realized by interconnection of adjacent pixels by discrete IC resistors to form a network as shown in Fig. 1b. It combines features of both the *zonal* and the *modal* approaches. Whereas the reflective backplane of the corrector has a pixel-type structure, which is typical for the *zonal* approach, *modal*-type control of the pixel array is implemented, which means that addressing of one control channel causes the whole array to respond. Only some of the pixels are addressed directly from the control unit (we call them *active* pixels), whereas the resistive network provides gradual voltage variation between the other pixels (*passive* ones). Thus, relatively few control channels allow the driving of a large array of pixels, which is suitable for correction of low-order aberrations. Implementation of the device by using a standard process makes it possible to integrate more electronic circuitry in the future and incorporate more complicated addressing schemes, making the technology scalable in this respect.

The distribution of voltage in this modulator can be found from the solution of the system of equations, which result from the Kirchhoff's rules defined for all nodes of the network. Capacitive and conductive properties of the LC layer should be also taken into account. Electro-optical characteristics, specific capacitance and conductance of the LC can be obtained by direct measurement of a simple LC cell[7]. We have conducted numerical simulations based on these principles.

To estimate how many intermediate passive pixels should be placed between two adjacent active pixels to obtain reasonable correction quality, we calculated electrical and optical responses of a modulator with 36 (6x6) active pixels and a variable number of passive pixels. In this simulation we calculated influence functions of the modulator and used them for approximation of various wavefront aberrations. We assumed a linear dependency of the phase response of the LC from the *rms* voltage; for real nematic LCs it corresponds to approximately half of the total phase delay variation range.

To evaluate the average optical performance of the wavefront corrector, we need to apply it to the whole class of optical fields. Earlier[8] we developed a method, which allows evaluating statistically average efficiency of the wavefront corrector. This method used the Kolmogorov statistical model of random wavefront aberrations produced by atmospheric turbulence. Modal wavefront correction is usually described in terms of complete orthogonal sets of

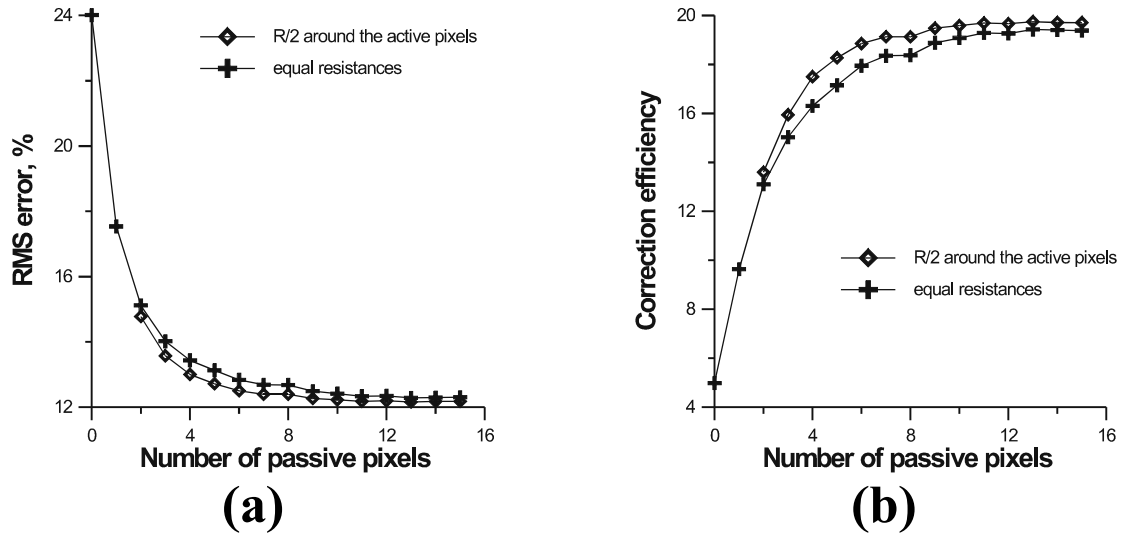


Fig. 2. *Rms* correction error (a) and correction efficiency (b) of 36-channel LC-MWC based on discrete IC resistors vs number of passive pixels placed between two adjacent active pixels.

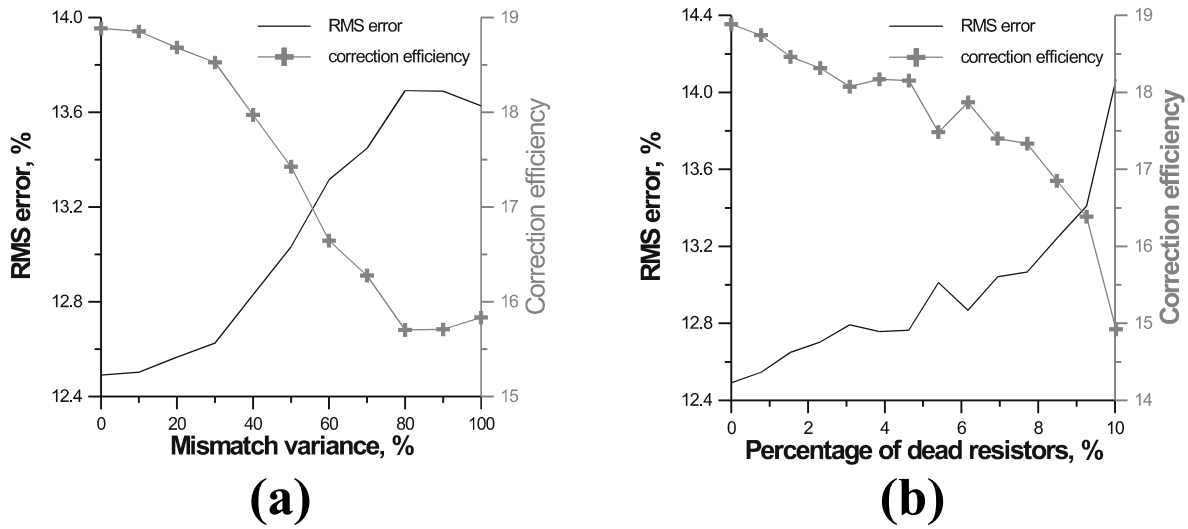


Fig. 3. *Rms* correction error and correction efficiency of 36-channel LC-MWC vs resistors' mismatch variance (a) and percentage of "dead" (open-circuit) resistors (b).

functions, such as Zernike polynomials or Karhunen-Loève functions. The latter is a special set of functions, best fit for representation of random wavefronts with statistics described by Kolmogorov's theory. In our method, the correction efficiency was evaluated as equivalent number of Karhunen-Loève modes resulting in the same fitting error. We also evaluated the *rms* error of correction in percents to the *rms* initial aberration.

Using this method we evaluated the correction efficiency of a 36-channel modulator for different numbers of passive pixels placed between two adjacent active pixels; the results are presented in Fig. 2. Zero passive pixels corresponds to the well-known case of a piston corrector. The results show that the efficiency of a 36-channel piston corrector is equal to 5 Karhunen-Loève modes, whereas use of passive pixels enables an increase of this to 19.7 modes, reducing the *rms* correction error by approximately a factor of 2. To demonstrate the possibility for improvement of the correction efficiency by adjustment of individual resistances, we have performed simulations for two different configurations of resistors. In the first case we assumed all resistances to be equal; in the second case the resistors connected to the active

pixels had a resistance that was two times lower than that of the other resistors. The improvement in the second case is clearly seen in Fig. 2. To find an optimum configuration of the resistances, a special investigation could be undertaken in the future.

It is seen from the graph that the correction efficiency saturates at 19.7 Karhunen-Loève modes for approximately 12 intermediate passive pixels. At the same time, for two times lower resolution (6 intermediate passive pixels) the efficiency is not significantly lower and is equal to 18.9 modes. The total amount of pixels in this case is 1296 (36x36); we used this configuration of pixels in our further simulations.

In practical IC manufacturing processes tolerances of minimum size resistors reach ±30%, whereas different resistors in the same chip can be matched to better than 0.1% by using special matching techniques[9]. In order to determine the optimum type and layout of the resistors it is important to know precisely how they should be matched. With this purpose we calculated how the correction efficiency depends on the resistance error. For our calculation we used a randomly generated array of resistances with Gaussian distribution having 100 kΩ average and a given standard deviation. The results presented in Fig. 3a show that even very large resistance variations do not seriously affect of the correction efficiency, and at 10% mismatch this effect can be neglected. We also simulated the situation when a certain amount of resistors does not function, i.e., has infinite resistance. The results in Fig. 3b show that 1-2% of open-circuit resistors can be tolerated. It means that the behavior of the resistive network as a whole can compensate defects in the individual elements.

## 3. IMPLEMENTATION

Silicon processes offer many options for the construction of resistors, where polysilicon resistors represent the most preferred choice for CMOS processes and diffusion resistors for bipolar ones[9]. Diffusion resistors are preferred for this particular application as they have two important advantages. First of all, they are formed by doping of certain areas of the silicon substrate and do not significantly affect the flatness of the substrate. This facilitates the placement of the resistors under the pixel layer, thus keeping the fill factor of the LC modulator high, which is much more difficult to achieve for polysilicon resistors. Secondly, poly resistors are more susceptible to overheating because they are usually surrounded by the oxide, which does not conduct heat well. On the contrary, monocrystalline silicon substrate in which the diffusion resistor is made is a good heat conductor. We estimated the heating of a 8 μm-thick 10 kΩ diffusion resistor during normal operation of the LC modulator (maximum 10 V change of voltage between two adjacent active pixels) to be less than 0.2 K.

Two process options for implementation of the hybrid corrector with diffusion-type resistors can be considered. The simplest variant is a custom process with only one diffusion; for instance, *p*-type diffusion in an *n*-type silicon wafer – see Fig. 4a. To provide isolation between the resistors, the substrate should be biased at the voltage $V_{max}$, which should be higher than any voltage applied to the resistors; in this case the *p*-*n* junction will be reverse-biased. Deposition of the substrate contact on the back of the wafer is required to provide biasing. Implementation with a *p*-type wafer and *n*-type diffusion is also possible.

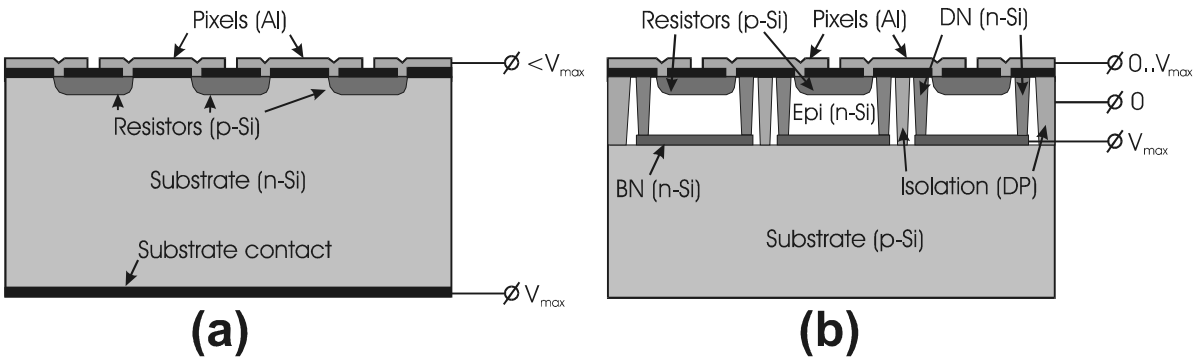


Fig. 4. Implementation of diffusion resistors in a custom (a) and a bipolar (b) processes.

Another option is to use a bipolar process with *p*-type substrate and *n*-type epitaxial ("epi") layer, which is grown on the wafer surface (Fig. 4b). The *p*-type diffusion of the resistors is made in the epitaxial layer. A highly-doped, low-resistive "buried" *n*-type diffusion (BN), which is formed before the epitaxial growth, and a highly-doped *n*-plug diffusion (DN) are used to entirely surround the *p*-type resistors and provide a low-resistive contact to the epi as well as preventing so-called latch-up effects due to the parasitic *pnp* to the substrate. The *n*-type islands, each containing a resistor, are separated by a deep *p*-type diffusion (DP) to the substrate that is a standard isolation method in bipolar processes. The main advantage of the custom process is that much less masks are involved than in the case of the standard bipolar process. However, the bipolar process has several important advantages. First of all, the *n*-substrate with backside contacting gives a higher resistive path to the small features of the resistor diffusion than the more direct contacting via deep *n*-diffusion and buried layer to the epi-island. For instance, if we have a current leakage from a 10 μm-wide stripe area of the diffusion, the resistance in the first case is about two orders higher than in the second case, and it may result in debiasing of the substrate. Due to the small thickness of the epi layer, biasing in the bipolar process is much more reliable.

The second problem that may occur for the single-diffusion custom process is the above mentioned "latch-up". This thyristor-type behavior of parasitic bipolar transistors may occur between different diffusions and the substrate[9].

The third advantage of the standard bipolar technology is that in the future additional electronic components can be placed on the chip for implementation of the multiplexed control, which makes possible further scaling of this technology to hundreds thousands of actuators.

For these reasons it was decided to use the bipolar process. We chose the DIMES03 process, which is available in DIMES Technology

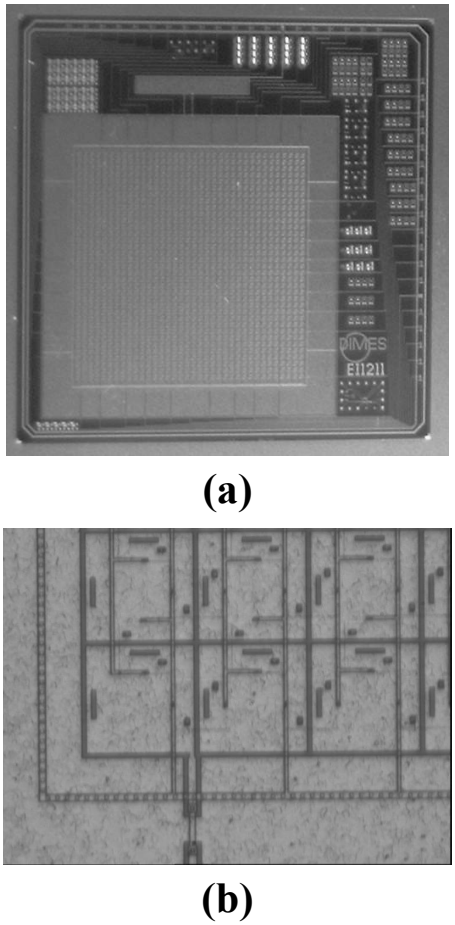


Fig. 5. Backplane of the hybrid LC corrector (a); structure of pixels (b).

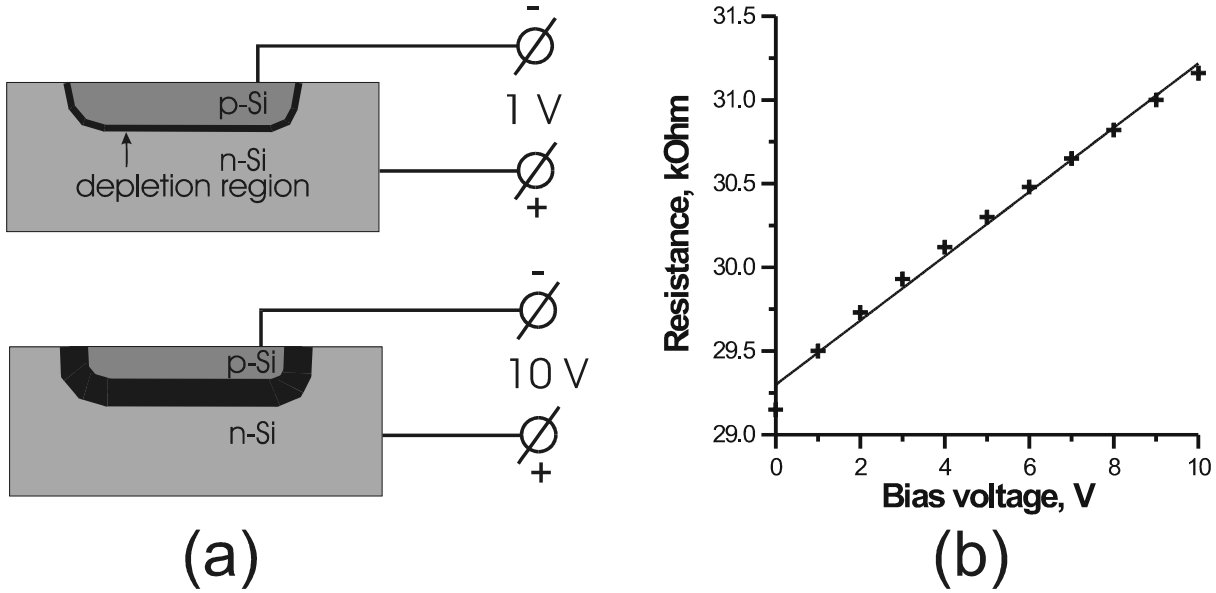


Fig. 6. Modulation of the resistance with bias voltage: explanation (a); measured modulation for a test resistor (b).

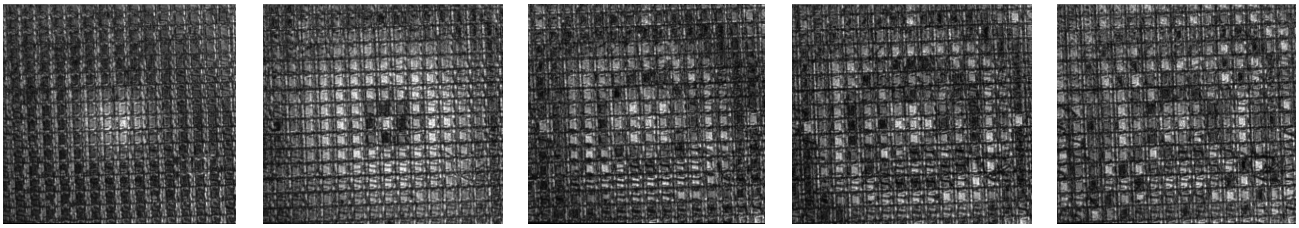


Fig. 7. Visualization of the influence function of an active pixel; frequency of the square waves 1 kHz, amplitude $V_1$ = 4.5 V for the active pixel in the center and $V_2$ for other active pixels. Values of $V_2$ are 4 V (a), 3.5 V (b), 3 V (c), 2.75 V (d) and 2.25 V (e).

Center, TU Delft. Diffusion-type resistors with a resistance of 29.4 kΩ were formed by selective doping of 4 μm-wide stripe areas on the surface of the silicon substrates. All resistors in the network were matched by the geometry and total length of horizontally and vertically oriented pieces in each resistor. In order to check the electrical parameters of the process, test structures were also placed on the chip.

The first prototype (see Fig. 5) had 1296 (36x36) pixels with 36 inputs; the pixel size was 220x220 μm; thus, the total area occupied by the pixels was 8.2x8.2 mm$^2$. The pixels were formed by patterning of an aluminum metallization layer, namely, the second metallization. Bondpads, 100x100 μm size, were placed at the periphery. Two of the bondpads provided high and low reference voltages to the substrate and to the epi islands, respectively. Other bondpads provided connection of signals to the active pixels; they were equipped with a pair of diodes, which served to keep the signal in the range between high and low reference voltages. It is required to avoid positive biasing of *p-n* junctions between the epi islands and the resistor diffusions.

The size of the whole die, including bondpads, was 15x15 mm$^2$. For this size it was still possible to use wafer stepper lithography with a resolution of about 0.15 μm. A full wafer process would allow manufacturing of a larger die but with a lower precision (about 1 μm) and supposedly lower yield due to use of contact lithography.

To facilitate assembling of the LC cells, the substrates were made slightly larger than the die, 18x18 mm$^2$ in size. The calculated fill factor value was 82.8%; it is estimated as a percentage of the flat pixel area with respect to the total area, which also includes gaps between pixels, contacts to the resistors and grooves imprinted from the lower metallization layer. The whole structure of pixels was covered with silicon nitride, which is used in DIMES03 for scratch protection.

A homogeneous 25 μm spacing between the silicon substrate and the cover glass was provided by teflon spacers. Planar alignment of the LC was generated by exposure of linearly photopolymerizable polymer (LPP) to the polarized UV light. Commercially available LPP Staralign$^{TM}$ 2100 from Rolic, Switzerland, and BL006 liquid crystal mixture from Merck, Germany, were used. Birefringence of BL006 is 0.286 (λ = 589 nm), which results in a maximum range of phase variation for this modulator of about 22 λ. The assembled LC cell was mounted on a custom PCB mount and electrically connected by wire bonding.

## 4. EXPERIMENTAL RESULTS

Electrical measurements of the test structures have shown good matching of the resistors since the resistance mismatch was less than 2 %. In addition, the resistance of the network was measured between two arbitrarily chosen active pixels; the experimental value was, with a discrepancy of only 1.5 %, in good agreement with that calculated with the numerical model. This result confirms the validity of the model.

It is supposed that during normal operation of the modulator the *n*-island is biased at the highest available potential. At the same time, as the modulator is driven by AC voltages,

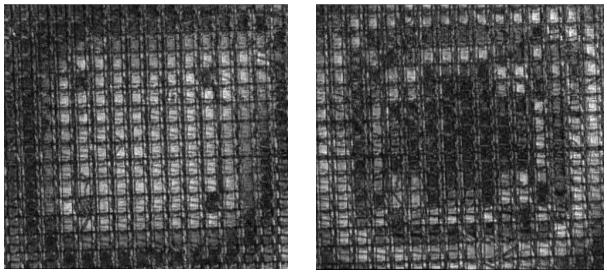


Fig. 8. Combined influence of four active pixels; frequency of the square waves 1 kHz, amplitude $V_1$ for 4 adjacent active pixels in the center and $V_2$ = 4.5 V for other ones. Values of $V_1$: 3.5 V (a) and 2.5 V (b).

the electric potential of the resistor can be varied in a wide range during one period. Due to widening of the depletion zone with increase of the epi bias (Fig. 6a), the effective thickness of the diffusion is reduced, which results in an increase of the sheet resistance. Thus, we should observe modulation of the resistance with bias, which may result in shift of the DC component of voltage with the amplitude of AC voltage. We measured this modulation on our test structures; one of the measurement results is presented in Fig. 6b. The average modulation was about 0.7 %/V. We estimated the maximum DC shift due to resistance modulation during normal operation of the device to be 0.08 V, which can be tolerated.

To drive the modulator, we used two 24-channel DAC boards from OKO Technologies (Delft, the Netherlands)[10]. Reliable multichannel generation of rectangular pulses was provided by custom control software developed using Ardence RTX[11], a real-time subsystem for Windows NT/2000/XP. The system generated 36 meander AC voltages with amplitudes up to 5 V and frequencies up to 5 kHz. Phase profiles generated by the modulator were studied using polarizational interferometer.

Responses of an arbitrarily chosen active pixel are shown in Fig. 7. Square wave signal with 4.5 V amplitude and 1 kHz frequency was applied to that pixel, whereas the amplitude of the bias AC voltage applied to other active pixels was varied in the range 4 to 2.25 V. The rotationally symmetric character of the interferometric patterns in Figs. 7a-7c shows that, despite the discretization, the distribution of the optical phase across the array of pixels has a modal character. Moiré patterns, as seen in Figs. 7d-7e, appear in the interferogram due to aliasing, when the phase variation between two adjacent pixels exceeds $2\pi$. An example of the combined influence of four active pixels is shown in Fig. 8.

Detailed investigation of the interferometric patterns shows significant roughness of the reflective surface of the aluminium pixels and rather poor quality of the LC alignment with many dislocations. Both these factors cause scattering of light, which results in a weak contrast of the interferometric patterns on a large scale. The most likely reason of the poor quality of the LC alignment is the poor optical quality of the standard protective silicon nitride coating. This is a PECVD layer with non-ideal surface roughness and optical transparency. In the present design no special measures were undertaken to bring the surface quality up to the optical standards.

In the next design we are intending to take appropriate measures to improve the optical quality of the reflective backplanes. First of all, the protective layer will be made of oxide and will be planarized by ion beam etching; then, a multilayer dielectric coating will be deposited on the planarized surface. Structure and dimensions of the pixels, the wires and the resistors will be optimized in order to increase the fill factor. In addition, we are also going to implement the structure of the resistive network which would provide the smoothest fitting of an arbitrary combination of low-order aberrations.

## 5. CONCLUSION

We report on progress in development of a modal LC wavefront corrector based on silicon technology. Our approach combines features of both the zonal and the modal approaches. The configuration of pixels is formed on the surface of a silicon chip by patterning of metallization layers. The pixels are interconnected by discrete IC resistors forming a network. Some of the pixels are addressed directly, whereas the resistive network provides distribution of voltage throughout the whole array of pixels. Implementation in the framework of a standard bipolar or CMOS process allows further scaling of this technology by integration of elements of control electronics into the backplane.

Feasibility of the proposed approach was demonstrated by numerical simulations. We performed analysis of the correction efficiency and investigated the influence of the resistors' mismatch. It was shown that rather poor matching and even non-functioning of some resistors can be tolerated. We also showed that the correction efficiency can be optimized by proper choice of the number of pixels and adjustment of individual resistances.

The bipolar process was chosen for implementation of the device. The first prototype, which had 36 active pixels and a total amount pixels of 1296 (36x36), was manufactured in DIMES Technology Center, TU Delft. Forming of the modal-type influence functions and their superposition were demonstrated by interferometric measurements. Improvement of the optical quality of the reflective backplanes will be targeted in the next design.

## 6. ACKNOWLEDGEMENTS

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