Microelectronic design of a pseudo voltage clamp for a 0.18um CMOS-based mesoscale neural interface for intracellular in-vitro recording and stimulation

Aitor del Rivero Cortázar

TU Delft

Microelectronic design of a pseudo voltage clamp for a 0.18um CMOS-based mesoscale neural interface for intracellular in-vitro recording and stimulation

by

Aitor del Rivero Cortázar

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday August 30, 2021 at 1:30 PM.

Student number:	4999339	
Project duration:	September 1, 2020 – June 30, 2021	
Thesis committee:	Prof. dr. ir. W.A. Serdijn,	TU Delft
	Prof. dr. ir. C.J.M. Verhoeven,	TU Delft
	Dr. T.M. Lopes Marta da Costa,	TU Delft, supervisor
	Ir. A.J.M. Montagne,	TU Delft, supervisor

TU Delft

Preface

This thesis is part of the Master's Degree in Electrical Engineering, Microelectronics, at Section Bioelectronics, Delft University of Technology, the Netherlands. Under an EU-Swiss mobility agreement, the research has been carried at the Bio-Engineering Lab, ETH Zürich, Basel, Switzerland.

Abstract
The need to understand how the brain works has sparked interest in electrode arrays to record neural signals. Intracellular recordings with nanoelectrodes that penetrate the cell allow better signal quality and additional functions such as voltage clamping to set the neuron's transmembrane voltage. The voltage clamp aims to facilitate the independent study of the ionic channel contributions to the overall neuron's transmembrane current for applications such as drug screening. This thesis aims to design a voltage clamp with CMOS technology to integrate into an intracellular neural interface system. The circuit, a trans-impedance amplifier, needs to be low-noise, small, and have wide clamping and output voltage ranges. The amplifier's design follows a structured methodology and uses symbolic analysis with the software SLiCAP and simplified EKV models aiming for easier readjustments and transparency for other researchers. The controller is an Operational Amplifier with a differential pair input-stage, an unbalanced common-source output-stage, and frequency compensation. The feedback network is a pseudo-resistor due to the enormous gains required to record the currents in the electrode of about $100\ pA \sim 1\ nA$. The final simulations estimate a trans-impedance gain from the electrode to the load range of $[2\ M, 1\ G]\ V/A$, a clamping voltage range of $[0.9, 3.16]\ V$, an output voltage range of $[0.5, 3.16]\ V$, and an output-referred noise between 0.095 and $0.41\ mV_{rms}$ depending on the gain. The power usage is $49.1\ \mu W/pixel$ and the area $0.0092\ mm^2/pixel$. Post-layout simulations show stability degradation due to the influence of parasitics in the pseudo-resistor.

Acknowledgments
The project would not have been possible without the dedication and support of the daily advisors Dr. Hasan Ulusan and Dr. Fernando Cardes, who accompanied me during the whole project. I would also like to thank my supervisor, Dr. Tiago Costa, for his feedback and the flexibility and trust he gave me to organize the work plan timeline and coordinate the two universities' academic goals.

It is indispensable to dedicate some lines to my supervisor Anton Montagne, who has been an essential mentor in this project and during all the Master's Degree. During my previous experiences in Higher Education, I have heard many times that we should "think out of the box," but felt that we were not given tools to open the box but just nice-looking paintings to cover its walls. I think Structured Electronic Design is one of those tools that I was looking for when I arrived at Delft. Montagne's method has allowed me to connect the pieces from different courses. It has also given me solid foundations about system design that will allow me to build solid knowledge on top in the future as an independent researcher. The combination of his passion, dedication, and experience is a priceless example for students and an excellent asset for TU Delft.

I would also like to thank Prof. Wouter Serdijn and Prof. Andreas Hierlemann for allowing me to be part of their fantastic research groups this academic year.

Lastly, I would like to mention that my studies at TU Delft have been possible thanks to the support by a grant from the" la Caixa" Banking Foundation (ID 100010434), whose code is LCF/BQ/EU19/11710061. I thank the Foundation for the opportunity to grow personally and professionally while studying abroad and wish that many other students have the opportunity to apply for this fellowship program for many more years.

Aitor del Rivero Cortázar
Basel, 15 August 2021

Contents

1 Introduction

Neural interfaces are electronic devices that interact with the nervous system of living beings, either recording or stimulating it.

The concept of neural recording arose in 1872 after Richard Caton observed electrical impulses on the brain surface of animals [50]. These findings were possible thanks to Luigi Galvani's previous research in bioelectricity in the 1780s. In 1912, Vladimir Pravdich-Neminsky performed the first electroencephalography (EEG) in animals [50]. This technique was later applied to humans by Hans Berger in 1924 [50]. Since then, neural recordings have helped neuroscientists make massive progress in modeling the nervous system and understanding diseases such as epilepsy, sight and hearing impairment, Parkinson's, dystonia, locked-in syndrome, or paraplegia. [50]. The upgrade of neural interfaces foretells breakthroughs in neuroscience and further discoveries about those diseases [58].

As part of the international efforts to progress in this high-impact field, several labs are working towards improving the performance of a specific family of neural interfaces: nanoelectrode-array based interfaces. This thesis joins those efforts. Namely, the context of this project is within mesoscale neural interfaces built using CMOS technology and nanoelectrodes as sensors to record intracellular signals from cells in vitro.

1.1. Types of neural interfaces and measurements

In this subsection, each sub-classification of the neural interface family is explained.

Scale of neural interfaces

On one side, microscale neural recording systems such as the patch-clamp record information on the level of the ionic channel, allowing neuroscientists to study the activation mechanism [25] [35]. While that insight is helpful for cell-level physiology research, it is limited from a functional and structural study perspective. On the other side, macroscale neural recording systems such as MRI, fMRI, PET, or EEG, cover the gap but lose the ability to target individual neurons in return [29]. An intermediate approach that has become very relevant in neuroscience research is to use mesoscale recording systems to target smaller regions while still providing information for functional analysis. Also, they integrate efficiently with stimulation systems.

The objectives of mesoscale systems are: 1) achieving a high spatiotemporal resolution to localize activity successfully at both cell and network levels, 2) obtaining a high signal-to-noise ratio (SNR) to increase the reliability of the information sorting, and 3) avoid damaging tissues or neuronal processes [43] [24]. Since these objectives contradict each other, trade-offs are needed, and over-design must be avoided. For example, a high spatiotemporal resolution requires many small electrodes and circuitry, which increases the noise. Similarly, a better SNR requires more area, which is limited by the resolution and the production cost. Additionally, the power consumption can increase, but that would cause a rise in the temperature in the recording sites that would lead to modifications in the neuronal processes, or even tissue damage [43].

Placement of the electrode
The properties of the recording depend heavily on the placement of the neural interface. Extracellular recordings take place out of the targeted neurons, while intracellular recordings extract the information directly from the inside of the targets.

Extracellular recording (Fig. 1.1 b) is a non-invasive method from the cell perspective since no puncturing is needed, enabling long-term measurements [24]. Furthermore, it provides an excellent spatial-temporal resolution because it can record thousands of sites at the same. The problem is that it cannot retrieve information from subthreshold events that are critical for understanding the synaptic connections among neurons [2]. This issue arises because the voltage variations in the extracellular medium are smaller than in the intracellular, so the signal-to-noise ratio (SNR) is small compared to the intracellular SNR.

Intracellular recording with traditional methods such as the patch-clamp technique (Fig. 1.1 a) has the opposite properties. It has a high SNR but lacks spatial resolution because the sensor is a glass pipette that requires a bulky mechanical setup [35] [1]. Besides, the ionic solution in the micropipette produces invasive chemical exchanges with the cell, which limits their life span [1].

The use of CMOS technology
A way of implementing a mesoscale neural recording system is by using microsensors and a CMOS (Complementary Metal-Oxide-Semiconductor) interface. The microsensors are integrated into large arrays that are in contact with a group of neurons [43]. The CMOS interface transports and processes the recordings in a millisecond time interval. These devices are known as Microelectrode Arrays (MEAs).

There are several reasons for using CMOS technology in the interface [43]: 1) integrating all elements in the same substrate allows a higher number of electrodes and higher density; 2) it is possible to use active switches to time multiplex signals and improve data transmission; 3) the parasitic capacitances and resistances are minimized since conditioning circuitry gets closer to the electrodes; 4) it allows for the inclusion of additional on-chip functionalities such as chip identification, spike detection, stimulation, or pH and temperature sensing; and 5) it allows to take advantage of the advanced lithography techniques.

However, using CMOS has also some limitations: 1) although it is true that lithography is very advanced and continues improving, the pace of the advances is not reflected directly on neuroelectronics [42]; 2) CMOS silicon substrate is not transparent in contrast to standard cell culture substrates used in biology; 3) some components may corrode upon long-term use [24].

In [2] a new approach called CMOS-neuroelectronic interface (CNEI) was presented. This technique uses CMOS circuitry and nanoelectrodes, which are much smaller than those of the MEAs. CNEI's are supposed to combine a high SNR due to its intracellular nature (Fig. 1.1 c), with a high spatiotemporal resolution close to extracellular recordings with MEAs. Another advantage is that the damage caused to the neuron is minimized in comparison to previous methods. In addition, stimulation and recording can be simultaneous. In other words, the new technology combines the advantages of both intra- and extracellular technologies.

Type of targeted cells
Recordings can be tagged as in vivo or in vitro if neurons under study are still on a living being or not, respectively. In vitro techniques can be sub-classified into acute tissue preparations or cell cultures. Preparations use cells that have been removed from the living being just before the measurement, while cultures use tissues that have been removed time ago or grew out of the living being. There are two types of cell cultures based on the degree of conservation of the cell structure: organotypic cultures, which maintain the structure, and dissociated cultures, which have a modified structure [24].

1.2. Modules of a CMOS-based neural interface

A CNEI contains different modules that are application-specific (Fig. 1.2). In all CNEIs, there is a nanoelectrode array and a recording module. Some also contain a stimulation module and additional subsystems depending on the final purpose of the CNEI.

This thesis targets a specific subsystem of the CNEI: the voltage clamp. Although it also has some recording properties, the voltage clamp can be considered part of the stimulation module. In the following paragraphs, there are more details about the nanoelectrode arrays and the two modules to picture a whole image of the thesis framework.

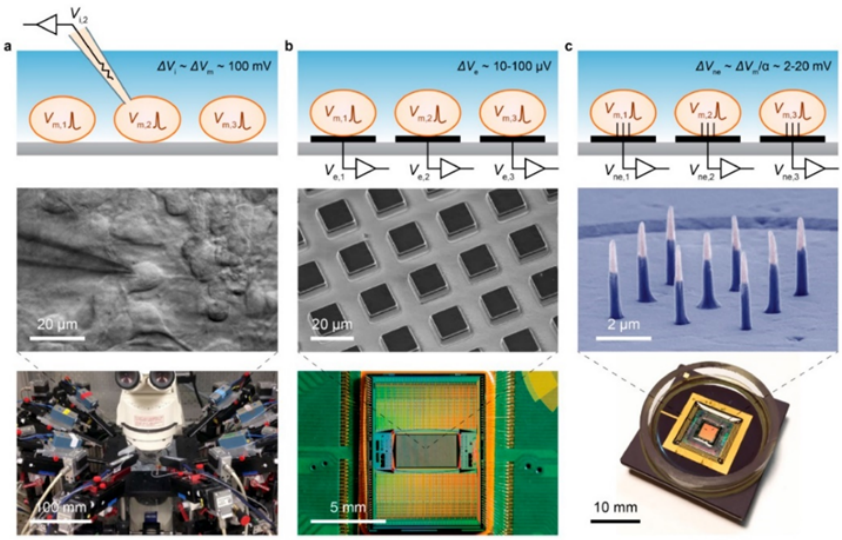


Figure 1.1: Diagram (top row), microscope image (middle row), and setup (bottom row) of an (a) intracellular recording using the patch-clamp technique, (b) extracellular recording with planar microelectrodes forming an array (MEAs), (c) intracellular recording with nanopillars forming an array (CNEI). The advantage of (a) is the quality of the signal, but the neuron is severely damaged, and the setup is very bulky. The advantage of (b) is the spatial resolution and the neuron health, but the signal amplitude is reduced. (c) Provides a large signal amplitude while keeping the neuron healthy for a longer time and has a good spatial resolution. Source: [1].

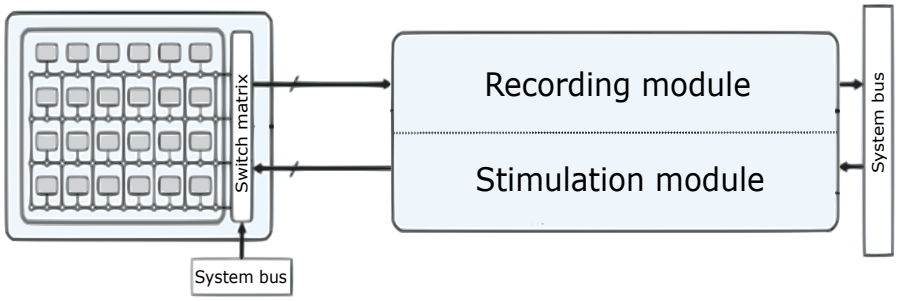


Figure 1.2: Simplified functional diagram of a CNEI. The CNEI always includes an electrode array and a recording module. These two modules capture and condition the neural signals so that their waveforms can be processed later. The CNEI usually contains a stimulation module that allows neuroscientists to set specific control variables or trigger activity in the neurons, e.g., a voltage clamp. Additionally, some other modules can be included in a CNEI, depending on the specific aims of the experiments, e.g., current generators or a temperature sensor.

The nanoelectrode array

The nanoelectrode array is a network of sensors on which the neurons are placed. The primary function of these sensors is to capture the intracellular signals of the neurons without corrupting their information. Therefore, the network needs to be reliable even if some links break.

Different nanoelectrode array topologies can be used depending on the application, which determines the desired level of performance, complexity, and reliability (Fig. 1.3). Fixed wiring topologies, using either passive or active circuitry, are those which do not multiplex signals. These topologies are simple, but they lack spatial resolution and suffer performance losses in return. On the other hand, multiplexed topologies are complex but boost spatial resolution and performance because interconnecting vias are reduced, leading to fewer parasitic elements and area usage.

Multiplexed topologies can be subcategorized into static [17] [18], [4] or dynamic [7] [6]. Dynamic multiplexing has a higher sampling rate. The electrode impedance is too high to operate at such high frequencies, and there is noise aliasing. Therefore, it is necessary to build an active-pixel sensor, which combines an electrode, an amplifier, and a low pass filter (LPF). This requirement makes the design more complex and affects the performance in terms of area, and noise [57]. In exchange, dynamic multiplexing increases the temporal resolution and allows to zoom in into Regions of Interest (ROIs) [24].

The scientific progress on electrode technology is slower than on CMOS technology, so it is desirable to transfer as much complexity as possible from the electrode to the CMOS interface [42]. The project in which this thesis is framed uses a nanoelectrode array topology with static multiplexing.

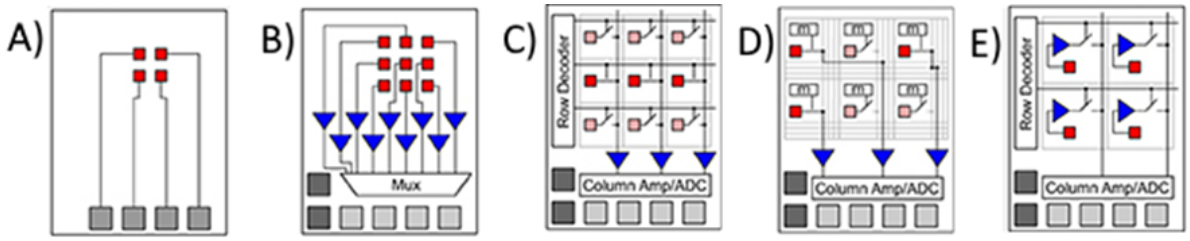


Figure 1.3: Different topologies that can be used for the nanoelectrode array: (a) fixed wiring array topology with passive circuitry, (b) fixed wiring array topology with active circuitry, (c) statically multiplexed array topology with row-column addressing, (d) statically multiplexed array topology with switch-matrix (flexible) addressing, (e) dynamically multiplexed array topology with row-column addressing. The level of complexity increases from (a) to (e). In current projects, the multiplexed topologies are predominant.

The recording module

The recording module combines signal conditioning, multiplexing, and data conversion elements that gather the information from the nanoelectrode array and delivers it to the processing units in a format that the latest can understand.

The conditioning circuitry is indispensable because the neural signal amplitude is tiny, and the electrode-tissue impedance is enormous, leading to power loss [28]. Hence, this circuitry includes amplifying stages to increase input impedance and voltage gain significantly. Another issue regarding neural signals is that they are very noisy. Consequently, the conditioning circuitry also includes several filters that remove power-line interferences, reduce the impact of thermal and flicker noise, and couple amplifiers [28]. Depending on the measurement conditions and the type of cells targeted, the required voltage gain, impedance, or filtering characteristic can vary dramatically. Therefore, it is common to include variable resistances, capacitances, or different operating points to adapt the neural interface to different scenarios.

The information gathered needs to be sent to an external device using a limited number of channels. Since the information is coming from many different sensors simultaneously, multiplexing is needed to share the channels. In most cases, the external device operates in the digital domain. An analog-to-digital converter (ADC) is used to convert the information.

The stimulation module

The stimulation module is a combination of circuits specifically designed to trigger activity in the neurons or set control variables. An example of these circuits is the voltage clamp, which fixes the transmembrane voltage of neurons while measuring the transmembrane current. This technique aims to determine the conductivity of each kind of ionic channel through the membrane of the neurons. This calculation is possible because the current of the neuron is formed from three main contributors, of which the voltage clamp cancels one and another can be canceled using drugs. Section 2.1 includes a detailed explanation of the voltage clamp from a physiological point of view. In conclusion, the voltage clamp records the transmembrane current from just one of the contributors allowing its independent study.

1.3. The voltage clamp

The inclusion of voltage clamps in CMOS-based neural interfaces is very recent. To our knowledge, the two prominent examples of voltage clamps in integrated circuits were published from 2019 onwards.

Status Quo

In both examples [49] [3], the authors exploit the already explained advantages of using CMOS technology to include the clamp into the neural interface. They also use a trans-impedance amplifier (TIA) as the primary element of the circuit.

On the one hand, Shepard et al. [49] presented a miniaturized multi-clamp integrated into an intracellular CMOS neural interface. Their project has scaled down significantly the size of a traditional microscale neural interface, namely the patch-clamp, which traditionally relied on discrete parts [39]. Despite scaling down the circuit, the sensor is a micropipette as in the original patch clamp. This pipette is modeled in Fig. 1.4 as a resistor R_s and a parasitic capacitance C_p. In other words, this work scales down the size of the processing circuitry of a patch-clamp. However, it does not convert it into a mesoscale interface because the micropipette limits the number of cells studied simultaneously.

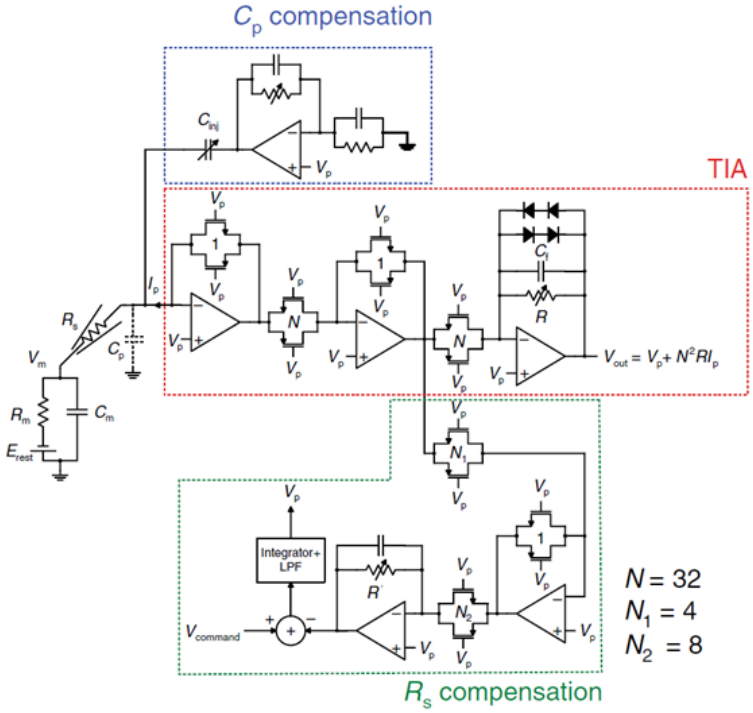


Figure 1.4: Schematic of an integrated microscale multi-clamp of an intracellular CMOS neural interface. The micro-pipette modeled with R_s senses the signal from a neuron. The compensation circuits attenuate the effects of the pipette and parasitics in terms of frequency response. The TIA allows to perform clamps and amplifies the signal that is sensed in the micro-pipette. Source: [49].

On the other hand, Ham et al. [3] published a CNEI with integrated voltage-clamp amplifiers. In this case, the interface is mesoscale because a nanoelectrode array is used. As it can be seen in Fig. 1.5, the basic working principle is that the voltage of the electrode can be fixed with $V_{s,1}$ through an amplifier with negative feedback. Then, the electrode voltage sets the membrane voltage. Because of the indirect nature of the voltage fixing from $V_{s,1}$ to V_m, the voltage clamp in the CNEI is known as the pseudo-voltage clamp. While clamping the voltage, it is possible to record the current through the electrode thanks to the trans-impedance character of the amplifier.

Since this thesis focuses on mesoscale interfaces, the voltage clamp in [3] is used as the primary reference.

Objective

This thesis designs a pseudo-voltage clamp for a CMOS-based mesoscale neural interface for intracellular recording and stimulation. The objective is to minimize the noise contribution of the circuitry to improve the signal-to-noise ratio of the current recording, provide the largest possible clamping voltage swing, and use a small area. Meanwhile, the rest of the performance aspects, such as bandwidth, stability, gain range, power, etc., must meet reasonable specifications. The design intends to be transparent and easily adjustable to allow fellow researchers to modify the design parameters once the electrodes are manufactured.

In summary, the research question can be defined as: How can a very low-noise, small, and sizeable voltage-clamp range pseudo-voltage-clamp be designed so that the result is flexible for future modifications?

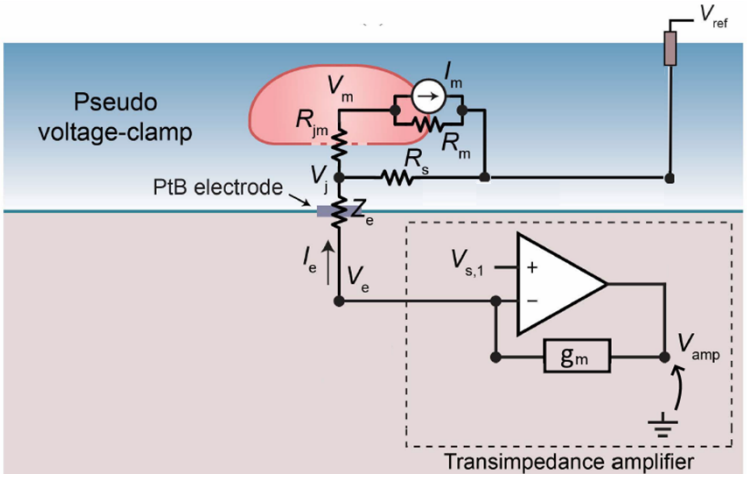


Figure 1.5: Schematic of a pseudo-voltage-clamp integrated in a CNEI. The sensor is a nanoelectrode represented with Z_e. The TIA clamps the voltage of the nanoelectrode V_e and amplifies the signal I_e that is sensed in it. Source: [3], edited.

Approach

There are two elements in the project which are essential to determine the methodology. First, it is not known if the design is feasible. Therefore, the method has to allow us to study show-stoppers, which are limitations imposed by the process. Second, some of the initial parameters are likely to change in the future. As a result, the method has to be flexible enough to adapt to those changes without causing a significant disruption to the final design and need to be transparent for other designers.

The selected method for topology design is called Structured Electronic Design (SED). While in the classic approach, known topologies are adapted to the new specifications, SED uses specs to create new circuits. In the classic approach, it is possible to spend long periods adapting previous circuits when there is no solution. In SED, if those specs are not feasible, it is not possible to create new circuits, but a show-stopper is found instead. Similarly, while fixes in the classic approach are frequently stacked, SED seeks an orthogonal design. This latest design approach allows designing step by step so that each decision does not severely affect the results of the previous steps. This procedure facilitates later readjustments in the design.

At the same time, at the level of transistor design, the thesis relies on the EPFL-EKV transistor model, which allows symbolic analysis while providing enough accuracy. The critical parameter in all expressions is the inversion coefficient (IC), which acts like an orthogonal proxy that defines the inversion level. In the square-law model, the parameter that describes the inversion level is V_{ov}. However, V_{ov} is only valid in strong inversion and is subject to the inaccuracy of V_{gs} in CMOS technology. The IC allows using the EPFL-EKV model smoothly for any operation region. Additionally, the EKV model and the IC proxy provide a transparent decision-making scheme that facilitates colleagues to reuse the work presented in this thesis in the future.

Thesis structure

This thesis is organized into six Chapters and one Annex.

After this Introduction, the Literature Review in Chapter 2 covers the basic theory behind the neural signals and the electrical model of the neuron. It also presents the types of nanoelectrodes used to record those signals and more insights about the chips currently used to do voltage clamps.

The Methodology in Chapter 3 explains in more detail the transistor level modeling and the system-level design approach that is used for designing. All design steps and decisions to create the controller and the feedback network of the amplifier are shown in Design, Chapter 4.

The Results in Chapter 5 include the relevant simulations of the whole system and summarizes the overall estimated performance. The Conclusions in Chapter 6 put those results into context and include suggestions for future research.

The Annex A includes supplementary materials as the scripts that are used to semi-automatize the design of the voltage clamp.

2

Literature review

This chapter covers the fundamentals in neurophysiology and nanoelectrodes, and it also provides a more detailed explanation of how Ham et al. [3] pseudo-voltage clamp works. Therefore, the literature review allows understanding how the information is generated in the source -the neuron-, how it is translated from the physiological to the electronics domain in the nanoelectrode, and how it is processed in the CMOS circuitry. This chapter also allows understanding the inverse pathway: how the CMOS circuity controls the physiological response by implementing the voltage clamp.

2.1. The physiology behind the voltage clamp

The source of the information that a neural interface is targeting is the neuron.

The neuron

Neurons are cells that are specialized in processing and transmitting information in the form of electrical signals. Like all biological entities, their morphology, which can be seen in Fig. 2.1, adapts to their purpose. Their axons carry electrical signals, namely changes in the voltage across the membrane that propagate as a wave and self-regenerate. These signals are called action potentials. The information encoded in the action potentials is transmitted to the subsequent neurons from the transmitter's axon to the receptor's dendrites using synaptic contacts. Most of these contacts work thanks to chemical neurotransmitters sent to the receptor to modify its electrical properties. When this happens, the recipient neuron might generate its own action potential.

The membrane

From the previous paragraph, it is evident that the membrane plays a crucial role in information transfer. Its formation relies on molecular polarity. The head of the membrane molecules is made of phosphoglyceride, which is hydrophilic, while the tail is composed of fatty hydrocarbon, which is hydrophobic. In an aqueous medium such as the human body, those molecules tend to form clusters in which the exposure of fats to water is reduced so that entropy increases [31]. This clusterization creates a bilayer of lipid molecules that isolate the inside from the outside of the neuron. However, the membrane has proteins that allow some ions to flow inwards or outwards at a rate that depends on variables. The most crucial variable is the potential difference across the membrane because voltage-dependent peptides regulate those proteins. In the case of the neurons, the main channels regulate the flow of sodium (Na+), potassium (K+), and chloride (Cl-).

At rest, the membrane is slightly permeable to Na+ but highly permeable to K+ and Cl-. The K+ concentration difference between the inside and outside of the cell (about 10-30 times lower in the outside[35] [8]) creates a diffusion gradient outwards. From the electrical perspective, the membrane can be seen as a leaky capacitor with an electric field inwards that inhibit the additional transfer of positive charge out of the membrane. This electric field comes from the K+ ions that have diffused outside, creating charge imbalance. The diffusional and electrical forces oppose and compensate each other while in dynamic rest (the net current is zero). The Goldman-Hodgkin-Katz equation gives the voltage across the membrane during dynamic rest. The equilibrium voltage for each ion species

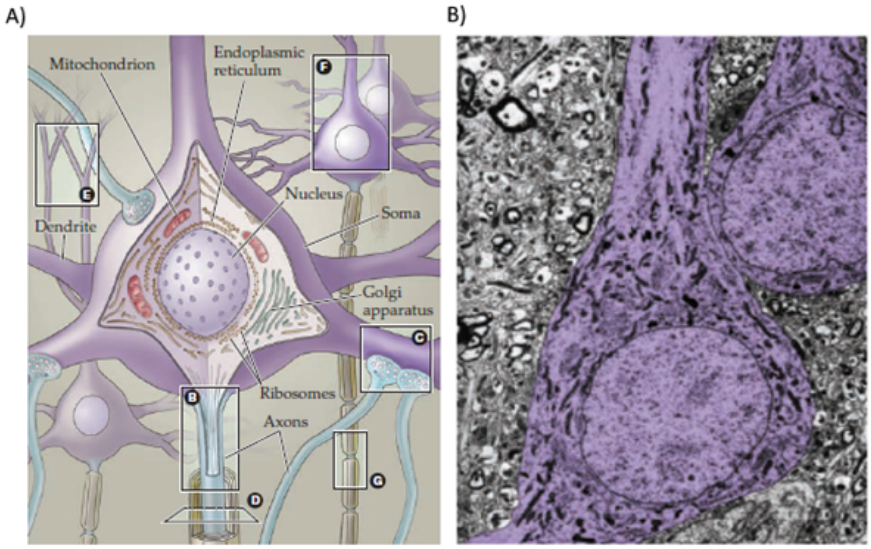


Figure 2.1: A) Diagram of a neuron and its parts. B) Picture of the neuron's soma. Source: [45].

can be obtained with the Nernst equation. The result of the Goldman-Hodgkin-Katz equation is about $-65\ mV$ in mammalian. The Cl- has a similar Nernst equilibrium voltage, while K+ has a lower one, and Na+ has a higher one. Therefore, K+ goes out while Na+ enters the cell. Na-K pumps maintain concentrations stable at the expense of ATP energy.

The action potential

As mentioned earlier, the information is encoded in action potentials, which are signal spikes that happen after surpassing a voltage threshold. An action potential is modeled with the voltage-gated mechanism, which defines the permeability for each ion species depending on the transmembrane voltage.

The permeability of an ion species is a quasi-continuous function that arises from the addition of many binary states. Those binary states represent an open or closed gate. In other words, a protein can allow or block the flow of ions through itself, and the larger the number of proteins that allow the flow, the larger the overall permeability of the ion species through the membrane is.

The probability of a gate being open is modeled with several enabling and disabling particles. Potassium gates are open if four "n" enabling particles are attached. In contrast, sodium gates are open if three "m" enabling particles are attached and one "h" disabling particle is not attached. Eqs. 2.1 and 2.2 give the overall transmembrane conductivities for those species. n_{rel}, m_{rel}, h_{rel} are the number of particles in the permissive state over the total number of particles.

$$G_K = G_{K,max} n_{rel}^4 \tag{2.1}$$

$$G_{Na} = G_{Na,max} m_{rel}^3 h_{rel} \tag{2.2}$$

The probability of those particles attaching to the gates is voltage-dependent. The rate at which the probability of particles being in a permissive state change versus the transmembrane voltage is called α, while the non-permissive state is called β.

The action potential (Fig. 2.2) is generated when the transmembrane voltage reaches a threshold from which the rest state does not longer hold (around -40mV). Below this threshold, β is more significant than α for both Na+ and K+, so most channels remain closed. Near the threshold, the α_{Na+} is much larger than α_{K+}. This difference makes the membrane permeable to the Na+, which flows into the cell due to the electric field. As a result, the transmembrane voltage goes from rest around $-65\ mV$ towards positive values. While the voltage increases, α_{K+} increases, so some K+ gates open. However, α_{Na+} also keeps increasing. Therefore, there is K+ flow out of the cell, but Na+ inflow keeps dominating the voltage increase. The inflection point occurs when V_m is around $20\ mV$. At that moment, the h-particles start attaching to the Na+ gates, so the inflow of Na+ stops while K+ keeps out-flowing.

This flow causes the transmembrane voltage to decrease, even below rest values. Because of this, it is much more difficult to trigger a new action potential until the rest voltage has been recovered, protecting information from flowing backward in the nervous system.

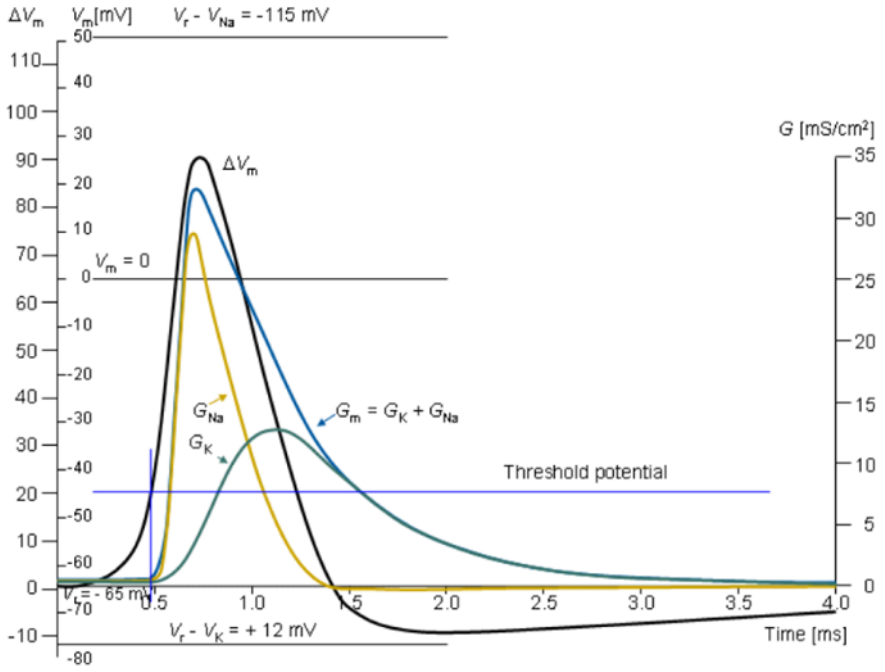


Figure 2.2: Conductance of each ionic channel and transmembrane voltage variation versus time when an action potential is triggered. Source: [35].

Sub-threshold events such as post-synaptic potentials (PSPs) and other small potential membrane oscillations do not generate action potentials but can also be recorded. The typical frequencies of membrane potential oscillations are between 1 and 50Hz, of PSPs about 100Hz, and of APs between 500Hz and 1kHz [51]. The total interest bandwidth for neural signals is between 1Hz and 10kHz.

Electrical model

The ionic flow across the membrane can be modeled with an electric circuit equivalent (Fig. 2.3). This equivalent is essential to model a neuron and interface it with an electronic system.

Each type of ionic channel can be modeled with a Nernst voltage source and a conductance whose value is given by Eq.2.1 & 2.2. When the voltage across the membrane is equal to the Nernst voltage of a channel, the net current through those channels is zero (equilibrium). The channel tagged as L, meaning leakage, model the effect of secondary channels such as the Cl- and is usually neglected in simplified models. Additionally, there is some current through the membrane that results from the capacitive coupling. This coupling can be modeled with a capacitor C_m that directly connects the inside and outside of the membrane.

The voltage clamp

As introduced in Chapter 1, the voltage clamp fixes the transmembrane voltage of neurons to allow the study of the conductivity of each kind of ionic channel. This technique can be easily explained using the electrical equivalent, bearing in mind that the current through the membrane is given by Eq. 2.3.

$$I_m = C_m \frac{dV_m}{dt} + (V_m - V_K)G_K + (V_m - V_{Na})G_{Na} + (V_m - V_L)G_L \tag{2.3}$$

Voltage clamping means that the voltage is fixed and constant (or changes are slow compared to the time constant of the equivalent impedance). Therefore, the capacitive branch is canceled by the voltage clamp. Additionally, one of the ionic channels is canceled by applying a Nernst voltage clamp to compensate the Nernst source (around $-101\ mV$ for the potassium, or around $-65\ mV$ for the sodium)

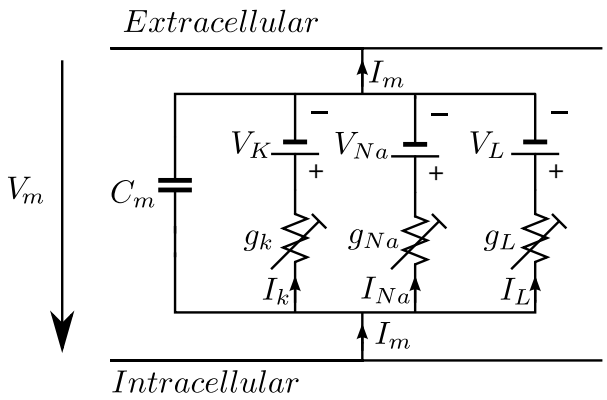


Figure 2.3: Electric model of a neuron. C_m models the current flow due to capacitive effects of the membrane. The other three branches represent the two main ionic channels (potassium K+ and sodium Na+) and the leakage channel (the rest of the species). V_K and V_{Na} are the Nernst voltages (around $-101mV$ and $-65mV$, respectively). g_K, g_{Na} are the conductances of the ionic channels, which depend mainly on the voltage or the presence of drugs.

or using drugs to make the conductance to be zero (tetraethylammonium -TEA- for the potassium, or tetrodotoxin -TTX- for the sodium). Lastly, the leakage branch can be ignored. Therefore,

$$I_m = (V_{clamp} - V_{ion})G_{ion} \tag{2.4}$$

, where V_{clamp} is a control variable, I_m is the measured variable, and the Nernst voltage of the ion species under study V_{ion} is known, so

$$G_{ion} = \frac{I_m}{(V_{clamp} - V_{ion})} \tag{2.5}$$

In conclusion, when a voltage clamp is applied, it is possible to cancel the current contributions of all branches but one, which allows an independent study of that particular branch.

2.2. Types of nanoelectrodes

The electrodes transduce the ionic currents coming from neurons into electrical currents that can be measured and processed using electronic circuits, namely CMOS devices. A wide variety of nanoelectrodes for intracellular recordings can be grouped depending on their material, shape, or how they perforate the cell.

Most nanoelectrodes are manufactured using noble materials such as gold or platinum, iridium dioxide, or novel materials such as carbon nanotubes. On the surface, it is common to add rough materials such as Pt-black, active chemical coatings such as engulfment-promoting peptides, or coatings combining hydrophilic and hydrophobic layers to mimic the membrane. The objective is to have chemically inert nanoelectrodes to increase the life-span of the recordings, to have a high surface-to-volume ratio to reduce the equivalent impedance [1], and also to prevent the formation of bubbles during current injection [14].

The most common shapes are the nano-pillars or tubes, straight or kinked; planar meta electrodes; mushrooms; and volcanos. Those shapes can be visualized in Fig. 2.4. Table 2.1 points to articles where the different shapes have been used. This table also summarizes the reported signal amplitudes, recording times, and the access method.

Regarding the perforation techniques, there are three main methods: spontaneous, electroporation, and optoporation. Spontaneous perforation is passive, which means that it does not require any impulse. It can be unaided, which is unlikely to happen, or aided, using hydrophilic and hydrophobic bands or engulfment-promoting peptides on the nanoelectrodes. Electroporation requires an electrical signal with enough power to break the membrane dielectric and form nanopores. It can be persistent if a holding current is applied afterward or non-persistent if there is no need for such current. Optoporation uses an optical signal to break the membrane. Its main advantage is that the poration signal is decoupled from the electrical activity of the neuron. Table 2.2 points to articles where each kind of poration was used. It also summarizes the type of signal that was used to perforate the membrane, if applicable.

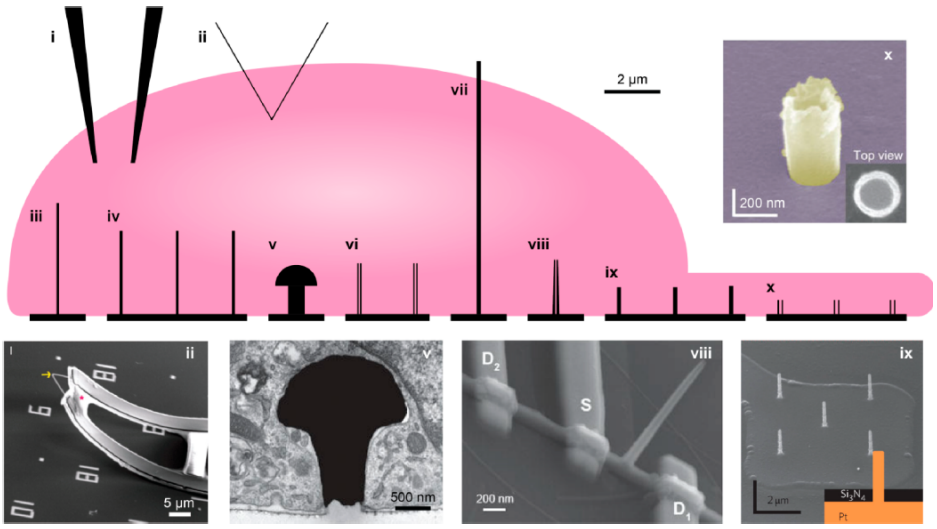


Figure 2.4: Diagram showing the silhouette of different types of nanoelectrode and pictures of some of them: ii) kinked, v) mushroom, viii) FET-based, ix) pillar, x) tube. Source: [1]

Table 2.1: Comparison of electrodes with different shapes.

Electrode type	**Signal amplitude**	**Recording time**	**Access method**
Nanopillars	Neurons: $< 5\ mV$ [48], $1 \sim 30\ mV$ [3], $30\ mV_{p-p}$ (hiPSC-derived dopaminergic) [33], $20 mV_{p-p}$ (hippocampal) [33]. Cardiomyocytes: $< 1.8\ mV$ [14], $< 1\ mV$ [15], $< 10\ mV$ [56], $25\ mV$ [32], $80\ mV$ [54]	120 sec (30% decay), 10 min back to extracellular, [56] days [32], 80 min [14]	Electroporation: [32][2]. Spontaneous: [33][30]. Optoporation: [15].
Planar meta-electrode	Cardiomyocytes: $\approx 4\ mV$ [16]	10-20 min [16]	Plasmonic optoporation
Mushroom	$< 5\ mV$ [14]	-	Electroporation
Volcano	Cardiomyocytes: $< 20\ mV$ [14]	≈1h [14]	Spontaneous

Table 2.2: Comparison between different electroporation techniques.

Work	**Type of poration**	**Signal type and shape**	**Properties**
Lin2016 [32]	Non-persistent electroporation	AC, voltage, square train	100 consecutive biphasic and symmetric, period: 400 μs, amplitude: 3.5 V
Lopez2018 [34]	Non-persistent electroporation	AC, voltage, square train	20 pulses, amplitude: 2 V, width: 10 ms, frequency: 50 Hz
Dipalo2018 [16]	Optoporation	AC, voltage, square train	Nd:YAG solid-state coherent laser (λ = 1,064 nm) 8 ps pulse width, repeated at 80 MHz
Desbiolles2019 [14]	Aided spontaneous		Optimized shape: high aspect ratio
Abbott2020 [2]	Persistent electroporation	DC, current	Access: -1nA Holding: -1.1nA
Lee2014 [30]	Non-aided spontaneous		
Liu2017 [33]	Non-aided spontaneous		
Tian2010 [54]	Aided spontaneous		Optimized adhesion: phospholipid bilayers.
Hai2010 [22]	Aided spontaneous		Optimized adhesion: engulfment-promoting peptide (EPP).
Robinson2012 [48]	Persistent electroporation	AC, voltage, square train DC, current	Voltage: 100ms pulses ±3V Current: –200 to –400 pA Adjustable holding current
Xie2012 [56]	Non-persistent electroporation	AC, voltage, square train	2.5 V, 200 ms biphasic pulses

Regarding Tables 2.1 & 2.2, it is vital to bear in mind that all those reported results were obtained in different contexts and, in many articles, this context is not fully defined. For example, there are significant differences between nanoelectrodes in large arrays due to fabrication issues, but only one of those nanoelectrodes is characterized in many articles. In other cases, the electrode impedance is measured, but the frequency of the test signal is not specified. Therefore, direct comparisons between electrodes in the different articles are not possible.

The takeaway from the tables is that the recording characteristics (e.g., the signal's amplitude, recording period, impedances) strongly depend on the type of electrode and the context of the measurement. Therefore, as long as the electrodes that will be used in the project are not manufactured and characterized, it is necessary to use an electrode model that is simple and generic enough to represent all electrodes.

2.3. State-of-the-art integrated voltage clamp

As explained in Chapter 1, the device of Ham et al. [3] can be used to perform a voltage clamp if the amplifier is configured as a trans-impedance amplifier (Fig. 1.5). The voltage clamp has a dual purpose since it is also used for persistent electroporation.

Working principle

To cause electroporation, the voltage clamp is set to about $V_e = -0.6 \sim -0.7\ V$, which generates current of about $I_e = -0.9 \sim 2.2\ nA$ [3]. After that, a holding current of a similar value is maintained to keep the neuron permeability, to compensate leakage current, and to keep the neuron at a healthy voltage [2].

On top of the electroporation and holding voltage/current, the voltage clamp can measure the conductivity of the ionic channels, which is the fundamental function of a voltage clamp. To do so, a $\Delta V_{s,1}$ is applied. The voltage variation is copied into the other port of the Operational Amplifier (OpAmp) as $\Delta V_e = \Delta V_{s,1}$. The voltage variation is then transferred to the membrane as a ΔV_m. This membrane voltage variation produces a ΔI_m that can be recorded as ΔI_e thanks to the trans-impedance character of the amplifier. The estimated ΔI_e is about $100\ pA \sim 1\ nA$ [3]. Ham et al. [3] considers that the transfers of voltages and currents of the electrode and the membrane relate proportionally with an attenuation factor, as seen in Eq.2.6.

$$\frac{\Delta I_e}{\Delta I_m} \approx \frac{\Delta V_m}{\Delta V_e} \approx \frac{R_m}{R_m + R_{jm}} \tag{2.6}$$

Transimpedance amplifier implementation

Ham et al. [3] chip contains 4096 pixels. Each pixel has a trans-impedance amplifier implemented with an OpAmp and a pseudo-resistor to set the TIA gain (Fig. 2.5). The OpAmp is formed by a cascoded balanced common source PMOS stage, an NMOS common source with Miller compensation, and an output buffer. The pseudo-resistor is implemented with a switched capacitor. Its effective resistance is given by the equation $R_{TIA} = \frac{1}{f_{TIA} C_{par}}$, where $C_{par} \approx 35\ fF$ is the parasitic capacitance of the anti-parallel diode pairs (DPS) used in the pseudo-current clamp, a different function of the chip. Table 2.3 summarizes the key figures.

Table 2.3: Estimated key figures of Ham et al. [3] pseudo-voltage clamp.

Parameter	**Value**
Input voltage range	$[1, 2.4]\ V$
Output voltage range	$[0.1, 2.5]\ V @ V_{s,1} = 1\ V$ $[1.3, 2.7] V @ V_{s,1} = 2.4\ V$
Noise	From $1.1\ pA_{rms}$ to $6.8\ pA_{rms}$ $(@1Hz - 4.7kHz)$
Area per pixel	$0.025\ mm^2$ (only the OpAmp)
Power per pixel	$225\ \mu W$ (only the OpAmp)
Bandwidth	$DC - 4.7\ kHz$

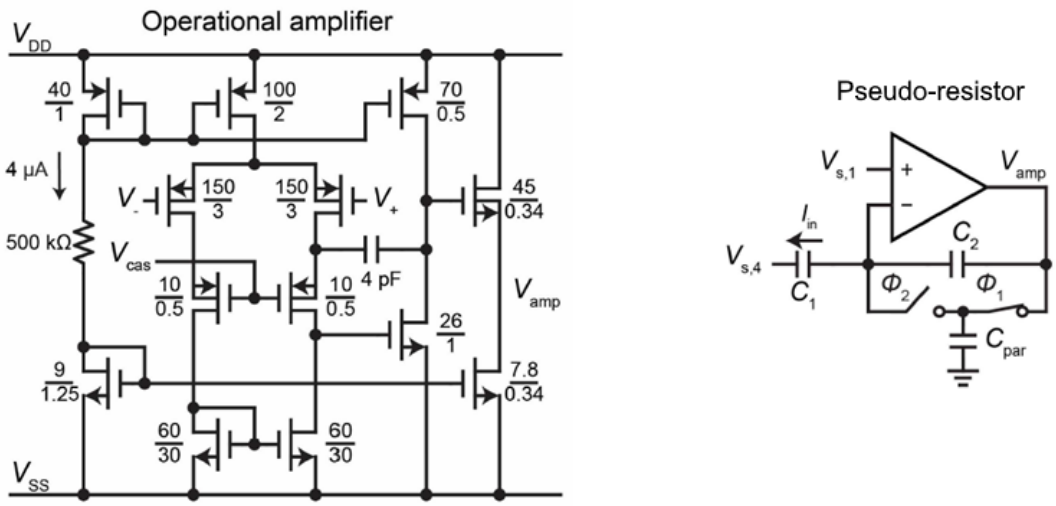


Figure 2.5: Schematics of the OpAmp and the pseudo-resistor used in [3] to create a pseudo-voltage clamp for an intracellular CMOS-based neural interface. Source: [3], edited.

3

Methodology

This chapter focuses on the methodology that is used to design the pseudo-voltage clamp. On the one hand, on the transistor level, the design relies on the EKV model. This model is suitable for design in strong inversion as the square-law model and also in moderate and weak inversion. Besides, it is simple enough to allow symbolic analysis, yet it is accurate enough for design purposes. On the other hand, the system level is designed using Structured Electronic Design (SED). This methodology allows detecting show-stoppers, having transparent design steps, and flexibility to modify parameters in the future.

3.1. Device modelling

Understanding the meaning of the inversion coefficient from a physical perspective is necessary to have a clear idea of the EKV model.

Device physics: inversion level

The difference in the concentration of dopants in each region of the PN junction in semiconductors generates a diffusion force. Because of the different polarity of the electronic species in the P and N areas, a built-up potential is also generated and opposes the diffusion forces. The combination of the species in the junction creates a depletion region. Fig. 3.1 represents this phenomena.

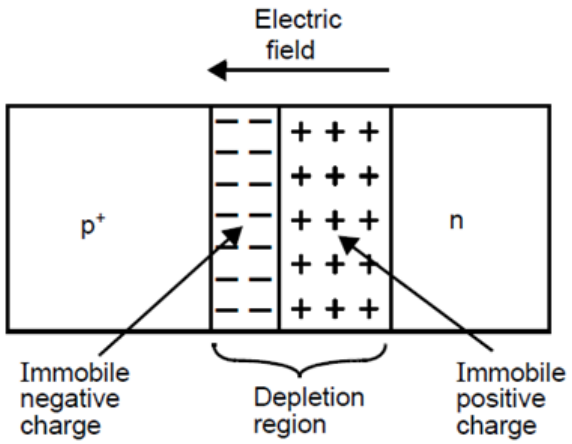


Figure 3.1: Diagram of a P-N semiconductor junction showing the redistribution of charges due to diffusion forces. This charge imbalance generates a electric field which compensates the diffusion force. When the forces are compensated, a deplection region with immobile charges is created. Source: [13]

An NMOS is formed by the union of N-P-N type semiconductors and a gate that regulates the charge in the region P. The gate is separated from the semiconductor with a dielectric layer.

When the voltage of the gate is negative, the positive charge from the p doped silicon is attracted near the gate, making the p area p+. The channel is “accumulated,” and there is just a leakage current between the drain and the source. [13].

When the voltage of the gate is positive, positive charges from the p doped silicon are pushed far from the gate, making the p area near the gate a depletion region with an equivalent capacitance represented in Fig. 3.2. The channel is “weakly inverted” and drives diffusion currents with an exponential behavior versus the gate voltage [13].

When the voltage of the gate is large enough, the depletion area becomes an n channel that connects the source and drain, as it is represented in Fig. 3.2. The channel is “strongly inverted” and drives drift currents with a quadratic behavior versus the gate voltage [13].

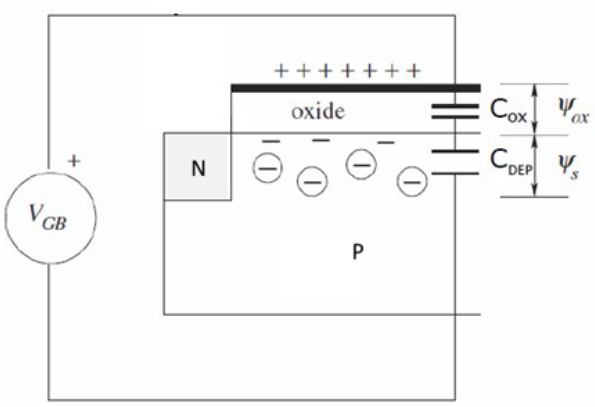


Figure 3.2: When a channel is inverted ($V_{GB} > 0$), negative charges (minus symbols in a circle) in the p area of an NMOS accumulate close to the gate oxide, forming a depletion region (weak inversion) and ultimately an n-channel between the source and the drain (strong inversion). The oxide and the depletion region capacitances are represented with C_{ox} and C_{DEP}, respectively. The n-channel is marked with minus symbols. Source: [44], edited

There is a state called “moderate inversion” between weak and strong inversion when the gate voltage equals the “threshold voltage.” This state happens when the concentration of holes in the body substrate far from the gate equals the number of electrons under the gate. The net current is a contribution from diffusion and drift currents. [13].

This explanation applies to PMOS transistors as long as the voltages and the regions P and N are reversed.

Limitations of the square-law

The inversion level in the square-law model is represented with the overdrive voltage V_{ov}, which is calculated as the difference between the gate voltage and the threshold voltage ($V_{gs} - V_{th}$). This definition is inconvenient in terms of accuracy and suitability for moderate or weak inversion [27].

On the one hand, the threshold voltage often varies by $0.1 \sim 0.2\,V$ due to process-voltage-temperature (PVT) variations [27]. This inaccuracy makes V_{ov} subject to large confidence intervals. Therefore, it is not possible to define the inversion level accurately with the square-law definition.

On the other hand, it is frequent to use V_{ov} to define the saturation voltage V_{sat}. If transistors are operating in weak or moderate inversion, the V_{ov} is negative or around zero, but the drain-source voltage needed to operate in the saturation region is always greater than zero. Therefore, the square-law is not only incapable of accurately defining the drain current–gate voltage relationship, but it also fails to describe the saturation requirements of a transistor in weak and moderate inversion.

Lastly, an additional limitation of the square-law model is the modeling of some short channel effects. For example, it misses the drain-induced barrier lowering (DIBL) and the vertical field mobility reduction (VFMR).

It would be necessary to turn to circuit simulations running on complex device models such as BSIM6 or PSP1 [27] to have an accurate picture of the inversion level, the saturation voltage, and other DC parameters. However, those models are too complex to use in design with symbolic analysis and have no physical meaning.

The EKV model for weak and strong inversion

The EKV model was created as a compact model for low-voltage, low-current analog, and mixed-signal circuits with short channel transistors for both design and simulation purposes [11].

In weak inversion the drain current is given by Eq. 3.1 [10].

$$I_D(WI) = I_{spec}\frac{W}{L}\exp(\frac{V_{GS}-V_{th}}{nU_T}) \tag{3.1}$$

where the sub-threshold factor n is given by the ratio between the deplection region capacitance and the oxide capacitance represented in Fig. 3.2; the thermal voltage U_t is given by the Boltzmann constant, the temperature, and the charge of an electron; and the specific current I_{spec} is given by the sub-threshold factor n, the electron mobility μ, the oxide capacitance, and the thermal voltage:

$$n(WI) \approx 1 + \frac{C_{DEP}}{C_{OX}} \tag{3.2}$$

$$U_T = \frac{kT}{q} \tag{3.3}$$

$$I_{spec} = 2n\mu C_{OX}U_T^2 \tag{3.4}$$

The g_m/I_D factor for weak inversion is constant and given by Eq. 3.5 [10].

$$\frac{g_m}{I_d}(WI) = \frac{1}{nU_T} \tag{3.5}$$

In strong inversion the current becomes quadratic, as given in Eq. 3.6 [10].

$$I_D(SI, \text{no effects}) = \frac{1}{2}\frac{\mu C_{OX}}{n}\frac{W}{L}(V_{GS}-V_{th})^2 \tag{3.6}$$

and g_m/I_D is not longer constant, as seen in Eq. 3.7 [10].

$$\frac{g_m}{I_d}(SI) = \frac{2}{V_{GS}-V_{th}} \tag{3.7}$$

The description of the $I_D(SI)$ with Eq. 3.6 does not consider second-order effects, such as velocity saturation (VS), VFMR, channel-length modulation (CLM), DIBL, or body effect (BE).

In a strong inversion, the velocity of the carriers is proportional to the lateral electric field. However, if the electric field is stronger than a critical value E_{crit}, the velocity does not longer increase. This limit is known as velocity saturation. It can be modeled introducing a correction factor to Eq. 3.6, as shown in Eq. 3.8 [10].

$$I_D(SI, \text{inc. VS}) = \frac{\frac{1}{2}\frac{\mu C_{OX}}{n}\frac{W}{L}(V_{GS}-V_{th})^2}{1+(V_{GS}-V_{th})\frac{1}{LE_{crit}}} \tag{3.8}$$

The VFMR happens in processes with slim oxide thickness, where the vertical electric field becomes strong. This field pulls the carriers closer to the imperfect silicon surface. Consequently, the effective electron mobility drops. It can be modeled introducing the VFMR factor θ in the correction factor of Eq. 3.8, as shown in Eq. 3.9 [10].

$$I_D(SI, \text{inc. VS, VFMR}) = \frac{\frac{1}{2}\frac{\mu C_{OX}}{n}\frac{W}{L}(V_{GS}-V_{th})^2}{1+(V_{GS}-V_{th})(\theta+\frac{1}{LE_{crit}})} \tag{3.9}$$

The CLM reduces the effective length of the transistor due to the drain depletion region widening. The larger the drain-source voltage (V_{DS}), the stronger the CLM effect. This effect makes the the term L in the previous equations to become $L' = L - l_{CLM}$, as in Eq. 3.10. The most important consequence is on the output conductance, which gains an additional factor $\delta l_{CLM}/\delta V_{DS}$, as seen in Eq. 3.11 [10]. This additional factor can be represented with the inverse of the Early voltage factor (V_{AL}), which is a quality factor that describes the production of output conductance g_o for a given I_D and per length unit.

The calculation of V_{AL} to represent the CLM is difficult. One of the simplest equations to estimate its value is given at Eq. 3.12 [10], where N_B is the doping concentration, ϵ_{Si} the permittivity of silicon, and ϕ_D the built-in potential of the pinched-off drain side of the channel and the drain.

$$I_D(SI, \text{inc. CLM}) = \frac{1}{2}\frac{\mu C_{OX}}{n}\frac{W}{L - l_{CLM}}(V_{GS} - V_{th})^2 \tag{3.10}$$

$$g_o(\text{inc. CLM}) = \frac{\delta}{\delta V_{DS}} I_D(SI, \text{inc. CLM}) \approx \frac{I_D}{L}\frac{\delta l_{CLM}}{\delta V_{DS}} = \frac{I_D}{L V_{AL_{CLM}}} \tag{3.11}$$

$$V_{AL_{CLM}} \approx 2\sqrt{\frac{qN_B}{2\epsilon_{Si}}}\sqrt{(V_{DS} - V_{DS,sat}) + \phi_D} \tag{3.12}$$

DIBL is an effect that appears in short-channel transistors. When the V_{DS} increases, the V_{th} decreases. This effect arises because the drain is so close to the gate that the drain voltage contributes to creating the channel between the drain and source. It can be modeled also with V_{AL}, as shown in Eq. 3.13 [10]. L_{min} is the minimum length of the process, ***DVTDIBL*** is the $\delta V_{th}/\delta V_{DS}$ for L_{min}, and ***DVTDIBLEXP*** describes the decrease of ***DVTDIBL*** for $L > L_{min}$.

$$V_{AL_{DIBL}} \approx \frac{I_D}{L g_m(-\textit{DVTDIBL}(\frac{L_{min}}{L})^{\textit{DVTDIBLEXP}})} \tag{3.13}$$

The equivalent V_{AL} including both CLM and DIBL is given by Eq. 3.14 [10]. The V_{AL} is, therefore, dependant on the inversion level of the device, the length, and the drain-source voltage. The value of the output conductance is updated in Eq.3.15.

$$V_{AL} = V_{AL_{DIBL}} || V_{AL_{CLM}} \tag{3.14}$$

$$g_o(\text{inc. CLM, DIBL}) = \frac{I_D}{L V_{AL}} \tag{3.15}$$

The body effect also affects the V_{th}. Considering NMOS, when the bulk voltage is smaller than the source voltage ($V_B < V_S$), more holes are attracted to the substrate, and V_{th} rises. When $V_B > V_S$, V_{th} decreases. This effect can be modeled with the body effect coefficient γ as in Eq. 3.16, where ϕ_0 is the silicon surface potential in strong inversion.

$$n = 1 + \frac{\gamma}{2\sqrt{(V_{GS} - V_{th})/n + V_{SB} + \phi_0}} \tag{3.16}$$

In conclusion, second order effects in strong inversion can be modeled with θ, E_{crit}, $V_{AL}(IC, L, V_{DS})$, and γ.

The EKV model with an orthogonal proxy representing the inversion level

As it was underlined before, the EKV model intends to model transistors in any inversion level. The equations of weak and strong inversion are unified using a parameter that represents the inversion level of the device. This proxy is orthogonal as long as all the parameters which define it are independent of the inversion level. While some authors use the g_m/I_D as orthogonal proxy [26], this figure of merit is not useful in weak inversion because g_m/I_D is constant, as seen in Eq. 3.5. An alternative is to use the inversion coefficient IC, which is defined in Eq.3.17 [10].

$$IC = \frac{I_D}{2n\mu C_{OX} U_T^2 \frac{W}{L}} = \frac{I_D}{I_{spec}\frac{W}{L}} \tag{3.17}$$

The problem of this definition is that n and μ depend on the inversion level, so if IC is defined in this way, it is not orthogonal [27] [10]. Some numerical accuracy is sacrificed to achieve orthogonality by defining IC as in Eq. 3.18 [10], where n_0 is the sub-threshold factor in moderate inversion, μ_0 is the low field electron mobility, and I_0 is the technology current. Those three parameters are no longer dependant on the inversion level because they are constant.

$$IC = \frac{I_D}{2n_0\mu_0 C_{OX} U_T^2 \frac{W}{L}} = \frac{I_D}{I_0 \frac{W}{L}} \tag{3.18}$$

Lastly, to include the VS and VFMR in those definitions, an additional parameter IC_{crit} is introduced. Its expression is Eq.3.19.

$$IC_{crit} = (\frac{LE_{crit}}{4n_0 U_T(\theta + \frac{1}{LE_{crit}})})^2 \tag{3.19}$$

Using the newly defined proxy and the correction factor, all parameters can be redefined for any inversion level. g_m is defined in Eq. 3.20 [10], V_{ov} in Eq. 3.21 [10], and $Vsat$ in Eq. 3.22 [10] and Eq. 3.23 [27]. The latest equation is a conservative estimation that is useful to ensure that a transistor is saturated despite confidence intervals, and is based on Eq. 3.7.

$$g_m = \frac{I_D}{nU_T(\sqrt{IC + 0.5\sqrt{IC}} + 1)}, IC = IC(1 + \frac{IC}{IC_{crit}}) \tag{3.20}$$

$$V_{ov} = 2nU_T ln(e^{\sqrt{IC}-1}), IC = IC(1 + \frac{IC}{4IC_{crit}}) \tag{3.21}$$

$$V_{sat} = 2U_T\sqrt{IC + 0.25} + 3U_T \tag{3.22}$$

$$V_{sat}(\text{conservative}) = \frac{2I_D}{g_m} \tag{3.23}$$

Capacitive effects modeling

An essential parameter of a transistor is the transit frequency f_t, which defines its speed. The value of f_t strongly depends on the capacitances within the transistor. The f_t can be calculated as in Eq. 3.24 [40].

$$f_t = \frac{g_m}{2\pi C_{iss}} \tag{3.24}$$

C_{iss} is the input capacitance with the output shorted and can be calculated from the total gate capacitances, as in Eq. 3.25 [41]. The dominant contributor is the C_{GS}, which can be calculated with Eq. 3.26 [41] if the intrinsic contributions are neglected. ϵ is the permittivity, and T_{OX} and C_{GSO} are process constants defining the oxide thickness and the gate-source overlap capacitance per unit area, respectively. Similarly, the rest of the capacitances can also be expressed in terms of process constants and dimensions.

$$C_{iss} = C_{GS} + C_{GD} + C_{GB} \tag{3.25}$$

$$C_{GS} = \frac{2}{3}WL\frac{\epsilon_0\epsilon_{SiO_2}}{T_{OX}} + C_{GSO} \tag{3.26}$$

Noise modeling

The noise of a transistor can be represented with two current noise spectral density contributors as in Fig. 3.3: one at the drain (Eq. 3.27) [40] and another at the gate (Eq. 3.30) [40].

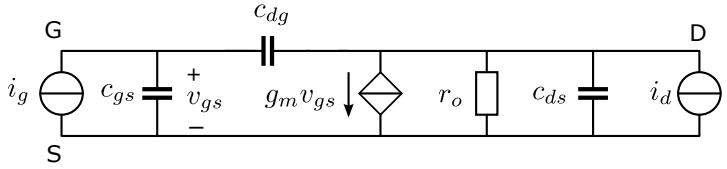


Figure 3.3: Small signal of a transistor and the noise sources associated with the gate and the drain represented as a current sources i_g and i_d, respectively.

$$S_{id} = 4kTn\Gamma g_m(1 + (\frac{f_l}{f})^{A_F}) = \frac{4kT}{R_N}(1 + (\frac{f_l}{f})^{A_F}) \tag{3.27}$$

$$\Gamma = \frac{1}{1 + IC}(\frac{1}{2} + \frac{2}{3}IC) \tag{3.28}$$

$$f_l = \frac{3K_F g_m}{8kTn\Gamma C_{gs}} \tag{3.29}$$

$$S_{ig} = 2qI_G(1 + f_c/f) \approx 0 \tag{3.30}$$

Both contributors have a white noise component coming mainly from thermal effects and a pink noise component coming from carrier mobility and density fluctuations due to trapping and de-trapping near the silicon-oxide interface. f_l and f_c are the corner frequencies where the pink and white noises have the same magnitude. K_F and A_F are EKV parameters that describe the pink noise level and the pink noise slope in the power spectrum density, respectively. S_{IG} is approximated to zero because I_G is usually below $1\ fA$. However, this assumption needs to be verified in the later stages of the design.

The simplified EKV for symbolic analysis and SLiCAP

SLiCAP (Symbolic Linear Circuit Analysis Program) [41] is a software package on Python that uses a simplified EKV model to calculate design equations, Laplace transfers, do noise analysis, or track poles and zeros of a system, among other functions. The use of SLiCAP is a fundamental part of the MSc project and directly impacts the results. Therefore, it is necessary to understand the EKV model and the differences of the simplified EKV model implemented in SLiCAP.

As it was seen in the previous subsections, a transistor can be modeled with θ, E_{crit}, $V_{AL}(IC, L, V_{DS})$, and γ for the second order effects; C_{GS},C_{GD},C_{GB}, for the frequency response; and K_F and A_F for the noise.

If SLiCAP is used symbolically, as it is intended, the larger the number of equations, the much larger the computation effort. To avoid unacceptable computing times, by now $V_{AL}(IC, L, V_{DS})$ is implemented as a constant V_{AL}, and the body effect factor γ is ignored. Besides, the C_{GS},C_{GD},C_{GB} are calculated using exclusively the extrinsic capacitance contribution, which is dominant. The rest of parameters remain unaltered and Eqs. 3.15 & 3.18-3.22 & 3.24-3.30 are implemented unchanged in SLiCAP. The definitions are available at `-SLiCAP_installation_path-/SLiCAP/lib/SLiCAP`.

Optimization using the IC

EKV models are a useful tool to work in weak/moderate inversion and model second-order effects. The proxy IC can also be used for transistor sizing purposes. Binkley's diagram (Fig. 3.4 [10]) perfectly summarizes the trade-offs on transistor-level design.

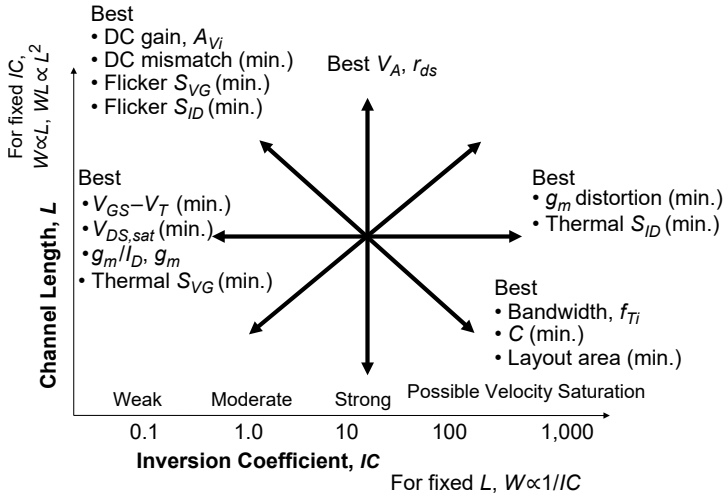


Figure 3.4: Tradeoffs in analog CMOS design based on the IC and the length of the transistors. Source: [10]

3.2. Orthogonal system design

This section describes the fundamental concepts of SED that are necessary to follow the design procedure in Chapter 4. The concepts are framed into subsections about noise, driving capabilities, feedback model (asymptotic gain model), accuracy and bandwidth, and frequency compensation.

The order of those subsections is essential. Firstly, the noise is studied. Suppose the noise specs cannot be met in an ideal scenario (e.g., considering only the contribution of the first stage of the controller). In that case, it will not be possible to meet the specification under any circumstance, and the design needs to be reconsidered. If the noise study is satisfactory, the driving requirements need to be analyzed to discover if a single-stage solution is feasible.

Once the noise and the driving requirements are satisfied, the accuracy and bandwidth requirements can be studied using the asymptotic gain model. This study allows determining the number of stages needed and the size of the devices in the signal path. Since introducing new stages likely degrades the stability, it might be necessary to introduce frequency compensation, which can also be designed with the help of the asymptotic gain model. Lastly, the circuit can be biased once all the signal-path is well defined and meets all specs.

Following this order and the SED concepts makes it less likely that the new decisions in each design step affect the previous. This isolation between design steps is the reason why SED is an orthogonal system design.

Noise and common-source stages

The study of the feasibility of noise specifications using SED is described at [40]. The key concepts are highlighted in the following lines:

- In a multiple-stage amplifier, the input stage determines the noise as long as each stage is close to an ideal two-port (unilateral behavior as close as possible to a theoretical nullor).
- Common-drain (CD) and common-gate (CG) amplifying stages are simply a common-source (CS) stage with feedback and are known as local feedback stages.
- Complementary parallel (e.g., push-pull) noise equivalent can be mapped into a non-balanced stage and ultimately to a common-source stage. The voltage noise spectrum is half and the current noise twice those of constituting elements. For the same noise performance as a CS non-balanced stage, it is necessary to halve the width and the drain current for each transistor (same area and total current in total, without considering the extra area of the PMOS to compensate for the reduction in the mobility).
- Anti-series stages (e.g., differential pair) noise equivalent can be mapped into a non-balanced stage and ultimately to a common-source stage. The voltage noise spectrum is twice and the current noise half as those of constituting elements. For the same noise performance as a CS non-balanced stage, it is necessary to double the width and the drain current for each transistor (x4 increase in area and current in total).
- The noise performance of a stage with feedback is equal or worse than the same stage without feedback. The feedback elements add noise unless the feedback elements are not energetic (e.g., transformer) or the feedback is ineffective (e.g., short-circuited output in a CD stage).
- The noise contribution of the feedback network is the same as if the feedback network is in series with the source impedance if the comparison is made in series (voltage and trans-admittance amplifiers).
- The noise contribution of the feedback network is the same as if the feedback network is in parallel with the source impedance if the comparison is made in parallel (current and trans-impedance amplifiers).

The takeaway is that if all stages are built from or on top of the CS stage, they will have an equivalent or worse noise performance. The best noise performance can be modeled with a CS stage. If the best is not enough, there is no solution (“show-stopper”). Later on, the CS stage can be converted into other stages by applying feedback and balancing techniques. Since the effect of feedback and balancing is

known, the conclusions derived for the CS stage can be adapted easily. Besides, with a careful design, we can ensure that each stage is as isolated as possible, such that the input stage mainly determines the amplifier noise.

The study of the noise in a CS stage can be easily simplified transforming the noise equivalent in Fig. 3.3 into a three-source input referred equivalent model, as shown in Fig. 3.5. The transmission matrix parameters B_1 and D_1 of a CS stage can be approximated as $-1/g_m$ and $-s/\omega_t$ as shown in Eqs. 3.31 & 3.32, respectively [40].

$$B_1 = \left.\frac{v_{GS}}{i_D}\right|_{v_D=0} = \frac{-1}{g_m(1 - s\frac{c_{gd}}{g_m})} \approx \frac{-1}{g_m} \quad \because \quad \frac{g_m}{C_{gd}} >> \omega_t = \frac{g_m}{C_{iss}} \tag{3.31}$$

$$D_1 = \left.\frac{I_G}{i_D}\right|_{v_D=0} = \frac{-S(C_{gs} + C_{gd})}{g_m(1 - s\frac{c_{gd}}{g_m})} \approx \frac{-sC_{iss}}{g_m} = \frac{-s}{\omega_t} \approx \frac{-sC_{gs}}{g_m} \tag{3.32}$$

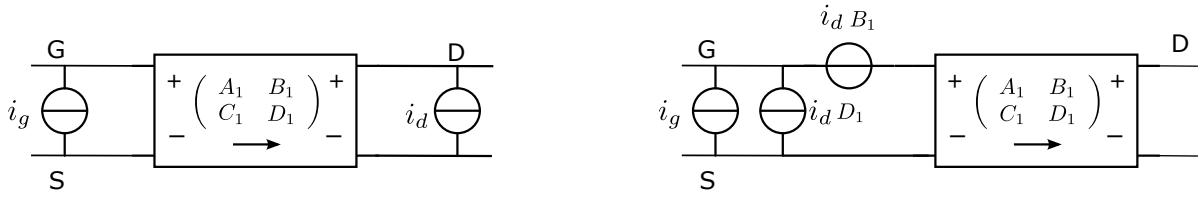


Figure 3.5: Transformation of the transistor current source i_d in Fig. 3.3 into the two sources $i_d B_1$ and $i_d D_1$ at the input of the transistor assuming a common source stage. The equations of the transmission parameters B_1 and D_1 are calculated in Eqs. 3.31 & 3.32, and the noise power densities in Eqs. 3.27 & 3.30

In conclusion, the steps that are needed to study and optimize the noise performance are the following:

- Step 0: Establish noise requirements.
- Step 1: Create a noise model using a CS single-stage amplifier as a controller.
- Step 2: Design the CS stage such that the noise performance is optimized. Check if the optimum is good enough to satisfy the requirements. If the noise requirement is not met, there is no possible solution (“show-stopper”).
- Step 3: Apply scaling factors to the optimum width and drain currents if a balanced stage is used.

Driving capabilities

The study of the feasibility of driving requirements using SED is described at [40]. The key concepts are stated in the following lines:

- In a multiple-stage amplifier, as long as each stage is close to an ideal two-port (unilateral behavior as close as possible to a theoretical nullor), the output stage determines the driving capabilities.
- All stages are built from or on top of the CS stage by applying feedback and balancing techniques. The conclusions derived for the CS stage can be used as the starting point and then adjusted for the new topologies because the effect of feedback and balancing is known.
- If the transistor parameters provide enough driving and satisfy the previous noise requirements, the amplifier’s design can start by considering a single-stage CS amplifier. If that is not the case, at least two stages are needed.
- The effect of the feedback network is the same as if the network is in series with the source impedance if the sensing is done in series (current and trans-admittance amplifiers).
- The effect of the feedback network is the same as if the network is in parallel with the source impedance if the sensing is done in parallel (voltage and trans-impedance amplifiers).

Asymptotic gain model

Negative feedback is the most powerful error reduction technique in low-frequency applications [40]. The quality of the feedback determines the bandwidth, linearity, and accuracy of an amplifier. However, the limitations in the controller can degrade the performance of the overall design. It is necessary to study the minimum requirements that a controller needs to let the feedback work properly. This examination can be performed with the asymptotic gain model (AGM) [40]. The elements that describe the AGM are presented in Fig. 3.6.

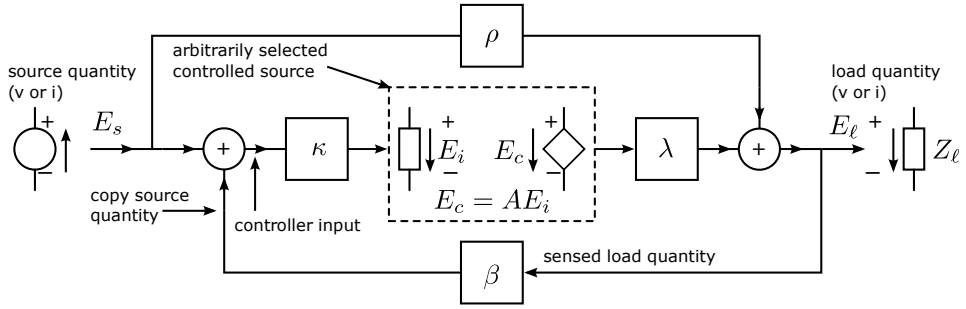


Figure 3.6: Asymptotic gain model that models the feedback of an amplifier. E_s: signal generated by the source. κ: transfer between the input of the controller and E_i. E_i: signal that controls the controlled source E_c. E_c: controlled source regulated by E_i. λ: transfer between the E_c and the output of the controller. E_l: signal received by the receptor. β: transfer of the feedback network. ρ: direct transfer between the source and the load that is not subject to correction in the feedback. Source: [40]

It is possible to calculate five functions that define the system using those elements: the ideal gain, the loop gain, the servo function, the direct gain, and the asymptotic gain. It is necessary to select as a reference source E_c one that if it becomes a nullor, the whole amplifier behaves as a nullor. In other words, if E_c has infinite gain, the controller input signal becomes zero. When a source is selected as a reference, it is considered an independent source in the AGM calculations. If the reference does not satisfy those requirements, the transfers are meaningless.

The five functions that describe the system in the AGM are described in the following lines:

- Ideal gain ($A_{f\infty}$): It is the amplifier gain if a nullor is used as a controller. In other words, it is the gain of the amplifier given by the feedback network and the loads without being affected by the controller's limitations.
- Loop gain (L): It is gain from the reference source E_c to the source E_i. In [**?**] it is known as return ratio.

$$L = \lambda A \beta \kappa \tag{3.33}$$

- Servo function (S): It represents the match between the ideal and the asymptotic gain due to the effect of the loop gain. In [**?**] it is known as discrepancy factor.

$$S = \frac{-L}{1-L} \tag{3.34}$$

- Direct transfer (D): represents the transfer between the amplifier's input and output that is not subject to feedback corrections. In [**?**] it is known as direct transmission term.
- Asymptotic gain (A_f): The asymptotic gain equals the ideal gain as long as the servo function is unity and the direct transfer is zero (e.g., if the controller is a nullor). It describes the real gain of the amplifier considering the non-idealities of the controller.

$$A_f = A_{f\infty} S + \frac{\rho}{1-L} \tag{3.35}$$

The AGM has several advantages in comparison to Black's model, which is frequently used. In fact, Black's model is just a particular case of the asymptotic gain with $\rho = 0$, $\kappa = 1$, $\lambda = 1$ and $\beta = -1/K$.

One of those advantages is that AGM allows a two-step design. First, the ideal gain can be designed considering the feedback network and the input and output loads. Then, the loop gain can be designed

such that it is large enough to cancel the effects of the direct transfer and such that the associated servo function is as close as possible to unity in the relevant bandwidth. If those requirements are met, the final asymptotic gain looks like the ideal gain for all the relevant bandwidth.

Additionally, AGM does not assume that the source and load impedances do not affect the loop gain of the amplifier. The effect of those loads is reflected in κ and λ. This advantage is significant, bearing in mind the large impedances that an electrode for neural applications has.

The limitation of the AGM is that the reference loop does not only require to be appropriately selected, but it also needs the local loops around it to be removed. The reason is that the measured loop gain from that reference could be the local loop gain instead of the overall loop gain.

There is a method that overcomes this limitation. This method was described by Middlebrook [36] in his General Feedback Theorem (GFT). The method allows the calculation of several loop gains simultaneously without the need for a reference source. All those loop gains contribute to the overall loop gain that describes the system.

Cadence's software, which is used in this project to verify all the circuits, has a loop gain probe [55] that is based on the GFT with a slight (and disputed [37]) variation regarding secondary loop gains. Although calculating several loop gains might be helpful for other applications as circuits with common and differential modes, the AGM is as valid as the GFT in this project because, in most cases, the contributions of these secondary gains are negligible for the overall loop gain [37]. Therefore, as long as a precaution is taken when selecting the reference source and canceling its local feedback, the loop gain obtained with the AGM should match the one from Cadence.

Accuracy and bandwidth

The study of the accuracy and bandwidth of an amplifier using SED is described at [40]. The key concepts regarding accuracy are highlighted in the following lines:

- The static inaccuracy of a negative feedback amplifier is determined by the static inaccuracy of the ideal gain (set by the feedback network) and the servo function (set by the controller).
- The static inaccuracy of the servo function is determined by the loop gain, as:

$$\delta_{MB} \approx \frac{1}{L_{MB}} \tag{3.36}$$

- If the accuracy is not enough to meet the specs, the loop gain must be increased. An option can be adding more stages. Alternatively, the inaccuracies of the ideal gain and the servo function could compensate for each other.

The essential concepts regarding the bandwidth are depicted in the following lines:

- The amplifier's bandwidth is the servo function bandwidth, which is determined by the loop gain - poles product.
- It is possible that undesired pole splitting across the Miller capacitance of a stage is causing a dominant pole to become non-dominant, making the bandwidth decrease. If this is the case, a cascode needs to be added.
- If the bandwidth is not enough, more stages can be added to add poles into the dominant range. The maximum contribution of one stage towards the loop gain - poles product is its f_t, so the minimum number of extra stages needed can be estimated using this parameter. For example, if the BW needs to be increased 1.1 times f_t, at least two extra stages will be required.

The fundamental concepts regarding adding more stages are outlined in the following lines:

- The connection between the controller's stages should satisfy that if any of those stages is replaced by an ideal nullor, the controller becomes a nullor.
- If the stages are not connected properly, the asymptotic gain deviates from the ideal gain. In opposition to the static inaccuracy, reducing the error by increasing the loop gain is not possible. Additionally, the common-mode and power supply rejection ratios might be affected. The amplifier also becomes more susceptible to the tolerances of the devices.
- The loop gain must have a 180º phase in DC to produce negative feedback. The phase contribution of the new stages needs to be considered to prevent positive feedback.

Frequency compensation
If the location of the poles and zeros of the servo function is not satisfactory (e.g., there are positive poles that lead to instability), several techniques can be applied to reallocate them into desired positions. The objective is to do so by maintaining the performance aspects.

The strategies to do frequency compensation using SED are described at [40]. Some strategies are pointed out in the following lines.

- Phantom zero introduces a zero in the loop gain that coincides with a pole in the ideal gain. For the frequencies above the zero, the loop gain increases. It can be implemented by introducing a pole in the source-input or output-load networks or a zero in the feedback network. It is the most harmless compensation technique. To be effective, it should not introduce new dominant poles or modify the existent dominant poles such that the bandwidth is reduced.
- Pole splitting changes the interaction between poles using local negative feedback around a stage. For the frequencies between the affected poles, the loop gain is exchanged with the local loop gain. Therefore, the performance in between those frequencies becomes worse. Additionally, it creates a positive zero due to the direct transfer in the local feedback.
- Pole-zero canceling, resistive broadbanding, and bandwidth reduction are brute force techniques. Brute force techniques should be avoided unless there is a clear argument favoring one of them in a specific application.

4

Design

This chapter describes the microelectronic design of the pseudo-voltage clamp for an intracellular neural interface as those introduced in Chapter 1.

4.1. Specifications

This section introduces the model of the system and the requirements that the system must achieve.

Model of the system

The proposed system, shown in Fig. 4.1, is a trans-impedance amplifier (TIA). The TIA allows tracking the current I_e by converting it to an output voltage V_o, which can be digitized with an analog-to-digital (ADC) converter. It is also possible to fix the voltage V_e through V_{clamp} to perform a voltage clamp thanks to the negative feedback.

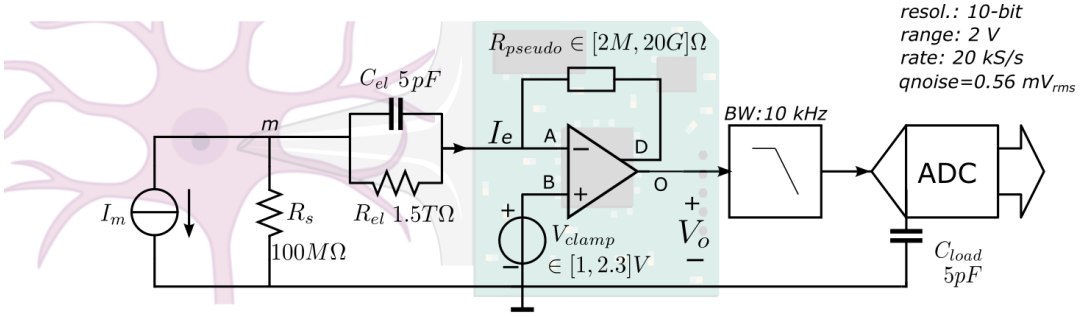


Figure 4.1: Diagram of the proposed system. I_m and R_s are the neuron membrane current and the solution resistance. C_{el} and R_{el} model the electrode. The amplifier is a TIA whose gain is set by a variable transconductance R_{pseudo} in the feedback loop. The voltage of the electrode can be clamped adjusting the voltage of node B, V_{clamp}. A passive filter prevents aliasing in the ADC, whose equivalent input capacitance is $5pF$.

The parts of the system which are designed in this project are the controller and the feedback resistor. Both are overprinted on the chip sketch.

The controller is in charge of eliminating the error signal between the terminals of the input port. Its implementation is an OpAmp whose design steps are explained in Section 4.2.

The feedback network gives the character of trans-impedance by sensing the output voltage and comparing it to the input current in parallel. Therefore, the trans-conductance value of the feedback sets the trans-impedance gain of the TIA. Ideally, this topology makes the input and output impedances to be zero. There are two main options for implementing the feedback network: making it active (e.g., a gm-cell) or passive (e.g., a pseudo-resistor). A standard resistor cannot be used because the resistance values are enormous. The design of the transconductance is explained in Section 4.3.

The neuron-electrode interface imposes the source impedance. The branch with the $R_s \approx 100\ M\Omega$ [51], known as the extracellular or solution resistance, models the losses in the neuron-electrode interface. The capacitance C_e of about $5\ pF$ [51] drives the non-Faradaic current of the electrode, and the

resistance R_e of about $1500\ G\Omega$ [51] drives the Faradaic current. On one side, the ideal representation of the non-Faradaic branch is a capacitor because it is a reversible distribution of electrochemical species [9]. On the other side, the Faradaic branch is represented with a resistor because irreversible chemical reactions cause it [9].

The load impedance is imposed by the input equivalent impedance of the ADC $C_{load} \approx 5\ pF$.

Requirements

The requirements for the system are based on the information in Chapters 1 & 2. The most relevant are the output and input voltage ranges, the trans-impedance gain, the bandwidth, and the noise. Those requirements are summarized in the Table 4.1 and explained afterward.

Table 4.1: TIA requirements summary.

Parameter	Value
Output voltage range	close to $[0, 3.3]\ V$
Input voltage range	$[1, 2.3]\ V$
Gain	$[2M, 20G]\ \Omega$
Bandwidth	$[DC, 10\ KHz]$
Noise	Around $0.56\ mV_{rms}$

If an ideal output stage is considered, the output voltage range is between the power supply $V_{dd} = 3.3\ V$ and ground $V_{gnd} = 0\ V$. The TIA should operate as close as possible to those limits.

Considering an ideal output stage again, and assuming that all the ADC range ($2\ V$) is leveraged, the most extreme clamps (input voltage) that can be applied are $1\ V$ and $2.3\ V$ because these voltages create output signals between 0 and $2\ V$, and 1.3 and $3.3\ V$, respectively. Nevertheless, more input voltage range is welcome since it is also possible to use the TIA without taking advantage of the full swing of the ADC.

The expected I_e is about $100\ pA \sim 1\ nA$ as mentioned in Section 2.3. However, some margin is positive to deal with larger or smaller attenuation since the electrode is not manufactured yet. Therefore, the TIA initially targets a range of $I_e \in \pm[0.5\ p, 0.5\ \mu]A$. In the later stages of the design, the physical limitations reduce this ideal range. The input voltage range of the ADC is $2V$, and its resolution is 10-bits (1024 levels). In most cases, the objective is to convert the input signal I_e into a V_o that takes advantage of the full range of the ADC. When the current is in the range $Ie \in \pm 0.5\ \mu A$, a gain of $2\ MV/A$ causes a $\Delta V_o = 2\ V$ (resolution of $1\ nA$). For tiny currents, the gain would become too large, so some resolution is sacrificed. For $I_e \in \pm 0.5\ pA$, a gain of $20\ GV/A$ causes a ΔV_o of $0.02\ V$ (resolution of $0.1\ pA$). In conclusion, the transconductance of the feedback network needs to have a variable value $R_{pseudo} \in [2\ M, 20\ G]\Omega$. This variable resistance cannot be implemented with a standard resistor because it is too big. Either it is implemented with active circuitry, or a passive structure is used as a pseudo-resistor. The main advantage of the former is the accuracy, while the latest is more efficient in terms of power. As an initial design decision, pseudo-resistors are chosen since accuracy is not critical.

As explained in Section 2.1, the TIA needs to deal with signals from $1\ Hz$ to $10\ kHz$, with priority on signals around 1kHz (the action potentials). The source impedance has high-pass properties, which already limit the lower frequencies. Therefore, the TIA can be designed with $BW : DC - 10\ kHz$.

The noise needs to be as low as possible. As there is not a precise specification, the quantization noise of the ADC can be taken as a reference. For an ADC of $10 - bit$ resolution and $2\ V$ range, the estimated quantization noise is around $0.56\ mV_{rms}$. The amplifier should have a similar output-referred noise level.

4.2. Controller

This Section explains the design process of the controller of the TIA, from the process modeling to the pre-layout simulations with an ideal resistor as a feedback network. The design steps order and methodology are explained in Chapter 3.

4.2.1. EPFL-EKV modelling of the process

The starting point to design the controller is to model the process because a bad matching between the EKV model and the process would make any design decision insignificant. In this project, some

parameters of the simplified EKV model in SLiCAP are updated while others remain with a default CMOS18 value.

Default model
As explained in Section 3.1, SLiCAP models the transistors using θ, E_{crit}, V_{AL},C_{GS},C_{GD},C_{GB},K_F,and A_F. The total capacitances are obtained considering only the extrinsic capacitances given by the aspect ratio and the capacitances per area unit C_{GBO},C_{GSO},C_{JB0}, and the oxide thickness T_{OX}.

All the parameters that have been mentioned have a standard value in CMOS18 given by Binkley [10], which are the default values used in SLiCAP. These values are declared in `-SLiCAP_installation_path-/SLiCAP/lib/SLiCAPmodels` [41]. However, to obtain meaningful results in the symbolic analysis the model needs to match the real characteristics of the process.

In this subsection the process to obtain V_{th},θ, E_{crit}, and n_0 is explained. In those cases, the calculation is based on graph matching between Cadence and SLiCAP results using a simple test-bench (Fig.4.2). The value of T_{OX} can be obtained directly from the process datasheets. On the other hand, V_{AL}, C_{GBO}, C_{GSO}, C_{JB0}, K_F, and A_F default values were initially used. The results of the simulations in later design steps verify that using the default parameters for the capacitances and V_{AL} is valid. However, the noise parameters had to be adjusted to represent the process truthfully.

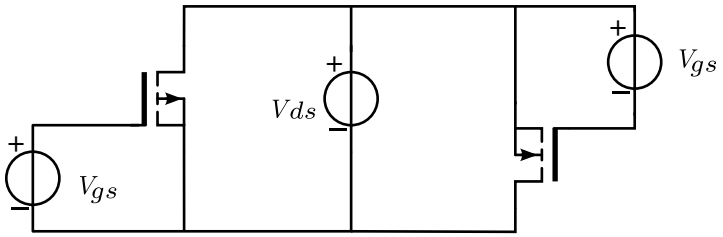


Figure 4.2: Schematic of the testbench that can be used to determine the simplified EKV paramters of NMOS and PMOS transistors.

Calculation of n_0 and V_{th}
The subthreshold factor and the threshold voltage can be calculated using the expression of the drain current in weak inversion (Eq.3.1). Applying a logarithm to both sides of the equation [10]:

$$\log I_D(WI) \approx \frac{V_{GS}}{n_0 V_T}\log e + \log I_0 \frac{W}{L}\exp(\frac{-V_{th}}{n_0 V_T}) \tag{4.1}$$

From Eq.4.1 it can be seen that a graph $\log I_D$ vs V_{GS} has a slope $n_0 V_T / \log e$ and an y-axis intercept at $log I_0 \frac{W}{L}\exp(\frac{-V_{th}}{nV_T})$. Since the thermal voltage, V_T, is known, n_0 can be calculated from the slope of the graph for small V_{GS}. Once n_0 is estimated, the only unknown variable in the y-intercept expression is the V_{th}. Therefore, V_{th} can be obtained looking at the graph for $V_{GS} = 0$.

Calculation of μ_0
In the equation of the drain current in strong inversion (Eq.3.6, repeated for clarity at 4.2), the only parameter that is still unknown is the μ_0. Its value can be estimated by comparing the graph I_D vs. V_{GS} from Cadence with other graphs with different values of μ_0 from SLiCAP, as long as the test-bench and control variables are the same.

$$I_D(SI, \text{no effects}) = \frac{1}{2}\frac{\mu C_{OX}}{n}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{4.2}$$

Calculation of θ and E_{crit}
Using small sized transistors in the test-bench and operating in strong inversion it is possible to characterize θ and E_{crit}. The equations to use in this case are Eqs.3.19 & 3.20 (repeated at 4.3). If g_m is plotted versus I_D, the degradation of the transconductance at large currents is caused by θ and E_{crit}.

$$g_m = \frac{I_D}{nU_T(\sqrt{IC + 0.5\sqrt{IC}} + 1)}, IC = IC(1 + \frac{IC}{IC_{crit}}), IC_{crit} = (\frac{LE_{crit}}{4n_0 U_T(\theta + \frac{1}{LE_{crit}})})^2 \tag{4.3}$$

Differently from the other variables, θ, and E_{crit} cannot be estimated independently because there are two unknown variables at the same time. However, the VS depends on V_{DS}, while VFMR does not. Therefore, it is possible to use the test-bench with two different V_{DS} and then adjust θ and E_{crit} several times until they converge. The adjustment is also made by comparing graphs from Cadence and SLiCAP until they match.

The script used to match the EKV model is explained in Annex A.1. Alternative parameter extraction algorithms are presented in [20] and [27].

Verifying the updated model

Fig.4.3 shows a comparison between using default parameters and those obtained in the latest paragraphs, which clearly shows an improvement. The adjustment process is repeated for the PMOS transistors.

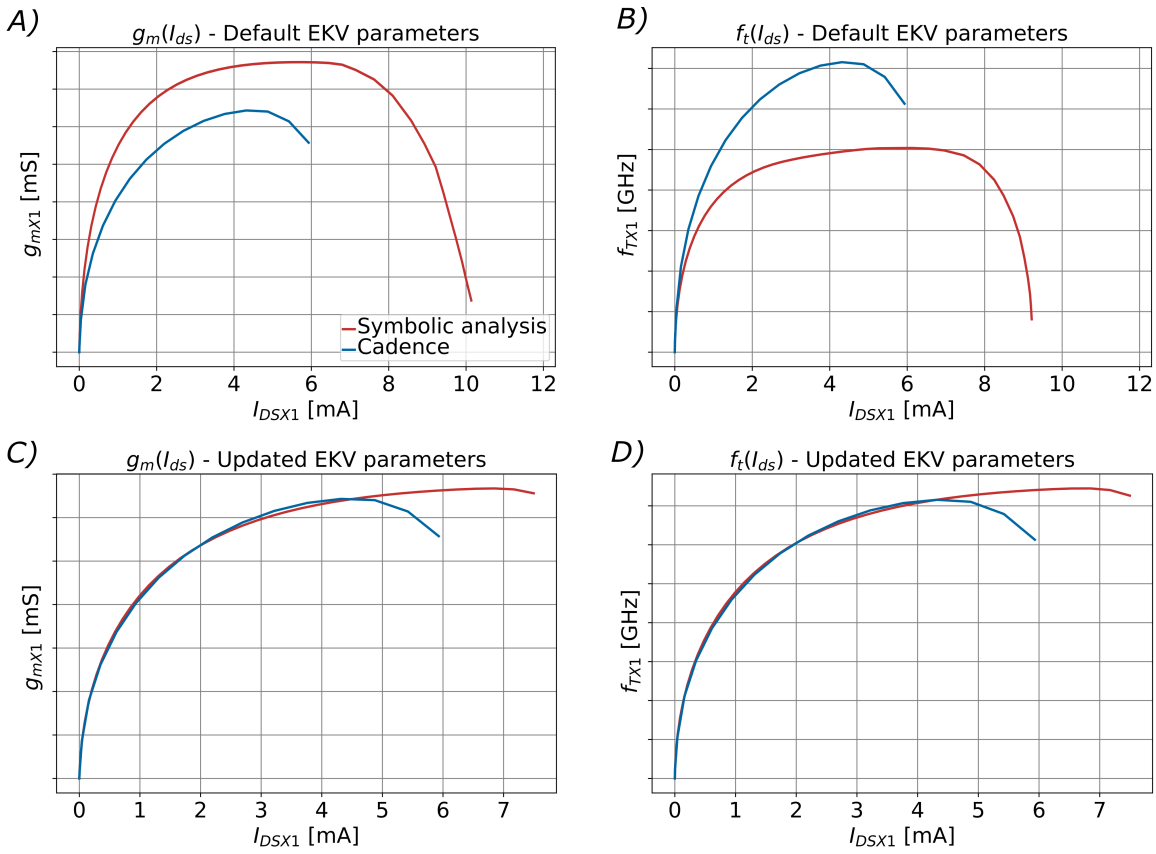


Figure 4.3: The graphs A) and B) represent the g_m and the graphs C) and D) show the f_t of the transistor, both versus its drain current. Please, note that process-related results are confidential, so some information such as the control variables and y-axis labels are hidden or slightly distorted. The red trace in all graphs is obtained with the simplified EKV model. In A) and C), the parameters of the EKV model are the default for CMOS18. In B) and D), the parameters are the ones obtained in this Section. The red traces in B) and D) match the Cadence simulation, which means that the five parameters that were adjusted and also the default capacitances are valid for $I_D < 5\ mA$.

4.2.2. Noise feasibility and optimization

The first parameter that is designed in SED is the noise, as stated in Section 3.2. It is possible to determine the feasibility of the noise requirements, optimize the noise performance, and analyze the estimated noise power spectrum density in more detail using a noise model and its symbolic equations.

Noise model

As it was explained in Section 3.2, the noise of an amplifier is given mainly by its input stage. Besides, this stage can be considered initially as a CS stage, so the noise source transformation in Fig.3.5

applies. Lastly, in trans-impedance amplifiers, the noise contribution of the feedback is equivalent to the feedback being in parallel to the source impedance.

Considering all those aspects, a model that could define the noise of the controller is proposed in Fig. 4.4. In this model, the feedback network noise equivalent (in grey) is only included to verify whether the feedback and controller contributions are in the same order of magnitude or if one dominates. The source noise is not included since its optimization is out of the scope of this thesis. The gate noise is assumed to be zero, as mentioned in Section 3.1.

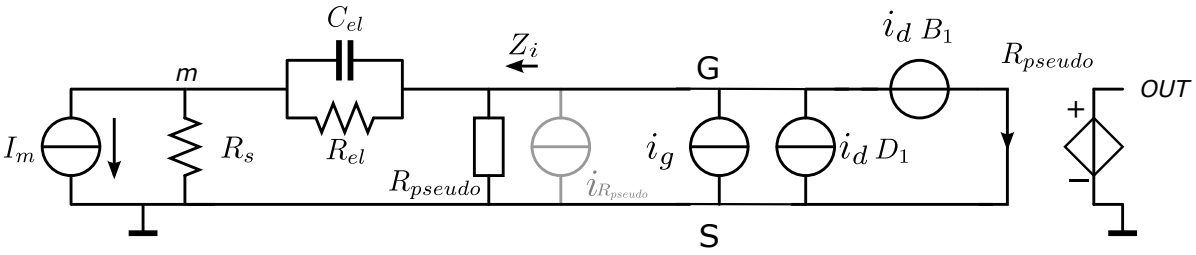


Figure 4.4: Diagram of the noise model of the system. The source impedances are the same as in Fig. 4.1. The feedback impedance R_{pseudo} is placed in parallel to the source since the feedback comparison of a trans-impedance amplifier is in parallel. Its noise contribution, in gray, is not considered when calculating the controller noise exclusively. The noise power density sources of the controller are the same as in Fig. 3.5. The noise of the source impedance is not considered in this project. The input-referred noise is detected as current between G and S. The output referred noise is detected as a voltage at node OUT.

Noise optimization: size and drain current

As established in Section 4.1, the noise should be around $0.56\ mV_{rms}$ to be in the same order of magnitude of the quantization noise in the ADC. Therefore, it is interesting to study if the output referred RMS noise of the amplifier can meet the spec and the sizing and bias conditions of the controller that ensure the lowest noise contribution.

An Eq. 4.4 that models the noise of the controller can be obtained from from Fig. 4.4. The noise tagged as $i_d B_1$ can be transformed into a current noise power density source through Z_i. The result of that transformation can be combined with the noise source $i_d D_1$ summing in voltage (they are correlated sources, both come from i_d). B_1, D_1 and S_{i_d} were defined in Eqs. 3.31, 3.32, and 3.27, respectively. The final equivalent noise depends on the constants A_F, K_F, n_0, which have been set already (Section 4.2.1), the temperature -37ºC-, and the Boltzmann constant k. It also depends on Z_i which is the parallel of the source and the feedback impedances, whose values are known (Section 4.1). Lastly, it depends on Γ, g_m, and C_{gs}.

$$S_{i,eq} \approx |D_1 + \frac{B}{Z_i}|^2 S_{i_d} = (|\frac{-j\omega C_{gs}}{g_m} + \frac{-1}{g_m Z_i}|^2 4kTn\Gamma g_m)(1 + (\frac{3K_F g_m}{8kTn\Gamma C_{gs} f})^{A_F}) \tag{4.4}$$

The analysis of the equation can continue. C_{gs} depends exclusively on the size of the transistor as it was defined in Eq.3.26. Γ depends just on the IC (Eq.3.28). g_m depends on the constants n_0 and U_T, the IC, and the drain current I_D (Eq.3.20). Finally, the IC depends on I_D, the size of the transistor and the constant I_0 (Eq.3.18).

In conclusion, Eq. 4.4 can be defined with known constants and the parameters I_D, W, and L. Since Z_i depends on the feedback network, the $gain = R_{pseudo}$ is also a variable. The final expression is complex and hard to integrate. However, using SLiCAP, it is possible not only to do so but also to create the noise equation directly from the model in Fig. 4.4.

Fig. 4.5 shows the output referred RMS noise versus W and I_D for $L = 2\ \mu m$, and three different gains: the minimum ($2MV/A$), an intermediate ($200\ MV/A$), and the maximum ($20\ GV/A$). The integration range is from $0.1\ mHz \approx DC$ to $10\ kHz$, and the input stage is considered as NMOS. A current-controlled voltage source is used to refer the noise to the output, limiting the validity of the results to the amplifier's bandwidth. The script that generates these 3-D graphs is available in Annex A.2.

From the graph, it is clear that W has a massive impact on the noise performance of the controller. However, this impact is limited to the case in which the W is too small. Once W is large enough, making it larger does not change much the total noise. If the optimization focuses on the worst-case scenario (largest gain), there is even a counter-effect: the larger the W, the larger the noise. Although this effect

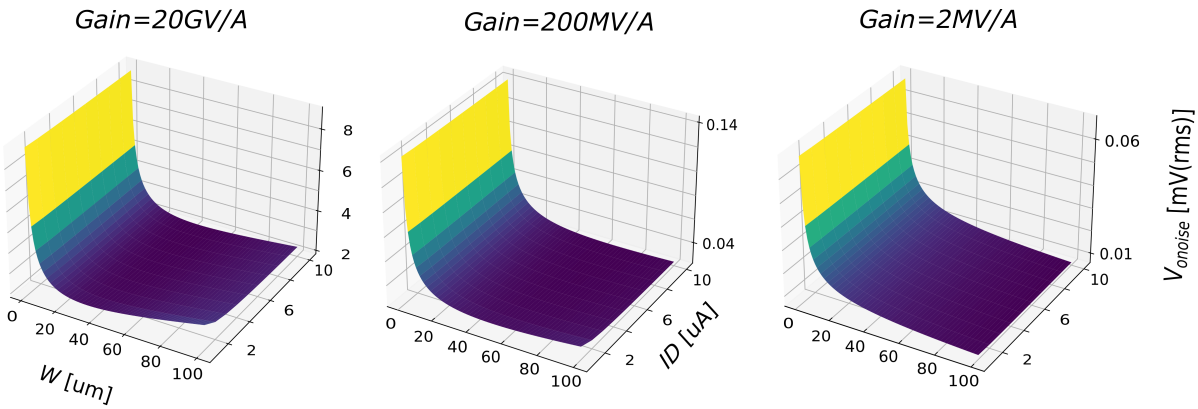


Figure 4.5: Output referred RMS noise of the controller versus the width W and drain current (ID) of the transistor ($L = 2\ \mu m$). The controller is assumed to be a single transistor common-source stage. The noise spectrum is integrated from $\sim DC$ to $10\ kHz$. For all gains if $W < 20\ \mu m$ the noise increases dramatically. The influence of ID is much slighter.

is not severe, it is clear that there is an optimum W_{opt} where noise is at its lowest or close to the lowest, while the area usage is kept reasonable. In other words, it is possible to design the first stage so that the noise is optimum but without wasting area.

The script can run several times with different L. In all those cases, it is possible to estimate a W_{opt}. All the combinations with $L \in [350\ nm, 5\ \mu m]$ show similar performance in terms of area and noise, so the pair $W_{opt} = 30\ \mu m, L = 2\ \mu m$ is selected as a good option for layout regarding aspect ratio.

The script can be also run for a PMOS noise equivalent. Traditionally, it has been considered that PMOS has a lower flicker (pink) noise but higher thermal (white) noise. However, in [10] it is pointed out that the actual noise needs to be checked, which can be quickly done in this case. The result is that the PMOS input stage has an equivalent RMS noise compared to an NMOS input stage. This statement is further discussed in Chapter 6.

Once W_{opt} and L are set, the only variable that is yet to fix is I_D. Fig.4.6 shows the output referred RMS noise versus I_D for $L = 2\ \mu m$, and $20\ GV/A$. The graph for other gains has the same shape, but the noise is scaled down. In all cases, $I_{opt} = 2\ \mu m$.

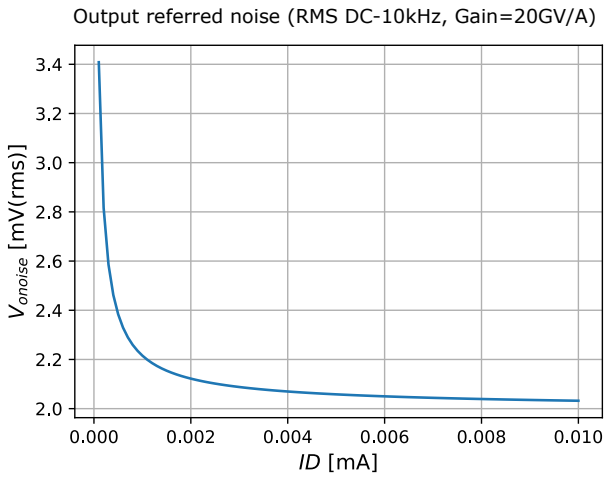


Figure 4.6: Output referred RMS noise of the controller versus the drain current (ID) of the transistor ($W = 20\ \mu m$, $L = 2\ \mu m$, $gain = 20\ GV/A$). The controller is assumed to be a single transistor common-source stage. The noise spectrum is integrated from $\sim DC$ to $10\ kHz$. For $ID < 2\ mA$ the noise increases exponentially.

Final noise estimations and analysis of noise spectrum shape

With $W = 30\ \mu m$, $L = 2\ \mu m$, and $ID = 2\ \mu A$, the estimated output referred RMS noise contribution of the controller versus the gain of the amplifier is plotted in Fig.4.7. If the noise spec strictly requires that the amplifier's noise is below $0.56\ mV_{rms}$, it would not be possible to operate with gains over $5\ GV/A$.

This limitation is because no matter what the rest of the amplifier looks like, the total noise would always be higher than the first stage's contribution. However, in this case, the spec is not strict: the amplifier's noise can be larger than the quantization noise of the ADC, although this is not desired.

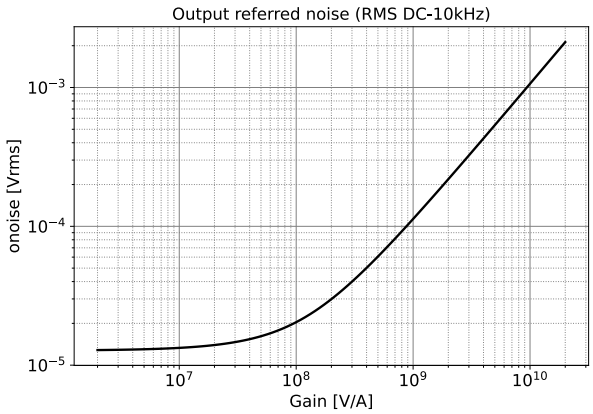


Figure 4.7: Final estimation of the controller's output referred RMS noise versus the TIA gain ($W = 20\ \mu u$, $L = 2\ \mu m$, $ID = 2\ \mu A$). The controller is assumed to be a single transistor common-source stage. The noise spectrum is integrated from $\sim DC$ to $10\ kHz$.

The contribution of the feedback network to the total output referred RMS noise is estimated using the gray source in Fig.4.4 ($i_{Rpseudo} = 4kT/R_{pseudo}$). Its contribution is in the same order of magnitude as the one from the controller. The total output RMS noise of the amplifier is expected to be $x2$ times the controller noise for the smallest and largest gains, up to $x5$ times for intermediate gains.

The output referred noise spectrum for the three reference gains is shown in Fig.4.8 (left). The contributions of each kind of noise (white, pink, and blue) are analyzed to understand better what determines the shape. Each contribution is shown in Fig.4.8 (right).

Blue noise comes from the current noise density source $i_d D_1 = i_d \frac{-s}{\omega_t}$. It is a current in the input, so it is transferred to the output scaled proportionally to the gain. That explains that the y-axis range of its spectrum is 10^{-24} to 10^{-17} for $gain = 2MV/A$, while it is 10^{-16} to 10^{-9} for $gain = 20\ GV/A$.

White noise comes from the thermal contribution of the voltage noise density source $i_d B_1$. As it is in the form of voltage in the input, it is first converted into current by the equivalent impedance Z_i, and later that current is transferred to the output scaled proportionally to the gain.

Pink noise comes from the flicker contribution of both $i_d B_1$ and $i_d D_1$. Therefore, part is directly transferred to the output, and the rest is first translated into current by Z_i.

As explained before, Z_i is the parallel connection of the source impedance $Z_e + R_s$ and the feedback impedance $R_{pseudo} = gain$. The larger the gain, the strongest the influence of the electrode in the shape of the spectrum because the source impedance path becomes dominant. Any noise contribution graph can be divided into three sections: 1) from $f = -\infty$ to f_x where the feedback impedance R_{pseudo} path dominates, 2) from $f = f_x$ to around $f = 300Hz$ where the electrode impedance path dominates and has a capacitive response, and 3) from $f = max(300Hz, f_x)$, where the electrode impedance path dominates and has a resistive response. In sections 1 and 3, the shape of the noise is such of its color, while in section 2, the slope of the capacitive effect is added. When the gain is small, f_x becomes larger and can make sections 2 and 3 disappear. This effect is why for $gain = 2MV/A$, the pink and white noises remain unaffected by the capacitive effect, while for $gain = 20\ GV/A$, there are large variations.

The blue noise coming from $i_d D_1$ is sometimes called "induced gate noise" and is usually neglected because its effect is expected only at very high frequencies. Thanks to the previous analysis, it can be seen that for this particular amplifier, this kind of noise is relevant for frequencies above just $1\ kHz$ when the amplifier gain is close to $20\ GV/A$.

Adapting size and bias current for a balanced stage

It is helpful to have a balanced input stage such as a differential pair to apply the clamp voltage. As mentioned in Section 3.2, it is necessary to double the width and the drain current of the transistors to achieve the same noise performance as the non-balanced stage. Since that means using two transistors, this is equivalent to use four times the area and power. In conclusion, the optimum noise of the amplifier with a balanced input stage is met when $W = 60\ \mu m$, $L = 2\ \mu m$, and $I_D = 4\ \mu A$.

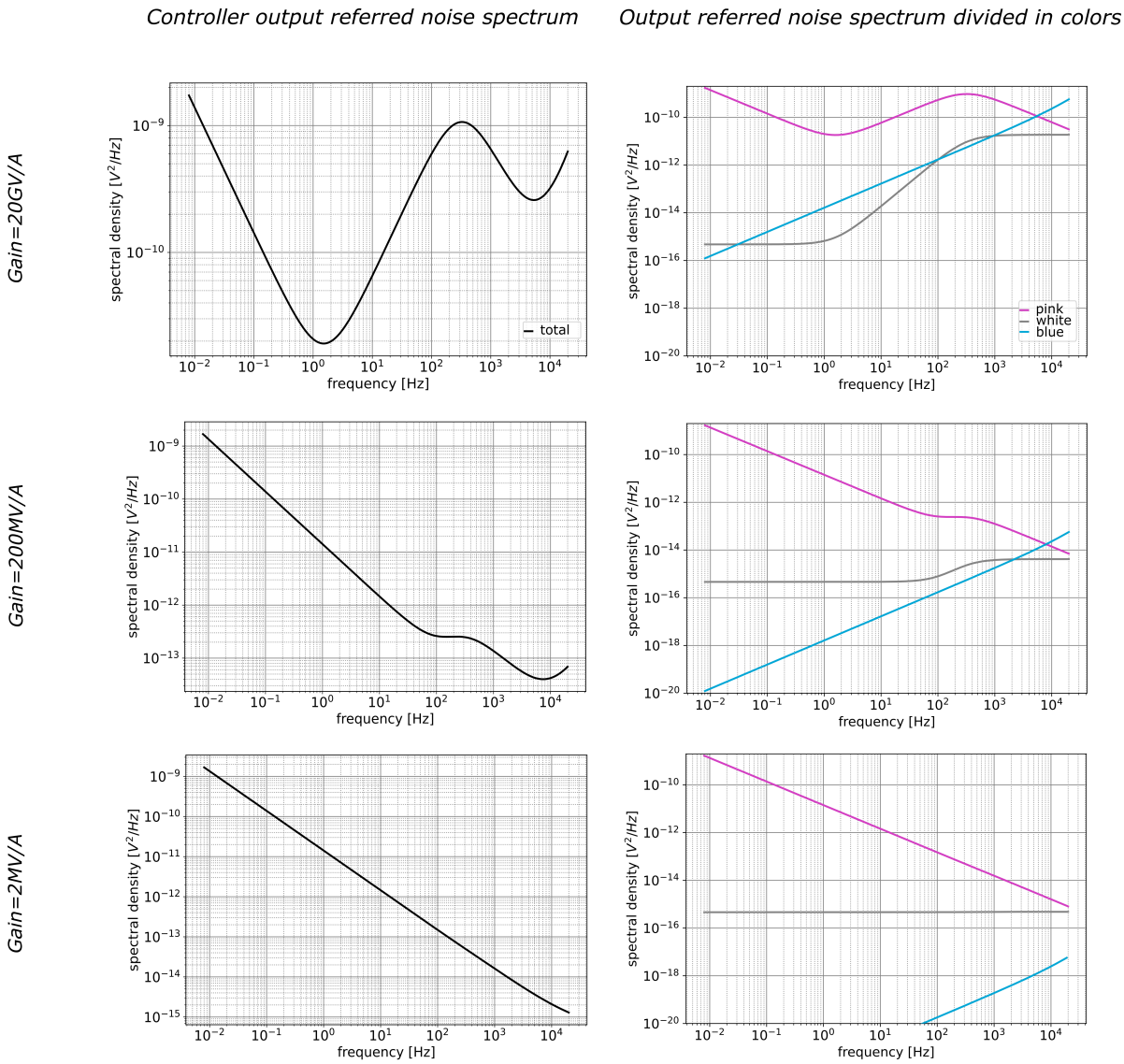


Figure 4.8: The graphs in the left column show the final estimation of the controller's output referred noise spectrum for the maximum, intermediate, and minimum gains. Their shape is different because some noise contributors dominate over others, and their transfers are modified for each case. The graphs in the right show the same output referred spectrums as in the left, but they are decomposed in colors (pink for the flicker, white for the thermal, and blue for the induced gate noise). In all cases, $W = 20\ \mu m$, $L = 2\ \mu m$, $ID = 2\ \mu A$, and the controller is assumed to be a single transistor common-source stage.

4.2.3. Driving capabilities

As it was explained in Section 3.2, the driving capabilities of an amplifier are given mainly by its output stage. Therefore, the driving capabilities impose the values of the biasing and sizing of the output stage. A single-stage amplifier could be considered if those values are compatible with the requirements of the input stage.

Biasing requirements

The relevant specs from Section 4.1 that need to be considered to design the ouput driving are the power supply $V_{dd} = 3.3V$, the maximum frequency $f_{max} = 10\ kHz$, the range of the ADC $\Delta V_{ADC} = 2V$, the ADC input capacitance (load) $C_{load} = 5pF$, and the feedback resistance (gain) $R_{pseudo} \in [2M, 20G]V/A$.

The transistor is a passive element that needs biasing to become "active." This biasing makes the transistor operate at a specific operating point, which must be sufficient to drive the load and the feedback. Fig.4.9 [40] shows an unbiased transistor with the four sources that are needed to bias it.

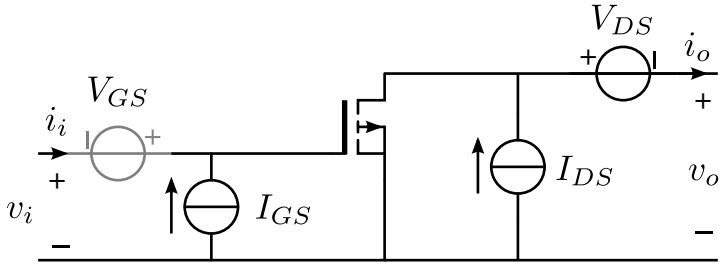


Figure 4.9: Schematic of an unbiased transistor with the four sources that defines its biasing. I_{GS} can be approximated to zero.

I_{DS} must ensure that the slew rate is enough to charge the load at $10\ kHz$ fully. Assuming a sinusoidal signal that means that

$$I_{DS} > 5\ pF \frac{2\ V}{2} 2\pi 10\ kHz = 0.314\ \mu A$$

Additionally, the biasing also needs to provide the current across the feedback, which is equivalent to be in parallel with the load, as explained in Section 3.2. In the worst-case scenario, that current is $0.5\ \mu A$.

In conclusion, I_{DS} needs to be larger than $0.814\ \mu A$ to drive the load and the feedback. However, some margin is given to deal with more steep signals than sines, as action potentials are. I_{DS} is set to $5\ \mu A$.

Sizing requirements

The sizing of the output transistor must ensure that it can handle the current from the load, the feedback network, and its own bias. In the worst-case scenario, that means that it needs to be capable of driving $5\ \mu A + 0.314\ \mu A + 0.5\ \mu A \approx 6\ \mu A$. A test bench for an NMOS output stage, as shown in Fig.4.10, can be used to verify the size of the transistor.

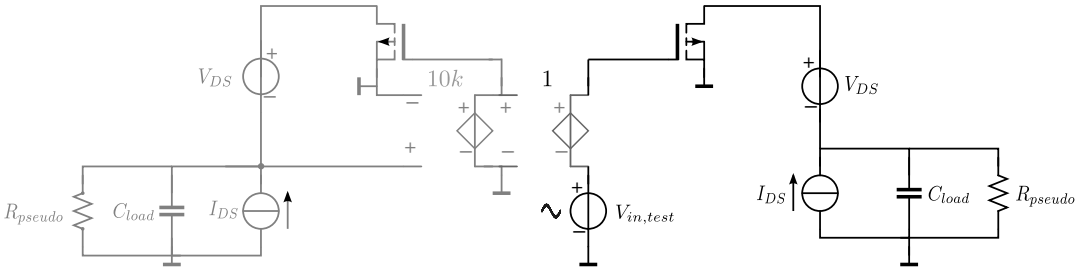


Figure 4.10: Schematic of the test-bench used to study the driving capabilities of a transistor. The circuit in gray is a model-based implementation of the V_{GS} source in Fig.4.9. The equivalent load is C_{load} in parallel to the feedback impedance R_{pseudo} because the sensing in a trans-impedance amplifier is in parallel. The biasing needs to be enough to drive the equivalent load. The transistor needs to sink currents from the biasing and the equivalent load. $V_{in,test}$ is a sinusoidal test signal.

Fig. 4.11 shows the results of the simulation for $W = L = 350nm$, and $V_{DS} = 1V$ with an NMOS device. As expected, the absolute slopes of V_{out} are clearly over the minimum slew rate for a $2V_{p-p}$ $10\ kHz$ sine ($20\pi\ kV/s$) thanks to the over-design of I_{DS}. The load capacitance discharge through the transistor is even quicker than the loading because the transistor can handle large currents: $W = L = 350nm$ is enough for NMOS and PMOS, without the need of adding margins. Once the capacitor is discharged, the output voltage remains constant as I_{DS} is sunk by the transistor.

Evaluation of a one-stage amplifier based on noise and driving requirements

As mentioned in Section 3.2, the option to design a one-stage amplifier could be considered if the noise and driving specifications are compatible. On the one hand, as obtained in the previous paragraphs, the size of the transistor can be $W = L = 350\ nm$ and $I_D > 5\ \mu A$ to ensure enough driving capabilities. On the other hand, in section 4.2.2, it has been explained that $W = 60\ \mu m$, $L = 2\ \mu m$, and $I_D > 4\ \mu A$ for optimum noise performance. Therefore, it would be possible to meet both noise and driving specs with a single-stage with $W = 60\ \mu m$, $L = 2\ \mu m$, and $I_D = 5\ \mu A$.

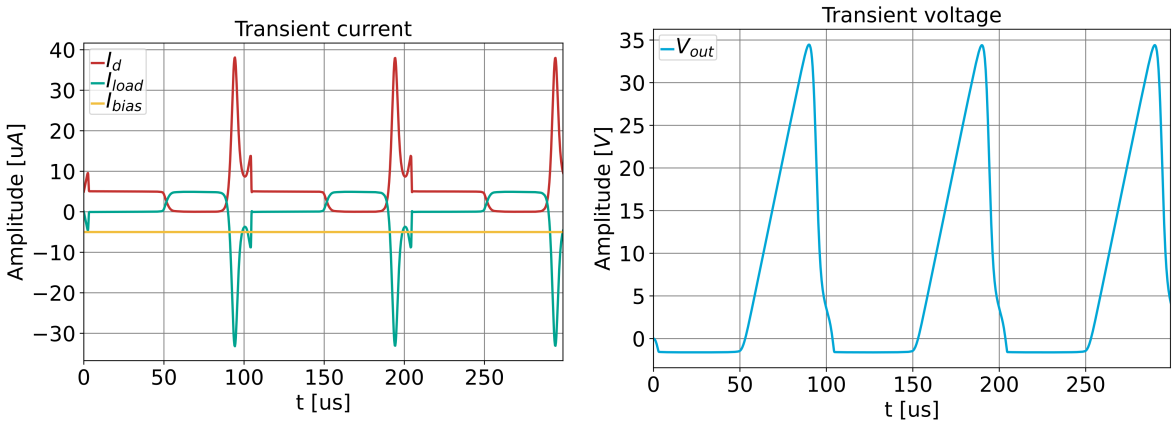


Figure 4.11: Simulation results of the test-bench in Fig. 4.10 when $V_{in,test} = 0.75sin(2\pi 10\ kHz \cdot t)$, $W = L = 350\ nm$, $C_{load} = 5\ pF$, $R_{pseudo} = 200\ M\Omega$, $I_{DS} = 5\ \mu A$, and $V_{DS} = 1.65\ V$. When the load is charging (e.g. from $50\ \mu s$ to $100\ \mu s$) the bias current drives the load with $5\ \mu A$. When the load is discharging, the transistor sinks the current from the biasing and the load. The output voltage slope is enough to ensure there is no slew rate in the load of the TIA.

4.2.4. Accuracy and bandwidth

In this Section, the controller is designed such that it satisfies the accuracy and bandwidth requirements. As mentioned in Section 4.1 the required bandwidth is $10\ kHz$. Regarding the accuracy, there is no spec. Firstly, the recorded signals' nature does not require much accuracy. Secondly, the accuracy performance is mainly limited in the ideal gain by pseudo-resistor. The calculations of the transfers rely on the AGM, as explained in Section 3.2.

One stage design: balanced common-source

As explained in the previous paragraphs, the starting point is the single-stage that satisfies the noise and driving requirements. This single-stage amplifier is shown in Fig.4.12. The reason to choose a common source stage is twofold. Firstly, as said in Section 3.2 CD and CG stages are a CS with local feedback, which would contribute to noise. Therefore, the CS stage is the best in terms of noise. Secondly, the CS stage is the closest to a nullor with a transmission matrix (0,0;0,0), making the whole amplifier closer to ideal. For example, thanks to the nullor-like properties, the noise contribution of the second stage does not contribute much.

The loop gain of the single-stage amplifier (Fig.4.13) can be calculated with the SLiCAP script in Annex A.3. From this loop gain, it can be seen that the bandwidth for $gain = 20\ GV/A$ is below $10\ kHz$. A second stage can be added to ensure that the bandwidth is over $10\ kHz$.

One characteristic of the script that might be surprising is that the C_{gd} of the transistors have been set to zero. The reason is twofold and has been mentioned in Section 3.2. On the one hand, eliminating the capacitance guarantees no local loop around the loop gain reference of the asymptotic model, which would corrupt the loop gain measurement. On the other side, this capacitance would cause pole splitting. Pole splitting might push a dominant pole out of the dominant frequencies, making the bandwidth decrease. In that case, the most likely design decision would be adding stages, while the appropriate solution would be adding a cascode instead. Suppose there is proof of severe pole splitting in the stage with canceled C_{gd} (e.g., the pole splitting is visible in the loop gain simulated with Cadence). In that case, the solution is to add a cascode to the stage, and all previous design decisions remain valid.

The script provides the loop gain Bode, its poles and zeros, and all relevant EKV parameters such as output impedance or capacitances. Tracking the poles and zeros from an early design stage allows exciting insights into the design in later stages, for example, in the frequency compensation or the analysis of the influence of parasitics. Table 4.2 shows a summary of the poles and zeros. The quick estimations are obtained based on the small-signal diagram in Fig. 4.14.

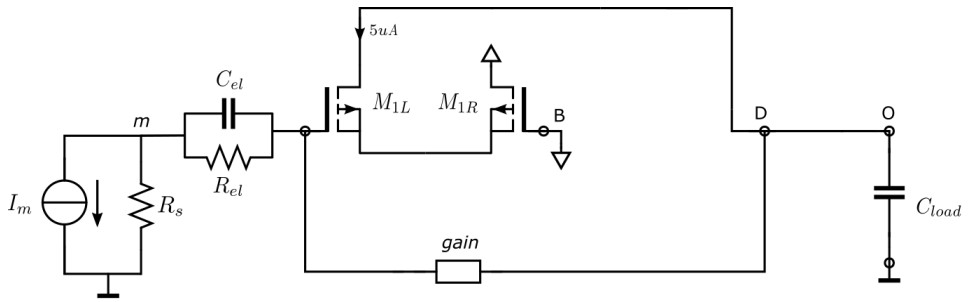


Figure 4.12: Schematic of the TIA with a single-stage controller. The stage is a balanced common-source ($M_{1,L\&R}$).

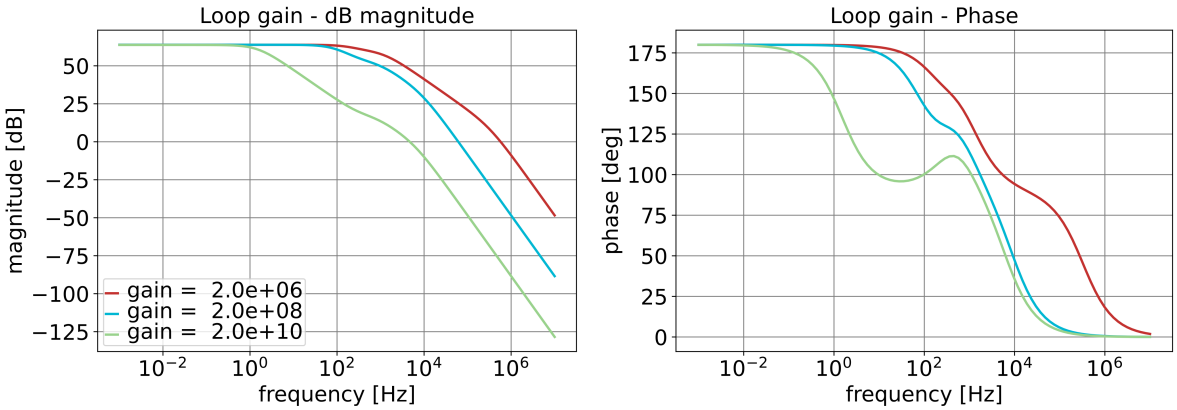


Figure 4.13: Loop gain of a TIA with a single-stage controller. The bandiwdth for large gains is below $10\ kHz$.

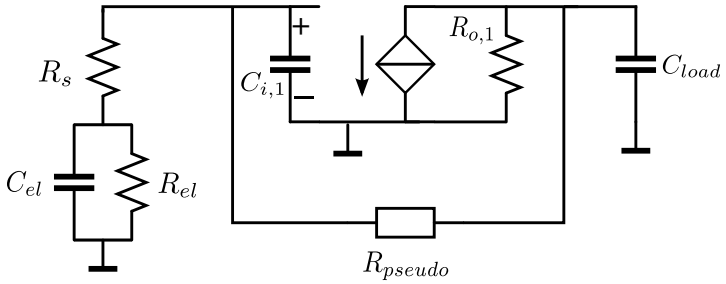


Figure 4.14: Small signal diagram of the TIA with a single-stage controller (Fig.4.12). This diagram is used to obtain the equations for the hand calculation of the poles and zeros of the loop gain (Table 4.2).

Table 4.2: Loop gain pole-zero tracking of the TIA with a single-stage controller. The status indicates whether the pole/zero is new, modified, or unmodified in respect to the previous design step. The hand calculation provides a quick and intuitive explanation for each pole/zero. The SLiCAP column indicates the frequency of the pole/zero according to the AGM for $gain = [20\ G, 200\ M, 2\ M]\Omega$.

Pole/zero	**Status**	**Hand calculation**	**SLiCAP**
Out pole (p_1)	New	$\frac{-1}{2\pi R_{o,1} C_{load}} = \frac{-1}{2\pi \cdot 32M \cdot 5p} = -1\ kHz$	$-[995, 1106, 1334]\ Hz$
Source pole (p_2)	New	$\frac{-1}{2\pi(R_s + R_{pseudo})C_{el}} = \frac{-1}{2\pi \cdot [102M, 20.1G] \cdot 5p} = -[1.58, 312]\ Hz$	$-[1.5, 92, 221]\ Hz$
Input pole (p_3)	New	$\frac{-1}{2\pi(R_s \| R_{pseudo})C_{i,1}} = \frac{-1}{2\pi \cdot [2,100]M \cdot 260f} = -[6, 300]\ kHz$	$-[6457, 9436, 327k]\ Hz$
Source zero (z_1)	New	$\frac{-1}{2\pi R_s C_{el}} = \frac{-1}{2\pi \cdot 100M \cdot 5p} = -318\ Hz$	$-318\ Hz$

Two stage design: balanced common-source + common source

The second stage is again a common-source. As said before, the CS stage is the closest to a nullor, making the whole amplifier closer to an ideal. As long as there is not a specific drawback using this stage, it is preferred.

The sizing strategy of the second stage is to use a moderate or weak IC (smaller L and larger W for constant I_D) so that the $V_{sat,M4}$ is small following Eq. 3.22. A small $V_{sat,M4}$ provides a large maximum output voltage as given in Eq. 4.5, which is a requirement stated in Section 4.1. Fig. 4.16 helps to visualize this. With $W_{M4} = 5\ \mu m$, $L_{M4} = 350nm$, and $I_{D,M4} = 5\ \mu A$, the bandwidth is well over $10\ kHz$, and the maximum output voltage is estimated at $3.13\ V$.

$$V_{max,out} = V_{dd} - V_{sat,M4} \tag{4.5}$$

The loop gain of the two-stage amplifier (Fig.4.17) can be calculated again with the SLiCAP script in Annex A.3. The new stage modifies the output pole p_1. Now, this pole is determined by the output resistance of the second stage rather than the first. A new intermediate pole p_4 is introduced by the input capacitance of the second stage. Lastly, a positive zero z_5 comes in due to the direct transfer through the Miller capacitance of the second stage. Table 4.3 shows a summary of the poles and zeros. The quick estimations are obtained based on the small-signal diagram in Fig. 4.18.

The servo function of the dual-stage contains positive poles, which means instability. This issue can also be seen looking at the phase margin in Fig.4.17, which has become negative. Therefore, the amplifier needs frequency compensation.

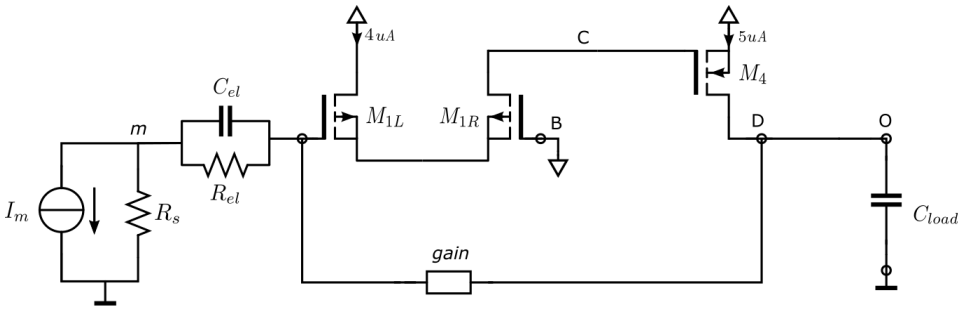


Figure 4.15: Schematic of the TIA with a dual-stage controller. The input stage ($M_{1,L\&R}$) is a balanced common-source and the output stage (M_4) is an unbalanced common-source.

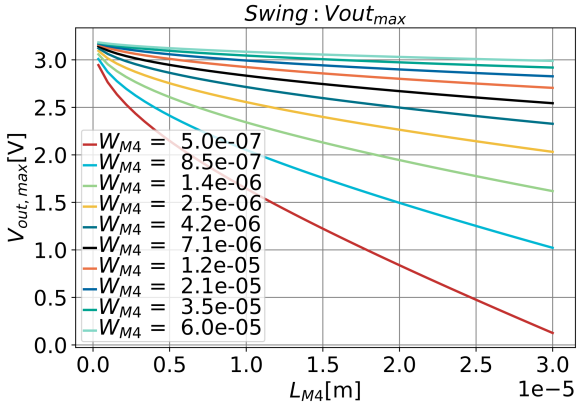


Figure 4.16: Estimation of the maximum output voltage $V_{out,max}$ of the TIA for different sizes of the output transistor M_4 with $I_D = 5\ \mu A$. The smaller the IC (smaller L and larger W for constant I_D), the larger the $V_{out,max}$. The objective is to maximize the $V_{out,max}$. $W_{M4} = 5\ \mu m$ and $L_{M4} = 350\ nm$ are selected.

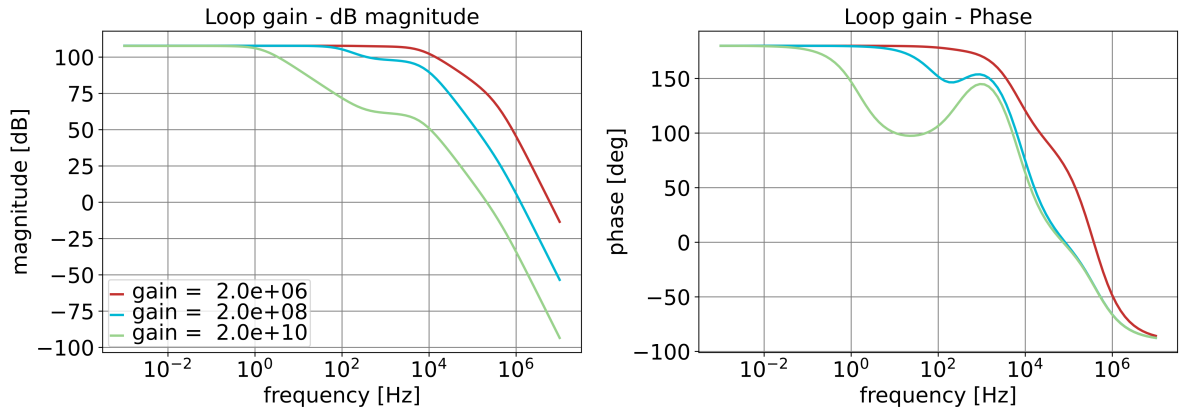


Figure 4.17: Loop gain of a TIA with a dual-stage controller. The TIA becomes unstable.

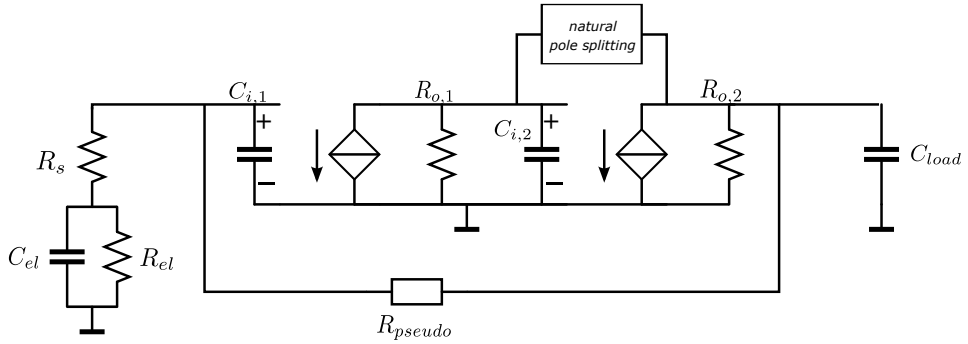


Figure 4.18: Simplified small signal diagram of the TIA with a dual-stage controller (Fig.4.15). This diagram is used to obtain the equations for the hand calculation of the poles and zeros of the loop gain (Table 4.3).

Table 4.3: Loop gain pole-zero tracking of the TIA with a dual-stage controller. The status indicates whether the pole/zero is new, modified, or unmodified in respect to the previous design step. The hand calculation provides a quick and intuitive explanation for each pole/zero. The SLiCAP column indicates the frequency of the pole/zero according to the AGM for $gain = [20\ G, 200\ M, 2\ M]\Omega$.

Pole/zero	**Status**	**Hand calculation**	**SLiCAP**
Out pole (p_1)	Modif.	$\frac{-1}{2\pi R_{o,2}C_{load}} = \frac{-1}{2\pi\cdot 2.8M\cdot 5p} = -11.4\ kHz$ + pole splitting ($\overleftrightarrow{p.s.}$)	$-[6703, 6693, 6693]\ Hz$
Source pole (p_2)	Same	$\frac{-1}{2\pi(R_s+R_{pseudo})C_{el}} = \frac{-1}{2\pi\cdot[102M,20.1G]\cdot 5p} = -[1.52, 303]\ Hz$	$-[1.5, 102, 303]\ Hz$
Input pole (p_3)	Same	$\frac{-1}{2\pi(R_s\|\|R_{pseudo})C_{i,1}} = \frac{-1}{2\pi\cdot[2,100]M\cdot 260f} = -[6, 300]\ kHz$	$-[6457, 9481, 304k]\ Hz$
Intermediate pole (p_4)	New	$\frac{-1}{2\pi R_{o,1}C_{i,2}} = \frac{-1}{2\pi\cdot 40M\cdot 10.5f} = -378\ kHz$ ($\overleftrightarrow{p.s.}$)	$-[422, 422, 445]\ kHz$
Source zero (z_1)	Same	$\frac{-1}{2\pi R_s C_{el}} = \frac{-1}{2\pi\cdot 100M\cdot 5p} = -318\ Hz$	$-318\ Hz$
P.s. direct (z_5)	New	–	$6\ GHz$

4.2.5. Design of the frequency response

The positive poles of the servo function need to be placed into the negative half-plane to ensure stability. As explained in Section 3.2, frequency compensation can be used to reallocate the poles and zeros, and the most recommended technique is the phantom zero.

Phantom zero

A priori, there are two options to implement a phantom zero in this amplifier. 1) A resistor R_{ph} between the output of the controller and the load, and 2) A capacitor C_{ph} in parallel with the feedback network. However, the latest is not feasible because the parasitic resistance of the capacitor is likely to be in the same order of magnitude as the pseudo-resistance, compromising the ideal gain.

A root locus sweeping the value of the phantom zero resistance R_{ph} confirms that a phantom zero is not enough to compensate the amplifier.

Pole splitting

Since phantom zero by itself is not sufficient to make the amplifier stable, the second-preferred strategy introduced in Section 3.2 is used instead: the pole splitting technique, sometimes known as Miller compensation.

A capacitor C_{ps} is added in between the gate and the drain of the second stage to implement the pole splitting. The pole splitting causes the output pole p_1 and intermediate pole p_4 to split away from each other, and the direct transfer positive zero z_5 to become much closer to the relevant bandwidth, around $5\ MHz$ instead of $5\ GHz$.

The sizing of the capacitor C_{ps} is such that the amplifier becomes stable but still has enough bandwidth. Besides, it is important to bear in mind that the compensation capacitor is one of the bulkiest elements of the amplifier.

The biggest challenge is to meet the stability and the bandwidth requirements for all gains between $2\ MV/A$ and $20\ GV/A$. A root locus sweeping the capacitance value reveals that for a gain of $20\ GV/A$ the minimum capacitance to ensure stability is $100\ fF$, while the maximum capacitance to ensure a bandwidth of $10\ kHz$ is $2\ pF$. On the contrary, for a gain of $2\ MV/A$, the minimum capacitance is $6\ pF$ and the maximum $850\ pF$. Therefore, the initial approach would be using two different capacitances ($C_{ps} = 2\ pF$ and $6\ pF$) to compensate the amplifier depending on its gain.

Pole splitting with series resistor and additional phantom zero

Even if the amplifier has no positive poles in the servo function, it is still on the edge of becoming unstable. A resistor R_{ps} can be included in series with the C_{ps} to improve the stability. This resistor compensates for the positive zero z_5 coming from the direct transfer through the pole splitting as long as its value is $1/g_{m,M4} = 18.8k\Omega$. If the resistor is larger than that, it can introduce a negative zero z_2 that can help improve the stability. The drawback of R_{ps} is that the loop of capacitors $C_{i,2}$, C_{ps}, and C_{load} in Fig. 4.21 is broken, so a new pole p_6 comes in into the system.

An additional method to give some more stability margin is to include the phantom zero with the resistor R_{ph} as it was discussed before. R_{ph} introduces a zero z_3 and a pole p_7. With those two methods combined, the minimum capacitance C_{ps} that is needed for large gains decreases. This relaxation allows reconsidering the use of two capacitors, which would make the compensation quite complex.

Simulating different scenarios with combinations of C_{ps}, R_{ps}, and R_{ph} reveal that $C_{ps} = 5\ pF$, $R_{ps} = 200\ \Omega$, and $R_{ph} = 4\ k\Omega$ is the best option. These values place the zeros z_2 and z_3 at the edge of the dominant frequencies range. This range varies between $10\ kHz$ and a few MHz depending on the gain of the amplifier. A drawback is that the use of $C_{ps} = 5\ pF$ limits the bandwidth for high gains. This issue will be further discussed in Chapter 6.

The compensated controller is shown in Fig. 4.19 and its loop gain is in Fig. 4.20. Table 4.4 shows the pole-zero tracking that highlights the poles and zeros that have been modified or introduced into the system due to the frequency compensation. All those results are obtained with the script in Annexes A.3 and A.4.

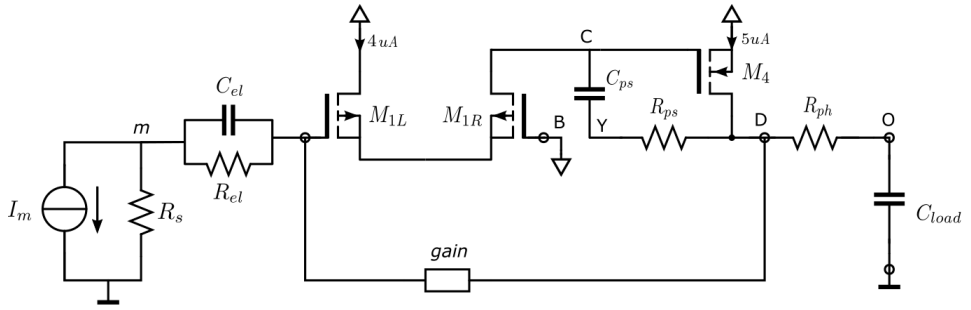


Figure 4.19: Schematic of the TIA with a dual-stage controller and frequency compensation. The input stage is a balanced common-source ($M_{1,L\&R}$) and the output stage is an unbalanced common-source (M_4). C_{ps} and R_{ps} are the pole-splitting elements around the second stage. R_{ph} is the phantom zero resistor in the output.

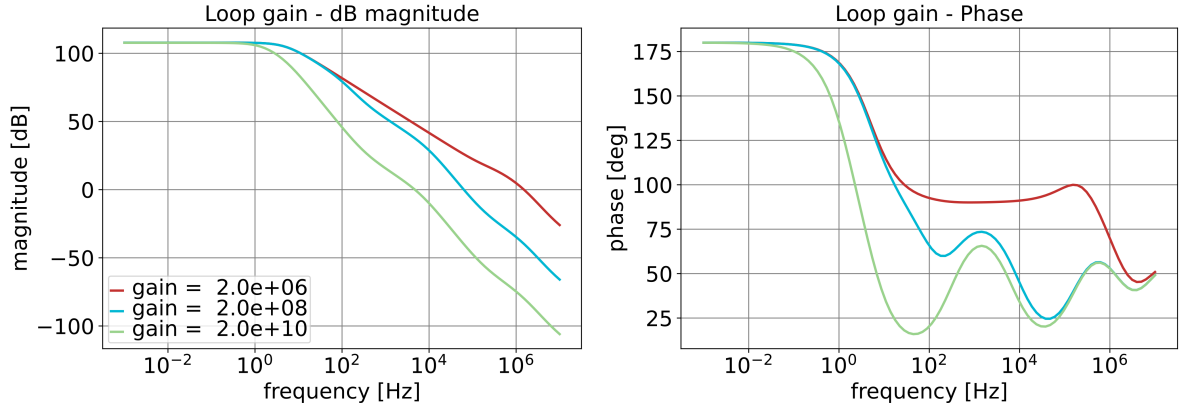


Figure 4.20: Loop gain of a TIA with a dual-stage controller after frequency compensation. The TIA becomes stable thanks to the frequency compensation.

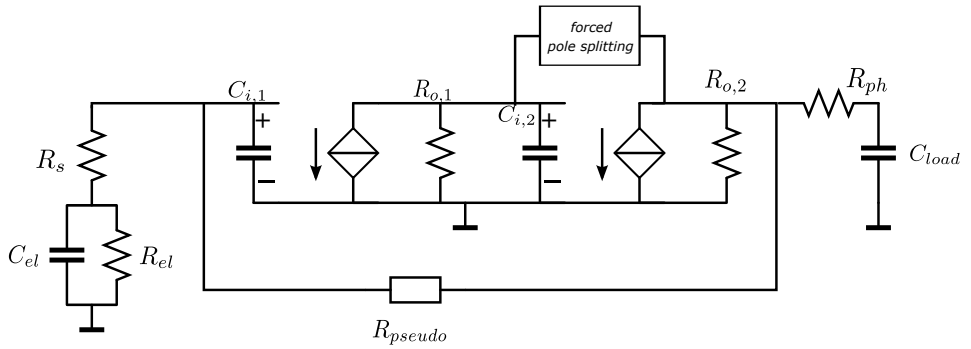


Figure 4.21: Simplified small signal diagram of the TIA with a dual-stage controller and frequency compensation (Fig.4.19). This diagram is used to obtain the equations for the hand calculation of the poles and zeros of the loop gain (Table 4.4).

Table 4.4: Loop gain pole-zero tracking of the TIA with a dual-stage controller and frequency compensation. The status indicates whether the pole/zero is new, modified, or unmodified in respect to the previous design step. The hand calculation provides a quick and intuitive explanation for each pole/zero. The SLiCAP column indicates the frequency of the pole/zero according to the AGM for $gain = [20\ G, 200\ M, 2\ M]\ \Omega$.

Pole/zero	Status	Hand calculation	SLiCAP
Out pole (p_1)	Modif.	$\frac{-1}{2\pi R_{o,2} C_{load}} = \frac{-1}{2\pi \cdot 2.8M \cdot 5p} = -11.4\ kHz$ + forced pole splitting ($\overrightarrow{f.p.s.}$)	$-5\ Hz$
Source pole (p_2)	Same	$\frac{-1}{2\pi(R_s+R_{pseudo})C_{el}} = \frac{-1}{2\pi \cdot [102M, 20.1G] \cdot 5p} = -[1.52, 303]\ Hz$	$-[1.5, 103, 312]\ Hz$
Input pole (p_3)	Same	$\frac{-1}{2\pi(R_s \| \| R_{pseudo})C_{i,1}} = \frac{-1}{2\pi \cdot [2{,}100] M \cdot 260f} = -[6, 300]\ kHz$	$-[6457, 9379, 308k]\ Hz$
Intermediate pole (p_4)	Modif.	$\frac{-1}{2\pi R_{o,1} C_{i,2}} = \frac{-1}{2\pi \cdot 40M \cdot 10.5f} = -378\ kHz(\overleftarrow{f.p.s.})$	$-1.5\ MHz$
P.s. Rps pole (p_6)	New	$\frac{-1}{2\pi R_{ps} C_{i,2}} = \frac{-1}{2\pi \cdot 200k \cdot 10.5f} = -75\ MHz$	$-58\ MHz$
Phantom z. pole (p_7)	New	–	$-18\ GHz$
Source zero (z_1)	Same	$\frac{-1}{2\pi R_s C_{el}} = \frac{-1}{2\pi \cdot 100M \cdot 5p} = -318\ Hz$	$-318\ Hz$
P.s. (Rps) zero (z_2)	New	$\frac{-1}{2\pi R_{ps} C_{ps}} = \frac{-1}{2\pi \cdot 200k \cdot 5p} = -159\ kHz$	$-174\ kHz$
Phantom zero (z_3)	New	$\frac{-1}{2\pi R_{ph} C_{load}} = \frac{-1}{2\pi \cdot 4k \cdot 5p} = -7.95\ MHz$	$-7.95\ MHz$
P.s. direct zero (z_5)	Modif.	–	$+5.45\ GHz$

4.2.6. Biasing

Once the amplifier satisfies all the bandwidth, accuracy, and stability requirements, it must be biased. Bias allows the transistors to achieve the operating point at which all the requirements were met and must not cause excessive degradation on the amplifier's performance.

The proposed amplifier with biasing is shown in Fig. 4.22. M_2 and M_3 are the top biasing of the first stage, M_6 is the bottom biasing, and M_5 is the biasing of the second stage.

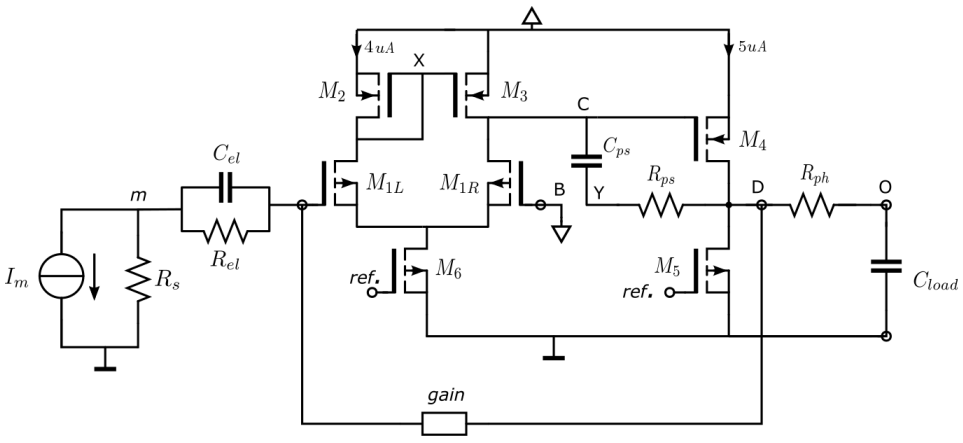


Figure 4.22: Schematic of the TIA with a dual-stage controller, frequency compensation and biasing. The input stage is a balanced common-source ($M_{1,L\&R}$) and the output stage is an unbalanced common-source (M_4). C_{ps} and R_{ps} are the pole-splitting elements around the second stage.R_{ph} is the phantom zero resistor in the output. M_2 and M_3 are the top biasing of the input stage, M_6 the bottom biasing, and M_5 the biasing of the second stage. M_5 and M_6 are connected to a reference as in Fig. 4.28.

Top biasing of the first stage

The relevant specs to design the top biasing of the first stage are the maximum input voltage range, which needs to be higher than $2.3\ V$ as explained in Section 4.1; the noise contribution; and the power

supply rejection ratio (PSRR). As a current mirror is selected for the biasing, an additional performance aspect that needs to be addressed is the speed.

Regarding the noise, the design of the first stage as a common-source stage seeks to reduce the noise contribution of later stages. However, the noise coming from the biasing of the first stage might still be relevant. The noise excess factor (NEF) is approximately given by Eq. 4.6 considering the noise transformations in Fig. 3.5 with $\Gamma = 1$, $n = 1$, and $D_1 = 0$. The design strategy is to increase the IC (reducing $g_{m,M2}$ with a larger L and smaller W for the same I_D).

$$NEF = (1 + \frac{g_{m,M2}}{g_{m,M1}}) \tag{4.6}$$

The maximum input voltage can be calculated as in Eq. 4.7, so $V_{GS,M2}$ should be reduced. Looking at Eq.3.21, that translates into a smaller IC (a smaller L and larger W for the same I_D).

$$V_{in,max} = V_{dd} + V_{GS,M2} - V_{sat,M1} + V_{GS,M1} \tag{4.7}$$

Regarding the PSRR, a rough estimation of the low-frequency voltage referred PSRR ($PSRRv@DC$) is given in Eq. 4.8 [52]. Considering the definition of g_o in Eq. 3.15, the L needs to be as large as possible. However, it is not feasible to have transistors larger than $10\ \mu m$ in this process.

$$PSRR = \frac{g_{m,M1}}{g_{o,M1} + g_{o,M3}} \tag{4.8}$$

Regarding the speed, it is given by the f_T of the transistors that form the current mirror. Based on Eq. 3.24, the size of the device, especially in terms of L, should be reduced.

Since the optimization of each parameter is opposed to each other, a trade-off is necessary. Fig.4.23 helps to select the proper size of the biasing. $W = 7.5\ \mu m$ and $L = 5\ \mu m$ provides an estimated $V_{in,max}$ around $3\ V$, a NEF of 1.25, a $PSRRv@DC$ of $61\ dB$, and an f_T of $2 \cdot 10^7\ Hz$ which makes its pole to have only a slight influence on the loop gain phase response dominant frequencies.

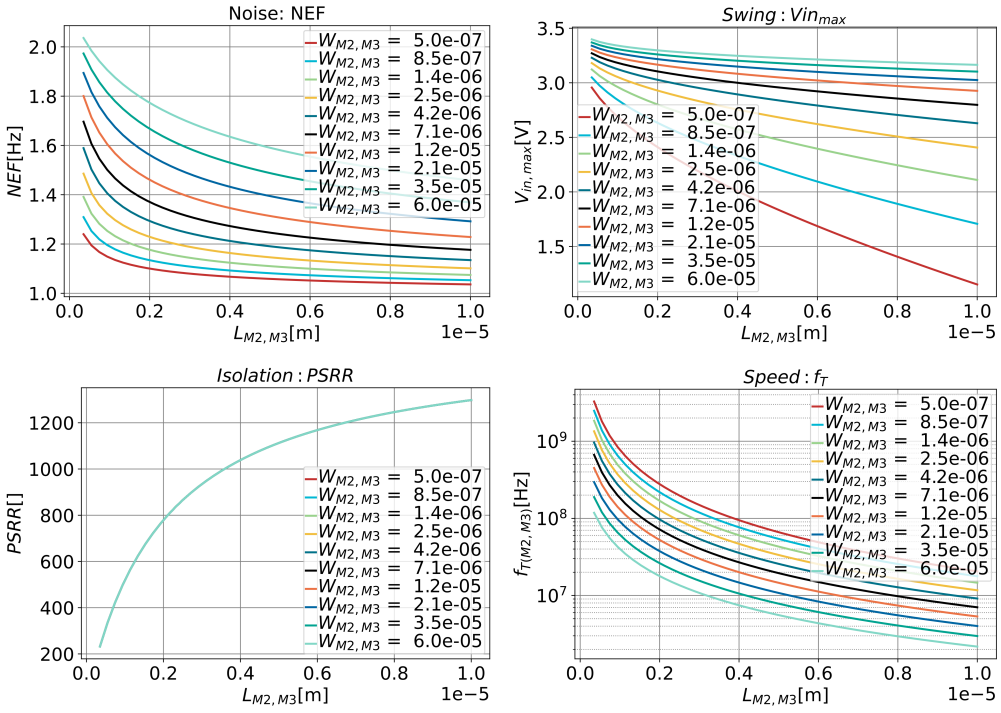


Figure 4.23: Estimations of NEF, the maximum input voltage of the TIA, the PSRR, and the f_T of $M_{3,4}$ versus $L_{M3,4}$ and $W_{M3,4}$. $ID = 4\ \mu A$. These parameters are essential for the overall performance, but they oppose each other. The noise contribution of the biasing decreases with larger IC (larger L and smaller W for the same ID). The maximum voltage is increased with the opposite sizing. The larger the L, the larger the PSRR, but the slowest the device is. The $V_{in,max}$ needs to be at least $2.3\ V$ and the f_t one decade over the amplifier bandwidth ($f_t > 2 \cdot 10^7\ Hz$). A good trade-off is found at $W = 7.5\ \mu m$, $L = 5\ \mu m$.

Bottom biasing of the first stage and second stage

Both bottom biasing networks are oriented to maximize the minimum voltages: the input voltage in the first stage and the output voltage in the second. Based on Eqs.4.9 and 4.10, the saturation voltages of both transistors need to be minimized. This requirement translates into a lower IC (smaller L and larger W for the same I_D), as given in Eq.3.22.

$$V_{in,min} = V_{GS,M1} + V_{sat,M6} \tag{4.9}$$

$$V_{out,min} = V_{sat,M5} \tag{4.10}$$

Fig. 4.24 helps to select the proper size of the biasing. Since both transistors can have the same sizing strategy, it is useful to size them with the same length and width proportional to their drain currents. With this sizing strategy, it is possible to reuse the reference network. Setting $L_{M5,M6} = 1.5\ \mu m$, $W_{M5} = 5\ \mu m$, $W_{M6} = 8\ \mu m$, the expected $V_{in,min} = 0.84\ V$ and $V_{out,min} = 0.17\ V$.

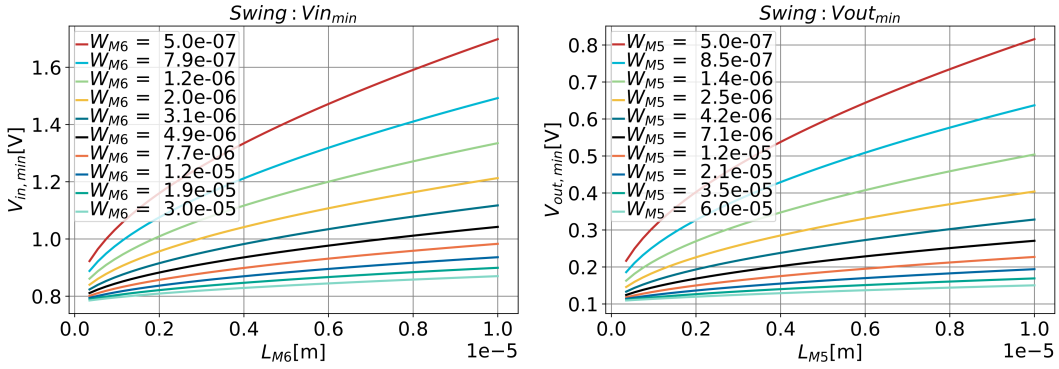


Figure 4.24: Estimations of the minimum input and output voltages of the TIA versus L and W of the bottom biasing of the first stage (M_6) and the biasing of the second stage (M_5), respectively. In both cases it is beneficial to lower the IC (smaller L and larger W for the same I_D). $V_{in,min}$ needs to be below $1\ V$ and $V_{out,min}$ as close to $0\ V$ as possible. $W = 5\ \mu m$, $L = 1.5\ \mu m$ are selected.

The influence of the biasing in the poles and zeros of the loop gain is tracked in Table 4.4. The most significant changes are the introduction of a pole $p_5@-f_t/2$ and a zero $z_4@-f_t$ due to the current mirror effect highlighted in Fig. 4.26. The output pole p_1 is also slightly affected because the output impedance of the second stage is now formed by the parallel between the output resistances of the second stage transistors and their biasing. The final loop gain is shown in Fig. 4.25. As expected, the only difference compared to the unbiased circuit is a slight decrease in the DC loop gain and the phase at high frequencies. The results have been obtained with the script in Annex A.3.

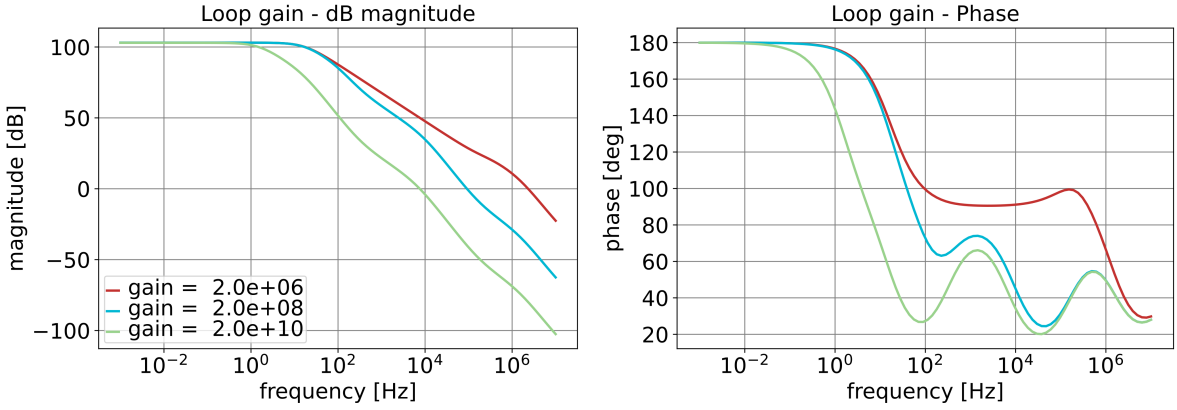


Figure 4.25: Loop gain of a TIA with a dual-stage controller after frequency compensation and biasing. The loop gain is not affected by the biasing but slighlty in the DC loop gain and in the phase for frequencies over the dominant bandwidth.

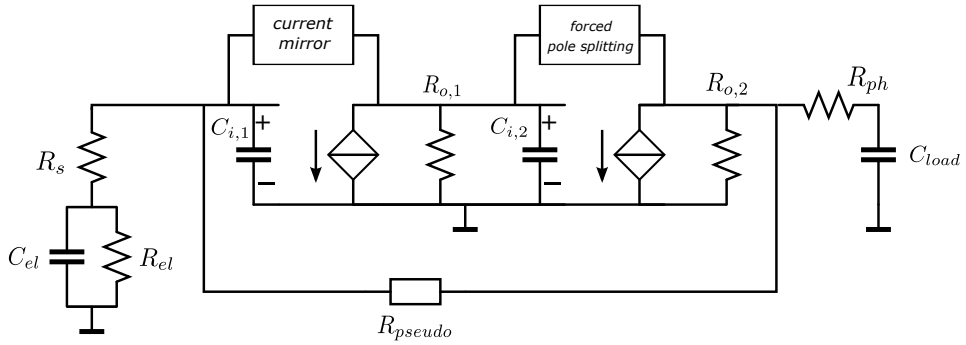


Figure 4.26: Simplified small signal diagram of the TIA with a dual-stage controller, frequency compensation and biasing (Fig. 4.22). This diagram is used to obtain the equations for the hand calculation of the poles and zeros of the loop gain (Table 4.5).

Table 4.5: Loop gain pole-zero tracking of a TIA with a dual-stage controller after frequency compensation and biasing. The status indicates whether the pole/zero is new, modified, or unmodified in respect to the previous design step. The hand calculation provides a quick and intuitive explanation for each pole/zero. The SLiCAP column indicates the frequency of the pole/zero according to the AGM for $gain = [20\ G, 200\ M, 2\ M]\ \Omega$.

Pole/zero	**Status**	**Hand calculation**	**SLiCAP**
Out pole (p_1)	Modif.	$\frac{-1}{2\pi R_{o,2}C_{load}} = \frac{-1}{2\pi\cdot 2.3M\cdot 5p} = -14\ kHz(\overrightarrow{f.p.s.})$	$-17\ Hz$
Source pole (p_2)	Same	$\frac{-1}{2\pi(R_s+R_{pseudo})C_{el}} = \frac{-1}{2\pi\cdot[102M,20.1G]\cdot 5p} = -[1.52, 303]\ Hz$	$-[1.5, 103, 312]\ Hz$
Input pole (p_3)	Same	$\frac{-1}{2\pi(R_s\|\|R_{pseudo})C_{i,1}} = \frac{-1}{2\pi\cdot[2,100]M\cdot 260f} = -[6, 300]\ kHz$	$-[6457, 9379, 308k]\ Hz$
Intermediate pole (p_4)	Modif.	$\frac{-1}{2\pi(R_{o,1}\|\|R_{o,cm(r)})C_{i,2}} = \frac{-1}{2\pi\cdot 22M\cdot 10.5f} = -689\ kHz(\overleftarrow{f.p.s.})$	$-1.5\ MHz$
Current mirror pole (p_5)	New	$f_t/2 = 9\ MHz$	$-8.7\ MHz$
P.s. Rps pole (p_6)	Same	$\frac{-1}{2\pi R_{ps}C_{i,2}} = \frac{-1}{2\pi\cdot 200k\cdot 10.5f} = -75\ MHz$	$-58\ MHz$
Phantom z. pole (p_7)	Same	–	$-8\ GHz$
Source zero (z_1)	Same	$\frac{-1}{2\pi R_s C_{el}} = \frac{-1}{2\pi\cdot 100M\cdot 5p} = -318\ Hz$	$-318.3\ Hz$
P.s. (Rps) zero (z_2)	Same	$\frac{-1}{2\pi R_{ps}C_{ps}} = \frac{-1}{2\pi\cdot 200k\cdot 5p} = -159\ kHz$	$-174\ kHz$
Phantom zero (z_3)	Same	$\frac{-1}{2\pi R_{ph}C_{load}} = \frac{-1}{2\pi\cdot 4k\cdot 5p} = -7.95\ MHz$	$-7.95\ MHz$
Current mirror zero (z_4)	New	$f_t = -18\ MHz$	$-19\ MHz$
P.s. direct zero (z_5)	Same	–	$+5.45\ GHz$

Summary

As a summary, Fig.4.27 shows a simplified sketch of the poles and zeros added in each stage and their influence on the stability. Fig.4.28 presents the final controller and all the transistor sizes.

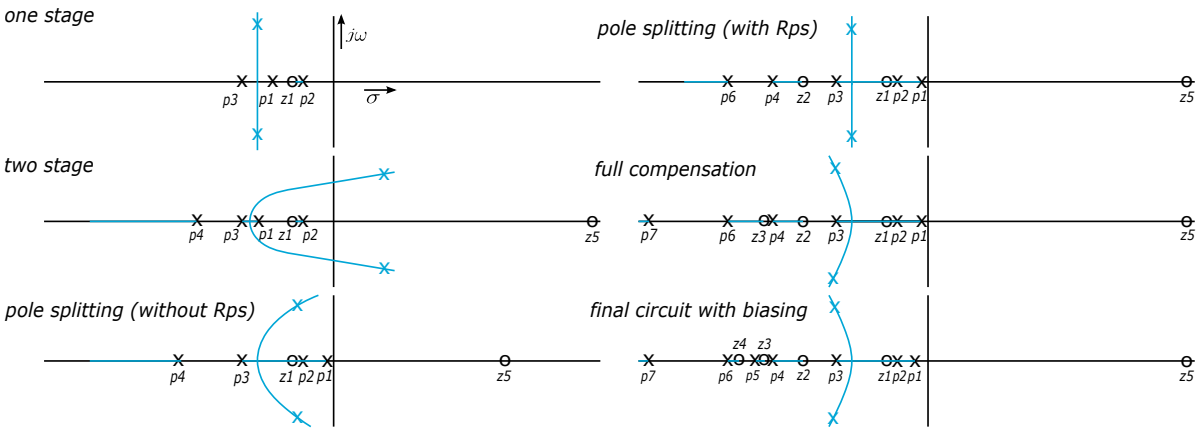


Figure 4.27: Conceptual pole-zero diagrams of the different design steps. The two-stage solution is unstable because two asymptotic gain poles (cyan crosses) are located in the positive half plane. The application of pole splitting and phantom zero help to bring back those poles into the negative half plane. The location and tags of the poles and zeros comes from Tables 4.2, 4.3, 4.4 & 4.5.

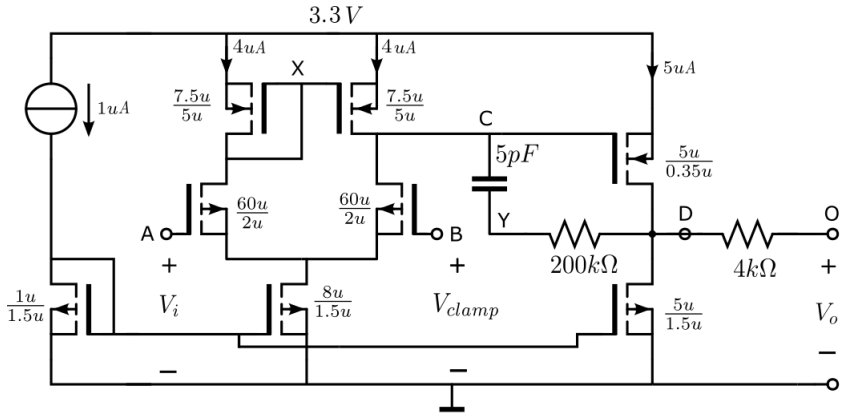


Figure 4.28: Final schematic and device sizes of the controller, including the reference network for the bottom biasing of the first stage and the biasing of the second stage. Nodes A, B, D, O are connected to the nodes with the same name in the system schematic in Fig. 4.1.

4.2.7. Symbolic analysis and Cadence results

This Section summarizes the most important estimations given by the symbolic analysis and compares critical parameters with the results in Cadence to verify that the process is well modeled.

Summary of the final estimations based on symbolic analysis

Fig. 4.29 shows the transfer functions of the asymptotic gain model described in Section 3.2 for the maximum, intermediate, and minimum TIA gains. Table 4.6 is a summary of the performance parameters of the TIA based on the symbolic estimations.

Table 4.6: Performance summary based on the estimations from the symbolic analysis

Parameter	Estimation
V_{in}	$[0.84, 2.97]\ V$
V_{out}	$[3.13, 0.171]\ V$
Noise (output)	$[0.014, 3.0]\ mV_{rms}$ depending on the gain
Bandwidth	$[8.7k, 2.5M]Hz$ depending on the gain
Payload area	$1.07 \cdot 10^{-9}\ m^2$

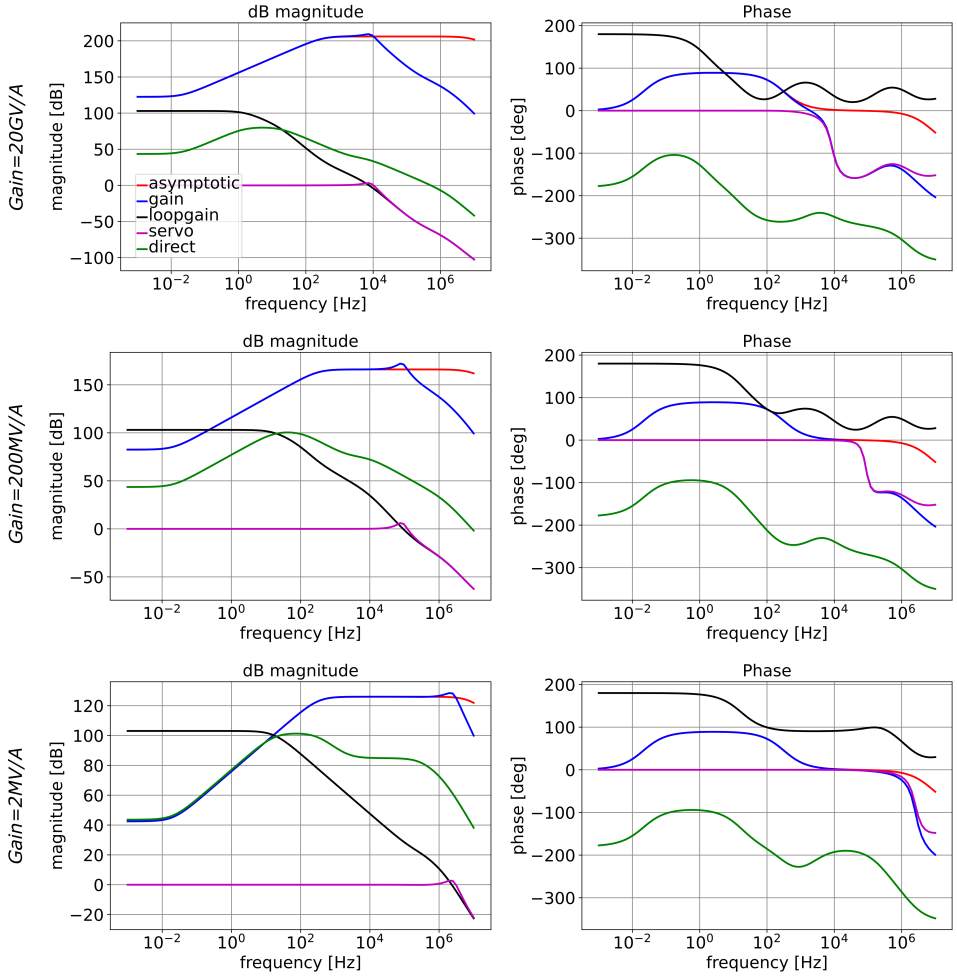


Figure 4.29: Transfer functions of the asymptotic for the maximum, intermediate, and minimum TIA gains. As explained in Section 3.2, the servo function indicates the bandwidth of the amplifier and the frequency range where the ideal gain follows the asymptotic gain. In all cases, the direct gain is much smaller than the loop gain or the gain, so it does not interfere with the result.

Comparisons with Cadence simulations

Until this point, all the calculations have been performed using the EKV models presented in Section 4.2.1 and symbolic analysis with SLiCAP. Therefore, it is necessary to verify that those models match the reality. The following paragraphs compare the operating point parameters, the loop gain, and the noise to the Cadence results.

Table 4.7 shows selected operating point parameters for both Cadence and SLiCAP. Generally, the match is satisfactory. The divergences are marked with a superscript. The first divergence, which affects the output resistance (Eq. 3.15), is likely coming from the simplification of V_{AL} that was explained in Section 3.1. V_{AL} depends on the level of saturation, among others. However, this is not being modeled in the symbolic analysis. The second divergence affects the V_{sat} of the transistors that operate in moderate inversion, using any of the two Eqs. 3.22 or 3.23. The third divergence affects the V_{th} (and therefore also the V_{GS}) of the transistors in the balanced input stage. The reason is that the body effect is not being modeled, as mentioned in Section 3.1.

None of the three divergences are severe enough to invalidate the results. This statement is demonstrated with the loop gain and noise comparisons. Fig. 4.30 shows that there are almost no differences in the loop gain but out of the dominant bandwidth in the loop gain. Similarly, the noise spectrum and estimations of the RMS output referred contribution of the controller are almost equal, as shown in Fig. 4.31. In conclusion, the simplified EKV model and its parameters can model the process accurately and with enough simplicity to be helpful in symbolic design. Besides, these EKV parameters can be reused for other projects with the same process.

Table 4.7: Comparison of operating point parameters estimated with SLiCAP/Symbolic analysis (cyan) and simulated with Cadence (black). All the parameters match very good. There are three slight variations marked with superscripts. Those differences are likely due to the simplifications in modelling V_{AL}, the neglecting of the body effect, and the equations of V_{sat}.

Parameter Cadence/Symbolic analysis	**M1L/R**	**M2**	**M3**	**M4**	**M5**	**M6**
$f_t[MHz]$	43	18	18	1080	281	277
	-	19	19	850	258	258
$g_m[\mu A/V]$	64	18	18	58	53	83
	78	19	19	56	56	89
$r_{out}[M\Omega]$	24/25	47	29	2.4	28	6.8
	20	50	50[1]	2.8	12[1]	7.5
$V_{sat}[mV]$	52	272	272	107	107	106
	58	318	318	170[2]	171[2]	171[2]
$V_{GS}[mV]$	963	975	975	691	833	833
	670[3]	943	943	686	830	830
$V_{th}[mV]$	1020	633	633	625	734	735
	710[3]	570	570	570	710	710

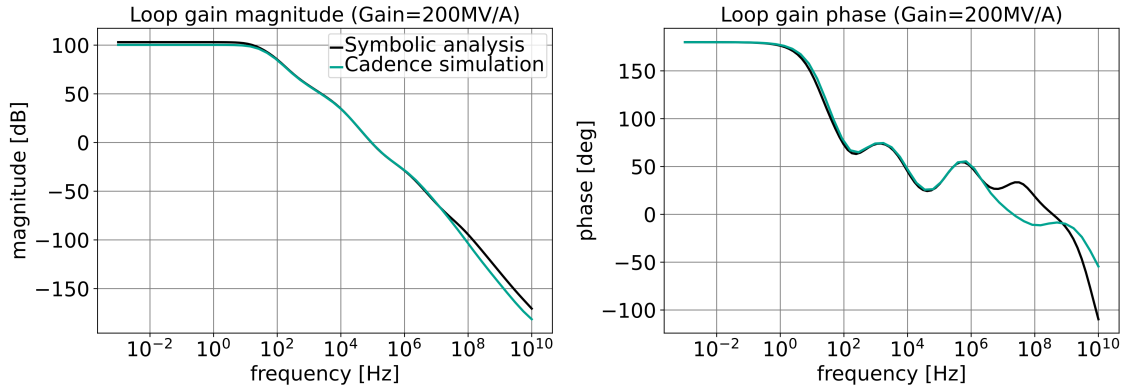


Figure 4.30: Comparison of the loop gain estimated with SLiCAP and the simulated in Cadence. They match almost perfectly but for frequencies out of the interest bandwidth.

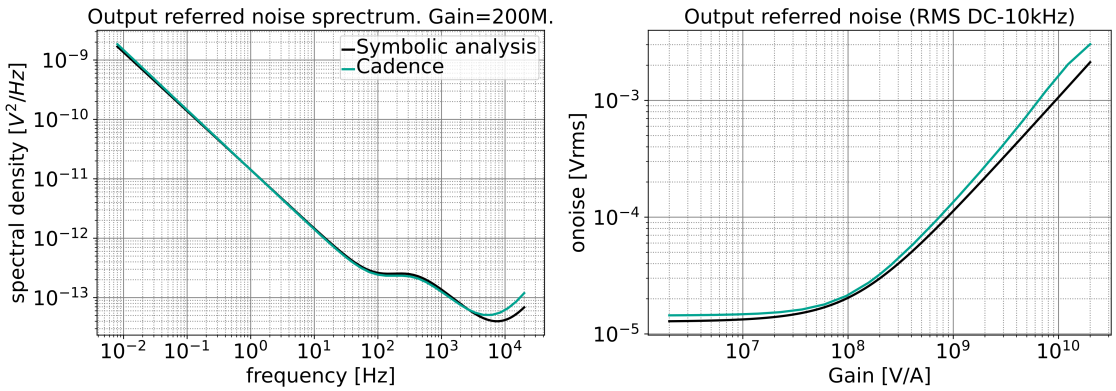


Figure 4.31: Comparison of the output referred noise spectrum and the output referred RMS noise ($\sim DC - 10\ kHz$) estimations with SLiCAP and simulations in Cadence. They match almost perfectly. At high frequencies there are noise contributions coming from elements that were not modelled in Fig. 4.4 or contributing to the NEF in Eq.4.6 but their influence is small.

4.3. Pseudo-resistor

As mentioned in Section 4.1, the transconductance in the feedback network is in charge of setting the trans-impedance gain of the amplifier. In terms of the asymptotic gain model, this network sets the ideal gain along with the source and load impedances.

A standard resistor cannot be used due to the enormous value of the resistance ($[2M, 20G]\ \Omega$). The two options are using active feedback such as a gm-cell or a passive structure that resembles a resistor as a pseudo-resistor. A gm-cell has a better performance in terms of accuracy and flexibility to do frequency compensation. However, the passive option outperforms in terms of simplicity, area, and power consumption a priori.

In principle, a pseudo-resistor suits better in this application since accuracy is not a relevant specification, while the area is. Not only the main reference [3] but also previous publications from our lab [17] have selected the pseudo-resistor with positive results.

A pseudo-resistor can be implemented in many different ways. For example, in [3] they use a switched capacitor, while in [17] they use pairs of transistors with the bulk connected to the drain. The design of a pseudo-resistor tends to be tricky because of parasitics' strong influence (or even intended use). Therefore, following the concept in [17], which has been tested in the lab before, seems safer. Besides, this option seems to show a better performance in terms of bandwidth. Nevertheless, the pseudo-resistor needs to be redesigned because the transistors are different compared to those in [17] and the gain range needs to be much broader due to the margins that were applied in Section 4.1.

4.3.1. Concept

The pseudo-resistance structure is based on a mirrored pair of CMOS transistors with connected gates and sources, as shown in Fig. 4.32 (a). This structure works as a floating resistor between terminals V_{in+} and V_{in-} and its equivalent resistance value is adjusted with V_{SG}.

For any V_{in} one transistor has its bulk connected to the drain, while the other has the bulk connected to the source (the drain and source have switched). When the elementary building blocks are connected in series, as in this case, the resistance is set by the least conductive block [21]. This effect means that the resistance is set by the transistor whose bulk is connected to drain, which follows Eq. 4.11 [53]. The slope of the traces in Fig. 4.32 (b) represents the inverse of the resistance depending on the control voltage V_{SG}.

$$R_{SD} = \frac{nU_T}{I_{SD}} \frac{e^{\frac{V_{SD}}{U_T}} - 1}{(n-1)e^{\frac{V_{SD}}{U_T}} + 1} \tag{4.11}$$

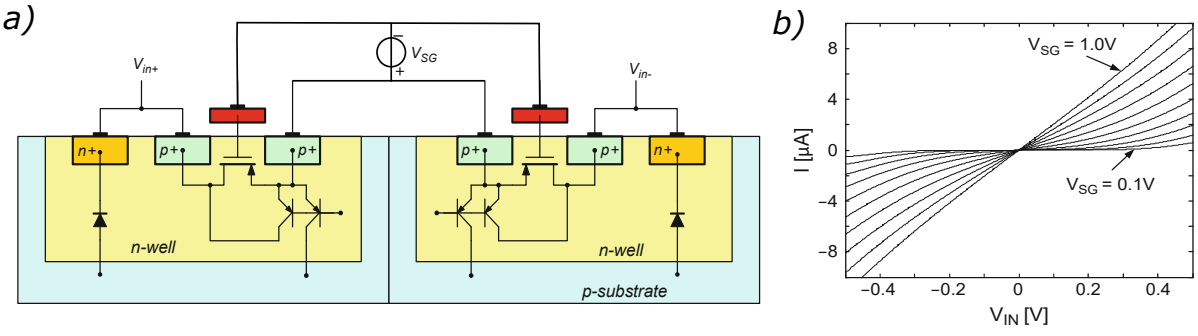


Figure 4.32: a) Cross-section view of the mirrored pair of PMOS transistors used to create a floating pseudo-resistance cell. The equivalent schematic includes parasitics, which limit the voltage swing across the terminals $V_{in,+}$ and $V_{in,-}$. The controlling voltage V_{SG} is applied between the gates and the sources. The drain and the bulks are connected. b) I–V characteristics of the cell in (a). Source: [53], edited.

The two main limitations of this structure are the voltage swing V_{in} and bandwidth limitations. The voltage limitation is caused by the forward-biased source-bulk diode connection current leakage, which becomes similar to the I_{SD} current when $V_{in} > 0.4\ V$ [53]. The bandwidth limitation is given by the capacitive effects of the n well-p substrate junction at the output of the circuit [53]. However, the structure has been used for applications at frequencies around 100kHz before [53].

4.3.2. Ideal cell

The objectives of the pseudo-resistor are to handle input voltages between at least $[1, 2.3]\ V$, output voltages as close as possible to $[0, 3.3]\ V$ ($2\ V$ swing), a bandwidth of $10\ kHz$, and a good response against the PVT. The last aspect is left for future research as discussed in Chapter 6.

As mentioned in the previous paragraphs, the voltage swing of a pseudo-resistance cell is limited to around $0.4\ V$, while the minimum required in the proposed system is $2\ V$. Therefore, it is necessary to place several cells in series as in Fig. 4.33 to divide up the voltage drops. Since the blocks are not linear, the equation for the voltage in each node is quite complex. Several combinations are simulated to avoid those calculations. Fig. 4.34 shows the comparison in the DC and AC responses between four and eight blocks as an example. The election is to use eight blocks.

The floating voltage V_c needs to be implemented with a biasing network. Therefore, the values of V_c need to be in a reasonable range. Voltages below $0.1\ V$ would be hardly controllable, while voltages over $1\ V$ would take too much headroom. On the other side, the differences between the two extreme values of V_c (those to get a resistance of $2M\ \Omega$ and $20G\ \Omega$) cannot be very close to each other, because that would make very difficult to set intermediate resistance levels.

The sizing of the transistors seeks to achieve the required resistance values with a good trade-off for the V_c. After many simulations, $W_{Mpr} = 350\ nm$ and $L_{Mpr} = 500\ nm$ is chosen. The V_c needs to be between 0.27 and $0.90\ V$ to achieve gains between $2M\ \Omega$ and $20G\ \Omega$ with eight pairs of those transistors.

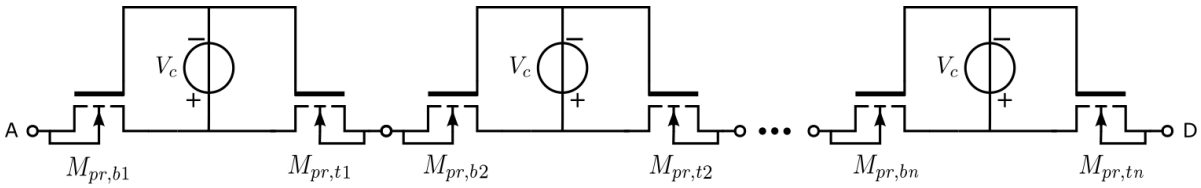


Figure 4.33: Schematic of the floating pseudo-resistance cells in Fig. 4.32. Eight cells are connected in series to allow a larger voltage swing between the two terminals A and D. Nodes A and D match those with the same name in the system schematic in Fig. 4.1.$V_c = V_{SG}$ is the controlling voltage. The size of the transistors is $W_{M,pr} = 350\ nm$ and $L_{M,pr} = 500\ nm$.

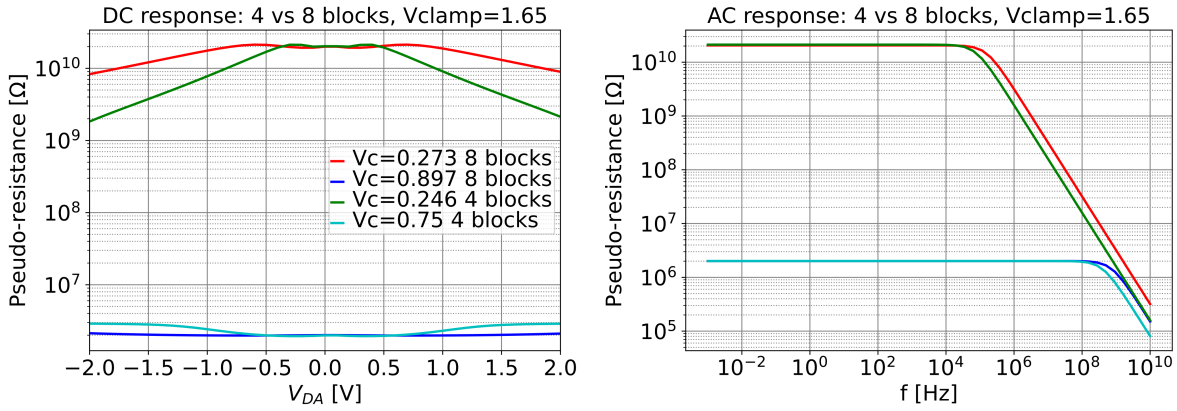


Figure 4.34: Comparison of the DC and the AC responses of a series connection of four or eight pseudo-resistance floating cells. The controlling voltages set the maximum and minimum TIA gains: $20\ GV/A$ and $2\ MV/A$. With eight blocks, the resistance variation is less than 100% for any swing value between -1.65 and $1.65\ V$. In both cases, the bandwidth is over $10\ kHz$.

4.3.3. Real implementation

As mentioned before, the voltage V_c is implemented with a biasing network. The most simple network is a voltage follower, which is the selected option. As it will be discussed in Chapter 6, more complex options have a better performance in terms of PVT.

Two different transistors are used to generate the voltages between 0.27 to $0.90\ V$. One of them is narrow and long, while the other is wide and short. The former generates voltages from 0.50 to $0.94\ V$, while the latest from 0.25 to $0.52\ V$. The transistor is selected with the digital signal's most significant bit (MSB) that sets the resistance value. This selection creates two operating modes: a low resistance mode (LR) for gains between $2\ M\Omega$ and $60\ M\Omega$ ($V_c \in [0.50, 0.90]\ V$), and a high resistance mode (HR) for gains between $60\ M\Omega$ and $20\ G\Omega$ ($V_c \in [0.27, 0.50]\ V$). The specific resistance value is set in each mode by adjusting the current I_c between 1 and $329\ nA$. Fig. 4.35 (a) shows the proposed structure.

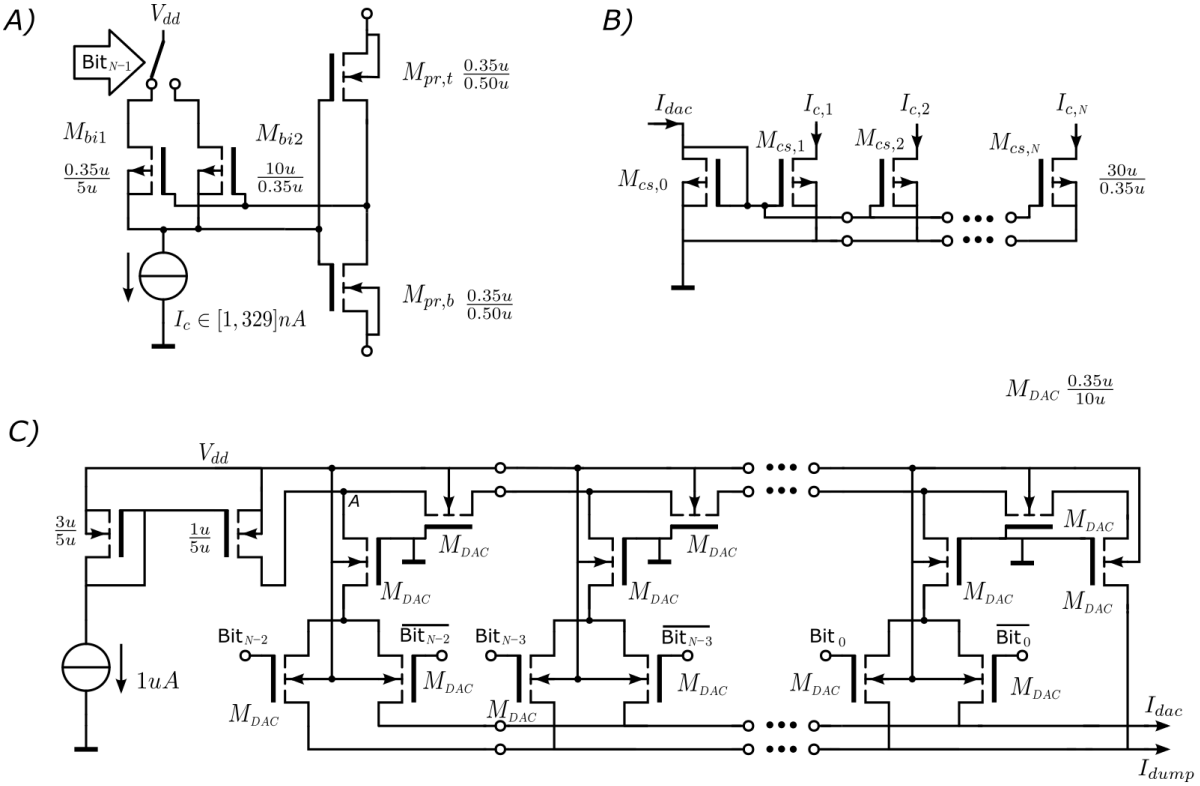


Figure 4.35: A) Pseudo-resistance cell in Fig. 4.33 with the floating controlling voltage source. M_{bi1} biasing is used to generate relatively small resistances ($2 \sim 60\ M\Omega$), while M_{bi2} creates large resistances ($60\ M \sim 20\ G\Omega$). The selection is made with the most significant bit of a control digital signal. The current source I_c, which sets the specific resistance value, is implemented with the current mirror in (B). The reference current I_{dac} can be generated in a DAC as in (C).

The size of the biasing transistors is chosen based on the targeted controlling voltage V_c and considering that I_c needs to be larger than $1\ nA$ due to process limitations. However, at the same time, I_c has to be as small as possible to reduce power consumption. Fig. 4.36 shows the V_c versus I_c that each selected transistor (LR: $350\ n/5\ \mu$, HR: $10\ \mu/350\ n$) is able to generate.

The ideal current source I_c needs to be implemented with passive devices. An option is to use a current mirror that copies a reference current as in Fig. 4.35 (b). While in the ideal implementation in Fig. 4.33 the gate voltage of the pseudo-resistance cell transistors ($M_{pr,t}$ and $M_{pr,b}$) has no restrictions (e.g., it could be negative), this gate voltage must be over a certain value if a current mirror is used. This threshold ensures that the current mirror transistors are saturated and respect their passive behavior.

The current mirror transistor's IC needs to be lowered with large width and short length to reduce the saturation voltage ($30\ \mu/0.35\ \mu$). Nevertheless, the minimum voltage between the two transistors $M_{pr,t}$ and $M_{pr,b}$ needs to be greater than $V_{SG} + V_{sat,cs}$. Even if $V_{sat,cs}$ is close to zero, there is a limitation on the output voltage of the amplifier given by V_{SG}. Fig. 4.37 shows that for output voltages below $0.5\ V$, the pseudo-resistance value is out of spec due to this limitation. Besides, the frequency response also deteriorates with the real implementation.

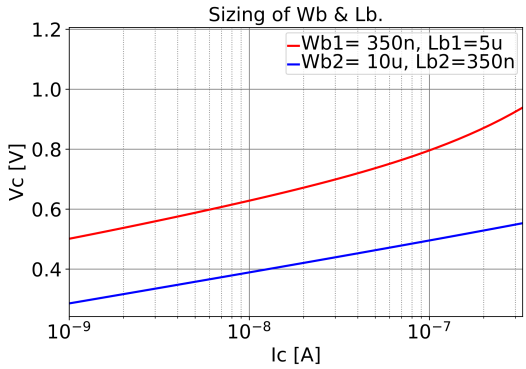


Figure 4.36: V_c versus $I_c \in [1, 329]\ nA$ for each operation mode of the circuit in 4.35 (a). The low resistance mode using M_{bi1} $(350\ n/5\ \mu)$ generates a $V_c \in [0.50, 0.90]\ V$. The high resistance mode with M_{bi2} $(10\ \mu/350\ n)$ generates a $V_c \in [0.27, 0.50]\ V$. As shown in Fig. 4.34 a $V_c \in [0.27, 0.90]\ V$ allows to adjust $R_{pseudo} \in [2\ M, 20\ G]\Omega$.

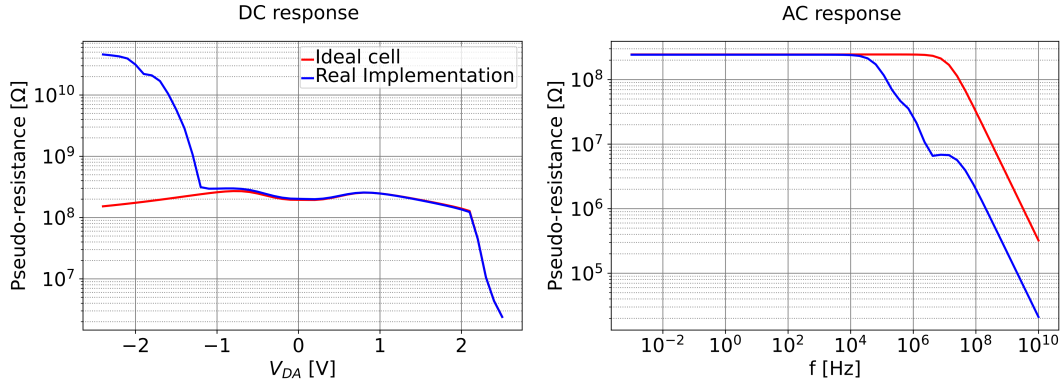


Figure 4.37: Comparison between the mid-gain DC and AC responses of the ideal pseudo-resistance cell from Fig. 4.34 and the responses of the biased pseudo-resistance cells in Fig. 4.35 (a) with $V_{clamp} = 1.65\ V$. When the output voltage is $0.5\ V$ $(1.65 - 1.15\ V)$ the pseudo-resistance stops working because the V_{DS} voltage of the transistors $M_{cs,N}$ is below V_{sat} or even negative for lower output voltages. The bandwidth is also degraded.

Reference current: DAC

The current reference that is copied in the current mirror can be provided by a digital-to-analog converter (DAC) as in Fig. 4.35 (c). The design of an optimized DAC is out of the scope of the thesis. However, an initial design is presented for completeness and testing a whole pseudo-resistor.

The DAC is based on the current division technique [12], which imposes that the current is split into half if it is injected into the node in between the sources/drains of two transistors that share the gate connection, as long as the rest of nodes are DC voltages. This property is no longer valid in case the devices are suffering from short-channel effects or mismatch [23].

As it can be seen in Fig. 4.35 (c), a $333\ nA$ current from the current mirror in the left is split in half in node A. The two transistors that divide the current in two have their gates connected to the ground, and they are long $(350\ \mu/10\ \mu)$ to ensure that they are in triode mode. Half of the current flows to the following current division cell, while the other half is either dumped into the ground or sent to the current mirror to bias the pseudo-resistance cell. The path of this halved current is decided by the bits from the digital signal that sets the pseudo-resistance value. The whole word is 8 bits, so seven are available in the DAC (one bit was already used to select the LR and HR modes in the biasing). An extra bit would be required to achieve the largest gains because the minimum current that can be selected with the 7-bit DAC is $2\ nA$ instead of $1\ nA$. However, those vast resistances are discarded due to bandwidth and stability limitations in later stages. Finally, the dumping line is loaded with a diode-connected NMOS with the same size as M_{cs} so that both OUT and DUMP terminals have the same voltage.

The performance of the whole pseudo-resistor with the DAC is almost equivalent to one with an ideal current replacing the DAC. The results with the DAC are not shown in this report because they overlap those in Fig. 4.37.

4.4. Layout

After all the Cadence simulations of the controller and the pseudo-resistor, the design can be implemented in a layout.

The layout has hundreds of rules for each particular process but also some generic strategies that are consistently applied [19]. In general, for a good layout, the elements need to have the same structure, size, orientation, and surroundings. Besides, the distance between devices needs to be minimized, and they should have common centroid geometries. Lastly, the devices should be placed on the same isotherm. There are several techniques to facilitate those strategies. The most important ones are division in fingers, the addition of dummies, folding, and interdigitation.

The division in fingers means to split a transistor into several narrower transistors in parallel. The purpose of doing so is to reduce gate resistance. However, an excess in the number of fingers causes additional parasitic capacitances. Typically, the width of each finger makes gate resistance to be below $1/5$ or $1/10$ of the $1/gm$ of the finger [47]. The script in Annex A.3 includes an estimation of the number of fingers for a good trade-off. An even number of fingers is preferred.

Adding dummies on both sides of a chain of transistors helps reduce stress in the transitions from the active area to the field oxide. This stress causes threshold voltage variations. Therefore, the devices on the sides with a different threshold should not be used but left as dummies. Unconnected dummies need to be connected to the ground or the supply rails to avoid electrostatic charge issues [19].

Folding and interdigitation allow having a symmetric and compact design. Interdigitation means that the fingers of different transistors are combined in the same transistor chain. Folding means that the transistors are halved and placed symmetrically around the cut.

Regarding the rules related to the process, they are specified in the process datasheets. Most of them are spacing rules that set the minimum distance between different types of implantation. The different types of implantation in use and the way they are represented in the layout blueprint are shown in Fig.4.38. Other process rules are related to minimum width lengths, minimum enclosures, or minimum extension of the polysilicon.

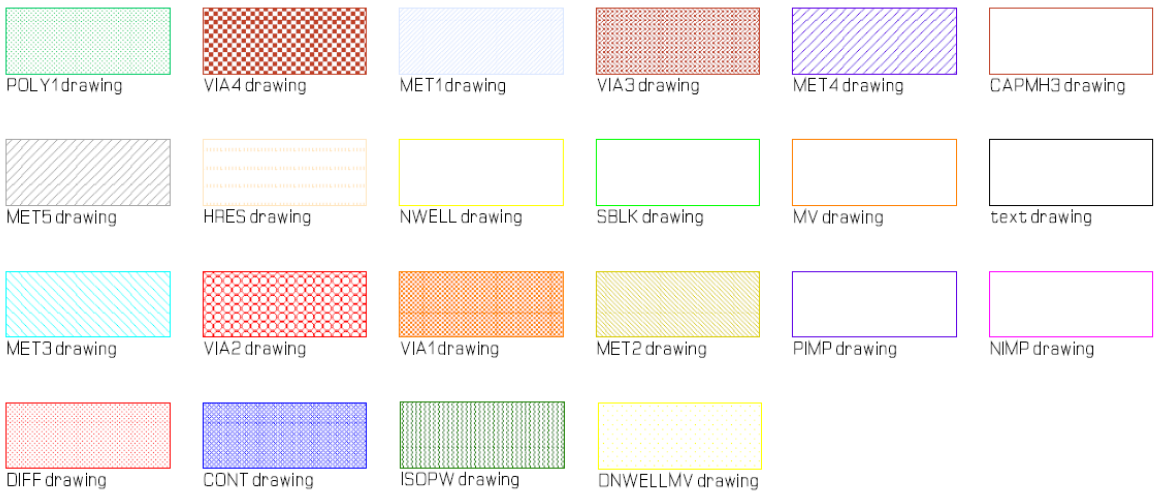


Figure 4.38: Legend of the types of implantations and layers in the layout blueprints in Figs.4.39 & 4.42

4.4.1. Controller

Fig. 4.39 shows the proposed layout for the controller. All the transistors are implemented with several fingers (M_1 4 fingers, M_2 and M_3 2, M_4 2, M_5 10, M_6 16, and M_7 2). The values are initially estimated with the results from Annex A.3 and later adjusted to be an even number and achieve a more compact layout. Besides, basic folding and interdigitation are applied for the transistors of the first stage. Lastly, dummies were added to the sides of each chain of transistors.

The resistors R_{ps} and R_{ph} are implemented in the poly-silicon. Other options as the diffusion layer or the n-well were considered. In the case of the R_{ps}, a parallel connection of two complementary MOS in triode as it is sometimes used for Miller compensation was also contemplated. However, this

option was discarded because the loop gain phase degrades. The capacitor C_{ps} is a multilayer metal-insulator-metal (MiM) capacitor that uses layers 2 to 5.

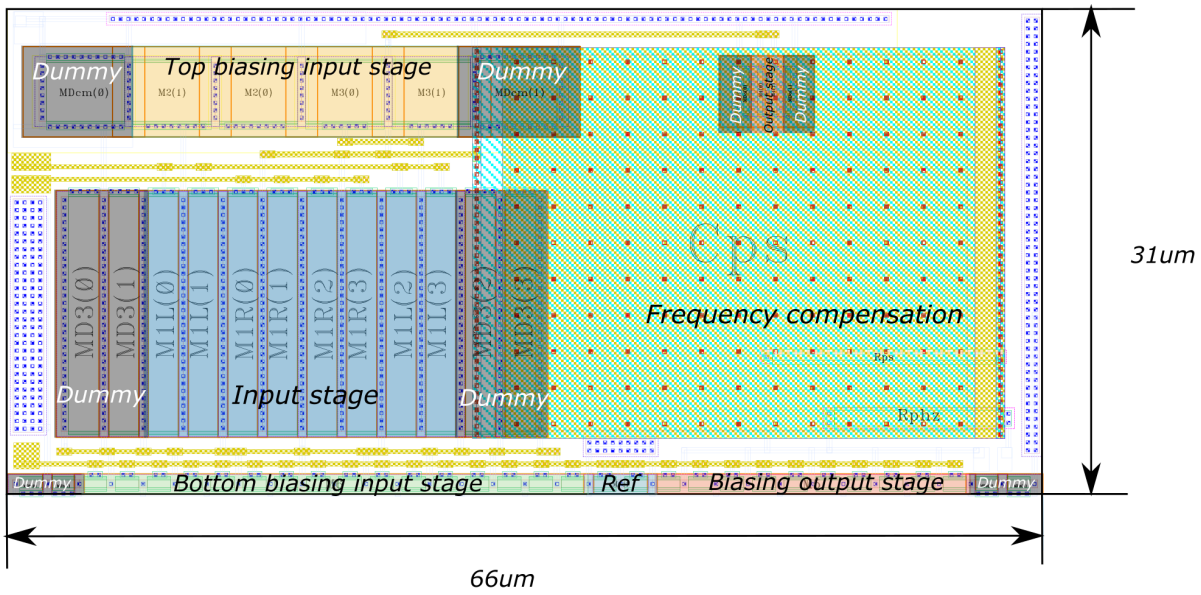


Figure 4.39: Layout of the controller. The different elements are highlighted with a semitransparent layer on top of the layout.

After the layout, it is possible to estimate the parasitics. Fig. 4.40 shows the small-signal circuit of the amplifier with the parasitic capacitances but those which are connected to GND or V_{dd}. This small-signal circuit allows tracking the influence of the parasitics in the poles and zeros of the loop gain.

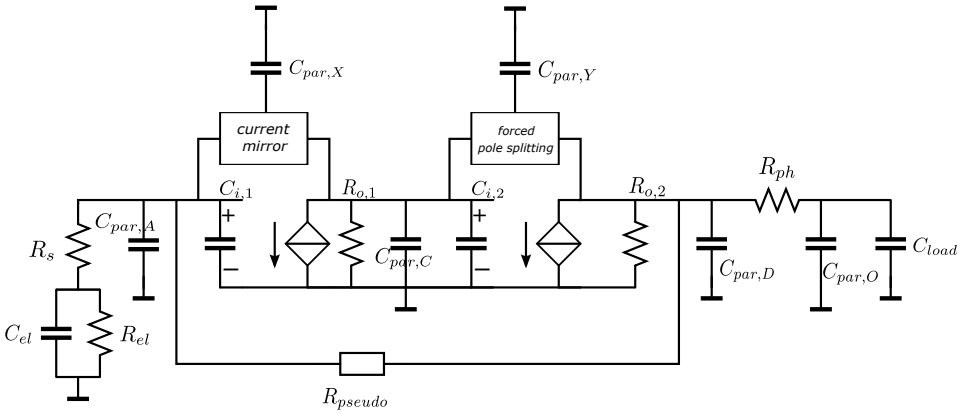


Figure 4.40: Simplified small-signal diagram of the TIA with a dual-stage controller, frequency compensation, and biasing (Fig.4.22). It also includes the parasitic capacitances that are estimated after the layout. This diagram is used to obtain the equations for the hand calculation of the poles and zeros of the loop gain (Table 4.8).

Based on the quick estimations, the most dangerous capacitances are those in the current mirror X node $C_{par,X}$, in between the pole splitting elements $C_{par,Y}$, and the capacitance in the intermediate node between the first and second stages $C_{par,C}$. The rest of the capacitances have a negligible effect on the loop gain. $C_{par,X}$ is dangerous because it can decrease the effective f_t of the current mirror affecting p_5; $C_{par,Y}$ because it can untune the pole splitting affecting p_1, p_4, and p_6; and $C_{par,C}$ because it is larger than the MOS capacitance at that node, affecting p_4 and p_6.

After studying the influence of each capacitor independently with the scripts in Annexes A.3 & A.4, it can be concluded that the pole splitting mechanism is not affected. The only pole that is expected to change significantly is p_6. There is also a slight reduction in the effective f_t of the current mirror modifying in a few kHz p_5 and z_4. The overall symbolic results are summarized in Table 4.8. Fig. 4.41

shows a comparison between the loop gain before and after layout with Cadence. It is verified that the loop gain is only affected above the dominant frequencies due to p_6.

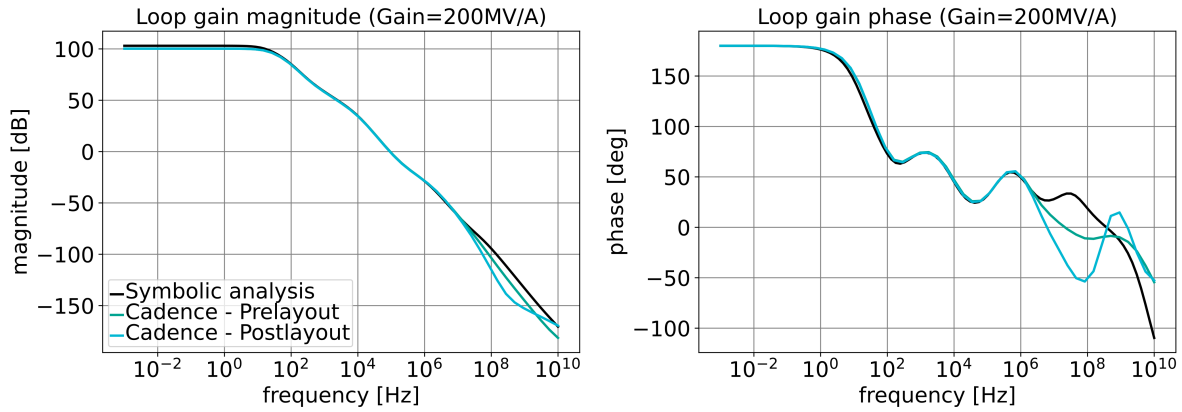


Figure 4.41: Comparison of the loop gain of the pre and post layout simulations. The prelayout symbolic analysis is shown as reference. The differences are above the dominant frequencies, so they don't affect to the performance.

Table 4.8: Loop gain pole-zero tracking of a TIA with a dual-stage controller after frequency compensation, biasing, and parasitic extraction. The status indicates whether the pole/zero is new, modified, or unmodified in respect to the previous design step. The hand calculation provides a quick and intuitive explanation for each pole/zero. The effect of the parasitics is highlighted in bold. The SLiCAP column indicates the frequency of the pole/zero according to the AGM for $gain = [20\ G, 200\ M, 2\ M]\Omega$.

Pole/zero	**Status**	**Hand calculation**	**SLiCAP**
Out pole (p_1)	Same	$\frac{-1}{2\pi R_{o,2}C_{load}} = \frac{-1}{2\pi\cdot 2.3M\cdot 5p} = -14\ kHz(\overrightarrow{f.p.s.})$	$-17\ Hz$
Source pole (p_2)	Same	$\frac{-1}{2\pi(R_s+R_{pseudo})C_{el}} = \frac{-1}{2\pi\cdot[102M,20.1G]\cdot 5p} = -[1.52, 303]\ Hz$	$-[1.5, 103, 312]\ Hz$
Input pole (p_3)	Same	$\frac{-1}{2\pi(R_s\|\|R_{pseudo})(C_{i,1}+C_{par,A})} = \frac{-1}{2\pi\cdot[2,100]M\cdot 260f\textbf{+10f}} = -[38, 380]\ kHz$	$-[6457, 9379, 308k]\ Hz$
Intermediate pole (p_4)	Same	$\frac{-1}{2\pi(R_{o,1}\|\|R_{o,cm(r)})(C_{i,2}+C_{par,C})} = \frac{-1}{2\pi\cdot 22M\cdot 10.5f\textbf{+25f}} = -203\ kHz(\overleftarrow{f.p.s.})$	$-1.5\ MHz$
Current mirror pole (p_5)	Modif.	$f_t/2\textbf{<}9\ MHz$	$-8.1\ MHz$
P.s. (Rps) (p_6)	Modif.	$\frac{-1}{2\pi R_{ps}(C_{i,2}+C_{par,C})} = \frac{-1}{2\pi\cdot 200k\cdot 10.5f\textbf{+25f}} = -22\ MHz$	$-21\ MHz$
Phantom z. pole (p_7)	Same	–	$-8\ GHz$
Parasitic pole (p_8)	New	$\frac{-1}{2\pi R_{ph}C_{par,D}} = \frac{-1}{2\pi\cdot 4k\cdot 8f} = -4.9\ GHz$	$-1.4\ GHz$
Source zero (z_1)	Same	$\frac{-1}{2\pi R_s C_{el}} = \frac{-1}{2\pi\cdot 100M\cdot 5p} = -318\ Hz$	$-318.3\ Hz$
P.s. (Rps) zero (z_2)	Modif.	$\frac{-1}{2\pi R_{ps}C_{ps}} = \frac{-1}{2\pi\cdot 200k\cdot 5p} = -159\ kHz$	$-174\ kHz$
Phantom zero (z_3)	Same	$\frac{-1}{2\pi R_{ph}C_{load}} = \frac{-1}{2\pi\cdot 4k\cdot 5p} = -7.95\ MHz$	$-7.95\ MHz$
Current mirror zero (z_4)	Same	$f_t\textbf{<}-18\ MHz$	$-18\ MHz$
P.s. direct zero (z_5)	Same	–	$+5.45\ GHz$

4.4.2. Pseudo-resistor

Fig.4.42 shows the proposed layout for the pseudo-resistor. The most relevant aspect of this layout is its size. The pseudo-resistance cells and the biasing transistors are isolated, needing an individual n-well and p-well, respectively. The spacing rules between those implantation regions make the layout design spread across a large area. Therefore, one of the advantages a priori of the passive feedback, its area, is not an advantage anymore. However, the advantage regarding power consumption is still true. In Chapter 6 there are some comments on how to reduce the area usage slightly. The transmission gates are in charge of selecting the biasing for HR or LR modes.

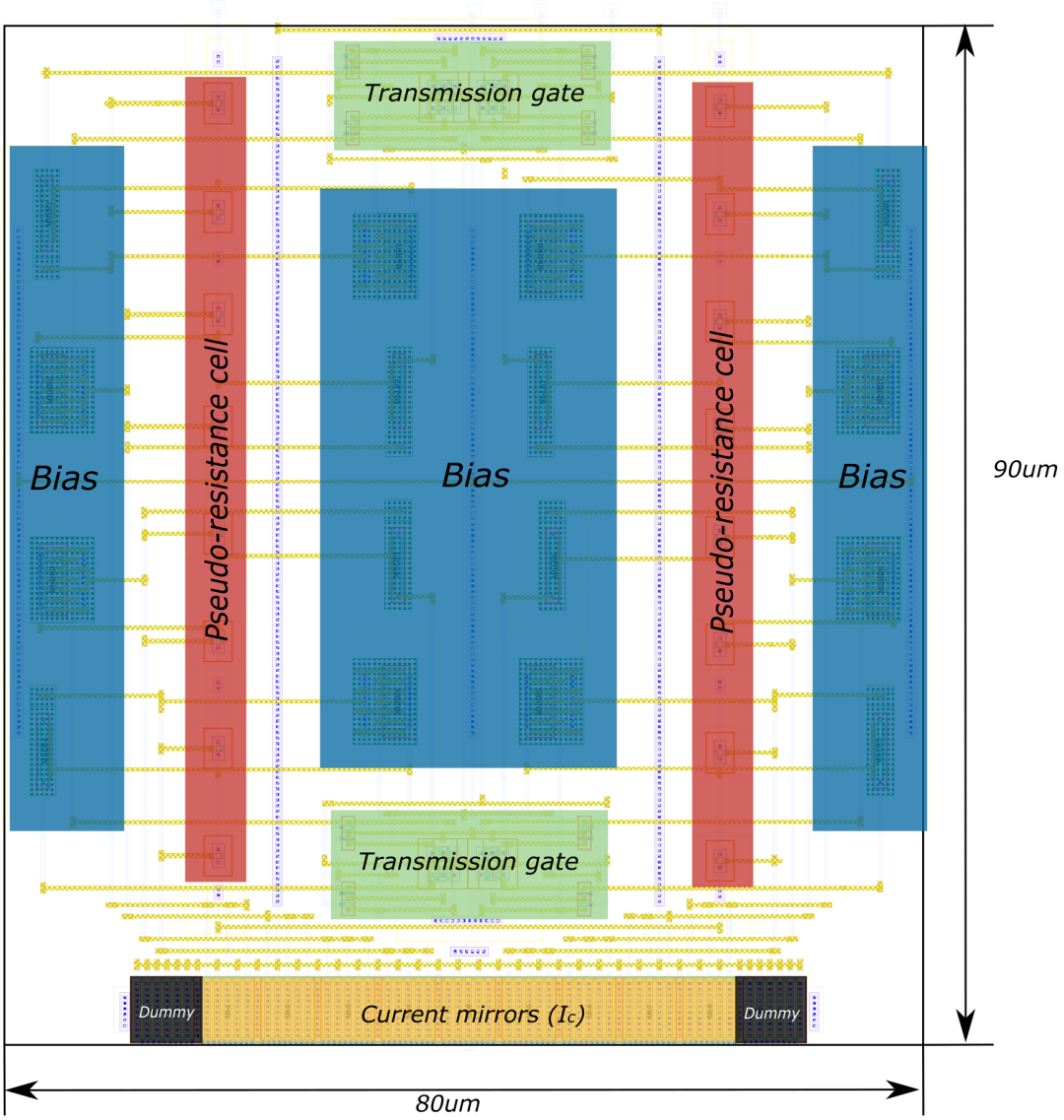


Figure 4.42: Layout of the pseudo-resistor. The different elements are highlighted with a semitransparent layer on top of the layout.

Post-layout parasitic extractions provide the estimated parasitic capacitances, which are shown in Fig.4.43. Those parasitics have a substantial effect on the bandwidth. Fig. 4.44 shows a comparison of the bandwidth for several gains in both HR and LR modes before and after layout.

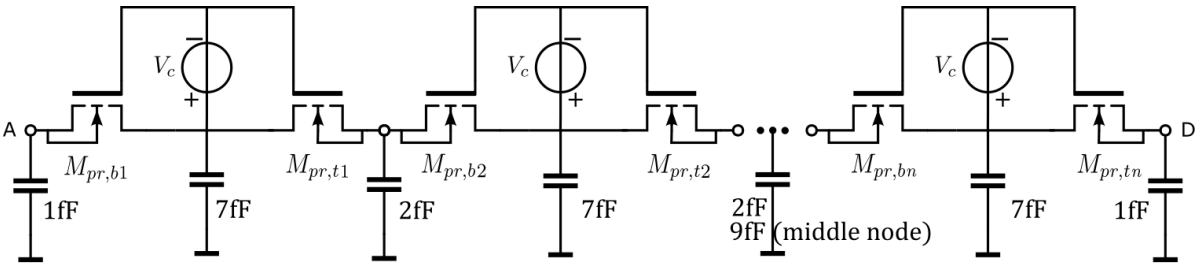


Figure 4.43: Schematic of the ideal pseudo-resistance cells in series (Fig.4.33) but adding the parasitics on each node after the postlayout simulations in Cadence. The structure reminds to an Elmore delay network.

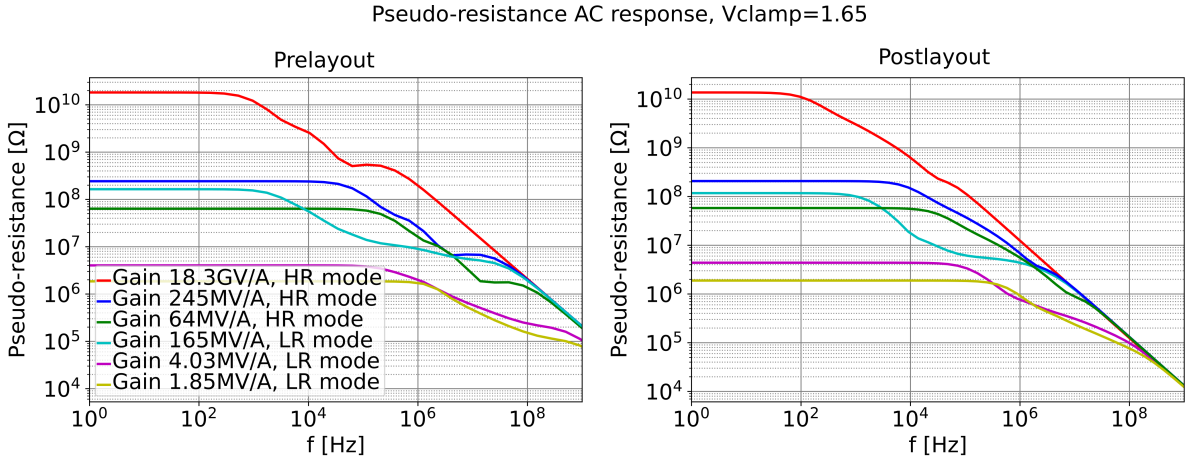


Figure 4.44: Comparison of the pre- and post-layout AC responses of the pseudo-resistor for different gains with $V_{clamp} = 1.65\,V$. The parasitic of the pseudo-resistor reduce its bandwidth significantly.

5

Results

After designing the controller and the pseudo-resistor, the combination is simulated in Cadence.

5.1. Pre-layout

In this section, the results of the pre-layout simulation of the whole system (source + load + controller + pseudo-resistor) are presented. The results related to the system requirements are highlighted.

Input and output voltage ranges

The target for the input and output voltage ranges are at least $V_{in} \in (1.0, 2.3)\ V$ and as close as possible to $V_{out} \in (0, 3.3)\ V$, respectively. Those specifications were explained in Section 4.1.

The calculation of the maximum and minimum input and output voltages is based in Eqs.4.7, 4.9, & 4.5. As explained in Section 4.3.3 the minimum output voltage is limited by the pseudoresistor biasing rather than one of those equations. The input range voltage is $V_{in} \in (0.90, 3.03)\ V$ and the output voltage range $V_{out} \in (0.5, 3.03)\ V$. The results satisfy the spec.

Noise

The noise requirement is an output referred noise close to the quantization noise of the ADC, which is about $0.56\ mV_{rms}$.

The noise spectrum for $gain = 200\ MV/A$ is shown in Fig. 5.1 as an example. The main difference with the spectrum of the contribution from the controller (Fig. 4.31) is between $10\ Hz$ to $10\ kHz$ where the noise coming from the pseudo-resistor is dominant. Therefore, the shape of the spectrum becomes flat at approximately $4kT\gamma gain$ in those frequencies.

The RMS noise ($DC - 10\ kHz$) is also shown in Fig.5.1. In this case, the contribution coming from the pseudo-resistor makes the total noise between 2 and 5 times larger depending on the gain, as estimated in Section 4.2.2. According to the graph, this statement is not valid for $gain > 1\ GV/A$. The reason is that the amplifier's bandwidth for those high gains is no longer $10\ kHz$. Hence, its output referred noise is not significant because it is effectively integrated in a smaller frequency range. The RMS noise for the mid-gain $gain = 200\ MV/A$ is $90\ \mu V_{rms}$, which is in spec.

Bandwidth and stability

The objective regarding the bandwidth is to have $DC - 10\ kHz$. There are no requirements on the over/undershoot, but the amplifier needs to be, of course, stable.

When a pseudo-resistor is used instead of an ideal resistor, the performance in terms of stability becomes much worse. This problem arises because the loop gain phase decreases sharply near the bandwidth limit. Almost all the phase margin if the pseudo-resistor is gone, as it can be seen in Fig. 5.2. However, the amplifier remains stable for $gain < 1\ GV/A$. For example, the transient response for $gain = 200\ MV/A$ is shown in Fig. 5.3. The output signal is a combination of the amplified membrane current stimuli and a voltage clamp which covers all the input voltage range $V_{in} \in [0.9, 3.16]\ V$.

The bandwidth of the amplifier is also limited, as mentioned before in the paragraph about the noise. In this case, it is because of the decision of using just one capacitor in the pole splitting frequency

compensation as mentioned in Section 4.2.6. For $gain > 1\ GV/A$ the bandwidth is no longer $DC - 10\ kHz$. Fig. 5.4(a) shows the servo function of the amplifier.

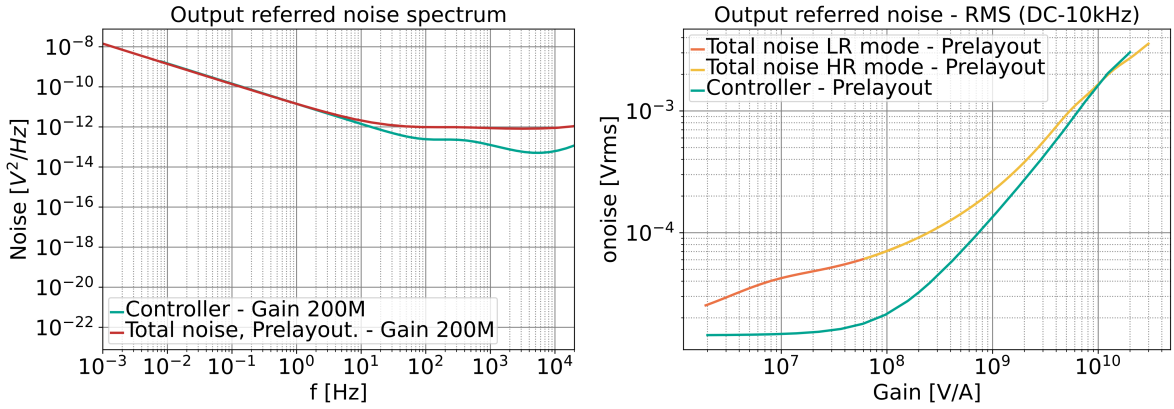


Figure 5.1: Noise spectrum for $gain = 200\ MV/A$ and output referred RMS noise versus gain. The traces represent the controller's contribution and the noise of the whole amplifier with a pseudo-resistor in the feedback network. In the spectrum between $10\ Hz$ to $10\ kHz$, the noise coming from the pseudo-resistor is dominant and flat around $4kTgain$. The pseudo-resistor contribution makes the total RMS noise between two and five times higher than the controller's contribution.

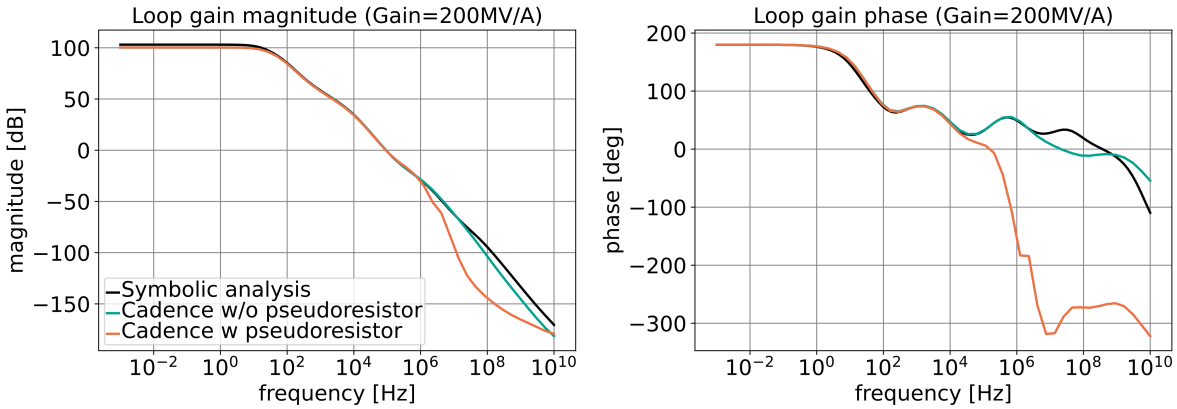


Figure 5.2: Loop gain of the system using an ideal resistor and a pseudo-resistor. The loop gain obtained in the symbolic analysis is left as a reference. When a pseudo-resistor is used the loop gain phase decreases significantly near the amplifier's bandwidth limit ($\approx 0.1\ MHz$) reducing stability margins.

Gain and accuracy

The ideal range of gain set in Section 4.1 is $[2M, 20G]\ V/A$. However, it is reasonable to set the operating range at $[2M, 1G]\ V/A$ considering the limitations in bandwidth and stability. This range is enough to record the smallest expected electrode currents ($100\ pA$). However, the reduction in the range of gains leaves less margin against an under-performing electrode.

Regarding the gain's accuracy, as mentioned before, it is not limited by the controller but by the pseudo-resistor. The PVT and mismatch of the pseudo-resistor set the variability of the TIA gain. A Monte Carlo analysis can be performed to obtain the statistical parameters. For low gains the variation is low (e.g. $\sigma/\mu = 0.06@gain = 2\ MV/A$), while for medium gains it increases (e.g. $\sigma/\mu = 0.42@gain = 200\ MV/A$), and even more for large gains (e.g. $\sigma/\mu = 0.54@gain = 20\ GV/A$). This variability is another reason to discard gains over $1\ GV/A$. The Monte Carlo graph for medium gains is shown in Fig. 5.5 as an example.

The AC gain of the whole amplifier, from source to load, is shown in Fig. 5.4 (b). As expected, there is a low pass filter effect due to the source impedance, which would make it challenging to record membrane oscillations considering the typical frequencies stated in Section 2.1. To remove those

effects, a positive feedback compensation as used in patch-clamp could be used. The AP's can be recorded without trouble.

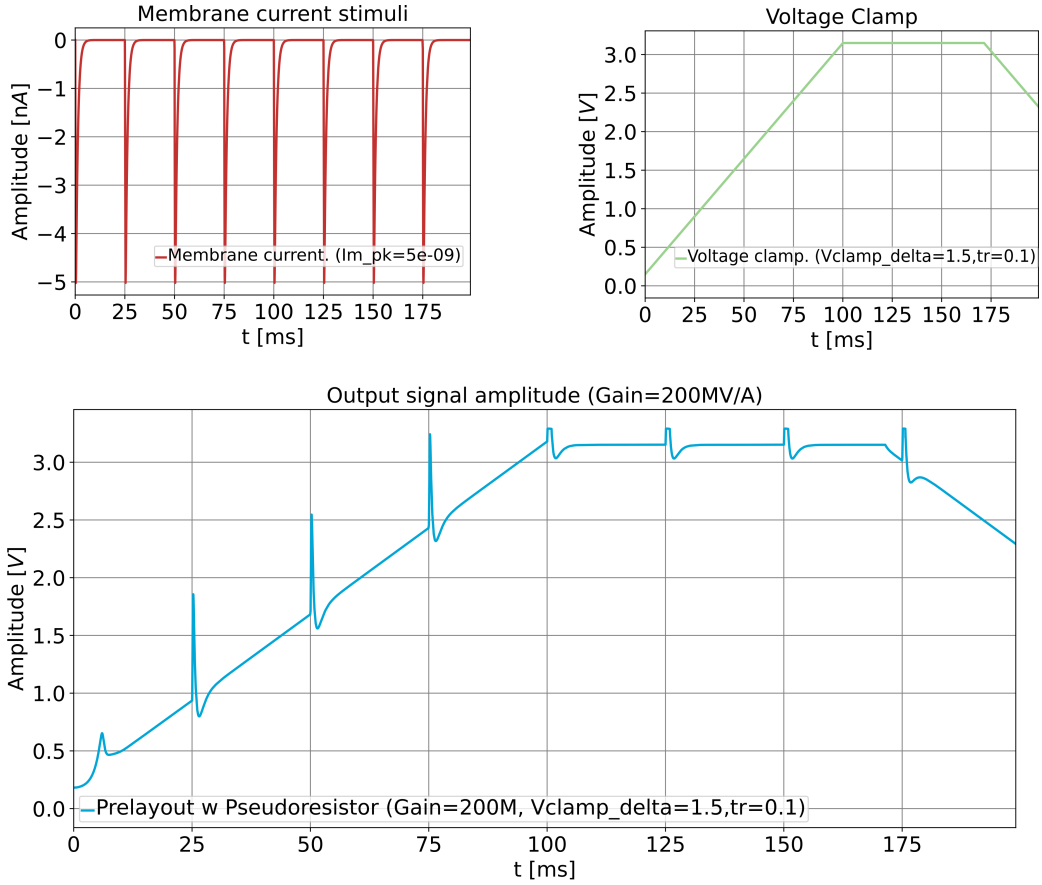


Figure 5.3: The membrane current stimuli signal (red) simulates currents through the membrane during action potentials based on the equations in [5]. The voltage clamp signal (green) sweeps all the input voltage range $[0.9, 3.16]\ V$. If the current source I_m and the voltage source V_{clamp} in Fig.4.1 generate those two signals, the voltage in V_o is the output signal amplitude (cyan). The amplifier in this case is stable, provides the expected amplification of the membrane current ($gain = 200\ MV/A$), and follows the voltage clamp.

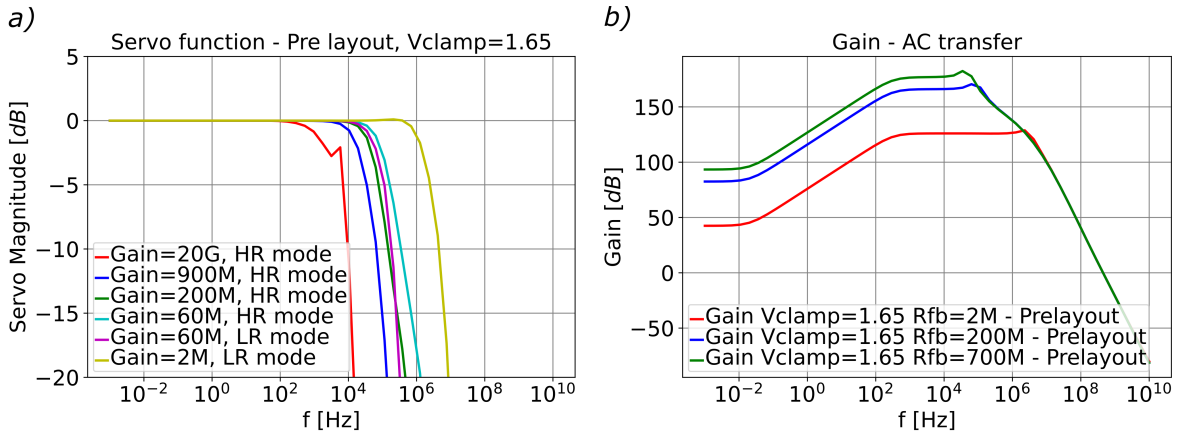


Figure 5.4: a) Servo function of the amplifier. For $gain > 1\ GV/A$ the bandwidth limit is below $10\ kHz$. b) AC gain of the amplifier from I_m to V_o. The amplifier can process AP's. The high-pass effect of the source should be compensated if the signals below $100\ Hz$ are relevant.

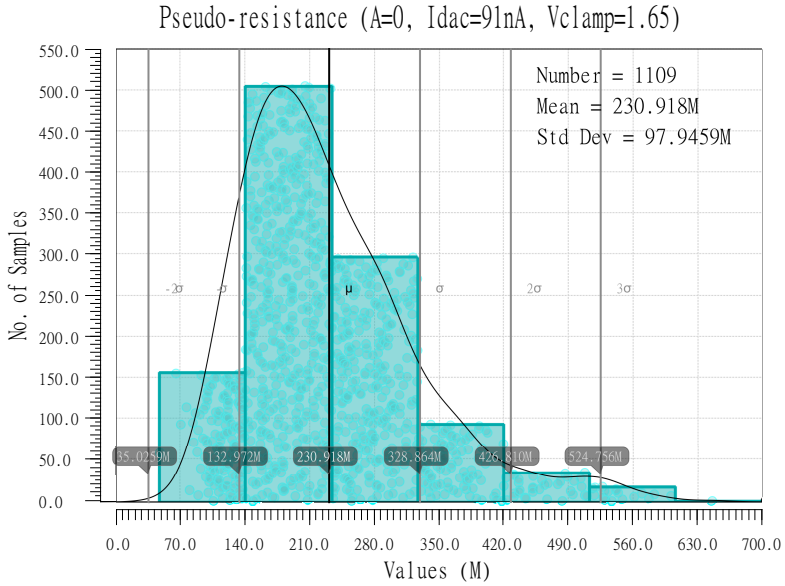


Figure 5.5: Example of the Monte Carlo simulation to model the PVT and mismatch of the pseudo-resistor and the TIA. $\sigma/\mu = 0.42$.

Other parameters

The power consumption is estimated at $49.1\ \mu W$: $40\ \mu W$ in the controller and $9.1\ \mu W$ in the pseudo-resistor (for mid-gains). As expected, the power consumption of the pseudo-resistor is lower than the controller, which was one of the reasons why passive feedback was chosen.

The PSRR depends on the amplifier's gain and the frequency, as shown in Fig. 5.6.

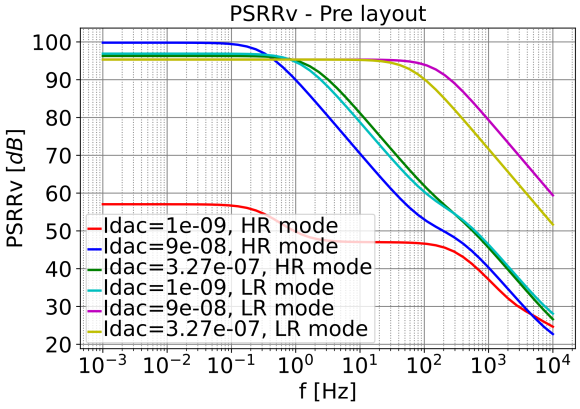


Figure 5.6: Voltage clamp referred PSRR (PSRRv). The PSRRv is defined as the ratio between the change in power supply voltage and the voltage clamp change that needs to be applied to compensate this effect [40].

As additional testing, the amplifier's stability was verified with no neuron on top of the electrode. The results were also verified for temperatures between 30-40ºC. There were no significant changes in any of those tests.

5.2. Post-layout

In this section, the results of the post-layout simulation of the whole system (source + load + controller + pseudo-resistor) are presented. The results related to the system requirements are highlighted and compared to the pre-layout simulations.

Input and output voltage ranges

The input range voltage is $V_{in} \in (0.92, 3.16)\ V$ and the output voltage range $V_{out} \in (0.5, 3.16)\ V$. The results do not vary much in respect to the pre-layout results.

Noise

The noise spectrum for $gain = 200\ MV/A$ is shown in Fig. 5.7 as an example. It is very close to the pre-layout spectrum. The output referred RMS noise ($DC - 10\ kHz$) is also shown in Fig.5.7. The RMS values for gains $2\ M$, $200\ M$, and $1\ GV/A$ are 0.025, 0.095, and $0.41\ mV_{rms}$. These values are minimally larger than in the pre-layout simulations, and they satisfy the target of $0.56\ mV_{rms}$.

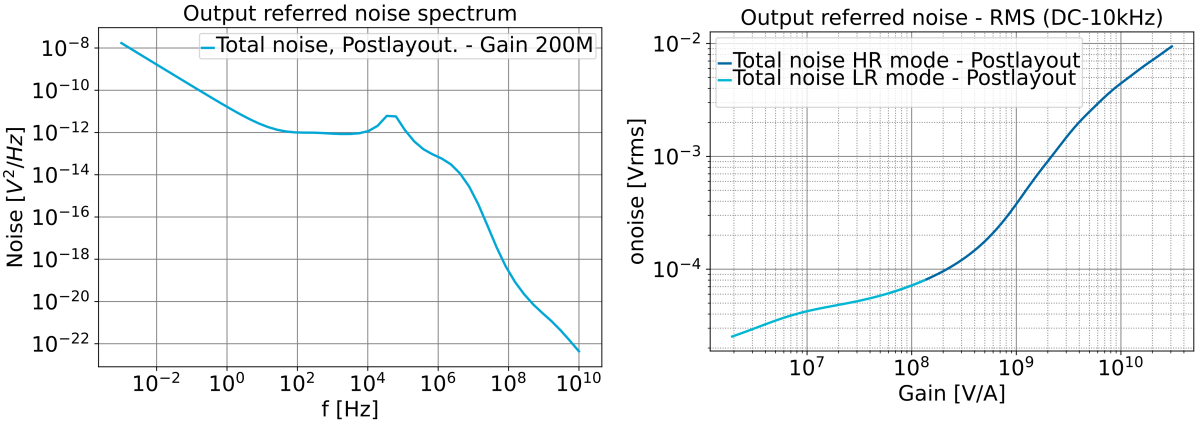


Figure 5.7: Noise spectrum for $gain = 200\ MV/A$ and output referred RMS noise versus gain in post-layout simulations. In the spectrum between $10\ Hz$ to $10\ kHz$, the noise coming from the pseudo-resistor is dominant and flat around $4kT gain$. For lower frequencies, the controller's pink noise dominates. For higher frequencies, the controller's blue noise dominates, but the noise power density decreases out of the amplifier's bandwidth. The RMS values for gains $2\ M$ and $1\ GV/A$ are 0.025 and $0.41\ mV_{rms}$.

Bandwidth and stability

As explained in Section 5.1, the performance in terms of stability becomes much worse when the pseudo-resistor is used. This performance degradation is even more severe in the post-layout simulations. It is so severe that the amplifier becomes unstable. The loop gain is shown in Fig. 5.8. The bandwidth slightly decreases compared to the pre-layout simulations.

The hypothesis to explain the stability degradation is that the pseudo-resistor is likely also becoming a delay. As it can be seen in Fig. 4.43, the parasitics in between the pseudo-resistance cells form a structure that is very similar to the Elmore delay diagram [46]. A delay tends to deteriorate the phase of the loop gain as it happens in this system [38].

Gain and accuracy

The post-layout Monte Carlo σ/μ ratios are the same as in the pre-layout. The AC gain is also the same. The graphs are not displayed to avoid redundancy.

Area

The total area is $0.0092\ mm^2$, of which $0.0072\ mm^2$ are used by the pseudo-resistor and $0.0020\ mm^2$ by the controller. As it was mentioned in Section 4.4.2, the initial hypothesis was that passive feedback would save up space, which is not true in this case.

Other parameters

The PSRR also degrades after the layout, as it can be seen in Fig. 5.9.

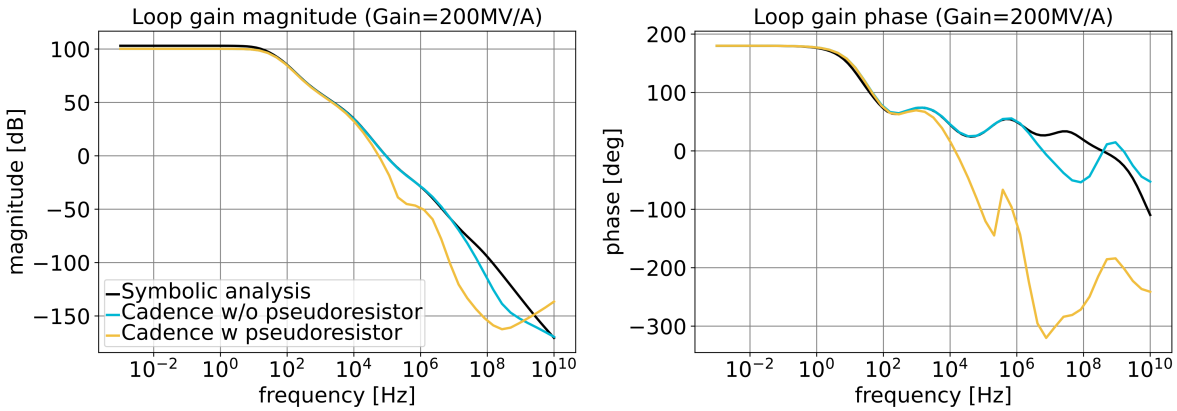


Figure 5.8: Loop gain of the system after layout using an ideal resistor and a pseudo-resistor. The loop gain obtained in the symbolic analysis is left as a reference. When a pseudo-resistor is used, the loop gain phase decreases significantly near the amplifier's bandwidth limit ($\approx 0.1\ MHz$), reducing stability margins. The effect is more severe in the post-layout simulations than in pre-layout (Fig.5.2), causing instability.

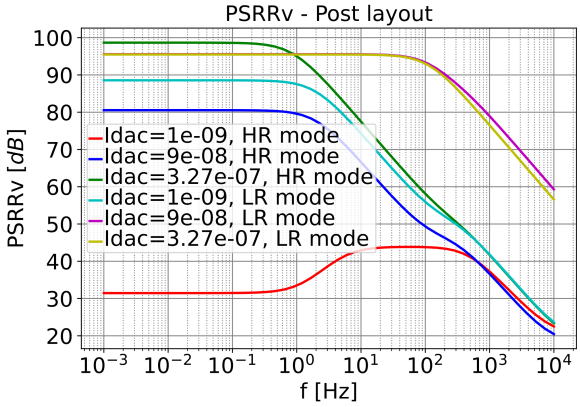


Figure 5.9: PSRRv of the amplifier after layout. The PSRRv at DC is lower than in the pre-layout simulations.

5.3. Summary

Table 5.1: Summary of the system requirements and the simulation results.

Parameter	**Target**	**Simulation**
Input voltage range	At least $[1, 2.3]\ V$	$[0.9, 3.16]\ V$
Output voltage range	Close to $[0, 3.3]\ V$	$[0.5, 3.16]\ V$
Output referred noise (RMS)	Around $0.56\ mV_{rms}$	$0.025\ mV_{rms}$@$2\ MV/A$ $0.095\ mV_{rms}$@$200\ MV/A$ $0.41\ mV_{rms}$@$1\ GV/A$
Gain	Ideally $[2\ M, 20\ G]V$	$[2\ M, 1\ G]\ V$ $\sigma/\mu = 0.41$@$200\ MV/A$
Bandwidth	$DC - 10\ kHz$	$DC - 10\ kHz@gain < 1\ GV/A$
Stability		Prelayout: Stable (@gains<1 GV/A) Postlayout: Not stable
Power		$49.1\ \mu W/pixel$
Area		$0.0092\ mm^2/pixel$

6

Discussion

6.1. Conclusions

In this project, a pseudo voltage clamp for a CMOS-based mesoscale neural interface for intracellular recording and stimulation has been designed.

The noise performance has been optimized using symbolic analysis. This analysis allowed not only to have an amplifier whose noise is very close to the minimum possible in this process but also avoided oversizing the input stage. Additionally, symbolic equations have been used to understand the shape of the noise spectrum.

The voltage swing has been a priority design parameter when sizing the transistors on both amplifier stages. The saturation voltages of the transistors limit the input and output voltage ranges, but the minimum output voltage is also limited by the biasing of the pseudo-resistor.

The amplifier occupies a small area compared to other devices in the literature, making it easy to integrate them into the pixels of the nanoelectrode array. However, most of the area is used by the pseudo-resistor, which contradicts the initial hypothesis that the passive feedback is more efficient in terms of area.

The amplifier has enough bandwidth to record APs for any gain. Recording high-frequency signals close to $10\ kHz$ is not possible for very large gains, while the effect of the electrode might restrict recordings below $100\ Hz$. These limitations must be re-assessed after the electrodes are characterized. If membrane oscillations and PSPs are relevant, including compensation techniques as in patch-clamps would probably be necessary.

The stability of the amplifier is the biggest issue. The device is stable with ideal resistive feedback, but using a standard resistor is not possible due to the large resistance values that it needs to generate. A pseudo-resistor is used to achieve those values. This pseudo-resistor degrades the stability performance. In pre-layout simulations, the amplifier is still stable but not for huge gains. However, in post-layout simulations, the stability margins fade away, and the amplifier becomes unstable. The hypothesis is that the pseudo-resistor introduces a delay in the feedback network.

The final gain range is established considering the bandwidth and stability limitations when using a pseudo-resistor. This range has been reduced compared to the initial target. However, the gain range can still deal with all the expected currents in the electrode but leave less margin. The margin intends to protect from a poor electrode performance, so there is less room for performance loss in the electrode.

The amplifier's power consumption is slightly less than in other devices in the literature. In this case, passive feedback, which is supposed to be more efficient in power consumption, satisfies the initial expectations. The pseudo-resistor consumes about 20% of the power of the device.

The design steps have been implemented in SLiCAP-Python scripts to make the design adaptable to future modifications. These scripts are semi-automatized because they require the user to modify some code elements after each adjustment manually. However, they significantly speed up readjustments and probably make the design process more transparent to other researchers. The scripts use a simplified EKV model of the process based on just 12 parameters (4 of them default CMOS18). This model has been proven accurate enough for design purposes, so it can be reused in future projects in the lab.

6.2. Future research

There are several suggestions for improvement that can be applied in future research.

Regarding the noise design, as it was mentioned in Section 4.2.2, it was studied whether it was better to have a PMOS or an NMOS input stage. The conclusion was that both were equivalent. However, at the time when that decision was made, the noise was not completely modeled since K_F was the default for CMOS18 and A_F was not modeled in SLiCAP. It would be interesting to re-assess the suitability of the PMOS input stage re-running the script with updated parameters.

Regarding the output voltage limitation due to the biasing of the pseudo-resistor, it could be improved by increasing the pseudo-resistance transistors' width because this change would make V_c smaller. As a reminder, the minimum voltage between the two transistors $M_{pr,t}$ and $M_{pr,b}$ needs to be greater than $V_c + V_{sat,cs}$ as explained in Section 4.3.3, so the smaller the V_c the better. However, as it was mentioned in Section 4.3.2 that would make it very difficult to control the value of the pseudo-resistance because the V_c values for the largest and smallest resistances would be too close. An alternative biasing for the pseudo-resistors could be proposed to be able to handle very little V_c. Additionally, as it was mentioned in Section 4.3.2, the biasing of the pseudo resistor could be improved to be less affected by PVT and mismatch. According to [21], an option could be using trans-diodes at the cost of noise, complexity and area.

Regarding the area, it would be possible to save around 9% by reallocating all the biasing devices of the pseudo-resistor in the same NWELL island in the middle of the layout, as shown in Fig.6.1.

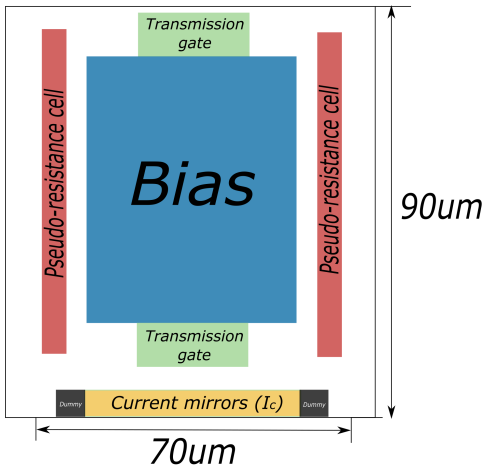


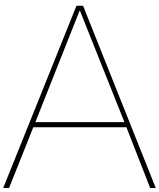
Figure 6.1: Proposed layout structure of the pseudo-resistor to save 9% of the total area.

Regarding stability, there are two primary modifications in the design that can help to improve the performance. One of them involves the controller, while the other one is about the feedback network.

On the one hand, it would be worth considering a single-stage controller design, which is usually more stable. The second stage was introduced because the bandwidth of a single-stage design was not enough for higher gains. Nevertheless, the frequency compensation of the two-stage design has made the bandwidth to be limited, too. Besides, the pseudo-resistor also introduces limitations in the bandwidth. A single-stage would reduce the loop gain, but the pseudo-resistance, not the controller, limits the accuracy, so this would not be an issue. The price to pay with a single-stage would be that the output voltage range cannot be optimized as well as with two stages, in which the second stage focuses on this particular aspect.

On the other hand, it would be necessary to reduce the delay effect of the feedback network if the hypothesis regarding the Elmore delay is true. An option could be reducing the number of pseudo-resistance cells in series. However, that would decrease the linearity and would limit the voltage swing across the feedback. If the linearity improves, it might be possible to use fewer devices in series. It could be interesting to study if using NMOS devices in the pseudo-resistance cells might help to reduce the leakage current through the parasitic PN junctions when fixing a common-mode voltage into both the DNWELL and PWELL.

If those options do not improve the stability, active feedback such as a gm-cell should be considered.



Supplementary materials

All the traces represented in the graphs in this report come from databases stored as comma-separated values (CSV) with simulation results. Those files are available in the lab's Wiki and upon request.

The scripts that were used to generate the results of this project are published in `https://github.com/aitordelrivero/MScThesisAdRC_Annex`. The instructions to install SLiCAP and run the scripts are available in the README. This thesis report includes flow diagrams with different shapes and tables that explain the workflow of the scripts in the following pages.

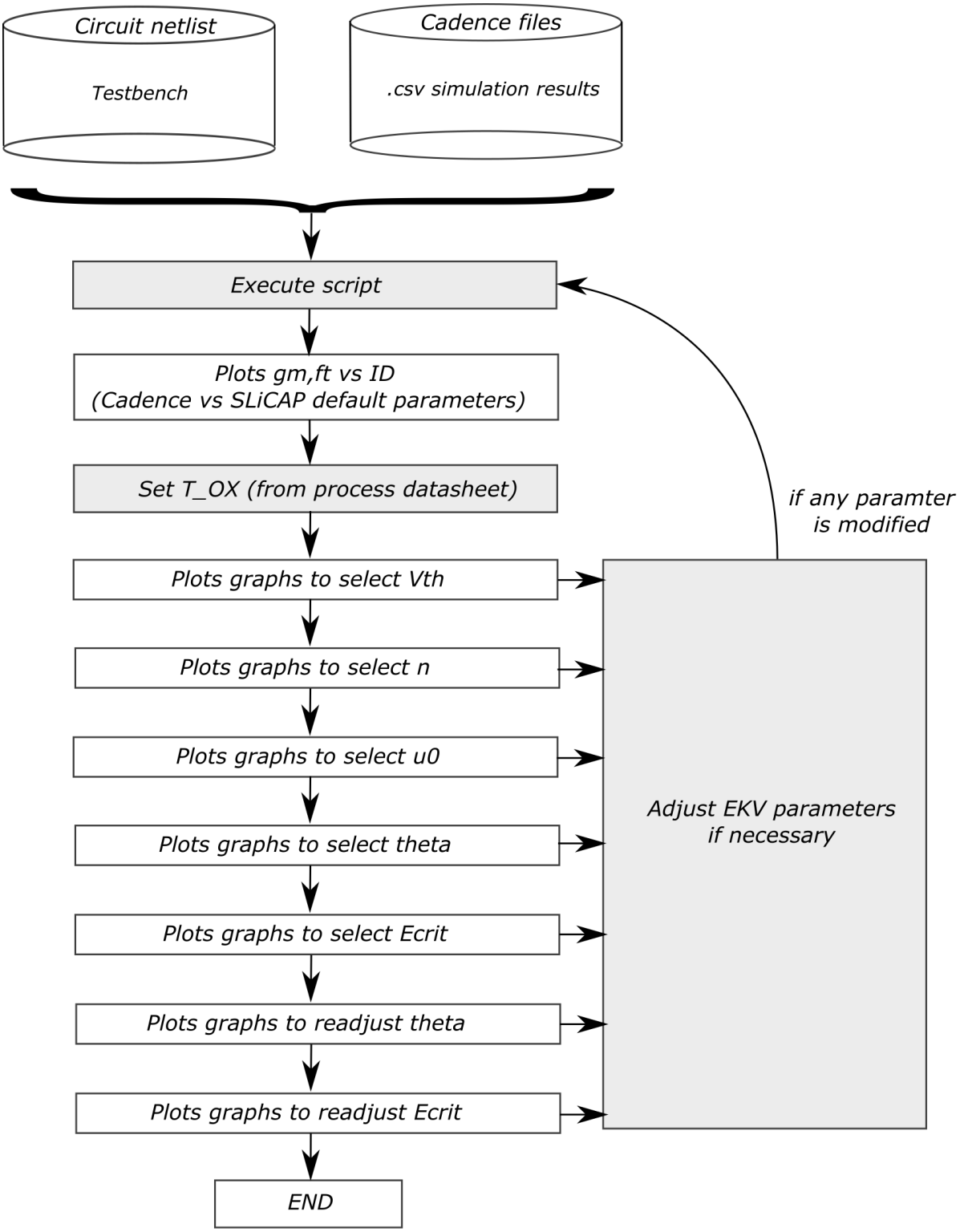
The cylinders represent data from external files that are used by the script to generate the results. This external information includes process parameters, circuit netlists, execution parameters given by the user, specifications of the system, and Cadence simulation results.

The variables of the script are summarized in a table on top of the diagrams. On the one hand, the variables unknown before the first execution and discovered or updated during the execution are highlighted in bold. On the other hand, the known variables have a tag indicating where their value was obtained.

If the script can be executed using different netlists, a summary table explains what variable can be discovered or updated with each netlist. Besides, it also specifies the variables that should have been obtained before executing the script with that netlist.

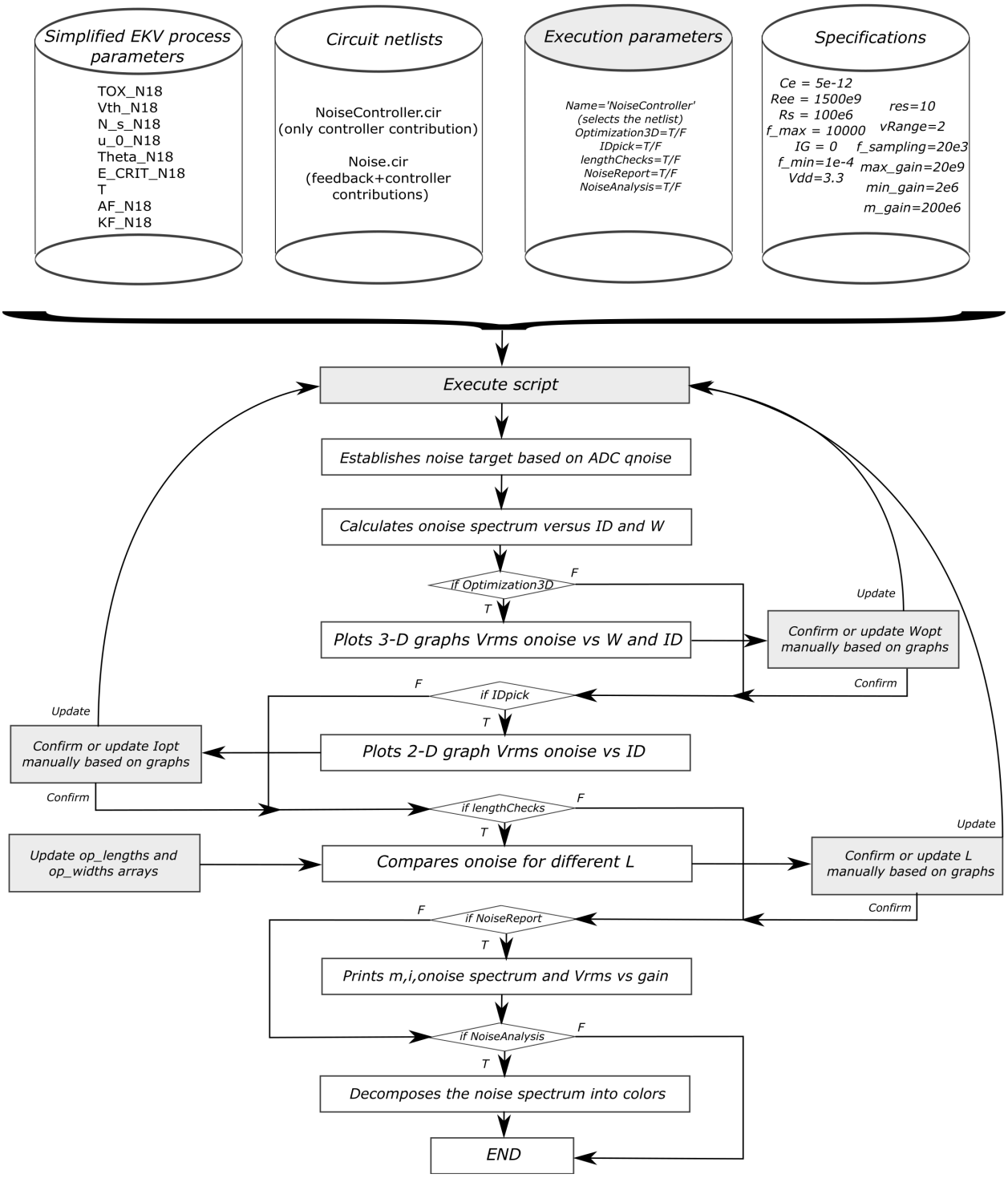
The shapes with a gray background indicate that the user needs to intervene.

A.1. Script - EKV adjustment



A.2. Script - Noise study

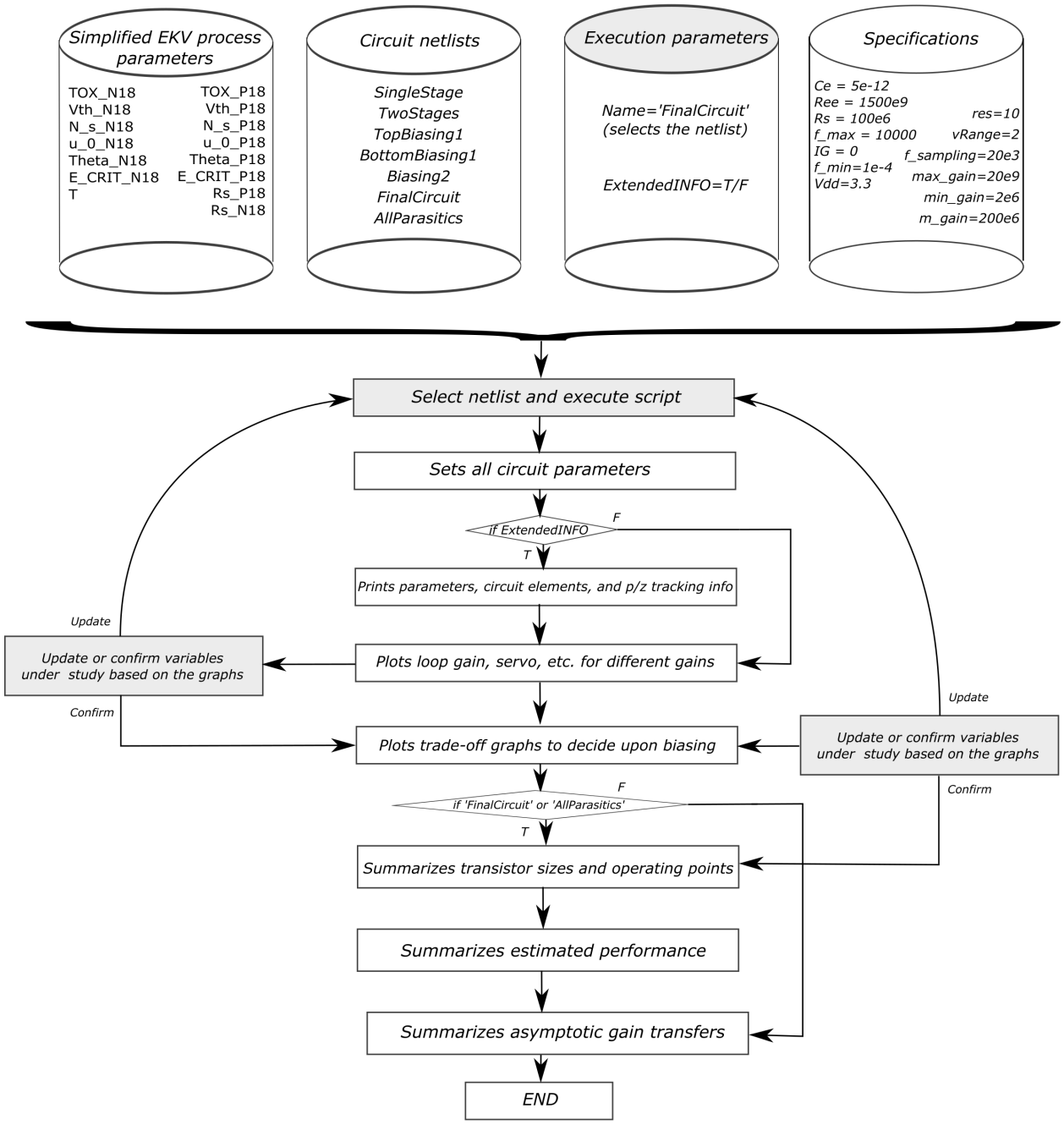
VARIABLE	VALUE	SOURCE
Wopt	**30u**	
lopt	**2u**	
L	**2u**	
NEF	1.25	Stages script



A.3. Script - Stages study

VARIABLE	VALUE	SOURCE	VARIABLE	VALUE	SOURCE
Wopt	30u	Noise script	Lbcm	**1.5u**	
L	2u	Noise script	Wb	**5u**	
Iopt	2u	Noise script	Lb	**1.5u**	
IDout	5u	Driving req.	Rps	200k	FreqComp script
Wout	**5u**		Cps	5p	FreqComp script
Lout	**350n**		Rph	4k	FreqComp script
Lcm	**5u**		CparX	10.5f	Cadence
Wcm	**7.5u**		CparC	25.0f	Cadence
Wbcm	**8u**		CparY	29.7f	Cadence

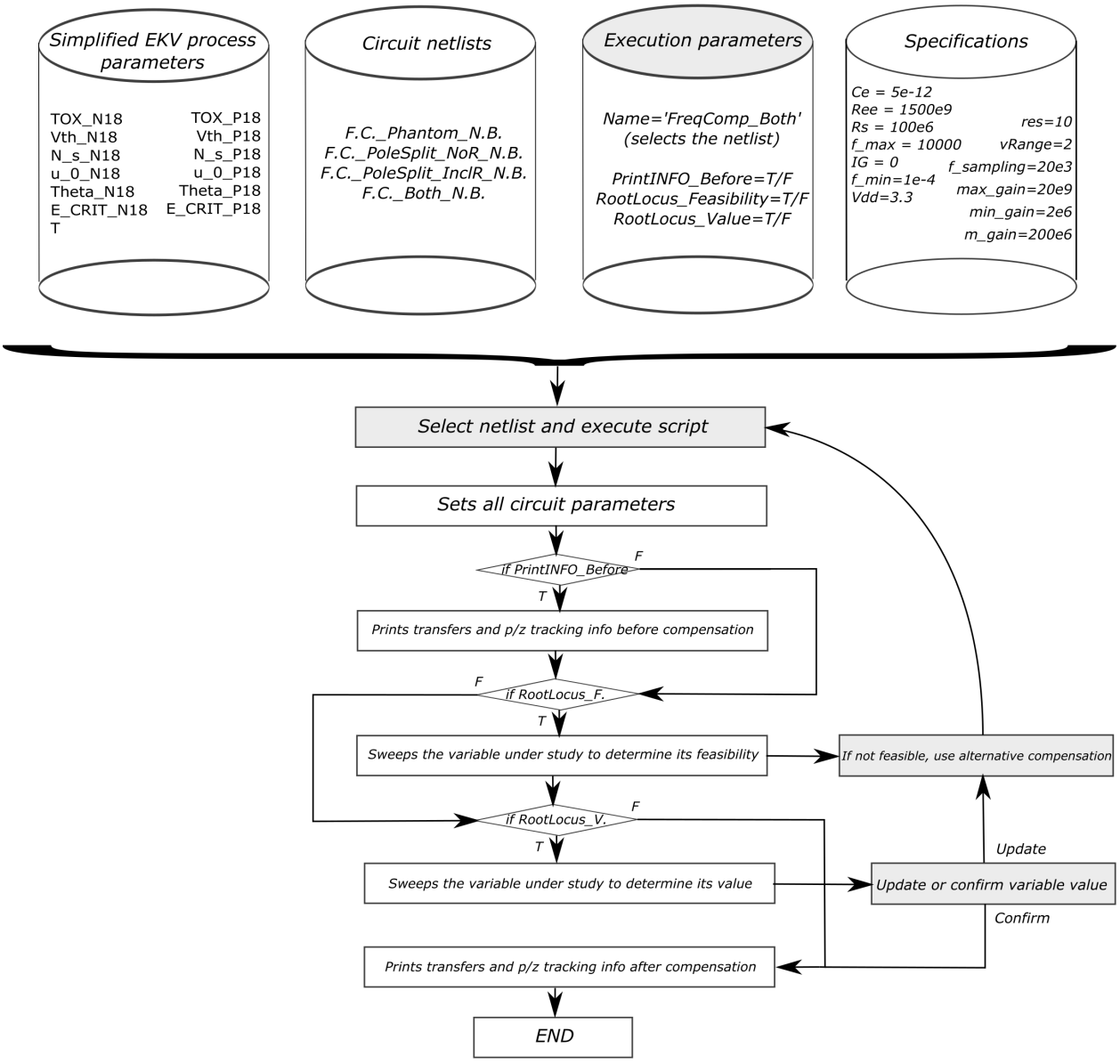
NETLIST	SETS	NEEDS
SingleStage		Wopt, L, Iopt
TwoStages	Wout, Lout	Wopt, L, Iopt
TopBiasing1	Wcm, Lcm	Wopt, L, Iopt
BottomBiasing1	Wbcm, Lbcm	Wopt, L, Iopt
Biasing2	Wb,Lb	Wopt, L, Iopt,Wout, Lout
FinalCircuit		All variables but Cpar_
AllParasitics		All variables



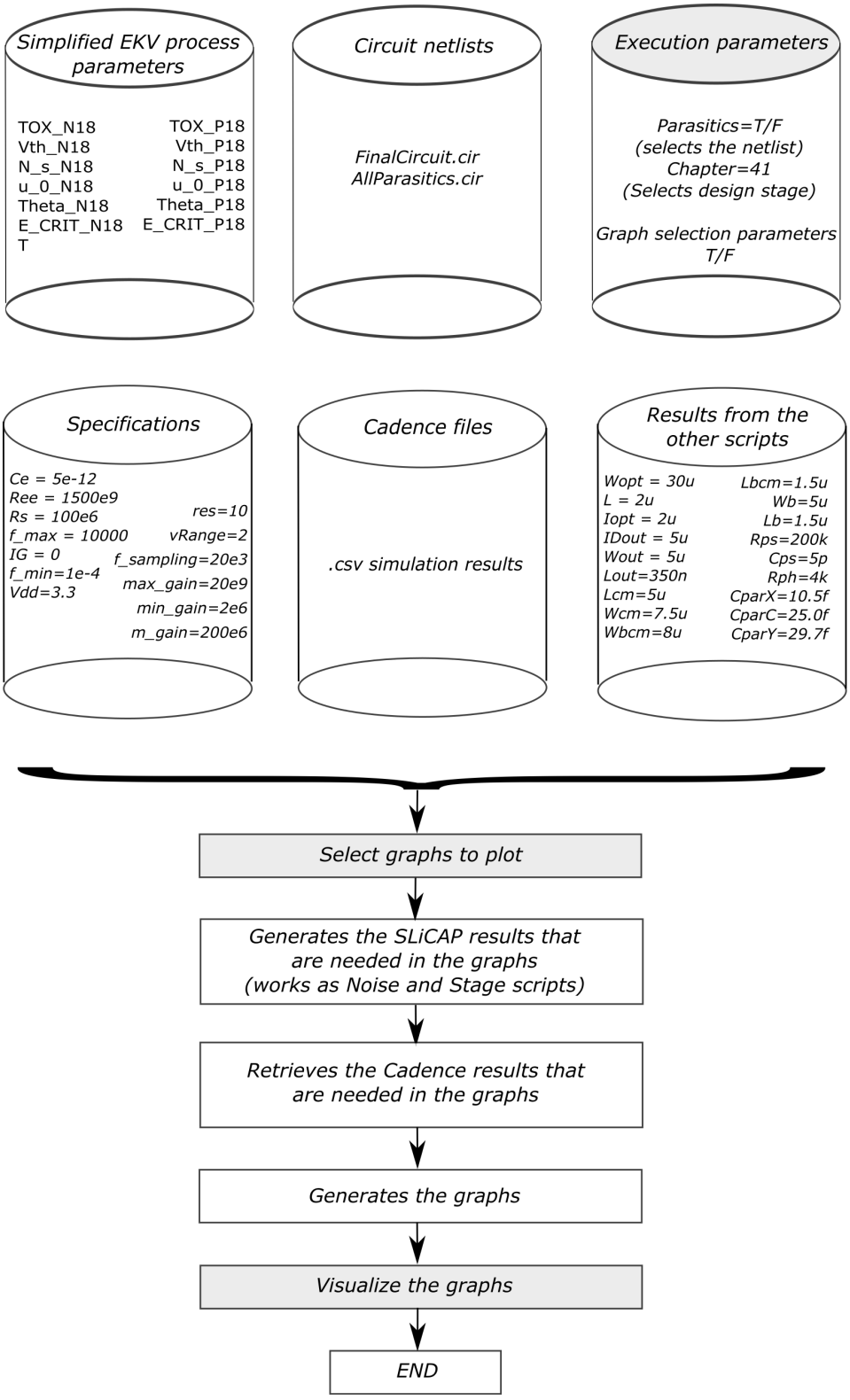
A.4. Script - Frequency compensation study

VARIABLE	VALUE	SOURCE	VARIABLE	VALUE	SOURCE
Wopt	30u	Noise script	Lbcm	1.5u	Stages script
L	2u	Noise script	Wb	5u	Stages script
Iopt	2u	Noise script	Lb	1.5u	Stages script
IDout	5u	Driving req.	Rps	**200k**	
Wout	5u	Stages script	Cps	**5p**	
Lout	350n	Stages script	Rph	**4k**	
Lcm	5u	Stages script	CparX	10.5f	Cadence
Wcm	7.5u	Stages script	CparC	25.0f	Cadence
Wbcm	8u	Stages script	CparY	29.7f	Cadence

NETLIST	SETS	NEEDS
FreqComp_Phantom_NoBias	Rph	Wopt, L, Iopt, IDout, Wout, Lout
FreqComp_PoleSplit_NoR_NoBias	Cps	Wopt, L, Iopt, IDout, Wout, Lout
FreqComp_PoleSplit_InclR_NoBias	Rps	Cps,Wopt, L, Iopt, IDout, Wout, Lout
FreqComp_Both_NoBias	Rph	Cps, Rps, Wopt, L, Iopt, IDout, Wout, Lout
FreqComp_Both		All variables but Cpar_



A.5. Script - Data visualization



Bibliography

[1] J. Abbott, T. Ye, D. Ham, and H. Park. Optimizing nanoelectrode arrays for scalable intracellular electrophysiology. *Accounts of Chemical Research*, 51(3):600–608, 2018.

[2] J. Abbott, T. Ye, K. Krenek, R.S. Gertner, S. Ban, Y. Kim, L. Qin, W. Wu, H. Park, and D. Ham. A nanoelectrode array for obtaining intracellular recordings from thousands of connected neurons. *Nature Biomedical Engineering*, 4(2):232–241, 2020.

[3] J. Abbott, T. Ye, K. Krenek, L. Qin, Y. Kim, W. Wu, R. S. Gertner, H. Park, and D. Ham. The design of a cmos nanoelectrode array with 4096 current-clamp/voltage-clamp amplifiers for intracellular recording/stimulation of mammalian neurons. *IEEE Journal of Solid-State Circuits*, 55(9):2567–2582, 2020.

[4] M. Ballini, J. Müller, P. Livi, Y. Chen, U. Frey, A. Stettler, A. Shadmani, V. Viswam, I. L. Jones, D. Jäckel, M. Radivojevic, M. K. Lewandowska, W. Gong, M. Fiscella, D. J. Bakkum, F. Heer, and A. Hierlemann. A 1024-channel cmos microelectrode array with 26,400 electrodes for recording and stimulation of electrogenic cells in vitro. *IEEE Journal of Solid-State Circuits*, 49(11):2705–2719, 2014.

[5] G. Baranauskas. Ionic channel function in action potential generation: Current perspective. *Molecular Neurobiology*, 35(2):129–150, 2007. ISSN 1559-1182.

[6] L. Berdondini, P. D. Van Der Wal, O. Guenat, N. F. De Rooij, M. Koudelka-Hep, P. Seitz, R. Kaufmann, P. Metzler, N. Blanc, and S. Rohr. High-density electrode array for imaging in vitro electrophysiological activity. *Biosensors and Bioelectronics*, 21(1):167–174, 2005.

[7] G. Bertotti, D. Velychko, N. Dodel, S. Keil, D. Wolansky, B. Tillak, M. Schreiter, A. Grall, P. Jesinger, S. Röhler, M. Eickenscheidt, A. Stett, A. Möller, K. Boven, G. Zeck, and R. Thewes. A cmos-based sensor array for in-vitro neural tissue interfacing with 4225 recording sites and 1024 stimulation sites. In *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, pages 304–307, 2014.

[8] F. Bezanilla. Voltage-gated ion channels. *IEEE Transactions on NanoBioscience*, 4(1):34–48, 2005.

[9] N. Bhadra and T. Vrabec. *Chapter 10 - Electrodes for electrical conduction block of the peripheral nerve*, pages 215–229. William Andrew Publishing, Oxford, 2015. ISBN 978-0-323-26208-8.

[10] D. Binkley. *Tradeoffs and Optimization in Analog CMOS Design*. Wiley, 2008. ISBN 9780470033692.

[11] M. Bucher, C. Lallement, C. Enz, F. Theodoloz, and F. Krummenacher. The epfl-ekv mosfet model equations for simulation. *Version 2.6*, 1998.

[12] K. Bult and G.J.G.M. Geelen. An inherently linear and compact most-only current division technique. *IEEE Journal of Solid-State Circuits*, 27(12):1730–1735, 1992.

[13] T. Carusone, D. Johns, and K. Martin. *Analog Integrated Circuit Design, 2nd Edition*. John Wiley Sons, 2011.

[14] B. X. E. Desbiolles, E. de Coulon, A. Bertsch, S. Rohr, and P. Renaud. Intracellular recording of cardiomyocyte action potentials with nanopatterned volcano-shaped microelectrode arrays. *Nano Letters*, 19(9):6173–6181, 2019.

[15] M. Dipalo, H. Amin, L. Lovato, F. Moia, V. Caprettini, G. C. Messina, F. Tantussi, L. Berdondini, and F. De Angelis. Intracellular and extracellular recording of spontaneous action potentials in mammalian neurons and cardiac cells with 3d plasmonic nanoelectrodes. *Nano Letters*, 17(6): 3932–3939, 2017.

[16] M. Dipalo, G. Melle, L. Lovato, A. Jacassi, F. Santoro, V. Caprettini, A. Schirato, A. Alabastri, D. Garoli, G. Bruno, F. Tantussi, and F. De Angelis. Plasmonic meta-electrodes allow intracellular recordings at network level on high-density cmos-multi-electrode arrays. *Nature Nanotechnology*, 13(10):965–971, 2018.

[17] J. Dragas, V. Viswam, A. Shadmani, Y. Chen, R. Bounik, A. Stettler, M. Radivojevic, S. Geissler, M.E.J. Obien, J. Muller, and A. Hierlemann. In vitro multi-functional microelectrode array featuring 59760 electrodes, 2048 electrophysiology channels, stimulation, impedance measurement, and neurotransmitter detection channels. *IEEE Journal of Solid-State Circuits*, pages 1–15, 2017.

[18] U. Frey, J. Sedivy, F. Heer, R. Pedron, M. Ballini, J. Mueller, D. Bakkum, S. Hafizovic, F. D. Faraci, F. Greve, K. Kirstein, and A. Hierlemann. Switch-matrix-based high-density microelectrode array in cmos technology. *IEEE Journal of Solid-State Circuits*, 45(2):467–482, 2010.

[19] C. Galup-Montoro and M. C. Schneider, editors. *CMOS technology, components, and layout techniques*, pages 88–133. Cambridge University Press, Cambridge, 2010. ISBN 9780521110365.

[20] W. Grabinski. Ekv v2.6 parameter extraction tutorial. In *ICCAP Users' Conference, Berlin*, 2002.

[21] E. Guglielmi, F. Toso, F. Zanetto, G. Sciortino, A. Mesri, M. Sampietro, and G. Ferrari. High-value tunable pseudo-resistors design. *IEEE Journal of Solid-State Circuits*, 55(8):2094–2105, 2020.

[22] A. Hai, J. Shappir, and M. E. Spira. In-cell recordings by extracellular microelectrodes. *Nature Methods*, 7(3):200–202, 2010.

[23] C. M. Hammerschmied. *CMOS A/D converters using MOSFET-only R-2R ladders*. Thesis, 2000.

[24] A. Hierlemann, U. Frey, S. Hafizovic, and F. Heer. Growing cells atop microelectronic chips: Interfacing electrogenic cells in vitro with cmos-based microelectrode arrays. *Proceedings of the IEEE*, 99(2):252–284, 2011.

[25] A. L. Hodgkin and A. F. Huxley. A quantitative description of membrane current and its application to conduction and excitation in nerve. *The Journal of Physiology*, 117(4):500–544, 1952.

[26] P. Jespers. *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*. Springer Science Business Media, 2009. ISBN 0387471014.

[27] P. Jespers and B. Murmann. *Systematic Design of Analog CMOS Circuits*. Cambridge University Press, 2017.

[28] T. Jochum, T. Denison, and P. Wolf. Integrated circuit amplifiers for multi-electrode intracortical recording. *Journal of Neural Engineering*, 6(1):012001, 2009.

[29] S.J.D. Lawrence, E. Formisano, L. Muckli, and F.P. De Lange. Laminar fmri: Applications for cognitive neuroscience. *NeuroImage*, 197:785–791, 2019.

[30] K. Lee, I. Kim, S. Kim, D. Jeong, J. Kim, H. Rhim, J. Ahn, S. Park, and H. Choi. Vertical nanowire probes for intracellular signaling of living cells. *Nanoscale Research Letters*, 9(1):56, 2014.

[31] A.L. Lehninger, D.L. Nelson, and M.M. Cox. *Lehninger Principles of Biochemistry*. W. H. Freeman, 2005. ISBN 9780716743392.

[32] Z. C. Lin, A. F. McGuire, P. W. Burridge, E. Matsa, H. Lou, J. C. Wu, and B. Cui. Accurate nanoelectrode recording of human pluripotent stem cell-derived cardiomyocytes for assaying drugs and modeling disease. *Microsystems Nanoengineering*, 3(1):16080, 2017.

[33] R. Liu, R. Chen, A. T. Elthakeb, S. H. Lee, S. Hinckley, M. L. Khraiche, J. Scott, D. Pre, Y. Hwang, A. Tanaka, Y. G. Ro, A. K. Matsushita, X. Dai, C. Soci, S. Biesmans, A. James, J. Nogan, K. L. Jungjohann, D. V. Pete, D. B. Webb, Y. Zou, A. G. Bang, and S. A. Dayeh. High density individually addressable nanowire arrays record intracellular activity from primary rodent and human stem cell derived neurons. *Nano Letters*, 17(5):2757–2764, 2017.

[34] C. M. Lopez, H. S. Chun, S. Wang, L. Berti, J. Putzeys, C. Van Den Bulcke, J. Weijers, A. Firrincieli, V. Reumers, D. Braeken, and N. Van Helleputte. A multimodal cmos mea for high-throughput intracellular action potential measurements and impedance spectroscopy in drug-screening applications. *IEEE Journal of Solid-State Circuits*, 53(11):3076–3086, 2018.

[35] J. Malmivuo and R. Plonsey. *Bioelectromagnetism - Principles and Applications of Bioelectric and Biomagnetic Fields*. Bioelectromagnetism: Principles and Applications of Bioelectric and Biomagnetic Fields. 1995. ISBN 978-0195058239.

[36] R.D. Middlebrook. The general feedback theorem: a final solution for feedback systems. *IEEE Microwave Magazine*, 7(2):50–63, 2006.

[37] R.D. Middlebrook. General feedback theorem and asymptotic gain model. 2008. URL `https://web.archive.org/web/20121025134918/http:/groups.yahoo.com/group/Design-Oriented_Analysis_D-OA/message/146`.

[38] L. Mirkin and Z. J. Palmor. *Control issues in systems with loop delays*, pages 627–648. Springer, 2005.

[39] MDS Molecular Devices. The axon guide, a guide to electrophysiology and biophysics laboratory techniques. Report, Technical Report, Analytical Technologies, 2008.

[40] A.J.M. Montagne. *Structured Electronic Design*. Delft Academic Press, 2018. ISBN 9789065624277.

[41] A.J.M. Montagne. Slicap: Symbolic linear circuit analysis program, 2018. URL `https://github.com/Lenty/SLiCAP_python`.

[42] A. Obaid, M. Hanna, Y. Wu, M. Kollo, R. Racz, M. R. Angle, J. Müller, N. Brackbill, W. Wray, F. Franke, E. J. Chichilnisky, A. Hierlemann, J. B. Ding, A.T. Schaefer, and N.A. Melosh. Massively parallel microwire arrays integrated with cmos chips for neural recording. *Science Advances*, 6 (12):eaay2789, 2020.

[43] M. E. J. Obien, K. Deligkaris, T. Bullmann, D. J. Bakkum, and U. Frey. Revealing neuronal function through microelectrode array recordings. *Frontiers in neuroscience*, 8:423–423, 2015.

[44] D. L. Pulfrey. *Understanding Modern Transistors and Diodes*. Cambridge University Press, Cambridge, 2010. ISBN 9780521514606.

[45] D. Purves. *Neuroscience*. Oxford University Press, 2012. ISBN 9780878936953.

[46] J.M. Rabaey, A.P. Chandrakasan, and B. Nikolić. *Digital integrated circuits: a design perspective*, volume 7. Pearson education, Upper Saddle River, NJ, 2003.

[47] B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2016. ISBN 9780072524932.

[48] J.T. Robinson, M. Jorgolli, A.K. Shalek, M. Yoon, R.S. Gertner, and H. Park. Vertical nanowire electrode arrays as a scalable platform for intracellular interfacing to neuronal circuits. *Nature Nanotechnology*, 7(3):180–184, 2012.

[49] S. Shekar, K. Jayant, M.A. Rabadan, R. Tomer, R. Yuste, and K.L. Shepard. A miniaturized multiclamp cmos amplifier for intracellular neural recording. *Nature Electronics*, 2(8):343–350, 2019.

[50] Royal Society. *iHuman: blurring lines between mind and machine*. Royal Society, 2019. ISBN 1782524207.

[51] M.E. Spira and A. Hai. Multi-electrode array technologies for neuroscience and cardiology. *Nature Nanotechnology*, 8(2):83–94, 2013.

[52] M.S.J. Steyaert and W.M.C. Sansen. Power supply rejection ratio in operational transconductance amplifiers. *IEEE Transactions on Circuits and Systems*, 37(9):1077–1084, 1990.

[53] A. Tajalli and Y. Leblebici. *Extreme low-power mixed signal IC design: subthreshold source-coupled circuits*. Springer Science Business Media, 2010. ISBN 1441964789.

[54] B. Tian, T. Cohen-Karni, Q. Qing, X. Duan, P. Xie, and C.M. Lieber. Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. *Science*, 329(5993):830, 2010.

[55] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert. Striving for small-signal stability. *IEEE Circuits and Devices Magazine*, 17(1):31–41, 2001.

[56] C. Xie, Z. Lin, L. Hanson, Y. Cui, and B. Cui. Intracellular recording of action potentials by nanopillar electroporation. *Nature Nanotechnology*, 7(3):185–190, 2012.

[57] X. Yuan, V. Emmenegger, M. E. J. Obien, A. Hierlemann, and U. Frey. Dual-mode microelectrode array featuring 20k electrodes and high snr for extracellular recording of neural networks. In *2018 IEEE Biomedical Circuits and Systems Conference (BioCAS)*.

[58] R. Yuste and G. M. Church. The new century of the brain. *Scientific American*, 310(3):38–45, 2014.