Fully Integrated SAW-Less Discrete-Time Superheterodyne Receiver

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Fully Integrated SAW-Less Discrete-Time Superheterodyne Receiver

Proefschrift

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To my dear parents, MohammadReza and Fatemeh

To my dear sister, Sara and her respected family

To my dear sister, Setayesh

To all my family members in Iran

And last, but not least, to my lovely wife Reyhaneh and her respected family

Contents

CHAPTER

1

Introduction

Humans are social creatures who, by nature, like to communicate with each other. Communication can be defined as "Imparting or exchanging of information by speaking, writing, or using some other medium" [1]. People have employed various methods of communication, for instance, carrier pigeons, smoke signaling, drums, fire beacons, and the telegraph. In the past, they used speech for short-range, however, for very long distances, communication has changed dramatically throughout history.

In recent years, new media were invented that have changed the way people communicate in both wired and wireless forms. Currently, people use gadgets extensively in order to be continuously on-line, and they expect to be able to access all available information and to be connected with other people all over the world. To achieve this goal, wireless connectivity is used comprehensively.

Electromagnetism was discovered by Michael Faraday in 1831 which led to the formulation of Maxwell's Theory of wave propagation in 1873. The modern cellular transmitter-receiver (transceiver) has a long history since the first international radio transmission was demonstrated in 1886. The successful business story of high performance cellular devices teaches us that the need for extensive wireless connectivity can be addressed only if increasing wireless functionality is embedded into a single device. Hence, there is a need to support several wireless standards in multi-mode/multi-band transceivers such as Global System for Mobile Communication (GSM), Third Generation (3G) cellular using wideband code division multiple access (WCDMA), Fourth Generation (4G) cellular, Wi-Fi (IEEE 802.11), Bluetooth, and Global Positioning System (GPS). An example of one of the most successful gadgets, the mainboard of the iPhone 6, is illustrated in Fig. 1.1. It consists of multiple integrated circuits (IC) for different applications mounted on the same board including, for example, the processor unit, power amplifier (PA), LTE Modem, LTE PA+Duplexer, NFC module, NAND flash memory, Wi-Fi module, power management system and, most

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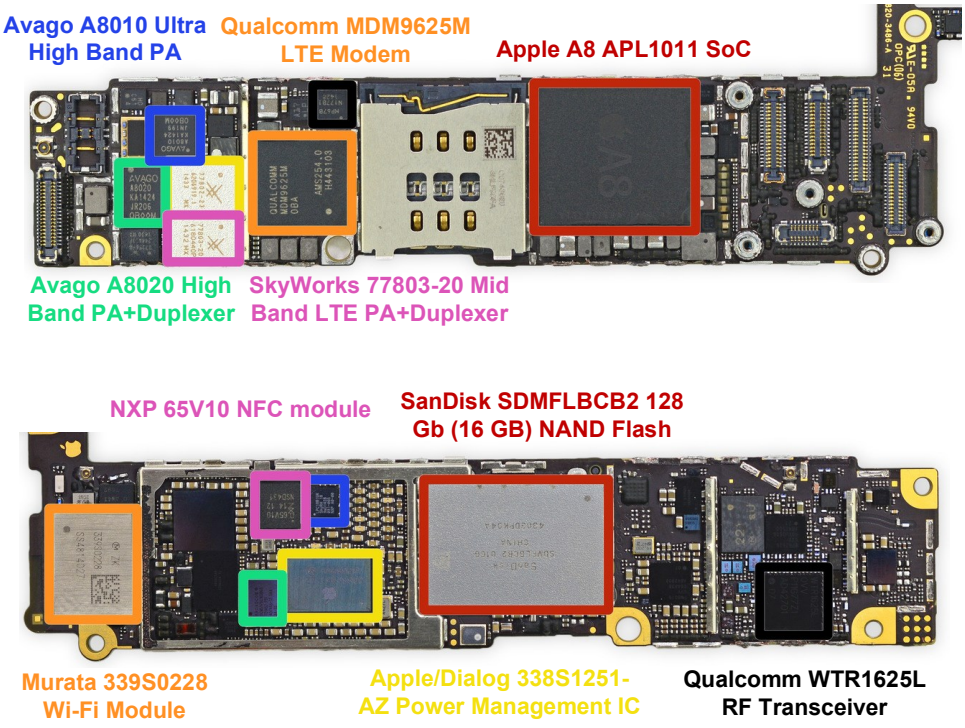

Figure 1.1: The front and back side of the iPhone-6 mainboard (Courtesy of Apple Inc.).

significantly, a radio-frequency (RF) transceiver. Each of the receiver modules in this mainboard contains surface acoustic wave (SAW) filters and switches, typically one per band, to attenuate out-of-band (OB) interferers before they reach the sensitive low-noise amplifier (LNA) input. To reduce cost and size of the total system-on-chip (SoC), in which the external antenna interface network is presently the greatest contributor, the recent trend is to eliminate these SAW filters and switches.

Consequently, there is a demand to have a high performance, low-power, low-area multi-mode/multi-band *fully* integrated SAW-less RF receiver which is capable of managing significant out-of-band interferers with to the eventual removal of SAW filters. RF receivers have conventionally used a zero/low intermediate frequency (IF) due to straightforward integration benefits of low-pass channel-select filtering and avoidance of images when zero-IF and their easy baseband filtering when low-IF [2–7]. However, there are many disadvantages associated with the zero-IF receiver, which are becoming ever more severe with CMOS scaling. These problems could be solved by increasing the IF frequency, as was the norm in the pre-IC era with superheterodyne radios. However, to reject the interferers at IF images, a high quality (Q)-factor band-pass filtering (BPF) would be required, which is extremely difficult to implement in CMOS.

The majority of commercial receivers are still continuous-time (CT), but several discrete-time (DT) receiver architectures have been reported in both industry [8] and academia [9–11]. Compared to CT receivers, DT receivers are more compatible with CMOS scaling,

fully reconfigurable and less sensitive to mismatches.

1.1 Aims and Scope

The fundamental research questions of this work are:

Can the discrete-time approach be utilized to design a high performance fully integrated SAW-less superheterodyne receiver with a high Q-factor band-pass filters? What are limitations in designing the image-reject band-pass filters using the discrete-time approach? What are consequences of sampling the RF signals and how can we preserve the purity of RF signals using the discrete-time approach?

The overall aim of this work is to explore the possibility of using the discrete-time approach for designing all the building blocks inside the superheterodyne receiver (except for low-noise transconductance amplifier (LNTA)), including RF mixer, low/band-pass filters, g_m-stages, and baseband filtering. After investigating possible solutions, the proposed architecture was first developed in 65 nm, since it was the best process available to us then, but the final breakthrough with much superior performance came at 28 nm, which got available to us under special arrangements.

Since the most important building block of the superheterodyne receiver is the filtering part, the first subgoal of this research is to propose a discrete-time charge-sharing (CS) band-pass filter (BPF) whose center frequency is proportional to a local-oscillator (LO) clock and a ratio of capacitors. Furthermore, noise and linearity performance of the CS-BPF need to be investigated. The second goal is to design a proof-of-concept receiver chip, implemented in 65 nm CMOS, using CS-BPFs, to validate the analysis, reconfigurability and speed capabilities of the CS-BPF.

The next goal is to explore the possibility of using the proposed CS-BPF in designing *fully* integrated 4G superheterodyne receiver meeting SAW-less requirements. Another goal is to investigate the possibility of designing the highly-linear LNTA to interface with antenna that is capable of meeting SAW-less requirements. The final goal is to design a complete SAW-less superheterodyne receiver using the discrete-time approach. The discrete-time analog signal processing ranges from the LNTA output up to the input of analog-to-digital (ADC) converters. The receiver is then implemented and experimentally verified.

The scope of this work is on the superheterodyne receiver including CS-BPFs. Other receiver building blocks, such as the LNA, mixer and IF g_m-stages are also considered. Also, the conclusions can be easily extended to other finer CMOS technologies.

1.2 Scientific Approach

The scientific approach in this work was partitioned into three major thrusts, each of them was separately implemented in three fabricated chips:

1. First, systematically explore the possibility of implementing the superheterodyne receiver in CMOS technology, then propose the DT CS-BPF and explore its limitations; next, apply DT CS-BPF as IF filtering stages. As a final step, implement a 65 nm CMOS test chip and validate the approach by measurements.

2. Utilize the DT CS-BPFs inside a new *feedback-based* receiver with much sharper filtering transfer function compared to the IF filtering in the first part. Also, limitations of these kinds of receivers are investigated. In the next step, the test chip of the feedback-based receiver is implemented in 65 nm CMOS technology, and finally the results are experimentally validated.

3. Since the blocker filtering characteristics of the CS-BPFs in parts 1 and 2 are not sufficient to meet the SAW-less requirements, a blocker-tolerant CS-BPFs is proposed as IF filtering in the finally implemented DT SAW-less superheterodyne receiver. In the next step, the SAW-less receiver is implemented in 28 nm CMOS technology. Finally results are experimentally validated.

Table 1.1: Thesis outline

Chapter	Purpose
Chapter 2	Setting up a common background for the research, the technical background of the research, together with analysis of different kinds of RF signal sampling.
Chapter 3	1. To utilize a new full-rate (4x) sampling mode of operation discussed in Chapter 2. 2. To analyze and propose a new architecture of a discrete-time (DT) superheterodyne receiver that avoids issues related to zero-IF receivers.
Chapter 4	To explore performance capabilities and limitations of the CS-BPF. A complex quadrature charge-sharing (CS) technique is proposed to implement a CS-BPF with a programmable bandwidth. It operates at the full sampling rate (4x), which was described in Chapter 2. The noise analysis of the CS-BPF is also investigated.
Chapter 5	To explore the possibility of making a high quality factor BPF at a very high IF, a highly reconfigurable superheterodyne RX is proposed that employs a 3^{rd}-order complex IQ charge-sharing band-pass filter (BPF) for image rejection and 1^{st}-order feedback based RF-BPF for channel selection filtering.
Chapter 6	To propose and demonstrate the first-ever fully integrated SAW-less superheterodyne receiver (RX) for 4G cellular applications. The low-power DT RX introduces various innovations in order to simultaneously improve noise and linearity performance: a highly linear wideband noise-canceling LNTA, a blocker-resilient octal CS-BPF, and a cascaded harmonic rejection circuitry.
Chapter 7	To answer the research questions defined in Section 1.1. General conclusions are drawn.

Therefore, for all of the above parts, following steps are taken:

- analyzing state-of-the-art receiver architectures;
- analyzing the available CT and DT filters;
- classifying key characteristics of the available filters and receivers;
- investigating the concept of DT CS-BPF by performing linearity, noise, and transfer function analysis;
- systematically exploring interactions of other building blocks inside RX with the DT CS-BPF;
- performing system-level noise and gain analysis of the receiver;
- designing and measuring the proof-of-concept chip to validate the effectiveness of the chosen architecture.

1.3 Thesis Outline

The outline of this work is given in Table. 1.1.

1.4 Original Contributions

The original individual contributions of this work are as follows:

- the analysis of state-of-the-art BPFs based on noise, linearity, and power consumption (Section 4.3);
- proposing of a new topology of BPFs: 4/4-phase CS-BPF (Section 4.3);
- performing a complete noise analysis of the 4/4-phase CS-BPF (Section 4.4);
- proposing the feed-back based RF receiver with integrated high-Q BPF and realizing it in 65 nm CMOS (Section 5.2);
- proposing a blocker-tolerant 8/8, 8/16, and generally M/N-phase CS-BPF (Section 6.4);
- deep analysis of the M/N-phase CS-BPF (Section 6.4);
- explanation of the inherent harmonic rejection capability of CS-BPF (Section 6.5.1);
- proposing an architecture of the first-ever SAW-less superheterodyne receiver; (Section 6.3)
- proposing a highly linear LNTA meeting the SAW-less requirements (Section 6.6.3);
- proposing a technique for multi-stage harmonic rejection (Section 6.5);
- proposing a circuit of highly linear IF transconductance amplifier (g_m-stage)(Section 6.6.4);
- performing lab verification of three ICs of 28 nm SAW-less superheterodyne RF receiver. The receiver features an IF frequency of 10–262 MHz, NF of 2.1 dB, IIP3 of 14 dBm, power consumption of 22–40 mW, worst-case uncalibrated image rejection of 65 dB, worst-case harmonic rejection of 58 dB and active area of 0.52 mm^2 (Section 6.7).

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CHAPTER

2

Background

The technical background overview of this research is now presented. The chapter starts with answers to the question "why discrete-time?". Then it gives a brief analysis on advantages of discrete-time approach versus continuous-time in finer CMOS technologies, in which V_{DD} decreases, MOS threshold voltage (V_{th}) stays almost constant, headroom decreases, and transistor cutoff frequency (f_T) increases. A general concept of discrete-time receiver is discussed for the zero intermediate-frequency (IF) and high-IF receivers. The frequency translations and folding of images in the discrete-time receivers are depicted in detail with timing diagrams of I/Q local oscillator (LO) and relevant I/Q currents and charges. The concept of sampling in receivers is described for 1x, 2x and 4x rates. The proposed full-rate mode (4x) is described in detail and advantages of higher sampling rate are explained. Also, it is mentioned how the poor image rejection in the 2x sampling receivers can be eliminated with the 4x sampling.

Linearity fundamentals in wireless receivers are reviewed in this chapter. Concepts, such as harmonic distortion, desensitization, intermodulation and 2^{nd}-order nonlinearity are discussed. The mathematical treatment of nonlinear sources is also mentioned.

2.1 Why Discrete-Time?

2

While key motivations of CMOS scaling have been to reduce transistor cost and to improve digital performance, conventional RF/analog designs do not benefit significantly. As shown in Fig. 2.1(a), going from 180 nm to 28 nm CMOS, V_{DD} is reduced almost by half while MOS threshold voltage (V_{th}) has not changed considerably. Therefore, the available precious voltage headroom for RF/analog design is now reduced dramatically [1]. Considering also the reduced MOS intrinsic gain [1] and its saturation linearity [2], RF/analog design is becoming generally more difficult. On the other hand, majority of cellular and wireless standard frequency bands are allocated in 0.4–6 GHz, and have not significantly changed for many years. Meanwhile, transistor cutoff frequency (f_T) has improved dramatically with scaling, (see Fig. 2.1(a)). This suggests that conventional RF/analog techniques, which were optimized for the older technology do not effectively use the ultra-high speed of transistors of scaled CMOS to improve performance. In contrast, discrete-time (DT) RF/analog building blocks (Fig. 2.1(b)) avoid using complicated analog components such as opamps. Most signal processing and filtering there are done using passive switched-capacitor circuits [3, 4] that can work at very low V_{DD}. As the technology scales, MOS switches become faster and tinier with less parasitic capacitances. Moreover, capacitor density improves, resulting in a reduced area. Clocks are also generated using digital logic that becomes also faster and more power efficient with the scaling. To provide signal gain, DT techniques use inverter-based gm-cells that are always compatible with digital technology with improving g_m over bias current. In this way, DT receivers directly benefit from scaling similar to digital circuits. Refs. [5–11] are examples of DT process-scalable receivers.

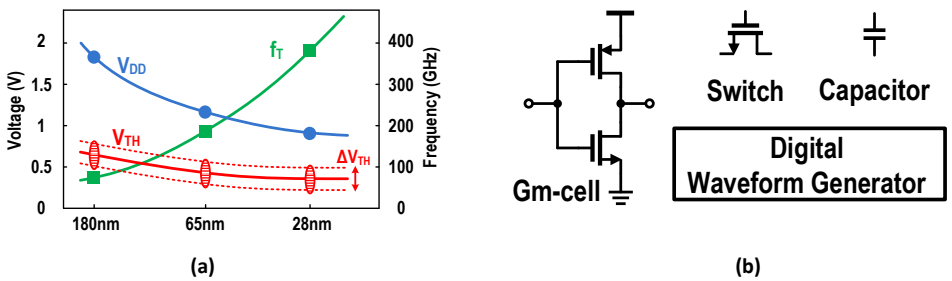

Figure 2.1: (a) Typical CMOS scaling trends for low-power/low-leakage process technology. (b) Components used in DT signal processing.

2.2 Discrete-Time Receiver

A simplified conceptual diagram of a DT ZIF receiver is shown in Fig. 2.2(a). It consists of a low-noise transconductance amplifier (LNTA), a pair of quadrature mixers and DT sampling LPFs. The received RF signal is amplified and converted into current, i_{RF}, by the LNTA with high output impedance. This current is then downconverted to ZIF by the quadrature mixers. The mixers are driven by the quadrature $LO_{I,Q}$ signals (at f_{LO}), which are differential 25% duty-cycle clocks with 90^o phase shift. Fig. 2.2(b) shows signal waveforms for a narrow-band modulated

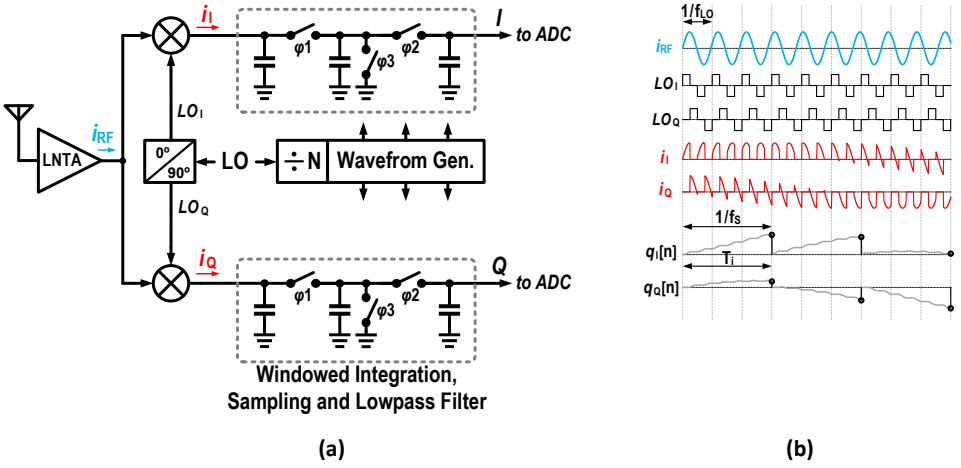

Figure 2.2: (a) A simple DT receiver with passive LPF; and (b) its waveforms at various nodes.

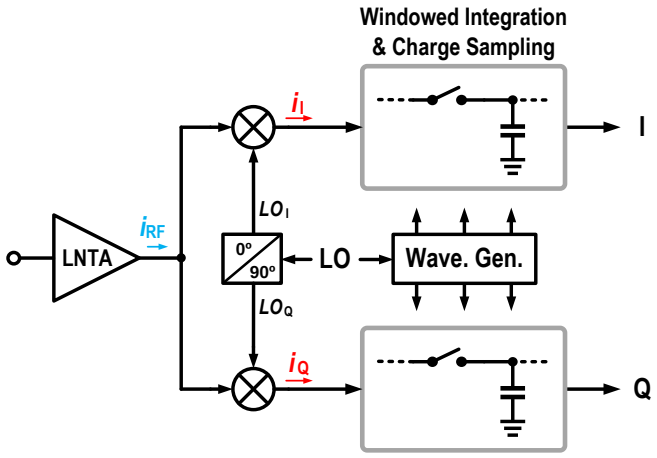

Figure 2.3: Signal sampling in a DT receiver.

RF signal. The downconverted current is integrated over a time window T_i and sampled as DT charge packets [4], $q_{I,Q}[n]$. The windowed integration (WI) forms a continuous-time (CT) *sinc* anti-aliasing filter just before the sampling, and attenuates unwanted signals folded from multiples of the sample frequency f_s (i.e., sampling images) [7–9, 12]. The DT data is then low-pass filtered by a passive switch-cap circuit (e.g., a 2$^{\text{nd}}$-order IIR [3, 4, 7]). In most of the DT ZIF receivers, this sampling is done at a significantly lower rate than f_{LO} [7–9, 13, 14].

2.2.1 1x Sampling in Zero-IF

Consider the case of a simplified DT ZIF receiver in Fig. 2.3, where the signal iI, Q is sampled at the same rate as the LO frequency ($f_s = f_{LO}$) [8], hereafter 1x sampling. Fig. 2.4(a) shows its time-domain signal waveforms. This RX has sampling images at multiples of f_{LO}. Fig. 2.4(b) shows the frequency translation. The wanted RF signal is downconverted to DC by mixing with the quadrature LO tone. At the same time, frequency bands near DC and $2f_{LO}$ are translated to $\pm f_{LO}$. The CT anti-aliasing filter created by WI has its notches coinciding with the sampling images. The narrower the bandwidth, the stronger the image attenuation [9]. After the sampling, attenuated images at multiples of $\pm f_s$ are folded over the wanted signal at baseband.

2.2.2 2x Sampling in Zero-IF

By doubling the sample rate to $f_s = 2f_{LO}$ (hence, 2x sampling), the ZIF receiver does not introduce any sampling images (other than those caused by the mixer's odd harmonics). As shown in Fig. 2.5(b), the anti-aliasing filter is widened twofold. After the 2x sampling, the "yellow" bands still remain at high frequency as they are not mixed with the wanted signal. Therefore, it is possible to further filter the images prior to decimation and folding over the wanted signal. The only images created by sampling are self-image of the wanted RF signal and the images that come from the odd harmonics of fRF (e.g., $3f_{RF}$, not shown in the figure), all attenuated earlier by the anti-aliasing filter.

2.2.3 2x Sampling in Superheterodyne

If the 2x sampling were to be used in a DT superheterodyne with high IF frequency (f_{IF}), where $f_{LO} = f_{RF} + f_{IF}$, it would show a poor image rejection. To illustrate that, let us assume spectra depicted in Fig. 2.6(b). The wanted signal is downconverted to $+f_{IF}$, while part of the image power is upconverted to $2f_{LO} + f_{IF}$. By sampling this signal at the 2x rate, this image folds over the wanted signal at $+f_{IF}$. In addition, note that the notch of WI is not aligned with the image (it is separated by f_{IF}), so the image is not effectively filtered out. To get further insight, let us

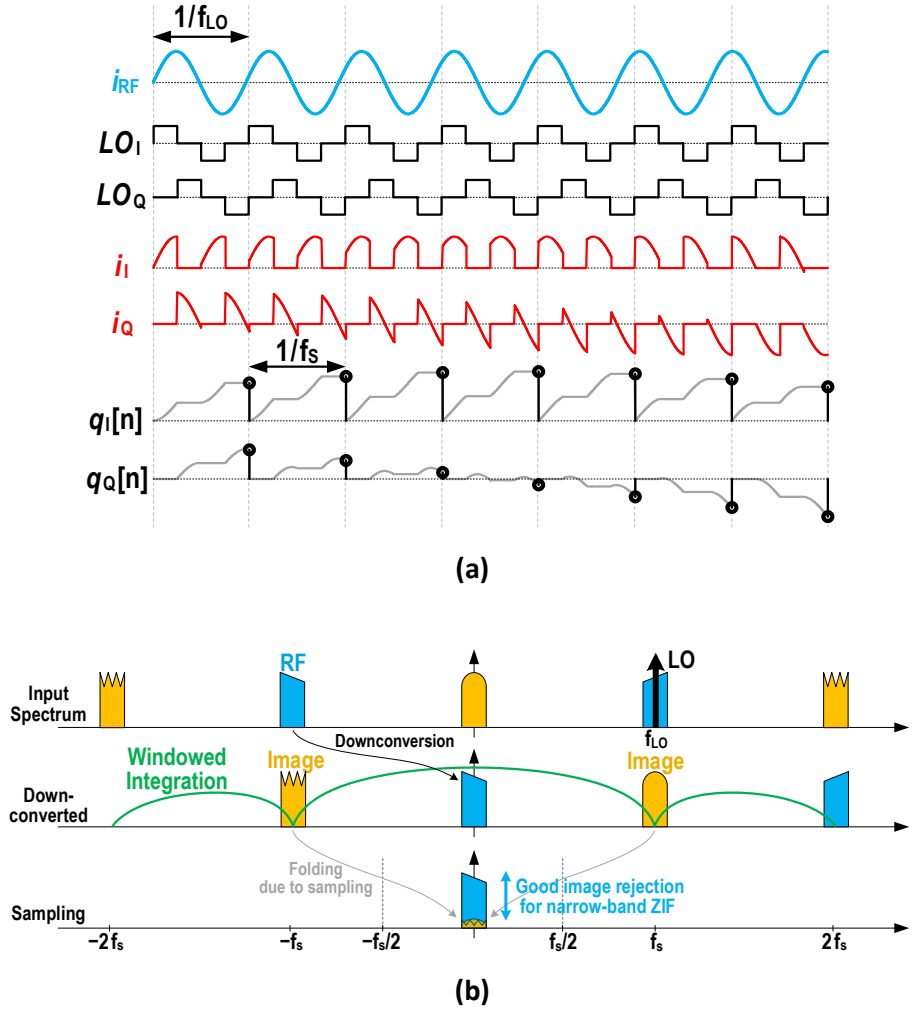

Figure 2.4: (a) Time-domain signal waveforms; and (b) frequency translation in a 1x sampling zero-IF DT receiver: input spectrum is shifted to right (RF downconversion) and after windowed integration is sampled.

closely inspect the resulting time-domain $q_I[n]$ and $q_Q[n]$ signals in Fig. 2.6(a). The phase shift between them is not exactly 90^o, as expected for quadrature signals. There is an error of half the sampling period that creates $\theta_{err} = (T_s/2) \times 2\pi f_{IF}$ [15] and limits the image rejection.

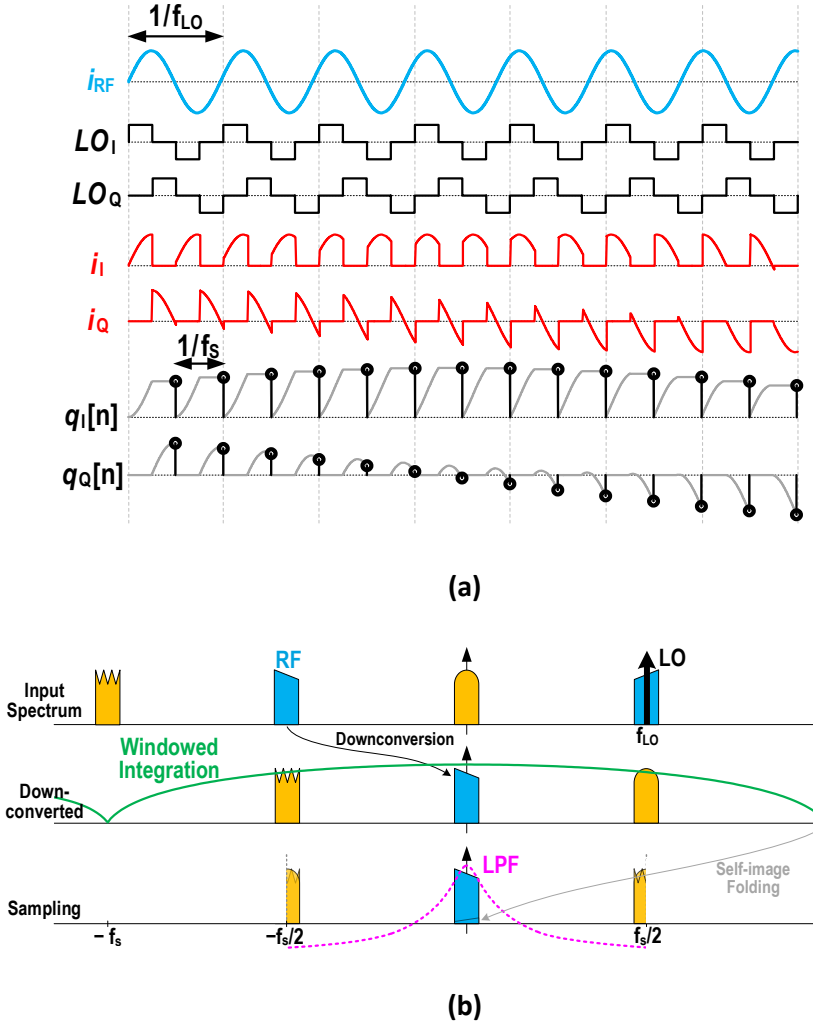

Figure 2.5: (a) Time-domain signal waveforms; and (b) frequency translation in a 2x sampling zero-IF DT receiver. "Yellow" bands after the sampling are folded on themselves, but remain apart from the wanted signal and can be filtered afterwards by a DT LPF.

2.2.4 Proposed 4x Sampling

To solve the above problem of high-IF images introduced by sampling, we propose advancing to a 4x sampling, i.e., $f_s = 4f_{LO}$. The I and Q sampled signals in Fig. 2.7(a) have now precisely 90^o phase shift. Although samples with zero value between non-zero samples seem to be non-informative, they are ensuring quadrature accuracy. Furthermore, consider the signal spectrum in Fig. 2.7(b). This time, the

upconverted image at the mixer output ($2f_{LO} + f_{IF}$) folds over $-f_s + f_{IF}$ by the sampling, keeping it apart from the wanted signal. Then a DT complex bandpass filter (BPF) is able to select the wanted signal and filter out the rest. The only images that are translated directly on top of the wanted signal are the mixer's odd harmonic images.

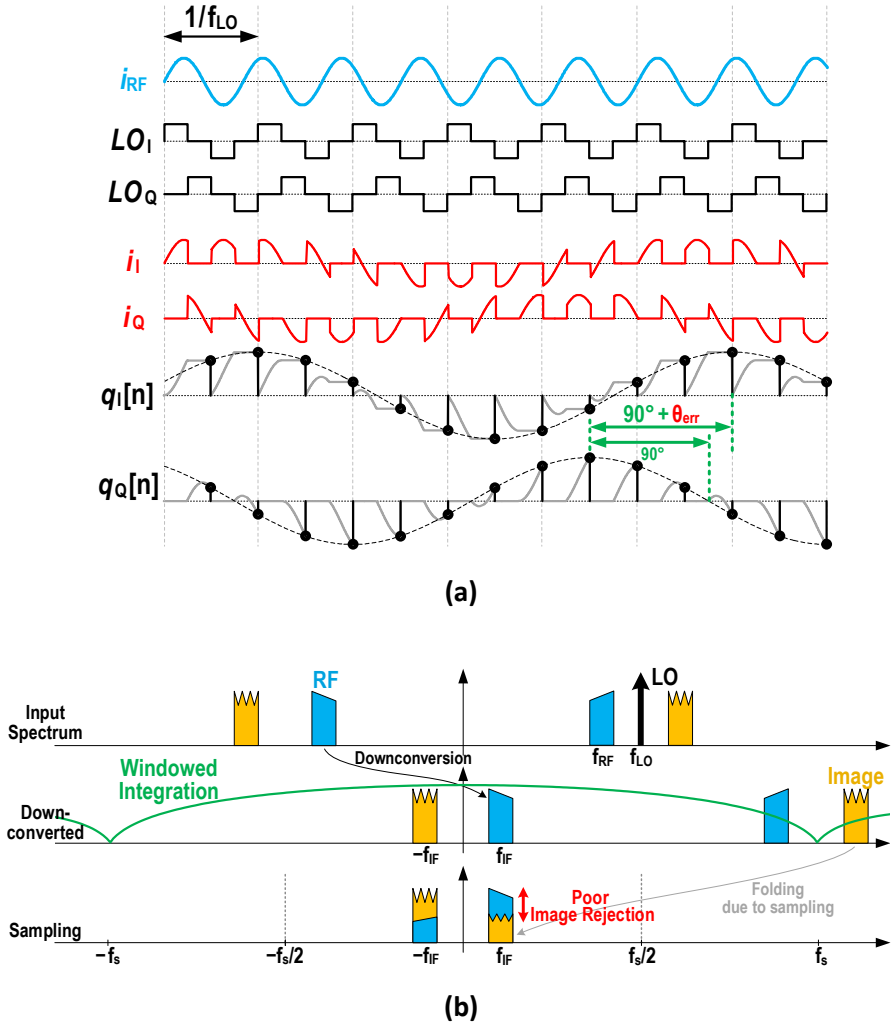

Figure 2.6: (a) Time-domain signal waveforms; and (b) frequency translation in a 2x sampling DT superheterodyne receiver. After the sampling, image is aliased on the wanted signal without enough attenuation.

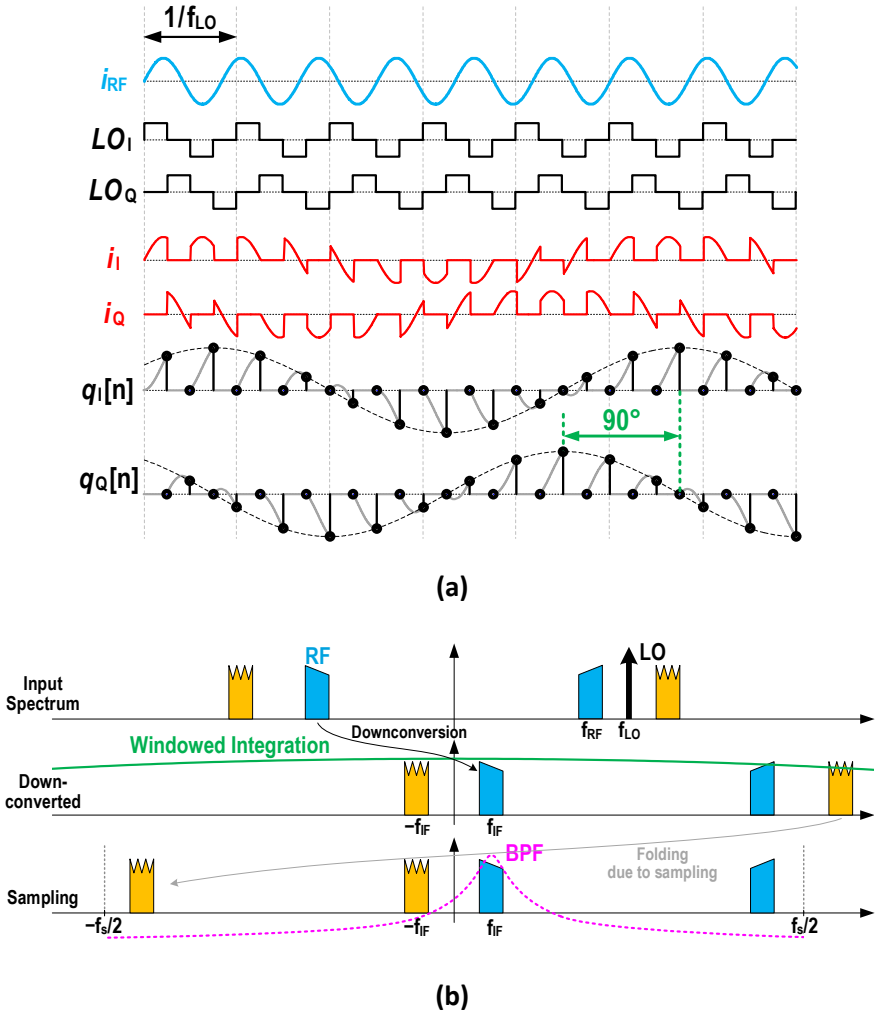

Figure 2.7: (a) Time-domain signal waveforms; and (b) frequency translations in a 4x sampling DT superheterodyne receiver. Since f_s is increased to $4f_{LO}$, IF image is completely distinct from the wanted signal and can be filtered afterwards by a DT BPF.

2.3 Linearity Fundamentals in Wireless Receivers

In a memoryless or static system, its output does not relate on past values of its input. For the memoryless linear system, the input/output characteristic is depicted by

$$y(t) = \alpha x(t), \tag{2.1}$$

where α is a function of time if the system is time-variant [16]. While analog and RF circuits can be approximated by a linear model for small-signal operation, nonlinearities play a role that are not predicted by small-signal models. In this context, I will mention the phenomena for memoryless systems whose input/output characteristic can be approximated by

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t). \tag{2.2}$$

where α_1 can be considered as the small-signal gain of the system, while the 2nd-order and 3rd-order nonlinearities arise from α_2 and α_3 coefficients [16].

2.3.1 Harmonic Distortion

If a sinusoid signal is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples ("harmonics") of the input frequency. If we apply $x(t) = A\cos\omega t$ to (2.2), then

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha 3 A^3}{4}\cos 3\omega t. \end{aligned} \tag{2.3}$$

In (2.3), the first term is a DC value originated from 2nd-order nonlinearity, the second is the "fundamental", the third is the second harmonic, and the fourth is the 3rd harmonic. Therefore, it can be stated that even-order nonlinearity introduces DC offsets. In a symmetric (fully differential) system, the even-order nonlinearities/harmonics can be eliminated. However, in actual implementation, the random inconsistencies make the system asymmetrical, yielding finite even-order harmonics rejection.

2.3.2 Desensitization

Another nonlinearity scenario could occur in the RF receiver is when a large interferer accompanies the received signal. Although the desired signal is very small, the receiver gain is reduced by the product generated by the interferer. This scenario is referred to as "desensitization", and it decreases the signal-to-noise ratio (SNR) at the receiver output.

To quantify desensitization, it is assumed that $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$ is applied to the RF input, where the first and the second term are the desired small RF signal and large interfere/blocker, respectively. By substituting input signal to

(2.2), it is detemined that the output is

$$y(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 A_1^2 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 \cos\omega_1 t + \cdots. \tag{2.4}$$

If the assumptions is that $A_1 \ll A_2$, (2.4) is simplified to

$$y(t) = \left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 \cos\omega_1 t + \cdots. \tag{2.5}$$

Therefore, the gain of the RF signal accompanied by the large interferer is changed from α_1 to $\alpha_1 + \frac{3}{2}\alpha_3 A_2^2$. If $\alpha_1\alpha_3 < 0$, which is the case in reality, for a sufficiently large A_2, the gain reduces to zero [16].

2.3.3 Intermodulation

In Section 2.3.1 and 2.3.2 the nonlinearities of an individual signal for harmonic distortion and a RF signal accompanied by a large interferer for desensitization are studied, respectively. Another phenomena in RF design is when *two* interferers accompany the desired signal. This is the most realistic situation that could possibly occur, and it reveals nonlinearity effect that may not express itself in a harmonic distortion or desensitization test [16].

If two interferes at ω_1 and ω_2 are applied to the input of any nonlinear system, the output spectrum contains components known as "intermodulation" products that are not harmonics of those interferer frequencies. Intermodulation (IM) products originate from *mixing* two interferers when their sum is experiencing a nonlinear term with a power greater than unity [16]. To clarify, assume $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$ is applied to a nonlinear system. Thus, (2.2) changes to:

$$y(t) = \alpha_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + \alpha_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + \alpha_3(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3. \tag{2.6}$$

By expanding all terms, the intermodulation components can be found at:

$$\begin{aligned} \omega &= 2\omega_1 \pm \omega_2 : \tfrac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \tfrac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \\ \omega &= 2\omega_2 \pm \omega_1 : \tfrac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_1 + \omega_2)t + \tfrac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_1 - \omega_2)t \end{aligned} \tag{2.7}$$

and fundamental frequencies at:

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 + \frac{3}{4}\alpha_3 A_1^2 + \frac{3}{2}\alpha_3 A_2^2\right) A_1\cos\omega_1 t + \left(\alpha_1 + \frac{3}{4}\alpha_3 A_2^2 + \frac{3}{2}\alpha_3 A_1^2\right) A_2\cos\omega_2 t. \tag{2.8}$$

Fig. 2.8 illustrates the results. Among these, the 3rd-order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are of particular interest because, if the desired signal at ω_{RF} is being received along with two large interferers at ω_1 and ω_2 at the input of a low-noise amplifier (LNA) with nonlinear characteristic and $\omega_{RF} = 2\omega_1 - \omega_2$, then, as a result, the IM product falls into the desired signal so the RF input is corrupted. Therefore, for measuring of IM, a common method is the "two-tone" test whereby two pure sinusoids of equal amplitudes are applied to the input [16]. The amplitude of the output IM products is subsequently normalized to that of the fundamentals at the output. Denoting the peak amplitude of each tone by A, the result can be indicated as

$$Relative\ IM3 = 20log\left(\frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2\right)dBc, \tag{2.9}$$

and "input third intercept point" (IIP3) is defined as input power where a 3rd-order IM product has the same amplitude as the desired signal (illustrated in Fig. 2.9) and can be stated as,

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.10}$$

Hence, in general, interferers can reduce RX performance with several mechanisms, such as gain compression, emergence of in-band IM products, cross-modulation, AM-to-PM distortion, and desensitization, e.g., [17, 18].

The critical phenomena in the front-end are determined by the interference and operating environment specified by the system for which the RF front-end is designed [18]. For example, in the 3G WCDMA system, since it is an FDD system, the transmitter and receiver are working continuously and simultaneously, and the transmitted signal leaks into the receiver due to the limited TX-to-RX isolation of the duplexer. The linearity is impacted by the transmitter output leakage into the receiver front-end input e.g., [19, 20]. Depending on the system type, the transmit-to-receive frequency offset can be in the range from tens to hundreds of MHz. In 3G Band 1, for instance [21], the transmit band has an offset of 190 MHz to the receive band. The out-of-band IIP3 is primarily determined by the transmitter leakage

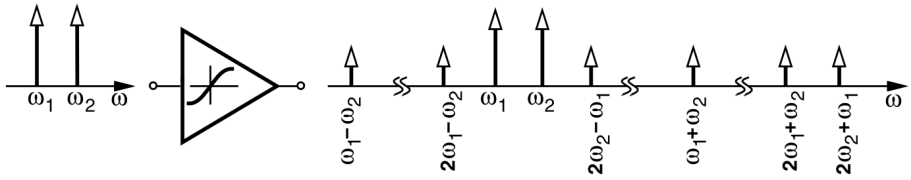

Figure 2.8: Intermodulation products for a nonlinear system in a two-tone test [16].

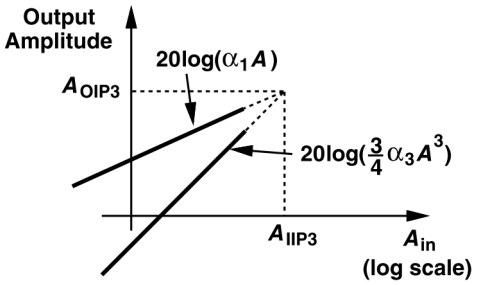

Figure 2.9: Definition of IIP3 [16].

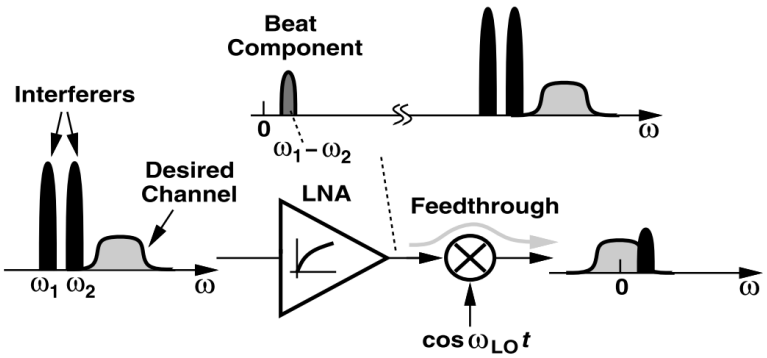

Figure 2.10: Effect of even-order distortion on RF receiver [16].

and out-of-band blockers at half and twice the transmit-to-receive frequency offset, specifically at offsets of 95 MHz and 380 MHz, respectively, from the desired RF signal. Depending on the interferer/blocker frequency allocations for various RX front-end in specific implementations, the out-of-band IIP3 requirement can be of the order of -3 to 10 dBm. Similarly, the variable transmit leakage amplitude to the RX band leads to an IIP2 requirement in the order of 45 dBm or more depending on the architecture of RX front-end. An in-band IIP3 requirement also arises from interferers/blockers at the offset of 10 and 20 MHz. Detailed blocker and intermodulation specifications for this standard can be found in [21].

2.3.4 Second-Order Nonlinearity

It is mentioned that IM3 distortion results in compression and intermodulation. With the same approach as the mechanism of 3^{rd}-order nonlinearity that is mentioned, exhibited in Fig. 2.10,it is assumed that two strong interferers at ω_1 and ω_2 experience nonlinearity such as $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ in a nonlinear system. The second order

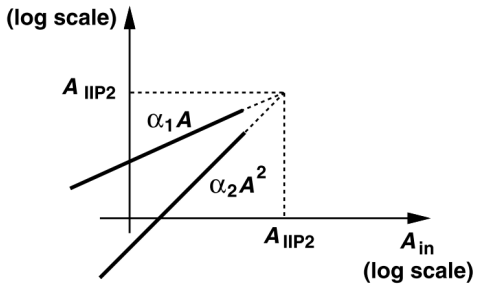

Figure 2.11: Definition of IIP2 [16].

term generates a low-frequency component, a so called IM2 product at $\omega_2 - \omega_1$. In actual implementation, any asymmetry in the mixer or in the LO clock waveform allow a fraction of generated IM2 product to transfer to the mixer output *without* any frequency translation, thereby corrupting a desired RF signal.

The "second input intercept point" (IIP2) is defined according to a two-tone test similar to that for IIP3 except that the output of interest is the low-frequency component rather than the intermodulation product [16]. If $x(t) = A\cos\omega_1 t + A\cos\omega_2 t$ is applied to the input of a system with second-order nonlinearity, the output is given by

$$\begin{aligned} y(t) &= \alpha_1 x(t) + \alpha_2 x^2(t) \\ &= \alpha_1(A\cos\omega_1 t + A\cos\omega_2 t) + \alpha_2 A^2 \cos(\omega_1 + \omega_2)t \\ &+ \alpha_2 A^2 \cos(\omega_1 - \omega_2)t + \cdots. \end{aligned} \tag{2.11}$$

whereby the amplitude of low-frequency IM2 component increases by a power of two as input amplitude increases. Thus, as depicted in Fig. 2.11, the IM2 component rises with a slope of 2. As an example, the value of A that creates the output IM2 product equal to the desired RF signal in the mixer, is given by

$$A_{IIP2} = \frac{1}{k} \cdot \frac{\alpha_1}{\alpha_2}, \tag{2.12}$$

where k is the attenuation factor experienced by the IM2 product as it passes through the mixer [16].

It should also be mentioned that the second-order nonlinearity of the receiver will square the modulated blocker signal, such as the TX leakage signal, producing DC and low frequency components which fall into and far from the receive band in the direct conversion and superheterodyne receivers, respectively. The AM (amplitude modulated) signal is demodulated into the RX channel with twice the bandwidth of the original interferers. Moreover, a powerfull blocking signal will also intermodulate due to second-order nonlinearity with the TX leakage signal to create a TX image which can fall into the band.

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CHAPTER

3

Discrete-time Superheterodyne Receiver in 65 nm CMOS

The zero/low intermediate frequency (IF) receiver (RX) architecture has enabled full CMOS integration. As the technology scales and wireless standards become ever more challenging, the issues related to time-varying DC offsets, second-order nonlinearity and flicker noise appear a real impediment to further progress. In this chapter, we propose a new architecture of a superheterodyne RX that avoids such issues. By exploiting discrete-time (DT) operation and using only switches, capacitors and inverter-based gm-stages as building blocks, the architecture becomes amenable to further scaling. The full-rate (4x) sampling mode was described in Chapter 2 and the proposed 65 nm CMOS RX utilizes the full-rate sampling scheme in all the IF stages. Full integration is achieved by employing a cascade of four complex-valued passive switched-cap based bandpass filters (BPFs) sampled at 4x of the local oscillator (LO) rate that perform IF image rejection. Channel selection is achieved through an equivalent of 7$^{\text{th}}$-order filtering. The RX is wideband and covers 0.4–2.9 GHz with noise figure of 2.9–4 dB. It is implemented in 65 nm CMOS and consumes 48–79 mW.

This chapter is based on two papers, coauthored with Massoud Tohidian, one published at ISSCC conference in 2014 [1], and the other submitted for publication in IEEE Transactions on Circuits and Systems I (TCAS-I) [2].

3.1 Proposed DT Superheterodyne Receiver Using 4X Sampling

As shown in Fig. 2.2, the signals at the mixer output are still continuous-time (CT). In reality, the windowed current integration, sampling and DT processing happen in the subsequent switched-capacitor block. In addition, the square-like waveforms of mixer clocks, LOI/Q, in Fig. 2.7(a) possess odd harmonics (i.e. $+3^{\text{rd}}$, -5^{th}, etc.), which not only downconvert high-frequency images on top of the wanted signal, but also upconvert the input spectrum to high frequencies around the harmonics. The sampling also folds spectrum of the signal that is outside of the Nyquist range into the $-f_s/2$ to $+f_s/2$ range. Since both mixing and sampling processes translate frequencies with respect to the LO harmonics and sampling rate, respectively, they make a rather complicated matrix for a complete picture of frequency translations.

The top-level diagram in Fig. 3.1 provides a straightforward yet accurate model for the DT receiver, illustrating its functionality and the scheme of frequency translations. Since the accumulated charge is read out by the switched-capacitor filter at the 4x rate, and also the states of mixer clocks are changing at the same rate (i.e., 4 times in each cycle), these operations are mutually commutative so it would make no difference if we (advantageously) consider the WI and sampling executed ahead of the mixing. In this way, the rest of signal processing after the sampling is done in the discrete-time domain . Therefore, the "DT mixers" interpret their input signals as DT input sequences instead of the CT square waveform. Also, the outputs of DT mixers become sampled-charge data rather than the CT i_I and i_Q waveforms of Fig. 2.7(a). Discrete-time charge packets after WI and sampling are described as:

$$q_{in}[n] = \int_{(n-1)T_s}^{nT_s} i_{RF} \cdot dt, \tag{3.1}$$

where i_{RF} is the result of LNTA input voltage (V_{RF}) multiplied by its transconductance $g_{m,LNTA}$. This WI creates a continuous-time *sinc* type filter [3–8]), prior to the sampler in Fig. 3.1:

$$H_{WI}(f) = T_s \times \frac{\sin(\pi f T_s)}{\pi f T_s} = T_s \times \text{sinc}\left(\frac{f}{f_s}\right). \tag{3.2}$$

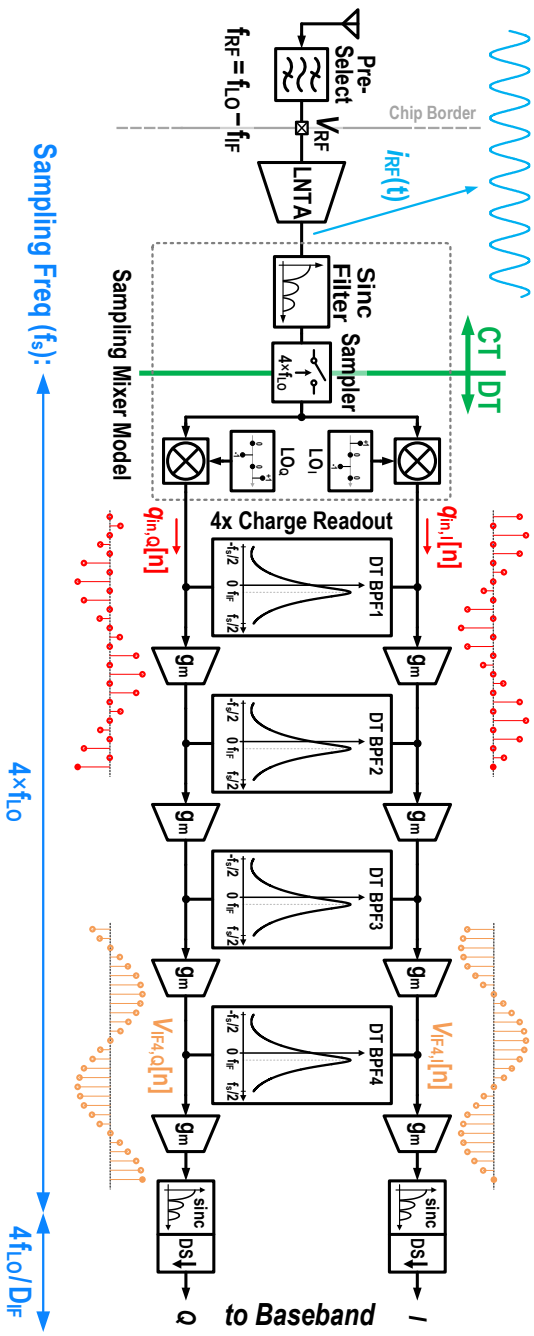


Figure 3.1: The proposed DT superheterodyne receiver using 4x sampling.

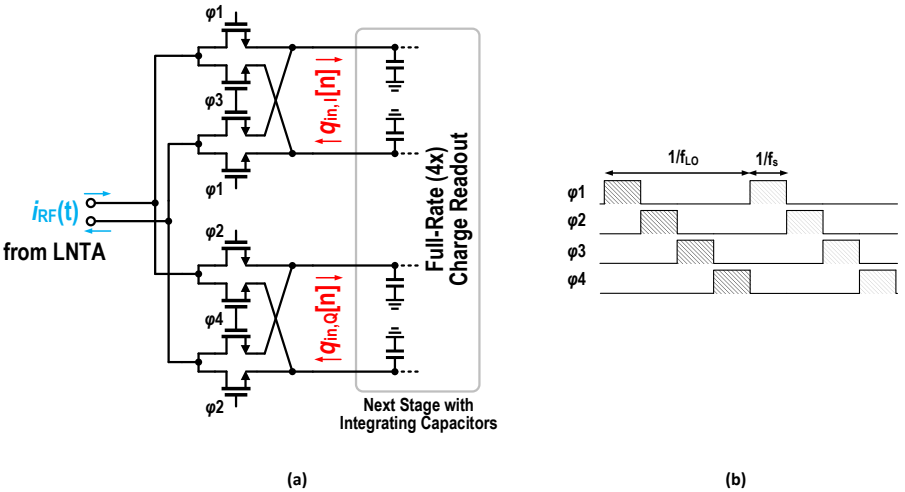


Figure 3.2: (a) Implementation of the sampling mixer in Fig. 3.1 with passive current commutating mixer. (b) Driving clock waveforms.

3.1.1 Sampling Mixer

The LO clock sequences in Fig. 3.1 are $LO_I[n]$={1 0 −1 0} and $LO_Q[n]$={0 −1 0 1} and could be written as:

$$\begin{cases} LO_I[n] = \frac{1}{2}e^{j\left(\frac{\pi}{2}n\right)} + \frac{1}{2}e^{-j\left(\frac{\pi}{2}n\right)} \\ LO_Q[n] = \frac{1}{2}e^{j\left(\frac{\pi}{2}n+\frac{\pi}{2}\right)} + \frac{1}{2}e^{-j\left(\frac{\pi}{2}n+\frac{\pi}{2}\right)} \end{cases}. \tag{3.3}$$

In frequency domain, they exhibit two tones at $\pm f_s/4$, which is f_{LO}, with 90^o phase shift between I and Q. From (3.3), downconversion gain of each DT mixer becomes $A_{mix,I/Q} = 1/2$. Implementation of the sampling mixer is depicted in Fig. 3.2 and consists of two current commutating passive mixers for I and Q paths.

3.1.2 DT I/Q Charge-Sharing Bandpass Filter (CS-BPF)

Fig. 4.5 shows the DT CS-BPF (first disclosed in [9]) used in the IF strip. Its input are DT charge packets ($q_{in,I}[n]$ and $q_{in,Q}[n]$), and its output are voltage samples ($V_{o,I}[n]$ and $V_{o,Q}[n]$). This filter is based on the idea of polyphase filter where inputs with different phases (e.g., quadrature I/Q) are combined with different phase shifts. Assuming the complex input and output signals of this filter are $q_{in}[n] = q_{in,I}[n] + j \cdot q_{in,Q}[n]$ and $V_{out}[n] = V_{out,I}[n] + j \cdot V_{out,Q}[n]$, DT transfer

function (TF) of this filter can be derived [10]:

$$H_{BPF}(z) = \frac{V_{out}}{q_{in}} = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)]\, z^{-1}} \tag{3.4}$$

The 4th-order CS-BPF are utilized to perform a IF image rejection and the passband gain of this filter is calculated to be:

$$A_{BPF} \approx \frac{1}{C_R} \quad \text{for } C_R \ll C_H \tag{3.5}$$

The detailed analysis and design of the CS-BPF is discussed in chapter 4.

3.1.3 Frequency Translations

The whole process of frequency translations that happen in the proposed HIF DT receiver is depicted in Fig. 3.3. As the continuous-time input signal enters the Fig. 3.1 receiver, it is filtered by the CT *sinc* filter described in (3.2). Images are then created due to sampling, as indicated in brown in Fig. 3.3(a). In this example (with $f_{RF} = f_{LO} - f_{IF}$), sampling images are at $-f_{LO} + f_{IF} + k\cdot(4f_{LO})$ and $f_{LO} - f_{IF} + k\cdot(4f_{LO})$ for k=1, 2, 3, ... From (3.2), *sinc* filter attenuations of the first two images (k=1) near 3rd and 5th f_{LO} harmonics are 9.5 dB and 14 dB, respectively, the same as image attenuation of a CT 4-phase mixer. The sampling images are further attenuated in this receiver by the LNTA and a preselect filter.

After sampling, the DT input spectrum is now spread from $-f_s/2$ to $+f_s/2$, where $f_s = 4f_{LO}$. Fig. 3.3(b) shows the wanted RF signal and the important images. After mixing the entire signal spectrum with the complex LO tone, the negative side is downconverted to around DC, while the positive side is upconverted to close to $\pm f_s/2$ (see Fig. 3.3(c)). At this point, the wanted signal is located at $+f_{IF}$ while its IF image (in red) at $-f_{IF}$.

The spectrum of Fig. 3.3(c) is then filtered by the complex DT BPFs in the IF strip (see Fig. 3.3(d)). At this point, out-of-band images and blockers are attenuated enough, such that the signal of interest can be decimated to a lower baseband sample rate, $f_{s,BB}$. This leads to power consumption reduction for the remainder of processing blocks. The decimation is being protected by a DT sinc antialiasing filter that is simply achieved by adding up DIF samples (a.k.a., moving average, MA). Therefore, the images are further filtered out (Fig. 3.3(e)) before downsampling and aliasing (Fig. 3.3(f)). Transfer function of the MA filter is:

$$H_{MA,IF}(f) = D_{IF} \times \text{sinc}(f/f_{s,BB}) \tag{3.6}$$

where $f_{s,BB} = f_s/D_{IF}$. A small resulting attenuation of the wanted signal at f_{IF} is neglected in the rest of the text. The decimation is trivially implemented by lowering the readout rate of the block succeeding the gm-cell. This way, several samples are

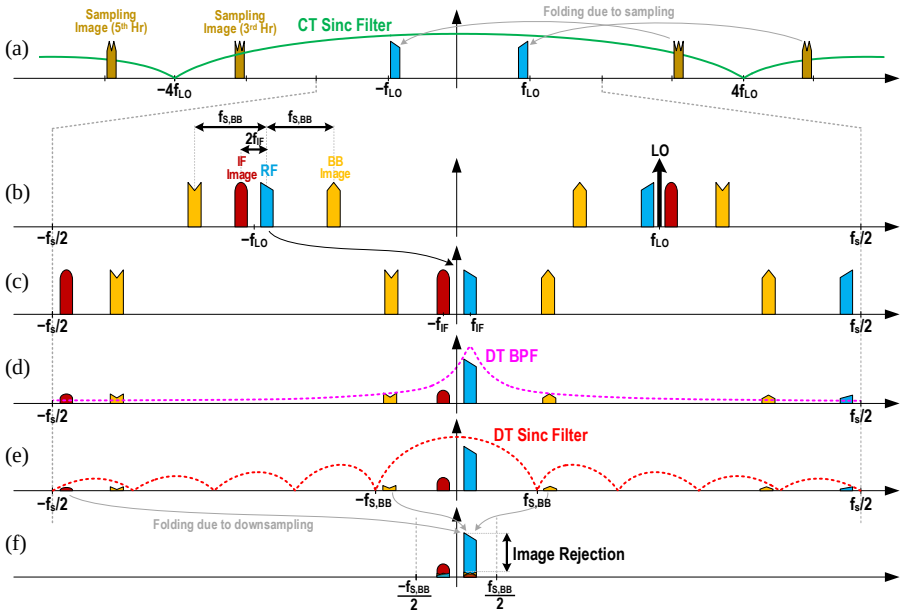


Figure 3.3: Frequency translations in the DT receiver: (a) images caused by sampling of CT signal; (b) input spectrum after the sampling; (c) downconverted spectrum after the DT mixer; (d) signals after IF filter stages; and decimation by (e) applying an antialiasing filter before (f) baseband downsampling.

accumulated, and then processed once (temporal decimation [11]). Considering the frequency translations in Fig. 3.3 and the receiver model shown in Fig. 3.1, we are now able to calculate gain of signals at different frequencies from the LNTA RF input to the IF strip output. Using (3.2), (3.3) and (3.5), gain of the wanted RF signal from LNTA input until V_{IF4} is:

$$G_{wanted} = V_{IF4,I/Q}/V_{RF} = \left[g_{m,LNTA} H_{WI}\left(f_{LO} - f_{IF}\right) A_{mix} A_{BPF}\right] \times \left[A_{gm,IF} A_{BPF}\right]^3$$
$$\approx \left[g_{m,LNTA} \text{sinc}\left(1/4\right) \times 1/2 \times \frac{1}{f_s C_R}\right] \times \left[\frac{g_{m,IF}}{C_R f_s}\right]^3 . \tag{3.7}$$

In the above equation $f_{IF} \ll f_{LO}$ is considered.

The closest image that could fold onto the wanted RF signal is the IF image at $f_{LO} + f_{IF}$. As shown in Fig. 3.3(e), part of the IF image energy after mixing and attenuation resides at $-f_s/2 + f_{IF}$. This signal is folded over the wanted signal after downsampling, assuming an even D_{IF}. Rejection of this image can be calculated by adding attenuations of the BPFs and DT moving average filter, from (3.4) and (3.6),

respectively. Considering $f_{IF} = f_{LO}/16$ and $D_{IF} = 16$, the total IF image rejection (caused by sampling) reaches more than 135 dB. However, quadrature inaccuracy of the practical LO signals also aliases a tiny part of IF image right after the mixers, from $f_{LO} + f_{IF}$ to $+f_{IF}$ in Fig. 3.3(b) and (c). The latter effect is predominant and limits the IF image rejection to 40–80 dB, depending on quadrature accuracy, layout, and mixer mismatch.

The second important class of images are baseband (BB) downsampling images. Translated back to the RF input, they are located at $f_{RF} \pm k \cdot f_{s,BB}$. The first two of them (for k=1) are shown in yellow in Fig. 3.3(b). After mixing down (Fig. 3.3(c)) and passing through the BPFs (Fig. 3.3(d)), they are attenuated by the DT MA filter (Fig. 3.3(e)), and then folded over the wanted signal via downsampling (Fig. 3.3(f)). By means of (3.4), the exact attenuation of BPF can be calculated. As a first-order approximation of (3.4) for midrange frequencies ($f_{IF} \ll f \ll f_s/2$), Bode plot of a 1st-order LPF with a 3 dB bandwidth of f_{IF} is being considered that is shifted to be centered at f_{IF}. So, BPF rejection at $f_{s,BB}$ offset from the passband is approximated as:

$$R_{BPF}(f) \approx \left.\frac{f - f_{IF}}{f_{IF}}\right|_{f=f_{IF}+f_{s,BB}} = \frac{f_{s,BB}}{f_{IF}} \tag{3.8}$$

Both sampling images are attenuated by the same amount, due to the symmetry around f_{IF}. The higher $f_{s,BB}$, the higher the attenuation. Then, the images are attenuated by the moving-average filter in (3.6). A higher $f_{s,BB}$ makes the images relatively closer to notches of the *sinc* filter thus improving attenuation. Adding up all these attenuations, baseband downsampling image rejection ratio (IMRR) becomes:

$$IMRR_{BB} \approx \left(\frac{f_{s,BB}}{f_{IF}}\right)^4 \Big/ \left|\mathrm{sinc}\left(\frac{f_{IF} \pm f_{s,BB}}{f_{s,BB}}\right)\right| \tag{3.9}$$

where a small attenuation of the wanted signal by (3.6) is neglected. By choosing a proper number of BPF stages and decimation factor to set $f_{s,BB}$, a desired IMRR can be achieved. Considering the f_{IF} and $f_{s,BB}$ used in our implementation, theoretical BB IMRRs could reach 59 and 63 dB for the images at $f_{RF} + f_{s,BB}$ and $f_{RF} - f_{s,BB}$, respectively. In transistor-level simulations, 46 and 51 dB rejections are obtained, respectively. The shortfall is due to lowering of the quality factor of BPFs by the output resistance of IF gm-cells.

3.1.4 RF Low-Noise Transconductance Amplifier

To be able to amplify the RF signal located at any of the supported frequency bands, wideband noise cancelling LNA [12] appears to be a good choice. As the proposed receiver is based on sampling the input charge, the RF amplifier needs

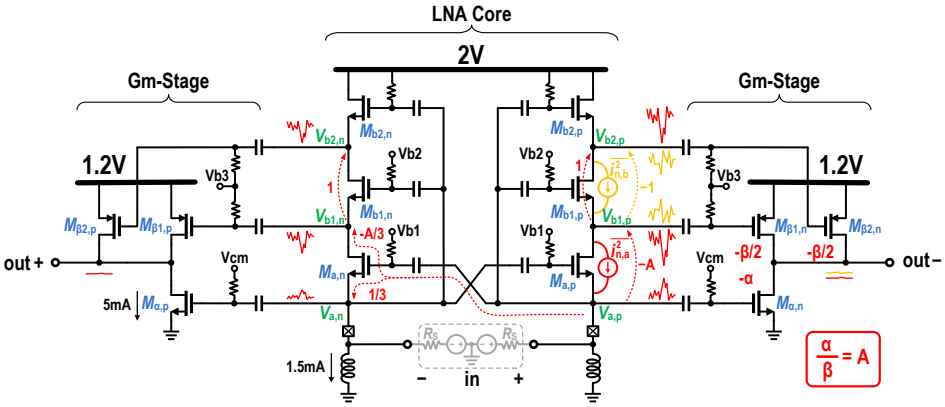


Figure 3.4: Wideband noise cancelling LNTA. Noise cancellation mechanisms of Ma and Mb1 is show in red and yellow, respectively.

to provide current rather than voltage, thus acting as a transconductance amplifier (TA) exhibiting a high output impedance. Core of the proposed LNTA in Fig. 3.4 is a combination of cross-coupled common-gate LNA [13] and common-gate-source-follower noise cancelling structure in [14]. The gm-stage produces the output current by adding three interstage in-phase signals generated by the LNA core. It can be shown that by properly sizing the output transistors, noises of M_a and M_{b1} transistor pairs are completely cancelled out and noise contribution of M_{b2} is significantly reduced.

The input transistor pair, Ma, provides the input matching. Thanks to cross-coupling of their gates to the differential input, input impedance (R_S) matching is achieved with half the input g_m, $g_{ma} = 1/(2R_S)$. Total gain of LNTA from input to output is provided by three paths: through V_a, V_{b1}, and V_{b2} nodes. It can be shown that, the total single-ended gain is:

$$g_{m,tot} = -\left(g_{m,\alpha} + g_{m,\beta}\left(2 + A\right)\right) = -2g_{m,\beta}\left(1 + A\right) \tag{3.10}$$

Also, total noise figure (NF) of the LNTA is calculated by referring noise contribution of M_{b2}, M_α and M_β from the output to the input, which is simplified to:

$$NF = 1 + \frac{\gamma_b}{4\left(1 + A\right)} + \frac{2\gamma_{\alpha,\beta}}{g_{m,tot}R_S} \tag{3.11}$$

where γ is MOS noise excess factor. The second term is due to noise of M_{b2} that is substantially reduced 4 times by the proposed noise splitting technique, and $1 + A$ times by signal gain from other paths. The third term is the total noise contribution of the g_m-stage that is reduced 2 times by the gain provided in the

LNA core. Fig. 3.5(a) plots noise figure of the LNTA with and without the noise splitting technique. Simulated noise figure and gm of our implementation is shown in Fig. 3.5(b). The parameter A is chosen to be about 1 (LNA core gain about 10 dB) in this design to have a balance between NF and IIP3. The covered LNTA frequency range is wideband: from 300 MHz up to 3 GHz (verified through measurements).

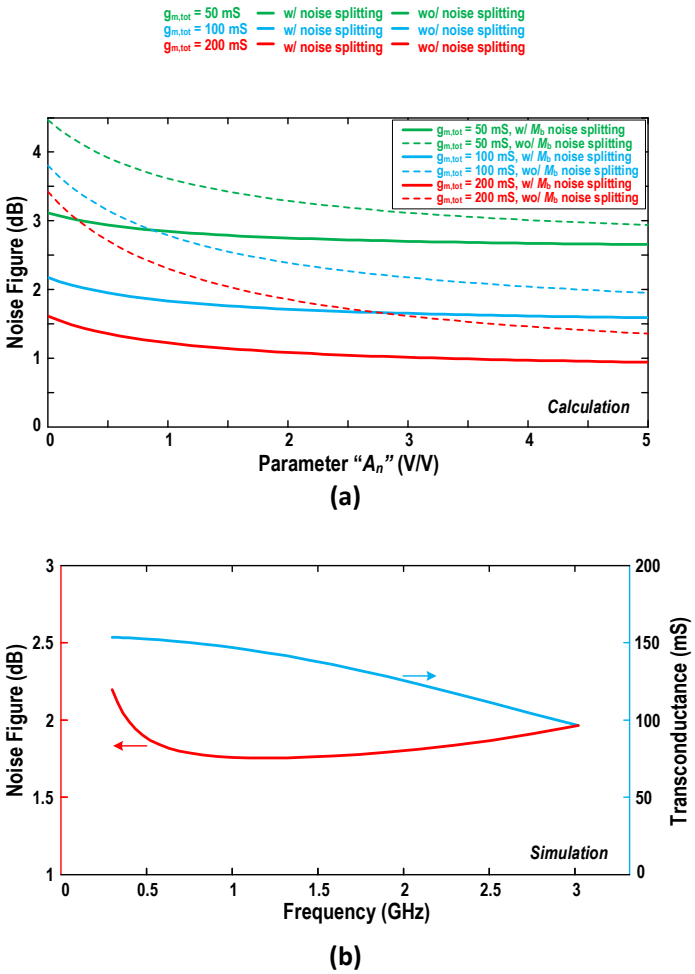


Figure 3.5: (a) Calculated LNTA noise figure versus A parameter (in Fig. 3.4), and (b) simulated noise figure and total g_m versus frequency, with S11< -10 across the range. Note that LNA core gain is $A + 2$.

3.1.5 Clock Waveform Generator

The RF mixer (Fig. 3.2) and IF BPF (Fig. 4.5) clocks are identical 25% duty-cycle clock waveforms at the LO frequency. First, an external clock at $2f_{LO}$ is fed in, then divided by 2 to generate four quadrature 50% clocks (LO_{1-4} in Fig. 3.6(a)). The divider consists of two latches arranged in a loop with a crossed feedback. As shown in Fig. 3.6(b) and (c), two clock-gated inverters with weak back-to-back inverters are used as a dynamic latch. Then, NAND gates are used to make the four 25% clocks (φ_{1-4}). The baseband clocks are generated similarly using standard cells with reference provided via a divide-by-4 of LO_1 clock.

3.1.6 DT Analog Baseband Signal Processing

The signal at the end of IF strip can be directly sampled and digitized using Nyquist-rate or band-pass ADC [15]. Afterwards, BB signal processing, including IF mixing and channel select filtering, can be done entirely in digital domain. However, this approach might not be always the most power efficient because of stringent sample rate and high dynamic range requirements imposed on the ADC. The alternative approach chosen in our implementation is to process the signal through DT analog BB, as shown in Fig. 3.7(a). The main goal of this BB strip is to reduce the required sample rate and dynamic range of the ADC by means of prior filtering and decimation. The proposed DT baseband consumes only a few milliwatts, while significantly saving power consumption of the ADC and digital BB.

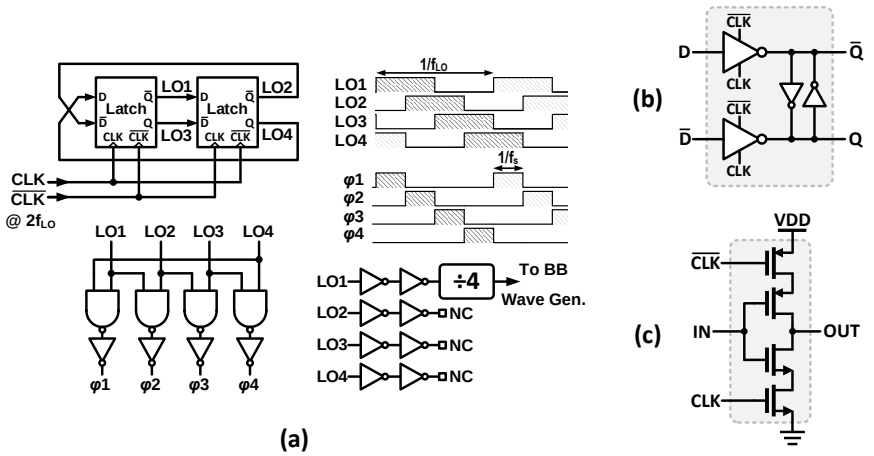


Figure 3.6: (a) RF and IF waveform generator. (b) Dynamic latch using (c) gated inverter.

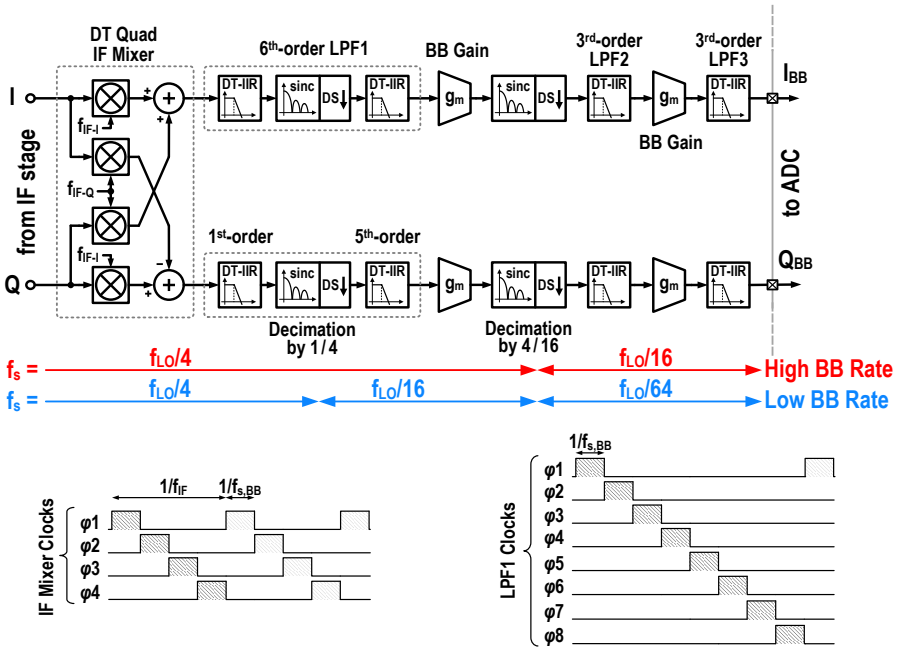


Figure 3.7: (a) Baseband DT signal processing of the receiver. (b) Required clock waveforms for the IF mixer and LPF1.

3.1.7 DT Analog Baseband Signal Processing

The first stage of the analog BB circuitry is a quadrature DT IF mixer. A set of *four* mixers downconvert the complex-valued IF signal to DC. Implementation of each mixer is similar to the passive RF mixer shown in Fig. 3.2. The baseband sample rate ($f_{s,BB}$) is chosen $4f_{IF}$ ($=f_{LO}/4$) to simplify the generation of IF mixer clocks. As shown in, the IF clocks are very similar to those in the RF mixer, but the period is $1/f_{IF}$. The IF mixer is the only circuitry in this receiver that limits the overall IIP2, even though it is still extremely high. Since the IF mixer is clocked at a much lower rate than the RF mixer, its IIP2 is substantially better [16]. Moreover, the IF filtering considerably improves its IIP2 referred back at the antenna.

The second stage of the analog BB strip is a channel-select DT 6^{th}-order LPF (IIR6), derived from the work in [3]. Fig. 3.8 shows the switch-level implementation. C_{H1} at the input port accumulates the input charge. Through a prearranged switching sequence, each of the C_S capacitors rotates the partial charge of C_{H1} to other history capacitors, CH_{2-6}, and then gets reset. Each charge-sharing operation within the cycle adds one order of filtering [3]. Using 8 sampling capacitors, each with a delay of one phase, increases the filter's sampling rate 8 times while using the same clock signals (parallelized operation). In the normal high sample rate

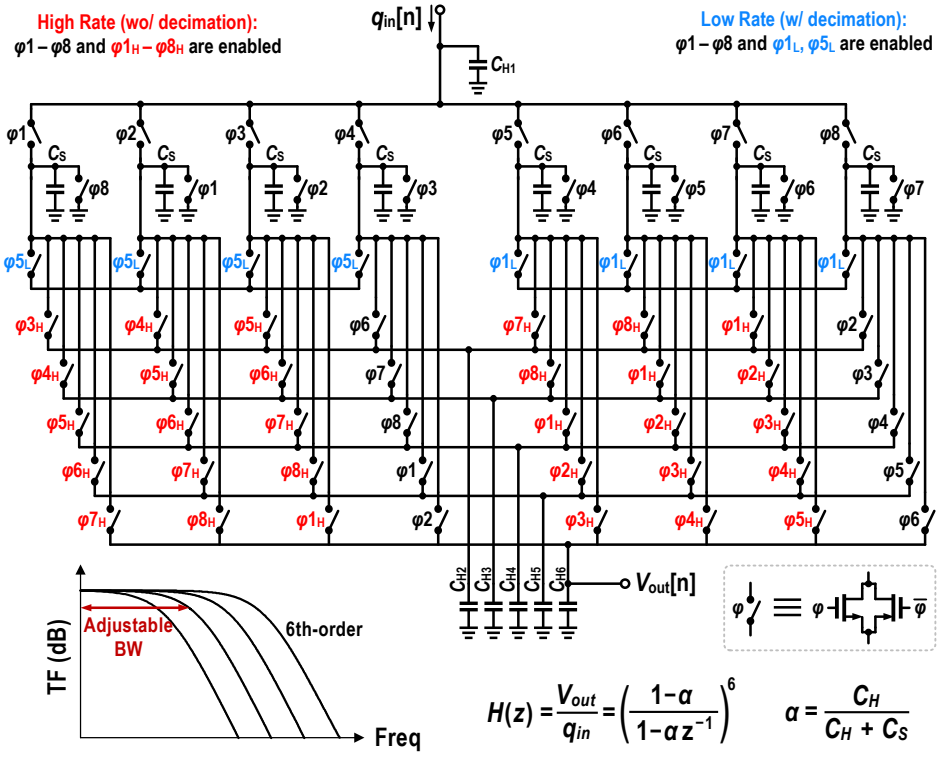


Figure 3.8: Implementation of the DT 6$^{\text{th}}$-order IIR low-pass filter with selectable decimation by 4.

mode, "black" and "red" switches are clocked and the filter works as described. This mode is used for high bandwidth signals up to 30 MHz (e.g., for the LTE standard). For narrowband signals (e.g., 200 kHz in GSM standard), the sample rate of $4f_{IF}$ (several 100s of MS/s) would be excessive, so further decimation should be done to save power. In this low sampling rate mode, only "black" and "blue" switches are clocked and the "red" switches are disengaged. After a set of four succeeding C_S's are charge-shared with C_{H1}, they are shorted together to make a spatial decimation by 4 [11]. Charge-sharing of the four C_S's makes a 4-tap MA as a *sinc* anti-aliasing filter prior to the subsequent decimation. Then one of them continues charge-sharing with CH_{2-6}. This also reduces the required C_H value to support the narrow bandwidth. Clock waveforms required for driving this filter are shown in Fig. 3.7(b).

Since the receiver path up to the end of IIR6 already enjoys ample gain and filtering, noise and IIP3 of the remaining stages are less of a concern so they can be implemented in an ultra-low-power fashion. After IIR6, two extra filter stages are cascaded with two g_m-cells. The g_m-cells are constructed as fully differential

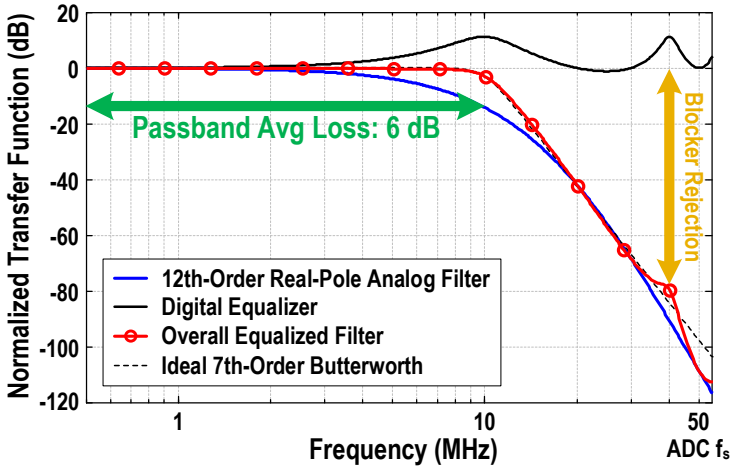


Figure 3.9: Digital equalization of 12$^{\text{th}}$-order real-pole transfer function to better than a 7$^{\text{th}}$-order Butterworth filter. The ADC and digital equalizer are clocked at 50 MHz.

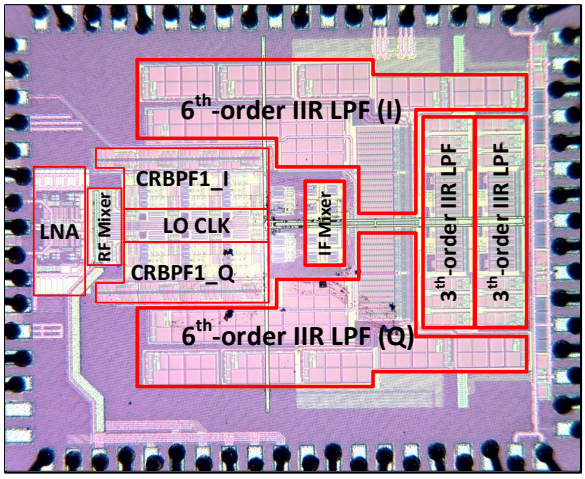


Figure 3.10: The proposed receiver's chip micrograph; 1.9×2.4 mm^2.

inverters. Both stages of the 3$^{\text{rd}}$-order IIR LPFs ("IIR3") are identical and use similar structure as in Fig. 3.8, though without spatial decimation. To further save power, their clocks are reduced by 4x. This creates a temporal decimation after the first baseband g_m-cell. At the bottom of Fig. 3.7(a), sample rate of each block from IF to the end of baseband is displayed. Due to the high total order of filtering, ADC sample rate could be further reduced below the receiver output sample rate without any other anti-aliasing filter.

3.1.8 Digital Equalization

Despite reaching the 12$^{\text{th}}$-order of DT analog filtering, only real-poles are realized. So this filter cannot be directly compared with complex-pole filter types (e.g., Butterworth). A high-order real-pole filter provides a gradual and smooth transition between its passband and its sharp out-of-band roll-off (Fig. 3.9). Therefore, [3] has proposed employing a low-power digital equalizer after the ADC to map the real-pole TF to a sharp complex-pole filter, but with a lower order. In Fig. 3.9, the total TF of BB filtering is mapped to a better 7$^{\text{th}}$-order Butterworth filter. In this way, passband of the filter experiences a small average loss of 6 dB, which can be compensated by the preceding gain stages or 1 additional ENOB in the ADC [3]. Taking into account the complete system-level view, the proposed BB processing consumes several times lower power (total I/Q baseband: 2.3 mW for 1.96 GHz RF input) than the conventional CT or active switched-capacitor approaches [17] while providing a much lower NF and a very high linearity [3].

3.2 Measurement Results

The receiver is implemented in standard TSMC 1P7M 65 nm CMOS and occupies an active area of 1.1 mm^2 (Fig. 3.10). It consists mostly of MOS switches, capacitors and inverter-based gm-cells, making it process scalable and amenable to digital deep-nanoscale CMOS. Majority of the chip area is occupied by capacitors used for baseband filtering that supports BB cutoff frequencies down to 100 kHz. Therefore, the chip area scales very well with the CMOS technology advancements.

Measured wideband transfer function of the complete receiver is plotted in Fig. 3.11. There are only discrete frequency points that can fold into the received band of interest. As analyzed in Section 3.1.3, major images (shown in yellow) are located at multiples of $4f_{IF}$ away from f_{RF}. The first two major images are rejected by 42 and 46 dB, which closely agrees with simulations. The reminder of images at f_{IF} multiples (in black) are much smaller, and are caused by the baseband decimations. The exception is the image of 37 dB rejection (marked in red) that was traced to uncalibrated I/Q clock mismatch. There, unaccounted parasitics on the mixer clock lines make the I/Q unbalanced. Based on simulations, a phase mismatch of about 1^o could lead to the measured degraded rejection. A more careful layout design solves this in future designs. Including an antenna preselect filter with a moderate out-of-band rejection of 35 dB, the total image rejection easily improves to better than 72 dB. Measured close-in transfer functions for different programmed bandwidths at low/high baseband rates are shown in Fig. 3.12. As a whole, RF bandwidth of the receiver is programmable from 200 kHz to 30 MHz.

Fig. 3.13(a) shows measured uncalibrated IIP2 and IIP3 at medium gain setting, in which the receiver meets the sensitivity specification in the presence of blockers.

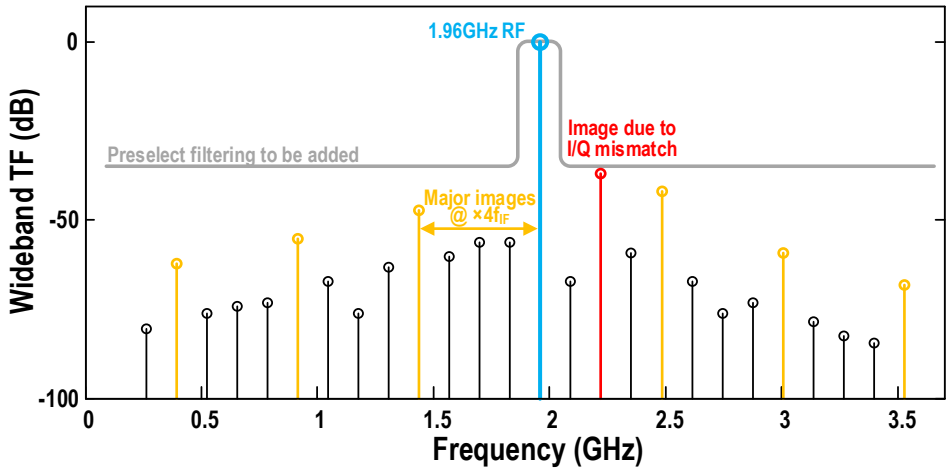


Figure 3.11: Measured wideband transfer function of the receiver.

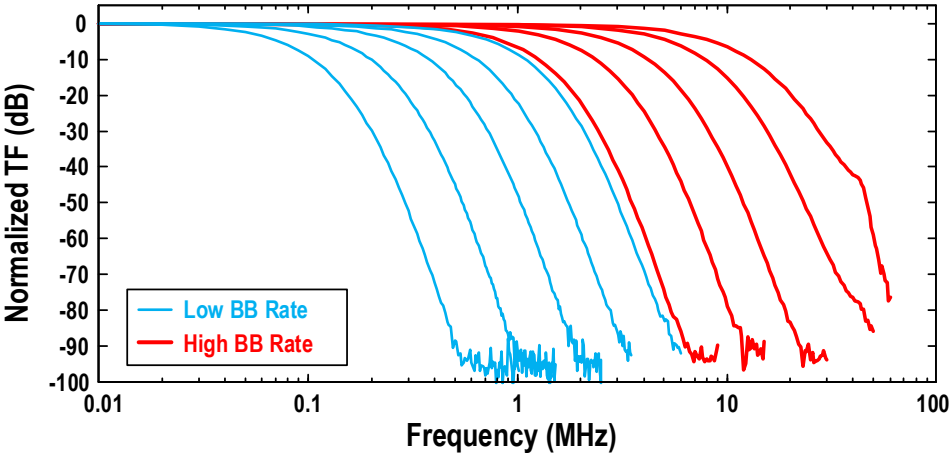
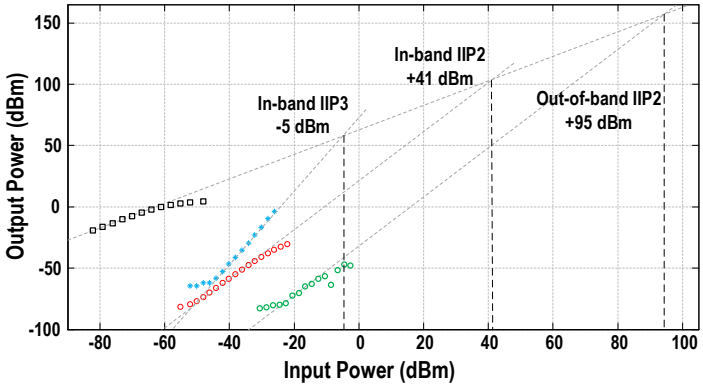


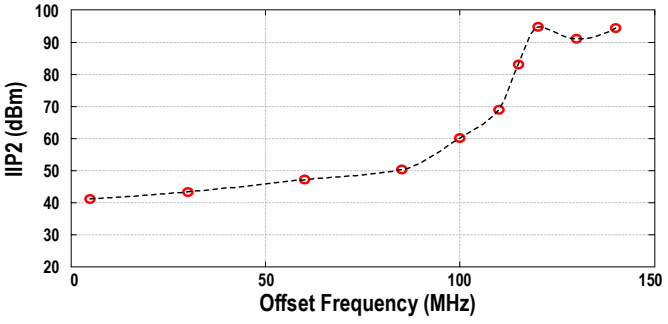
Figure 3.12: Measured close-in transfer function of the receiver.

In-band IIP3 is measured at −5 dBm, which is mainly limited by the linearity of IF g_m-cells. While the high-IF front-end has infinite IIP2, the IF mixer limits the receiver's IIP2. The IF filters in this receiver attenuate blockers and so, out-of-band IIP2 increases rapidly at higher frequency offsets (Fig. 3.13(b)), from +41 dBm in-band to +95 dBm at 120 MHz offset, all uncalibrated. Although this receiver does not claim to be SAW-less, the proposed architecture appears to be a path to reach such SAW-less operation that could meet most stringent IIP2 requirements, even in the FDD mode.

Plotted in Fig. 3.14, noise figure of the complete receiver is between 2.9–4.0 dB



(a)



(b)

Figure 3.13: (a) Measured IIP2 and IIP3. (b) Measured IIP2 versus offset frequency.

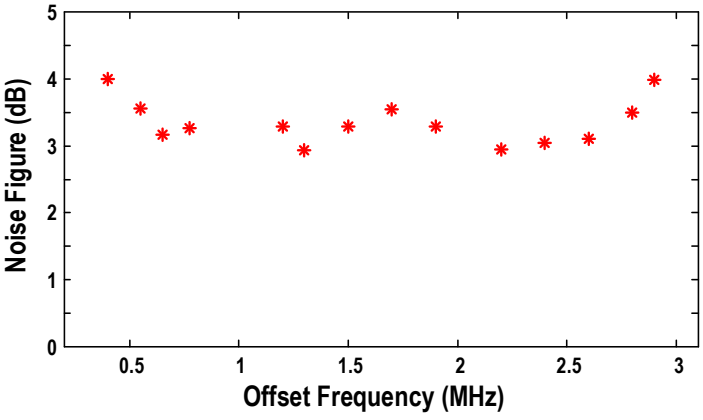


Figure 3.14: Measured noise figure of the complete receiver versus RF frequencies.

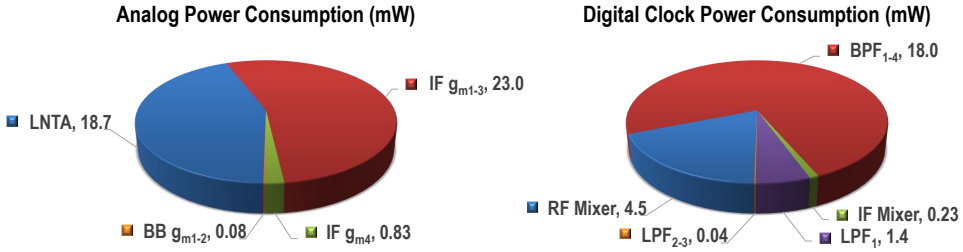


Figure 3.15: Power consumption budget of various blocks at maximum gain setting for 1.96 GHz RF input.

Table 3.1: Performance summary and comparison with state-of-the-art

	This Work	[9]	[15]	[18]	[6]	[19]	[20]	[21]
Technology	65 nm	65 nm	65 nm	90 nm	90 nm	65 nm	28 nm	90 nm
Architecture	Superhet.	Superhet.	Superhet.	Zero-IF	Zero-IF	Zero-IF	Zero-IF	Zero-IF
Description	Full DT	DT / N-Path	N-Path	Full DT	CT / DT	DT / CT	Full CT	Full CT
Analog BB / Order	Yes / 7th[§]	No	No	Yes / 2[¶]	Yes / 3[¶]	Yes / 2[¶]	Yes / 2[&]	Yes / 2[&]
RF Frequency (GHz)	0.4 – 2.9	0.5 – 1.2	1.8 – 2.2	0.5 – 3.8	0.8 – 6	0.5 – 3	0.4 – 6	0.8 – 2.2
Supply Voltage (V)	1.2 / 2	1.2	1.2 / 2.5	1.2	1.0 / 2.5	1.2 / 2.5	0.9	1.5
Power[†] (mW)	48 – 79	24.5	39	67 – 115	45.5 – 65.5	~ 210 – 540[#]	35 – 40	19.5 – 22.6
NF (dB)	2.9 – 4.0	7.5	2.8	5.3 – 6.0	5 – 5.5	5.5 – 8.8	1.8 – 3.1	2.2 – 3.2
Max Gain (dB)	83	35	55	58 / 64	> 47	35	70	61.5
In-band IIP3 (dBm)	-5	+10	-8.5	+1 / +2.5	-3.5	> -12.5	+4	N/A
Out-of-band IIP2 (dBm) / Calibration	+95 / No	–[*]	–[*]	38 – 52 / No	+60 / No	> +46 / No	+80 / Yes	+90 / Yes
Channel BW[‡] (MHz)	0.2 – 30	4.5	4	0.2 – 20	0.2 – 20	~ 26	1 – 100	~ 0.2 – 3.8
Area (mm^2)	1.1	0.45	0.76	0.5	3.8[##]	1.85[#]	0.6	–[*]

[†] At highest gain setting
[§] 12th-order real-pole mapped to a 7th-order Butterworth
[#] Synthesizer and bias is excluded
[‡] Two times BB bandwidth
[¶] Real-pole
[##] Including synthesizer
[*] Not reported
[&] Biquad

for different bands from 0.4–2.9 GHz. At higher frequencies, duty cycle of φ_{1-4} RF clocks is reduced because of a limited rise/fall times. Hence, the gain of RF mixer reduces, which directly degrades the RX noise figure.

Table 3.1 summarizes the measured RX performance and compares it with published state-of-the-art. The analog part consumes 43 mW in total for the high-gain setting. The clock waveform generator consumes 5–36 mW that linearly scales with f_{LO}. Fig. 3.15 shows power consumption budgeting of different blocks. Full chain of the receiver has a maximum gain of 83 dB.

3.3 Conclusion

The complete chain of discrete-time (DT) superheterodyne receiver with high reconfigurability for cellular and other wireless applications is described. The full monolithic integration is made possible by the proposed DT BPF. In addition to the insensitivity to flicker noise and time-varying DC offsets, the superheterodyne shows an extremely high IIP2 without requiring any calibration. This characteristic makes this architecture a suitable candidate for future SAW-less receivers that work in FDD mode. DT signal processing using passive switched-capacitor circuits makes this receiver process scalable. It only uses switches, capacitors, and inverter-based gm-cells. The use of a high-order, but very low-power and low-noise baseband DT filters, reduces the required ADC sample rate and dynamic range thus leading to a lower total power consumption.

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CHAPTER

4

Structure of Charge-Sharing Band-Pass Filter

A complex quadrature charge-sharing (CS) technique is proposed to implement a discrete-time band-pass filter with a programmable bandwidth of 20–100 MHz. The BPF is part of a cellular superheterodyne receiver and completely determines the receiver frequency selectivity. It operates at the full sampling rate (4x) (described in Chapter 2) of up to 5.2 GHz corresponding to the 1.2 GHz RF input frequency, thus making it free from any aliasing or replicas in its transfer function. Furthermore, the advantages of CS-BPF over other band-pass filters such as, N-path, active-RC, G_m-C, and biquad are described. A mathematical noise analysis of the CS-BPF and the comparison of simulations and calculations are presented. The entire 65 nm CMOS receiver, which does not include a front-end LNTA for test reasons, achieves a total gain of 35 dB, IRN of 1.5 $nV/\sqrt{Hz}$, out-of-band IIP3 of +10 dBm. It consumes 24 mA at 1.2 V power supply.

This chapter is based on a journal paper published in the IEEE Transactions on Circuits and Systems I (Regular Papers) [1].

4.1 Introduction

Monolithic RF receivers (RX) have conventionally used a zero/low intermediate frequency (IF) due to straightforward silicon integration of low-pass channel-select filtering and avoidance of images (when zero-IF) or their easy baseband filtering (when low-IF) [2–7]. However, their drawbacks, such as poor 2^{nd}-order non-linearity, sensitivity to $1/f$ (flicker) noise and time-variant DC offsets, are all getting ever more severe with CMOS scaling. These problems could be solved with increasing the IF frequency, as was the norm in the pre-IC era with superheterodyne radios. However, to avoid the interferers and blockers at IF images, a high quality (Q)-factor band-pass filtering (BPF) is required, which is extremely difficult to implement in CMOS using continuous-time circuitry.

The integration problem of high-IF BPF was solved in [8, 9] and [10]. A high-Q complex frequency translation ("N-path") filtering at the high-IF stage was used in [8] as an alternative to the conventional CT BPF. However, that filter cannot reject images defined as interferers at odd harmonics of the IF frequency because the N-path filter *inherently* features replicas there. Therefore, there is an increased demand for highly integrated BPFs that would be free from any of those replicas and still compatible with CMOS scaling suitable for superheterodyne RX. In [9, 10], we have proposed a full-rate charge-sharing (CS) discrete-time (DT) operation that is largely free from replicas and which additionally offers a freedom to change the IF frequency in face of large blockers, thus avoiding desensitization.

In this chapter, we describe in detail such high-IF DT BPF filter capable of realizing a fully integrated superheterodyne RX. The filter exploits passive switched-capacitor techniques and, as such, is amenable to CMOS scaling and is very robust to mismatches. Its center frequency and bandwidth are well controlled via clock frequency and capacitor ratios. Section 4.2 gives an overview of various types of bandpass filtering. Section 4.3 begins with basic principles of CS-BPF and then continues with detailed structure and continuous-time model of CS-BPF. The noise analysis of CS-BPF and circuit implementation of the front-end RX are presented in Section 4.4 and Section 4.5, respectively. The measurement results are demonstrated in Section 4.6.

4.2 Overview of Band-Pass Filtering

As an overview, transfer functions of different types of BPFs are compared in Fig. 4.1. CT filters, such as G_m-C and biquad, do not exhibit any aliasing or replicas but their structure is very complex and they consume a lot of power. Furthermore, their input-referred noise and linearity are much worse compared to other filters due to a number of active g_m-cells used. Active-RC filters are divided into two subcategories: sample-based and continuous-time. Both use opamps or g_m-cells as

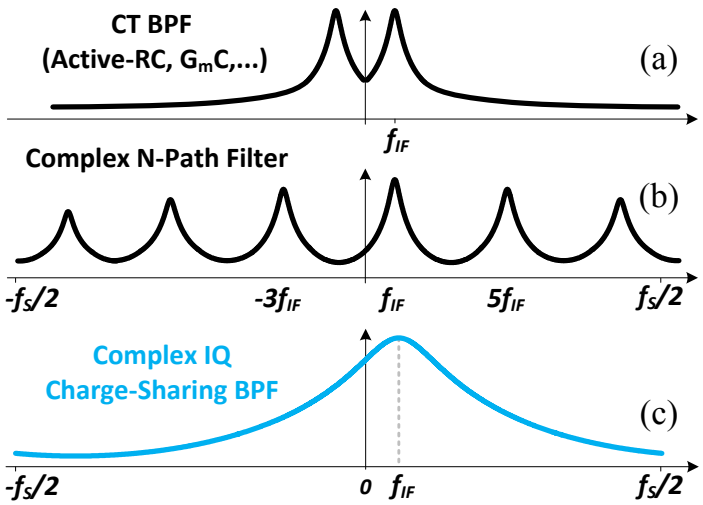

Figure 4.1: Transfer function comparison of different types of BPFs (a) CT BPF, (b) Complex N-path, (c) DT CS-BPF.

active components. They typically consume a lot of power and they also tend to be large in order to reduce flicker noise generated by the active devices.

Key advantage of the full-rate CS-BPF compared to the N-path filters [3, 11–14] is that its transfer function has only one peak in the entire sampling frequency domain of $-f_s/2$ to $f_s/2$, as shown in Fig. 4.1(c). Another advantage is that it features a theoretically infinite IIP2 compared to the limited IIP2 of N-path filters. The only drawback of DT CS-BPF compared to N-path filter is that it has a smaller Q-factor, which can be solved by cascading several CS-BPF stages or using a positive feedback [14].

The simplified block diagram of N-path filter is shown in Fig. 4.2, which comprises one mixer and baseband capacitor (C_{BB}) for a traditional N-path filter [13], or two mixers and C_{BB} for a modified N-path filter [15]. The input signal is down-converted to DC by the mixer, filtered by a low-pass filter, and then up-converted by the same [16] or another mixer [14, 15]. The 2^{nd}-order non-linearity of the mixer depends on LO frequency, and any mismatch in the mixer switching transistors [17]. The typical IIP2 of the mixer is between 50-70 dB [18]. Therefore, as illustrated in Fig. 4.2, in both the traditional and modified N-path filters, the IM2 product can be generated due to the down-conversion to DC by the mixer, which coincides with the wanted signal. However, the CS-BPF does not experience any frequency translation, thus no IM2 products.

As an application example of such a BPF, the feedback-based superheterodyne RX utilizing a charge-sharing (CS) technique and N-path notch filter was proposed in [9]. Although the N-path notch filter is used as a channel select filter, the N-path

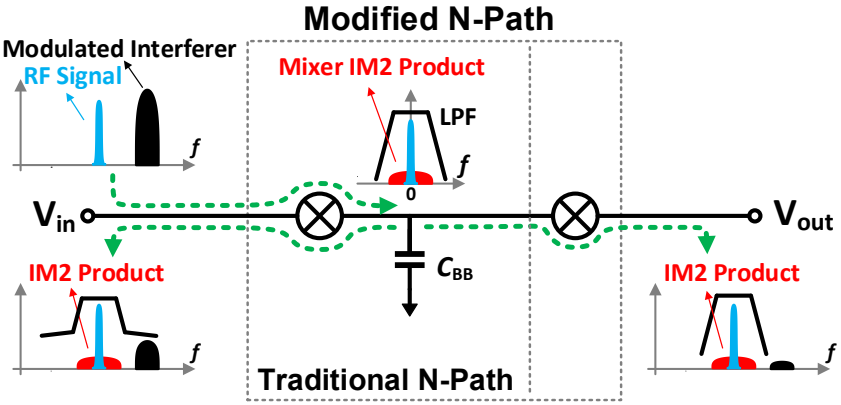

Figure 4.2: N-path filter and its 2nd-order non-linearity.

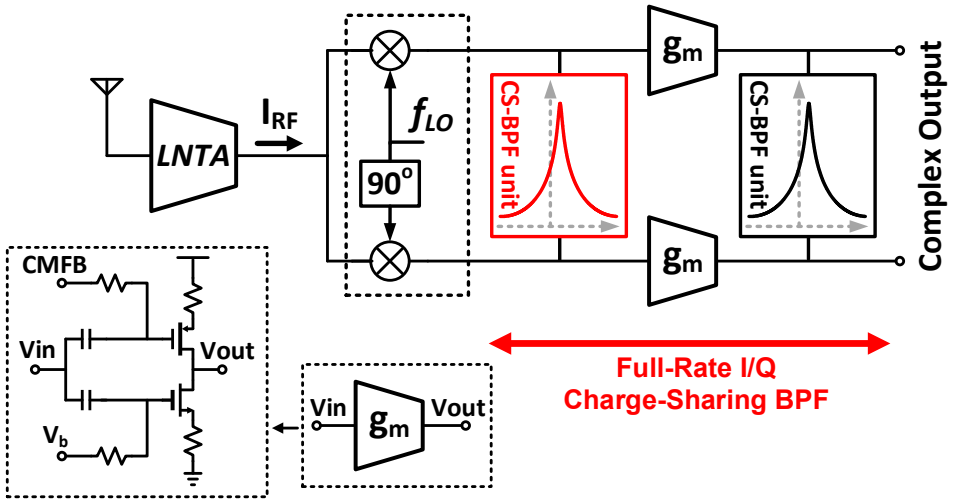

Figure 4.3: Block diagram of the high-IF receiver containing the proposed BPF and schematic of IF gm cell.

folding is of no concern there due to the strong protection offered by the preceding high-IF CS filters. Also, in [10], a complete fully integrated superheterodyne RX using the CS technique and a BB filtering was proposed. The folding due to the lower sampling frequency of the BB filters is also of no real concern as it is protected by the preceding high-IF CS filters.

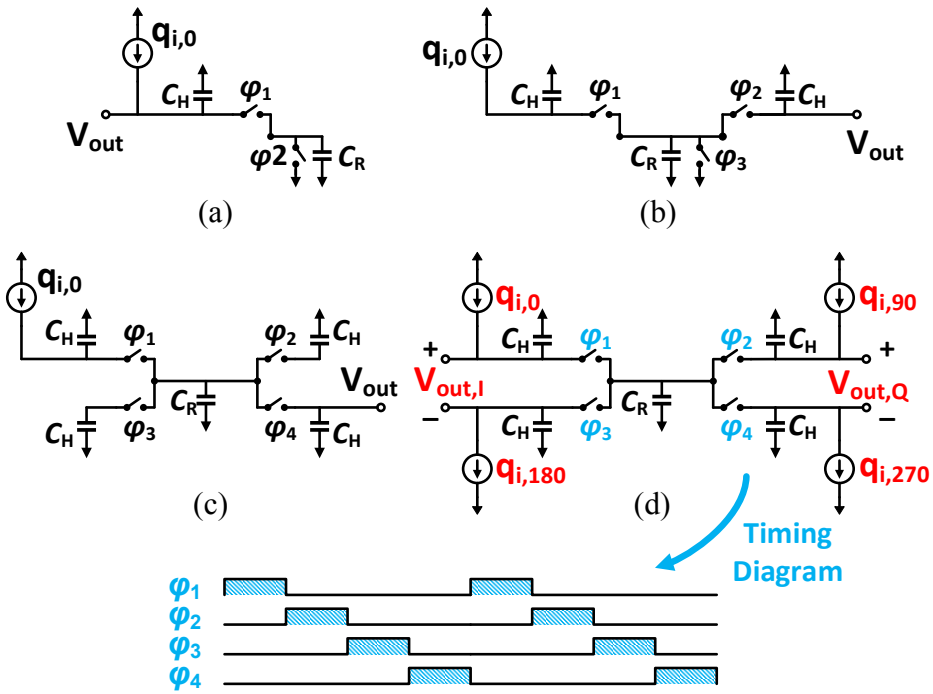

Figure 4.4: Basic concepts of DT charge-sharing IIR filtering: (a) 1st-order real-valued LPF filter; (b) 2nd-order real-valued LPF filter; (c) 4th-order real-valued LPF filter; and (d) 1st-order complex-valued BPF filter.

4.3 Charge-Sharing Bandpass Filter (CS-BPF)

The block diagram of the superheterodyne RX front-end is shown in Fig. 4.3. The RF signal of f_{RF} frequency is converted to current, $\mathrm{I_{RF}}$, via a low-noise transconductance amplifier (LNTA). Then, $\mathrm{I_{RF}}$ is down-converted to an intermediate frequency f_{IF} current $\mathrm{I_{IF}}$ by a passive mixer comprising commutating switches clocked at f_{LO} rate with rail-to-rail 25% duty-cycle. The $f_{IF} = |f_{LO} - f_{RF}|$ frequency could be in the 1–100 MHz range. However, to avoid the unnecessary increase in power of IF circuitry, f_{IF} should be placed just beyond the flicker noise corner of the devices comprising the RX circuitry [9]. Mixers driven by the 25% duty-cycle clocks have a higher conversion gain from RF to IF and also introduce less flicker noise compared to counterparts driven by the 50% duty-cycle clock [2]. Hence, this justifies our choice of the double-balanced mixer driven by the 25% clock.

The down-converted $\mathrm{I_{IF}}$ current flows into a complex full-rate I/Q CS-BPF. Multiple unit filters of 1st-order could be cascaded to get high-Q BPF centered at f_{IF}. The proposed filter provides enhanced RX selectivity and rejects unwanted blockers and images inherent to the high-IF architecture.

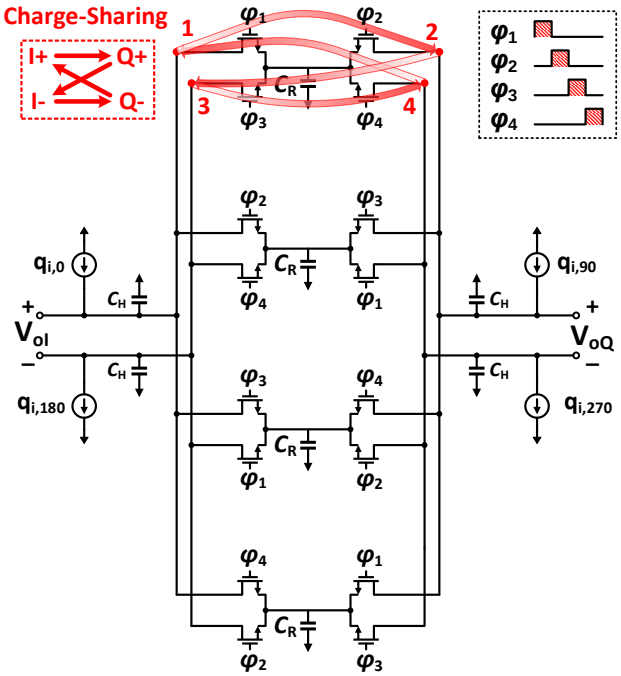

Figure 4.5: Complex CS-BPF unit circuit.

4.3.1 BPF Unit Structure

The well-known real-valued DT IIR low-pass filter (LPF) is shown in Fig. 4.4(a) [19]. The input charge packet is the integrated input current (provided by a g_m-cell) on C_H and C_R during φ_1 over a time window T_s. At φ_1 going inactive, C_R samples a portion, $C_R/(C_R + C_H)$, of the integrated input charge. As a result, the DT circuit shown in Fig. 4.4(a) has a 1$^{\text{st}}$-order DT IIR characteristic, with C_R acting as a lossy component ("switch-capacitor resistor") that leaks the total charge out of the system. Therefore, it prevents the C_H voltage from overflowing, thus ensuring stability. The order of the Fig. 4.4(a) DT IIR filter can be further increased to 2$^{\text{nd}}$ or 4$^{\text{th}}$, as shown in Fig. 4.4(b) and Fig. 4.4(c), respectively. At the end of φ_1, the sampled charge on C_R is just shared with another C_H capacitor. This mechanism can arbitrarily increase the IIR filter's order [20].

The basic quadrature (i.e., with four outputs) CS-BPF can be synthesized from the 4$^{\text{th}}$-order DT IIR filter (with a single real output) by applying input charge packets $q_{i,0}$, $q_{i,90}$, $q_{i,180}$ and $q_{i,270}$ with a multiple of 90$^{\text{o}}$ degree phase shifts, as shown in Fig. 4.4(d). During each phase of φ_1, φ_2, φ_3 and φ_4, four input charge packets are accumulated into their respective history capacitors, C_H. At the end of each phase, each C_R containing the previous packet is ready to be charge-shared with C_H

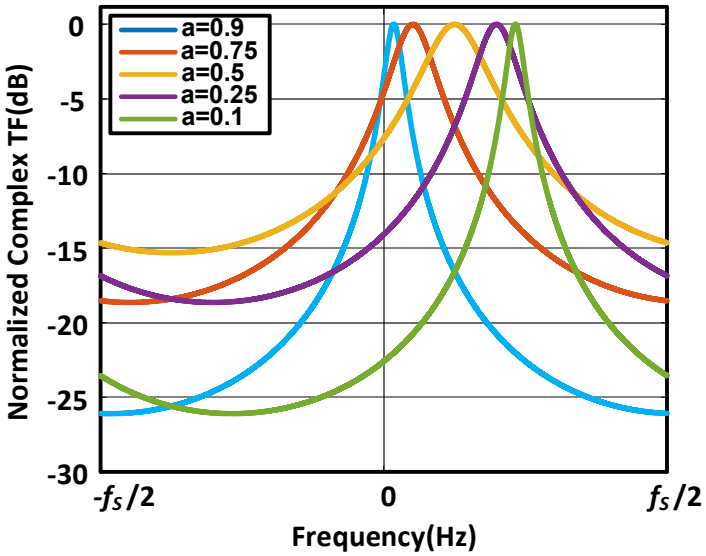

Figure 4.6: Ideal CS-BPF transfer function.

containing the current input charge packet and the “history" charge. Therefore, in each phase, rotating capacitor C_R removes a charge proportional to $C_R/(C_H + C_R)$ from each C_H and then delivers it to the next C_H. The four quadrature outputs can be read out at the sampling rate of $f_s = 1/T_s = f_{LO}$. In that case, The CS-BPF is not full-rate anymore and its sampling frequency would be equal to f_{LO}.

The basic concept of the I/Q charge-sharing filtering with *active* opamps was introduced in [21] for a different low-IF application with very low sampling rate of 1 Msample/s. In our work, the 5.2 Gsample/s CS-BPF is fully passive without any opamps, constructing DT filters that are much more robust to mismatches than the RC, LC and G$_m$-C type of filters because of the excellent capacitor matching in advanced CMOS. The other advantage of the proposed filter is that it is fully compatible with process scaling due to the filter's passive nature.

The schematic of the fully passive full-rate 1$^{\text{st}}$-order CS-BPF unit is shown in Fig. 4.5. The time-domain I/Q output voltage expressions at $t = nT_s$, can be written as

$$V_{oI}[n] = \frac{C_H V_{oI}[n-1] - C_R V_{oQ}[n-1] + q_{in,I}[n]}{C_H + C_R}, \tag{4.1}$$

and

$$V_{oQ}[n] = \frac{C_H V_{oQ}[n-1] + C_R V_{oI}[n-1] + q_{in,Q}[n]}{C_H + C_R}. \tag{4.2}$$

By defining the complex input charge as $q_{in,C} = q_{in,I} + jq_{in,Q}$ and complex output

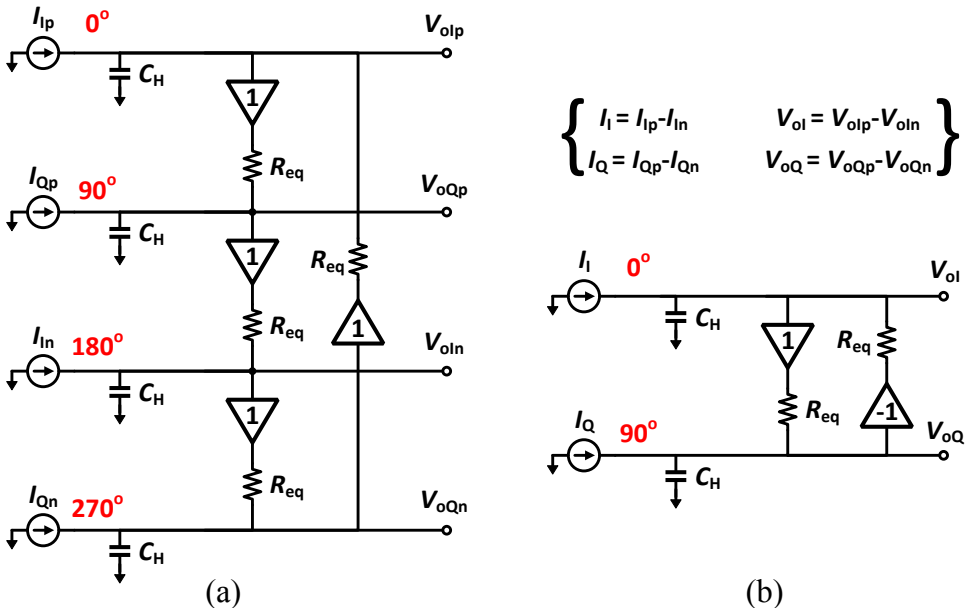

Figure 4.7: Schematics of the continuous-time model of quadrature DT CS-BPF with: (a) single-ended and (b) differential inputs.

voltage as $V_{oC} = V_{oI} + jV_{oQ}$, the z-domain complex transfer function of the filter can be derived as

$$H_{CS-BPF}(z) = \frac{V_{oC}(z)}{q_{in,C}(z)} = \frac{k}{1-(a+j(1-a))z^{-1}}, \tag{4.3}$$

where, $k = 1/(C_H + C_R)$, $a = C_H/(C_H + C_R)$. The position of CS-BPF complex pole is determined by a. According to (6.7), the charge-sharing technique forms a 1st-order complex filter. The ideal transfer functions of the filter for different a coefficients are shown in Fig. 4.6. The CS-BPF is acting as a LPF centered at DC in the extreme case of $a = 1$, while for the extreme case of $a = 0$, CS-BPF is acting as an N-path filter centered at $f_s/4$. Also, the filter bandwidth increases, when $a < 0.5$, and decreases, when $a > 0.5$ with the increase of the center frequency f_c.

4.3.2 CS-BPF Continuous-Time Model

The switched-capacitor circuit of CS-BPF can be modeled as an RC network for frequencies of interest below $f_s/10$. The continuous-time (CT) equivalent model of the DT CS-BPF is shown in Fig. 4.7 for (a) single-ended and (b) differential inputs. Phase of input currents (I_{Ip}, I_{Qp}, I_{In} and I_{Qn}) should be 0^o, 90^o, 180^o and 270^o, respectively, that can be generated with the conventional quadrature

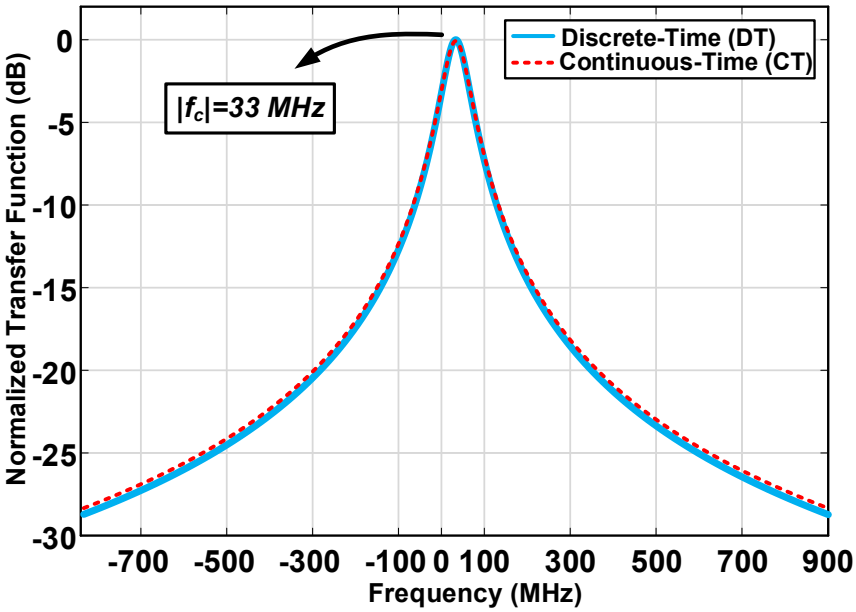

Figure 4.8: Transfer function comparison between the discrete-time CS-BPF and its continuous-time model.

current-commutating passive mixer. R_{eq} is an equivalent DT resistance of C_R and is equal to $1/(C_R f_s)$. The input currents are integrated into C_H's and the charge-sharing with C_R's is modeled with R_{eq} isolated by a unity-gain buffer to account for DT time-division duplexing (TDD) isolation between the quadrature paths. The CT transfer functions (TF) of Fig. 4.7(a) and (b) are ultimately the same. Since the differential input interpretation reduces the number of expressions to half, the differential TF analysis will be carried out below. The s-domain voltage-current expressions of the Fig. 4.7(b) circuit can be written as

$$V_{oI}(s) = I_I(s) \cdot \frac{R_{eq}}{1 + sR_{eq}C_H} - V_{oQ}(s) \cdot \frac{1}{1 + sR_{eq}C_H}, \tag{4.4}$$

and

$$V_{oQ}(s) = I_Q(s) \cdot \frac{R_{eq}}{1 + sR_{eq}C_H} + V_{oI}(s) \cdot \frac{1}{1 + sR_{eq}C_H}. \tag{4.5}$$

By defining a differential complex output as $V_{oC}(s) = V_{oI}(s) + jV_{oQ}(s)$, and differential complex input current as $I_{in,C}(s) = I_I(s) + jI_Q(s)$, the complex s-domain transfer function of the CS-BPF can be derived from (6.8) and (6.9) as

$$H(s)|_{s=j\omega} = \frac{V_{oC}(s)}{I_{in,C}(s)} = \frac{R_{eq}}{1 - j(1 - R_{eq}C_H\omega)}. \tag{4.6}$$

Consequently, the center frequency of the proposed CT-models lies at Fig. 4.7 is at

$$f_c = \frac{1}{2\pi R_{eq} C_H} \tag{4.7}$$

and the complex input impedance is equal to R_{eq}. Also, the bandwidth of the CS-BPF can be found from (6.10) and (6.7), which is equal to $1/(\pi R_{eq} C_H)$ for $a \approx 1$. Therefore, there is always a direct relationship of $f_c \approx \mathrm{BW}/2$ for $a \approx 1$. It should be mentioned that (6.10) can be derived from (6.7) by performing a bilinear transformation with an approximation of $sT_s < 2$ and substituting $z = (2 + sT_s)/(2 - sT_s)$ and $s = j\omega$ into (6.7). As an example, for a CS-BPF with $C_R = 1\,\mathrm{pF}$, $C_H = 19\,\mathrm{pF}$ and $f_s = 4\,\mathrm{GHz}$, we find $R_{eq} = 250\,\Omega$ and $f_c = 33.5\,\mathrm{MHz}$. The corresponding DT and CT transfer functions are plotted in Fig. 4.8 and show excellent agreement.

4.4 Noise Analysis of CS-BPF

The total output noise of the CS-BPF contains the noise of all switches within the passive switched-capacitor network. At first, let us analyze the noise of the simplest switched-capacitor circuit in Subsection *A*. Afterwards, the detailed noise analysis of the CS-BPF will be described for DT/CT model in Subsection *B*.

4.4.1 Voltage Sampler Output Noise

A voltage sampler that includes noise of its switch is drawn In Fig. 4.9(a). Let us assume that V_{in} is zero. When the switch is turned on, it has a finite resistance R_{on}. A series voltage source models the resistor's thermal noise with a constant power spectral density (PSD), as shown in Fig. 4.9(b).

$$S_R(f) = 4kTR_{on}, \qquad f \geq 0 \tag{4.8}$$

where k is Boltzmann constant and T is the absolute temperature. When the switch is on, noise of the resistor is shaped by the RC filter with a time constant of $\tau = R_{on}C_R$ and then appears at the output. At the moment the switch is disconnected, the output noise is sampled and held on C_R. The periodical sampling at f_s causes noise folding from frequencies higher than $f_s/2$, to the 0-to-$f_s/2$ range where they add up, as shown in Fig. 4.9(c). If the time constant τ is much shorter than the turn-on time of the switch, it can be shown that the summation of all folded noise will be flat (i.e., white noise) [22]. As shown in Fig. 4.9(d), the single-sided noise spectral density of the sampled output noise is [22]

$$\overline{v_n^2}(f) = \frac{kT}{C_R f_s/2}, \qquad 0 \leq f \leq f_s/2. \tag{4.9}$$

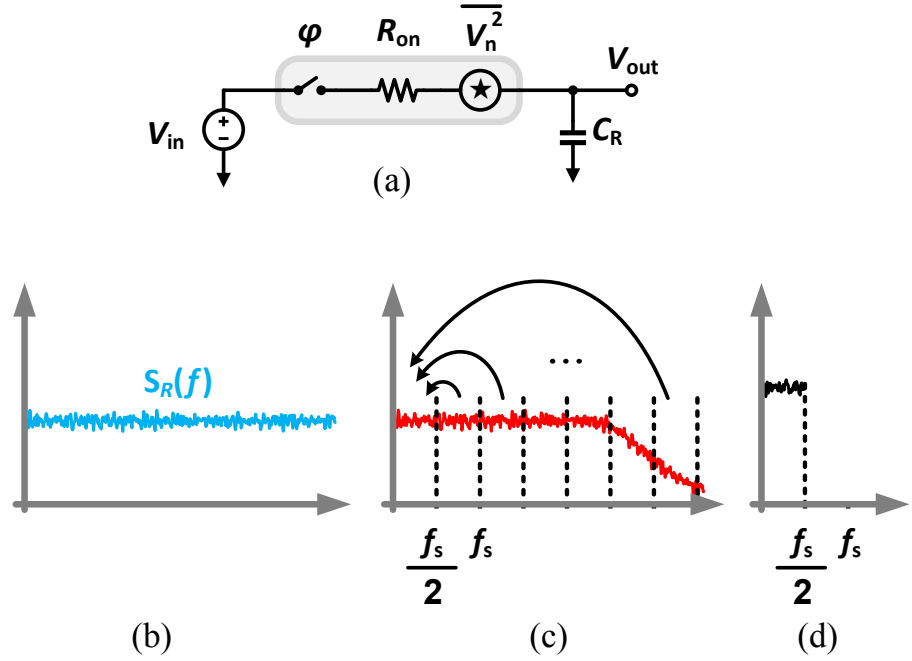

Figure 4.9: (a) Noise circuit model of a voltage sampling process. (b) Noise of a switch resistance. (c) Noise shaped by RC filter. (d) Sampled noise.

It should be noted that the integrated power density of this noise over the entire frequency range is kT/C_R.

To simplify calculations for more complicated switched-capacitor circuits, we can make the following assumption: the continuous-time noise source with PSD of (4.8), can be considered as a discrete-time noise source with PDS described in (4.9). In this way it is not necessary anymore to consider the effect of RC filtering.

4.4.2 DT CS-BPF Noise Model

The simplified noise model of CS-BPF for only one C_R is shown in Fig. 4.10. The input charge packets are assumed zero and the switches are assumed ideal. The first purpose of the following calculations is to find the DT output noise levels $V_{oIp}, V_{oQp}, V_{oIn}$, and V_{oQn} generated by input noise sources $\overline{V_{n1}^2}, \overline{V_{n2}^2}, \overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$. The second purpose is to find the total pseudo-differential output noise of I or Q paths in both DT and CT models. The above mentioned input noise sources have two conditions: (1) they are uncorrelated, and (2) the stochastic value of each of them is equal to (4.9). We first assume $\overline{V_{n2}^2}, \overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$ are zero, to calculate the noise transfer function only from $v_n = \sqrt{\overline{V_{n1}^2}}$ to all outputs. The time-domain noise

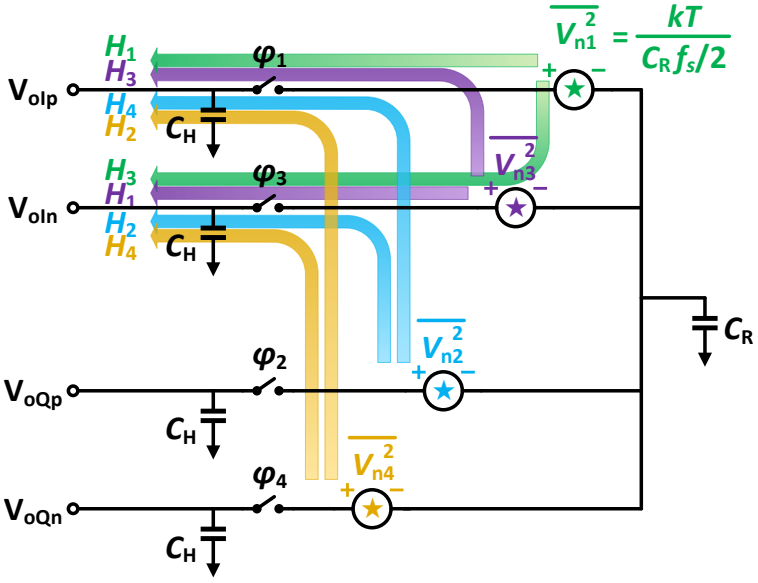

Figure 4.10: CS-BPF noise model for only one of the switches

outputs at $t = nT_s$ with respect to the input noise source $v_n[n]$ can be written as

$$V_{oIp}[n] = aV_{oIp}[n-1] + bV_{oQn}[n-1] + bv_n[n], \tag{4.10}$$

$$V_{oQp}[n] = aV_{oQp}[n-1] + bV_{oIp}[n-1] - bv_n[n-1], \tag{4.11}$$

$$V_{oIn}[n] = aV_{oIn}[n-1] + bV_{oQp}[n-1], \tag{4.12}$$

and

$$V_{oQn}[n] = aV_{oQn}[n-1] + bV_{oIn}[n-1] \tag{4.13}$$

where, $a = C_H/(C_H + C_R)$, and $b = 1 - a$ are the same as before. By converting the time-domain expressions to z-domain, we find DT noise transfer functions as,

$$H_1 = \frac{V_{oIp}}{v_n} = -\frac{b(1-az^{-1})^3 - b^3z^{-4}}{b^4z^{-4} - (1-az^{-1})^4}, \tag{4.14}$$

$$H_2 = \frac{V_{oQp}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right), \tag{4.15}$$

$$H_3 = \frac{V_{oIn}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right)^2, \tag{4.16}$$

and

$$H_4 = \frac{V_{oQn}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right)^3. \tag{4.17}$$

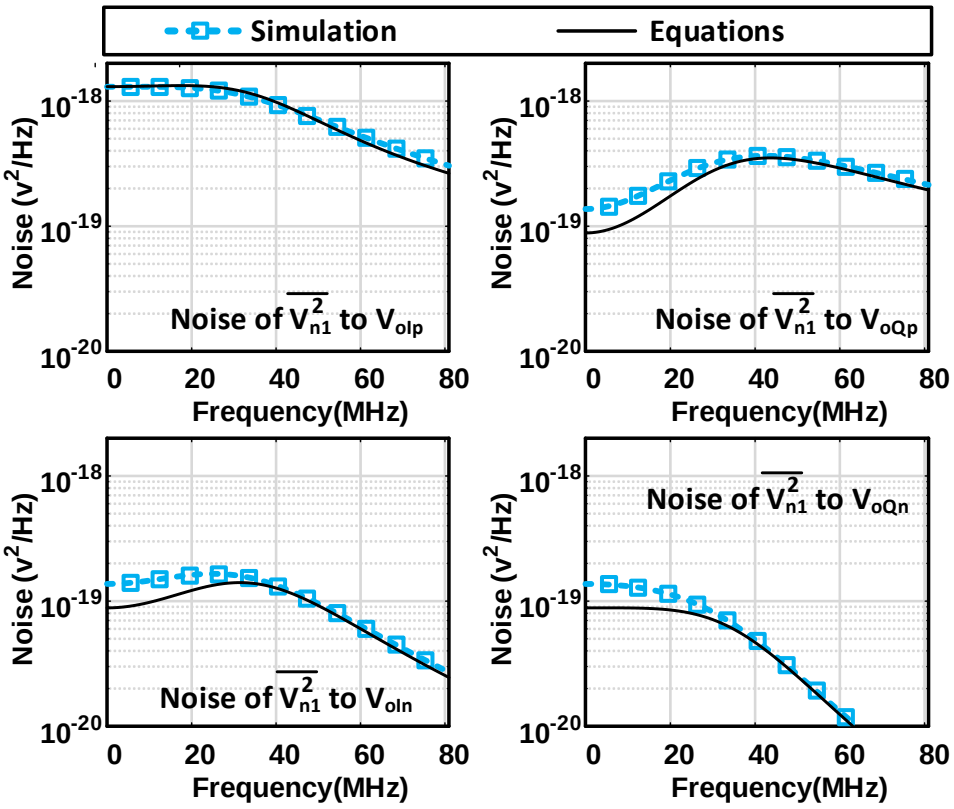

Figure 4.11: Output noise PSD calculations compared with transistor-level simulations.

The above expressions are derived based on the assumption of $\overline{V_{n2}^2}$, $\overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$ being zero. It should be mentioned that, since the circuit is symmetric for all four input noise sources in Fig. 4.10, the noise TF of other DT input noise sources to output combinations are exactly the same as (4.14)–(4.17). The only difference is that the outputs in the expressions should be changed according to the DT input noise sources; for instance the noise TF of $\sqrt{V_{n3}^2}$ to V_{oIn} is the same as (4.14). The detailed noise TF for each DT input noise is also illustrated in Fig. 4.10. To calculate a differential DT output noise ($V_{on} = V_{oIp} - V_{oIn}$) with respect to all four input noise sources, we should consider that the differential DT output noise is composed of a sum of four uncorrelated noise contributions, as shown in Fig. 4.10. Also, each of them has two correlated noise contributions in the differential output. The correlated noises are shown with the same color (see Fig. 4.10). Therefore, we find the DT differential output noise PSD as

$$\overline{V_{on}^2} = \left|(H_1 - H_3)^2\right| \overline{V_{n1}^2} + \left|(H_4 - H_2)^2\right| \overline{V_{n2}^2} + \left|(H_3 - H_1)^2\right| \overline{V_{n3}^2} + \left|(H_2 - H_4)^2\right| \overline{V_{n4}^2}. \tag{4.18}$$

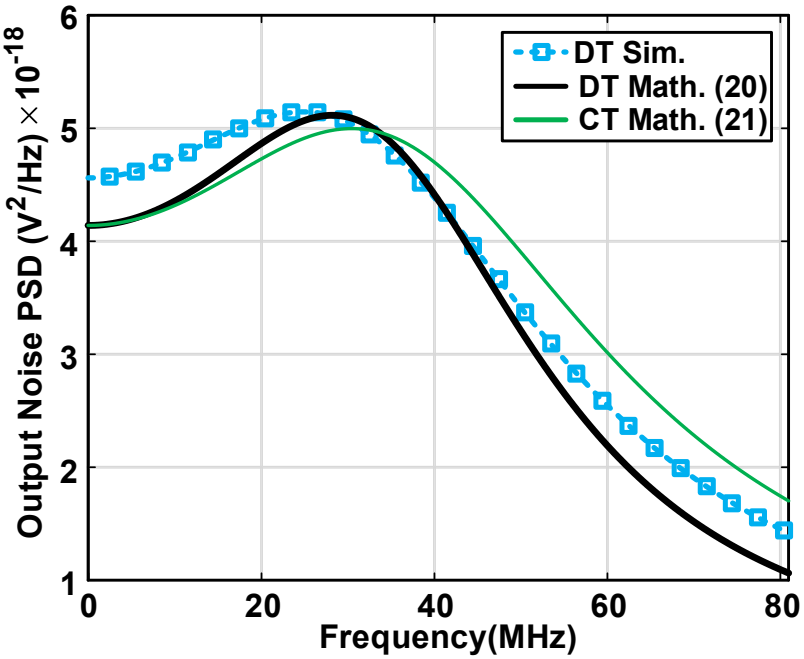

Figure 4.12: Output noise PSD calculations compared with simulations.

Since the absolute value of four input sources are the same, (4.18) can be simplified as

$$\overline{V_{on}^2} = \left(2\left|(H_1 - H_3)^2\right| + 2\left|(H_2 - H_4)^2\right|\right) \cdot \overline{V_{n1}^2}, \tag{4.19}$$

$$\overline{V_{on}^2} = \frac{2\,b^2\left(\left(\cos\left(\frac{w}{fs}\right)\right)^2 b - a\cos\left(\frac{w}{fs}\right) + a^2\right)}{(b^2+a^2)\left(\cos\left(\frac{w}{fs}\right)\right)^2 + (2\,b^3 - 4\,b^2 + 4\,b - 2)\cos\left(\frac{w}{fs}\right) + a^2\,(b^2+1)} \cdot \left(\frac{kT}{C_R f_s/2}\right) \tag{4.20}$$

and by substituting $z = e^{j\omega/f_s}$, the differential output noise PSD is simplified to (4.20). The comparison of calculated output noise PSD based on (4.14)-(4.17) with transistor-level simulations are illustrated in Fig. 4.11, for C_R=4 pF, C_H=19 pF, and $f_s = f_{LO} = 1$ GHz. The differential output noise PSD of the CT model of Fig. 4.7 can be calculated based on the same approach; DT noise PSD derived in (4.20). We find the total CT differential output $(V_{oIp} - V_{oIn})$ noise PSD as

$$\overline{V_{on}^2}(\omega) = \left(\frac{2(R_{eq}C_H\omega)^2 + 4}{(R_{eq}C_H\omega)^4 + 4}\right) \cdot (4kTR_{eq}). \tag{4.21}$$

It should be pointed out that integrating the DT differential output noise PSD

in (4.20) over 0-to-$f_s/2$ yields kT/C_T, with C_T being the total differential output capacitance equal to $(C_H + C_R)/2$. On the other hand, integrating the CT noise PSD in (4.21) over the entire range of 0 to ∞ is again equal to kT/C_T, with $C_T = C_H/2$. Note that the unity gain buffers in Fig. 4.7 are merely conceptual to account for the DT isolation, hence noiseless. If one were to implement the CT circuit of Fig. 4.7, noise contributions of the buffers would have to be accounted for. Consequently, the DT CS-BPF of Fig. 4.5 has a potential to out-perform its CT counterpart.

As the final verification, Fig. 4.12 compares the total output spot noise plots obtained via the diverse means: calculated DT, based on (4.20); calculated CT, based on (4.21); and schematic-simulated DT. The following conditions are used: C_R=4 pF, C_H=19 pF, and $f_s = f_{LO} = 1$ GHz. Although all simulations and calculations are performed for the CS-BPF with one C_R, the presented approach is valid for the full-rate CS-BPF with only one difference: the f_s in full-rate CS-BPF is 4 times higher than CS-BPF with one C_R.

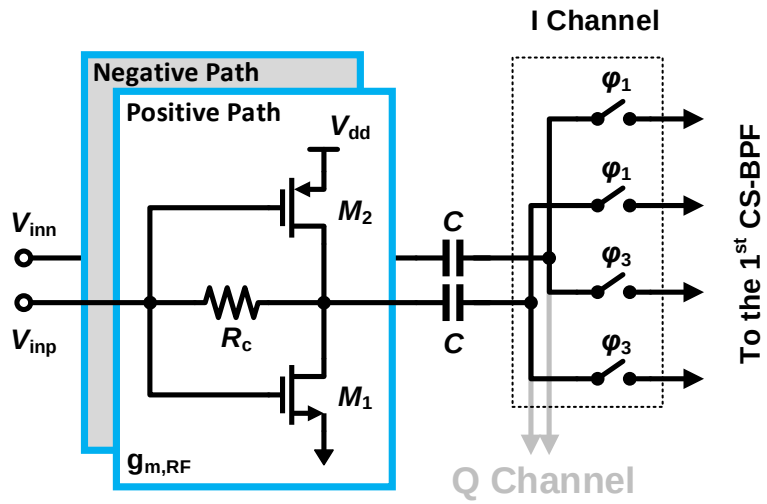

Figure 4.13: Circuit implementation of g_{mRF} and mixer.

4.5 Circuit Implementation

To accurately measure the BPF linearity, we have replaced the LNTA with a simple self-biased inverter-based transconductance amplifier (g_{mRF}) for higher IIP3, and designed for small transconductance as not to degrade the linearity. Since the gain provided by g_{mRF} is small, its contribution to the input-referred-noise (IRN) is predominant. The schematics of the g_{mRF} and RF mixer are shown in Fig. 4.13.

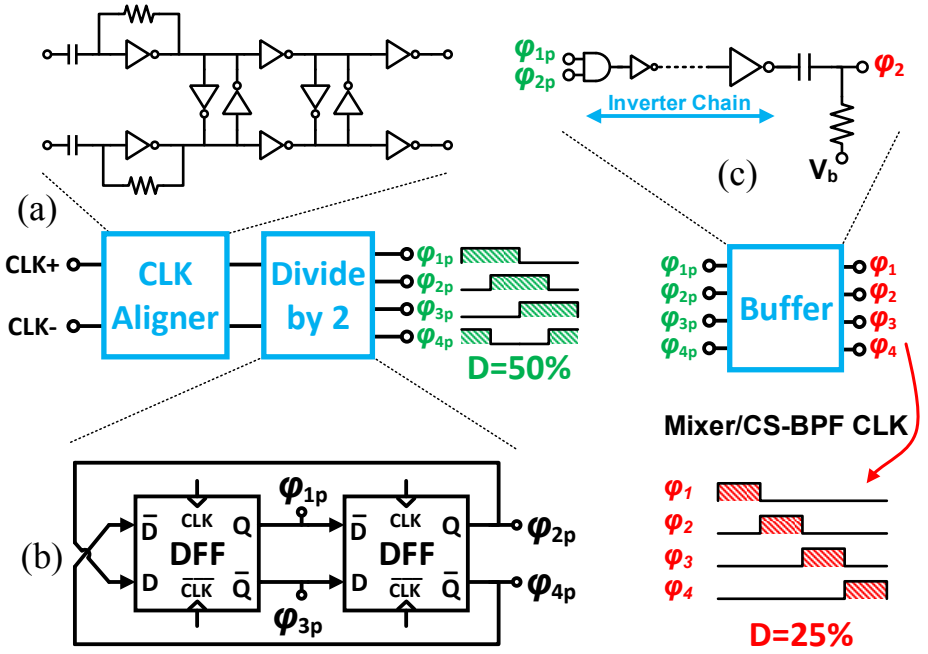

Figure 4.14: Schematic of the clock generation circuit (a) CLK aligner circuit, (b) Divider and (c) 25% clock generation circuit with buffer stage.

The self-biasing of g_{mRF} is accomplished by R_c resistors connecting its input and output. The value of R_c in parallel with the output impedance of g_{mRF} should be high enough as not to degrade the Q of 1st CS-BPF. The DC block capacitors (C) are used to eliminate the DC current flowing into CS-BPF. The differential RF input voltage to g_{mRF} is converted to a pseudo-differential AC current feeding the commutating CMOS passive mixers of I and Q channels. The RF mixer in Fig. 4.13 is only shown for the I channel.

The clock phases φ_1 and φ_3 comprise a pseudo-differential 25% duty-cycle (D) LO clock driving the CMOS switches. Fig. 4.14 presents the clock generation circuit for both the mixer and CS-BPF. The differential input clock, CLK, with D=50% is applied to the aligner circuitry that is responsible to compensate for any phase mismatch between the CLK+ and CLK- differential phases. The CLK aligner circuit (see Fig. 4.14(a)) consists of two inverters at the input to convert the sinusoidal inputs to the square-wave clock with D=50% and the two stages of back-to-back inverters for further aligning the complementary edges of the square-wave clock.

As shown in Fig. 4.14(b), the divide-by-2 circuit consists of two D flip-flops arranged in the loop to generate the D=50% clocks, φ_{1p}, φ_{2p}, φ_{3p} and φ_{4p}, with 25% delay between adjacent edges. The mixer clock is generated by the buffer

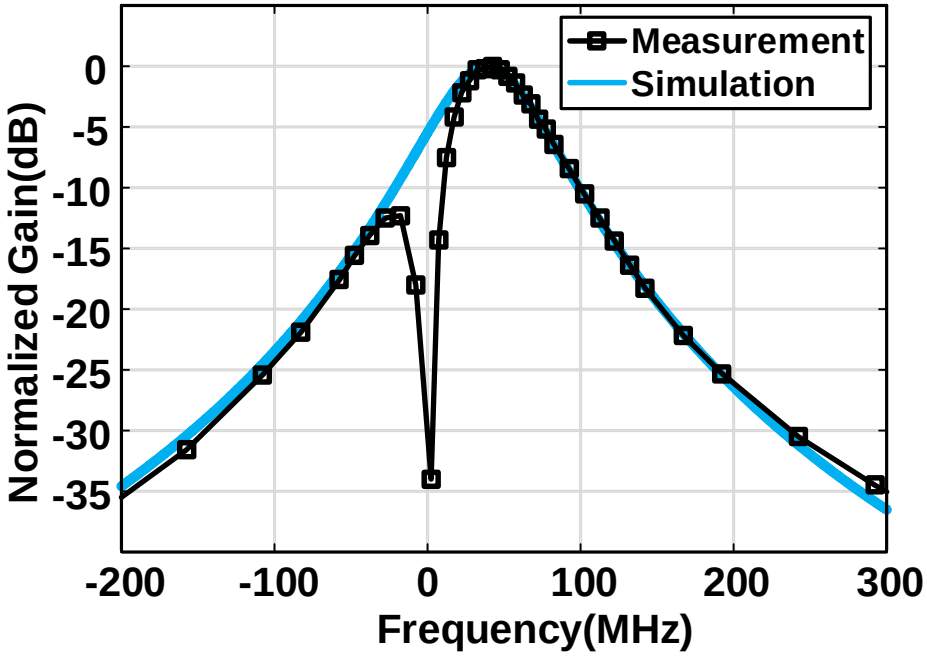

Figure 4.15: Comparison of measured transfer function with an ideal transfer function that includes output impedance of g_m-cells.

shown in Fig. 4.14(c). The CS-BPF switches are driven by the clocks generated in another buffer with the same schematic as drawn in Fig. 4.14(c). It comprises AND gates and the chain of inverters for proper driving of the load capacitance of NMOS switches. Also, to increase the driving capability of sampling switch transistors in the quadrature mixer and CS-BPF, a clock boosting technique (using V_b, see Fig. 4.14(c)) is utilized to increase gate-source voltage while the pass transistor is turned on.

The CS-BPF operates at clock frequency f_{LO} with 25% duty-cycle clocks and its effective (i.e., differential I/Q) sampling frequency f_S is equal to $4f_{LO}$. Thus, the effective sampling time T_S is equal to $1/(4f_{LO})$. In order to maximize linearity, it is crucial to set the switch sizes of Fig. 4.5 in such a way that T_S would be between 3τ–4τ. τ is the $R_{on}C_R$ time constant of the DT circuit and R_{on} is an equivalent resistance of the sampling transistor in the triode region. The output resistance of the IF g_m-cell should be at least 3x higher than R_{eq} in order to not decrease the Q and bandwidth of the following CS-BPF.

4.6 Measurement Results

The proposed RX with the same structure as Fig. 4.3 but with three-stage CS-BPF together with its surrounding circuitry was fabricated in TSMC 1 poly and 7 metal layers 65 nm CMOS. The chip micrograph is shown in Fig. 4.16. The implemented RX occupies 0.45 mm^2 active area and consumes 24.5 mA at 1.2 V power supply.

4.6.1 Test Setup

The proposed front-end IC is wire-bonded to a printed circuit board (PCB) providing DC and RF input connectivity ports, while high-IF output signals are measured with a high performance oscilloscope, as shown in Fig. 4.17. The transfer function measurement setup of the RF CS-BPF is shown in Fig. 4.17(a). After providing the proper power supply voltages, the LO frequency and RF input frequency should be applied to the RF front-end. The quadrature (I/Q) IF outputs are connected to high performance "RTO 1044" digital oscilloscope and the process of taking fast fourier transform (FFT) from the IF output signals has performed with it's own digital oscilloscope software GUI. The IF g_m-cell gains and the value of C_H and C_R capacitors controlled by the DIP switch shown in Fig. 4.17(b).

The measured complex transfer function of the RX is shown in Fig. 4.15. The measured curve is also compared to an ideal mathematic transfer function that includes the output impedance of all g_m-cells, which was extracted from transistor-level simulations. The measured curve shows a very good agreement with the mathematic modeling except for a notch at DC. It is due to the high-pass characteristic of a DC block capacitor in the g_m-cell (see Fig. 4.3) together with the resistor providing bias and common-mode voltages.

To demonstrate the CS-BPF reconfigurability, the measured transfer functions for different center frequencies f_c and bandwidths are depicted in Fig. 4.18. The transfer function rejection of the filter improves by increasing frequency without having any replica the same as Fig. 4.1(c). The measured center frequency of transfer functions are controlled by changing C_H (see Eq. (4.7)). C_H capacitors are implemented as a digitally switchable binary weighted capacitor using the conventional MOM capacitors and MOS switches. Hence, the C_H value can be changed via 6 digital bits.

The complete front-end provides a total gain of 35 dB at the maximum gain setting. The measured and simulated IRN of the front-end are shown in Fig. 4.19. The abrupt increase in IRN at the low frequencies is caused by the flicker-noise of the g_m-cell at IF stage. As discussed in Section 4.3, this curve suggests that the IF frequency should be placed at 30 MHz or a bit higher. Also, the reason that the measured IRN is high is that the front-end (g_{mRF} and 1^{st} CS-BPF) gain is low not to sacrifice the linearity of the RX. As a consequence the higher IRN is measured.

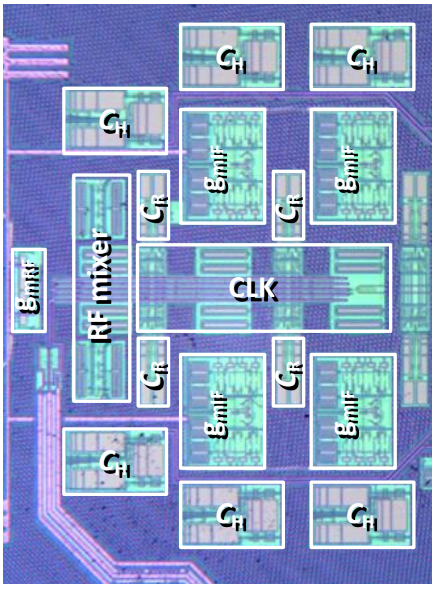

Figure 4.16: Chip micrograph.

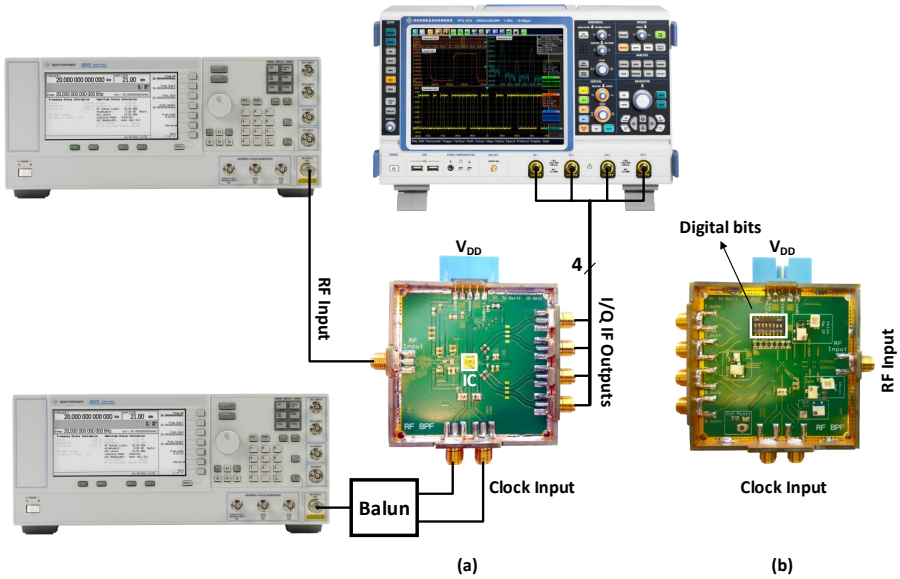

Figure 4.17: (a) Measurement setup and PCB of the proposed front-end for top layer, (b) PCB bottom layer.

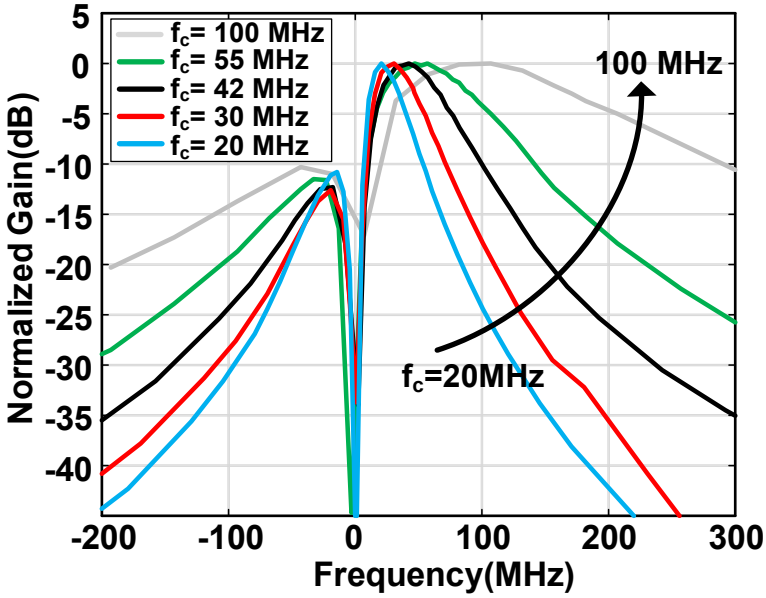

Figure 4.18: Measured transfer function for different IF frequencies. Center frequency f_c aligns with f_{IF}.

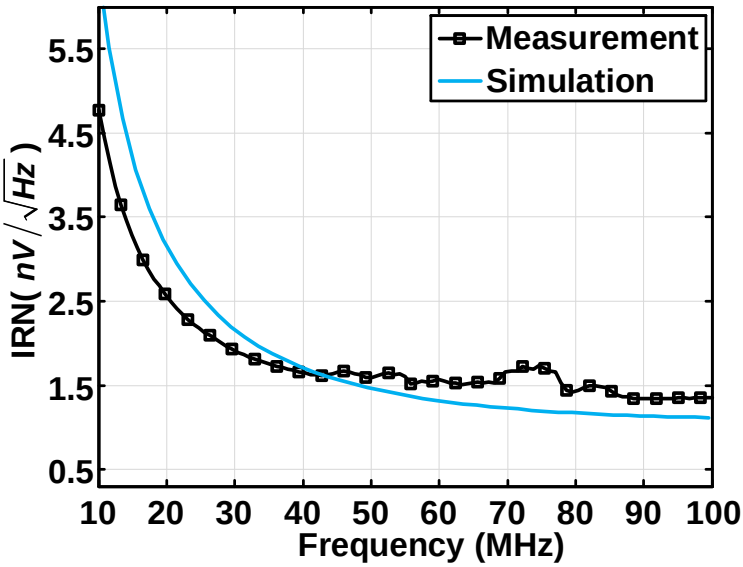

Figure 4.19: Measured and simulated IRN for $C_H = 10\,\text{pF}$ and $C_R = 1\,\text{pF}$.

Shown in Fig. 4.20, the out-of-band IIP3 of the RF frond-end ("g_{mRF}+1$^{\text{st}}$ CS-BPF") is measured by applying two-tone at the input of the chip. The out-of-band

Table 4.1: Summary and comparison with state-of-the-art.

	This work	[8]	[13]	[14]
CMOS Tech. [nm]	65	65	65	65
Type	filter	receiver	filter	filter
Vdd [Volts]	1.2	1.2/2.5	1.2	1.2
Power [mW]	28	39	2-20	18-57
IRN $[nV/\sqrt{Hz}]$	1.5	0.87	0.9-1.3	0.87
IB-IIP3 [dBm]	0	N.A	N.A	-12
OB-IIP3 [dBm]	+9.5	N.A	+14	+26
BW [MH]	24—125	4	35	8
Filter order	6	6	2	6
IF Freq. [MHz]	20—100	62	—-	—-
Freq. Range [GHz]	0.5—1.2	1.8-2.2	0.1-1	0.1-1.2
Active Area $[mm^2]$	0.19	0.76	0.07	0.27

two-tone frequencies are at 1100.009 MHz, 1200 MHz to have enough filtering at the output of RF frond-end for reducing the linearity contribution of the rest of the RX

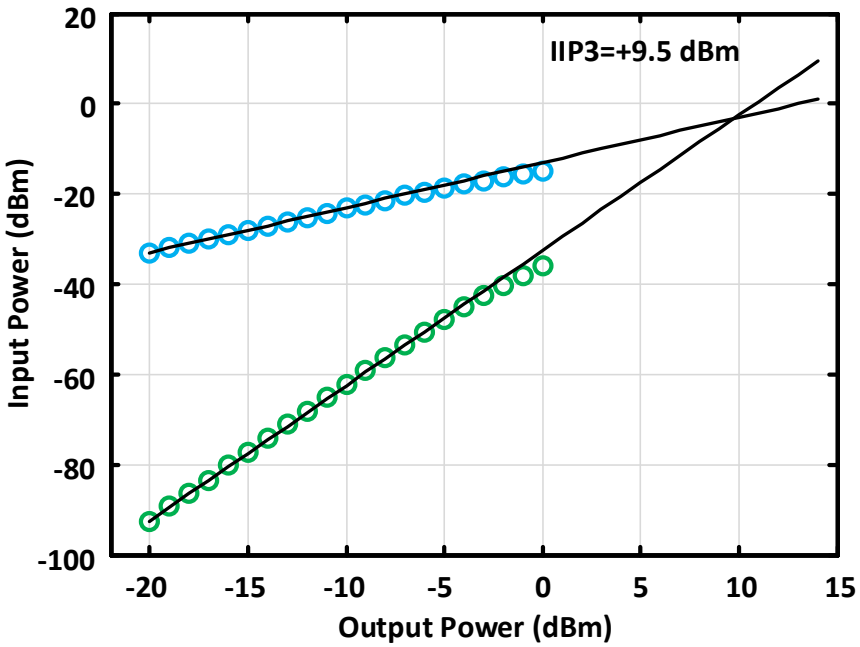

Figure 4.20: The measured out-of-band IIP3 of the RF front-end ($g_{mRF} + 1^{st}CS - BPF$).

chain. The measured IIP3 is +9.5 dBm and we believe the measured IIP3 is chiefly limited by the linearity of the g_{mRF}-cell because the simulated IIP3 of the CS-BPF itself is more than +30 dBm. Table 4.1 shows summary of the filter and compares it to state-of-the-art. Compared to other designs except [13], the power consumption of our test chip is less but, the filter order of our test chip is two order higher than [13]. Compared to [14], the power consumption of our test chip is almost half for the highest sampling frequency. Also, CS-BPF provides higher reconfigurability, and wider BW selectivity of 24—125 MHz. Also, It has a digitally controllable IF center frequency range of 20—100 MHz larger than $1/f$ corner frequency, unlike other filters [13, 14]. Although, input g_m-cell has degraded linearity of the test chip, the in-band and out-of-band IIP3 of 0 dbm and +10 dBm is achieved, respectively.

4.7 Conclusion

Process-scalable fully integrated band-pass filters (BPF), free from replicas to be suitable for high-IF or superheterodyne receivers (RX) are in high demand to solve the issues related to continuous-time (CT) and N-path filters. We propose and analyze a discrete-time (DT) charge-sharing (CS) BPF that is entirely passive and uses transistors only as switches. The center frequency of the proposed BPF filter is digitally controllable via clock frequency and capacitor ratios and thus insensitive to PVT variations. It is free from aliasing and replicas while operating at a GSample/s rate. The proposed filter performance is verified in 65 nm CMOS for the wide RF frequency range of 0.5—1.2 GHz and a digitally controllable center frequency of 20—100 MHz. Measured noise performance and transfer function of the filter accurately fit both the mathematical theory and the CT schematic model. The experimental results indicate the proposed filter to be a prime candidate for future superheterodyne receivers.

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CHAPTER

5

Feedback-based Superheterodyne Receiver

In this chapter, we propose a highly reconfigurable superheterodyne receiver that employs a 3rd-order complex IQ charge-sharing band-pass filter (BPF) for image rejection and 1st-order feedback based RF-BPF for channel selection filtering. The operating RF input frequency of the receiver is 500 MHz–1.2 GHz with varying high-IF range of 33–80 MHz. All the gain stages are merely inverter-based g_m-stages. The total gain of the receiver is 35 dB and in-band IIP3 at mid-gain is +10 dBm. The NF of the receiver is 6.7 dB, which is acceptable for the receiver without an LNA. The architecture is highly reconfigurable and follows the technology scaling. The RX occupies 0.47 mm^2 of active area and consumes 24.5 mA at 1.2 V power supply.

This chapter is based on a paper presented at IEEE RFIC in 2013 [1].

5.1 Introduction

Integrated RF receivers (RX) are typically zero-IF or low-IF (i.e., homodyne) because of the well-known benefits, such as: high-level of integration, the use of low-pass filtering for channel selection, and avoidance of an external IF band-pass filter (BPF). Weak desired signals are likely accompanied by large blocking interferers. These blockers can dramatically degrade the receiver performance by causing gain compression and higher-order nonlinearities as well as increasing its noise figure

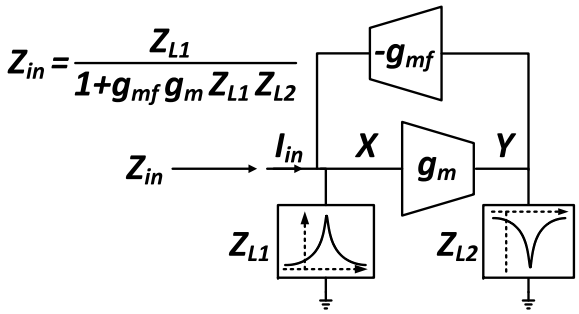

Figure 5.1: The basic concept of impedance combinations.

(NF). Conventionally, these out-of-band blockers are filtered out by a bulky and expensive SAW filter placed prior to the LNA input. Since the RF wanted signal could be weak and the dynamic range requirements of a given specification need to be met, the gain of the LNA should be kept high and the blockers should be filtered out. Otherwise, the mixer and the following stages could get saturated. SAW-less receivers have been recently discussed in [2, 3]. They are all based on a homodyne architecture. Unfortunately, they all exhibit well-known homodyne RX issues, such as sensitivity to 1/f noise and varying dc offsets, finite IIP2, which will keep on getting worse with the inevitable scaling of the process techonology.

In this chapter, we propose a superheterodyne receiver of high-IF that solves the aforementioned issues of the homodyne receivers. Another integrated superheterodyne RX was proposed in [4]. It filters the blockers through an N-path filter, as opposed to the DT filtering approach here. However, the image folding issue is not addressed there. The image folding issues of prior attempts are solved here through a discrete-time (DT) charge-sharing filtering. On the other hand, the blockers are filtered through a feedback-based high-Q RF BPF. The new architecture is process scalable and highly reconfigurable.

The N-path filters offer high-Q BFP filtering with precise control of the center frequency through clock adjustment [4]. Despite a very high-Q filtering, N-path filters provide only around 7–16 dB of filtering rejection due to the poor switch on-resistance in mixers. On the other hand, this type of filter suffers from folding of images from $(N-1)f_{IF}$ and $(N+1)f_{IF}$ with a normalized gains proportional to $1/(N+1)$ and $1/(N-1)$ [4]. For example, the images of the 16-path filter fold onto the wanted signal via the 24 dB attenuation, which does not appear sufficient. Therefore, it is essential to use pre-filtering (i.e., pre-select, SAW, N-path) to get rid of the images, which degrade NF and causes image folding. Usually, the gain of LNAs is around 10–20 dB, which can saturate the output of an LNA at a presence of a blocker that can be as large as 0 dBm ($600\,\mathrm{mV_{p-p}}$). Therefore, in order to prevent the saturation, it is needed to use the BPF right after LNA to attenuate the blockers.

5.2 High-Q RF BPF Structure

The novel idea of the high-Q RF BPF comes from a combination of two types of impedances. As shown in Fig. 5.1, the input current is converted to voltage at node X through multiplication by Z_{L1}. Then, it is converted to current and sinked on Z_{L2}. The resulting V_Y voltage gets fed back to input node V_X by a transconductance in the feedback path. As shown in Fig. 5.1, the input impedance of the circuit is $Z_{L1}/(1 + g_{mf}g_mZ_{L1}Z_{L2})$. When the gain $g_{mf}g_mZ_{L1}Z_{L2}$ is smaller than unity, the input impedance is equal to Z_{L1}, which in this design happens at frequencies far from the wanted signal. On the other hand, the input impedance becomes $1/(g_{mf}g_mZ_{L2})$ in the case that $g_{mf}g_mZ_{L1}Z_{L2}$ is much larger than unity, which happens at frequencies very close to the wanted signal. The first impedance Z_{L1} is a 3rd-order complex IQ charge-sharing filter, which acts here as a wide-bandwidth BPF centered at $+f_{IF}$ to filter out images of the wanted signal. The basic concept of IQ charge sharing filter was introduced in [5] for low-IF with low sampling rate.

The second impedance Z_{L2} is a complex 8-path notch filter (recently introduced in [6] for a real-valued version) to achieve a very sharp high-Q BPF at RF through feedback path. Fig. 5.2 depicts a detailed construction of a low-impedance node after the RF mixer for blockers with an extra filtering at image frequencies. Input matching of the circuit is provided by the input 50 Ω resistance. First, the RF input signal is converted to a current using a simple inverter-based g_m stage followed by a 25 % passive mixer clocked at f_{LO}. The complex output current of the mixer needs a complex low-impedance node for blockers to eliminate the saturation of the g_m output. As shown in Fig. 5.3, the blockers are attenuated because of the complex high-Q BPF, while the complex full-rate wideband IQ charge-sharing BPF (including the feedback) rejects other image components, including those at -f_{IF}. The filtered complex signals go through two similar wideband IQ filters for more attenuation of the images and amplification of the wanted signal. Output signals of the last (third) IQ filter go through a complex notch filter centered at $+f_{IF}$ followed by TIA in order to feed back the complex signals to the mixer output. The complex notch filter rejects the wanted signal and passes all blockers and unwanted signals, which get fed back through a transconductance (g_{mf}) and will be canceled at the mixer output.

Fig. 5.4 shows the concept of IQ charge-sharing wideband BPF. The input current is integrated into the total capacitor $C_t = C_H + C_r$ during four phases of the non-overlapping 25% full-rate LO clock. The full-rate operation means that it works at the maximum sampling frequency of $4f_{LO}$ to avoid decimation. The main drawback of an early decimation would be an unwanted folding due to the change of the sampling rate between stages. Therefore, in order to avoid aliasing, it is crucial to keep the sampling frequency at full rate. After each integration of the current into C_t of each quadrature path, a small portion of the total charge $\frac{C_r}{C_t}q_{in}$ is shared between the real and imaginary paths in the next clock cycle. This operation forms

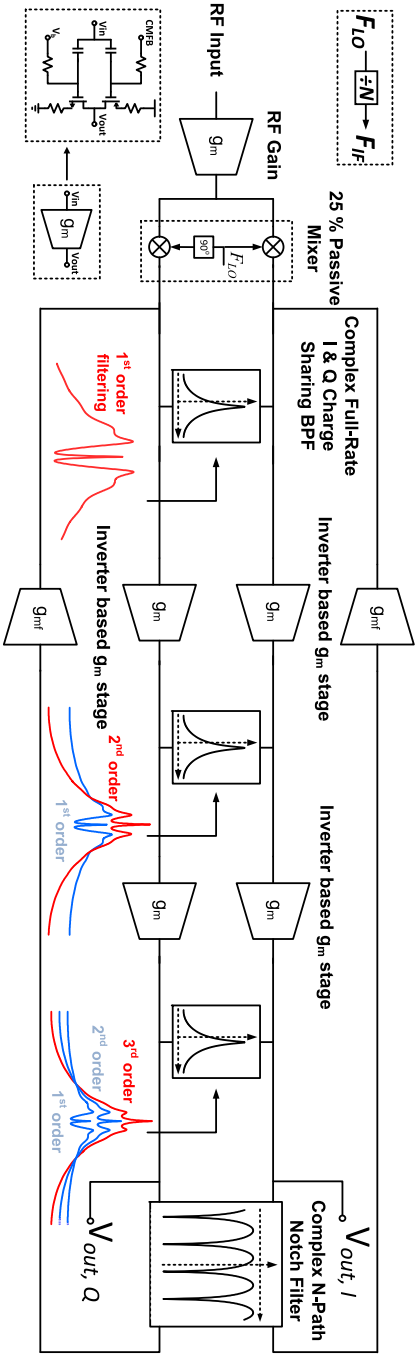

Figure 5.2: Detailed block diagram and operation of the high-IF receiver with high-Q BPF.

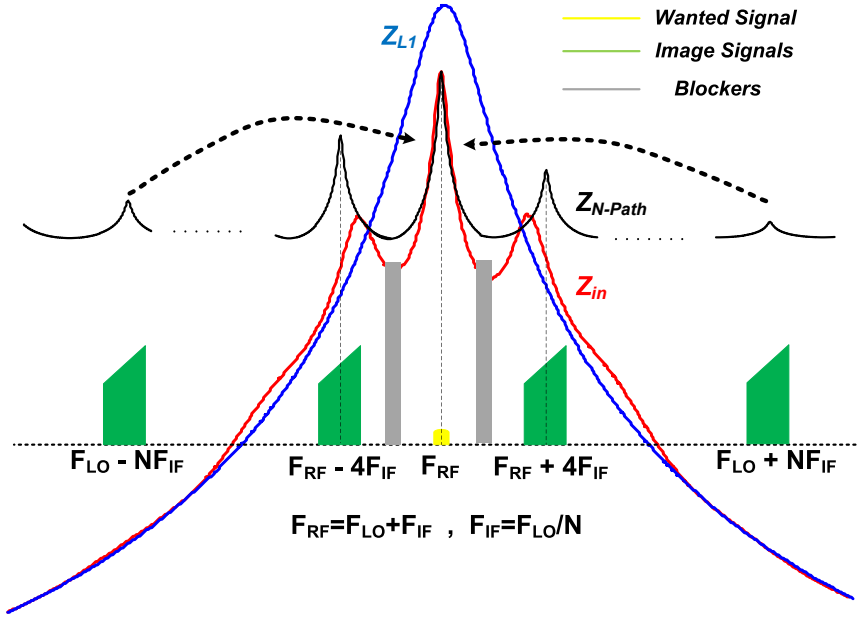

Figure 5.3: Frequency translation of the high-IF receiver compared to a typical N-path filter.

a complex filter with a transfer function given by

$$H(z) = \frac{Vout(z)}{Qin(z)} = \frac{k}{1-(a+jb)z^{-1}}, \tag{5.1}$$

where $k = 1/(C_H + C_r)$, $a = C_H/(C_H + C_r)$ and $b = C_r/(C_H + C_r)$. According to Eq. 6.1, the charge-sharing process forms a 1st-order complex filter centered at

$$f_c = \frac{f_s}{2\pi} arctan \frac{b}{a}. \tag{5.2}$$

Therefore, it is possible to adjust the center frequency f_c by changing the coefficients a and b. However, it is not possible to make the filter very sharp because the DT charge sharing is a lossy operation, which increases bandwidth of the filter. f_c is a bit sensitive to the capacitance ratio mismatch, as compared with the N-path filter, in which the center frequency is exactly equal to the operating clock frequency. The main advantage of this structure is that the IQ charge-sharing BPF has a very robust filtering at frequencies located at $f_s/2$. As a result, it is feasible to use it as the wideband BPF centered at f_{IF} to reject image signals located at harmonics of f_{IF}. The other benefit of this filter is that its sampling frequency is equal to $f_s = 4f_{LO}$. Therefore, no unwanted folding occurs as compared to the N-path filter,

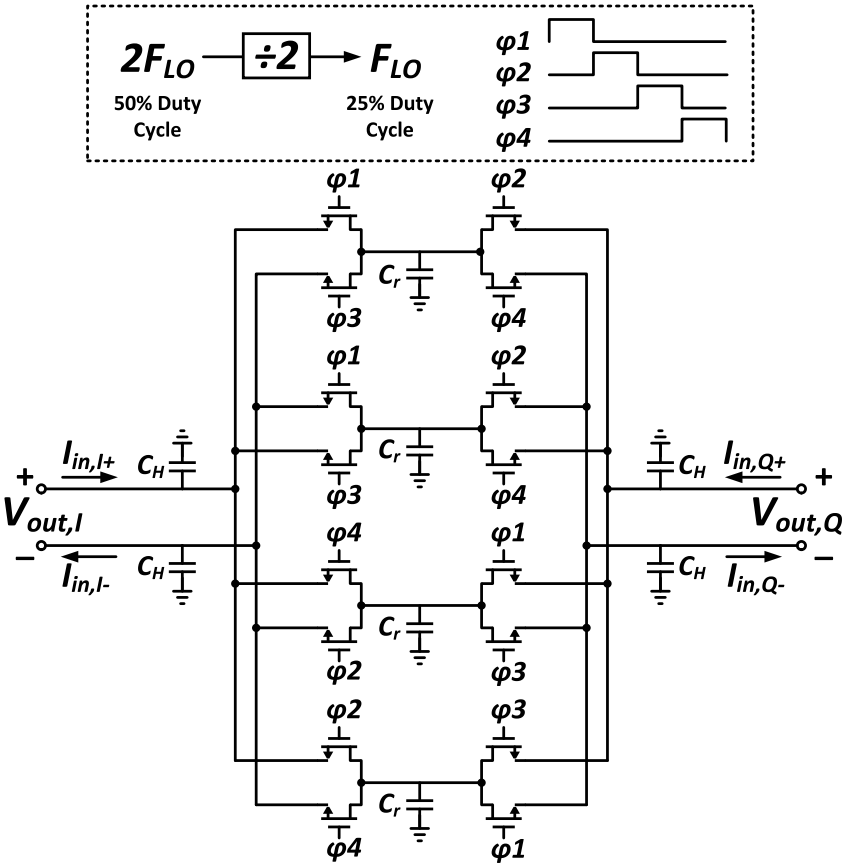

Figure 5.4: Circuit level schematic of the wideband IQ charge-sharing BPF.

which suffers from harmonics folding.

The proposed architecture offers several advantages over the state-of-the-art receivers. The high-IF RX eliminates the homodyne RX issues, such as LO feedthorough, dc offset, 1/f noise and 2$^{\text{nd}}$-order nonlinearity, which force all the active devices to be very large. Here, all the gain blocks are simple inverter-based g_m stages. All switches and capacitors, which are used in the filters, are amenable to the technology scaling. The proposed high-Q BPF has a superior image rejection as compared to the N-path filter. In mixer-based BPFs, such as the N-path filter, the rejection of the image components is ultimately limited by the mismatch between the LO clock of I and Q paths. On the other hand, there is no inherent limitation here on the level of image component rejection other than the NF degradation and power consumption of LO distribution.

The circuit of the on-chip complex notch filter is depicted in Fig. 5.5. The wanted signal at f_{IF} is downconverted by the mixers and filtered through the C-R filter,

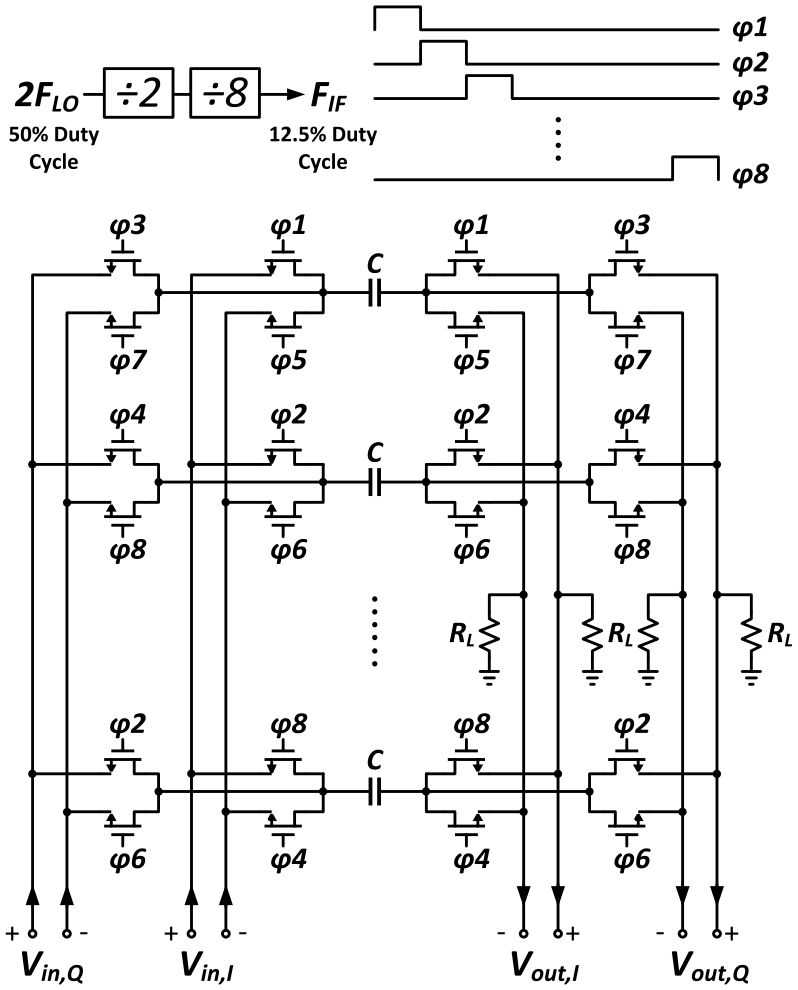

Figure 5.5: Circuit level of the complex notch filter centered at f_{IF}.

which acts as a HPF at dc. Then, the signal is upconverted to the IF frequency with the second mixer. Similarly to the N-path filter, harmonic mixing might also happen in the N-path notch filter. However, it is not an issue in this RX since the image components are already filtered out via the preceding complex wideband IQ charge-sharing filter. The 8-phase clock for the notch filter is provided by dividing the main LO by 2 and then further dividing it by 8, through the chain of ÷2 dividers, The ÷2 divider ensures that the 8-phase output clocks are non-overlapped.

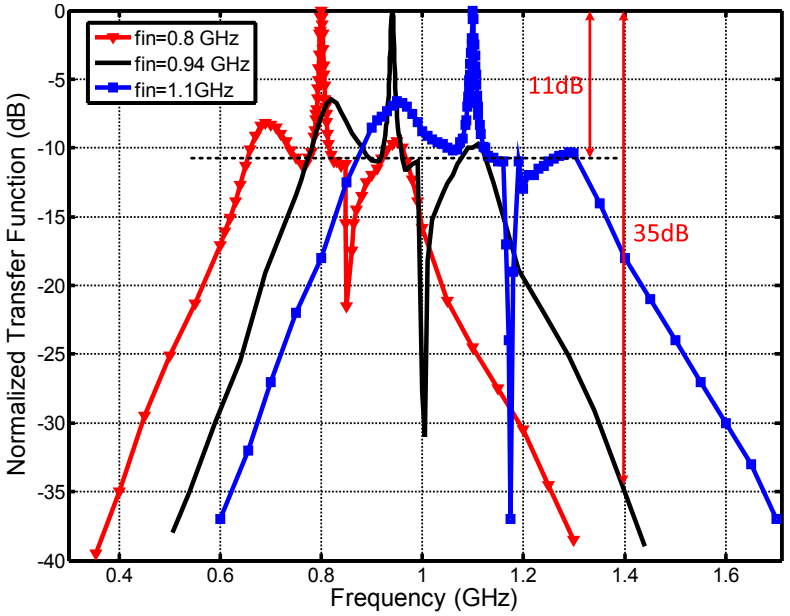

Figure 5.6: Measured transfer function of the receiver.

5.3 Measurement Results

The receiver (RX) chip is fabricated in 65 nm CMOS technology. The input signal lies in the range of 500 MHz to 1.2 GHz, corresponding to the IF frequency of 33.33 MHz to 80 MHz. The C_H and C_r capacitors are binary adjustable between 3.8–11 pF and 1.2–2 pF, respectively. The notch filter capacitance (C in Fig. 5.5) is 5 pF . The measured RX gain is 35 dB and the NF is 6.7 dB at the max gain. The in-band IIP3 is +10 dBm at the 25 dB gain with a two-tone test at +5 MHz and +10 MHz; it is 0 dBm at +1 MHz and +2 MHz. The measured RX transfer function at various LO frequencies is demonstrated in Fig. 5.6. The notch in the transfer function is due to the dc block capacitors in the feedforward path of the g_m stages shown earlier in Fig. 5.2. This further improves IM2 and clock feedthrough. The BW of the RX is 4.5 MHz. It can be seen that the rejection around the RF frequency is more than 10 dB. The images at $7f_{IF}$ and $9f_{IF}$ could theoretically be folded into the wanted signal in the complex notch filter. However, this is not an issue because these images are already rejected through 35 dB attenuation in the IQ charge-sharing BPF. Note that no pre-select filters are used here. Therefore, any possible folded images from $7f_{IF}$ and $9f_{IF}$ are first attenuated by 53 dB (35 dB+18 dB). On the other hand, it should be possible to employ the high-Q N-path filter in the feedforward path to improve the filtering function after the IQ charge-sharing BPFs. The two "shoulders" around f_{RF} in Fig. 5.6 are due to the transition from the filtering function of the

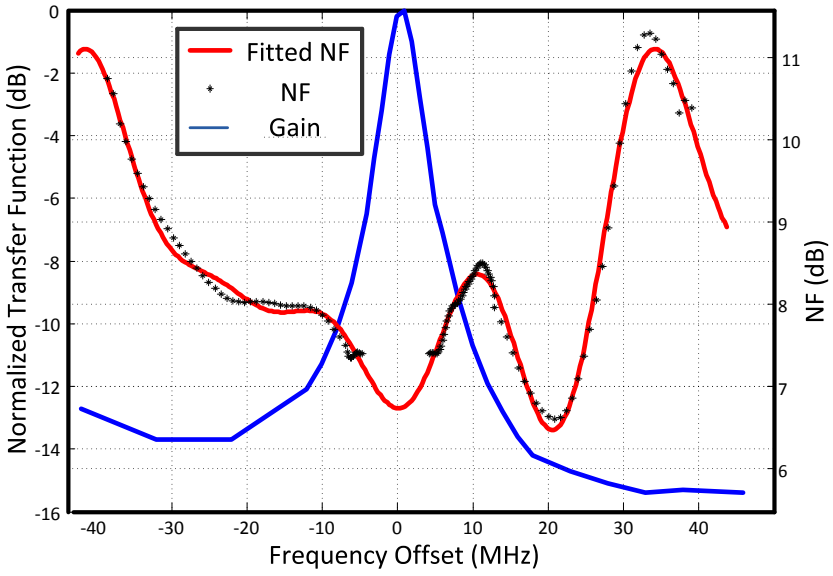

Figure 5.7: Measured transfer function and NF around desired RF frequency versus frequency offset.

Table 5.1: Summary and comparison with state-of-the-art

	This work	[4]
CMOS Technology	65 nm	65 nm
Active Area	0.45 mm^2	0.76 mm^2
Power Consumption	24.5 mA	21 mA
Rejection @ f_{LO}-7f_{IF} f_{LO}+9f_{IF}	<-53 dB	<-18 dB
NF (dB)	7.5	2.8
IIP3 (dBm) @ 1M,2M	0	—-
IIP3 (dBm) @ 5M,10M	+10	—-
IIP3 (dBm) @ 10M,20M	+2	—-
BW (MHz)	4.5	4
RX Frequency (GHz)	0.5-1.2	1.8-2.2

sharp high-Q RF BPF to the IQ charge-sharing BPF. The measured close-in transfer function and NF are depicted in Fig. 5.7.

The Q-factor of the BPF is 208 and the total power consumption of the RX is 24.5 mA. The performance of the RX is summarized and compared in Table 5.1 with the only other published high-IF RX [4]. A clock generation circuit consumes 6 mA at 1.2 V. The active area of RX including the clock generation is 0.45 mm^2, as shown in Fig. 5.8. The presented high-IF RX with high-Q complex BPF offers

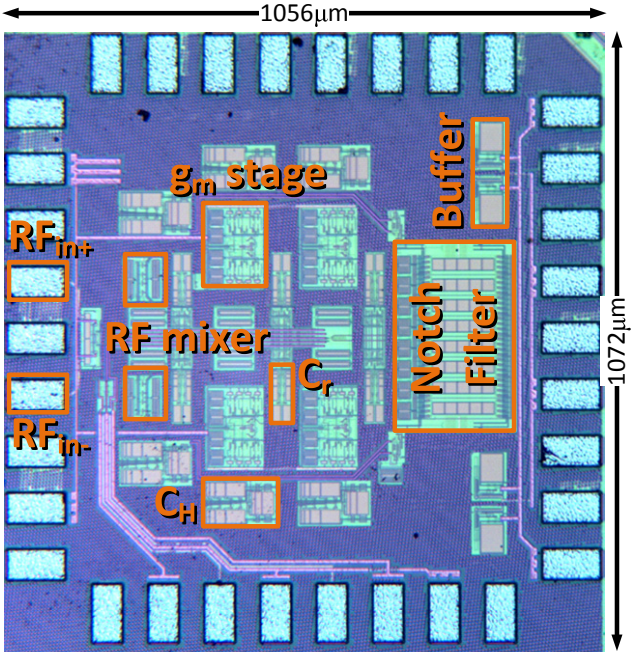

Figure 5.8: Chip micrograph.

superior filtering at RF frequencies in addition to the strong filtering of the image components, while achieving low power consumption in a very small chip area. It should be emphasized that the LNA was not implemented in this chip in order to better characterize the linearity and noise. Hence, the NF given in Table 5.1 is high, just as expected, due to the low gain of the RX front-end (i.e., g_m & mixer) stage, which is about 6 dB.

5.4 Conclusion

The first-ever superheterodyne receiver that rejects image folding is proposed and demonstrated. The concept of impedance combination is utilized to realize the complex high-Q RF BPF that rejects the image folding that has prevented the widespread adoption of high-IF RX architectures in the past. The RX occupies 0.45 mm^2 and consumes 24.5 mA at 1.2 V.

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CHAPTER

6

SAW-less Discrete-Time Superheterodyne Receiver

In this chapter, the first fully integrated SAW-less superheterodyne receiver (RX) for 4G cellular applications is demonstrated. The RX operates in discrete-time domain and introduces various innovations in order to simultaneously improve noise and linearity performance while reducing power consumption: a highly linear wideband noise-canceling LNTA, a blocker-resilient octal charge-sharing band-pass filter, and a cascaded harmonic rejection circuitry. The RX is implemented in 28 nm CMOS with no calibration required. It features NF of 2.1–2.6 dB, an infinite IIP2, and IIP3 of 8–14 dBm, while drawing only 22–40 mW in various operating modes.

This chapter is based on two papers, one published in IEEE VLSI Symposium in 2015 [1], the other one submitted for publication in IEEE Journal of Solid-State Circuits [2].

6.1 Introduction

Conventional multi-band, multi-standard cellular receivers (RXs) require many external duplexers, surface acoustic wave (SAW) filters and switches, typically one per band, to attenuate out-of-band (OB) blockers before they reach the sensitive

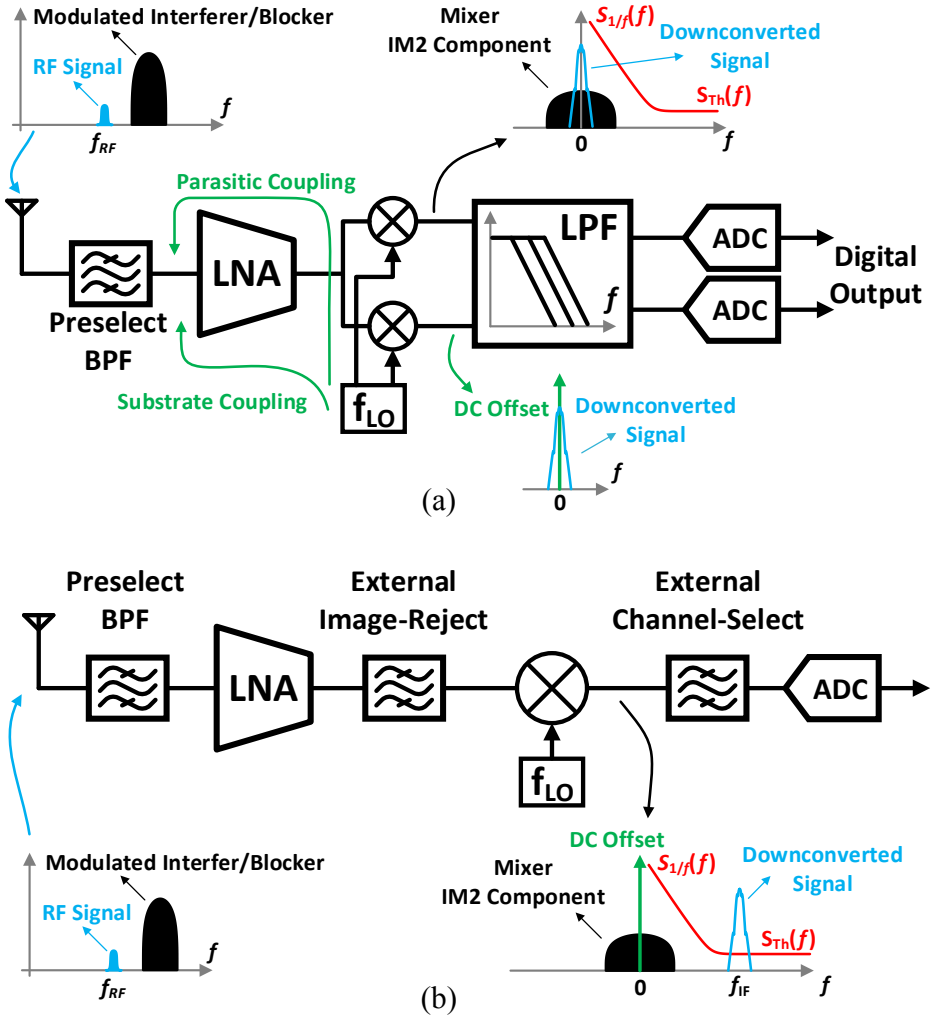


Figure 6.1: Comparison of conventional receiver architectures: (a) zero-IF/low-IF; and (b) superheterodyne.

low-noise amplifier (LNA) input. In time-division duplexing (TDD) systems, external SAW filters can be eliminated if the RX chain can handle large interferers (e.g., 0 dBm at 20 MHz away from a GSM channel of interest [3]). On the other hand, for frequency-division duplexing (FDD) systems, the external SAW filters are responsible for not only the filtering of out-of-band blockers but also for duplexing, i.e., separation of concurrent transmit (TX) and RX operations. To reduce cost and size of the total system solution, in which the external antenna interface network is nowadays the largest contributor, the recent trend is to eliminate SAW filters and switches by using

a highly linear wideband RX [4–9]. As a consequence, the isolation of TX-to-RX, and the suppression of TX interferers are worsening, which all further increase RX linearity requirements in FDD systems.

The resulting reductions in out-of-band filtering implies tough IIP2 requirements (e.g., 90 dBm [9, 10]) for zero-IF (ZIF) and low-IF (LIF) receivers. The IIP2 performance of such receivers depends mainly on the second-order nonlinearity of LNA and RF mixer in the receiver chain, as shown in Fig. 6.1(a). Since the typical IIP2 of RF mixer is between 50–70 dB [11], ZIF/LIF receivers require highly sophisticated calibration algorithms [9, 12–17] to be frequently executed to account for variations in power supply [6, 18–22], process corner [22], temperature [23], mixer transistor's gate bias [18], RF blocker frequency [16, 19, 21, 22], LO frequency [19, 21, 22], LO power [22] and channel frequency [23]. Also, the IIP2 calibration time is rather very slow and it needs to be run repeatedly due to environmental and operational changes [18].

Superheterodyne or high-IF (HIF) architectures, on the other hand, can have a theoretically infinite IIP2. As shown in Fig. 6.1(b), the desired signal and modulated blocker at the RF input will be down-converted to a considerably higher IF and DC, respectively; thus the modulated blocker can be completely filtered out by a band-pass filter (BPF) [24, 25]. For this reason, there is an increasing interest in uncalibrated high-IIP2 SAW-less superheterodyne receivers with integrated blocker-tolerant BPFs that are amenable to technology scaling.

The outline of the chapter is as follows. An overview of wireless receivers is presented in Section 6.2. In Section 6.3, the general ideal of the proposed RX with M/N-phase discrete-time (DT) operation is discussed. Section 6.4 provides detailed analysis of the M/N-phase DT CS-BPF. Section 6.5 gives a description of a cascaded three-stage harmonic rejection (HR) circuitry. Design and implementation of the receiver chain are described in Section 6.6, with measurement results given in Section 6.7. Finally, conclusions are drawn in Section 6.8.

6.2 Overview of State-of-The-Art Wireless Receivers

The pioneers of RFIC integration [26] have quickly realized the superiority of operating receivers at ZIF/LIF rather than at HIF: simpler architecture, and a much higher level of monolithic integration as a result of using low-frequency low-pass filters (LPF) for channel selection [see Fig.6.1(a)]. This was despite the many issues associated with ZIF/LIF receivers: time-variant DC offsets, sensitivity to 1/f (flicker) noise, large in-band LO leakage and the second-order nonlinearity [4–9]. Those issues were viewed rather as an inconvenience and handled through various calibrations. However, high-performance cellular ZIF/LIF receivers now require extensive calibration efforts. For example: an intensive IIP2 calibration needs to be concurrently run in the background with DC offset and HR calibration [10, 20].

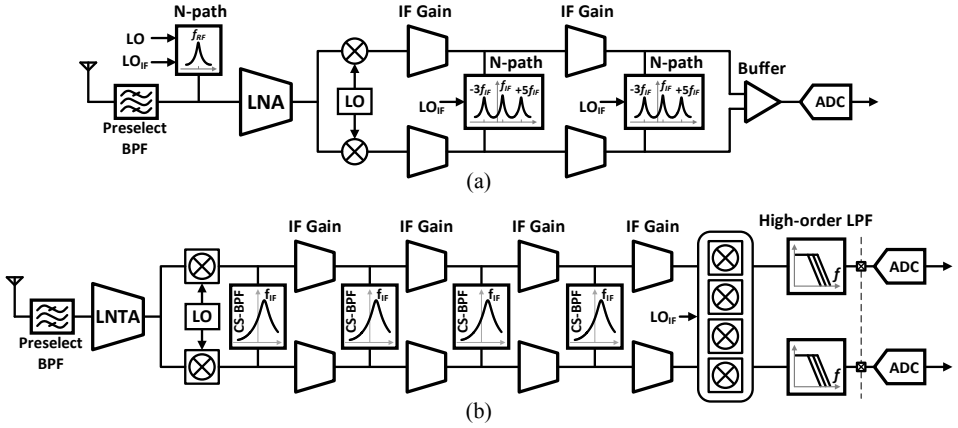


Figure 6.2: State-of-the-art superheterodyne receivers.

A superheterodyne architecture, shown in Fig. 6.1(b), pushes the IF frequency much higher such that the aforementioned problems are not a major concern anymore. Despite the obvious advantages, the superheterodyne radios have been abandoned for decades because it was extremely difficult to integrate a high quality (Q)-factor BPF for image rejection in CMOS using continuous-time (CT) circuitry [26].

The integration problem of high-IF BPF was addressed in [27] [see Fig. 6.2(a)] utilizing an N-path filtering technique [28–33]; and in [34, 35] [see Fig. 6.2(b)], [36] using a discrete-time (DT) quadrature charge-sharing (CS) BPF [37, 38]. The N-path filter cannot reject images defined as blockers/interferers at harmonics of the IF frequency because it *inherently* features replicas there [27]. On the contrary, a transfer function of the DT CS-BPF has only one peak in the entire sampling frequency domain of $-f_s/2$ to $f_s/2$, which makes it a proper candidate as an integrated BPF for superheterodyne receivers [37]. The center frequency and bandwidth of the full-rate DT CS-BPF in [34, 36] are precisely controlled via f_s and capacitor ratios. Additionally, that filter comprises only transistors as switches and capacitors, which occupy a small area and follow the process scaling very well. Unfortunately, CS-BPF in [34, 36] has insufficient blocker rejection to support the SAW-less operation.

In this work, we propose the superheterodyne architecture shown in Fig. 6.3 that utilizes a novel charge-sharing BPF based on an M/N-phase signaling and an extra pole to improve filtering. Combined with a proposed highly linear wideband LNTA and cascaded harmonic rejection (HR) stages, the first-ever SAW-less high-IF (superheterodyne) RX is thus demonstrated. By exploiting two stages of the M/N-phase CS-BPF, the desired signal is amplified while the images and in-band/out-of-band blockers are progressively filtered-out thoroughout the receiver chain.

As stated above, the proposed architecture has several key advantages compared

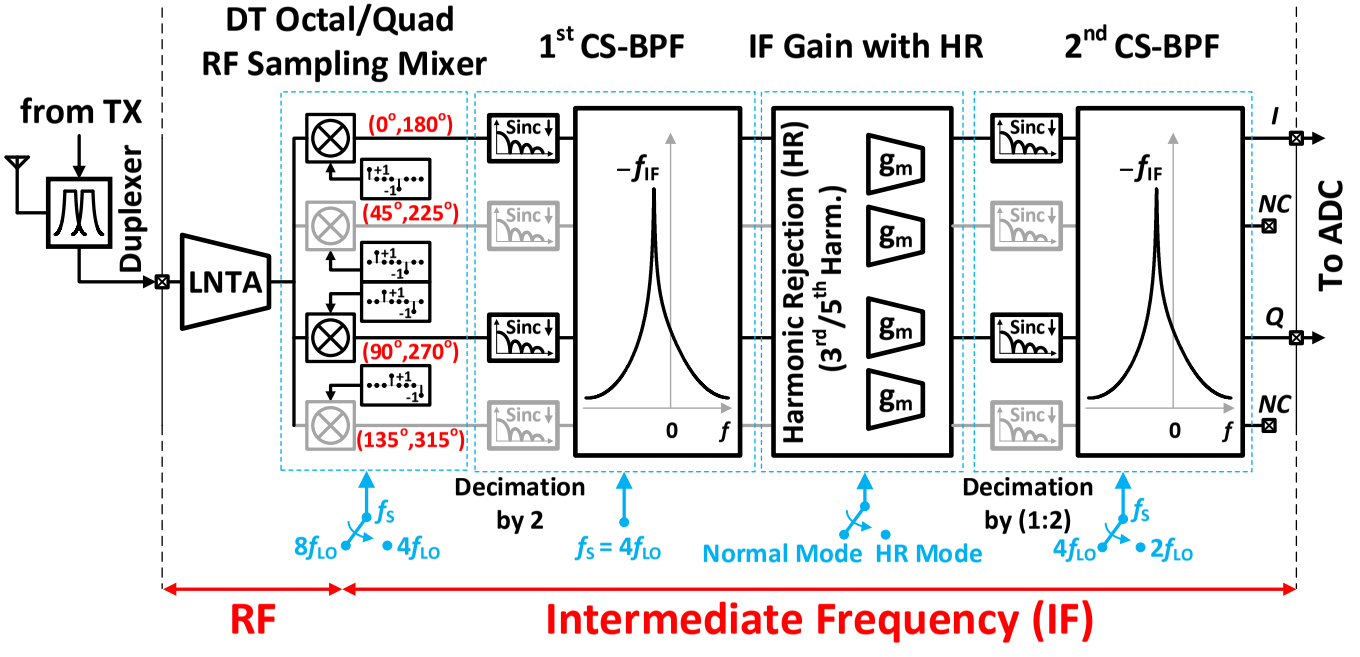


Figure 6.3: Proposed superheterodyne receiver architecture including two stages of CS-BPF filtering and three stages of harmonic rejection.

to state-of-the-art LIF RXs. First, since its IF is high, the issues associated with LIF RXs are eliminated, specially IIP2 and the need for DC offset calibration. Also, 1/f noise is not a concern anymore, so the active IF amplifiers use minimum length transistors. Second, two stages of DT CS-BPF consist of only capacitors as information charge storage devices, and transistors as switches. All of this makes the structure *fully* compatible with the technology scaling. Moreover, the proposed RX offers the same level of monolithic integration as LIF RXs *without* using any calibration. Furthermore, the proposed RX exhibits clear advantages over the traditional superheterodyne RXs, which are summarized below. First, it includes two stages of integrated blocker-tolerant complex image-reject CS-BPFs and three stages of harmonic rejection circuitry. Second, since the center frequency (i.e., coinciding with the chosen IF) of the M/N-phase DT CS-BPF is well controlled by clock frequency and ratio of capacitors, the IF frequency could be changed, thus avoiding RX desensitization in face of extremely large blockers. Finally, the second mixer and baseband filters have moved to the digital domain after the ADC (external in this work), hence they are ideal.

6.3 Proposed SAW-Less Super-Heterodyne Receiver

Digital circuits benefit from process scaling in both speed and energy due to, respectively, the increase in transistor transit frequency, f_T, and lowering of its dimensions with every finer process technology node. However, analog/RF circuitry is getting worse, except for LNAs[1], because the threshold voltage, V_{th}, remains almost constant while the supply voltage, V_{DD}, decreases. Also, the intrinsic gain and signal swing are reduced. All of those make analog/RF circuitry not amenable to CMOS scaling [39–43].

One the other hand, the DT approach is fundamentally based on building blocks that scale very well: transistors acting as switches, switched capacitors, inverter-based g_m-cells and digital clock generation circuitry. Hence, the RF performance improves with newer CMOS technology [44] [34]. These reasons motivate us to exploit the DT approach in the proposed SAW-less superheterodyne RX shown in Fig. 6.3.

The input voltage at the antenna is converted to current by LNTA and down-converted to high-IF by DT sampling RF mixer, as shown in Fig. 6.3. The octal (i.e., 8-phase) mixer can be reconfigured to operate in the quadrature (i.e., 4-phase) mode if the detected reception conditions are not demanding. After the mixer, the sampled down-converted signal is fed to the DT CS-BPF to attenuate images and out-of-band blockers. To reduce the power consumption of the 1$^{\text{st}}$ CS-BPF even further, the decimation by 2 can be performed by integrating two samples, thus giving rise to the anti-aliasing *sinc*-type transfer function. In addition to all advantages of the two-stage CS-BPF, each of them provides intrinsic 3$^{\text{rd}}$/5$^{\text{th}}$ harmonic rejection that can be further improved by turning on the additional HR block. The 2$^{\text{nd}}$ CS-BPF is

[1] LNA noise figure improves when f_T increases.

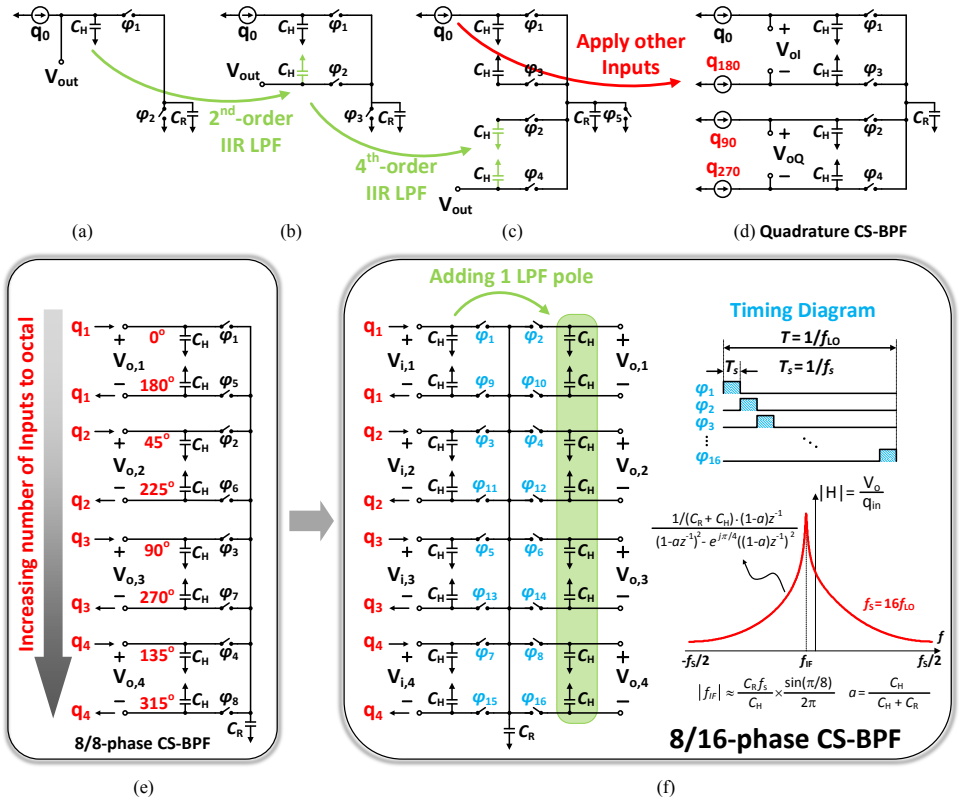


Figure 6.4: Evolution towards (f) M/N-phase CS-BPF ($M = 8, N = 16$), starting from (a) the simplest 1st order IIR LPF, then through (b) 2^{nd} order IIR LPF, through (c) 4^{th} order IIR LPF, through (d) conventional CS-BPF, and finally through (e) 8/8-phase CS-BPF.

cascaded via inverter-based gm-cells providing flicker-noise-free gain. The sufficient front-end filtering provided by the two-stage CS-BPF (unlike in [34]) allows to directly digitize the IF signal using a low-power ADC, and move the *second mixer* and baseband filtering into the digital domain. As calculated, a 10-bit 400 MS/s ADC should be sufficient after the two stages of CS-BPF filtering, while consuming less than 2 mW with state-of-the-art SAR ADC [45]. Also, it should be mentioned that the IIP2 generated by ADC is not a concern, because the ADC's IM2 component is at DC and the desired signal is at IF. The only possible limitation on the IIP2 in the proposed receiver is the quantization noise of the second digital mixer, but it can be arbitrarily reduced by increasing its word-length.

6.4 DT M/N-phase Charge-Sharing Band-Pass Filter (CS-BPF)

The DT CS-BPF exhibits clear advantages over the traditional types of filters, such as active-RC, N-path, g_m-C and biquad. The active-RC and g_m-C filters are substantially noisier due to the noise contributions from opamp and g_m components. Those components also generate flicker noise, so to suppress it, their area needs to be very large. Furthermore, typical IF and BB filters need to be reconfigurable, in which the required bandwidth scales over a decade. Since the bandwidth in active filters is determined by the RC or C/g_m time constant, the capacitors should be up to 50% larger to compensate for RC and g_m-C mismatches. This contributes to their area disadvantage. As far as the N-path filters are concerned, they suffer from replicas at harmonics of their mixer switching frequency, while CS-BPF has only one peak in the entire sampling frequency. Also, in the traditional N-path filter, the stop-band rejection is severely limited by the switch on-resistance.

Further in this section: The causes leading to creation and evolution of CS-BPF are detailed in Subsection 6.4.1 followed by a description of the proposed 8/8-phase and 8/16-phase CS-BPFs in Subsections 6.4.2 and 6.4.3, respectively. After detailed comparison of different kinds of M/N-phase CS-BPFs, the general z-domain transfer function of M/N-phase CS-BPF is derived.

6.4.1 Conventional Quadrature CS-BPF

Fig. 6.4(a) shows the well-known DT IIR LPF [46]. The input current i, generated by a g_m-cell, is integrated on the history, C_H, and rotating, C_R, capacitors as the input charge packet $q_0 = \int_{(n-1)T_s}^{nT_s} i \, \mathrm{d}t$ during φ_1 over a time window T_s. At φ_1 going inactive, C_R samples a portion of the total "history" charge. As a result, the DT circuit illustrated in Fig. 6.4(a) has a 1$^{\text{st}}$-order IIR characteristic, with C_R acting as a lossy component (termed "switched-capacitor resistor"). The order of the Fig. 6.4(a) DT IIR filter can be further increased to 2$^{\text{nd}}$ or 4$^{\text{th}}$, as shown in Fig. 6.4(b) and Fig. 6.4(c), respectively; or indefinitely beyond, as demonstrated in [47]. The conventional quadrature CS-BPF with a single real-valued output can be synthesized from the 4$^{\text{th}}$-order DT IIR filter by applying input charge packets q_0, q_{90}, q_{180} and q_{270} with a multiple of 90$^{\text{o}}$ degree phase shifts, as shown in Fig. 6.4(d) [37]. By defining the complex-valued input constructed from two differential signals having the quadrature relationship, $q_I = q_0 - q_{180}$ and $q_Q = q_{90} - q_{270}$, the complex transfer function of a conventional quadrature CS-BPF is derived as:

$$H(z) = \frac{V_{oI}(z) + jV_{oQ}(z)}{q_I(z) + jq_Q(z)} = \frac{k}{1 - (a + j \cdot (1-a))z^{-1}}, \tag{6.1}$$

where,

$$k = 1/(C_H + C_R), \tag{6.2}$$
$$a = C_H/(C_H + C_R). \tag{6.3}$$

This transfer function has a 1st-order complex BPF characteristic with it's peak located at:

$$f_{IF} = \frac{f_s}{2\pi} arctan(\frac{1-a}{a}). \tag{6.4}$$

The filter comprises only capacitors and switching transistors. Its center frequency f_{IF} only depends on the sampling frequency f_s and capacitor ratios. Hence, it is fully amenable to process scaling.

6.4.2 8/8-Phase CS-BPF

The filtering characteristic and tolerance to out-of-band blockers of the conventional quadrature CS-BPF can be *significantly* enhanced by increasing the number of inputs, corresponding history capacitors, and digital clock phases to 8 (i.e., octal) or more. As an example of such a filter, the schematic of a 8/8-phase CS-BPF is proposed in Fig. 6.4(e), where it features 8 inputs/outputs, 8 history capacitors and 8 digital clock phases. The inputs, which are generated by the DT mixer for the first filter, are differential integrated charge packets q_1, q_2, q_3, q_4 that are phase shifted by 0, 45°, 90°, 135°. As in the traditional CS-BPF, C_R shares the charge between various C_H's. By defining the complex output voltage as

$$V_{oC} = V_{o,1} + e^{j\pi/4}V_{o,2} + e^{j\pi/2}V_{o,3} + e^{j3\pi/4}V_{o,4}, \tag{6.5}$$

and complex input charge as

$$q_{iC} = q_1 + e^{j\pi/4}q_2 + e^{j\pi/2}q_3 + e^{j3\pi/4}q_4, \tag{6.6}$$

and following the same approach as presented in [37], we find the complex transfer function of the 8/8-phase CS-BPF, driven by ideal input charge packets, as

$$H_{8/8}(z) = \frac{V_{oC}(z)}{q_{iC}(z)} = \frac{k}{(1-az^{-1}) - e^{j\pi/4}(1-a)z^{-1}}, \tag{6.7}$$

where, k and a are the same as in (6.2), (6.3). The peak of the transfer function lies at

$$f_{IF} = \frac{f_s}{2\pi} arctan\left(\frac{(1-a)sin(\pi/4)}{a + (1-a)cos(\pi/4)}\right). \tag{6.8}$$

The 8/8-phase CS-BPF has a 1st-order BPF characteristic centered at f_{IF}. In addition to the filtering improvement over its conventional counterpart, this filter

is capable of filtering images and out-of-band blockers at $3^{rd}/5^{th}$ LO harmonics. It should be noted that this filter still maintains the *full* compatibility with the technology scaling due to its DT passive nature.

6.4.3 8/16-phase CS-BPF

To further improve the filtering order and characteristics of the 8/8-phase CS-BPF, we propose to add an IIR LPF (of single or multiple poles) during the charge-sharing process in-between every two adjacent inputs. As an example of such a filter, one LPF pole is added between each pair of adjacent input history capacitors, C_H, in Fig. 6.4(f) to give rise to an 8/16-phase CS-BPF. This filter has 8 inputs, 8 outputs, 16 C_H's (8 of them are input C_H's) and 16 non-overlapped clock phases with a duty-cycle of 1/16. The input is interpreted as four *differential* charge packets (q_1, q_2, q_3, and q_4) with multiples of 45° degree phase shifts provided by the DT mixer. The eight individual *single-ended* input charge packets are accumulated into their respective input C_H's . At the end of each odd-numbered phase $\varphi_1, \varphi_3, ...\varphi_{15}$, the rotating capacitor C_R samples a charge from the active C_H. In the following even-numbered phase of $\varphi_2, \varphi_4, ...\varphi_{16}$, C_R containing the previous packet is charge-shared with a newly introduced history capacitor, termed "output C_H", which contains the intermediate (i.e., additionally LPF filtered) version of the "history" charge. Therefore, in each phase, C_R removes a charge proportional to $C_R/(C_H + C_R)$ from each C_H (whether input or output) and then delivers it to the next C_H. The newly introduced output history capacitors add significant extra filtering thus improving blocker resiliency. They also provide convenient pick-up nodes for the dedicated output port that is now physically separate from the input.

6.4.4 Proposed General M/N-Phase CS-BPF

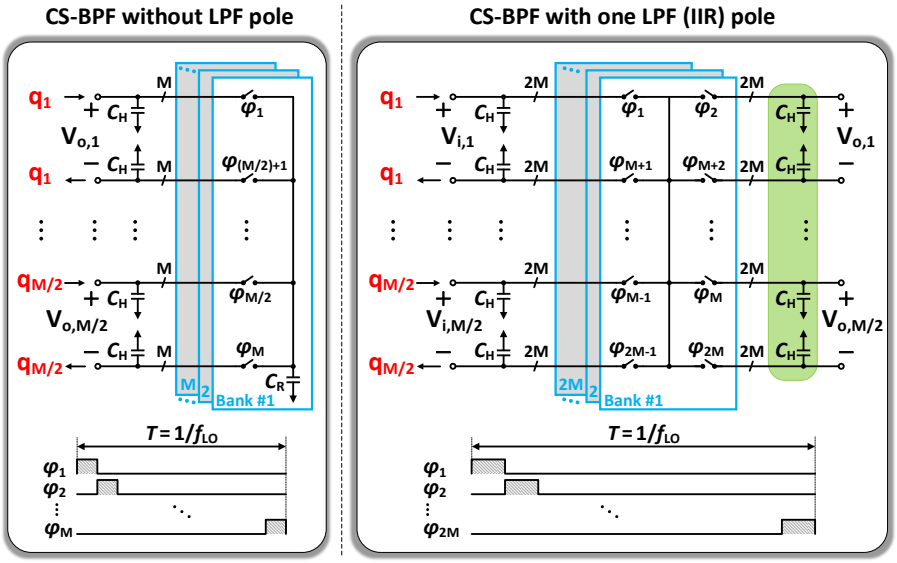
In the above case, the 8/16-phase CS-BPF does not operate at the full-rate and so all eight outputs can be read out at the maximum sampling rate of $f_s = 1/T_s = f_{LO}$. By defining the V_{oC} and q_{iC} the same as (6.5) and (6.6), the filtering transfer function of the filter driven by ideal charge packets, as shown in Fig. 6.4(f), can be proven to be

$$H_{8/16}(z) = \frac{V_{oC}(z)}{q_{iC}(z)} = \frac{k \cdot (1-a)z^{-1}}{(1-az^{-1})^2 - e^{j\pi/4}\left((1-a)z^{-1}\right)^2}, \tag{6.9}$$

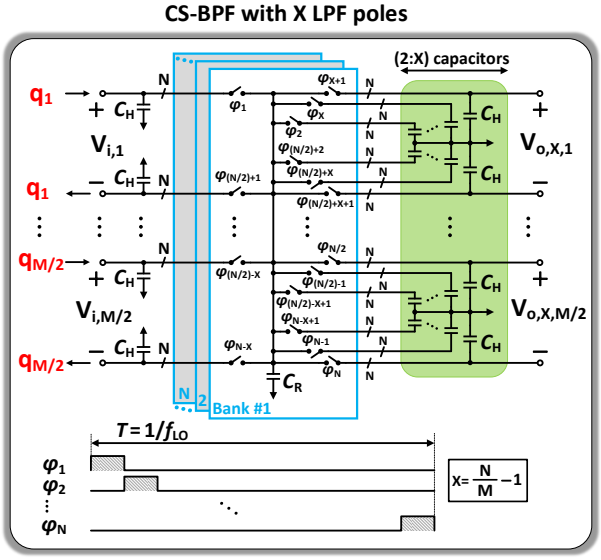
where, k and a are the same as (6.2) and (6.3), respectively. We find the center frequency of the filter to be

$$f_{IF} = \frac{f_s}{2\pi} arctan\left(\frac{(1-a)sin(\pi/8)}{a + (1-a)cos(\pi/8)}\right). \tag{6.10}$$

To summarize, the blocker-resilient 8/16-phase CS-BPF features a sharp and



(a) ***M/M*-phase CS-BPF** (b) ***M/(2M)*-phase CS-BPF**



(c) ***M/N*-phase CS-BPF**

Figure 6.5: Various full-rate M/N-phase CS-BPF configurations.

highly linear transfer function (TF) in order to filter images and out-of-band blockers even at $3^{rd}/5^{th}$ harmonics of LO. The out-of-band filtering of blockers is improved significantly compared to [34, 37] by increasing the number of input phases of CS-

BPF and adding the LPF pole between each pair of adjacent input history capacitors. The center frequency of the filter is fully controllable by the capacitance ratios and sampling frequency, thus making it insensitive to PVT.

Fig. 6.5 proposes various configurations of the single-stage full-rate CS-BPF: (a) without the additional LPF poles; (b) with one LPF pole; and (c) with $X = (N/M-1)$ LPF poles between the adjacent history capacitors. For extending the CS-BPF to a general form, we use the notation of "M/N-phase CS-BPF", where it has M inputs, M outputs, N history capacitors, N non-overlapped clock phases with a duty-cycle of $D = 1/N$, and X LPF poles in the charge-sharing loop. Inputs of the filter are interpreted as differential charge packets, $q_1, q_2, ..., q_{M/2}$, that are phase shifted by $0, 2\pi/M, 4\pi/M, ..., (M-2)\pi/M$ radians and, for the first CS-BPF, provided by the M-phase DT mixer.

To support the full-rate operation, parallelism/interleaving techniques are used to increase the sampling frequency to $f_s = Mf_{LO}$ [37]. As in any sampling system, frequency components at $f_s \pm f_{IF}$ are folded to the desired frequency at IF. Therefore, larger values of M increase f_s, thus pushing away the closest folding frequencies. Similarly, increasing M improves the CS-BPF tolerance to blockers but at the same time introduces more complexity.

To investigate the transfer function of full-rate M/N-phase CS-BPF, the time-domain output voltage expressions at $t = nT_s$, where $T_s = 1/f_s$, can be derived as

$$V_{i,1}[n] = \frac{C_H V_{i,1}[n-1] + C_R V_{o,X,M/2}[n-1] + 2q_1[n]}{C_H + C_R}, \tag{6.11}$$

$$V_{i,h}[n] = \frac{C_H V_{i,1}[n-1] + C_R V_{o,X,h-1}[n-1] + 2q_h[n]}{C_H + C_R}, \tag{6.12}$$

$$V_{o,2,j}[n] = \frac{C_H V_{o,2,j}[n-1] + C_R V_{i,j}[n-1]}{C_H + C_R}, \tag{6.13}$$

$$V_{o,l,j}[n] = \frac{C_H V_{o,l,j}[n-1] + C_R V_{o,l-1,j}[n-1]}{C_H + C_R}, \tag{6.14}$$

where $i \in [1, M/2], j \in [1, M/2], h \in [2, M/2]$, and $l \in [3, X]$. By performing a conversion from time-domain to z-domain , the general transfer function and center frequency can be derived as

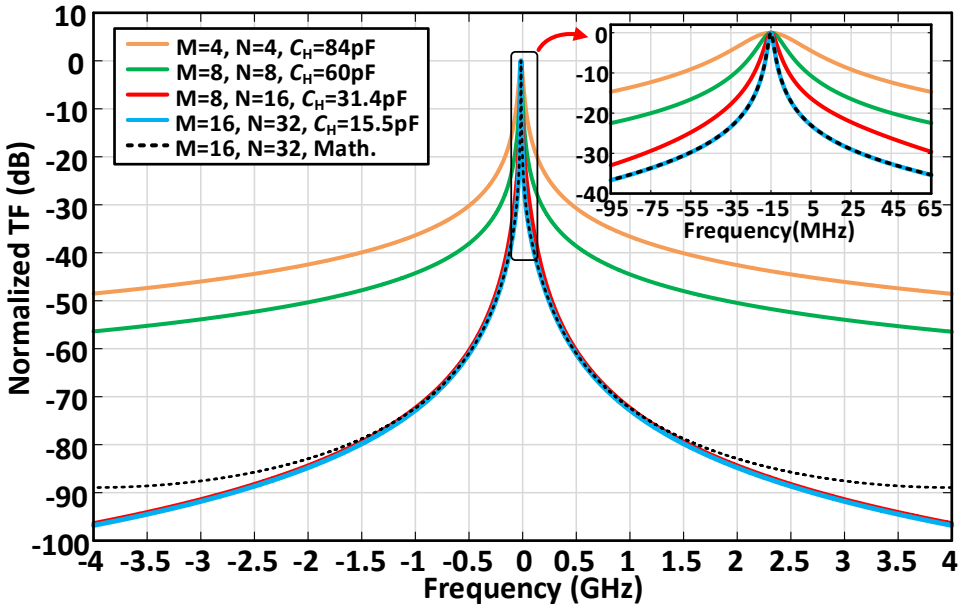


Figure 6.6: Ideal transfer function of M/N-phase CS-BPF.

$$H_{M/N}(z) = \frac{\sum_{l=1}^{M/2} (V_{o,X,l}(z)) e^{j(2l-2)\pi/M}}{\sum_{l=1}^{M/2} (q_l(z)) e^{j(2l-2)\pi/M}} \tag{6.15}$$

$$= \frac{k \cdot \left((1-a)z^{-1}\right)^{\frac{N}{M}-1}}{(1-az^{-1})^{N/M} - e^{j2\pi/M}\left((1-a)z^{-1}\right)^{N/M}},$$

and

$$f_{IF} \approx \frac{f_s}{2\pi} arctan\left(\frac{(1-a)sin(2\pi/N)}{a+(1-a)cos(2\pi/N)}\right), \tag{6.16}$$

where, k and a are the same as (6.2) and (6.3), respectively. The simulated and calculated normalized complex transfer functions are plotted in Fig. 6.6 for the conventional (i.e., 4/4-phase), 8/8-, 8/16-, and 16/32-phase CS-BPF with the following conditions: C_R=1 pF and f_s=8 GHz, and the same IF frequency (f_{IF}=15 MHz). The switch resistance is assumed to be sufficiently small. Most notably, the filter-

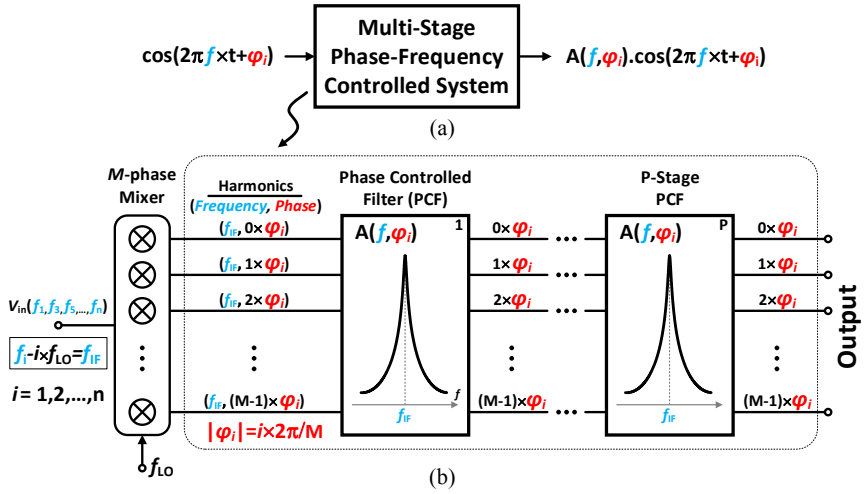


Figure 6.7: Concept of (a) multi-stage phase-frequency controlled system, (b) multi-stage phase-controlled filter (PCF).

ing characteristic of the M/N-phase filter is improved substantially for higher M. Filter's rejection for far-out frequencies depends on its order. Since both 8/16- and 16/32-phase CS-BPFs have a 2^{nd}-order characteristic, they have the same rejection at far-out frequencies. Nevertheless, the close-in rejection of the 16/32-phase filter is higher than that of 8/16-phase. Also, the calculated transfer function based on (**??**) agrees well with simulations.

6.5 Harmonic Rejection

The differential mixer driven by a square-wave clock is a linear time-variant circuit that down-converts the desired signal together with undesired interferers at higher LO harmonics. In narrow-band receivers, those interferers are not of a major concern because of a customary RF band filtering right after the antenna. In *wideband* RF receivers, such RF band select filtering would be very difficult, so it is the LO harmonics instead that need to get rejected. The required level of LO harmonic rejection (HR) is 60–100 dB, which is almost impossible with only one HR stage due to practical amplitude and phase mismatches. A two-stage HR was introduced in [48], but it prevents further HR improvements because of the non-redundant (i.e., quadrature) signal representation. In this section, we propose a mismatch insensitive HR concept that can be arbitrarily cascaded without any bound on the HR capability.

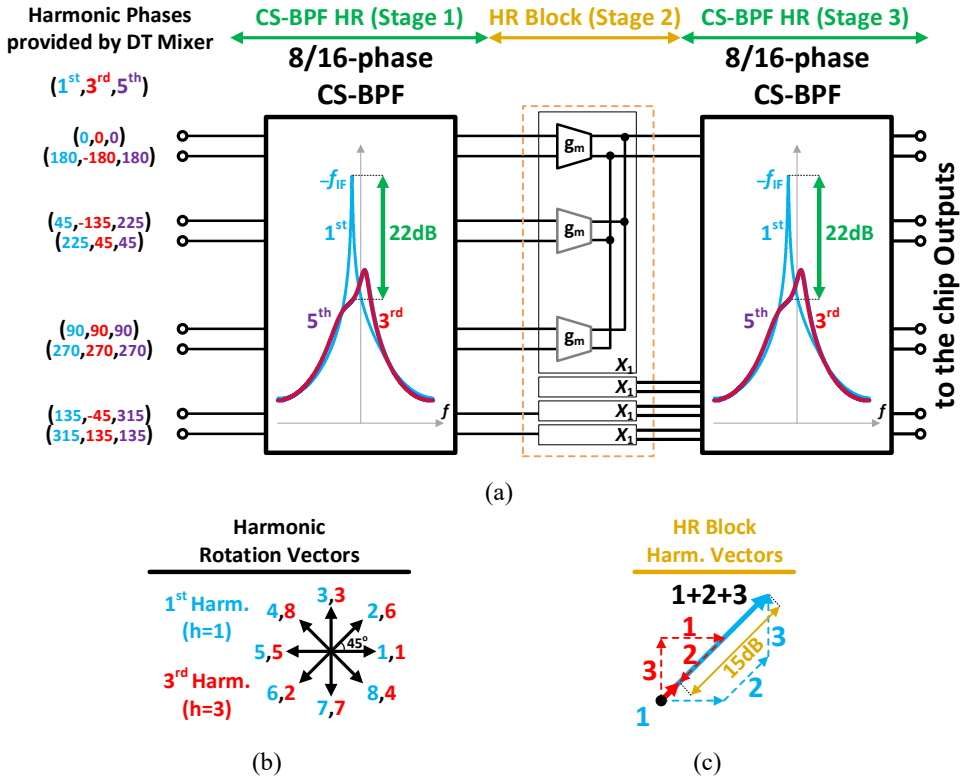
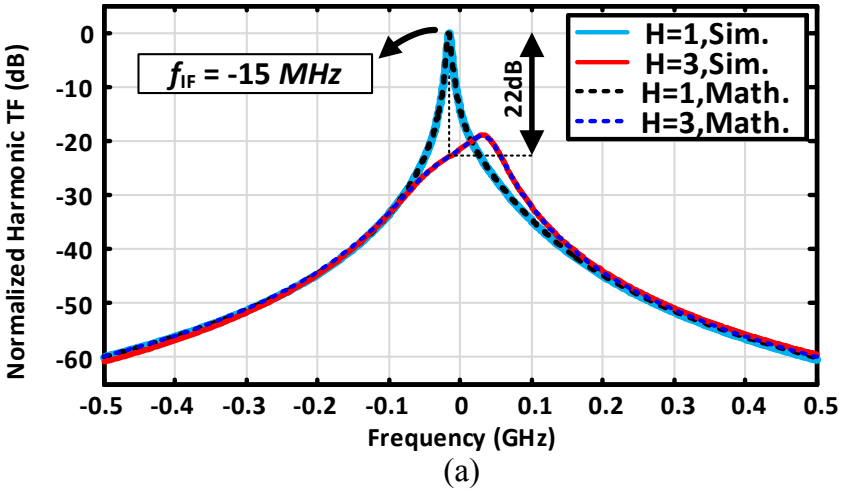
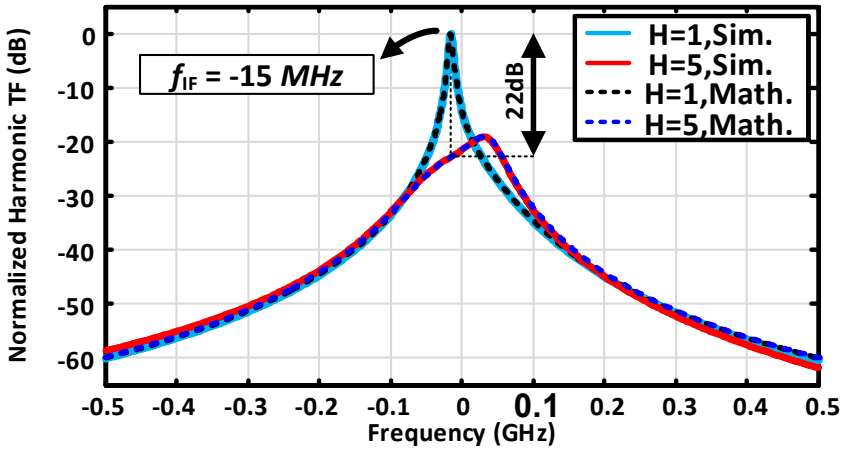


Figure 6.8: (a) Proposed harmonic rejection stages in the superheterodyne receiver, (b) harmonic rotation vectors and (c) harmonics cancellation summation.

Fig. 6.7(a) starts with a high-level model of a multi-stage phase-frequency control system. Its key feature is that the harmonic transfer function depends on *both* the input frequency f and phases $\phi_i, i = 0, 1, 2, \cdots$. Multiple phases ϕ_i can be generated with an M-phase mixer, shown in Fig. 6.7(b), which not only down-converts the desired signal at the fundamental but also does the interferers at higher $3^{\text{rd}}, 5^{\text{th}}, ..., \text{n}^{\text{th}}$ LO harmonics to the same IF frequency with multiple phases of $|\varphi_i| = (i-1) \times 2\pi/M$ where $i = 1, 2, ..., M$. Therefore, instead of storing the harmonic information in the frequency domain, as is the case before the mixer $(f_1, f_3, f_5, ..., f_n)$, it is now stored as phases in the M mixer output lines, with $M > 4$ to ensure redundancy, where it will be preserved as long as the number of lines is maintained. The multiple phases in M lines can be processed by the phase-controlled filter (PCF) leading to a different transfer function for every harmonic.



(a)



(b)

Figure 6.9: Transfer functions of 8/16-phase CS-BPF for different harmonics, both calculated and simulated.

6.5.1 CS-BPF Harmonic Rejection Concept

In our implementation, the PCF HR circuitry consists of three stages in total, as shown in Fig. 6.8. It includes two stages of CS-BPFs. Although the 1^{st} and $3^{rd}/5^{th}$ input harmonics are down-converted to the same IF frequency by the octal mixer, the phase difference between two adjacent lines for the 1^{st} and $3^{rd}/5^{th}$ harmonics are $\pi/4$ and $(-3\pi/4)/(5\pi/4)$, respectively. The charge-sharing phases of the signal for the 1^{st} (blue), 3^{rd} (red) and 5^{th} (purple) harmonics are shown in Fig. 6.8(a). Assuming the even harmonics are removed due to the differential configuration, the

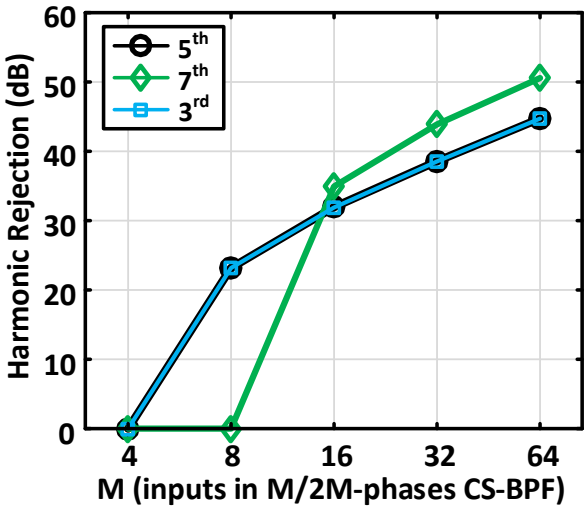


Figure 6.10: Harmonic rejection of 8/16-phase CS-BPF for different harmonics versus M.

phase difference of odd harmonics is sensed by CS-BPF and so the general harmonic TF of the M/N-phase CS-BPF and φ_i can be found as

$$H(z,\varphi_i) = \frac{1/(C_R+C_H)\cdot\left((1-a)z^{-1}\right)^{\frac{N}{M}-1}}{(1-az^{-1})^{N/M}-e^{j\varphi_i}\cdot((1-a)z^{-1})^{N/M}}, \tag{6.17}$$

$$\varphi_i = (-1)^{\frac{i-1}{2}}\times i\times 2\pi/M, \tag{6.18}$$

respectively, where, $i\in[1,2,...,n]$, and a is equal to (6.3). Fig. 6.8(b) shows the corresponding arrangement of phase rotation vectors. The HR for $3^{\text{rd}}/5^{\text{th}}$ harmonics is ∼22 dB for each CS-BPF, which can be infinitely improved by cascading CS-BPFs since the octal format fully preserves the harmonic information. HR is further improved by the proposed "stage-2"İ HR block. It consists of four X_1 blocks, each comprising three *identical* g_m-cells adding three adjacent vectors. This results in amplification of the 1^{st} and partial rejection of the $3^{\text{rd}}/5^{\text{th}}$ harmonic vectors, as shown in Fig. 6.8(c). The two proposed techniques are mismatch insensitive and do not require any calibration, whereas other well-known approaches, such as HR-mixers [6, 48–51] , suffer from such sensitivity so they require extensive calibration. Also, HR-mixers and switch-capacitor HR [52] cannot be further enhanced because the combined output signals are converted to I/Q (quadrature), thus causing irreversible aliasing of the harmonic phase information.

The simulated normalized transfer functions of the $1^{st}, 3^{rd}$ and 5^{th} harmonics are compared in Fig. 6.9 with calculations based on (6.17). The following conditions apply: C_R=1 pF, C_H=31.4 pF and f_s=8 GHz. The plots verify that the 3^{rd} and 5^{th} harmonics are attenuated by 22 dB. Furthermore, based on (6.17), the $3^{rd}, 5^{th}$ and 7^{th} harmonic rejection levels are plotted in Fig. 6.10 versus the number of inputs M for the $M/2M$-phase CS-BPF. The conditions are: C_R=1 pF, C_H=31.4 pF and f_s=8 GHz.

6.6 Design and Implementation of the Receiver Chain

We have described so far the evolution of the M/N-phase charge-sharing band-pass filter (CS-BFP) towards its full exploitation as an image reject filter in the fully integrated SAW-less discrete-time superheterodyne receiver. In this section, we describe a detailed design implementation of the receiver, starting with various operational modes of the fully reconfigurable M/N-phase CS-BPF.

6.6.1 4/16-Phase and 8/16-Phase CS-BPFs

The two implemented CS-BPF filters are each programmed as either quadrature (4/16-phase) or octal (8/16-phase). In either mode, the filter is clocked by 16 non-overlapped signals with D=1/16 and the filter's center frequency is located at IF with no replicas present. The 16 history, C_H, and 16 rotating, C_R, capacitors in the full-rate CS-BPFs shown in Fig. 6.5(b) and (c), are actually 8 differential capacitors each, in order to save the chip area by ×4. Also, due to the differential implementation, common-mode voltage and even-order nonlinearity of the prior stages are canceled out. C_H and C_R are digitally tunable with 8-bit binary-weighted codes to support variable IF of -10 MHz up to -90 MHz for 2G band.

6.6.2 Clock Generation Circuitry

Block diagram of the clock generation is shown in Fig. 6.11. An external sinusoidal input is converted to a 50% duty-cycle clock after passing through the input buffer. It drives three clock generation circuits. The first circuit provides all the clock phases required for the RF mixer while the remaining two provide all the clock phases for the CS-BPFs. All three circuits are independently programmable to operate in either the octal or quadrature mode. In these modes, the mixer clock generation has a respective output duty-cycle of 12.5% and 25%, while the clock for both CS-BPFs is always at D=6.25%, as shown in Fig. 6.11. To be able to further save dissipated power, the dividers are used to enable decimation by 1, 2 or 4 for both CS-BPF stages.

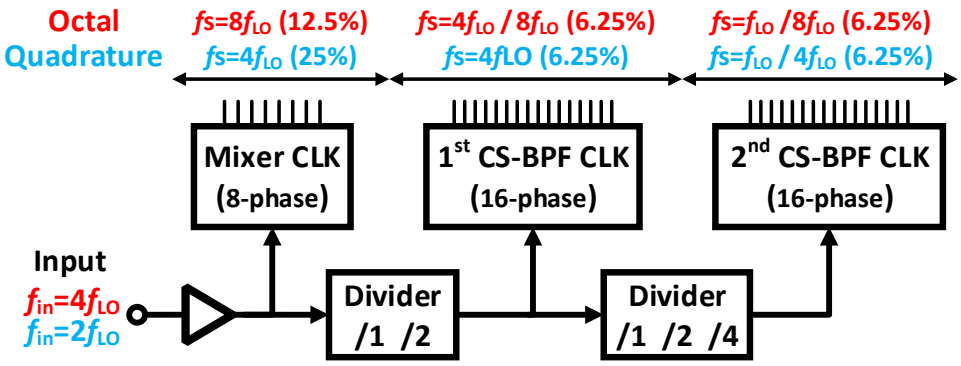


Figure 6.11: Clock generation block diagram.

Functional block diagram of the clock generation circuitry for the mixer and the two CS-BPF stages is the same. Fig. 6.12 shows an example of the mixer LO generation. The CK and $\overline{\text{CK}}$ input clocks with D=50% are driving 8 and 4 dynamic latches connected back-to-back in a loop for the octal and quadrature modes, respectively. The latch outputs are followed by digital gates, which produce 12.5% (octal) and 25% (quadrature) duty-cycle clocks. The final output is selected between the octal or quadrature outputs by 8 multiplexers. Therefore, in the quadrature mode half of the mixer switches are off.

The effect of LO phase noise or jitter on the switch capacitor circuits is discussed in detail in [53–55]. It can be proven that the CS-BPF and generally passive switch capacitor filters are robust to many nonidealities such as clock jitter, charge injection, nonzero rise/fall times of the clock, and switch resistance [55]. Moreover, there is no need to have a special clocking scheme such as bootstrapped driving and dummy switches [55]. Also it has been shown that integration sampler, IIR, FIR filters are exceptionally robust to the clock jitter [55]. The results can be further generalized for the CS-BPF.

6.6.3 Low-Noise Transconductance Amplifier (LNTA)

Fig. 6.13(a) shows a fully differential schematic of the proposed LNTA, which simultaneously features low NF and high IIP3 (only single-ended signal waveforms are shown). The noise-canceling common-gate transistors (M_{n1}/M_{n2}) provide the RX input matching. The noise-canceling operation is as follows: the input signal gets amplified by transistors M_{n1}/M_{n3} and M_{p1} in a differential feed-forward manner, whereas the thermal noise of M_{n1} channel experiences subtraction at the output nodes because of the out-of-phase correlated noise voltages at V_x and V_{outn}. The 3$^{\text{rd}}$-

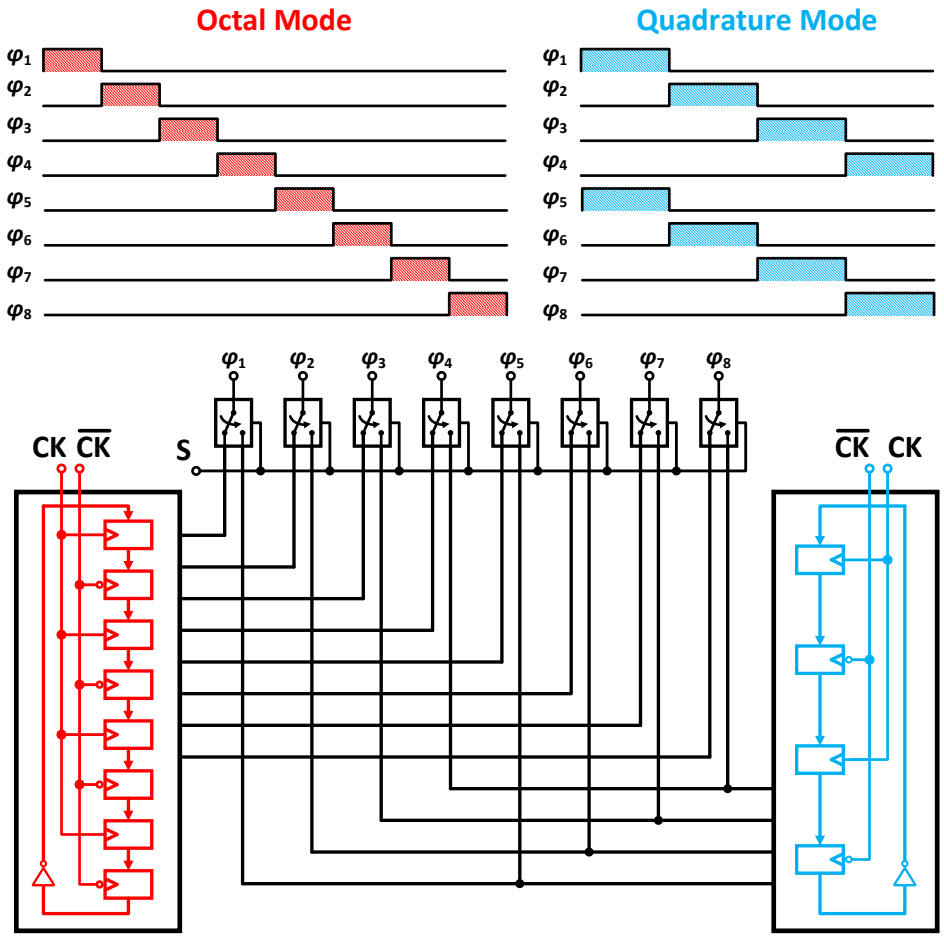


Figure 6.12: Functional block diagram of the mixer clock generation for both octal and quadrature modes.

order non-linearity of M_{n1} and M_{n3} can be simultaneously canceled at the differential output because M_{n1} and M_{n3} operate in weak and saturation regions, respectively, resulting in out-of-phase g_{m3} (3^{rd}-order transconductance) to each other. Therefore, partial cancellation of the IM3 component happens at the differential output. The cancellation happens at the desired frequency because at other frequencies an additional IM3 is generated due to the 2^{nd}-order non-linearity of M_{n3}. Simulated (with extracted parasitics) NF and gain of LNTA with a resistive load is shown in Fig. 6.13(b) across 0.1–4 GHz.

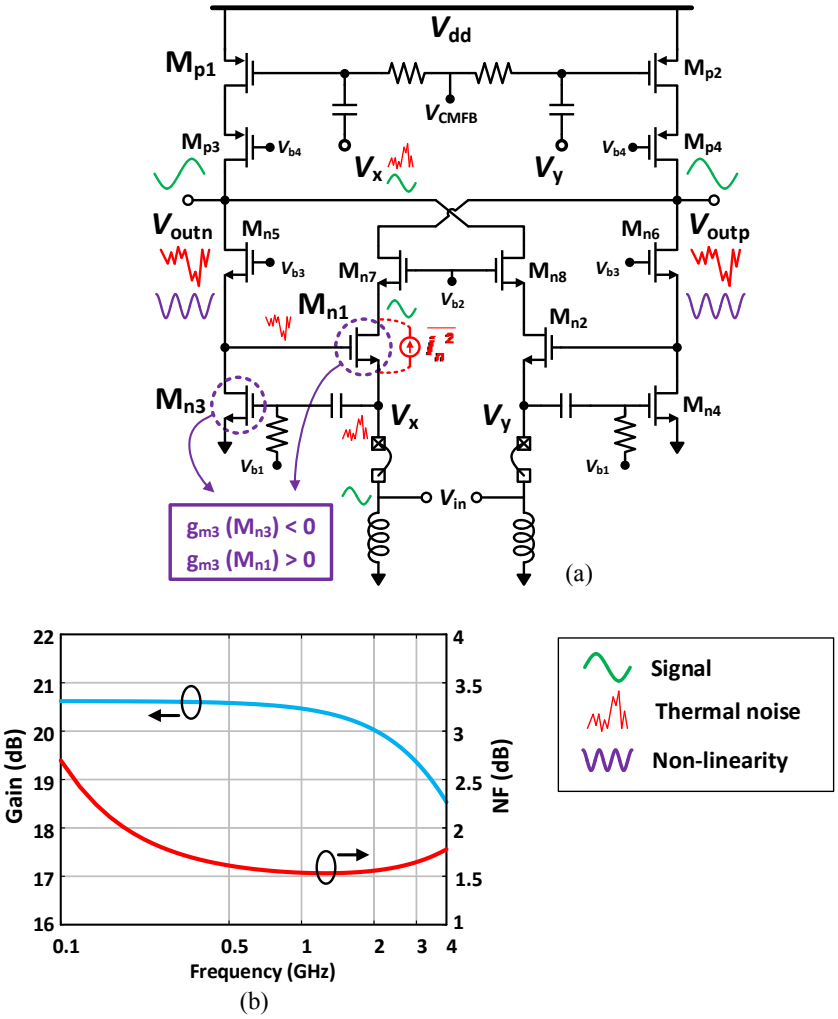


Figure 6.13: (a) LNTA schematic, and (b) it post-layout simulated noise figure and gain.

6.6.4 IF Stage Transconductance Amplifier (g_m-cell)

Fig. 6.14 shows a schematic of the pseudo-differential inverter-based IF transconductance amplifier with a common-mode (CM) rejection load. The g_m-cell operates at 0.9 V supply and a pair of complementary thick-oxide PMOS/NMOS transistors is utilized to increase the transconductance linearity to >+11dBm (simulated) for all corner cases within a temperature range of −30°C to 100°C [56]. The common-mode

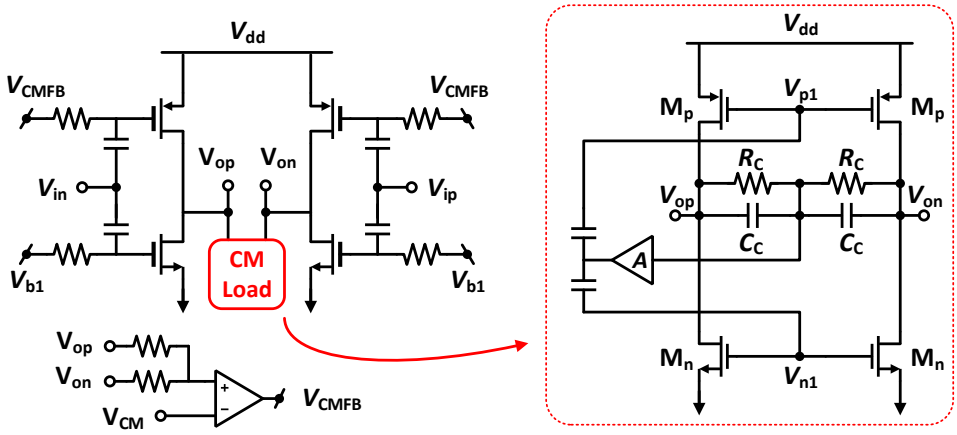


Figure 6.14: The IF g_m-cell schematic with common-mode rejection load.

feedback circuitry provides a proper bias of $V_{DD}/2$ to the outputs.

To suppress any possible CM oscillation in the RX chain, the CM gain of the g_m-cell is drastically reduced by placing a CM load at its output. It features different impedances for the CM and differential-mode (DM) signals. The impedance for DM signals is very high; it is proportional to the small-signal drain resistance of the CM load transistors M_n and M_p, while the impedance for CM signals is very low, equal to $1/((g_{mn} + g_{mp})A)$, where g_{mn} and g_{mp} are the small-signal transconductance of M_n and M_p.

6.7 Measurement Results

Fig. 6.15 shows the chip micrograph of the proposed superheterodyne RX for 4G cellular mobiles realized in TSMC 28 nm CMOS [1]. The active area is 0.52 mm^2, which is mostly occupied by C_H and C_R capacitors of the two CS-BPFs. Both the receiver and clock inputs are differential and so wideband "hybrids" are used to interface with 50 Ω single-ended instrumentation. All the measurements are performed at high RX gain without any calibrations, even those concerning the linearity. The chip is wire-bonded to a printed circuit board (PCB) providing DC and RF input connectivity ports, while high-IF output signals are measured with a high performance oscilloscope, as shown in Fig. 6.16 and the characteristics of PCB lines and cables are de-embedded from the measurement results. The transfer function measurement setup of the RF CS-BPF is shown in Fig. 6.16. After providing the proper power supply voltages, the serial peripheral interface (SPI) controls internal registers. The quadrature (I/Q) IF outputs are connected to high performance

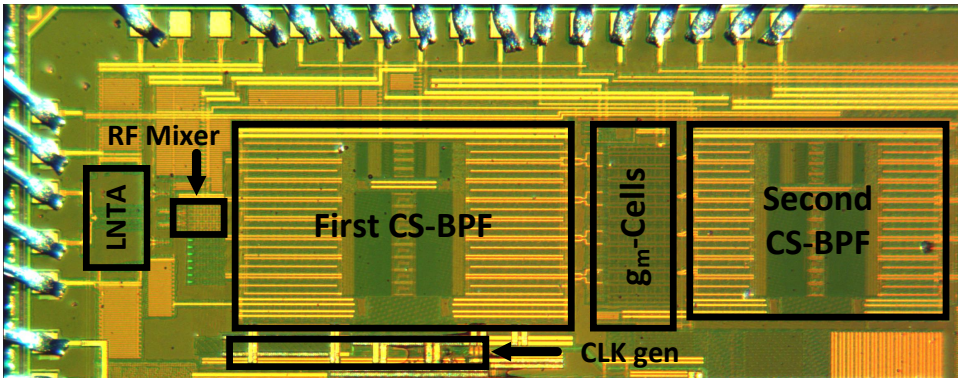


Figure 6.15: Chip micrograph of the proposed discrete-time superheterodyne receiver.

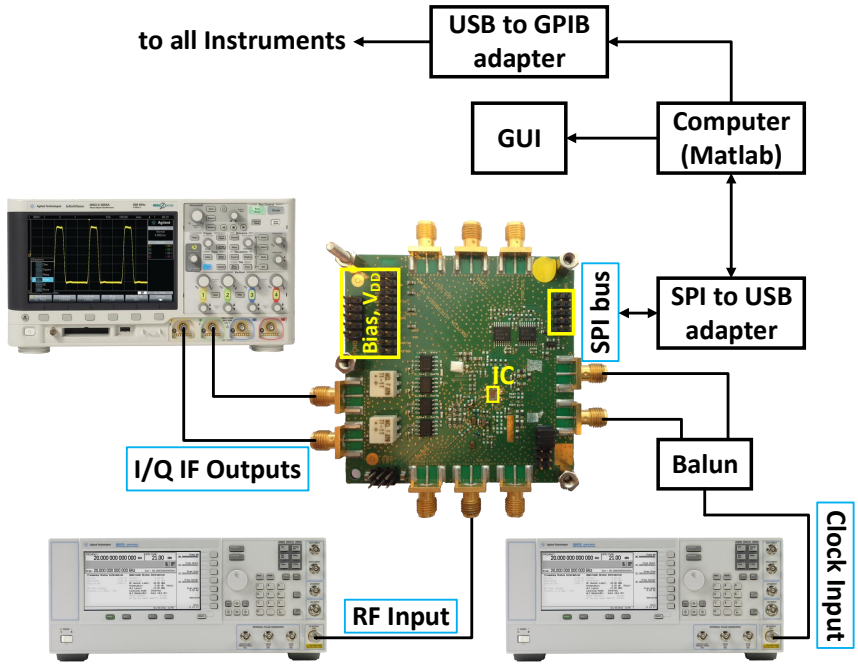


Figure 6.16: Chip micrograph of the proposed discrete-time superheterodyne receiver.

"DSO-X 3052A" digital oscilloscope.

Matlab scripts are developed to make the chip testing automatic or semi-automatic. the graphical user interface (GUI), shown in Fig. 6.17 are designed to facilitate the testing process and visualize results of close-in transfer function, wideband transfer

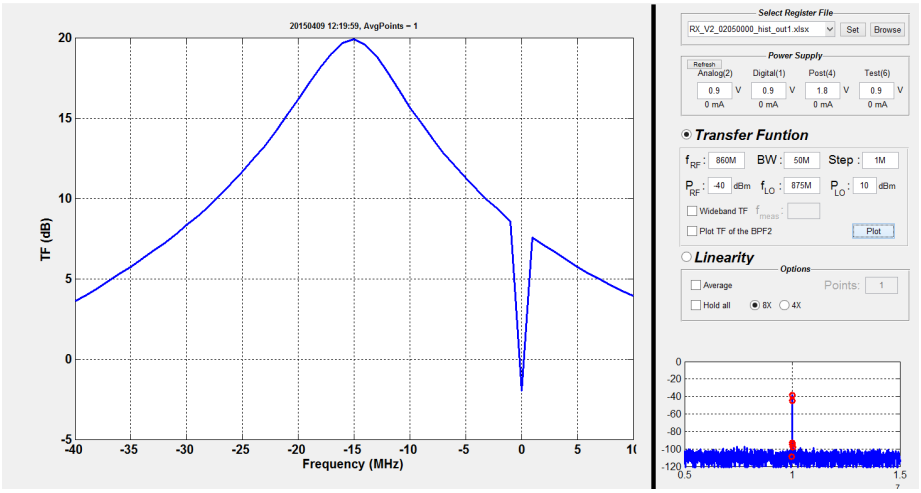


Figure 6.17: GUI interface for chip testing for: (a) transfer function, and (b) linearity measurements.

function, IIP2, IIP3 and CP linearity measurements. The LO frequency and RF input frequency are applied to the chip through GPIB connection and FFT of the output I/Q IF signals have been taken in the MATLAB script.

The measured normalized transfer functions are shown in Fig. 6.18 for "2G band-

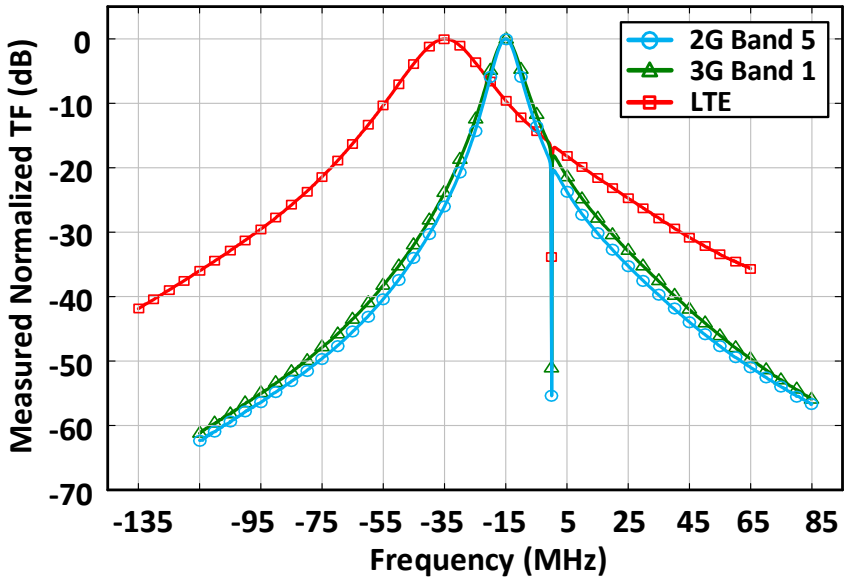


Figure 6.18: Measured RX transfer function for different bands.

5", "3G band-1" and "LTE" with 0.85, 2.1 and 2.5 GHz RF input frequencies. The RX bandwidth is 6.5 MHz for 2G/3G and 20 MHz for LTE, while IF frequency is -15 MHz and -35 MHz for 0.85–2.1GHz and 2.5GHz carriers, respectively. Also, the absolute value of IF in the proposed receiver can be variable in a face of large blocker, within the range of 10–90 MHz, 25–220 MHz, and 29–262 MHz for 2G, 3G, and LTE bands, respectively.

Fig. 6.19 shows the RX gain at 0.85 GHz and 2.1 GHz carriers for I channel only. By recombining the I/Q channels, an extra 6 dB gain can be obtained. The overall pass-band gain of LNTA and 1st CS-BPF in 2G band-5 and 3G band-1 is around 18 dB and 17.5 dB, respectively. The gain of IF g_m-cell and 2^{nd} CS-BPF is measured by subtracting the total RX gain from the gain provided by LNTA and 1st CS-BPF. That peak gain value is 17 dB and 16.5 dB for 2G and 3G, respectively. The total RX gain is between 29–35 dB for 0.85–2.5 GHz carriers. Although the 1st and 2^{nd} CS-BPFs are identical, the former shows a sharper filtering characteristic due to a larger output resistance of LNTA versus that of IF g_m-cell.

The comparisons of measured transfer functions of LNTA and 1st CS-BPF with calculations per (6.17) are shown in Fig. 6.20(a) and (b), respectively, for 3rd and 5th harmonics. The difference between the measured and calculated 1st harmonic at IF is due to the effect of LNTA output impedance. The 19 dB rejection of 3rd and 5th harmonics per each CS-BPF stages is measured at IF.

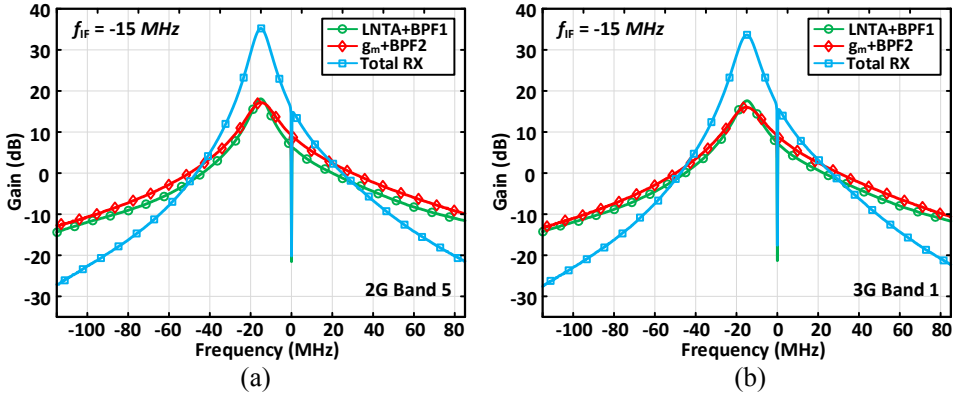


Figure 6.19: Measured RX gain versus output frequency.

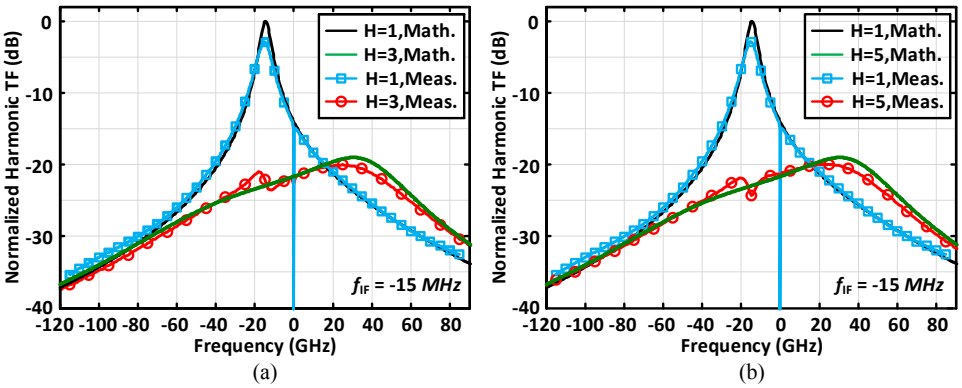


Figure 6.20: Comparison of the normalized measured $1^{st}, 3^{rd}$ and 5^{th} harmonic TF with calculation for 2G band. All transfer functions are normalized to maximum gain of 1^{st} harmonic extracted from the calculation.

The measured wideband transfer functions in the normal and HR modes for three ICs is shown in Fig. 6.21. All the images are rejected by more than 65 dB, including the IF image, in all three measured ICs without any calibration. The worst-case HR of 58 dB is achieved when the HR-block is enabled: 38 dB from the two-stage CS-BPFs, 17dB from the HR-block, and the rest is provided by the LNTA's limited bandwidth. The highlighted images are multiples of smallest LO frequency in the clock generation circuitry with an offset of $\pm f_{IF}$.

Fig. 6.22 plots the measured receiver NF of 2.1–2.6 dB with an LO frequency of 865 MHz, 2115 MHz and 2535 MHz for 2G, 3G and LTE, respectively. The minimum

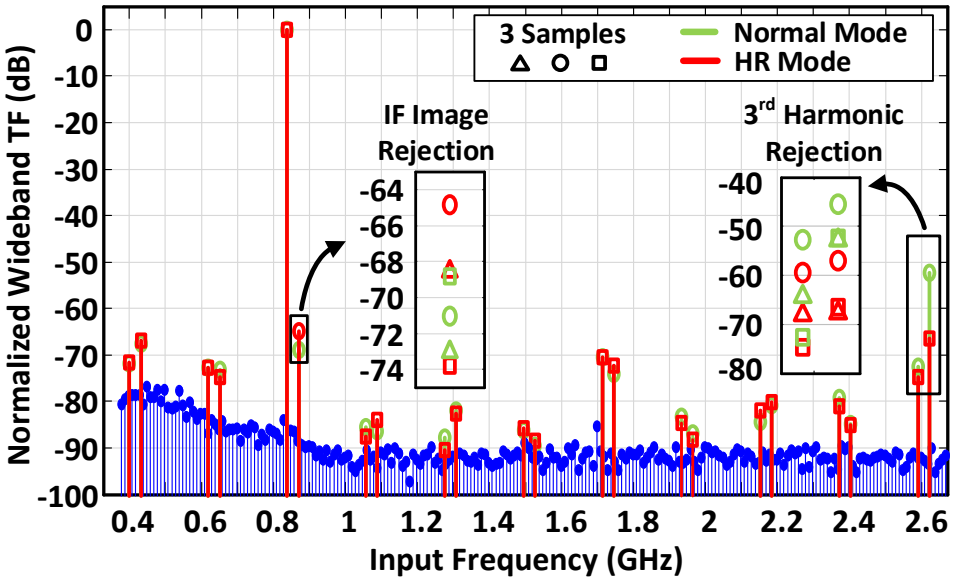


Figure 6.21: Measured wideband transfer function of the complete RX.

Table 6.1: Noise figure contribution of each building block in the RX chain

	LNTA	RF Mixer	CS-BPF1	IF g_m-cell	CS-BPF2
2G band-5 [%]	89.27	0	4.97	4.98	0.78
3G band-1 [%]	84.89	0	6.86	6.81	1.44

noise figure in each standard happens at the center frequency of CS-BPFs, which coincides with the IF location. Also, the NF contribution of each building block is summarized in Table 6.1 for 2G band-5 an 3G band-1.

The simulated (post-layout extracted) out-of-band IIP3 of CS-BPF is more than +30 dBm. Furthermore, because of its strong blocker filtering, out-of-band IIP3 is mainly determined by the linearity of LNTA. Fig. 6.23 shows the measured out-of-band IIP3 of the RX versus offset frequency for 2G and 3G. It should be mentioned that the linearity was measured at the maximum gain (i.e., the lowest noise figure) and without any calibration. The variation of out-of-band IIP3 over offset frequency is due to the linearity dependency of LNTA on the offset frequency. The peak IIP3 of +14 dBm is achieved for the offset frequencies specified by the 2G/3G standards at duplex (f_{TX}) and half duplex ($(f_{TX} + f_{RX})/2$) frequencies.

For the IIP2 measurements, there are several IIP2 test cases that the two most important ones are:

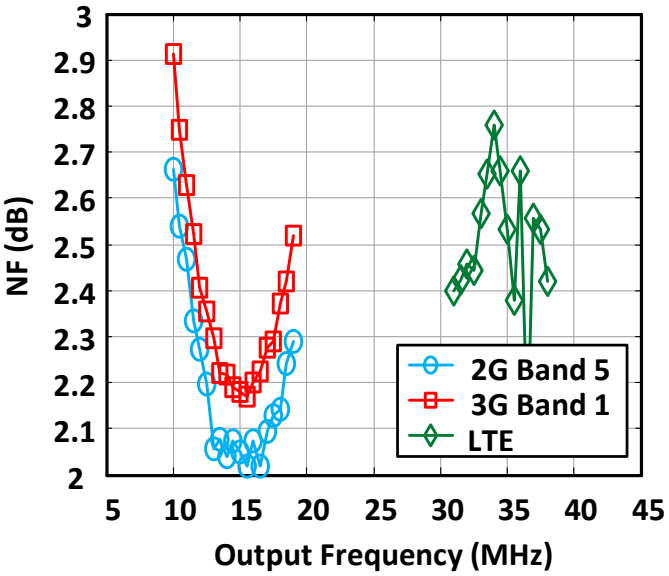


Figure 6.22: Measured noise figure for 2G, 3G and LTE bands.

1. closely spaced tones or a modulated single tone IIP2 test case (limitation in mixer IIP2)

2. far away two-tone cases (limitation in LNA)

The test case that prevent us from removing the SAW filter is the first one since if there were no SAW filter in the RX chain, the IIP2 of more than +90dBm would be needed. The second test case is the one that should be also investigated in wideband RXs. However, it is not actually that *stringent* compared to the first test case. Let us calculate the needed IIP2 for the second test case. Assuming the blocker level of -32.5 dBm applied to the RX, if we need a sensitivity of -99 dBm and SNR of 9 dB to maintain the signal purity. The IM2 component should be below -108 dBm. Therefore, the needed IIP2 for the second test case is 43 dBm. To clarify the situation, we have performed an IIP2 measurement for both test cases.

For the first test case, since the RX architecture is superheterodyne with an IF frequency of -15 MHz to -35 MHz, the applied two-tone or one modulated tone with 7.5 MHz bandwidth will be down-converted to around DC, thus *completely* filtered-out.

For the second test case, two tones are far away from each other and the generated IM2 is actually in-band. In the proposed RX, the two tones should be located at $f_{RF} + spacing$ and $2f_{RF} + spacing$ while f_{RF} is 860 MHz in 2G band-5. As shown

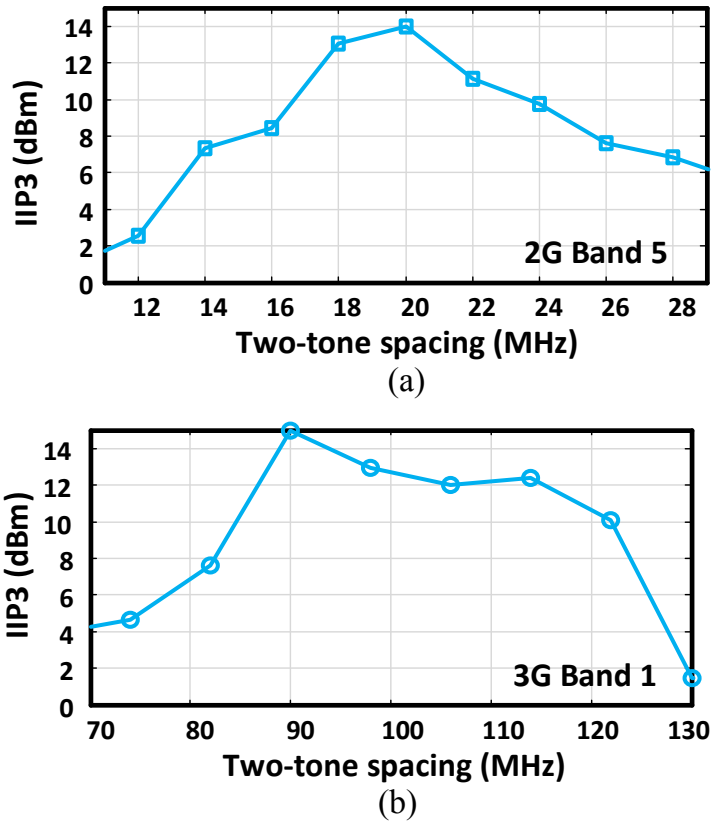


Figure 6.23: Measured IIP3 for (a) 2G and (b) 3G bands versus frequency offset.

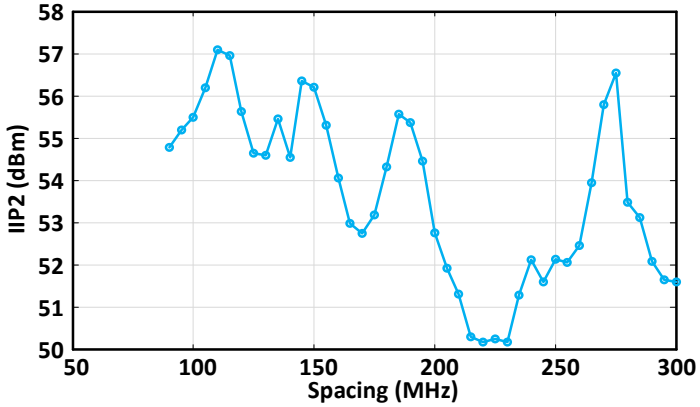


Figure 6.24: Measured IIP2 for far away two-tone case at $f_{RF} + spacing$ and $2f_{RF} + spacing$ while f_{RF} is 860 MHz versus spacing.

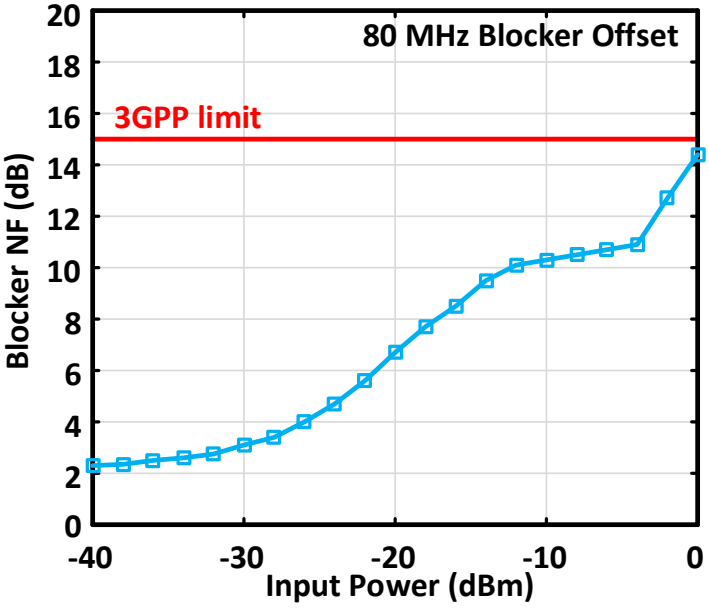
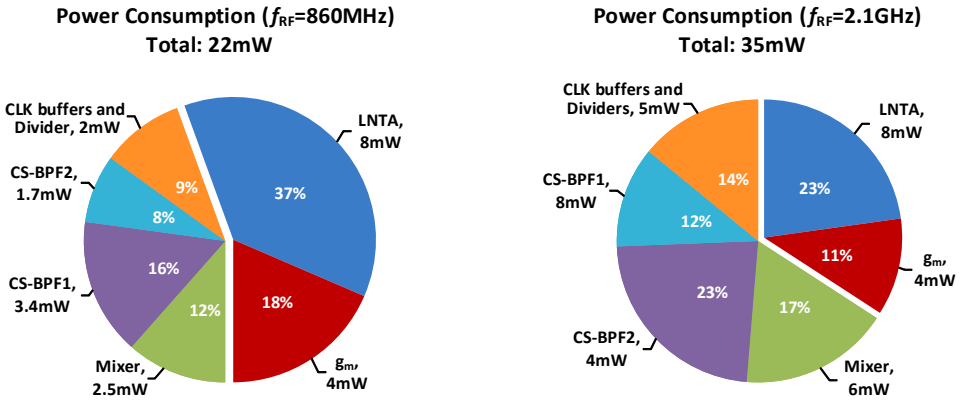


Figure 6.25: Measured blocker noise figure at 80 MHz offset frequency.



(a) (b)

Figure 6.26: Measured RX power consumption for (a) 2G band-5 (f_{RF} = 860 MHz); and (b) 3G band-1 (f_{RF} = 2.1 GHz) carriers.

Table 6.2: Performance summary and comparison with state-of-the-art

	This work	[27] JSSC '11 Broadcom	[34] *ISSCC* '14 TUDelft	[6] JSSC '14 IMEC	[7] *ISSCC* '14 Broadcom	[5] *ISSCC* '14 MediaTek	[4] JSSC '13 UPavia
Architecture	Superheterodyne			zero-IF			
CMOS Tech. [nm]	28	65	65	28	28	40	40
SAW-less	Yes	No	No	Yes	Yes	Yes	Yes
RF Input	Differential	Single-Ended	Differential	Differential	Differential	Differential	Differential/Single-Ended
RF Frequency [GHz]	0.5–2.5	1.8–2.2	1.8–2.5	0.4–6	0.1–3.3	0.85–2.4	1.8–2.4
NF [dB]$^{\#}$	2.1/2.2/2.6	2.8	3.2–4.5	(1.8–3)(4.6†)	1.7	1.7–2.4	3.8/1.9
Supply [V]	0.9	1.2/2.5	1.2/2.0	0.9	1.0	1.5	1.2/1.8
HR [dB]	>58*	N/A	N/A	50(70$^{\$}$)	60/60	N/A	54/65
OB-IIP3 [dBm]	14	-6.3	—	8/5	11.5	0.4	18/16
IB-IIP3 [dBm]	-10	-8.4	-7	+4**	—	1.9	—
OB-IIP2 [dBm]	Infinite§	N/A	85$^{¥}$	55(88$^{\$}$)	55	55	64
OB-Blocker NF [dB]	14	N/A	N/A	14(10†)	5	11	7.9
Image Rej. [dB]	>65*	35	37	N/A	N/A	N/A	N/A
S11 [dB]	<-10	<-10	<-10	<-10	<-10	<-10	<-10
Power [mW]	22/35/40	39	55-65	40/35	36–62	39–46.5	32/32
IF [MHz]	2G: 10–90 3G: 25–220 LTE: 29–262	110	27-200	zero	zero	zero	zero
Area [mm^2]	0.52	0.76	1.1	0.6	5.2	0.57	0.84/0.74

*Worst-case without calibration and measured 3 IC samples, $^{\$}$with calibration,
$^{¥}$due to an IF mixer(2^{nd} Mixer), † with optimized setting,
$^{\#}$1dB typical input balun loss should be included in TDD mode for RXs with differential inputs,
§for closely-spaced or modulated interferers, **Reduced gain setting

in Fig. 6.24, the IIP2 more than +50 dBm is achieved in a wide frequency spacing when the LNTA is set to mid gain because in that case there is no need for LNTA to be at high gain setting.

The RX blocker tolerance is demonstrated by means of the blocker NF tests. Fig. 6.25 shows the NF as a function of the 80 MHz blocker power. NF remains below the 15 dB limit for the ≤0 dBm blocker. Also an external BPF is used to reduce the impact of the LO generation phase noise on the input RF band.

The measured power consumption of the RX chip versus input frequency is shown in Fig. 6.26. The overall RX power consumption varies from 22 to 40 mW dependent on input RF band and related clock frequency. The main contributor to the overall RX power is analog part for "2G band-5". As the clock frequency increases for "3G band-1", the main contributor is the power consumed by DT part including RF mixer, CS-BPF1, CS-BPF2, and clock buffers and dividers.

Table 6.2 compares the proposed DT RX with state-of-the-art RXs. While being the best-in-class in meeting the key performance parameters without any calibration, its power consumption and area are generally the lowest, and it does not suffer from any issues related to DC offsets, flicker noise or IM2 products since its IIP2 is infinite.

6.8 Conclusion

A new architecture of a discrete-time superheterodyne receiver targeting a SAW-less operation of the 4G cellular standard is proposed and demonstrated. The consequence of reduced filtering at the antenna interface network forces much better linearity and filtering of the on-chip RF front-end. Consequently, the LNA is made wideband with a new noise cancellation scheme. The RF mixer and two stages of bandpass filtering are octal, which provides strong filtering and allows to naturally reject input harmonics. The CS-BPF with several extra LPF poles in charge-sharing rotation path has a blocker-tolerant transfer function, making it a suitable candidate not only for SAW-less superheterodyne receivers, but also for low-IF RXs. The architecture is realized in 28 nm CMOS and is amenable to further scaling.

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CHAPTER

7

Conclusion and Future Works

In this chapter, general conclusions are drawn. The reader is advised to refer to the detailed separate conclusions at the end of each chapter for further details.

Three different superheterodyne architectures have been investigated. Furthermore, a proof-of-concept chips are fabricated for each of the architectures and results are experimentally validated. Two of the receivers were implemented in 65 nm CMOS, while the third one was designed and implemented in 28 nm CMOS technology to meet SAW-less requirements.

This research has ultimately culminated in the proposal and demonstration of the new architecture of a discrete-time (DT) superheterodyne receiver targeting a SAW-less operation of the 4G cellular standard. The complete chain of the DT superheterodyne receiver with high reconfigurability for cellular and other wireless applications is described.

The full monolithic integration is made possible chiefly by the proposed DT band-pass filter (BPF). The general idea of charge-sharing (CS) for generating BPFs is developed such that they are free from replicas making them suitable for high-IF or superheterodyne receivers. The center frequency of the proposed BPF filters is digitally controllable via clock frequency and capacitor ratios, and thus making it insensitive to PVT variations. They are free from aliasing and replicas while operating at a GSample/s rate. The general idea of the CS-BPFs was investigated

and an inherent harmonic rejection of those filters was explored in detail.

The proposed architectures and building blocks are insensitive to flicker noise and time-varying DC offsets. The complete integrated chain of SAW-less superheterodyne cellular receiver is now feasible in silicon thanks to the high-Q CS-BPFs. The SAW-less superheterodyne RX shows an infinite IIP2 without requiring any calibration. The consequence of reduced filtering at the antenna interface network due to the removal of SAW filters forces much better linearity and filtering of the on-chip RF front-end. Consequently, the LNA is made wideband with a new noise cancellation scheme. DT signal processing using passive switched-capacitor circuits makes this receiver process scalable. It only uses switches, capacitors, and inverter-based gm-cells.

While we have demonstrated the SAW-less superheterodyne receiver, I believe there are still a lot of things that need to be done, such as adding carrier aggregation while sharing some of the building blocks in the front-end to save the cost. Furthermore, the RF input frequency of the SAW-less DT superheterodyne receiver is up to 2.5 GHz and the maximum allowable RF input frequency can be further improved up to 6 GHz in order to cover the full frequency range of software-defined radios (SDR). This could be done by designing a separate LNTA and mixer connected to the common 1st CS-BPF for the frequencies between 2.5–6 GHz.

In summary, this work has shown that the proposed DT SAW-less superheterodyne architecture is the way to the future of the RF receivers.

Summary

There are nowadays strong business and technical demands to integrate radio-frequency (RF) receivers (RX) into a complete system-on-chip (SoC) realized in scaled digital processes technology. As a consequence, the RF circuitry has to function well in face of reduced power supply (V_{DD}) while the CMOS device threshold voltage (V_{th}) stays almost constant. Therefore, a conventional or continuous-time (CT) approach could not be efficiently utilized to design and implement the SoC, whereas a discrete-time (DT) approach offers the advantage for RF building blocks to operate properly in a smaller headroom. Furthermore, in finer CMOS technologies, transit frequency (f_T) increases while CT RF building blocks do not benefit except for low-noise amplifiers (LNA). However, the performance of DT RF building blocks improves because of the higher sampling frequency (f_s), lower power supply, and sharper clock edges provided by technology scaling.

Nowadays, most integrated RF receivers are zero-IF (ZIF) because of well-known advantages such as less complicated architecture and easy channel-selection integration. They require many external duplexers, surface acoustic wave (SAW) filters, and switches, typically one per band, to attenuate out-of-band (OB) blockers. However, there are many issues associated with ZIF receivers such as time-variant DC offsets, sensitivity to $1/f$ (flicker) noise, large in-band LO leakage, and second-order nonlinearity. For solving those issues, high-performance cellular SAW-less ZIF receivers now require extensive calibration efforts. For example, an intensive input 2^{nd}-order intercept point (IIP2) calibration must be simultaneously operated in the background with DC offset and harmonic rejection (HR) calibrations. Also, this calibration is susceptible to many factors such as variations in power supply, process corner, temperature, RF blocker frequency, local oscillator (LO) frequency, LO power, and channel frequency.

On the other hand, a superheterodyne architecture pushes the IF frequency much higher so that the aforementioned problems are eliminated. Despite the advantages, the superheterodyne radios have not been utilized in cellular receivers simply because

of the difficulty with integration of a high quality (Q)-factor band-pass filter (BPF) for image rejection in CMOS using CT circuitry.

In this thesis, a new class of filters, i.e., charge-sharing (CS), is discussed that is being invented and developed to be utilized in not only superheterodyne but also in ZIF receivers. The proposed filter not only filters OB-blockers but also rejects interferers at the harmonic of LO frequency which is an extraordinary advantage especially for SAW-less receivers when there is no external filtering prior to the receiver input. Using these techniques, for the first-time ever, the superheterodyne receiver is proposed that meets the specification for SAW-less receivers.

Chapter 1 briefly provides an overview of the blocks inside conventional RF radio transceivers. It mentions that there is a tendency in RF transceivers to support many of the multi-mode/multi-band communication standards such as Fourth Generation (4G) cellular application, Bluetooth, and Wi-Fi in one SoC. Also, the organization of the thesis has been described in details in this chapter.

Chapter 2 establishes a common background for this thesis. Furthermore, it provides the background information for different sampling modes of operation such as subsampling (1x), half-rate sampling (2x) and full-rate sampling (4x) together with their frequency translations. Also, the technical mathematic background related to nonlinearity is briefly consolidated in this chapter.

Chapter 3 discusses the first implemented DT superheterodyne receiver that utilizes the full-rate (4x) sampling mode of operation to solve a number of issues related to previous DT receivers.

Chapter 4 explores performance capabilities and limitations of the proposed CS-BPF. A complex quadrature charge-sharing technique is proposed to implement a CS-BPF with a programmable bandwidth. It operates at the full sampling rate (4x), which was described in Chapter 2. Also, the complete noise analysis of the proposed CS-BPF is investigated. Additionally, the CT model of the CS-BPF is presented, and the filtering characteristic of proposed model has excellent agreement with the simulation result of the DT circuit. Finally, the implemented chip is fabricated in 65 nm CMOS, and the measured results are compared with simulations.

Chapter 5 explores the possibility of creating a high quality (Q)-factor BPF at a very high IF because the CS-BPF proposed in Chapter 4 does not provide adequate selectivity. As a result, a highly reconfigurable superheterodyne RX is proposed that employs a 3^{rd}-order complex IQ CS-BPF for image rejection and 1^{st}-order feedback based RF-BPF for channel selection filtering. The proposed RX is the first attempt to achieve high-Q factor BPF at a very high-IF without replicas and images. Furthermore, the chip is fabricated in 65 nm CMOS technology, and the simulated results are completely verified by the measured results.

Chapter 6 proposes and demonstrates the first-ever fully integrated SAW-less superheterodyne receiver for 4G cellular applications. The low-power DT RX introduces various innovations that simultaneously improve noise and linearity

performance: a highly linear wideband noise-canceling LNTA, a blocker-resilient octal CS-BPF, and a cascaded harmonic rejection circuitry. The chip is fabricated in 28 nm CMOS technology, the characteristics of the fabricated chip are extensively measured, and the results are compared with the simulations.

Chapter 7 draws the conclusions of this thesis work and provides recommendations for future research.

Samenvatting

Bij moderne radio-ontvangers streeft men vanuit kostenoverwegingen naar de integratie van een compleet systeem-op-chip (SoC) in digitale-halfgeleidertechnologie. Bij zo'n SoC integratie in digitale-CMOS technologie wordt gebruik gemaakt van steeds kleinere dimensies, wat resulteert in een reductie van de toelaatbare voedingsspanning (V_{DD}) terwijl de drempelspanning van de gebruikte transistoren (V_{th}) nagenoeg gelijkt blijft. Hierdoor kan de analoge ofwel tijd-continue ("continuous-time", CT) aanpak niet langer worden toegepast bij het ontwerp van de SoC. Daarentegen maakt de tijd-discrete ("discrete-time", DT) aanpak, in deze kleinere spanningsruimte, wel goed werkende RF-schakelingen mogelijk. Ook neemt voor geavanceerde CMOS technologieën, bij steeds kleinere dimensies, de transistorafsnijfrequentie (f_T) verder toe waarvan de CT-RF bouwblokken, met uitzondering van de lage-ruis versterker (LNA), echter niet noemenswaardig profiteren. Daarentegen maakt deze technologieschaling wel verbeterde prestaties van de DT-RF bouwblokken mogelijk d.m.v. een hogere bemonsteringsfrequentie (f_s), een lagere voedingsspanning en steilere klokflanken. Tegenwoordig gebruiken de meeste geïntegreerde RF ontvangers een "Zero-IF" (ZIF) architectuur vanwege de bekende voordelen, namelijk, een verminderde complexiteit en een eenvoudigere kanaalselectie. Deze architectuur vereist echter veel externe duplexers, "Surface Acoustic Wave" (SAW) filters en schakelaars. In de praktijk, meestal één per frequentieband om de "out-of-band" (OB) stoorsignalen te verzwakken. Er zijn echter veel problemen verbonden aan ZIF ontvangers. Zoals de tijdsafhankelijke-gelijkstroom afwijkingen en de gevoeligheid voor; $1/f$ (flikker) ruis, in-band LO lekkage en tweede-orde niet-lineariteiten. Voor het verhelpen van deze problemen vereisen moderne mobiele ZIF ontvangers, die geen gebruik maken van SAW filters, een uitgebreide kalibratie. Zo moet b.v. de kalibratie voor het verhogen van het 2^e-orde ingangs-interceptie punt (IIP2) gelijktijdig worden uitgevoerd met die van de DC-offset en "harmonic rejection" (HR) kalibratie. Ook zijn er veel factoren die deze kalibratie beïnvloeden zoals variaties in; voedingspanning, proces, temperatuur, stoorsignaalfrequentie, lokale oscillator

(LO) frequentie, LO vermogen en het gekozen ontvangstkanaal.

Bij een superheterodyne architectuur is de IF-frequentie veel hoger waardoor de bovengenoemde problemen niet langer aanwezig zijn. Ondanks dit voordeel worden superheterodyne radio's niet gebruikt in CT gebaseerde mobiele ontvangers. Dit vanwege de problemen die optreden bij de CMOS integratie van een banddoorlaatfilter (BPF) met een hoge kwaliteitsfactor (Q), welke vereist is voor de onderdrukking van de spiegelfrequentie.

In dit proefschrift wordt een nieuwe filter klasse, gebaseerd op ladingdeling (charge-sharing (CS)), geïntroduceerd en ontwikkeld die niet alleen gebruikt kan worden in super-heterodyne maar ook in ZIF ontvangers. Dit filter onderdrukt niet alleen OB-blokkers, maar ook de stoorsignalen bij de harmonische frequenties van de LO, wat een belangrijk voordeel is in SAW-vrije ontvangers wanneer er geen extern filter aanwezig is. Gebruikmakend van deze technieken introduceren we een nieuw type superheterodyne ontvanger die voor het eerst in de geschiedenis voldoet aan de specificaties voor SAW-vrije ontvangers.

Hoofdstuk 1 geeft een beknopt overzicht van de functieblokken in conventionele RF radio-ontvangers. Er wordt ingegaan op de algemene trend bij RF ontvangers om meerdere multi-mode/multi-band communicatiestandaarden te ondersteunen in een enkele SoC, zoals: de vierde-generatie mobiele communicatie (4G), Bluetooth en Wi-Fi. Ook wordt de opbouw van dit proefschrift gedetailleerd besproken.

In **Hoofdstuk 2** wordt de algemene achtergrond van dit proefschrift gegeven. Het verschaft ook achtergrondinformatie over diverse bemonstering modi zoals "sub-sampling" (1x), "half-sampling" (2x) en "full-sampling" (4x) met hun bijbehorende frequentieomzetting. Tevens wordt de wiskundige achtergrond voor het berekenen van niet-lineaire effecten beknopt toegelicht.

In **Hoofdstuk 3** wordt een eerste implementatie van de DT superheterodyne ontvanger besproken die gebruik maakt van een "full-sampling rate" (4x) bemonsteringtechniek om een aantal van de problemen gerelateerd aan eerdere DT ontvangers op te lossen.

Hoofdstuk 4 onderzoekt de prestaties en beperkingen van de voorgestelde CS-BPF. Een complexe kwadratuur-ladingsverdeling techniek wordt geïntroduceerd om een CS-BPF te implementeren met een programmeerbare bandbreedte. Deze configuratie werkt op de "full-sampling rate" (4x) die eerder al werd beschreven in hoofdstuk 2. Tevens wordt er een complete ruisanalyse gegeven van het voorgestelde CS-BPF. Aanvullend wordt het CT-model van de CS-BPF getoond, waarvan de filter eigenschappen van dit model goede overeenkomsten vertonen met het gesimuleerde resultaat van het DT circuit. Tenslotte is de ontworpen chip gefabriceerd in een 65 nm CMOS proces en worden de meetresultaten vergeleken met simulaties.

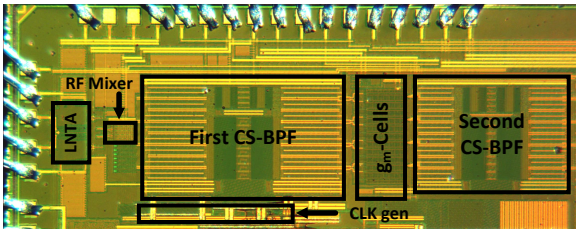
Hoofdstuk 5 onderzoekt de mogelijkheid om een BPF met een hoge kwaliteitsfactor (Q) te maken op een zeer hoge IF, omdat de in hoofdstuk 4 behandelde CS-BPF niet de juiste selectiviteit verschaft. Als resultaat wordt een her-configureerbare

superheterodyne RX voorgesteld, die werkt met een complexe 3^e-orde IQ CS-BPF voor de onderdrukking van de spiegel-frequentie en een eerste-orde tegengekoppeld RF-BPF voor de kanaalselectie. Deze geïntroduceerde RX is de eerste poging om een BPF met een hoge Q-factor te realiseren op een zeer hoge IF zonder last te hebben van replica- en spiegel frequenties. Ook deze chip is gefabriceerd in 65 nm CMOS technologie en de gesimuleerde resultaten zijn geverifieerd met de meetresultaten.

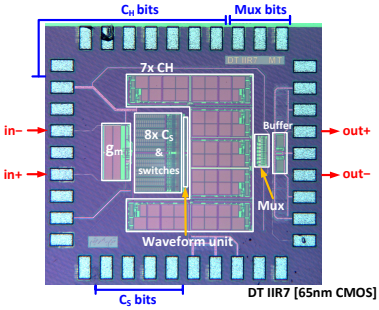
In **Hoofdstuk 6** wordt voor de allereerste keer een volledig geïntegreerd SAW-vrije super-heterodyne ontvanger (RX) voor 4G mobiele toepassingen getoond. Deze laagvermogen DT-RX introduceert diverse innovaties die samen de ruis en lineariteit prestaties verbeteren zoals: een zeer lineaire breedband-ruis-onderdrukking LNTA, een blokker bestendig CS-BPF en gecascadeerde schakelingen die de harmonischen onderdrukken. De chip is gefabriceerd in 28 nm CMOS technologie, de eigenschappen van de gefabriceerde chip zijn gemeten en vergeleken met de simulaties.

In **Hoofdstuk 7** worden de conclusies en aanbeveling voor toekomstig onderzoek gegeven.

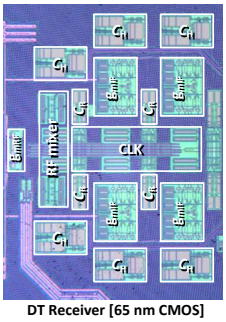
Fabricated ICs



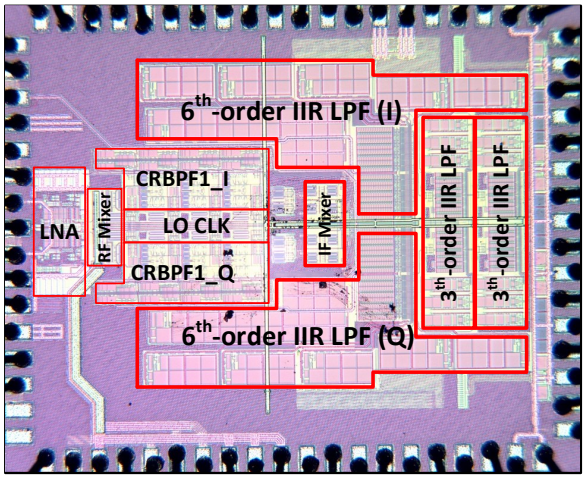
SAW-less DT Receiver [28 nm CMOS]



DT IIR7 [65nm CMOS]



DT Receiver [65 nm CMOS]



DT Receiver [65 nm]

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Journal Papers

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[3] M. Tohidian, **I. Madadi**, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 49, iss. 11, pp. 2575–2587, Nov. 2014. [IEEE Xplore link (Open Access)]

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- M. Tohidian, **I. Madadi**, and R. B. Staszewski, "Superheterodyne receiver," WO2013189547, Published on 27-Dec-2013.
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گلعذاری ز گلستان جهان مارا بس — زین چمن سایه آن سرو روان مارا بس
من و همصحبتی اهل ریا دورم باد — از گرانان جهان رطل گران مارا بس
قصر فردوس به پاداش عمل می بخشند — ما که رندیم و گدا دیر مغان مارا بس
بنشین بر لب جوی و گذر عمر ببین — کاین اشارت ز جهان گذران مارا بس
نقد بازار جهان بنگر و آزار جهان — گر شمارا نه بس این سود و زیان مارا بس
یار با ماست چه حاجت که زیادت طلبیم — دولت صحبت آن مونس جان مارا بس

Poet: Hafez (Ghazal number: 268)

Iman Madadi
October 16, 2015
Delft, The Netherlands

About the Author

Iman Madadi received the B.S.E.E. degree from K. N. Toosi University of Technology, Tehran, Iran, in 2007, and the M.S.E.E. degree from the University of Tehran, Tehran, Iran, in 2010. He is currently working toward the Ph.D. at Delft University of Technology, The Netherlands. He was a consultant at M4S/Hisilicon, Leuven, Belgium, in 2013–2014, designing a 28 nm SAW-less receiver chip for mobile phones. His research interests include analog and RF IC design for wireless communications. He holds six patents and patent applications in the field of RF-CMOS design.