Delft University of Technology
Master's Thesis in Computer Engineering

Digital Control of Multi-channel RF Energy Harvesters

Ehsan Zabihi

embedded software

TU Delft Delft University of Technology

Digital Control of Multi-channel RF Energy Harvesters

Master's Thesis in Computer Engineering

Embedded Software Section
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands

Ehsan Zabihi
e.zabihi@student.tudelft.nl, ehsan@nowi-energy.com

23rd February 2018

Author
Ehsan Zabihi (e.zabihi@student.tudelft.nl, ehsan@nowi-energy.com)
Title
Digital Control of Multi-channel RF Energy Harvesters
MSc presentation
28th February 2018

Graduation Committee

Dr. Arjan van Genderen	Committee member Contact address: a.j.vangenderen@tudelft.nl
Prof. Dr. Koen Langendoen	Chair Contact address: k.g.langendoen@tudelft.nl
Dr. Przemysław Pawełczak	University supervisor Contact address: p.pawelczak@tudelft.nl
Dr. Andre Luis Rodrigues Mansano	Company supervisor Contact address: andre@nowi-energy.com

Preface

This master thesis designed an adaptive matching network for an RF block of an energy-harvesting sensor.

Reaching to this point was not possible without the help of many people. At first, I am very grateful to my parents who have supported me in my life and my education. I also would like to thank Dr. Przemysław Pawełczak, my supervisor at TU Delft, and Dr. André Mansano, my supervisor at Nowi-Energy B.V. I learned a lot from their feedback during my thesis.

Since this thesis has been performed at Nowi-Energy B.V, I also would like to thank people there. I am thankful to Simon Van der Jagt, CEO, and Omar Link, COO of Nowi for the opportunity, facilities, and instruments they provided me to work on my thesis.

Contents

Chapter 1

Introduction

The advent of Wireless sensor networks (WSNs) is made feasible due to advances in sensor systems and components. Thanks to the ultra low power *Microcontrollers*, low power communication protocols, and ultra low power sensors, there are still challenges in this field such as suppling the sensor[1].

Many different methods have been offered by now to supply these sensors. Each has different applications generally. It is possible to supply the required energy of sensors from light, heat, mechanical vibrations, and radio frequencies [2]. The common thing between all these sources is that it is possible to supply any type of WSNs via these sources.

The concept of powering sensors wirelsessly brings us to define a new type of sensors. Technically, sensors which are powered and communicated wirelessly are called *Autonomous Sensors* which work as the nodes to collect data in WSN. The less power consumption they have, the more they become autonomous. Since they work most of their time in *inactive mode*, their average power consumption can be reduced. This makes powering them via environmental sources less difficult.

Generally, powering an autonomous sensor can be done via batteries or *energy harvesting* techniques. Since using batteries for many number of sensors imposes cost, moving to energy harvesting sources removes this issue. Among many different energy harvesting sources which were mentioned, RF signal is a good candidate thanks to the growing number of WiFi signals indoor and GSM signals outdoor.

RF signals are emitted by electromagnetic waves which they carry information. At the same time, the electromagnetic signals are carrier of energy. Depending on the transmitter-receiver distance, received electromagnetic signals have different strengths. This power can produce energy in a proper designed receiver. This receiver circuit is called *Energy harvester* which is embedded in an autonomous sensor. The efficiency of energy harvester is crucial since the amount of stored energy is dependent on the energy harvesting block.

The efficiency of this block is dependent on different number of circuits in the energy harvesting section of the sensor. These circuits can be designed separately by keeping in mind to have the maximum efficiency. However, since these blocks are connected to each other as input source or as a load, they have bidirectional effect on each other. This reason pushes designers to combine the energy harvesting blocks to one block called *rectenna*.

In a rectenna, different factors play rule to boost the efficiency. Efficiency of the matching block, *quality factor* , efficiency of the rectifier, impedance of the antenna, and load impedance of the rectifier are the factors which have impact on the rectenna efficiency. On the other hand, these parameters are dependent on the received RF signal frequency.

What makes the rectenna efficiency maximized is the matching between the rectifier and the matching block of the antenna. Since an autonomous sensor can be installed in different places with different RF signals frequencies, an automatic system is required to adapt the rectenna for each environment.

1.1 Problem Statement

It will be shown that to be able to gain the maximum energy, the antenna of harvester should be matched to the proper frequency which has the highest energy. The matching system connects to the interface between rectifier input and output of antenna matching block. Since the rectifier has nonlinear input impedance variable with frequency and input power [3], the matching process is crucial. From another point of view, this matching is needed since it is not possible to have an antenna which is able to cover hundreds of megahertz of bandwidth and offering high quality factor at the same time. The quality factor has direct proportion to the amount of harvested energy. This means, the higher the quality factor, the more it is possible to harvest. In other words, the challenge is maximizing sensitivity to boost the output voltage of harvester and its efficiency. The current RF energy harvesters for battery-less sensors lack an intelligent block [4], [5], [6], [7] needed to adapt antenna to the most powerful frequencies for a wide range of frequency and with a simple design. The comparison table 2.1 shows the advantages of this design over the other design from different perspectives. This block is designed such a way that it searches for all the frequencies in different bands. Then, it finds the frequencies with the power above a certain threshold. The frequency with the highest energy in a certain band is selected at the end of the process. The process is repeated after a certain period of time to search for other frequencies. If there is a better candidate, the matching network of antenna will be tuned on the new frequency. Otherwise, the previous frequency will be kept.

The block explained above is the core of the design. However, the energy

consumption of this system should be kept in mind due to the fact that the energy of an autonomous sensor is very limited. The proposed block should not consume a lot in comparison to the energy consumption of the whole sensor and at the same time should increase the efficiency of the whole sensor. In this thesis, we will review all the needed requirements for this design and presents the designing steps in details.

To design and implement the idea, a system architecture point of view is followed. The idea starts with a needed application. Therefore, we used a *top-down* approach by starting with the *requirements* of the system. Designing continues with simulation of the idea in *system level*. A system level simulation is then applied to verify the system level design. Next, a *gate level* analysis is studied to investigate more on the implementation level of the design. The energy consumption and performance analysis are done by looking at circuit level step.

This thesis tries to answer to the following research question. The question is: How to design a digital control system to tune the matching network of an energy harvester to boost harvesting efficiency?

1.2 Thesis Organization

Chapter 2 presents background and related work in the field. Chapter 3 provides the GSM and WiFi signal measurements. Chapter 4 discusses the design, modeling, and simulation of the designed system in system level. Chapter 5 presents the lower level design of the system. Chapter 6 concludes and discusses the future work.

Chapter 2

Background

To be able to implement our idea, we first need to introduce general concepts in autonomous sensor. Then, we can proceed to the design steps in the next chapters.

An autonomous sensor which is depicted in 2.1 can be divided into the following blocks[8]. *Power source* supplies the sensor system. From a power source point of view, the rest of the sensor is considered as a *load*. Power source can be a primary battery, a RF harvester, or a solar harvester in an autonomous sensor. The *power management* block manages the need of load with respect to the capability of power source. Depending on how this block is designed in comparison with the load and power source, it can even decrease the efficiency of the system. It should be noticed that while power management block tries to manage the supply of the whole system for different supply inputs, it consumes some power as well as a load. An example of this system can be implemented using the*BQ25570* from *Texas Instruments* [9]. This component is a low power energy harvesting chip for power management in WSNs.

The block power management is responsible for supplying the components of the sensor with the proper voltage. The input of the block can be any type of energy harvesting source.

The load itself consists of three other blocks. The first block of the load is *sensor*. They should be low power enough to be enable to supply them with limited power source.

The next block is an *MCU*. This unit receives and calculates the data from the sensor and sends it to the next block for wireless transmission of data.

The third block is *wireless transceiver*. Again for this block, the low power protocols should be considered [11].

After specifying the type of blocks for an autonomous sensor, *power profile* of the load is important to study and consider. IoT sensors are mostly designed in such a way that they are in *inactive* or *sleep mode* most of the

time and they are *active* only for a small fraction of time. At the same time, due to leakage current of circuits, energy consumption of the whole sensor belongs to its sleep mode mostly than its active mode. In addition, energy consumption of the active mode is in orders of magnitude bigger in comparison to sleep mode. Combination of active and sleep mode of the sensor pushes us to use *average power consumption*. Using average power consumption gives an overview of the power during time rather than looking only at peaks of power.

2.1 Power Sources of Autonomous Sensors

After giving a general explanation about different blocks of autonomous sensors, we need to focus on the power sources which can supply these sensors. It is possible to divide the power sources as below:

- Energy Harvesting

  The advance of technology in silicon from one side and high demand for wireless systems and IoT sensors from the other side made battery-less sensors very popular. This energy can be harvested from ambient sources. Many scientific papers ([12] and [7]) have proposed different sources of energy for harvesting. This thesis focuses only on RF harvesting systems and tries to design an adapting method to make RF harvesters more efficient.

- Primary Batteries

  Supplying sensors using batteries is much simpler than using energy harvesting methods. However, it has some drawbacks. The battery should be monitored and replaced with a new one during time. Not only does this cost money, but also it is a time-consuming task.

After reviewing different possible sources of power for sensors, we move to prove the energy harvesting idea. The next section presents the proof.

2.2 Reason for Antenna Matching Control

Paper [13] show that not only is it efficient to tune the antenna for the required frequency, but also it is critical for the performance of the system. Figure 2.2 depicts the *power* versus *frequency* of a filter for different *quality factors*. This figure also shows the relation between quality factor and the amount of *harvested energy*. The expression 'Q boosts voltage' can be defined as a rule in RF energy harvesting field. It means 'that the more Q, the more voltage and higher power'. In other words, wide band matching should not be applied for energy harvesting.

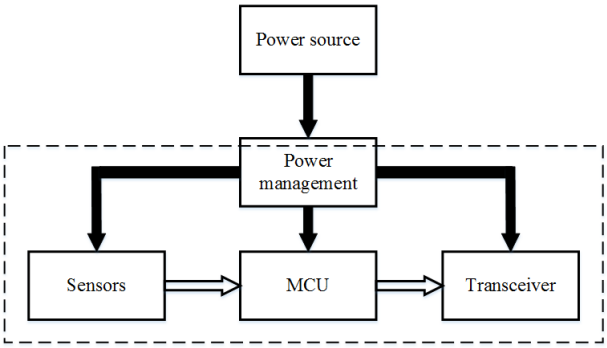


Figure 2.1: Components of an autonomous sensor. The dashed line separates the power supply and power consuming blocks. The blocks inside the box consume the power provided by the power source. The block power management is placed on the dash lines. This means that this block can be considered as a part of the load and also can be part of the power source [10]. Black arrows represent the supplied voltage of the sensor blocks. White arrows represent the data and instruction path between blocks.

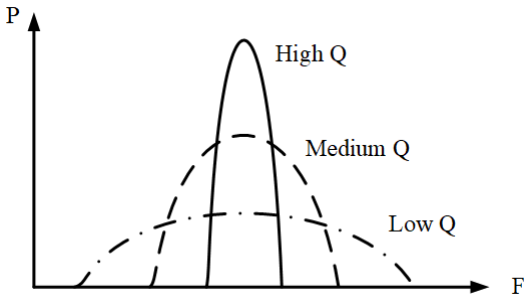


Figure 2.2: Power versus frequency[14].

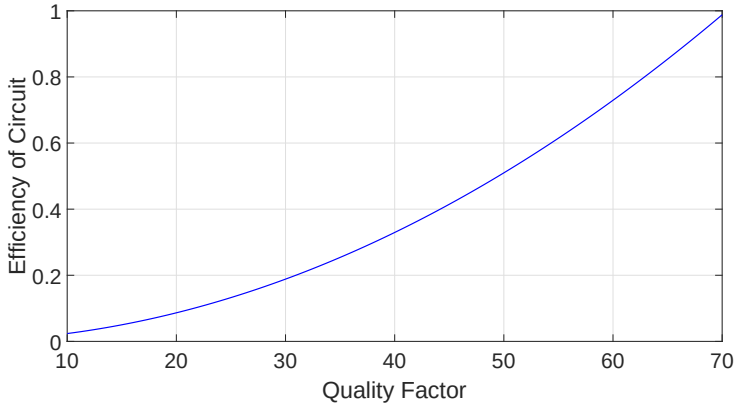


Figure 2.3: Efficiency of rectifier against quality factor.

In order to have higher efficiency, the antenna should be matched with the rectifier circuit. The importance of this idea is also proved in patents [15] and [8]. It is also shown in [16] and [17] the dependency of the harvested voltage to quality factor.

The available RF-power in the environment is spread over a wide spectrum and it is not constant. Only peaks of energy can be harvested over the spectrum.

The following relation shows that increasing in Quality Factor (Q) increases the Efficiency of the rectifier.

$$\eta_{circuit} = \frac{R_{ant}}{R_L} 2k^2(1+Q)^2 \tag{2.1}$$

Where k is assumed from 1 to 1.7, R_L is 10 MΩ by considering a resistive load, and R_{ant} of 50Ω. After proving this relationship, we can show how the efficiency is related to the Quality Factor.

The following relation shows the Efficiency of the matching network and the Quality Factor (Q) [13]:

$$\eta_m = \frac{1}{1+\frac{MMF}{Q}} = \frac{Q}{Q+MMF} \tag{2.2}$$

A parameter called Mismatch Factor (MMF) is defined as the amount of mismatch between matching network and the rectifier. Equation 2.3 formulates MMF[13]:

$$MMF = \frac{X_{in} + (R_{ant} - R_{in})}{R_{ant} + R_{in}} \tag{2.3}$$

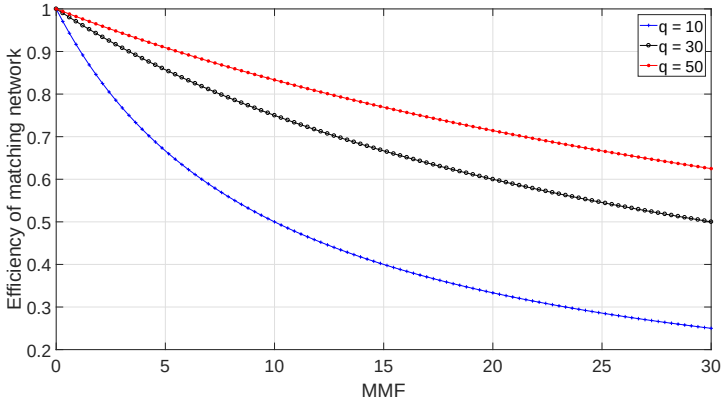
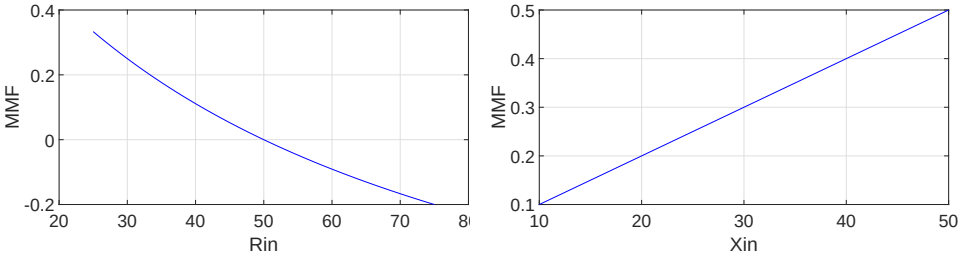


Figure 2.4: Efficiency of matching network against MMF.



(a) MMF against input resistance. (b) MMF against input impedance.

Figure 2.5: MMF against input resistances.

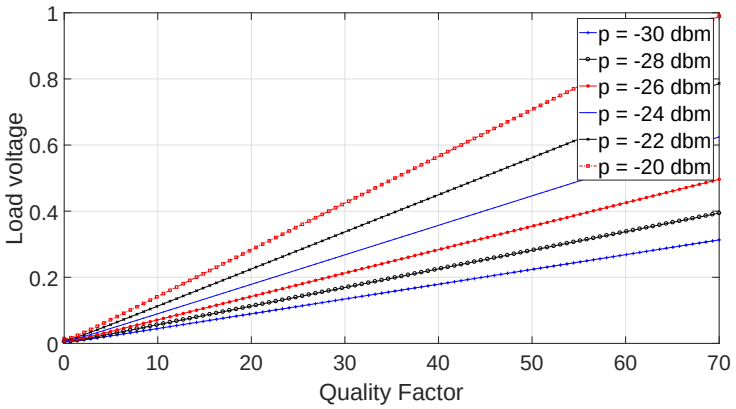


Figure 2.6: Load voltage versus quality factor for different powers.

2.3 Load Voltage When Matched

After tuning the rectifier to the matching block of antenna, the load voltage or output voltage of the matching block of antenna is calculated via the following equation[3]. The load voltage is the input voltage of the rectifier circuit.

$$|V_L| = \sqrt{2P_{av}R_S}\sqrt{1+Q^2} \tag{2.4}$$

This equation shows that increasing Q boosts the output voltage. In this equation, P_{av} is the average voltage received by the antenna and R_s is the series resistance of the antenna.

For $R_s = 10$ and quality factor from 0 to 70, the load voltage is drawn in Figure 2.6. Using this graph, it can be concluded that load voltage of the matching block is dependent on quality factor.

2.4 Comparison with Previous Works

The proposed system differs from other works such as the ones discussed in [10] and [18] by offering simpler tuning system, designed for 2.4GHz WiFi frequency, and with limited power consumption in mind.

For the comparison, three parameters which show important differences between all works are put in the table 2.1.

Y. Lim, et al [4] uses an analog circuit to control. They use 3 different blocks and 5 components. The control circuit controls an array of capacitor. The sensing is done by the measuring current. The search for frequency used a binary algorithm. It can be used for any number of antennas.

K. Buisman, et al. [5] utilizes an analog circuit which consists of 10 analog passive components. The circuit controls a varactor by voltage sensing at

Table 2.1: Comparison table of different designs related to this thesis.

Work	Operating voltage of control loop	Control loop voltage polarity	Control system dependency to frequency
This work	< 2 V	unipolar	Independent
Y. Lim, et al.	Independent	unipolar	Independent
K. Buisman, et al.	< 18 V	unipolar	2 GHz
Q. Gu, et al.	—	unipolar	100 MHz - 600 MHz
C. Chanlo, et al.	30-60 V	bipolar	900 MHz

2 GHz. The system is made in such a way that it is independent of any number of antennas and uses a linear search method.

Q. Gu, et al. [6] uses a mixed-signal system with 6 blocks to control multiple varactors. The measurement is done by the impedance measurement.

C. Chanlo, et al. [7] also uses a mixed-signal which contains 7 blocks and 2 components to control an array of capacitors. The sensing is done by phase detection (current and voltage sensing).

2.5 Potential Energy of RF Signals

RF Energy harvesters can harvest and transfer the ambient RF signal to an useful energy to be stored and consumed. Since there is potential energy in ambient RF signals, it is useful to find the relation between RF signals and potential energy. The RF signal power gives us an insight how much energy it is possible to receive. Then, the comparison between the receiving energy and energy consumption of the system will show how much efficient would be the automatic tuning of the rectenna. For this comparison, we first find the receiving power. In the chapter 4 and 5, we find the power consumption of automatic tuning system and then compare the receiving energy of harvester and consuming energy of tuning system.

Using the relation $P = 1mW.10^{\frac{x}{10}}$ [19] in which P is the power in *miliwatt* and x is the RF signal strength in *dBm*, we can find and show the possible harvesting energy when converted and stored. This relation shows the RF energy in the environment when there is no loss in RF to DC conversion. In other words, the result from the relation is the maximum energy that is

possible to store.

The minimum power that we can harvest is -30 dBm and the maximum is -20 dBm (due to saturation effect of rectifier). The potential power for 1 second of -30 dBm is 1e-06 *joule per second* which is the unit of *power* (0.1995 uJ/s). On the other hand, -20 dBm gives 10e-05 J/s (= 10 uJ/s) of power. Since the system might start in a random environment (with random RF signals), the matching network can not be matched for all environments. This means that we will have high 'Mismatch Factor' (MMF). The logarithmic nature of (RF) power conversion to energy makes a non-linear relation between different input power steps and energy.

Also, our RF measurements (which will be presented in the next chapter) prove the potential energy in RF ambient signals. The measurement result shows that the -22.87 dBm RF signal power gives about 5.1642e-06 J/s (= 5.1642 uJ/s). Another measurement shows that by receiving -25.85 dBm, the potential energy is 2.5996e-06 J/s (= 2.6 uJ/s). This shows that if we miss the RF power in ambient signal even for 3 dBm (25.85-22.87) due to mismatch of the harvester to the ambient signal, we will have almost half less collected energy (5.1642/2.5996 = 2).

In the next chapter, we will show the above discussion using real measurements. We will discuss about different measurements and also the potential energy of RF signals using measurements.

Chapter 3

GSM and WiFi Signal Measurements

Before going into design steps, we need to measure the environment that we want to harvest energy from. This chapter first introduces the tools and instruments for measurements. Then, it presents measurement results in tables and discusses the relevance of measurement results with designing the automatic matching system.

3.1 RF Measurement Tools

First, we start with RF (WiFi & GSM) measurements by utilizing a *spectrum analyzer*. The spectrum analyzer is handheld *Rohde & Schwarz Rider FPH* series with frequency range of 5 KHz to 4 GHz, resolution of 1 Hz, sweep time of 1 ms to 1000 s, and input impedance of 50 Ω [20]. This machine is able to detect and record RF signals in two different modes of *frequency mode* or *zero span mode* (with a *center frequency*). Also, an antenna from *Omnilog* is used to receive RF frequencies with omni-directional design and frequency range from 300 MHz to 8 GHz [21]. The used antenna type is *OminLOG 30800*.

In the next part, we present the findings and gathered information.

3.2 Measured RF Frequencies

RF measurement is the input requirements of our system design. The harvester system is aimed to harvest from GSM and WiFi frequencies. In order to know how it is possible to harvest energy from these signals, it is required to study their pattern and behavior. In this thesis, we study and do measurements on both WiFi and four GSM bands, i.e, *GSM850*, *GSM900*, *GSM1800*, and *GSM1900*. However, we focus mostly on designing the system based on WiFi frequencies. Then, we prove in the next chapters that

it is possible to utilize the designed system in any other bands and also in GSM frequencies.

3.2.1 RF Bands Measurement

Using the spectrum analyzer, it is possible to have a sample of frequencies from 0 GHz to 3 GHz at only one screen. This overview helps on deciding to work on the frequencies with enough potentials for tuning and harvesting energy. A research also has been done before in [22]. This study worked on measuring 270 locations in London. The captured data shows that almost half of these locations have enough energy to harvest. The result of this research is available in [23].

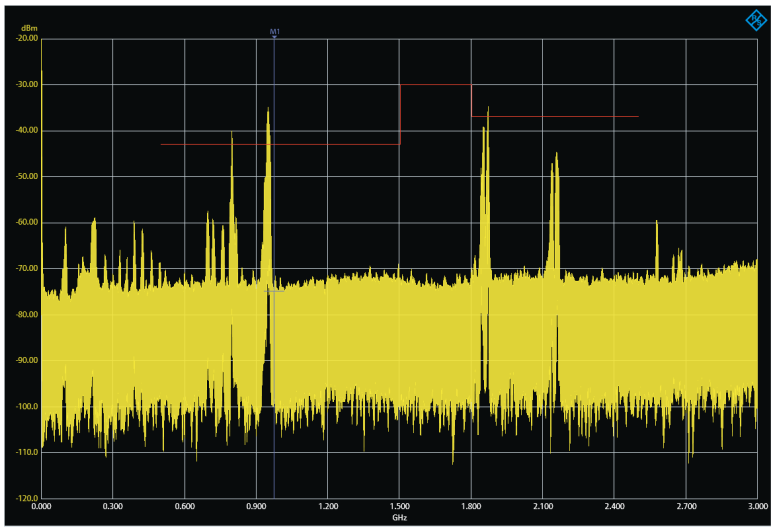


Figure 3.1: RF full range frequency, frequency mode.

Some explanations help to understand the screenshot better. First, a *red line* shows the *power threshold* by which frequencies beyond that are strong enough to trig the harvester. The threshold line is not totally flat due to different responses of the antenna to different frequencies. In fact, we can see three different regions with different threshold levels. First one is from 0.5 GHz to 1.5 GHz, second region is from 1.5 GHz to 1.8 GHz, and 1.8 GHz to 2.5 GHz is the third one. This non-flat compensation information is given by *Aaronia* which is the manufacturer of antenna. The antenna has better response from 1.5 GHz to 1.8 GHz. This means that to see the equal effects for all frequencies, this range of frequency should be compensated by increasing the threshold. Passing the threshold line in this range has the same effect on harvester when other frequencies outside of the range pass the line. This is also true for frequencies from 0.5 GHz to 1.5 GHz and 1.8 GHz to 2.5 GHz.

We will continue studying these frequencies in the following sections in more details by measuring first WiFi band and later GSM.

3.2.2 WiFi Band Measurements

This measurement is done only indoor, since WiFi signals can not be received with enough power outside. The signal is very weak (below the threshold to trigger the harvester) even if we are close to a WiFi router due to the interference of objects such as walls and metals used in buildings. Therefore, we only focused on doing measurements inside buildings and offices for WiFi measurements. It should be noted that indoor measurement is not only for WiFi, but it has been done for GSM bands as well.

Since the measurement environment has direct effect on measurement, we need to specify the conditions that the measurements are done. The location is indoor (office at Yes!Delft building), distance from routers is 3 m, and height of the spectrum analyzer from the earth is 1 m. The routers under measurement were able to emit maximum 0.1 W of power with a horizontal wireless router antenna.

The above-mentioned measurement setup gives the following results. The screenshots are taken by *R&S InstrumentView* [21] software.

3.2.3 Recorded Results of WiFi Measurement

Figure 3.2 shows the recorded frequency of WiFi channel on zero span mode. The frequency is set on 2.4533 GHz. This recorded information shows very well that the emitted power from WiFi router has enough potential to trigger harvester.

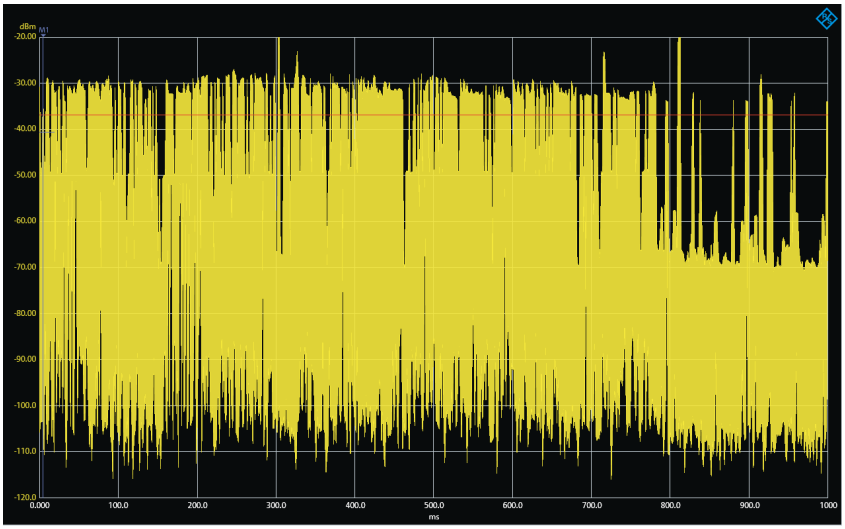


Figure 3.2: WiFi frequency, zero span mode, center frequency: 2.4533 GHz.

The table 3.1 puts all the measurement data together. Three different measurements are done in the same location. The first measurement is out of 500 recorded data sets. The measurements are done with 3 meters distance to WiFi router. During the first measurement, 3 to 5 people were present in the measurement location. For the second and third measurements, 6 to 8 people were present on average. It should be mentioned that for some measurements due to presence of both 2.4 G and 5 G WiFi routers, it was not possible to rely on those results since the measurement machine was able to measure up to maximum 3 GHz.

The power row in the table is the received power for the three different measurements in dBm. Each measurement gives the energy in *Joule* mentioned in the second row. For instance, the second measurement with -22.87 dBm signal strength gives 5.1642 μJ of energy. The conversion from dBm to Joule is done with 100 % efficiency. In the hardware of autonomous sensor, the matching network and the rectifier blocks are in between from the antenna to storage capacitor. This means that the efficiency of conversion is dependent on the efficiency of these two blocks. The more efficiency of the blocks, the higher energy we can convert from dBm to Joule.

Measurement	1	2	3
power (dBm)	-27.5010	-22.8700	-25.8510
Energy (J)	1.7779e-06	5.1642e-06	2.5996e-06
High resolution (peak duration)	1.4089e-04	5.4350e-04	4.0103e-04
Low resolution (number of peaks/s)	24.5000	32.4700	90.4283
Average power per second (W)	6.1369e-09	9.1134e-08	9.4272e-08

Table 3.1: Recorded information of WiFi measurement.

The spectrum analyzer is able to measure in two different recording resolutions: *High resolution* and *Low resolution*. In the high resolution mode, the machine makes a 10ms window to record each data set. Using this mode, the duration of each peak is recordable. Then in the low resolution mode, each data set is recorded for 1s which is possible to record and count the number of peaks. Table 3.1 contains both modes. For the second measurement and in high resolution mode, *average peak duration* is 543.50 us. In the same measurement and for low resolution mode, *average number of peaks per second* is 32.47 s. Putting all the data together, it is possible to collect 91.13 nW of power per second.

In addition, the measurements show the maximum peak of -22 dBm which occurs 32 times per second. Also, for -27.5 dBm and 25.85 dBm, the peaks of power occur 24.5 and 90.4 times, respectively.

3.2.4 GSM Band Measurements

GSM measurement starts with finidng *cell towers*. Nearest cell towers can be found using many applications on smart phones such as *Network Cell Info Lite* [24] application. In addition, there are websites such as [25] and [26] which locate updated list of cell towers on the map.

GSM range is divided in different frequency bands. The bands an their frequencies are summarized in a table called ARFCN [27]. ARFCN is *Absolute radio-frequency channel number* which helps to find GSM channel frequencies. This table contains each band with the frequencies. Each frequency has *uplink* and *downlink* dedicated frequency. Uplink is the frequency in which a cellphone sends data to its cell tower. Downlink frequency is also the frequency where cell phone receives data from the tower. Uplink and downlink frequencies are represented by F_{UL} and F_{DL}, respectively. These two frequencies are used to set the spectrum analyzer on a proper frequency for GSM measurement to avoid wasting time to look for right frequencies.

The ARFCN table summarizes different GSM bands with their different frequencies. For eaxample, choosing ARFCN = 1022 gives F_{UL} = 889.6 MHz and $F_{DL} = F_{UL}+45 = 934.6$ MHz for *uplink* and *downlink* frequencies, respectively.

Table 3.2: GSM frequency bands table extracted from ARFCN.

	GSM850	GSM900	GSM1800	GSM1900
Uplink	824 - 849 MHz	870.4 - 915 MHz	1710 - 1785 MHz	1850 - 1910 MHz
Downlink	869 - 894 MHz	915.4 - 960 MHz	1805 - 1880 MHz	1930 - 1990 MHz

3.2.5 Recorded Results of GSM Measurement

For the GSM measurement, it is required to mention the measurement condition like the one we did for WiFi measurement. Each measurement needs to have specified *position*, *orientation*, *Cell ID*, *distance from the tower* and *height of the spectrum analyzer from the earth*. Table 3.3 presents the GSM measurement. For this measurement, cell id is '427961'. The measuring location is with orientation of 150° SE, distance of 150 m from the tower, and distance of 30 cm from the earth. Measurements with different cell towers proved that the strength of the received signal depends on the direction and distance of the receiver antenna to cell towers. This means that telecommunication operator company did not show any effect on measurement of the signal strength. In [3], the RF power of 900 MHz GSM station is between 0.01 to 0.1 uW/cm^2 for -30 dBm to -20 dBm.

Table 3.3 presents all the data taken into account for GSM measurement.

Table 3.3: GSM measurement table.

Number	Frequency	0 span (1ms)	0 span (10ms)	Time length of measurement (mins)
1	700 MHz-894 MHz	—	—	2
2	Full range	—	—	2
3	GSM900 Downlink	—	—	2
4	GSM1800 Downlink	—	—	2
5	—	—	947 MHz	5
6	—	947 MHz	—	5
7	—	—	954 MHz	2
8	—	954 MHz	—	2
9	1.8 GHz-2 GHz	—	—	1
10	1.84 GHz-1.88 GHz	—	—	1
11	—	—	1.86 GHz	2
12	—	1.86 GHz	—	2

As it was mentioned before, this thesis mostly focuses on WiFi signals. However, to prove the point that it is crucial to tune harvester antenna on the most powerful frequencies, GSM measurement is also done. Figure 3.3 depicts a sample of measured GSM frequency. Frequency column in table 3.3 shows the range of frequency where the spectrum analyzer is set. Span column means that the spectrum analyzer is set on frequency mode with a specific frequency. Span mode has two different timings of 1 ms and 10 ms. 1 ms span shows the center frequency with more details. On the other hand, 10 ms-span mode gives a better overall view about the measured frequency.

The fifth column which is time length shows the time dedicated for each measurement. This time length is concluded after several measurements in different days and locations for hours. It was concluded that each measurement for minutes gives a precise result.

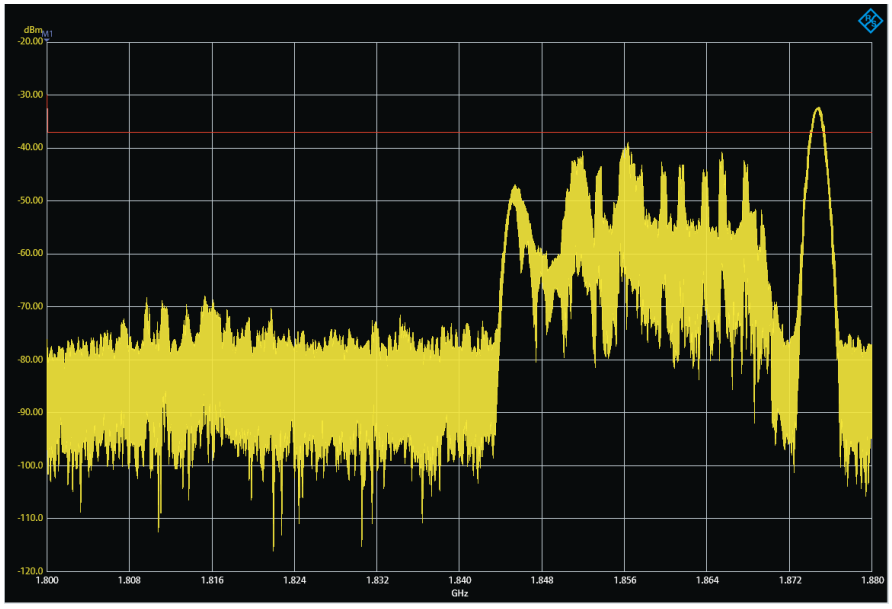


Figure 3.3: GSM1800 band, frequency mode, center frequency: 1.84 GHz.

Chapter 4

System Level Design, Modeling, and Simulation

RF measurements are done to understand the behavior of RF signals. These signals are considered as the input data which we want to harvest energy from. In this chapter, we first talk about an algorithm for tuning the antenna. Then, we continue with the implementation. The implementation step contains *analog* and *digital* blocks which we analyze very briefly. The design and simulation are done at *system level* by using *simulink* of *MATLAB*. For designing each block, first its behavior is described. Then, the way and the components to build up each block is discussed. Some of the blocks are modeled using MATLAB. The rest are modeled using *hardware* components. The reason to use MATLAB was the flexibility to change and modify the behavior of each block easier and faster. In some cases, hardware is used for modeling since no flexibility was required for modification.

4.1 Introducing the Algorithm

Algorithm 1 presents the desired algorithm. The algorithm starts with assigning *ch_num* parameter which represents *channel number* for scanning. It enters a *while loop* up to 14 iterations for 14 channels of WiFi. At the beginning of the loop, first *ch_num* channel number which is one is given to the channel controller (*ch_controller*). This controller saves the channel number and passes the channel number to a *Sample and hold* block. This block takes a sample and stores the value. Then, the channel controller increases the channel number by 1. The saved channel number goes to sample and hold to sample the value of the next channel. Before going to the next channel, the algorithm *compares* the two first channel values *(mem_ch)* and *(mem_ch + 1)*. Depending on the value of each channel, the greater one is chosen and the less one gets blocked behind the first step (line 9 of algorithm). The chosen channel is pushed to to a memory called

Algorithm 1 Adaptive tuning algorithm.

```
1:  procedure ALGORITHM(ch_num) ▷ The selection between 14 channels
2:      ch_num ← 1
3:      while ch_num ≤ 14 do                ▷ We have 14 channels to scan
4:          mem_ch_num ← ch_num
5:          Sample_ hold mem_ch
6:          ch_num ← ch_num + 1
7:          mem_ch_num ← ch_num
8:          Sample_ hold mem_ch
9:          Compare mem_ch & mem_ch + 1
10:         if mem_ch ≤ mem_ch + 1 then
11:             mem_ch_select ← ch_num + 1
12:         else
13:             mem_ch_select ← ch_num
14:     dac_val ← mem_ch_select
15:     return dac_val          ▷ The select channel has DAC analog value
```

mem_ch_select. This flow goes on until 14 channels. At the end, the best candidate is chosen as the one with highest power potential. The algorithm returns a proper value to set a varactor for the best channel.

4.2 Algorithm Implementation

We discussed in the last section about an algorithm which is designed to search for the frequency with highest power. The algorithm can be implemented in hardware directly or written as a software on a general purpose hardware such as MCU. Since this system is going to be embedded with other parts of a sensor, we tried to design the system with blocks for chip implementation. Therefore, different hardware analog and digital blocks are used to design the whole tuning algorithm on hardware.

Figure 4.1 depicts the possible implementation of the algorithm with hardware blocks. The blocks in the box with dashed line are the parts which belong to the algorithm. The blocks connected to input of the system are represented here to give an overview of whole system and help explaining the system work flow better.

At the beginning, the antenna of harvester is placed, which absorbs the radiated RF signals from RF transmitters. The antenna is wideband and able to absorb GSM and WiFi frequency bands. It is an advantage that we can absorb a wide range of frequencies. On the other hand, it has a drawback that the absorbed energy is not high enough with wide band tuned antenna as it was discussed in Chapter 2. The solution to this issue is an on the fly tuning system which can match a block for all specific frequencies. This

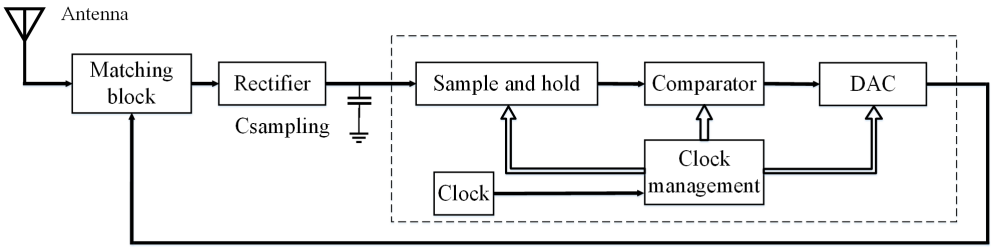


Figure 4.1: The whole matching system.

system is placed in the dashed line box which we will explain in detail.

The *matching block* tries to match itself with the rectifier block. Rectifier contains diode to rectify and make a DC voltage out of the received RF signals. The output of this block goes to a *DC-DC converter* (not represented here) for voltage boosting. At the same node (output of rectifier), the first sample and hold block is connected.

First, the channel controller sets the the channel number on 1. A block such as a DAC translates the the received value from the controller to a voltage to set the varactor. At this time, the rectifier block matches fully with the matching block of antenna. Matching helps to deliver the maximum voltage from the received RF signal to the rectifier and also maximum output DC voltage. The fully transferred RF signal to DC signal goes to a sample and hold block. Sample and hold circuit is able to measure the generated analog value of rectifier output. The first block holds this value until all 14 channels are sampled and stored. As it was described in the algorithm section, the controller increases the channel number and gives the value to be translated for varactor. The rectified voltage of the second channel is measured and stored in another sample and hold block. These two units of sample and hold are connected to a comparator. The comparator compares the two measured and stored value of sample and hold units. The channel with greater power can get permission to go the next level of comparison. The one with less power gets blocked before the sample and hold unit and stays there without further movement in the flow. The last kept channel is the strongest candidate which have had permission to go to all next levels during the comparison flow.

After finding the best candidate, a digital to analog conversion by a *linear amplifier* or a *multiplier* block converts the related value of the best channel to an analog value for tuning. This analog value is related to the strongest channel to tune the rectifier to the matching block.

Matching network is the first and last block at the same time. The control voltage is fedback from the converter block to the matching block. Matching block is tuned via *varactor*. Each block will be described in the coming sections.

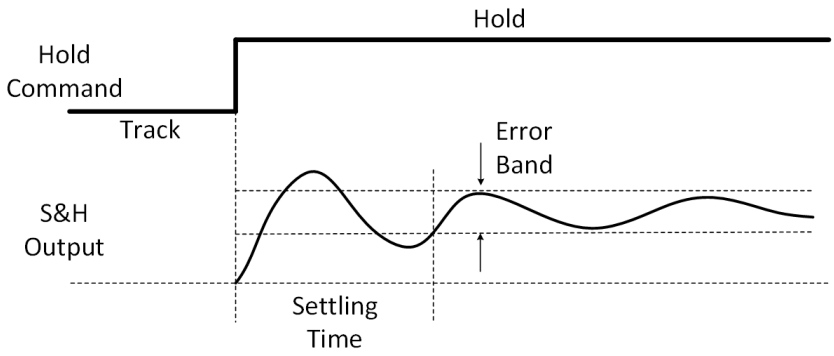


Figure 4.2: Sample and hold circuit timings.

4.3 Sample and Hold

In this design, a *sample and hold* circuit is used to read the input value and hold it. After measuring each channel value, this circuit reads the related voltage of the channel. Then, it works like a memory and holds the value for comparison with the next channel.

A work [28] offers a sample and hold circuit with 1.4 pW average power consumption. For a sample and hold circuit, important specifications should be considered to have the correct performance in our design.

The output time reading of sample and hold should be longer than the *settling time*. Since each channel has its own sample and hold block, the clock speed can not be faster than a limit. This limitation is formulated as:

Settling time is actually the charging time of the input capacitor of sample and hold circuit. Settling time is sometimes called *acquisition time* or tAC.

The other important parameter for timing is *aperture time* or tAP. Due to propagation delay between the sample and hold controller and the switch, it takes a short time for sample and hold circuit to stop following input voltage.

4.3.1 ADC

Not only for modeling, but also for implementation of the system, SAR algorithm is chosen. *Successive approximation* (SAR) is a method to convert analog values to digital via a binary search. This method offers low cost, simple operation, and more importantly, low power operation [29]. Another advantage with this type of ADC is flexibility. SAR can be cut for any number of resolution without circuit modifications. The less number of bits by cutting means the less energy consumption. Works of [30] and [31] also show that this type of ADC is a good choice with this application. SAR is chosen when energy consumption is the most important factor and resolution

and speed are in the second priority. Other types of ADCs are pipe-lined and sigma-delta converters. These ADCs are used for high performance systems rather than low power systems.

The trade-off design for ADC is between current consumption and speed. The rule is the least current while the highest speed. Also, there is a relation between conversion time and energy consumption. The less conversion time means the less energy consumption [30].

First, we start with ADC. After specifying the ADC, we can determine the parameters of the rest. ADC parameters to be determined are energy per sample, voltage, resolution, number of blocks (dependent on the type of ADC), speed, conversion time, die area, and flexibility. A research [31] suggests that for battery-less sensor designs, energy consumption of ADC should be less than 1nJ for 8-bit sampling at 1 V of power supply.

Since we want to measure the peaks of voltage, we need to find these limits. Using the discussion in Section 2.5, the minimum detectable power is determined by rectifier (the diode) which is -30 dBm or 1 uW. This means that receiving power less than -30 dBm will not be able to trigger the rectifier. On the other hand, the maximum acceptable power (before saturating the rectifier) is determined by input RF source which is -20 dBm or 10 uW. In real cases, input RF source is a WiFi router. We specify these two minimum and maximum input powers by P_{min} and P_{max}. In other words, -30 dBm is represented by P_{min} and -20 dBm is represented by P_{max} in this thesis.

We need to translate these two boundaries of power to voltage. These boundaries give the specification for ADC design. To do so, we need to find the conversion formula (relation) and efficiency of the rectifier. By running RF simulation of the modeled rectifier on ADS simulator, we see that the output voltage varies from 40 mv to 500 mv for -30 dBm to 20 dBm, respectively.

The input behavior of the ADC is depicted in Figure 4.3. This figure shows the charging behavior of ADC. The figure is divided in three different regions. The first region shows the time before changing to a channel with more potential. The voltage 40 mV is the minimum possible output of the rectifier. When the system switches to a channel with higher power at time a, the input of ADC can not sense the new input immediately. This delay is due to charging time of *sample & hold* capacitor of ADC. This means that after switching the channels, the input capacitor of ADC needs to be charged/discharged for new measurements. This time can be seen between two t_{start} and t_{end} time points. The less input capacitance of ADC makes it possible to switch channels faster. This time period is shown in region 2. The slope between points t_{end} and t_{start} is the speed of charging. This is the boundary of switching speed. It is not possible to switch channels faster than this period since ADC needs time to charge and do the conversion. The region 2 contains two different charging slopes which one is linear and

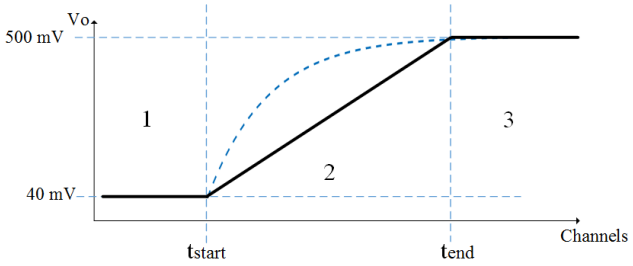


Figure 4.3: ADC input response to channel switching.

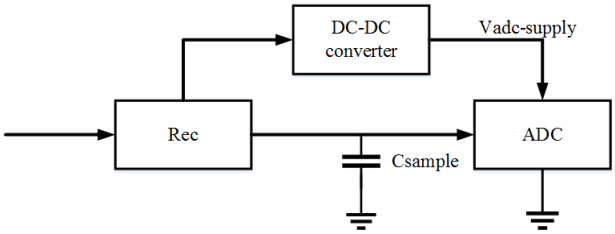


Figure 4.4: ADC voltage supply.

another one is a logarithmic slope. The linear slope is shown for better representation of charging the input capacitor. However, the logarithmic slope is the real charging curve. This curve is drawn by $V = V_b[1 - e^{-t}/RC]$ which is the charging equation of a capacitor. In this equation, V_b is the voltage which capacitor reaches while time goes to infinite. R and C are also values which determine the resistor connected to capacitor under charging. After passing this period, the input of ADC is on a stable state to read a valid input and convert it. The point b is the stable point of valid measurement. The region 3 shows the safe time to do the conversion. This also means that this region is the correct place to switch channels.

The voltage of ADC is supplied by the configuration give in Figure 4.4. Another reason to use SAR can be discussed here as well. Since pipe-lined and sigma-delta ADCs are designed for high-performance systems, they need more voltage than SAR. The ADC is supplied with the DC-DC converter.

ADC Resolution

To be able to find the resolution of ADC, we need to know the likely steps of input power. If we suppose the steps of input power is 1 dBm, then we need to translate it to voltage. This voltage determines the minimum resolution of ADC. Measuring for each 1 dBm step looks like quantization. Quantization is a process by which continuous (infinite set of elements) of input values are mapped to values which is countable (finite set of elements). Quantization decreases the *dynamic energy* consumption of the search algorithm, since it

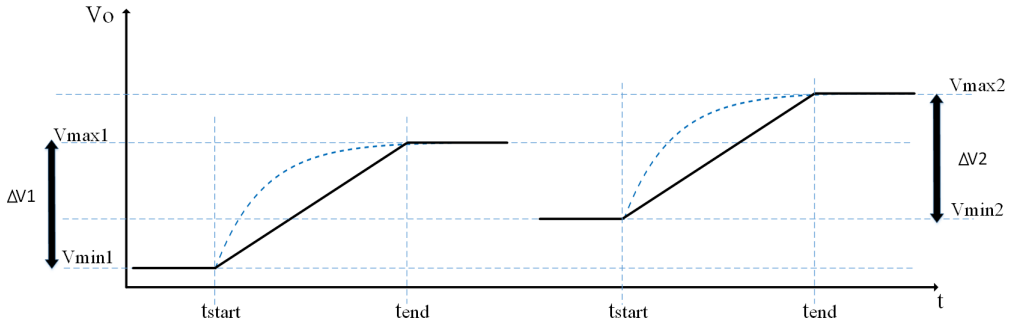


Figure 4.5: Two different measurement methods by sampling at t_{end} and by measuring voltage difference of start and end charging points.

limits the the number of switching action.

4.4 Signal Measurement Method

After charging the sampling capacitor, we need to consider the possible ways of measuring sampled voltage. There are two ways to do: one is measuring *slope* and the other one is *voltage peak*.

Charging slope of sampling capacitor is proportional to the start of sampling time by ADC (speed). We specify sampling voltage by V_{sample}, start time of sampling by t_{start}, and end time of sampling by t_{end}. If we find V_{sample} @ t_{start} and V_{sample} @ t_{end} then by using the relation $\Delta V_{sample} = V_{sample}@t_{end} - V_{sample}@t_{start}$ it is possible to find the voltage difference between start and end points. However, this voltage difference might misinterpret the measurements since there can be two channels with the same slope of charging but different peaks of voltage. Figure 4.5 shows this issue better. Both charging curves have the same charging slope ($\Delta V1 = \Delta V2$). However, V_{max1} and V_{max2} are not equal. This means that if we rely on slopes (voltage differences), we might have wrong conclusion.

The second way which is also used in this design is measuring peaks. If we do $V_{sample}@t_{end}$ of each channel, then we can compare V_{sample} of each channel and make decisions for selecting the channel based on this way of measurement.

4.5 Channel Switching Speed

4.5.1 ADC Speed

The lowest boundary is the sampling rate of the ADC. We can not sample faster than this limit. The sample & hold time which is around 10 μs is already calculated for a typical SAR. On the other hand, the other boundary

is the time length for the worst case charging time of *sampling capacitor*. Worst case charging time is the state when it takes the longest time to charge from the lowest available voltage (40 mV) to highest possible (500 mV).

4.5.2 Sampling Capacitor

Choosing sampling capacitor is affected by sample and hold block. Sampling capacitor needs to be chosen in relation with the sample & hold capacitor. Since input current is in nA to fA range (depending on the input impedance of the sample & hold), the S & H capacitor draws current and affects negatively on the measurement results. To avoid any wrong ADC voltage reading, we did a measurement using two capacitors. One of the capacitors represents sampling capacitor and the other one represents the input capacitance of ADC. It was concluded that when one of the capacitors is at least 10 times bigger than the other one, voltage reading of ADC will not be affected by the drawing current of smaller capacitor (input capacitance of ADC). This means that choosing capacitors with this values gives a right measurement. Therefore, sampling capacitor should be at least 10 times or bigger in order not to be affected by S & H capacitor.

$$C_{sampling} \geq 10.C_{S\&H} \tag{4.1}$$

It should be noted that designing the combination of the sampling capacitor, sample and hold block, and switching time is not a straightforward method. This is a trial and error procedure.

4.6 Delayed Clocking in Cold Start

When the system starts working for the first time to find the first channel, the clock should be longer since the sampling capacitor does not have any charge. This means that $C_{sampling}$ should start charging from zero volt. This cold start needs more time for the system to reach to a stable point.

To calculate this period, we take the worst case which is the highest output voltage of the rectifier. The highest possible voltage of rectifier is 500 mV which we represent it by $V_{\max_{rec}}$. We need to have output impedance of rectifier ($R_{out\ \mathrm{rec}}$) to calculate cold start time of $C_{sampling}$.

Constant charging time of the $C_{sampling}$ is found by $\tau = R_{out\_rec}\ .\ C_{sampling}$. A 5τ (because of the constant charging of a capacitor in a RC circuit) is needed for a full charge of capacitor, which can be represented by $5\tau_{sampling}$. Since the formula 4.1 shows that $C_{sampling}$ is 10 times bigger than $C_{S\&H}$, the speed bottleneck between $C_{sampling}$ and $C_{S\&H}$ is $C_{sampling}$.

Using the above discussion, this means that the period of the cold start clock should be longer than the other periods of clock. Therefore, the *cold start clock period* ($T_{coldstart}$) can be found by Equation 4.2:

$$T_{coldstart} \geq 5.\tau_{sampling} \tag{4.2}$$

After the first run of the system, we can define a *warm start* since the $C_{sampling}$ has a previous charge. This makes charging faster than the first run.

The first run of the tuning system can either be done by a *secondary battery* or the external RF power. However, if the tuning block is going to fed by an external RF signal, the harvester requires more energy than its normal operation time. Equation [3] shows the initial power:

$$P_{startup} = \frac{V_{rec,threshold}^2}{2\eta_A R_{rec,p}} \tag{4.3}$$

in which η_A is the receiving antenna radiation efficiency, $V_{rec,threshold}$ is the minimum voltage bias of the rectifier diode, and $R_{rec,R}$ is the equivalent parallel input resistance of the rectifier. For $R_{rec} = 1K\Omega$, $V_{rec,threshold} = 0.15V$, and $\eta_A = 0.8$, the initial energy to run the tuning system is 14.0625 uW which is equivalent to -18.52 dBm.

The receiving antenna radiation efficiency is calculated by Equation 4.4:

$$\eta_A = \frac{P_{rad}}{P_{accepted}} \tag{4.4}$$

where $P_{accepted}$ is the received power by the antenna and P_{rad} is the radiated power from the antenna.

We can also interpret this power when using a secondary battery. However, this power is calculated when the rectifier is in the path of current. Another design can be connecting this battery after the rectifier which means that even lower required power to initiate the system.

4.7 Clock/Block Management

The adaptive matching system is a *synchronous* or *clock-based* design. Clocking of the system is important to help us calculate timing and dynamic energy consumption of the design. Timing of the system can be divided into three different steps:

- Clock stabilization step;
- Calculation step;
- Result step;

When the system starts for the first time, a *clock stabilization* state is needed to have a stable clock. This step takes 1 cycle of clock. The next state is *calculation step*. During this step, all the channels are measured one

by one. Then, they are passed to the comparator. The best candidate is passed to the next cycle to be compared with another channel. Measuring and comparing instructions are done in one clock cycle at the same time. At the of 13 clocks of measuring and comparing, the best candidate comes out. The result is ready at the 15th clock cycle.

Figure 4.6: An overview of clock cycles of the system.

4.8 Pipelining

One advantage of the design is the *pipelining*. This increases the speed and efficiency of tuning by running more instructions in each clock cycle. The result is paying zero cycle for each channel and in conclusion fourteen clock cycles to read, measure, and find the best channel. Figure 4.7 signals the flow. It contains three different instructions run in one clock. *Instruction 1* sets varactor for the first channel. At the same clock, the received voltage from the output of rectifier is sampled and stored which is represented by *I2*. In the next clock, three instructions run. *I3* is the instruction for comparison of measured and held channel values. The output of this instruction is the best channel of clock one. This output is the input to the next clock. This flow goes on until all 14 channels are measured and compared. At the 15th clock, the best channel is the result of flow.

4.9 Instruction and Data Path

It is possible to divide the paths of connecting blocks in the system to two different paths of *instruction path* and *data path*. In the instruction path, the commands to run instructions move. Except clock and clock management block, we have 15 lines of instructions in the system. Another path is data path. Since the proposed system is a *mixed-signal system*, it consists of both analog and digital data. The system contains 14 lines of data which are from sample and hold block to the comparator. These lines contain all the measured values of channels. The rest of the data lines are analog lines.

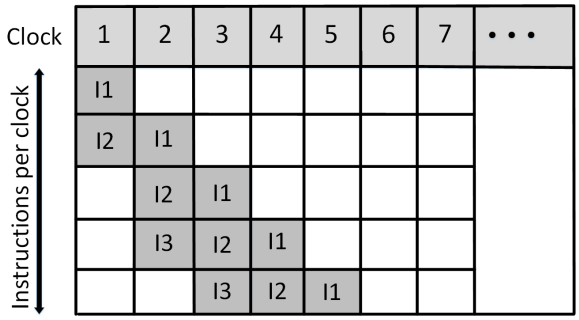


Figure 4.7: Pipelining in tuning system design. This Figure depicts this flow partially to save space since the rest of clocks are the same as clock two.

4.10 Tunable Devices

There are devices which can be used and tuned for RF systems. Thin-Film Barium Strontium Titante (BST), MEMS-based Switches and Varactors, Conventional semiconductor-based varactors, Semiconductor-based switches, and Modern Semiconductor-based varactors are all discussed in [32] as tunable components.

This study discusses and ranks the tunable components based on different possible parameters of RF systems. The factors considered are tuning range, loss (Q), capacitance density, control voltage, tuning speed, voltage handling, linearity, and reliability. Each method has some limitations and advantages. However, for our tuning block, we require two important features. First, it should be controlled with very low voltage from 0 to less than 2 V since we have very limited voltage in our system (sensor). Second, it should have ultra low leakage in the scale of nA to avoid energy loss as much as possible. However, it does not need to be very fast since the system does not need to jump in many different frequencies. Also, linearity of the tunable component is not important, since we can compensate any non-linearity using the proposed algorithm.

In the matching network, C_{match} and L_{match} have fixed values of 5 pF and 9 nH, respectively. The varactor range is from 2.2 pF to 50 pF. These values of capacitance and inductance are able to cover from 2.408 GHz to 2.485 GHz which are relevant frequencies of all 2.4 GHz WiFi channels.

Figure 4.9 shows the behavior of the varactor by capacitance (pF) versus *bias voltage* (V). A line is drawn in parallel to the behavior of the varactor on the left side of the curve. The line shows that for the bias voltage from 0 to almost 2 V, the capacitance change of varactor is linear with respect to its bias voltage. This is a great response since we only have limited voltage in our system. At the same time, the varactor response is linear to the available voltage. As this figure shows, ΔC_{tune} of 47.8 pF is required for all the channels to find the best one.

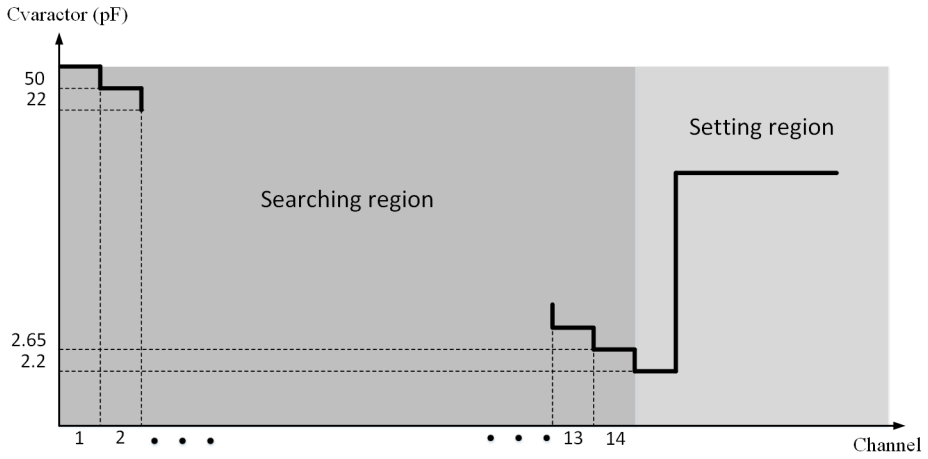


Figure 4.8: Varactor iterations to tune on the best channel. The rest of channels with their varactor values are presented by Table 4.1.

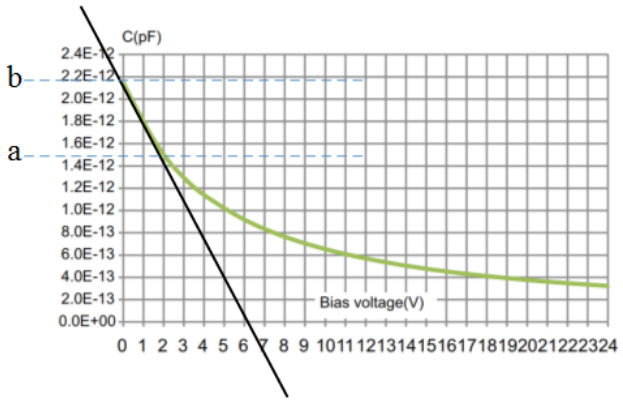


Figure 4.9: Varactor response.

This varactor is made by *Parascan* technology which is for tunable integrated capacitor. The figure 4.9 is extracted from datasheet of *STPTIC-15G2* which is a varactor component from STMicroelctronics [33].

To model this component, a line is modeled using $y = mx + b$ in which m is simply the slope of drawn line in parallel to varactor response for the range from 0 to 2 V.

The more details can be studied in [34].

The table 4.1 is calculated simply by finding the equal input impedance (Z_{in}) of the matching network. We can find input impedance of the matching network by $Z_{in} = Z_{Cmatch} \parallel Z_{Lmatch} + Z_{Rectifier} = Z_{Cmatch}(Z_{Lmatch} + Z_{Rectifier})/Z_{Cmatch} + Z_{Lmatch} + Z_{Rectifier}$. In this relation, Z_{Cmatch} is the input impedance of the matching capacitor, Z_{Lmatch} is the impedance of the inductor, and $Z_{Rectifier}$ is the input impedance of rectifier. All these

WiFi channel	1	2	3	4	5	6	7
center frequency (GHz)	2.412	2.417	2.422	2.427	2.432	2.437	2.442
Varactor value (pF)	50	22	13	9.7	7.5	6.2	5.3
WiFi channel	8	9	10	11	12	13	14
center frequency (GHz)	2.447	2.452	2.457	2.462	2.467	2.472	2.484
Varactor value	4.55	4	3.6	3.2	2.9	2.65	2.2

Table 4.1: Varactor value for each WiFi channel.

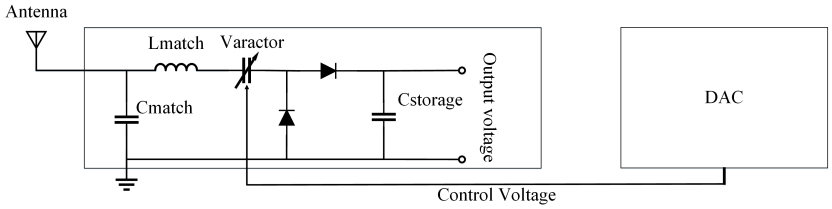


Figure 4.10: Feedback line from DAC to tune varactor.

elements are shown in Figure 4.10.

4.11 Drift of Tuned Channel

Drift is an undesired slow movement of set point to a random point. Drift can happen due to, for example, temperature change and aging components. This causes error in the output of system. In our design, the effect can tune the varactor to a wrong channel and then receiving less energy. To solve this problem, there are many approaches to do it at the circuit level. However, since we are designing in system level, we can solve this issue by running the algorithm as frequent as possible to make sure that the rectifier is tuned on the correct channel. This re-tuning step can put back the system to the proper channel.

4.12 Interfacing Digital to RF Section

After designing a digital/mixed signal system, it should be connected to the RF section. This connection is done via a trimmable capacitor. Trimming of t his capacitor changes the input capacitance of the rectifier which matches to matching block of antenna. Setting of varactor can be represented on *Smith chart*. Figure 4.11 shows the smith chart with odd channels of WiFi. For instance, *m1* represents channel 1 and *m3* represents channel 5.

By increasing WiFi channel number from 1 toward 14, the *markers* of smith chart move toward left on the *blue line* on the Smith chart. When a marker is placed on the middle point of Smith chart, it shows coefficient 1 which is multiplied to the input impedance of the rectifier. This point is the place where is the best point that matching block is matched to the input impedance of rectifier.

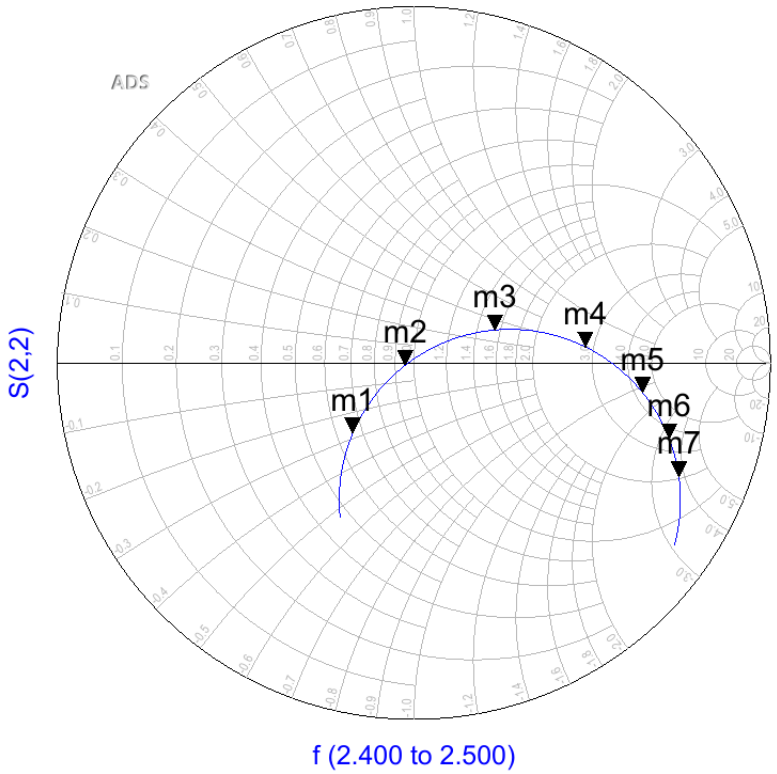


Figure 4.11: Odd WiFi channels marked on smith chart.

The movement between WiFi channels are not linear. This means that as the Table 4.1 states, the difference between capacitances for tuning is non-linear.

4.13 Effect of the Matching System

Matching boosts the harvester efficiency. Figure 4.12 depicts the effect of matching on efficiency. The parameter for comparison is the output voltage of rectifier. This figure shows the output voltage for -20dBm, -25dBm, and -30dBm of RF input power. The dark blue bar shows the voltage when the antenna is connected directly to rectifier and there is no matching circuit

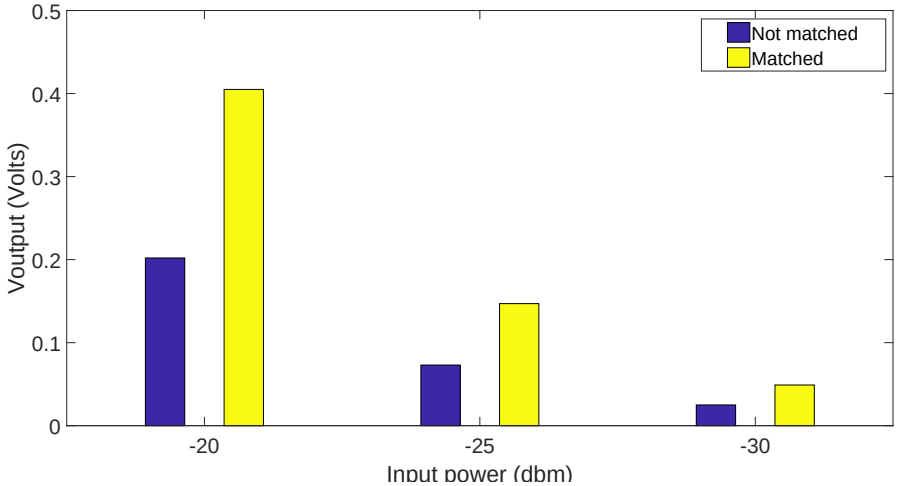


Figure 4.12: Output voltage of harvester with matched and unmatched cases.

between antenna and rectifier. The yellow bar shows the same when they are matched. It can be seen almost 50% of improvement in output voltage amplitude when antenna and rectifier are matched [16].

This result can also be used to prove the reason for matching that was presented in Chapter 2. In other words, this result shows improvement in efficiency while antenna and rectifier are matched.

The next section will present the simulated results of the system from simulink.

4.14 Simulation Results

This section presents the simulation results of the proposed system. Simulink of MATLAB is the software used to design, model, and simulate system. Each block is designed by coding via Simulink. For some components of our system, Simulink has already the blocks. For instance, pre-designed blocks are used to model sample and hold block. On the other hand, clock management block is modeled completely by writing Simulink codes. Modeling and testing of each block is done first separately independent of each other to check the performance and functionality of the blocks. Then, we started connecting each block starting from the input of the system to its output.

Figure 4.13 shows the control signals of the system. The first signal is the *clock* which is the trigger signal of the system. The second signal called *random signal* which is the random input of the system. This random generator models a WiFi source with all 14 channels. These channels are seen totally

random from the system point of view since WiFi channels are chosen by router manufacturers or users. Also, Figure4.14 depicts the output signal of the algorithm. The rest of signals and their blocks are described in detail in each section of this chapter.

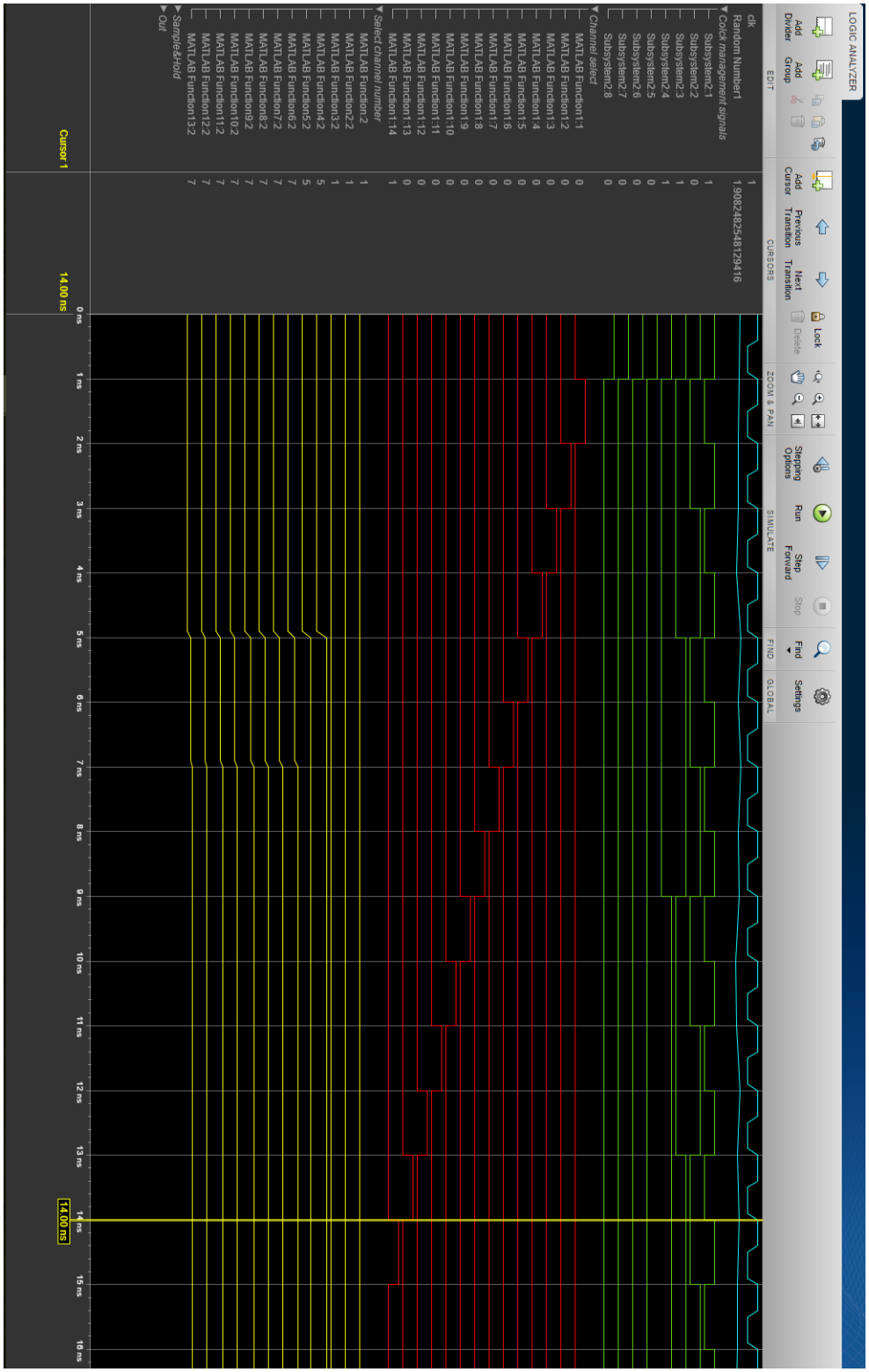


Figure 4.13: Simulated control signals of the designed system.

Figure 4.14: Simulated output signals of the designed system.

Chapter 5

Power Consumption Analysis

After designing the system, it is time to look at the energy consumption of the implemented algorithm. Since it is not possible to calculate the energy consumption from the system level design, it is required to look at the lower level of the system, which is a circuit level. Designing the thesis idea consists of both analog and digital blocks. Finding the energy consumption of digital blocks is more predictable than analog ones, since these digital circuits can be designed and fabricated by *standard cells* from *cadence* software which are pre-designed in the software. Standard cells are the cells which have known fabrication technology and geometry designs. This makes the energy and timing calculations more straightforward and predictable. It should be noted that we need to pay attention to the difference of energy and power during all the calculations in this thesis.

Our design is going to be implemented by *CMOS* transistors by digital chip designers in the future. For a CMOS-based circuit, *dynamic* power consumption, *static* power consumption, and *short circuit* power consumption are considered as three different sources of energy consumption. Each source needs to be taken into account to have an overall estimation of the power consumption. To be able to do so, we dive more into these three sources of consumption.

The whole energy consumption is the sum of all blocks in the system which is defined in 5.1 as:

$$E_{\text{total}} = Clock_{division_{\text{energy}}} + Clock_{management_{\text{energy}}} + Comparator_{energy} + DAC_{energy} + Multiplier_{energy} + Varactor_{energy} \tag{5.1}$$

5.1 Energy Consumption of Software-Based Models

The tuning system is modeled by both hardware and software in Simulink. Estimating the power consumption of the modeled blocks by hardware is done by circuit analysis. However, for the software-modeled blocks, we need to translate the their design from software to hardware to be able to predict their energy consumption. We tried to model the blocks by only decision control programming structure commands (like IF in C programming language), since it could make software-to-hardware translation easy for energy consumption calculation. Each IF consists of different input conditions which are give to AND logic gates. The *clock management* block is modeled by 15 IF each of which contains 8 AND inputs. Also, the *varactor setting* block is modeled by 14 lines of IFs with 14-input AND gates.

This translation now gives us a precise number to calculate the energy consumption of the software-modeled blocks. We will calculate their energy consumption in the next sections.

5.1.1 Dynamic Power Consumption

Dynamic power consumption is calculated by the sum of *transient power consumption* (P_T) and *capacitive load power consumption* (P_L). This energy is consumed when node capacitances charge in a circuit. This energy is formulated by $E = C_L V_{DD}^2$ when a transition happens from ground to V_{DD} while there is C_L a capacitive load.

Some solutions to minimize dynamic current consumption is offered. Minimizing supply voltage while the performance requirements are met, capacitances, transitions through layout, circuit, logic, architecture techniques, fan-out (the number of inputs that can be connected to a specified output). Some of these techniques are in system level and some are in circuit level. There is also another step which is implementation phase which can decrease power consumptions due to layout [35].

5.1.2 Transient Power Consumption

As the name offers, this current is consumed when the transistor switches from one state or logic to the other state. When switching happens, V_{DD} and GND of the power supply becomes short-circuit for a short amount of time. This happens since N-MOS and P-MOS switches are ON at the same time. Another reason for this current is charging and discharging of the internal capacitances of the transistor while it switches the states.

As we see, this current is consumed in a dynamic condition. Formulating this source of the consumption gives us $P_T = C_{PD} V_{DD}^2 f_I N_{SW}$ in which P_T is transient power consumption, V_{DD} is supply voltage, F_I is frequency of

the input signal, N_{SW} is number of bits which are being switched, and C_{PD} is dynamic power-dissipation capacitance [35].

To understand the charging and discharging capacitances easier, it is possible to model all those capacitances as one big capacitance. Then this modeled capacitor is the one which is between V_{DD} and GND of the supply [35].

5.1.3 Capacitive-Load Power Consumption

Not only does a circuit contain internal capacitances, but also external load capacitances should be taken into account for a correct power estimation. Like the internal capacitances, this capacitance is also dependent on the switching frequency formulated by $P_L = C_L V_{DD}^2 f_O N_{SW}$ in which P_L is capacitive-loaded power consumption, V_{DD} is power supply, f_O is output signal frequency, C_L external (load) capacitance, and N_{SW} is total number of outputs switching.

5.1.4 Total Dynamic Power Consumption

Putting all the mentioned relations for dynamic power consumption gives the relation $P_D = P_T + P_L = (C_{pd} \times f_I \times V_{cc}^2) + (C_L \times f_o \times V_{cc}^2)$.

5.1.5 Static Power Consumption

Static power consumption is sometimes also named as *steady state current* or *quiescent current*. Ideally, static power consumption of a CMOS device is zero. However, fabrication process of a CMOS transistor makes some parasitic diodes in a typical CMOS. This current called sub-threshold leakage current which flows in any transistor with a potential difference between its source and drain, even when the gate is turned off. This current depends on the source/drain potential and the source/channel potential. The root of static power consumption is leakage current of the reverse-biased modeled diodes between the substrate of the transistor and its diffused region. Leakage current is formulated by $I_{leakage} = i_s(e^{\frac{qv}{kT}} - 1)$ which i_s is reverse current of the diode when saturated, V is the voltage across the modeled diode, k is Boltzmann's constant ($1.38 \times 10^{-23} J/K$), q is electronic charge (1.602×10^{-19} C), and T is temperature. Since this design is going to be implemented on a chip directly, the calculated static current estimates the current very well. In case of using off-shelf components, this current can be extracted from the component data sheet, which has higher current due to the other needed circuitry in the device.

There are some solutions to static power consumption. This power can be minimized by decreasing the source/drain channel potential by reducing the supply voltage of the transistor. Also, the transistors which are not

needed can be powered down. This causes to have less leakage current from unnecessary circuits and transistors.

5.2 Total Power Dissipation

Putting both static power consumption (P_{static}) and dynamic power consumption ($P_{dynamic}$) gives the total power consumption is formulated as $P_{tot} = P_{static} + P_{dynamic}$. The ultimate goal for the low power design can be written as equation 5.2.

$$P_{Leakage} == P_{Dynamic} \tag{5.2}$$

5.3 Speed vs Power Consumption

As it was discussed in the previous section, all formulas show that power consumption has proportional relation with speed. However, one can infer that we can decrease the frequency as much as possible to shrink the power consumption. For instance, it is possible to put the frequency on 1 Hz and have lower power consumption than feeding the system with 10 Hz frequency. This trick might help to decrease the power consumption, but it takes more time for the system to run the algorithm and find the proper channel of WiFi or GSM channel. Taking more time means more energy since energy is product of power and used time. In addition, the later we tune the antenna on the proper frequency, the less energy we can collect since we miss some likely peaks of energy because of delayed tuning.

The above discussion means that we need to investigate on the relation of power consumption and speed of our system. First, we need to separate the *dependent* and *independent* sources of power consumption to speed. Our discussion in the previous sections show that static power consumption is independent of clocking frequency of the system. This means that increasing or decreasing the clocking frequency does not have any effect on static power consumption. However, there is only one relation between speed and static power consumption is that it is possible to run the algorithm as fast as possible and then turning all the blocks OFF by using external switches.

The above-mentioned calculations requires to find the following relations:

- First, we need to see what is minimum harvested power which can drive the harvester to collect energy. Supposing that we receive enough energy just over -30 dbm, we need to calculate the stored energy for time *t*. The faster we can tune, the less energy we lose. Fast tuning should be done until we do not consume more energy than the received power.

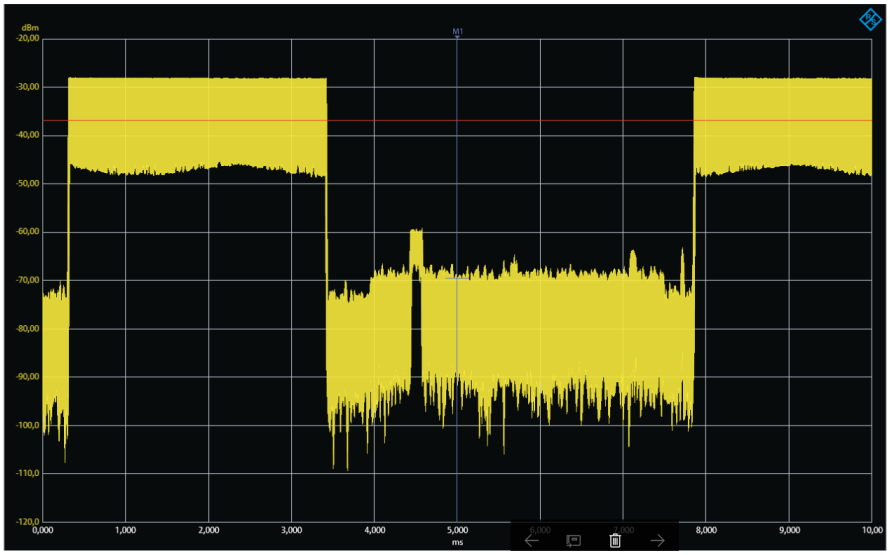


Figure 5.1: WiFi channel length in zero span mode.

- The second parameter is the current consumption vs speed in a digital circuit. Tuning speed can be increased as long as we do not consume too much of power.

Figure 5.1 depicts the frequency 2.4533 GHz channel length on zero span mode with 10 ms sweep time. Using this information, we can find the the minimum and maximum switching speed of our system. This figure shows the best measured time length that a frequency channel can pass the minimum limit for harvesting energy. Two important results can be concluded from this figure. First, it refers again to the discussion in chapter 2 to prove the idea of harvesting energy from RF signals. The second result which belongs to this chapter is that it is possible to find the system sampling speed using this figure.

The duty cycle of the figure 5.1 is 45 % for the average of best case. By referring back to the discussion in Chapter 2, we can have uJ/ S of energy.

To find the speed time, we can use the average number of peaks. Using the table, the received RF signals pass the threshold 32 time per second with 0.5 ms length for the average of worst case time length. This gives 16 ms above the minimum threshold during 1 second.

Using the above discussion, it can be concluded the minimum time length of 0.5 ms for the shortest and maximum of 3 ms for the longest time of RF signal. These two time limitations help calculating specifications of system such as clocking and speed of the system and sampling capacitor value. To avoid missing any peak, the average of worst case number of peaks should be taken into account which is 0.5 ms.

Now, after finding the maximum speed of the system and the value of

$C_{sampling}$, sample and hold speed can be found based on the mentioned parameters. As it was mentioned in Chapter 4, $C_{sampling} \geq 10C_{\text{S\&H}}$ must hold. In other words, the charging impedance of the $C_{sampling}$ is the output impedance of rectifier and discharging loop of it is made by the input impedance of the sample and hold block. This means that the input impedance of sample and hold must be at least 10 time greater than the output impedance of rectifier to avoid any undesired voltage fluctuations.

5.4 Timing of Sample and Hold

The next block after the $C_{sampling}$ is sample and hold. The clock frequency can not be faster than the *settling time* of the sample and hold capacitor, since the output of the each sampled channel should reach to a stable point. Therefore, the clock frequency f should be less than the *settling time*. In other words, the relation $T \geq settling\ time\ of\ sample\ and\ hold$ must hold. The output of the sample and hold blocks are connected to the comparator. This also gives another reasons to delay the clock more than settling time to avoid any wrong comparison.

5.5 Timing of Comparator

The comparator is designed in a *cascaded* or *water fall* way. The whole comparator block is made of 14 units of comparator in a cascaded hierarchy. Each unit can work with the speed of *f*. However, the design in this thesis requires the comparator block to follow the relation as below to give sensible output:

$$Comparator_{frequency} \leq \frac{1}{channel\ numbers} * clock\ frequency\ = \frac{1}{14} * clock\ frequency \tag{5.3}$$

Due to direct connection of the all comparator blocks, there should be a careful design to avoid any *race condition*. This totally depends on the designing of the comparator unit. If the paths in the unit are equal, it helps to avoid race condition.

5.6 Calculation of Energy Consumption of Different Blocks

In this section, we find energy consumption for the main building blocks so we can apply their energy consumption to the other blocks. Each digital block can be made of different combination of *Inverter*, *NOR*, and *NAND*

gates. Using *standard cells*, power consumption of each main block can be calculated beforehand. This means that power consumption of digital circuits are predictable.

5.6.1 Analog to Digital Converters

ADCs are one of the high energy-consuming blocks. This means that designing and choosing right and proper parameters for ADC is highly important. For the sensors with very limited amount of energy, the most crucial parameter on an ADC is its energy consumption. The energy consumption of an ADC is dependent on other factors such as *number of bits (N)*, *source voltage (V_{DD})* and an ADC design coefficient called F_{ADC}. Putting all these parameters together, it is possible to formulate the energy consumption as:

$$\begin{aligned} ADC_{consumption} = static\ consumption + dynamic\ consumption = \\ satic\ consumption + number\ of\ sampling \times energy\ per\ sample \end{aligned} \tag{5.4}$$

In our design, V_{DD} is 1 V. Also, F_{ADC} for the latest ADC designs is $5 \times 10^{13}/V.J$ [11] is extracted in *sampling rate* of 100 kHz, *sampling bit* of 8 bits, voltage supply of 1 V and at 25°C temperature [11].

Table 5.1 helps to specify both static and dynamic power consumption of ADC. Static power consumption is 70 pW for this ADC architecture [11]. Dynamic power consumption is calculated by multiplying *Number of sampling* by *Energy per sample*.

5.6.2 Clock Division

The next block is *Clock division*. In order to have precise timing and run each instruction in a proper time, a clock division is used. This block is made of registers which each register is made of D-FFs. Each D-FF in turn is made of logical gates. Dynamic energy consumption of a D-FF can be extracted from a previous work [11]. This consumption is calculated for two 0 and 1 states of D-FF for different *fan-outs*. For all 15 clocks to have the best channel, these D-FFs consume 1686 fJ or 1.686 pJ. In average, 105.375 fJ is consumed in each clock cycle.

5.6.3 Sample and Hold

Like the other blocks, the most important parameter for sample and hold block are power consumption and speed. Work [28] offers a low power sample and hold circuit with 1.09 nW power consumption.

Sample and hold takes samples from $C_{storing}$. The timing of sampling is defined by (V_L) and (V_H) which are the lowest and highest voltage of capacitor, respectively. The charging time of the $C_{sampling}$ is defined by $T_{sampling}$

which is dependent on RF power, the rectifier efficiency, the sampling capacitor, and the drawing current of sample and hold block [3]. Since sample and hold circuit is designed with high input impedance characteristic in mind, it draws low current and has small effect on charging of $C_{sampling}$. The maximum energy stored in $C_{sampling}$ is found by the following equation:

$$E_{average} = \frac{1}{2} C_{sampling}(V_H^2 - V_L^2) \tag{5.5}$$

Where V_L and V_H are output voltages of rectifier which are 40 mV and 500 mV, respectively.

5.6.4 Varactor

The varactor current consumption is 100 nA. The range of voltage is from 0 to 2 Volts. Therefore, these numbers give the information for power calculation of the varactor. Energy consumption of the varactor can be calculated easily by taking into account the current, voltage, and time length of the power from Figure 4.10.

5.6.5 Digital to Analog Converter

The next block is DAC to convert the selected and stored channel for tuning by varactor. A suitable and related DAC for our system is discussed in [36]. This DAC satisfies our system need because of two reasons. The first reason is that this DAC is designed with one reference voltage than two. Since the sensor has limited voltage, using one reference voltage is an advantage. Providing two reference voltages in such a limited system adds unnecessary complexity and increases power consumption. The second reason is ultra low energy consumption of the DAC. The consumption is calculated as[36]:

$$E_{avg} = [0.25 + 3 \times \sum_{i=1}^{N-3} (2^{N-i-5})] C V_{ref}^2 \tag{5.6}$$

where N is the number of bits, C is the amount of capacitance in the DAC circuit, and V_{ref} is the voltage reference of the DAC. In our design, we had to use two DACs. One which is 14 bits is used to switch the channels for the first search time. The second DAC is 4 bits and used to set the varactor after finding the best channel. Using the relation 5.6, we find the energy consumption of both DACs. Having $V_{ref} = 1V$, $C = 100nf$, we have N = 14 and N = 4. For the 4-bit DAC, the energy consumption is 18.75 nJ. Also, for N = 14, the energy consumption is 153.55 nJ.

Table 5.1: Overview of energy consumption of each block.

Block	Static	Dynamic
ADC	70 pW	31 pJ
Sample and Hold	1.09 nW	—
Comparator	—	6.17 pJ
DAC	—	18.75 nJ (4-bit)
	—	153.55 nJ (14-bit)
Clock Division	—	1.686 pJ

5.7 Summarizing Energy Consumption

After calculating the energy consumption of all blocks, we need to put the elements of energy consumption together to find the overall consumption.

Table 5.1 shows all the findings about energy consumption of blocks.

The propoesed comparator is done at work [37]. The advantage with this design is that it turns off automatically after each comparison. By this means, it is possible to cut the static power consumption of this block. Since the static current consumption in autonomous sensors is the key source of power consumption, using [37] helps to decrease the total power consumption. The delay for this comparator at frequency 166.6 KHz is 5.6 uS.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis designed a control system to match the antenna impedance for RF energy harvesting IoT sensors.

It was shown in Chapter 1 that advent of low power components from one side and appearing sources of RF like WiFi routers and GSM cell towers from the other side are shaping a new path to supply IoT sensors.

By referring to a general architecture of an energy harvesting sensor powered by RF signals in Chapter 2, we concluded that we need to supply energy for three fundamental blocks of the sensor. Using the relation 2.1, we found out that there is a relation between quality factor and efficiency of energy harvesting rectifier. To simplify the relation, a parameter called 'MMF' was defined. This parameter showed that it is related to the input impedance of rectifier and impedance of antenna. After drawing this relation for different qualify factors, we saw that increasing MMF decreases efficiency of matching network. MMF more than 30 can decrease efficiency down to even 10 %. Also, a research in Chapter 2 helped us make a table to find and define proper parameters of our matching system. The comparison in this table showed us that we need to design a system with low unipolar operating voltage (less than 2 V) with the ability to cover both WiFi and GSM frequencies.

Next, indoor and outdoor RF measurements are done to see if these signals are able to deliver our minimum required energy to trigger and harvest energy. Table 3.1 summarized all the findings and showed the capability of the RF bands for harvesting. Not only from power point of view, but also timing and duty cycle of signals were needed to design our matching system. We found minimum period of 0.5 μs and maximum of 3 s for these RF sources.

Chapter 4 used the input data from timing specifications of Chapter 3 and summarized parameters of Table 2.1 in Chapter 2. First, we designed the required hardware in Figure 4.1 for the Algorithm 1. The required hardware for this algorithm needs five blocks.

In the last chapter, a power consumption study is carried out to find the efficiency of our designed system in this thesis. To do so, we divided power consumption of the system into two different sources of dynamic and static power consumption. Among all blocks, ADC and Sample and Hold blocks have 1.097 nW of static power consumption together. Then, dynamic power consumption is calculated which is 38.856 pJ for three blocks of ADC, comparator, and clock division block. In addition, dynamic power consumption of DAC is 18.75 nJ for 4-bit and 153.55 nJ for 14-bit configuration.

6.2 Future Work

For the future work, DAC can be removed from the system and comparator can be connected directly to bank of capacitors. In this case, it is possible to save more die ares on the future chip where this thesis design is going to be implemented. However, the weights of capacitor bank should be calculated based on the proper frequencies.

To make the system more efficient, it is possible to design it in such a way that it starts first scanning with channels 1, 6, and 11. Then, the system can search for the other channels.

About the varactor values, it is possible to find its values more precisely. The values mentioned in this report is simulated for -22 dBm power. It is possible to find the values for the whole possible range from -30 dBm to -20 dBm.

It was explained that autonomous sensors are in sleep mode most of the time. This means that the bottleneck of power consumption is in inactive mode than active mode. The energy consumption in inactive mode is due to the leakage current of blocks and circuits. This makes the idea of designing switches for the blocks quite efficient since unnecessary circuits can be turned off in inactive times. For this type of switch, it should be kept in mind that the switch should be able to deliver the required current of the block by having much less leakage current than the block.

Bibliography

[1] A. N. Parks, A. P. Sample, Y. Zhao, and J. R. Smith. A wireless sensing platform utilizing ambient RF energy. In *Biomedical Wireless Technologies, Networks, and Sensing Systems (BioWireleSS), 2013 IEEE Topical Conference on*, pages 154–156, 2013.

[2] S. Kim, R. Vyas, J. Bito, K. Niotaki, A. Collado, A. Georgiadis, and M. M. Tentzeris. Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms. *Proceedings of the IEEE*, 102(11):1649–1666, Nov 2014.

[3] M Stoopman. *Circuit Design for Highly Sensitive RF-Powered Wireless Sensor Nodes*. PhD thesis, Delft University of Technology, Sep 2016.

[4] Y. Lim H. Tang S. Lim and J. Park. An adaptive impedance-matching network based on a novel capacitor matrix for wireless power transfer. *IEEE Transactions on Power Electronics*, 29(8):4403–4413, Aug 2014.

[5] K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu, and L. K. Nanver. Low-distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology. In *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, pages 389–392, June 2005.

[6] Q. Gu and A. S. Morris. A new method for matching network adaptive control. *IEEE Transactions on Microwave Theory and Techniques*, 61(1):587–595, Jan 2013.

[7] C. Chanlo A. van Bezooijen, M. A. de Jongh, L. C. H. Ruijs, F. van Straten R. Mahmoudi, and A. H. M. van Roermund. A GSM/EDGE/WCDMA adaptive series-LC matching network using RF-MEMS switches. *IEEE Journal of Solid-State Circuits*, 43(10):2259–2268, Oct 2008.

[8] Johor Bahru Y. S. Tang Johor Bahru Y. Yuan S. Bakhri, W. M. D. Chia B. Sunil Nicholas Fernandes M. Lee. Radio receiver with adaptive tuner. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, March 2012.

[9] https://www.ti.com/lit/an/scaa035b/scaa035b.pdf. [Accessed: 13- Dec- 2017].

[10] M. T. Penella-Lopez and M. Gasulla-Forner. *Powering Autonomous Sensors*. Springer, 2011.

[11] L. Doherty, B.A. Warneke, B.E Boser, and K.S.J Pister. Energy and performance considerations for smart dust. *International Journal of Parallel and Distributed Systems and Networks*, 4(3):121–133, 2001.

[12] Q. Gu and A. S. Morris. A new method for matching network adaptive control. *IEEE Transactions on Microwave Theory and Techniques*, 61(1):587–595, Jan 2013.

[13] S. Hemour, Y. Zhao, C. H. P. Lorenz, D. Houssameddine, Y. Gui, C. M. Hu, and K. Wu. Towards low-power high-efficiency RF and microwave energy harvesting. *IEEE Transactions on Microwave Theory and Techniques*, 62(4):965–976, April 2014.

[14] John Bird. *Newness Enginnering Scienece Pocket*. Pearson Education, Inc., third edition edition, 2011.

[15] C. Sui Y. Zhu J. H. Spears, W. Smith. Methods for tuning an adpative impedance matching network with a look-up table. US 8072285 B2, Sep 2008. [Online]. Available: https://www.google.ch/patents/US8072285.

[16] I. Adam, M. F. A. Malek, M. N. M. Yasin, and H. A. Rahim. RF energy harvesting with efficient matching technique for low power level application. *ARPN Journal of Engineering and Applied Sciences*, 10:8318–8321, 2015.

[17] Zohaib Hameed and Kambiz Moez. Design of impedance matching circuits for RF energy harvesting systems. *Microelectronics Journal*, 62:49–56, 2017.

[18] Ellicott City Yongfei Zhu Nashua John H. Spears, Johnsburg Wayne Smith Crystal Lake Chenggang Sui. Radio receiver with adaptive tuner. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, March 2012.

[19] Williant Stallings. *Wireless communications and networks*. Pearson Education, Inc., second edition edition, 2005.

[20] https://rohde-schwarz.com. [Accessed: 13- Dec- 2017].

[21] https://aaronia.com. [Accessed: 13- Dec- 2017].

[22] C. Henrique Petzl Lorenz D. Houssameddine Y. Gui C.M Hu K. Wu Simon Hemour Y. Zhao. Towards low-power high-efficiency RF and microwave energy harvesting. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2:31 & p. 420–432, March 2012.

[23] M. Piuela, P. D. Mitcheson, and S. Lucyszyn. Ambient RF energy harvesting in urban and semi-urban environments. *IEEE Transactions on Microwave Theory and Techniques*, 61(7):2715–2726, July 2013.

[24] http://wilysis.com/networkcellinfo. [Accessed: 10- June - 2017].

[25] https://opencellid.org/. [Accessed: 13- Dec- 2017].

[26] https://www.cellmapper.net/. [Accessed: 13- Dec- 2017].

[27] http://www.telecomabc.com/a/arfcn.html. [Accessed: 13- Dec- 2017].

[28] S. A. Mahmoud and T. B. Nazzal. Sample and hold circuits for low-frequency signals in analog-to-digital converter. In *2015 International Conference on Information and Communication Technology Research (ICTRC)*, pages 36–39, May 2015.

[29] C. Huang, K. Buisman, M. Marchetti, L. K. Nanver, F. Sarubbi, M. Popadic, T. L. M. Scholtes, H. Schellevis, L. E. Larson, and L. C. N. de Vreede. Ultra linear low-loss varactor diode configurations for adaptive RF systems. *IEEE Transactions on Microwave Theory and Techniques*, 57(1):205–215, Jan 2009.

[30] https://www.ti.com/europe/downloads/Choose [Accessed: 13- Dec-2017].

[31] M. D. Scott, B. E. Boser, and K. S. J. Pister. An ultralow-energy adc for smart dust. *IEEE Journal of Solid-State Circuits*, 38(7):1123–1129, July 2003.

[32] S. Hemour, Y. Zhao, C. H. P. Lorenz, D. Houssameddine, Y. Gui, C. M. Hu, and K. Wu. Towards low-power high-efficiency RF and microwave energy harvesting. *IEEE Transactions on Microwave Theory and Techniques*, 62(4):965–976, April 2014.

[33] Parascan tunable integrated capacitor. [Accessed: 13- Dec- 2017].

[34] http://stmicroelectronics.com. [Accessed: 13- Dec- 2017].

[35] Abul Sarwar. *CMOS power consumption and Cpd calculation.* Texas Instruments, Texas, TX, June 1997.

[36] S. Behnam Yazdani, A. Khorami, and M. Sharifkhani. A low-power digital to analog converter for sar adcs using one reference voltage. In *2015 23rd Iranian Conference on Electrical Engineering*, pages 1109–1111, May 2015.

[37] A. Valaee and M. Maymandi-nejad. An ultra low-power low-voltage track and latch comparator. In *2010 17th IEEE International Conference on Electronics, Circuits and Systems*, pages 186–189, Dec 2010.