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Monitoring the degradation of SiC MOSFETs undergoing thermo-mechanical stresses

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***Abstract*—This study investigates the degradation behavior and reliability of silicon carbide (SiC) MOSFETs under power cycling tests to address their vulnerability to thermo-mechanical stresses. Five 650 V SiC MOSFETs (IMW65R107M1H) were subjected to controlled thermal cycles, and key parameters such as body diode voltage, thermal resistance, and junction temperature were monitored. The degradation mechanisms, including bond wire fatigue and gate oxide defects, were identified through abrupt and gradual changes in the body diode voltage. A Weibull distribution was used to model the component lifetime, estimating a B-10 lifetime of 7279 cycles for devices with varying ΔT_j between 120 °C and 140 °C. Furthermore, the body diode voltage and gate leakage current were highlighted as effective precursors for early failure detection. This research provides insights into improving SiC MOSFET reliability and lays the groundwork for early warning systems in high-power converter applications.**

***Index Terms*—Reliability, Power Cycling Test, Lifetime Degradation Monitoring, Silicon-Carbide MOSFET**

I. Introduction

Reliability is defined as the probability that the product will perform its designated function without failure for a specific period. Commonly, the reliability is improved by adding redundant components or reducing the relevant stresses. Assessing the effectiveness of these measures requires knowledge about the expected component lifetime based on the underlying stress-dependent degradation mechanism. For high-power converters, the weakest components are semiconductor devices and capacitors [1], [2]. During the lifespan of semiconductors, they are exposed to repeated heating and cooling. These thermal cycles are primarily caused by variations in the load, switching actions, and environmental conditions. During these thermal cycles, the layers of the semiconductor expand and contract at different rates, resulting in shear stresses due to the difference in coefficient of thermal expansion (CTE) between the adjacent layers and the fixed constraints between layers [3], [4]. Those thermo-mechanical stresses can lead to bond wire cracks, bond wire lift-off, solder fatigue in the chip or the baseplate and reconstruction of chip metallization [5]. Failures in the chip and bond wire are the most common.

Commonly used semiconductor devices are silicon insulated-gate bipolar transistors (IGBT) and metal-oxide-semiconductor field-effect transistors (MOSFET). In addition, the SiC MOSFET is thriving due to its increased breakdown voltage, increased switching speed, increased thermal conductivity and reduced losses [6], [7]. These properties improve the reliability. However, the reduced chip area, increased power density and longer bond wires reduce the reliability [6], [7]. Moreover, the SiC MOSFET is more sensitive to gate oxide degradation than the MOSFET made of silicon.

The reliability of the converter can be increased by reducing the thermo-mechanical stresses on the semiconductors or by adding redundancy at system level. Alternatively, component-level redundancy can be explored by adding MOSFETs in parallel to take over in case of failure of the original MOSFET. A challenge with the second option is to prevent the original MOSFET from failing in a short circuit. Therefore, it is crucial to predict when a particular MOSFET is going to fail so its operation can be suspended. This requires condition monitoring algorithms based on failure precursors and correlating them with the remaining useful lifetime.

The aim of this paper is to study the behavior of the SiC MOSFET during the degradation process. In this paper, five SiC MOSFETs are thermally degraded and the body diode voltage, junction voltage, thermal resistance and lifetime are investigated. Furthermore, early warning precursors for wear-out failures are compared. With this information, the end of the lifetime of the MOSFET can be predicted and action can be taken to prolong the lifetime of the converter.

This paper is structured as follows: the methodology of the experiments is discussed in section II. Next, the results are discussed in section III, including a discussion of the body diode voltage, junction temperature, thermal resistance, thermal cycles to failure, Weibull distribution and effects after failure. In section IV, the precursors for an early warning system for bond wire fatigue are discussed and lastly, a conclusion is given in section V.

II. Methodology

The thermal and power cycling tests are valuable methods to impose thermal-mechanical stresses and determine the semiconductor device's lifetime [4], [8]. During the thermal cycling test, the heatsink is heated and cooled repeatedly. The devices will follow the thermal cycle of the heatsink. During the power cycling test, the pulsating current flowing through the device will heat the device. During this test, the heatsink has a fixed temperature and is used to cool down the device. The thermal

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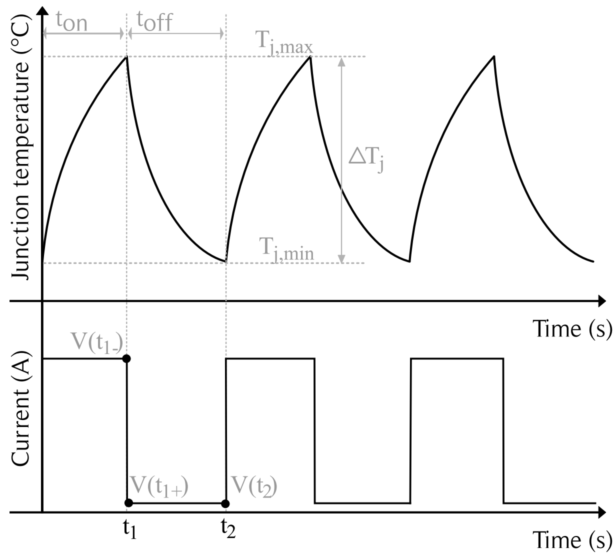

Fig. 1: Illustrative representation of junction temperature cycles created by the pulsating current flowing through the body diode. For every cycle, the voltage is measured three times.

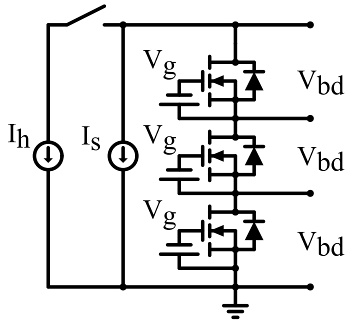

Fig. 2: Schematic representation of the test setup.

cycles can be executed faster in the power cycling test since only the device itself needs to be heated. Fig. 1 represents the junction temperature cycles obtained during the power cycling test. The other layers of the semiconductor device also experience thermal cycles and since each layer has a different coefficient of thermal expansion (CTE), thermo-mechanical stresses are created between adjacent layers.

Fig. 2 shows a schematic representation of the test setup. Herein, I_h indicates the pulsating current that heats the device. I_s is a small bias current that flows through the diode to measure the voltage drop and calculate the junction temperature during the cooling period. V_g is the gate-source voltage and V_{bd} is the measured voltage drop over the body diode. The chosen parameters for this power cycling test are summarized in Table I, in which T_{hs} is the temperature inside the heatsink.

The junction temperature cycles can not immediately be measured with the desired accuracy, so the voltage over the body diode is used. The relationship between the junction temperature and the diode's voltage drop is established during the calibration. In the calibration, the heatsink is set at different

TABLE I: Settings of the thermal cycling test.

Parameter	Setting
I_h	13 A
t_{on}	45 s
t_{off}	45.003 s
I_s	100 mA
V_g	0 V
T_{hs}	20 °C

temperatures, and the voltage drop over the diode is measured while applying a low-bias current. This current is set at 100 mA to prevent self-heating and have a negligible impact on the voltage drop across the drift region. The junction temperature is assumed to be the same temperature as the heatsink after reaching a steady state. The body diode voltage has a negative linear relationship with the junction temperature.

In the following experiments, five 650 V SiC MOSFETs are tested. The chosen MOSFETs for this experiment are the IMW65R107M1H from Infineon [9]. The MOSFETs will be degraded using the body diode losses to create thermal cycles.

III. Results

Throughout the degradation of the MOSFETs, the body diode voltage drop is measured three times in every cycle, as indicated in Fig. 1. The body diode voltage at the start and end of the cooling phase are used to calculate the junction temperatures. Furthermore, the electrical resistance and thermal resistance are measured. The values of these parameters at the start of the experiment are given in table II. The next part will discuss the measured parameters throughout the degradation test.

TABLE II: The parameters at the start of the test.

Parameter	S1	S2	S3	S4	S5
V(t_{1-}) (V)	4.0516	4.0687	4.0503	4.0288	4.1687
V(t_{1+}) (V)	1.7034	1.6728	1.6702	1.4432	1.6734
V(t_2) (V)	2.0874	2.0856	2.0847	2.1044	2.0998
$T_{j,max}$ (°C)	134.8	143.4	144.2	234.5	150.5
$T_{j,min}$ (°C)	10.6	10.8	10.9	12.3	13.6
ΔT_j (°C)	124.2	132.6	133.3	222.2	136.9
R_{on} (mΩ)	309	311	309	308	318
$R_{th,ja}$ (K/W)	2.1416	2.2053	2.2808	3.8129	2.2581

A. Body diode voltage

The voltage drop over the body diode is measured during each thermal cycle. Fig. 3 shows the diode's voltage drop for each cycle number at the end of the heating period V(t_{1-}), at the start of the cooling period V(t_{1+}) and at the end of the cooling period V(t_2). During the heating period, a 13 A current is flowing through the diode. The current is reduced to 100 mA during the cooling period.

The voltage drop over the body diode at 13 A current is used to monitor the degradation. It is known that cracks in the bond wire and solder layer abruptly increase the voltage, while gate oxide defects gradually increase the voltage. Since a SiC MOSFET is tested and V_{GS} = 0 V, the channel is not entirely closed and gate oxide defects are visible in the body diode's voltage. This gradual increase of V(t_{1-}) is around 0.06 % per

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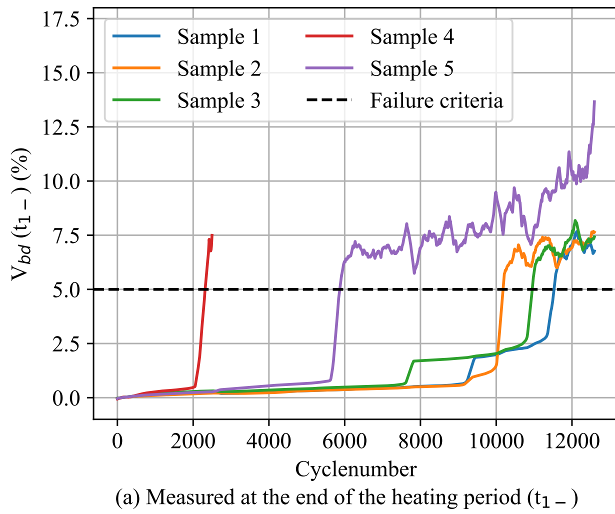
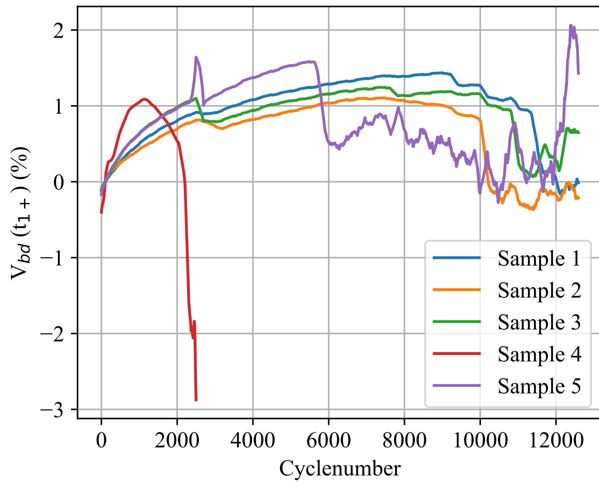
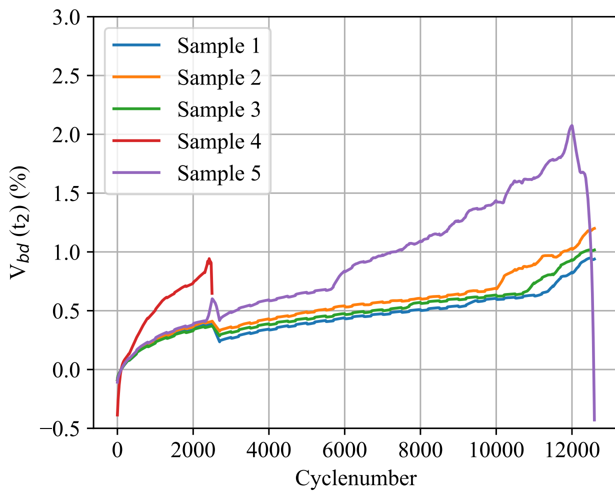


(a) Measured at the end of the heating period (t_{1-})



(b) Measured at the start of the cooling period (t_{1+})



(c) Measured at the end of the cooling period (t_2)

Fig. 3: Percentage increase of the body diode voltage throughout the power cycling test.

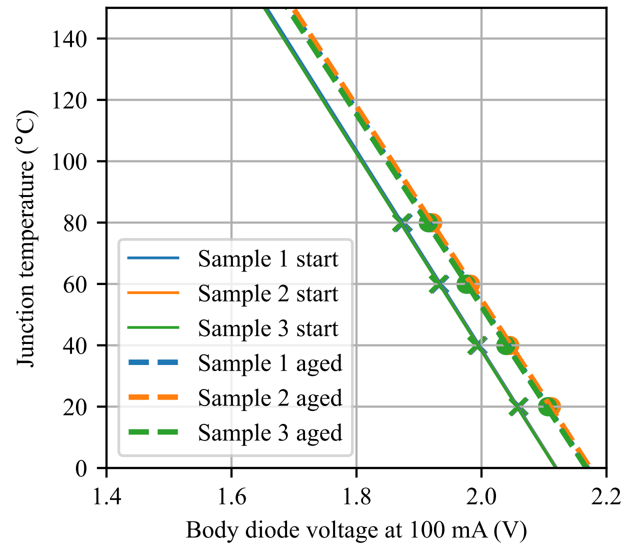


Fig. 4: The relation between the junction temperature and body diode voltage before and after the degradation test.

1000 thermal cycles at the start but increases up to 0.5 % per 1000 thermal cycles. Moreover, this voltage undergoes two abrupt jumps. After the first jump, the voltage reaches a stable value again, whereas after the second jump, the voltage becomes unstable. After the second jump, the failure criteria (5 % increase) is reached. The first voltage jump can be used for developing an early failure warning system.

B. *Junction temperature*

During the cooling period, a current of 100 mA flows through the diode. The measured voltage at the start of the cooling period V(t_{1+}) is around 1.7 V, while it is 2.1 V at the end of the cooling period V(t_2). Even though the current through the diode is the same, the measured voltage increases with the decrease in junction temperature. Hence, these voltages are used to calculate the maximum and minimum junction temperatures of each thermal cycle.

A calibration was performed before and after the degradation test, shown in Fig. 4. Unfortunately, the relation between the temperature and measured voltage changed throughout the degradation; The offset of sample 1 was reduced by 0.17 % while the slope was reduced by 2.43 %. This will eventually lead to a temperature mismatch of approximately 15 °C. For example, V(t_2) of sample 1 started at 2.0874 V and ended at 2.1097 V. Based on the calibration before the degradation, $T_{j,min}$ is 10.6 °C and 3.4 °C at the end. Based on the calibration after the degradation, $T_{j,min}$ is 18.8 °C at the end.

Throughout the degradation test, the heatsink temperature is around 20 °C and the cooling fluid inside the heatsink fluctuates around 14 °C. $T_{j,min}$ is expected to be constant throughout the degradation, assuming t_{off} is high enough to cool down completely. Moreover, the case temperature of the MOSFETs is measured. The case temperature is 40.0 °C

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and increases abruptly to 42.0 °C after 10 000 cycles. This is consistent with the observed abrupt increase in V($t_{1\text{-}}$) and associated power losses.

The shift in the calibration curves means that the physical properties of the SiC MOSFETs are changing. The cause of the shift could be the gate oxide defects. If so the problem can also be solved by applying a negative gate voltage to completely shut the channel of the SiC MOSFET. A solution for obtaining a more reliable junction temperature is to execute multiple calibrations throughout the degradation and interpolate the shift. The disadvantage is that calibrations are time-consuming and impose additional stresses on the devices, since the whole system is passively heated.

C. Junction voltage

The measured voltage of the body diode (V_{bd}) is an accumulation of the voltage drop over the p-n junction and resistance, shown in (1), where V_j is the voltage drop over the p-n junction, I is the current flowing through the diode, R_{bw} is the resistance of the bond wires, R_{drift} is the resistance of the drift region and R_{channel} is the resistance of the channel.

$$V_{\text{bd}} = V_{\text{j}} + I \cdot (R_{\text{bw}} + R_{\text{drift}} + R_{\text{channel}}) \tag{1}$$

This equation holds for all three measured voltages per cycle, only the current and temperatures vary per measurement point. During the cooling phase and measurement of V(t_2) and V(t_{1+}) the current is very low and the junction voltage will dominate the measured voltages.

Furthermore, it is assumed that the junction temperature of V($t_{1\text{-}}$) and V(t_{1+}) are the same since they are measured right after each other. By subtracting the equations for V($t_{1\text{-}}$) and V(t_{1+}), the junction voltage drops out of the equation and the equation is rewritten to find the value of the resistances, shown in (2).

$$R_{\text{bw}} + R_{\text{drift}} + R_{\text{channel}} = \frac{V(t_{1\text{-}}) - V(t_{1+})}{I_{\text{h}} - I_{\text{s}}} \tag{2}$$

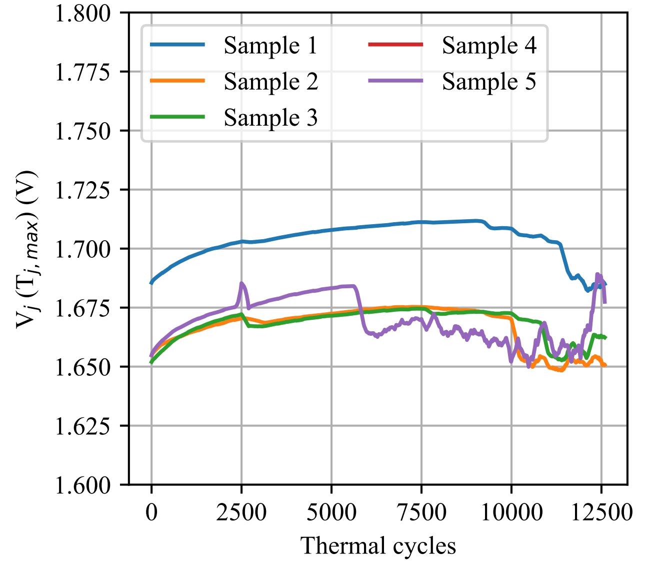
After knowing the value of the summation of the resistances, the junction voltage can be calculated with (3).

$$V_{\text{j}} = V_{\text{bd}} - I \cdot (R_{\text{bw}} + R_{\text{drift}} + R_{\text{channel}}) \tag{3}$$

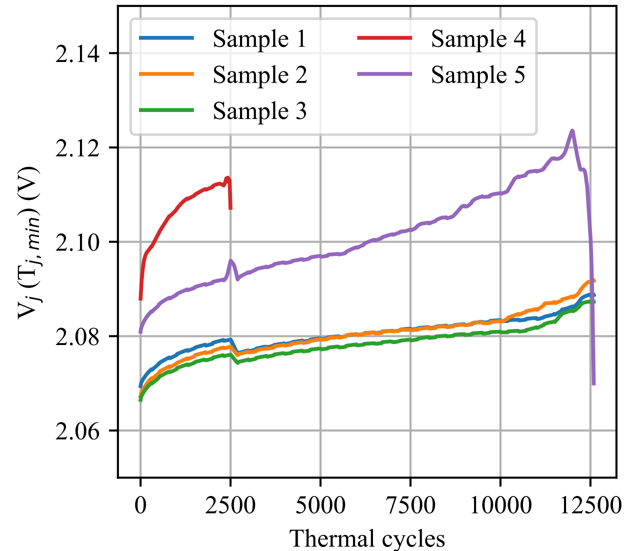
Filling in V(t_{1+}) gives V_{j} at the maximum junction temperature while V(t_2) results in V_{j} at the minimum junction temperature. The obtained results are given in Fig. 5. The junction voltage varies depending on the junction temperature. The results obtained with V($t_{1\text{-}}$) or with V(t_{1+}) are identical.

D. Thermal resistance

After every 500 thermal cycles, a thermal response measurement is performed to obtain the thermal resistance from junction to ambient, i.e. MOSFET, thermal pad and heatsink. The results are shown in Fig. 6. The thermal resistance from junction to ambient remains constant except for the last measurement of sample 5, which could be caused by the voltage's instability at the end of its lifetime.



(a) Junction voltage at maximum junction temperature



(b) Junction voltage at minimum junction temperature

Fig. 5: Junction voltage of the body diode.

The thermal resistance of sample 4 is higher than for the other samples because the connection from the MOSFET to the heatsink was weak. This also resulted in a higher $T_{\text{j,max}}$ compared to the other samples, which is in line with (4), where P_{loss} is the power loss, Z_{th} is the thermal impedance and T_{hs} is the heatsink temperature.

$$T_{\text{j,max}}(t) = P_{\text{loss}} \cdot Z_{\text{th}} + T_{\text{hs}} \tag{4}$$

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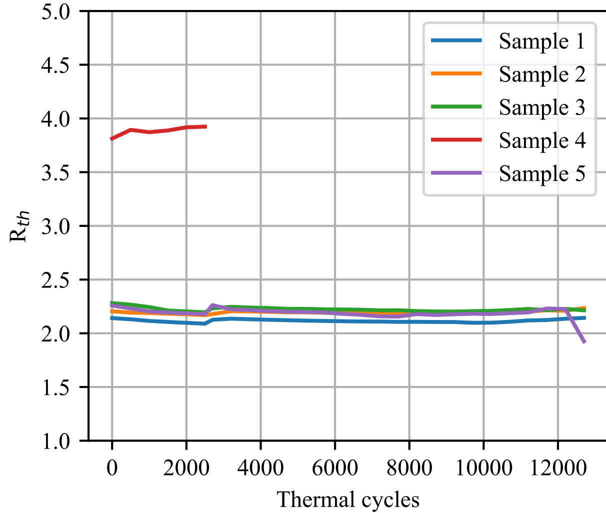

Fig. 6: Junction to ambient thermal resistance throughout the degradation.

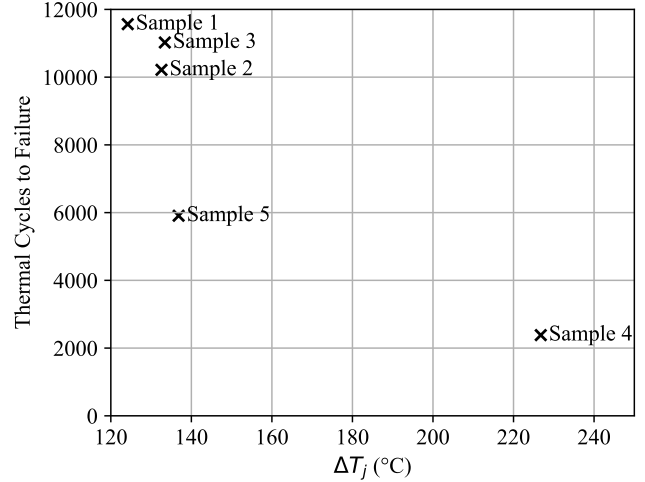

Fig. 7: The thermal cycles to failure against the temperature fluctuations.

TABLE III: The thermal cycles to failure.

	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
N_f	11 565	10 217	11 024	2384	5911

TABLE IV: The Weibull distribution and lifetime parameters.

	5 samples	4 samples	3 samples
α	9248	10 512	9906
β	2.59	6.11	5.27
B-10 lifetime	3890	7279	6474
B-50 lifetime	8030	9905	9252

E. Thermal cycles to failure

The number of thermal cycles to failure (N_f) is defined as the moment that the voltage over the body diode during the heating period increases by at least 5 %. Table III gives the thermal cycles to failure of every sample. Sample 4 is the first one that meets the failure criteria. This makes sense since the thermo-mechanical stresses are proportional to the temperature fluctuations and sample 4 has higher $T_{\mathrm{j,max}}$ and ΔT_{j}. The ΔT_{j} versus N_f is plotted in Fig. 7.

F. Weibull distribution

Weibull distributions are useful tools for studying device and system reliability [10]. The five samples are fitted for a Weibull distribution. The best fit is obtained with $\alpha = 9248$ and $\beta = 2.59$. With these values, the failure density function and reliability function are shown in Fig. 8 in blue. Based on this curve, the B-10 lifetime is 3890 thermal cycles, i.e. 10 % of the MOSFETs is expected to have failed. Moreover, 50 % of the MOSFETs is expected to have failed at cycle 8030.

In this experiment, sample 4 has a higher ΔT_{j} and should be removed when investigating the reliability of samples with ΔT_{j} between 120 °C and 140 °C. In this case, the Weibull distribution is best fitted with $\alpha = 10\,512$ and $\beta = 6.11$. The increase of β would give a narrower failure density curve and steeper reliability function, as shown in Fig. 8 in orange. Furthermore, the B-10 lifetime is improved to 7279 cycles and B-50 lifetime is 9905 cycles.

Moreover, the Weibull distribution is fitted with three samples that are closest to the median temperature. The median temperature in this experiment is 133.3 °C of sample 3. The fitting is done with samples 2, 3 and 5 and the resulting failure density function and reliability function are shown in Fig. 8 in green. The α is reduced to 9906 and the β to 5.27 compared to the fitting with four samples, since sample 5 failed significantly earlier than sample 1, 2 and 3. The reduction in α shifts the peak and curve of the failure density function to the left and the reduction of β makes the curve wider and the intensity of the peak lower. The reliability function is also shifted to the left and the B-10 and B-50 lifetimes are therefore also reduced to 6474 and 9252 thermal cycles respectively.

G. Failure effects

After the power cycling test, each sample is investigated. MOSFET samples 1, 2, 3 and 5 can still conduct and block the power. However, the measured voltage drop and electrical resistance fluctuate. There is expected to be a bond wire crack and the contact area will change after each thermal cycle. Moreover, the gate leakage current is around 0.95A in forward mode and 0.25A in body diode mode. In sample 4 an open circuit is created between the source to drain.

IV. Early warning precursors

In the literature, bond wire fatigues are detected by an abrupt increase in the channel resistance ($R_{\mathrm{ds,on}}$), body diode voltage drop (V_{bd}), thermal resistance (R_{th}), leakage gate current or leakage drain current [11]–[15]. Furthermore, the gate oxide degradation is detected with a gradual increase in $R_{\mathrm{ds,on}}$, V_{bd}, leakage gate current or leakage drain current. Additionally, the gate oxide degradation will shift the threshold voltage,

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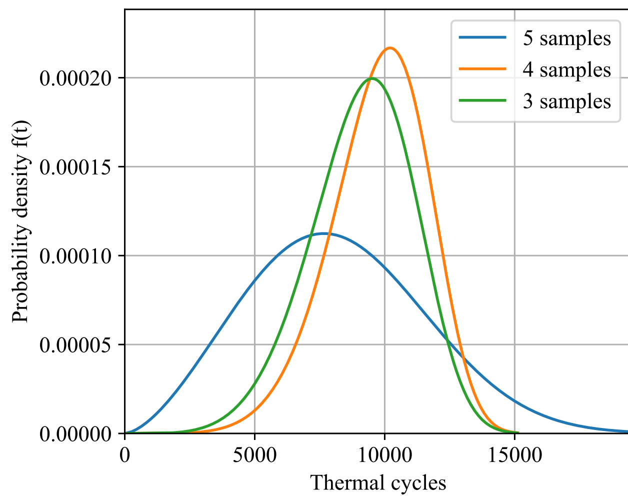
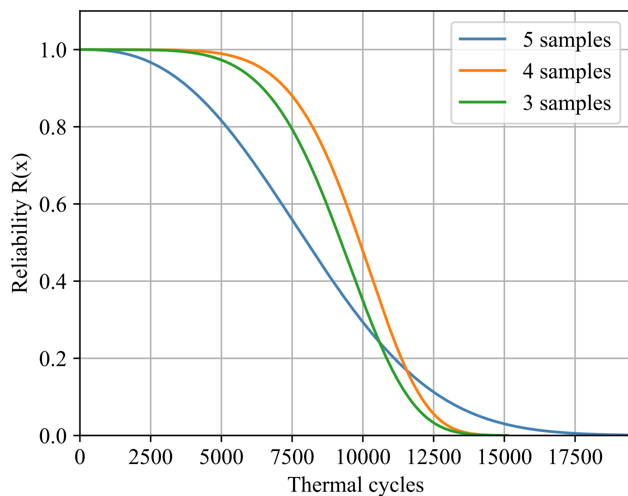


(a) Failure density



(b) Reliability function

Fig. 8: Weibull distribution of 3, 4 and 5 samples.

increase the gate-source capacitance and decrease the gate-drain capacitance [16], [17].

In this experiment, the body diode voltage during the heating period is an excellent precursor to detect bond wire fatigue since it increases sharply in a few hundred thermal cycles. Also, the gradual increase in the body diode voltage can be used to detect gate oxide degradation. The thermal resistance from junction to ambient is not significantly affected throughout the degradation and is not reliable as an early warning system. Furthermore, the junction temperature can be used to track bond wire fatigue and the difference in calibration curves can be used to track gate oxide degradation. Moreover, the gate leakage current can also be used as a precursor to detect failures and may also serve as an early warning system.

V. Conclusion

This paper studies the behaviour of five SiC MOSFETs during the degradation process. The degradation due to thermo-mechanical stresses is created with the power cycling test. During the degradation process, the body diode voltage, thermal resistance and junction temperature are investigated. The four samples with a ΔT_{j} around 130 °C have a lifetime of 6 thousand to 12 thousand thermal cycles. These samples are matched with a Weibull curve, resulting in $\alpha = 10\,512$ and $\beta = 6.11$ and a B-10 lifetime of 7279 thermal cycles. Furthermore, the body diode voltage is an excellent precursor for an early failure warning system.

References

[1] F. Blaabjerg, H. Wang, I. Vernica, B. Liu, and P. Davari, “Reliability of power electronic systems for ev/hev applications,” *Proceedings of the IEEE*, vol. 109, no. 6, pp. 1060–1076, 2021.

[2] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, “Condition monitoring for device reliability in power electronic converters: A review,” *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, 2010.

[3] S. Peyghami, P. Palensky, and F. Blaabjerg, “An overview on the reliability of modern power electronic based power systems,” *IEEE Open Journal of Power Electronics*, vol. 1, pp. 34–50, 2020.

[4] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, “Fast power cycling test of igbt modules in traction application,” 06 1997, pp. 425 – 430 vol.1.

[5] A. Abuelnaga, M. Narimani, and A. S. Bahman, “A review on igbt module failure modes and lifetime testing,” *IEEE Access*, vol. 9, pp. 9643–9663, 2021.

[6] K. Suganuma, *Wide Bandgap Power Semiconductor Packaging: Materials, Components, and Reliability*. Oxford, United Kingdom: Woodhead Publishing, 2018.

[7] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Wiley, 2002.

[8] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, “Application manual power semiconductors,” in *Application Manual Power Semiconductors*. Nuremberg, Germany: SEMIKRON, 2011, p. 466.

[9] Infineon Technologies AG, “Datasheet IMW65R107M1H,” 2024.

[10] A. O’Conner, M. Modarres, and A. Mosleh, *Probability Distributions Used in Reliability Engineering*. College Park, MD: University of Maryland Center for Risk and Reliability, 2011.

[11] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akın, “A new complete condition monitoring method for sic power mosfets,” *IEEE Transactions on Industrial Electronics*, vol. PP, pp. 1–1, 02 2020.

[12] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, “Degradation assessment and precursor identification for sic mosfets under high temp cycling,” *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2858–2867, 2019.

[13] B. Yu and L. Wang, “Real-time extraction of sic mosfets’ degradation features under improved accelerated power cycling tests for dc-sspc application,” *IEEE Transactions on Power Electronics*, vol. 38, no. 5, pp. 6489–6503, 2023.

[14] Y. Shi, Y. Chen, C. Peng, W. Zhu, and H. He, “Competitive failures decoupling and mechanisms analysis of sic mosfet module under power cycling stress,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 6, pp. 5877–5888, 2023.

[15] B. T. Vankayalapati, S. Pu, F. Yang, M. Farhadi, V. Gurusamy, and B. Akin, “Investigation and on-board detection of gate-open failure in sic mosfets,” *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4658–4671, 2022.

[16] A. J. Lelis, R. Green, D. B. Habersat, and M. El, “Basic mechanisms of threshold-voltage instability and implications for reliability testing of sic mosfets,” *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316–323, 2015.

[17] M. Farhadi, F. Yang, S. Pu, B. T. Vankayalapati, and B. Akin, “Temperature-independent gate-oxide degradation monitoring of sic mosfets based on junction capacitances,” *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8308–8324, 2021.

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