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31.4 A -91dB THD+N Resistor-Less Class-D Piezoelectric Speaker Driver Using a Dual Voltage/ Current Feedback for LC Resonance Damping

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Piezoelectric speakers are gaining popularity on account of their improving form-factor and audio quality, making them a good fit for many audio applications such as in televisions, laptops, etc. Such speakers can be modelled as a large capacitive load, and so are typically driven by a Class-AB amplifier via a series resistor that ensures driver stability, and limits load current, but wastes power [1,2]. In [3], the Class-AB amplifier is replaced by a more power-efficient Class-D amplifier (CDA) in series with an additional inductor. However, a series resistor is still required to damp the resulting LC resonant circuit, which could otherwise draw excessive currents when excited by large-signal distortion (e.g. clipping) harmonics around the LC resonance frequency. Alternatively, by using a feed-forward architecture based on LC filter diagnostics to limit overshoot currents, the series resistor can be replaced by a second inductor, at the expense of increased system complexity and cost [4].

This paper describes a resistor-less Class-D piezoelectric speaker driver that only requires a single inductor. LC resonance is damped by a dual-voltage/current feedback architecture, which is enabled by an on-chip current-sensing scheme. Furthermore, the use of a push-pull (PP) modulation scheme minimizes the amplifier's idle power consumption. Finally, chopping is implemented to improve linearity and PSRR across output power levels. The amplifier can drive load capacitances up to 4µF at full scale ($10.2V_{RMS}$ from a 14.4V supply) with peak currents of ~4.4A, without the losses associated with a series resistor. It consumes 3.5W for a 10kHz FS output signal and 122mW during idle operation, while achieving a peak THD+N of -87.3dB and –91dB, with 1kHz and 6kHz input signal, respectively.

Figure 31.4.1 shows a simplified system block diagram of the proposed driver. In addition to a voltage-feedback (VFB) path, a parallel current-feedback (CFB) path is implemented to increase the output impedance of the CDA around the LC resonance (f_{LC}), thus achieving damping without the power penalty of a series resistor. The output load current $I_O=V_{SW}/Z_{load}$ is sensed via a small sense resistor R_S, and thus the effective feedback factor of the CFB, $\beta_{CFB} = V_{SW}/V_{CFB} = R_SK/Z_{load}$, where Z_{load} is the load impedance seen at the switching output node (V_{SW}), and K is a CFB gain factor. The combination of the two feedback paths results in an overall feedback factor (β_{Total}) with a peak around f_{LC} and a fixed gain (normalized to unity) at other frequencies. This causes a notch in the CDA's closed-loop transfer function (V_{SW}/V_{IN}) that increases its output impedance around f_{LC}, and thus damps LC resonance. Since the notch is created by the LC impedance itself, it is insensitive to LC tolerance and aging. As shown in Fig. 31.4.1, increasing K results in more damping, but also increases the CFB gain in the audio band, and thus increases the effect of CFB nonlinearity. Further away from f_{LC}, the highly linear VFB dominates and determines the CDA's unity-gain frequency. In this work, K is made programmable.

Load-current sensing is achieved by sensing the IR drop across two on-chip sense resistors $R_{S-P/N}$ (20mΩ) in the H-bridge, as shown in Fig. 31.4.2. In a PP modulation scheme, only one side of the H-bridge switches, depending on the polarity of the audio signal, while the other side is grounded via a non-switching low-side device ($M_{L-P/N}$) and $R_{S-P/N}$. This single-sided switching scheme reduces switching losses by half, and significantly reduces the ripple current during idle operation since the pulse width would theoretically approach zero [5]. It also enables the use of a single readout amplifier to provide a quasi-continuous measure of I_0 by switching its input between the two sense resistors depending on the polarity of the audio signal (20Hz to 20kHz).

Compared to off-chip resistors, on-chip resistors offer a more compact and low-cost current-sensing solution. However, they have nonlinear IV characteristics, which worsen at high load currents, due to the combination of their temperature dependence and self-heating. To mitigate these effects, the CFB path is established via the virtual ground of the 2nd integrator (Fig. 31.4.2), ensuring that CFB non-linearity and noise are suppressed by the gain of the 1st integrator. Inserting a lowpass filter ($f_{LP} = 1/(2\pi C_2R_2)$ ~ 40kHz) in the CFB path results in a flat CFB gain (K) (referred to the CDA input) above 40kHz, thus allowing some flexibility in setting f_{LC} (>40kHz). While increasing f_{LP} would further suppress CFB non-linearity, it would also require a higher f_{LC}, and therefore a smaller L for a certain C_L, resulting in larger ripple currents and power loss. $R_{S-P/N}$ are implemented with diffusion resistors, since they are less susceptible to aging than poly resistors, and they also exhibit less temperature dependence than metal resistors.

As illustrated in Fig. 31.4.3, the PWM signals for a PP-modulated output stage H-bridge are generated by comparing the differential output of the loop filter ($LF_{OUT,diff}$) with two 180° phase-shifted triangular carriers ($V_{TRI,diff}\pm$). When $LF_{OUT,diff}$ is lower than both $V_{TRI,diff}\pm$, V_{SW-P}=0V and V_{SW-N}=14.4V; when $LF_{OUT,diff}$ is higher than both $V_{TRI,diff}\pm$, V_{SW-P}=14.4V and V_{SW-N}=0V, otherwise, $V_{SW-P/N}$=0V. Since the single-sided switching operation creates large CM content at $V_{SW-P/N}$, mismatch in R_{IN}/R_{VFB}, and low CMRR in the 1st integrator can cause significant distortion, especially for large signals [5]. To mitigate mismatch, R_{IN}/R_{VFB} are chopped. Switching nonidealities are reduced by ensuring that the chopping transitions occur when both $V_{SW-P/N}$ are grounded, such that CH_{HV} only switches near-zero signals. To minimize the CM-to-DM leakage due to the finite CMRR of the 1st integrator, a CM regulator is used to fix the virtual ground CM voltage ($V_{V.gnd,CM}$) to a DC value (~1.1V). In-band CM-to-DM leakage due to the mismatch of $R_{CMin-1/2}$ and $R_{CMout-1/2}$ in the CM regulator is also removed by chopping.

A fully differential 3rd-order CIFF loop filter, based on active-RC integrators, is used to create high loop gain around the output stage. Besides R_{IN} (20kΩ) and OTA_1, $R_{CMout-1/2}$ also contribute noise and are set to 25kΩ as a trade-off between noise and the output swing of the CM regulation amplifier. The closed-loop gain of the CDA is set by R_{FB}/R_{IN} (=8). An oscillator, based on an active-RC integrator, generates both $V_{TRI,diff}\pm$ (1MHz, thus 2MHz f_{PWM}), and the chopping clock (f_{CHOP} = 125kHz). The edges of the latter are aligned with the peaks of $V_{TRI,diff}\pm$ to ensure that the chopping transitions occur when both $V_{SW-P/N}$ are grounded. All RC networks are made 2-bit trimmable to account for process spread, and share the same trim code. Core LV devices (1.8V) are used for CH_{IN} and CH_{Vir}, whereas HV LDMOS devices are used for CH_{HV} [6].

The prototype IC, shown in Fig. 31.4.7, was fabricated in a 0.18µm BCD process and occupies 7mm². Powered from 14.4V / 1.8V supplies (P_{VDD} / A_{VDD}), it drives a 4µF capacitor via a series 1.1µH inductor (f_{LC} ~75kHz). The amplifier draws 8.5mA / 5mA from P_{VDD} / A_{VDD} during idle operation. Figure 31.4.4 (Top) shows the THD+N across input frequency for an output voltage $V_O = 5V_{RMS}$ with CFB gain K=1.25/2.5 respectively. Across output amplitude (Fig. 31.4.4 Bottom), the THD+N peaks at -87.3dB / 86.8dB and -91.1dB / 89.5dB for 1kHz and 6kHz inputs for K=1.25 / 2.5, respectively. Figure 31.4.5 (Top-Left) demonstrates the efficacy of the CFB by comparing the measured system STF (normalized to a unity gain), with a simulated STF (parameters extracted from LC impedance measurement) with the same LC filter used in the measurements. The STF peaking is reduced by 20dB and 22dB for K= 1.25 and 2.5, respectively. Figure 31.4.5 (Bottom-Left) shows the amplifier's power consumption across output amplitude while driving C_L = 4uF. The amplifier consumes 4.9W for a $4.4A_{peak}$ load current, which is dominated by the conduction and switching losses of the output stage. To emulate the same damping using a conventional CDA, a resistor (0.2Ω and 0.35Ω corresponding to K=1.25 and 2.5, respectively) would then need to be connected in series with C_L. A power saving of about 1.9W and 3.5W is achieved with K=1.25 and 2.5, respectively. As anticipated, the choice of K is a trade-off between the amount of damping, thus power saving, and large-signal linearity. Figure 31.4.5 (Top-Right) shows the measured PSRR when P_{VDD} is perturbed by a $1V_{RMS}$ sine wave.

Figure 31.4.6 summarizes the performance of the proposed piezoelectric driver and compares it with the state of the art. Thanks to the dual voltage/current feedback architecture, it is the only piezoelectric driver capable of damping LC resonance without a series resistance or any foreground calibration, and it offers a very compact load configuration (1L+C_L). The CDA can deliver ~$4.4A_{Peak}$, 1.5× higher than [1] and 3× higher than [2,3]. Compared to [4], it achieves a 3.7× better THD+N for 1kHz input signal, a 3.6× reduction in idle power consumption, and 3.9× lower power consumption for large load current ($3.5A_{peak}$). Moreover, it achieves competitive DR, output noise, and PSRR.

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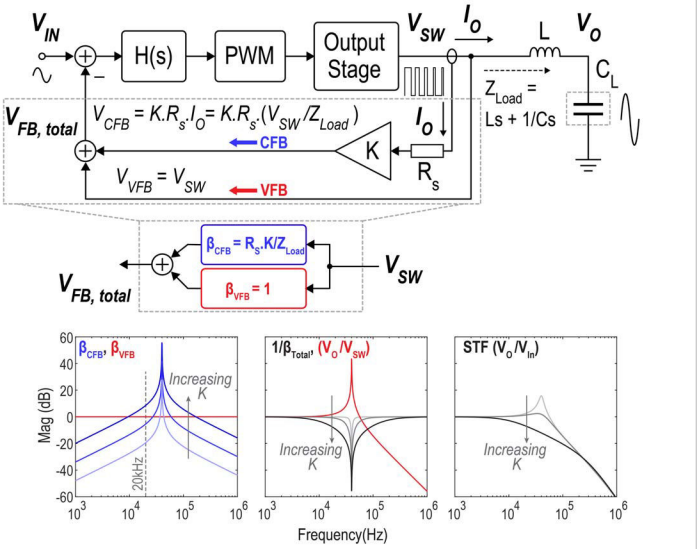

Figure 31.4.1: Simplified block diagram of the proposed dual voltage/current feedback piezoelectric speaker driver (Top); and the effect of CFB on the LC resonance and forward-path STF (Bottom).

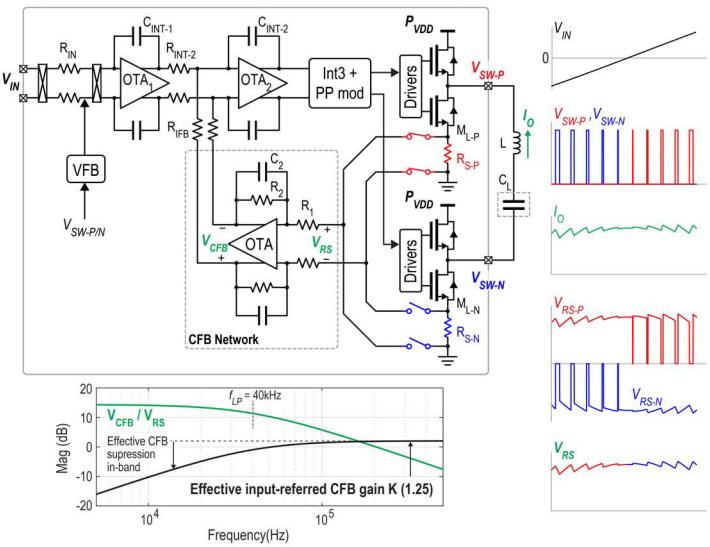

Figure 31.4.2: Simplified schematic of the CFB network (Top-Left); corresponding waveforms of signals (Right); and effective input-referred CFB gain K (Bottom-Left).

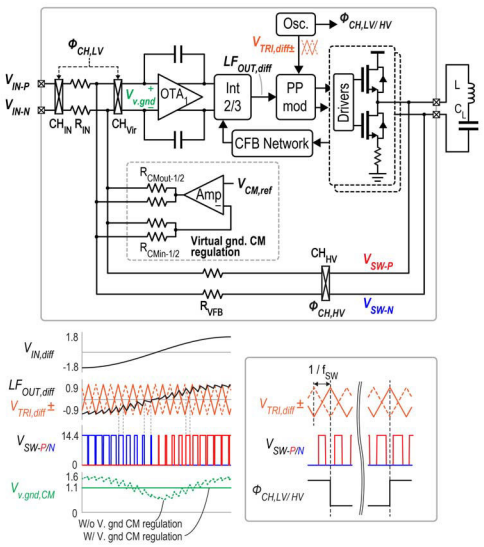

Figure 31.4.3: Simplified schematic of the CDA with chopper network and virtual ground CM regulation (Top), and corresponding waveforms of PP modulator and chopper signals (Bottom).

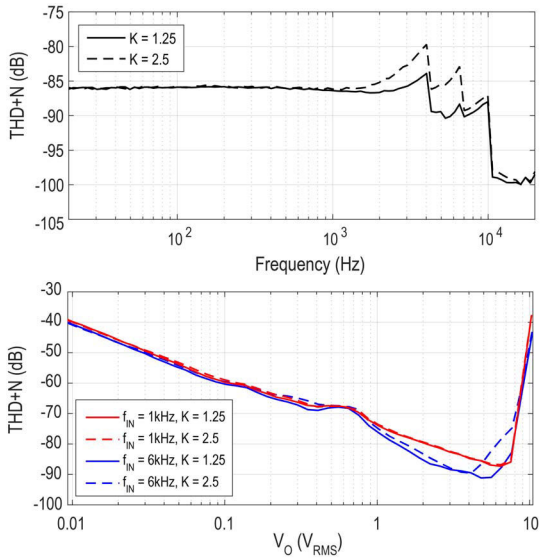

Figure 31.4.4: Measured performance of the CDA for P_{VDD} = 14.4V and C_L = 4µF: THD+N across f_{IN} for V_O = 5V_{RMS} (Top), and THD+N across output amplitude (Bottom).

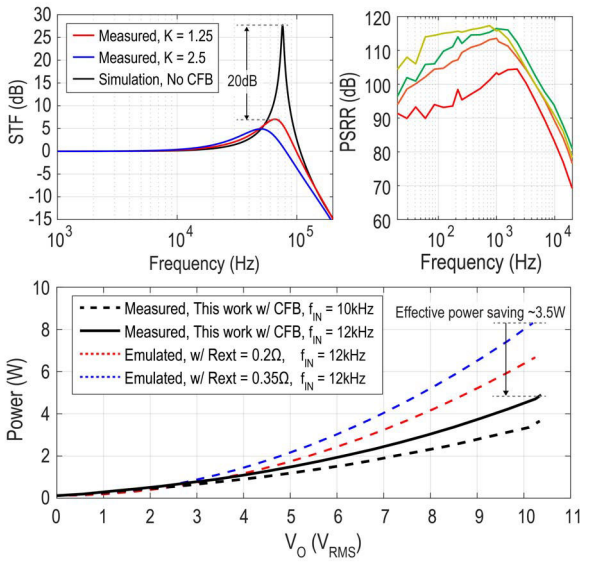

Figure 31.4.5: Effect of CFB on LC resonance (Top-Left); PSRR of the CDA [4 samples] (Top-right); power consumption vs V_0 for C_L = 4µF and f_{IN} =10kHz and 12kHz (Bottom).

	This Work	DRV5825P [4]		LM48560 [1]	MAX9788 [2]	TPA2100 [3]
Architecture	Analog in, Class-D	Digital in, Class-D		Analog in, Boost + Class-H	Analog in, Boost + Class-G	Analog in, Boost + Class-D
		1 channel	2 channel			
PVDD (V)	14.4	12	24	3.6	3.6	3.6
Piezo Load (uF)	4uF	1uF	4uF	1.5uF	1uF	1uF
Resistorless	Yes	Yes		No	No	No
Configuration	L + C_L	2L + 2C + C_L		R + C_L	R + C_L	R + L+ C_L
I_Q (mA)	8.5	37	130	4	8	5
P_O (mW)	122.4	444	3120	14.4	28.8	18
THD+N $_{PEAK}$ (dB) (fin = 1k)	-87.3 (K=1.25) -86.8 (K=2.5)	-77.0	-77.6	-66.0	-94.0	-66.0
THD+N $_{PEAK}$ (dB) (fin = 6k)	-91.1 (K=1.25) -89.5 (K=2.5)	-	-	-	-	-
Dynamic Range (dB) [A-wt.]	106.5	111 (24V supply)		-	106	-
SNR (dB) [A-wt.]	105.8	111 (24V supply)		98	108	94
Output noise (uVrms) [A-wt.]	45	45		134	-	-
Peak Current (A)	4.4	7.5	15	2.8*	1.4*	1.2*
Power Consumption (W)**	3.5	-	13.9	-	-	-
PSRR (dB) (20- 20kHz)	> 68	72***		> 50	> 58	> 80

* Estimated from plots

** C_L = 4uF, f_{IN} = 10kHz, V_O =10.2V_{RMS}

*** reported only at f_{SUPPLY} = 1kHz

Figure 31.4.6: Performance summary and comparison with existing state-of-the-art piezoelectric speaker drivers.

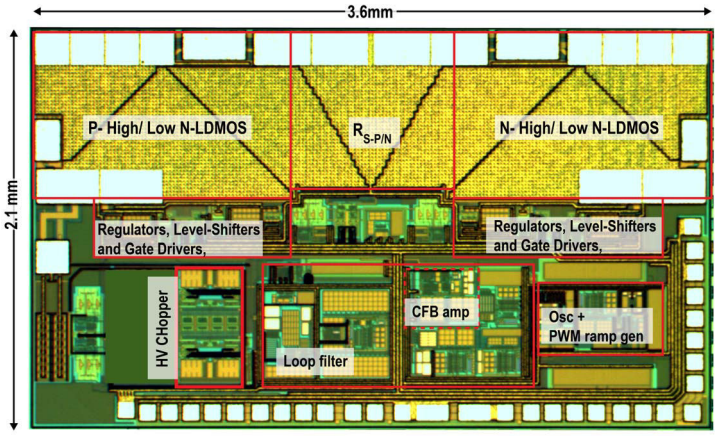

Figure 31.4.7: Die micrograph of the CDA.

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