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An Efficient Rectifier Hybridizing Synchronized Electric Charge Extraction and Bias-Flipping for Triboelectric Energy Harvesting

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***Abstract*—A triboelectric nanogenerator (TENG) is a kinetic energy transducer with small and time-varying internal capacitance, which increases the difficulties of extracting harvested energy. In this paper, an efficient rectifier, hybridizing synchronized electric charge extraction (SECE) and bias-flipping techniques, is proposed. The two techniques alternatively operate at opposite voltage polarities of the TENG. By taking advantage of the varying capacitance, the proposed synchronized extraction and flipping (SEF) rectifier shows significantly improved energy extraction performance. The design is implemented in a 180-nm high-voltage BCD technology, and the results show a 7.4X energy extraction enhancement, 65-V voltage tolerance, and 35-nA quiescent current.**

***Index Terms*—Energy harvesting (EH), synchronized switch harvesting on inductor (SSHI), synchronous electrical charge extraction (SECE), triboelectric nanogenerator (TENG)**

I. Introduction

Internet-of-Things (IoT) and biomedical devices are used to make people's lives smarter and easier. Most of them are powered by batteries, which will run out of energy eventually. Energy harvesting technology is considered an alternative power supply with more durability and a smaller form factor. The triboelectric nanogenerator (TENG) is one of the kinetic energy transducers proposed recently. It transforms kinetic energy into electrical energy via the displacement current generated by contact electrification [1]. Different from conventional kinetic energy transducers, such as electromagnetic generators and piezoelectric transducers (PT), TENG is advantageous in harvesting energy from low-amplitude and irregular vibrations, i.e., it is not limited by a fixed resonant frequency [2]. Hence, its applications in ambient and biological energy harvesting are largely widened [3]–[5].

Fig.1 presents a typical TENG and its electrical characteristics. The top and bottom electrodes produce an inherent capacitance, C_T, that is small and time-varying due to the displacement. Varying from tens to hundreds of pico-farads, C_T introduces high open-circuit voltage and asymmetric output impedance, decreasing energy extraction efficiency when using passive rectifiers. With the increasing research interest in triboelectric energy harvesting (TEH), several solutions were proposed previously. A dual-output full-bridge rectifier (FBR) with maximum power point tracking (MPPT) was proposed to improve the energy extraction performance of passive rectifiers [6], [7]. Active rectifiers were employed, such as synchronized switch harvesting on inductor (SSHI) [8], [9], multi-chip-stacked bias-flip (MCS-BF) [10], and multi-shot synchronous electric charge extraction (SECE) [11] rectifiers, to increase the energy harvesting efficiency. The bias-flip technique aligns the phases of the output voltage, V_T, and current, I_T, to decrease the energy loss when charging C_T. However, during the negative-I_T semi-period of TENG, C_T increases, which leads to electrostatic energy degradation of the flipped charge on C_T ($E = \frac{1}{2}Q^2/C$). This phenomenon only applies to varying-C_T TENGs, the majority of widely used TENGs. Hence, constant-C_T TENGs, such as wind-driven TENGs, are exempted from this energy loss. On the other hand, the SECE rectifier has lower energy extraction efficiency due to the charge-sharing loss. Therefore, efficient energy extraction circuits for varying-C_T TENGs are needed to minimize the electrostatic energy loss.

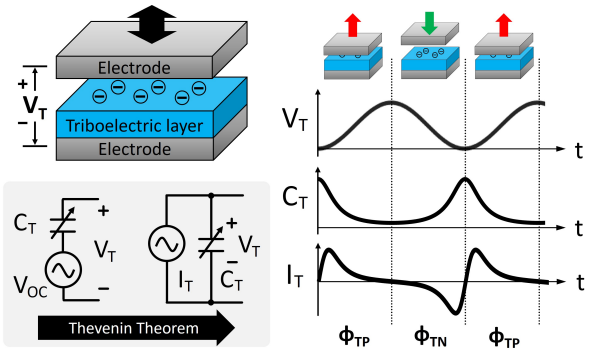

Fig. 1: The structure, equivalent circuit and characteristics of a typical TENG.

This work proposes a synchronized extraction and flipping (SEF) rectifier, hybridizing SECE and bias-flip techniques, to optimize energy extraction performance from TENGs. The theoretical research and topology of the proposed energy harvester will be first presented in Section II. Then, implementation details are presented in Section III, followed by the layout design and simulation results discussed in Section IV. Finally, the conclusion is drawn in Section V.

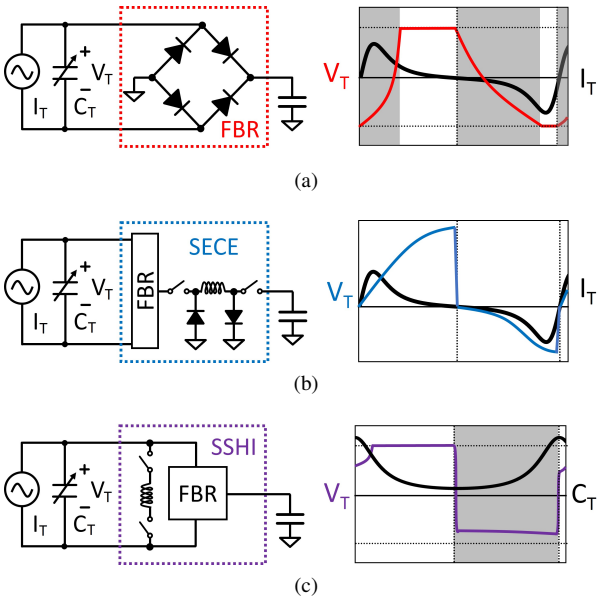

Fig. 2: The circuit and operation waveform of an (a) full-bridge, (b) SECE, and (c) SSHI rectifiers.

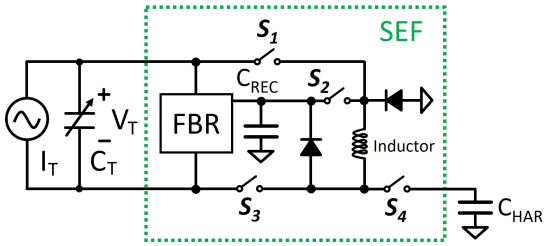

Fig. 3: The proposed synchronized extraction and flipping (SEF) technique for triboelectric energy harvesting.

II. Proposed Synchronized Extraction and Flipping Technique

A. Triboelectric energy harvesting optimization

Similar to piezoelectric energy harvesting, the internal capacitor of TENG, C_T, introduces a phase difference between the output voltage and current when harvesting energy via FBR, as presented in Fig.2(a), which causes energy loss. SECE and SSHI rectifiers were proposed to tackle this issue. An SECE rectifier accumulates the charge on C_T and extracts it when V_T reaches the peak. However, the current BCD technology can hardly tolerate the high open-circuit voltage from TENGs. On the other hand, an SSHI rectifier flips V_T when I_T changes polarity and extracts energy to a storage capacitor through a full-bridge rectifier (FBR). Nevertheless, the flipped charge will lose energy during the negative period due to the increasing-C_T as shown in Fig.2(c). Therefore, in this paper, we propose a new synchronized extraction and flipping (SEF) rectifier, employing the SECE and SSHI techniques in different half periods to optimize the energy extraction performance from TENGs.

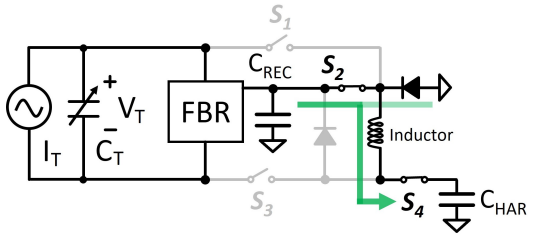

Fig. 4: The operation and current path when V_{REC} exceeds breakdown voltage.

B. Operational principle

Fig.3 presents the diagram of the proposed SEF rectifier. The FBR block and a rectification capacitor, C_{REC}, are used to store the extracted energy temporarily and to maintain the rectification voltage V_{REC} at a high level. Due to the high open-circuit voltage of the TENG, the maximum output power point is usually at hundreds of volts; thus, V_{REC} should be maintained at the breakdown voltage of the device to maximize the extracted power. The energy is converted to the harvesting capacitor C_{HAR} when V_{REC} exceeds breakdown voltage via a shared inductor, with the current path presented in Fig.4.

The operation waveform of the proposed SEF rectifier is shown in Fig.5. When I_T switches from positive to negative, when C_T is at its minimum value, an extracting phase occurs to completely extract the energy stored in C_T to C_{HAR} with the phases presented in Fig.5(b). At this moment, an SECE operation is more advantageous than a bias-flip operation because C_T will increase in the following semi-period, which degrades the energy of charge on it. Thus, emptying the charged in C_T reduces the subsequent electrostatic energy loss. Besides, it eliminates the polarity difference between V_T and I_T to reduce the energy loss in charging C_T. After a semi-period, I_T switches from negative to positive, and C_T is at its maximum value. Since C_T will decrease in the next semi-period, the charge on C_T can help harvest electrostatic energy. Hence, a bias-flip operation is more preferred here, compared to an SECE operation. Thus, bias-flipping is employed to synchronize the polarities of V_T and I_T and retain the charge in C_T. The operation phases of the bias-flipping are presented in Fig.5(c). Therefore, the proposed SEF is the most optimized electrostatic energy extraction method compared to single SECE or SSHI.

III. Implementation

A. System architecture

The architecture of the proposed SEF rectifier is presented in Fig. 7. The high-voltage (HV) 180-nm BCD technology is utilized to achieve a maximum device break-down voltage of 65V. The switches operating in HV region are implemented with laterally-diffused MOS (LDMOS) transistors with a breakdown voltage of 65V, while the control circuit works at 1.8V to lower the power consumption of the whole system. The TENG state detector monitors V_T and thus is designed with HV isolation and low-voltage (LV) MOSFETs. Based on

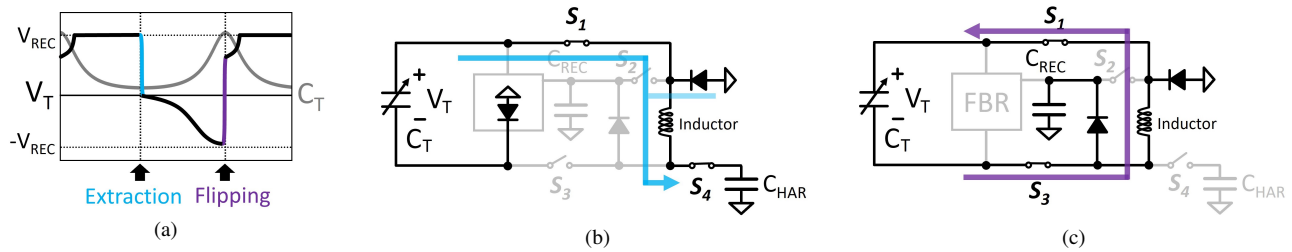

Fig. 5: (a) The operation waveform of SEF, and the current path when (b) synchronized extracting and (c) bias-flipping.

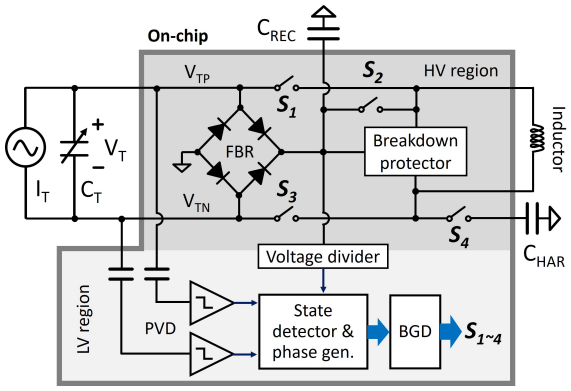

Fig. 6: The top-level block diagram of the proposed system.

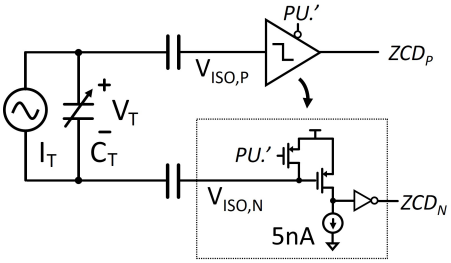

Fig. 7: The proposed peak voltage detector with HV capacitive isolation and fast low-power falling-edge trigger.

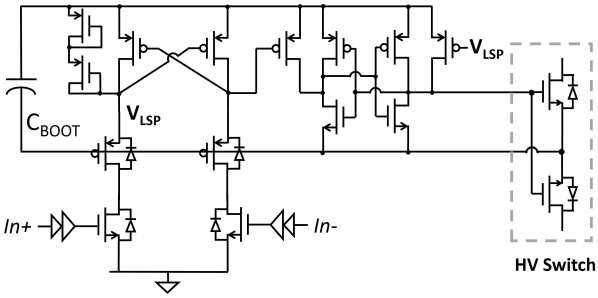

Fig. 8: The circuit diagram of the bootstrap gate driver (BGD) block and the HV switch (HVS).

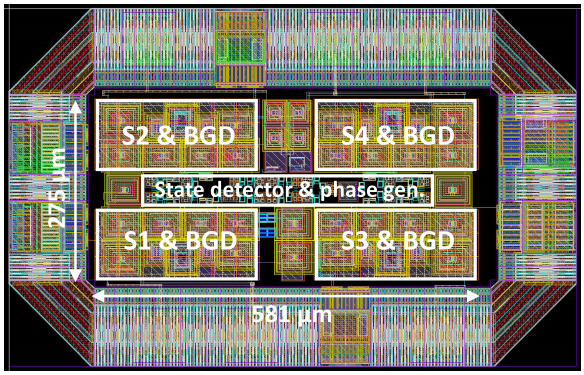

Fig. 9: The layout of the proposed rectifier.

the current state, the phase generator block will control the HV switches via bootstrap gate drivers (BGDs). The details of the state detector and BGDs will be elucidated in the following.

B. TENG state detector and phase controller

The voltage drop at the outputs of TENG when I_T crosses zero is monitored by a peak voltage detector (PVD). It consists of two parts: an HV capacitive isolation and a fast low-power falling-edge trigger. To protect LV MOSFET, V_{ISO} is pulled up when there is a sharp V_T variation. When utilized to sense the TENG state, the V_T variation can be converted to the trigger without degradation due to the high input impedance. This trigger is designed to operate at 1nA quiescent current, achieving fast responses to voltage drop.

In addition to TENG state detection, the PVD is also utilized to determine the flipping phase length in the bias-flip operation. During the flipping phase, V_T oscillates. The oscillation should be stopped after exactly a half pseudo-period when V_T reaches the maximum. To achieve this, fast responses to the voltage change are required. Thanks to the quick response of the PVD, nanosecond-scale control is achieved, which guarantees efficient bias-flipping.

C. High-voltage switch and bootstrap gate-driver (BGD)

Fig. 8 presents the circuit diagram of the BGD and the HV switches driven. The HV switch comprises two n-type LDMOS with source terminals connected to reject leakage current through the body diode. Due to poor mobility, LDMOS switches should be well-sized to hold the current. With a 1-mH inductor and thanks to the small C_T, the current flowing through the inductor is at the mA level; hence, the on-resistance of switches does not result in severe energy loss. The BGD drives this switch by controlling the gate-source voltage. To drive the switch, V_{BOOT} is charged to 5V first.

TABLE I: Comparison of the state-of-the-arts.

	JSSC 2021 [7]	TCAS-I 2021 [8]	JSSC 2022 [10]	**This work***
Process	180-nm BCD			
TENG capacitance	Varying	Varying	Fixed	**Varying**
Extraction Technique	Dual-output FBR	P-SSHI	MCS-BF	**SEF**
Inductor	10mH	2×1mH	10mH	**1mH**
Quiescent current	121nA	53nA	N/A	**35nA**
Power extracted by rectifier (P_{EXT})	3.9-10.5 µW	1.53mW	1.2mW (2-chips) / 823 µW (3-chips)	**133 µW**
FoM ($P_{\mathrm{EXT}}/P_{\mathrm{FBR,ideal}}$)	N/A	1.62×	3.14× (2-chips) / 2.14× (3-chips)	**7.4×**

* Simulation results

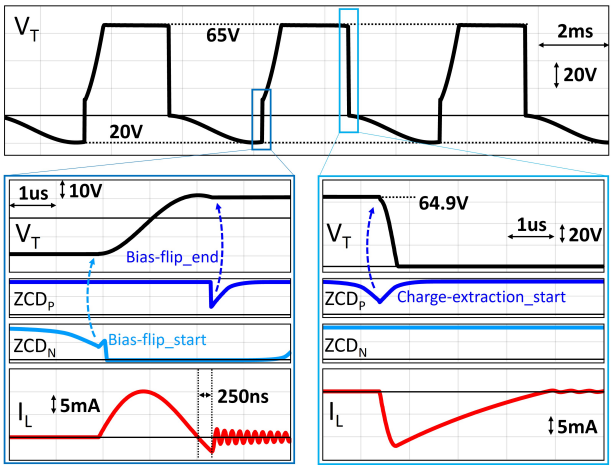

Fig. 10: The waveform of key signals in the rectifier.

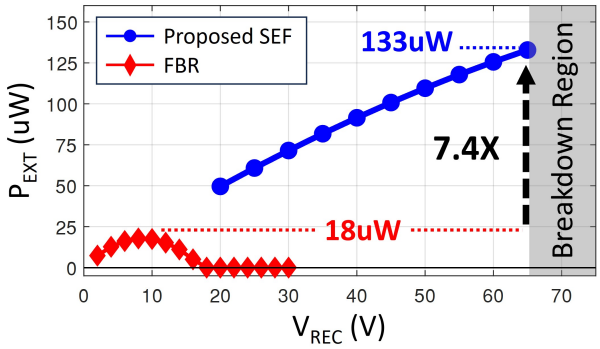

Fig. 11: The extracted power versus rectified voltage.

After providing a pulse to $In+$, the gate terminal of the switch is connected to V_{BOOT} so that when the source voltage lifts, the gate voltage follows to avoid the breakdown of the LDMOS. The switch is turned off by giving a pulse to the other input node $In-$ so that the V_{gs} is set to zero. This structure is advantageous in low static power consumption and can achieve free level shifting between 0V and 65V.

IV. Post Layout and Simulation Results

The layout of the proposed SEF rectifier is shown in Fig.9, with key blocks highlighted. The chip occupies an active area of $0.16\,\mathrm{mm}^2$ ($0.46\,\mathrm{mm}^2$ with pad-ring). The TENG model used in the simulations has an open-circuit voltage of 200V and capacitance varying between 45pF and 550pF. A segment of the transient waveform of V_T is presented in Fig. 10 when the operation frequency of the TENG is set as 200Hz. The system can operate at a maximum voltage of 65V. The bias-flip starts when PVD detects voltage drop at the negative side of V_T (V_{TN}). The flipping stops when a voltage drop is detected at the positive side of V_T (V_{TP}), which indicates that V_T reaches the peak. Due to the parasitic capacitance of the circuit, the voltage drop is delayed from the zero-crossing point of I_L by around $250\,\mathrm{ns}$, which leads to a slight degradation in the flipping efficiency. Thanks to the FBR, the voltage at either side of the inductor is limited to 65V to avoid on-chip device breakdown. Then, at the next zero-I_T moment, synchronized charge extraction starts after detecting a voltage drop at V_{TP}. The extraction stops when V_{TP} drops below $0\,\mathrm{V}$, which eliminates the need for precise control due to the current path through the diode.

The output power in a range of rectification voltage V_{REC} is presented in Fig. 11. The output power reaches a peak of $133\,\mu\mathrm{W}$ when V_{REC} is equal to $65\,\mathrm{V}$, which is 7.4 times higher compared to an ideal FBR. Thus, the proposed SEF rectifier effectively improves the energy extraction efficiency from TENGs. Besides, the quiescent current of the proposed rectifier is only $35\,\mathrm{nA}$, which strengthens the advantage of this system in low-power application scenarios.

Table. I compares the proposed rectifier with state-of-the-art triboelectric energy harvesting interfaces from different perspectives. This is the first time to hybridize the SECE and bias-flip techniques in triboelectric energy harvesting, achieving energy extraction enhancement of 7.4 times the output power of an ideal FBR and low-power sensing with a 35nA quiescent current.

V. Conclusion

This paper presents an efficient rectifier hybridizing the synchronized electric charge extraction (SECE) and bias-flipping techniques. Taking advantage of the varying internal capacitance of a TENG, the proposed rectifier minimizes the electrostatic energy loss and improves the energy extraction efficiency. Thanks to the HV process, the rectifier can tolerate 65V at the maximum to extract more energy and sense the TENG state with only $35\,\mathrm{nA}$ quiescent current. The energy extraction performance is enhanced by 7.4 times compared to a passive FBR interface.

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