Energy harvesting on the human body

Hybrid charge pump design for cold start compatibility and high efficiency harvesting with minimal footprint

by

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Abstract

This work proposes a new charge pump design suitable for energy harvesting on small human wearable devices. By using only one system for both cold start and high efficiency harvesting, the required silicon area is heavily reduced. The most fitting energy transducer is determined to be a photovoltaic cell, based on aspects of voltage, power and size. Both indoor and outdoor lighting conditions are suitable.

The literature on fully integrated voltage boosting with special attention to cold start shows that the capacitive charge pump is the best solution for high efficiency, low power and small size voltage boosting. For cold start applications, a Dickson charge pump with dynamic charge transfer switches is the best solution. For achieving high efficiency conversion, the Makowski charge pump is the best.

The proposed design combines the advantages of the Dickson charge pump for cold start and the high efficiency aspects of a Makowski charge pump for normal operation in one system with minimal silicon area. Using capacitor splitting, the conversion ratio of the cold start charge pump can be orthogonally chosen from the conversion ratio of normal operation. Dynamic charge transfer switches are used for the cold start charge pump to increase the performance.

An implementation of the proposed design is made in Cadence Virtuoso and is tested for cold start capability and efficiency across five process corners and three temperatures. The results prove that the proposed design can achieve high efficiency energy harvesting that is on average 5% below the efficiency of a normal Makowski charge pump. Cold start was achieved from 100 mV that is boosted to a battery voltage of 1.8 V within the micro-watt power range. With these results, the proposed charge pump is suitable for photovoltaic energy harvesting in small devices. The required silicon area is reduced by 50%, compared to systems where cold start and high efficiency harvesting are provided by separate systems.

The proposed design is made into a lay-out, which is currently being tested and will be manufactured in the coming months.

Preface

I would like to express my gratitude to all that have aided me this year. It has been a wonderful experience of learning, meeting people and collaboration. First, I want to thank Nowi energy for providing a challenging and fascinating project to work on. Working with all of you has been a great pleasure and has been a major part of my motivation. With special thanks to Andre Mansano and the IC team for supporting me with their knowledge. Throughout the year, posing ideas to you and discussing possibilities have been a great learning experience. Special thanks as well to Trang Bui for designing the front cover of the thesis.

Next, I want to thank Wouter Serdijn for his supervision on the project. Wouter Serdijn has always been an inspiration throughout the bachelor and master courses and is one of the major reasons to apply for this project to begin with. During the project asking him questions and posing ideas came at the reward of deeper questions that exposed the fundamentals of the issue at hand. With this fundamental understanding came a thorough evaluation and optimal solution that set the standard for the project.

Finally, I want to show my appreciation for my family and friends for their support. With your encouragement, this project became a pleasure to work on. Your interest in the topic boosted my interest even further. My special thanks goes to Rana, for her everlasting encouragement.

Luc van Wietmarschen
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1 Introduction

Technology is pushing devices to become smaller and smaller. Especially CMOS technologies offer miniaturised electronic systems to fit on single chips. These advancements have made IoT (Internet of Things) devices popular. Biomedical applications also see great use for these small electronics. The move to possible electroceuticals seems within reach and already many health applications rely on miniature electronics.

One major concern is the power usage of these devices. Batteries have not undergone much size reduction and often form the largest part of an electronic system. On top of that, battery life-time is not sufficiently long and batteries contain toxic materials that are unwanted, especially for biomedical applications. Connecting a device to the power grid solves the need for a battery, but this obviously limits the placement of devices and their mobility. Storing energy on (super)capacitors reduces the size and toxic aspects of storage. Unfortunately, these have a smaller energy density than batteries and would thus require constant replacement or recharging. Thus, a technological gap remains between the miniaturisation of smart electronics and the means to power them.

1.1. Energy harvesting

Luckily, a solution to the power demand has been found in energy harvesting. Energy harvesting is a manner of extracting energy from ambient sources to power electronics. Ambient sources can be in any of the energy domains. For example, in the mechanical domain vibrations and pressure contain energy and for the electromagnetic domain there is solar irradiation and radio signals. Each of these sources comes with their own transducers, often multiple per source. Never replacing batteries due to depletion and achieving autonomous operation can be achieved by utilising these energy sources.

However, the energy that can be extracted from these sources is minor. Careful management of the power is needed to extract as much energy as possible, especially considering small applications, where little room is available for the transducer. The sun does not always shine as bright and GSM signal strength differs depending on distance and reflections, indicating the unpredictability of ambient sources. This unpredictability adds to the need for power management.

In general, an energy harvester consists of the components visualised in Figure 1.1.

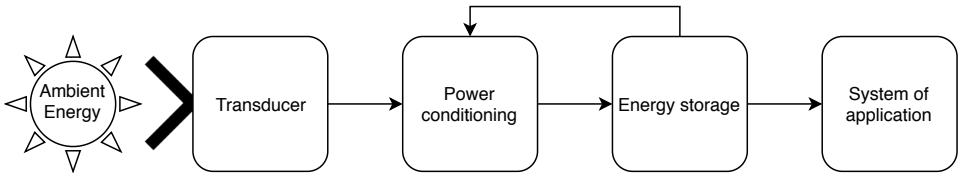

Figure 1.1: Schematic illustration of an energy harvesting system implementation. The arrows represent flow of energy.

Ambient energy sources often display a large range of possible energy states as the environment changes constantly. Therefore, directly connecting the transducer to the energy storage will result in unpredictable behaviour and losses. Hence, an energy conditioning circuit is needed to ensure that the correct voltage levels are met and power is extracted efficiently. To this goal, active circuits are required and thus energy is

consumed. As can be seen in Figure 1.1, the power conditioning block is powered by the storage. With the goal of extracting as much energy as possible comes the demand of low power consumption of the harvesting system itself. Therefore, creating self-driving manners of conditioning energy harvesters is of interest.

1.2. Cold start

With the virtue of not having to replace the power storage when empty comes the issue of not being able to access the power storage during critical phases of operation. The most important phase is the so-called 'cold start', where the device is fully energy depleted.

Normal circuits manage signals and energy by the use of active circuits, but an active circuit cannot operate without energy present. In the cold start scenario, the storage element does not possess enough energy to feed any component, meaning that the system cannot harvest energy and is stuck in a powered-down state. Cold start scenarios are most prominent after fabrication, where the device has never been powered on. Another cold start scenario is after a prolonged period of energy drought, causing the storage element to fully deplete.

Most solutions in literature utilise an additional circuit purely focussed on providing cold start. The system with cold start support will generally look as given in Figure 1.2. The cold start circuit should be able to start from minimal amounts of input power without the help of stored energy. The cold start circuit will scavenge energy to supply the power conditioning system only, so that normal energy harvesting can be done as soon as possible. After normal operation is achieved the energy from the cold start storage is often added to the main energy storage. The cold start system is less critical in efficiency compared to the power conditioning system, as it is only a one-time measure to start the circuit. The more important aspects of the cold start system are self-starting capability and minimal impact on the overall system performance during normal operation.

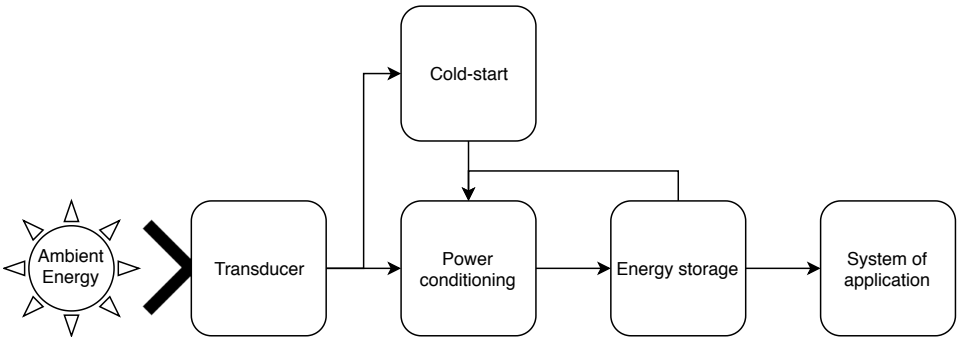

Figure 1.2: Schematic illustration of an energy harvesting system implementation with additional cold start circuit. The arrows indicate flow of energy.

1.3. Maximum power point tracking

Another important aspect of energy harvesting is maximum power point tracking (MPPT). Ambient energy sources change in power level often over a large power range. In different power points the transducer will change characteristics, most notably the impedance seen by the power conditioning circuit. The power conditioning system has to adjust to the new power point for optimal harvesting efficiency. The matching is less critical for high power conditions, as there is already a lot more power being delivered to the system.

The aim of MPPT is to identify the current power level delivered by the source and to adjust the harvester such that it operates for this point. This work considers small applications with little available power, thus the MPPT system should operate at low power and high power efficiency. Most MPPT techniques rely on complex calculations, but these are too power hungry to implement here.

1.4. Application and design goals

Although not the focus of this work, an application is used as guidance to make design choices. For the interest of bio-electronic applications a wearable device for humans is chosen. An implantable device would be more interesting, but also limits the design significantly and is likely not doable in the time-frame given for

this project. Implantation possibilities are given in the background information, but are not further explored. Of course, implantation of the device could be a next step in further research.

The project is assigned by Nowi-energy and their desire is to have a possible harvester solution for wearable devices around the wrist, such as a smart-watch, in the future. This work takes this as a start point for design. Important aspects of this energy harvester are the cold start capability and minimal size, since the wearable has little room for components. The design goals for the energy harvester are formulated from these desires as follows:

- The device will utilise the optimal ambient energy source for a wrist worn wearable;
- The device will harvest energy in the micro-watt range;
- The device will condition the energy such that it can be stored on a small battery or capacitor;
- The device will be able to cold start from low voltage levels;
- The device will achieve high conversion efficiency out of cold start;
- The device will be fully integrated except for the transducer and storage unit;
- The device will occupy as little silicon area as possible.

1.5. Structure

This work starts with a literature overview on energy sources that are suitable for the wrist worn energy harvester. All sources and their transducers are compared on aspects of importance and the best suited source and transducer is chosen. After that, background information on energy harvesting circuits is given and the sub-systems of importance are indicated. Special attention is given to cold start capability. With the background information given and the energy source chosen, a system is proposed that fulfils the design goals.

A detailed design of the charge pump is given next. This charge pump requires minimal silicon area and achieve high conversion efficiency after cold start, making it the most notable subsystem presented in this work. First, the theoretical framework that led to the charge pump design is given and after that the implementation is fully explained. A test case is given that suits the design goals. A proof of concept is simulated in Cadence Virtuoso for multiple process corners and operation temperatures for the test case. The results are discussed next and a conclusion on the proposed system is given after that. Lastly, future work is mentioned including recommendations for further implementation of the system.

2

Energy sources

2.1. Introduction

The topic of this thesis is energy harvesting on/in the human body, with special focus on cold starting the device. To achieve the optimal manner of energy harvesting, it is important to know what types of energy are available from the human body and what their aspects are.

The human body is capable of producing very constant energy sources (e.g. body temperature) and also very unpredictable ones (e.g. body movements). However, predictability is not the only aspect of importance for an energy source. For example the possible power that can be harvested with current (and future) harvesters is of great importance, as is the way this power is available (higher voltage or current). For the aspect of wearing the harvester, or possibly implanting the harvester, size and volume also play an important role and will significantly limit other aspects.

This chapter starts with the figures of merit for the application, setting limits to what energy sources are feasible. Next, each type of energy source is discussed. Lastly, an overview and conclusion are given that determine the direction this research takes for human body energy harvesting.

2.2. Figures of merit

The aspects that are of importance for an energy source are determined from the IC energy harvesting perspective, thus from the electrical domain. In this field the most useful parameters are voltage and power. Of course, these are inseparable from current, resistance, conductance and charge over time. Voltage and power are taken as the main aspects and thus used to characterise electrical systems.

One other aspect is the size of the harvester, considering a human has to carry the device. The most desirable would be a harvester that is fully integrated in IC technologies, since it is the smallest possible and the easiest to implement with other components. Especially for implanted devices these dimensions are more strict.

2.2.1. Voltage constraints

In IC design a certain level of voltage is needed to drive transistors, the basic building block for integrated systems. This level is determined by the technology and known as the threshold voltage (V_{th}), the minimum gate to source voltage needed for conduction. The threshold voltage is determined by many factors, such as temperature, oxide-thickness, bulk voltage and parasitic effects. This does leave opportunities to lower the threshold voltage through design. It is possible to reduce the needed voltage level down to 50 mV-100 mV in common technologies, such as 0.18 µm CMOS [1–4]. However, higher voltages are much more desired to ease the used technique and reduce current leakage. A more desired voltage level would be around 400 mV to 700 mV.

Due to the fact that most energy sources and harvesters cannot deliver these levels of voltage (consistently), many technologies to boost voltages have been developed. Designing a voltage booster will be one of the challenges of this research, if the harvester itself does not provide a high enough voltage. As described in literature voltages as low as 15mV can be boosted successfully [5], but more consistently, systems requiring around 50mV are found.

2.2.2. Power desires

Due to the use of active elements and the fact that ideal elements do not exist, the system dissipates energy. A high voltage alone will not suffice to harvest energy; power is needed as well. It is key to deliver more power to the system than it is using, otherwise building up energy needed to power other components is impossible. This sounds obvious, but remains an often overlooked aspect of energy harvesting.

Most energy harvesting IC applications use capacitors to store energy and use the metrics of said capacitor to indicate power. Indications of power can be: the current fed to the capacitor, the charge build-up on the capacitor over a period of time or the time it took to charge a capacitor to a certain voltage. To relate all metrics to power the following equations can be used:

$$\begin{aligned} P &= V \cdot I = V \cdot dq/dt = dE/dt \\ P_{cap} &= \int_0^Q V(q)dq = \int_0^Q \frac{q}{C}dq = \frac{Q^2}{2C} = \frac{1}{2}CV^2 \end{aligned} \tag{2.1}$$

Where P is the power, P_{cap} is the power stored on a capacitor, E the energy, V the voltage, I the current, Q the final charge on the capacitor, C the capacitance of the capacitor and t the time.

For an energy harvester it is of course the goal to harvest maximum energy, and thus the power delivered in time by a source is the most determining characteristic. However, with respect to cold start it might be more advantageous to sacrifice some power for a higher voltage to drive a first stage of the system. For most energy harvesting scenarios the target lies within the micro-watt range of desired power.

2.2.3. Size and scalability constraints

Since the device will be implemented on or in the human body, the size of the device plays an important role as well. On the body sizes of more than a couple of cm^2 becomes uncomfortable and inside the body one should be considering the mm^3 to μm^3 range. Optimally the harvester would be IC compatible and part of the system on a chip. For a wearable, a size of 4 cm^2 would be the maximum. This allows plenty of room for other components and be comfortable.

Most harvester types come with specifications that indicate how much power could be harvested per surface area on a device. This specification often assumes a linear relation between power and volume and thus leaves the aspect of scalability in the dark. For example, it is well known that inductors lose most quality at micro scale, as they exhibit extremely low Q-factors at these sizes. Another example could be a Peltier element, a thermal to electrical energy conversion element that relies on a difference in temperature. At micro scale the opposing sides of the element might be so close that heat flows easily from one side to the other, significantly reducing the difference in temperature and thus the output power.

It is also important to note what shape the harvester can take. Some devices require their design to be a square box or sphere, whereas others can be made of multiple smaller components that are later connected. Some harvesters allow for other components to be placed close or integrated with the harvester and others require their own space to operate.

2.3. Thermal energy

Thermal energy harvesters (TEH) are very popular due to the ease of having a DC output voltage that is linearly related to the temperature difference and relatively high power delivery. The major disadvantage of off-the-shelve thermal energy converters is their size and low output voltage.

This section first discusses the aspects of the human body as a thermal energy source, followed by a couple of types of harvesters with their advantages and disadvantages. The section is concluded with an overview of existing thermal harvesters and their specifications.

2.3.1. The human body as thermal energy source

The human body regulates its internal temperature quite precisely at 37°C. Since thermal energy harvesting relies on temperature differences, harvesting inside the body is clearly limited. On the other hand, harvesting on the human body is more feasible. Here, a difference in temperature of 15°C is seen, assuming room temperatures of 20°C.

However, this temperature difference does not represent the harvesting scenario. As the harvester is taking energy from the temperature difference and because heat leaks around the device, the temperature difference decreases. The constant power that can be harvested thus depends on the static temperature difference that can be established. The hot side of the TEH is regulated by the energy spent by the body to increase the

temperature, whereas the cold side can be aided with a heat sink element. In literature, a steady temperature difference of around 3 – 5°C should be achievable on the body (using a heat sink and a device of several cm^2) [6, 7].

A person could also be outside, thus not a room temperature environment. When outside the temperature difference depends on the climate and could both be better and worse. When exercising, the body produces more heat, leading to an increase in temperature at the hot side of the TEH, possibly allowing for higher temperature differences. However, if the climate induces temperatures higher than the body temperature the effects are reversed. On top of that the heat sink is now be at the hot side of the TEH and thus hindering harvesting. Using thermal energy harvesting on the human body can thus best be done in a controlled environment.

H. Wong *et al.* identified what part of the lower arm could best be used to harvest thermal energy and found that the palm of the hand is kept at the highest temperature when harvesting [8]. This is most likely due to the veins running close to the surface.

2.3.2. Discrete Peltier element

Most articles that discuss thermal energy harvesting consider a discrete Peltier element as their energy source. The Peltier element is schematically given in Figure 2.1.

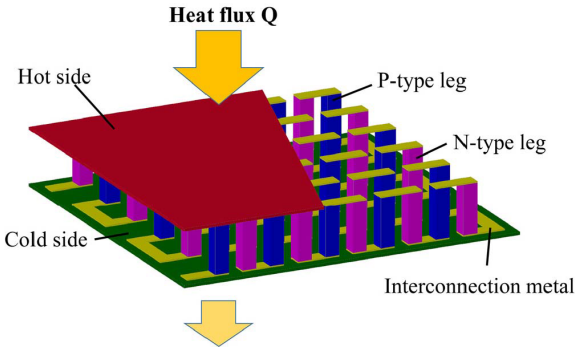

Figure 2.1: Schematic view of a thermal energy harvester [9].

Peltier elements generate currents by temperature differences in p-type and n-type materials. Each pair of p-type and n-type legs form a thermocouple. Connecting multiple thermocouples is used to sum the power output of each separate thermocouple. A flow of temperature is needed to generate power, indicated as the heat flux.

The number of legs can easily be changed to achieve different power and voltage behaviour, but the thermal properties of the hot and cold side are dependent on size and thickness. Of-the-shelf elements produce around $50\,mVK^{-1}$, a power output of around 1 mW and range in size from $10\,mm^2$ to $25\,cm^2$, too large for implantable applications and borderline acceptable for larger on-body applications [6, 10, 11].

2.3.3. Integrated Peltier element

A logical step is to integrate a Peltier element in a standard CMOS process to reduce size and greatly enhance compatibility for IC applications. In [12] a fully integrated Peltier element of 408 thermocouples was achieved within $925\times745\,\mu m^2$. Ultimately achieving an output voltage of 0.4 mV and output power of 124.8 nW at a temperature difference of 15 K. The design is characterised by $4.22\,mVmm^{-2}K^{-1}$ and $4.08\,nWmm^{-2}K^{-1}$. Meaning that roughly 10 mm would be needed to achieve the voltage levels displayed by discrete elements, which is feasible in-vivo and fine on the human body. However, an integrated system with these dimension is costly to produce.

2.3.4. Pyroelectric harvester

To step away from the Peltier element and its limitations researchers have developed Pyroelectric harvesters. These harvesters have a far higher thermodynamic efficiency and do not require a large heat sink to get a good thermal gradient. The pyroelectric effect is based on certain dielectric materials that can spontaneously depolarise under temperature change [13].

Energy can only be generated with temperature oscillations, a drawback when considering biomedical

applications. On top of that, targeted temperature differences below 20 °C are not reported, a difference (especially in oscillation) that is not seen on the human body. Therefore, the pyroelectric harvesters are not be considered for this research.

2.3.5. Existing thermoelectric generators

Table 2.1 gives an overview of developed TEGs, assorted by size. The voltage and power produced is given as a function of temperature. Keeping in mind that the static temperature gradient is around 3 to 5 Kelvin, it can be seen that not a lot of power and low voltages are to be expected. Also, note that power seems inversely proportional to voltage for most designs, most clearly seen from the first two entries.

Table 2.1: Existing TEGs and their specifications. [9] is a summary of multiple works and thus has multiple TEGs.

Source	**Size** [mm^2]	**Voltage** [mVK^{-1}]	**Power** [nWK^{-2}]
[9]	35	11.2	0.56
[9]	32.5	0.39	1072
[9]	25	1.25	105
[9]	16	200	4.16
[9]	9	14.4	22.7
[9]	2.25	22.6	5.65
[9]	1	0.34	838
[12]	0.93×0.75	2.9	$2.8\,nWK^{-1}$

2.4. Kinetic energy

Humans tend to move or at least have organs that move, making the mechanical domain a logical choice for human energy harvesting. Kinetic energy harvesting is characterized by a source delivering an acceleration, often given in g at a certain frequency, where $1g = 9.81\,m\,s^{-2}$.

This section begins with examining the available power from kinetic energy from the human body. After that, two different types of kinetic energy harvesters are discussed: piezoelectric harvesters and electrostatic harvesters. Next, more focus is put on electrostatic harvesters for their more complex operation and the possible high voltages that can be produced, which is of interest for cold start purposes.

2.4.1. The human body as kinetic energy source

Movement in and on the human body is very location dependent. As can be imagined, the ankle moves a lot during walking, whereas the jaw moves during speech. These movements are not very predictable and can rarely be characterised with one frequency. The heart or lungs on the other end move far more periodically, although this period still changes with strain.

One aspect of importance is the strain that is imposed by the harvester on the body. Since energy is taken from the movement, the body must deliver this energy on top of the energy it would need for the movement alone. Harvesting as much energy as possible from any part of the body should not impose too much effort for the body, especially with vital motions such as breathing and heart pumping. Also speech should not be impaired by some heavy device on the jaw. Locations such as the ankle and wrist could pose less of a problem as people already tend to wear accessories there without effort.

2.4.2. Maximum available kinetic power

Modelling the available kinetic energy is often done by considering a mass, spring, damper (MSD) system that is excited by the movement. The energy in the MSD system is then seen as the possible available energy. The conversion from the mechanical to electrical domain is thus not yet taken into account.

In [6], available kinetic power is examined considering the head. Considering transient movements, the authors approximate the average power that can be harvested to be 25 µW. These results are based on the movements of the head during walking mostly. One other possible location would be on the jaw, where chewing and speech are the main source of kinetic energy. The estimation is that 700 µW is available there, although more uncomfortable to wear.

[14] considers the movements of the wrist, ankle and waist. It is found that normal daily activities, excluding walking and running, should produce up to 5 µW on the wrist. With walking for five minutes, the average

power could build up to 8 µW and running can provide 350 µW. These measurements are however quite simplistically taken and [15] acquires more accurate data on these movements. In general, it can be expected that movements of the human body are in the 0.1Hz to 50Hz range, with most in the lower ranges.

2.4.3. Kinetic energy harvesters

Kinetic energy harvesters can be made fully integrated with Micro Electro Mechanical Systems (MEMS) technology. Many applications already exist that convert mechanical energy into electrical energy using MEMS. A MEMS device does not require any part to be exposed to the environment, as acceleration effects the entire system. This allows for the harvester to be placed anywhere in the device, allowing for much more freedom in design. Mechanical energy harvesters that are not MEMS devices are too large to consider for this project.

Two types of Kinetic harvesters are discussed here that are both produced in MEMS technology. First the piezoelectric harvester and second the electrostatic generator.

2.4.4. Piezoelectric conversion

A well-known mechanical to electrical domain conversion is through the piezoelectric (PE) effect, where a movement of charge is generated from deformation of a PE material. The movement of charge poses a voltage difference, which can be harvested as electrical energy. One common practice is to integrate a PE material along a structure that bends. The simplest manner is using a cantilever, which is relatively easy to build in MEMS technology. An example of such cantilever is visualised in Figure 2.2. A cantilever can be characterised as a MSD system and thus connects to the previous section on available power.

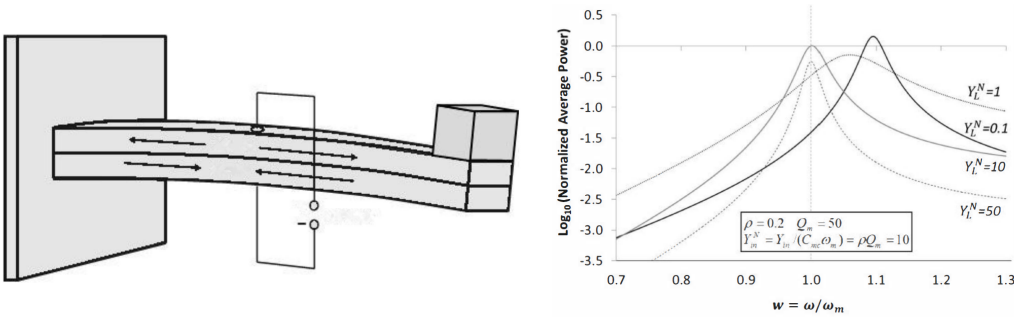

Figure 2.2: (a) General cantilever design for PE harvesters. (b) Normalised frequency dependency of power produced by a PE harvester. Both from [16].

The energy generated by the PE material depends on the amount of total deformation and the amount of deformations per second. These two aspects are interlinked, as a system with higher amplitude in movements moves slower. The optimal power generation is achieved at the resonance frequency of the MSD system, where amplitude and frequency are optimally balanced. Unfortunately, this resonance frequency is often a lot higher than frequencies found on the human body and the power conversion rapidly drops at other frequencies [10, 16–18]. This behaviour is also seen in Figure 2.2(b).

Techniques have been developed that can increase the power conversion outside of this bandwidth. For example a voltage applied to the material can change the mechanical stiffness, thus changing the resonance frequency. Another option is using a RLC tank circuit, but this requires quite a large inductor. To emulate this large inductor it is possible to apply a so-called BiasFlip [16, 18].

2.4.5. Electrostatic generator

One other type of harvesters that rely on kinetic energy are electrostatic vibration energy harvesters (e-VEH). These harvesters rely on a variable capacitor with a charge difference present on the plates. The variation in capacitance is generated by moving the plates. As the capacitance changes the voltage over the capacitor also changes, generating an electrical signal that can be harvested. Another way to see it is as the electrostatic equivalent of a magnet and coil: the moving charge generates a changing electric field between the plates which induces a movement of charge in the circuit, thus a current. This is also visualised in Figure 2.3. The magnet and coil type of harvester (magnetostatic harvester) is not examined further due to the required magnetic element and coil that cannot be made efficiently in MEMS technologies.

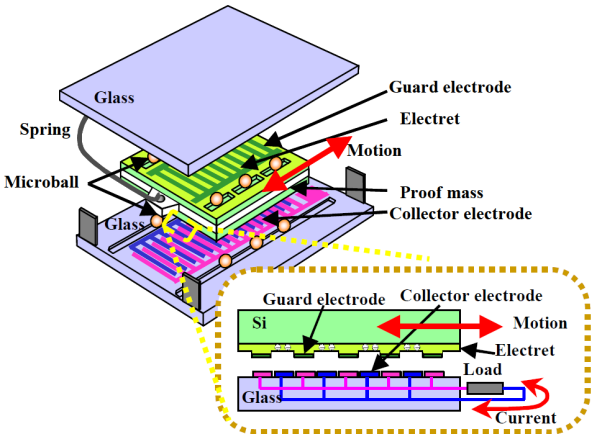

Figure 2.3: Electrostatic generator with the general manner of operation given. [19]

MEMS implementation The e-VEH can be built in MEMS technology, with one of the capacitor plates on the substrate and the other (moving) plate as a suspended mass. Quite similarly to the PE harvester the e-VEH harvester harvests the most power when the mass is moving at the resonance frequency. At this frequency, the mass moves optimally in speed and amplitude and thus generates the most power. A design proposed in [20] utilises two types of springs with different spring constants that support the mass to realise a non-linear response, resulting in a broadening of the frequency range at the cost of peak power.

In the end the device was able to produce 3 µW average output power with voltages from 10 to 38V peak-to-peak when subjected to pseudo-random vibrations ranging from 26 to 40 Hz at an $1.2g_{rms}$ acceleration. A peak output power was found of 6 µW at $1.4g$ accelerations of 40 Hz.

Initial charge creation One very important aspect is the required charge on the capacitor. From a cold-start perspective it is not possible to provide this charge through a conditioning circuit. The most common solution is to use an electret material, a material that can hold a high charge density after processing (up to $2\,\mathrm{mC\,m^{-2}}$) [19–25].

One other possibility is the use of triboelectric contacts. Here the initial charge is generated by having each electrode composed of materials with different electronegativity conditions and does not come with a pre-charge. The charge generated relies on many random components and is often lower than that of electret counterparts, resulting in less power converted. The advantage is that no post-processing is needed to set the initial charge.

One last option is to create the high charge needed by the use of a Bennet's doubler. A Bennet's doubler is a device which creates a high static voltage through a sequence of operations utilising at least three metal plates. A traditional Bennet's doubler requires very specific movements that would be hard to realise in an IC, let alone an energy depleted system. The solution proposed by [26–29] is to integrate the e-VEH part with the Bennet's doubler with the use of diodes. The main drawback here are the losses in the components and the requirement to have at least a small charge present at the start of the system.

2.4.6. Existing kinetic energy harvesters

Table 2.2 gives the specifications of some piezoelectric harvesters. As can be seen the input characteristics are not standardised. The sizes also vary quite a lot, especially since some designs future disk shaped PE harvesters. In Table 2.3 a number of e-VEH devices that have been produced and their specifications are given. All these devices are electrostatic harvesters. As can be seen lowering size and frequency comes at the cost of power and voltage.

Comparing Table 2.2 and Table 2.3 gives insight into the differences between PE and electrostatic harvesters. The first thing to note is that e-VEHs are often smaller and can operate at lower frequencies, making them more suitable for human body motion harvesting. The e-VEHs are also capable of producing far higher voltages. The downside of the e-VEHs are the high produced voltages. The voltages are quite high for CMOS implementations and will result in higher parasitic losses and more strain on the device.

Table 2.2: Overview of piezoelectric harvesters. mm_{pp} means the maximum displacement of the tip in mm.* Only the frequency of acceleration is given.

Source	Size	Kinetic input	Max power	Optimal load	Voltage
[30]	10×1 cm^2	1g at 4Hz	70 µW	1.4 kΩ	310 mV
[31]	19×14 mm^2	0.16g at 212Hz	280 µW	23 Ω	2.56 V
[32]	400 µm radius	0.01g at 8kHz	26 nW	300 kΩ	80 mV
[33]	9.2×1.5 cm^2	5.5g at 1.5Hz	3.7 µW	10 MΩ	6 V
[34]	23×23 mm^2	$0.8mm_{pp}$ at 80Hz	1.5 µW	333 kΩ	700 mV
[35]	50 mm radius	10-110Hz*	2.45 µW	200 kΩ	700 mV

Table 2.3: e-VEH overview of other works. mm_{pp} means the maximum displacement of one of the plates in mm. * One harmonic of the heart movement is at 20Hz, on which the system focusses.

Source	Size	Kinetic input	Max power	Optimal load	Voltage
[20]	12×11mm^2	1.2g at 26-40Hz	3.4 µW	-	$20V_{pp}$
[36]	$5 \times 5 \times 5$mm^3	20Hz, Heart motion*	10 µW	-	-
[19]	24×27mm^2	1.4g at 20Hz	40 µW	7 MΩ	$16.7V_{rms}$
[22]	20×20mm^2	$1.2mm_{pp}$ at 20Hz	700 µW	2.5 MΩ	$42V_{rms}$
[23]	30×30mm^2	$5mm_{pp}$ at 10Hz	7.7 µW	80 MΩ	$25V_{rms}$
[37]	17×19mm^2	0.5g at 16-28Hz	1.5 µW	40 MΩ	$8.2V_{rms}$
[38]	38 mm diameter	2πrad s^{-1}	80 µW	-	$60V_{pp}$
[39]	4×2mm^2	1.6g at 10Hz	2.5 µW	20 MΩ	$8V_{pp}$

2.5. Photo Voltaic

Photovoltaic (PV) energy harvesting is well known from current solar panel technology. For wearable or implantable PV harvesting a major reduction in size is needed. Especially in CMOS technology, the PV harvesters can best be called PV cells (also known as solar cells). The difference between photo diodes (PD) and PV cells is that the PD is often used as a sensor and is tuned to that purpose. The tuning includes focus on specific wavelengths and does not focus on maximum power output. The PV cell is designed to receive energy from a broad spectrum and is fabricated for high power output. One great advantage of PV cells is their scalability, as all specifications of PV cells scale almost linearly with size.

First, this section discusses the important characteristics of light as an energy source. Next, three sources of light for harvesting are examined: From the human body, from the sun and lastly from artificial light sources. After that, the specifications of light harvesters are explained. Power and voltage specifications for state-of-the-art PV harvesters under multiple conditions are given at the end of the section.

2.5.1. Characteristics of light

Energy from light sources is often characterised from the perspective of the human eye (in lux), but for the purpose of an energy harvester the radiometry approach is preferred. Radiometry characterises light by the distribution of the radiation's power in space. The received radiant flux (power) per surface area is called the **irradiance** (in W m^{-2}) and is the most used specification of light sources, sometimes referred to as intensity. The opposing measure is **radiosity** (also in W m^{-2}), which is the outgoing flux per surface area. It is important to note that irradiance depends on the source output power, the distance between source and receiver, the spectral profile of the source and the spectral sensitivity of the receiver.

Especially the latter two are often overlooked and can be deceiving, as observing light by eye alone gives a different impression than is acquired from measurements. For example silicon (a basic component of ICs) seems dark and opaque to the eye, but is transparent for infra-red radiation. Another misconception is that a fluorescent lamp seems bright to the eye and thus energetic, but it only transmits energy at very specific wavelengths, making the total energy a lot lower.

2.5.2. The human body as PV energy source

The human body is almost a perfect radiator in the infra-red spectrum (thus black-body radiation), with an emissivity coëfficient of $e = 0.98$ (where $e = 1$ would be the ideal radiator). For the average human body the radiosity is close to 66 W m^{-2} at room temperature, when using the basic equation for radiation heat transfer. For a small harvester of 1 mm^2 the maximum possible power that can be harvested is thus 1 µW, which is not

too bad. Losses are not taken into account and it should also be noted that the light emitted is in the infra-red spectrum, so a PV cell that is sensitive in this region should be used.

In essence this energy harvesting transfer is from the thermal domain to the radiation domain to the electrical domain. The radiosity is calculated assuming a black-body radiation that relies on a temperature difference between the body and surrounding air, thus the problems mentioned about temperature differences of the thermal energy case should again be taken into account.

2.5.3. PV energy in/on the human body

As mentioned before there are many other sources of PV energy outside of the human body, obvious ones being lamps and the sun. Harvesting this energy requires a clear path between the source and receiver, thus the harvester location on the body is of importance. For example clothing blocks light easily. The human body is also a quite good absorber of light and implants deep in the body receive close to no light. However, applications close to the skin surface can still receive energy, as was shown by [4] where 1.6 µW was harvested under pork skin, fat and muscle tissue with an irradiance of $10\,\mathrm{W\,m^{-2}}$ from a halogen lamp.

For harvesters on the body even more power is available. Especially wearables such as watches are often exposed to light and can be of areas up to a square centimetre. Other possible locations would be on the head or on clothing. Unfortunately, wearing a device on the head is not conventional and thus might be rejected by users, but an accessory on clothing can be more approved. For example, fashion that includes solar panels is already on the market.

2.5.4. Solar energy

The sun, much like the human body, can be characterised as a black-body radiator. The sun is a lot hotter (5400 K) than the human body and thus provides far more power, even at the earth surface. Taking into account the effects of the atmosphere it is safe to say that the sun delivers $1000\,\mathrm{W\,m^{-2}}$ irradiance when at zenith. The irradiance drops to roughly $750\,\mathrm{W\,m^{-2}}$ at an angle of 37°, which is at the height of the USA on the globe. The solar spectrum is a broad spectrum from roughly 250 to 2500 nm although two-thirds of the power is in the 250 to 1100 nm range. The peak of the spectrum is in the visible light range, which is why our eyes developed to be most sensitive to this spectral band.

The greatest downside of using solar energy as a source is that the sun does not always shine and that humans spend a lot of time inside, where there is also less solar energy. On average, a day in the Netherlands receives a total of $2.5\,\mathrm{kWh\,m^{-2}}$ global irradiation [40]. For the average day length of 8 hours in which a person spends one hour outside an irradiance of $39\,\mathrm{W\,m^{-2}}$ is found. However, during winter it may be that a person is only outside in the morning before sunrise and in the evening after sunset, resulting in no solar energy received.

2.5.5. Artificial PV energy

Time during the day that is not spent in the sun is often spent under artificial lighting, another source of PV energy. Lamps on their own are far more predictable over the course of a year compared to the sun. However, there are many types of lamps, each with their own radiosity and emission spectrum. The spectra are determinant for the type of solar cell that should be used to harvest the energy.

The most common light profiles within the visible light spectrum are qualitatively given in Figure 2.4. These are generalised spectra, as lamps can often be fine-tuned slightly (as seen by the cool white and warm white LED difference). The irradiance that is available from the lamps depend on how many lamps are in use and how much energy is fed to them. In a research with PV energy in an arbitrary office, an average of $1.63\,\mathrm{J\,cm^{-2}}$ radiant energy is seen during workdays, whereas $0.37\,\mathrm{J\,cm^{-2}}$ is seen on the weekends, when the lights are mostly off [42].

Most offices operate with Fluorescent (CFL) lighting at the moment, but it is expected that LED lighting will take over in the future [43, 44]. [44] performed measurements of each of these sources to indicate the illumination at 400 lx to give a more quantitative description of the sources. The resulting spectral irradiance is given in Figure 2.5. This figure neatly displays the difference between radiometry and photometry. Both sources result in a luminosity of 400 lx, but from the irradiance it can be seen that the power for the CFL is concentrated in small peaks and that the LED spreads the power.

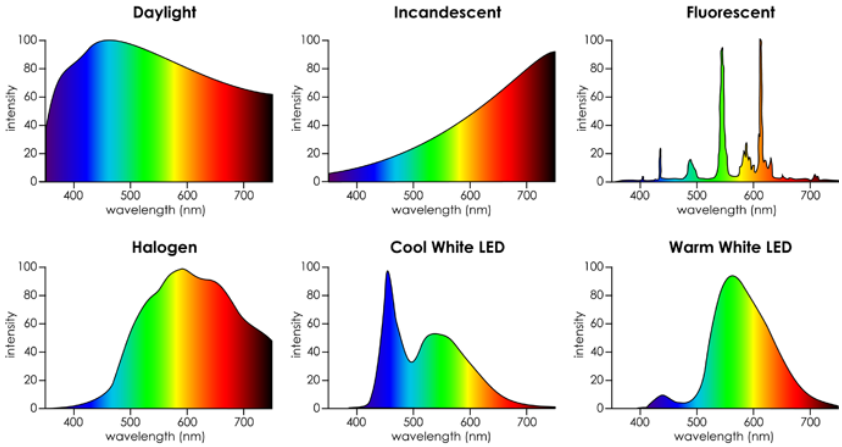

Figure 2.4: Qualitative representation of the light intensity produced by common light sources for different light wavelengths [41]. The Incandescent bulb intensity drops rapidly after 800 nm.

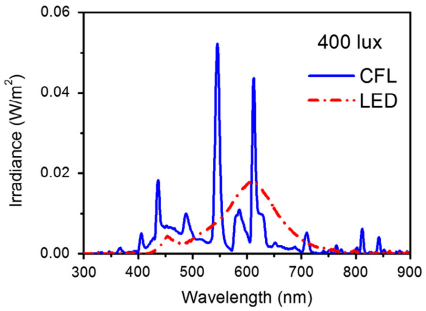

Figure 2.5: Quantitative spectral irradiance of a CFL (Lexman, class A, 39.2 lm/W electrical to optical efficacy) and LED (Lexman, class A+, 62.2 lm/W) light source at 400 lux [44].

2.5.6. PV cells

PV cells are fabricated similarly to photo diodes and electrically behave the same. Voltages produced by a single cell are around the threshold voltage. Combining cells in series increases the voltage but limits the current.

Kirchhoff's law dictates series elements to have the same current through each element, which means that the lowest performing solar cell pulls the current of the entire system down. The opposing case holds for cells in parallel, here the currents are free to differ, but the voltage of the entire harvester is determined by the least performing cell.

Correctly balancing series and parallel connections is thus of the essence to achieve maximum power output at high enough voltages. In the case where one of the cells is receiving no light the effect is most apparent and can result in the entire harvester malfunctioning. In these cases it is often desired to switch a cell completely off from the rest of the harvester. This does however require overhead, which increases power consumption.

Another aspect of harvesting with PV cells is maximum power point tracking (MPPT). The optimal power harvesting happens when the load matches the PV cell, but the impedance of a PV cell changes with irradiance and temperature. The MPPT objective is to actively adjust the load impedance to keep the power conversion optimal. Many algorithms and implementations of MPPT exist, but all require energy to operate and cannot be used for cold start.

The size limitations for wearable/implantable devices do not concern PV cells much, since the devices scale very well. Since it is a CMOS compatible technology, solar cells of square micro-meters are easily made. On top of that, PV cells only require one side to be unobstructed from the light source, allowing for other parts of the system to be on the bottom. Thermal harvesters and RF harvesters do not have this luxury.

2.5.7. Existing PV devices

Research is being conducted in the field of energy harvesting both from the sun and artificial light sources. From the pure perspective of converting light into electricity the advancements are made with adaptations in materials used for PV conversion. This perspective fits the research, as the aim is to characterise the energy source and not the conditioning.

Due to the scalability of PV cells the output power is characterised by power over area. Since the connections between cells can be used to adjust power vs voltage the output voltage is characterised per PV cell. Unfortunately, artificial light sources are most often characterised in lux, making it impossible to give a quantitative description of the source without knowing the exact experimental set-up. For the purpose of this research it is still possible to give a meaningful estimation of power sources using the qualitative sources, as they can be linked to normal world environments.

Indoor lighting often ranges from 200 lx to 600 lx. Outside the sun is the main source. 1 Sun is the often used term for solar irradiance at 1000 $W m^{-2}$ under standardised conditions: at 25°C, a spectral coefficient of 1.5 air mass on a clear day on a surface facing the sun under a 37 degree angle [44]. 1 Sun is comparable to 100 klx. Solar luminance drops to roughly 30 klx in cloudy conditions.

Multiple types of PV cells are characterised in Table 2.4. The most common cells are those made from poly-Si and amorphous silicon (a-Si), designed to harvest solar energy. Sanyo designed an a-Si cell that was made for indoor harvesting. Dyed solar cells (DSC) are cells that utilise dyes to specialise in capturing indoor lighting, where the '8nM I' indicates a specialised type where 8 nmol Iodide is used to create the electrolyte. Copper indium gallium selenide (CIGS) and organic photovoltaic (OPV) are other common PV cell technologies.

Table 2.4: Overview of PV cells metrics under different light conditions, where CFL (Lexman, class A, 39.2 $lm W^{-1}$ electrical to optical efficacy), LED (Lexman, class A+, 62.2 $lm W^{-1}$) and 1 sun (AM 1.5G, 1000 $W m^{-2}$, 25°C) are the sources. All findings are from [44], except the last two, which are from [43]. Note that the last two techniques were measured under 200 lx.

Light source:	**1 Sun**		**300 (200) lux LED**		**300 lux CFL**	
Technique	**Power density** ($mW mm^{-2}$)	**Voltage** (mV)	**Power density** ($nW mm^{-2}$)	**Voltage** (mV)	**Power density** ($nW mm^{-2}$)	**Voltage** (mV)
poly-Si	150	560	40	190	50	220
a-Si Power film	49	1600	13	290	12	280
a-Si Solems	34	800	66	500	75	500
a-Si Sanyo	0.006	850	77	640	91	640
DSC	23	770	55	560	51	550
DSC 8nM I	0.028	750	110	550	120	550
CIGS	0.055	-	(9)	(150)	-	-
OPV	0.015	-	(16)	(350)	-	-

As can be seen in Table 2.4 the energy that can be harvested from sunlight is high, whereas energy from indoor sources is a lot lower. The achieved voltages also indicate that series connections are needed to achieve voltages high enough to overcome the threshold voltages.

2.6. Radio Frequency energy

Apart from PV, another band in the electro-magnetic (EM) domain is of interest to harvesting, namely the radio frequency (RF) band. The RF band is specified from 3kHz to 300GHz. Within this band, the signals from technologies such as Wi-Fi, Bluetooth, GSM, Digital TV, 3/4/5G, FM radio and AM radio are to be found. These signal sources are present around populated areas and can thus provide a reliable source of energy.

First, the available RF energy from sources around the human body are specified in this section. Next, RF harvesters and their characteristics are explained. Last, the specifications of existing RF harvesters are given.

2.6.1. Available RF energy on/in the human body

In [45] measurements were done throughout London at a total of 270 positions defined by the London Underground access stations. The findings are given in Figure 2.6. What can be seen is that on the streets the most energy could be found for GSM signals, around the 900 (GSM900) and 1800 MHz (GSM1800) and that Wi-Fi energy is scarce.

Band	Frequencies (MHz)	Average S_{BA} (nW/cm^2)	Maximum S_{BA} (nW/cm^2)
DTV (during switch over)	470-610	0.89	460
GSM900 (MTx)	880-915	0.45	39
GSM900 (BTx)	925-960	36	1,930
GSM1800 (MTx)	1710-1785	0.5	20
GSM1800 (BTx)	1805-1880	84	6,390
3G (MTx)	1920-1980	0.46	66
3G (BTx)	2110-2170	12	240
WiFi	2400-2500	0.18	6

Figure 2.6: Measurements of RF power density in London by [45]. MTx is the mobile transmit band and BTx stands for the base transmit band.

What is also shown in Figure 2.6 is that the available power is very location dependent, seen by the difference between maximum and average power. [45] also expands on this finding by noting the amount of transmission towers producing above average energy densities in urban and semi-urban regions. The amount of towers in the urban areas is double that of the semi-urban regions.

2.6.2. RF harvesters

RF energy is harvested through the use of antennas. The efficiency of an antenna is determined by the gain and directivity of the antenna in comparison to the isotropic antenna, where directivity indicates the sensitivity of the gain to orientation of the antenna. An isotropic antenna is a theoretical antenna that is insensitive to direction and has no internal losses. The directivity and gain are inherently inversely dependent, resulting in a trade-off.

The gain is greatly determined by the size to wavelength ratio. The optimal length is given by

$$d_{opt} = \lambda/2 = \frac{c}{2f} \tag{2.2}$$

With λ being the wavelength, c the speed of light in vacuum and f the frequency of the signal. For example a common GSM signal at 1800 MHz would require an antenna of 83 mm, too large for this research. Designing antennas of smaller size is possible for this wavelength, but it always comes at a penalty in harvested power.

Common micro antennas are loop shaped, reducing the size needed. The area within the loop is also part of the antenna though and should not be filled with conducting components, as this disturbs the EM waves passing through the antenna and reduces the gain. Therefore using a RF energy harvester requires a space free of other components on both sides, making the total system larger.

2.6.3. Existing RF harvesters

For this research only antennas that are designed to be omnidirectional are considered, since the antenna will constantly move with the wearer and it is not possible to direct the antenna. Common compact antennas are built as rectennas, where the antenna is combined with a rectifier circuit.

Table 2.5: Examples of rectenna's and their aspects. Power is given in dBm, where -20dBm equals 10 µW.

Source	Size	Antenna gain	Frequency	Power in	Power out	Voltage out
[46]	35×34mm^2	0.659dBi	868MHz	-20dBm	2.54 µW	70 mV
[47]	80×60mm^2	8.6dBi	2.45GHz	-20dBm	4 µW	106 mV
[48]	40×33mm^2	-	2.45GHz	-20dBm	1.5 µW	60 mV
[49]	31×49mm^2	-	2.45GHz	-18dBm	2.45 µW	70 mV

2.7. Biochemical energy

One field of energy that actually is more profound inside the body than outside is biochemical energy. The human body gets energy from glucose and stores it as ATP. Both these molecules can be broken down to ex-

tract the energy. Currently three techniques are known to extract electrical energy from glucose: by enzymes, microbial or solid state conversion.

All three of these biochemical harvesters are examined in this section for power and voltage production, as well as feasibility. The section is concluded with the aspect of bio-compatibility of these devices.

2.7.1. Glucose fuel cells

Fuel cells that use enzymes can be extremely small and generate about 4.6 µW with a footprint of 1 mm^2 [50]. The only problem is that the enzymes degrade over time, thus the harvester can last only several weeks.

Microbial fuel cells utilise living micro-organisms to oxidise glucose allowing electrical energy to be extracted. Microbial fuels are quite efficient and can provide 10 $\mu W mm^{-2}$. However, microbial materials are not implantable, as the body reacts badly [50].

The last option is the use of solid state catalysts, which are more bio-compatible and can be stable for up to several months. These fuel cells produce about 10 to 100 $nW mm^{-2}$ at an output voltage of 150 mV [50].

The durability of enzyme fuel cells make standard batteries the more preferred option for now and excludes this type of harvester from the research.

2.7.2. Bio-compatibility

Devices and materials are never fully bio-compatible. A certain time frame must always be mentioned for a specific location and application. For the topic of glucose fuel cells the application and location influence the bio-compatibility greatly. The immune system is easily triggered by non-native users of glucose and will attack those. On top of that a device should not harvest too much glucose so that cells surrounding the device starve. [50] estimates that 1mW can be harvested from the body without harm done. As to prevent attacks by the immune system it is suggested to harvest from cerebrospinal fluids, where the immune system is less present.

2.8. Overview

Now that all energy sources and their harvesters have been explored, it is time to compare them. The harvesters that were examined are:

- Peltier based TEHs
- Pyroelectric based TEHs
- Piezoelectric based kinetic harvesters
- Electrostatic based kinetic harvesters
- Photovoltaic harvesters
- RF harvesters
- Biochemical harvesters

First, it is decided what harvesters are not possible due to their sizes or other physical limitations. These devices are not considered in further comparison. Next, the remaining harvesters are compared by their abilities of power and voltage production.

2.8.1. Physical restrictions

First, biochemical energy will not be used due to bio-compatibility restrictions and the fact that they only operate inside the body. Pyroelectric harvesters are also not be considered further due to the required input being a temperature difference of over 20 °C peak-to-peak in oscillation, which is not expected to be found on the human body.

Some harvesters require exposure to the environment to operate. This can be a disadvantage for further design. Table 2.6 sums up the required exposure per harvester. The KEHs are easiest to place in a system, whereas the TEH and RF harvester require strict placement.

An RF harvester needs its own space in a system, as electrically conducting materials disturb the EM-field. Implementation of the harvester on chip is very limited due to the electrical components present on the chip. The electronic components disturb the incoming energy in the RF domain and significantly lower the efficiency. The human body itself also blocks signals and limits the possible available energy. On top of

Table 2.6: Exposure required for each harvester.

Harvester	Exposure required
Peltier TEH	One side connected to body, One side exposed
PE KEH	None
Electrostatic KEH	None
Photo-Voltaic harvester	One side visual light transparent
RF harvester	All sides RF transparent

that, the shape of the antenna is not free to be bent or reshaped for better system integration, making the design even more limited.

Thermal harvesters do not allow for other system parts to be implemented in the space taken by the TEH, due to the thermal gradients that must be applied on these surfaces. On top of that, one of the surfaces should be in close contact with the body in order to conduct heat from there. For a simple wearable device this thermal connection might be weak due to an air gap. The shape of the TEH would ideally follow the body to maximise surface contact. However, most TEHs are stiff and are not suited for this task. On the other side of the harvester a high surface to mass ratio is desired to lose heat, which limits the system design of other parts around the harvester.

The kinetic energy harvesters stand out for the minimal required exposure. Both techniques can be constructed using MEMS technologies and thus a box is required somewhere in the system. Around this box the design is free of limitations.

The PV harvester can be made on top of the active circuit or anywhere else that is at the surface facing light. The shape is free to be chosen, as multiple smaller PV cells can be connected to form one large PV cell.

2.8.2. Achievable power and voltage

Taking into account the scenarios in which the device will be used on the human body, an estimation of the achievable power and voltage for certain sizes is given in Table 2.7. For each harvester certain assumptions are taken and certain aspects need to be noted.

Table 2.7: Comparison between harvesting techniques on their size, power and voltage aspects.

Harvester	Size range	Power range	Voltage range
Peltier TEH	1 to 35 mm^2	66 nW to 17.2 µW	800 mV to 1.6 mV
PE KEH	10 cm^2	70 µW	310 mV
Electrostatic KEH	8 to 400 mm^2	2.5 to 700 µW	2.8 V to 42 V
PV harvester outside	1 to 400 mm^2	5.8 mW to 2.3 W	400 to 1000 mV
PV harvester inside	1 to 400 mm^2	12 to 120 nW	220 to 640 mV
RF harvester	12 to 15 cm^2	1.5 to 2.5 µW	60 to 70 mV

The thermal harvesters are assumed to operate under a static temperature difference of 4 K. As noted in the section on thermal harvesters, the amount of power available is inversely proportional to the available voltage. This is visualised in the table by having the power range from lowest to highest and the voltage from highest to the lowest value.

The PE KEH has only one value, as only one source used an input signal that is close to that of expected human motion. The used harvester is from [30], which uses an input oscillation of 1g at 4Hz, which assumes the harvester to be in motion.

Electrostatic KEH are more tuned to human motion in most researches, although still at the higher end of the spectrum (10-20Hz). This again indicates that the harvester must be in motion to reach these values. It must be mentioned that the high voltages will cause more unwanted capacitive coupling in devices.

The PV harvester is split in outside and inside performance. Outside is taken as the assumption that a person spends one hour outside in sunlight in the Netherlands, this ends up to be an irradiance of 39 $W m^{-2}$, as explained in Subsection 2.5.4. For the inside case a 300 lx fluorescent lighting is taken as commonly seen in offices.

Lastly, RF harvesters are taken in the Wi-Fi and GSM900 band.

2.9. Conclusion

From Subsection 2.8.1 on the sizes and shapes of the harvesters it can be concluded that RF and thermal harvesters are undesirable for small and integrated systems. From Table 2.7 it can also be seen that RF harvesters must be made quite large. So, both RF and thermal harvesters will not be used.

The piezoelectric harvester is also of greater size, although it is expected that smaller sizes are possible. Due to the higher frequencies required for reliable output these devices are also not chosen.

Both the electrostatic and photovoltaic harvesters seem suitable as harvesters for a wearable device. They have the sizes that are acceptable and can deliver voltages in higher ranges. The electrostatic harvester has the downside of voltages being very high and the frequency dependence on power production. The PV system produces very little power indoors and depends heavily on available light.

For implementation of the electrostatic KEH, a system that can handle the high voltages is needed and will be challenging to design. Techniques to widen the oscillation frequency are most certainly needed. The output signal of a KEH is highly variable. Production of these devices is challenging, especially with the needed pre-charge.

Implementing the PV harvester brings the challenge of very little power output when indoors, while at the same time handling high power influx in bright sunlight. On top of that, MPPT should be designed for the operation outside of cold-start and maybe even during cold-start. PV modules are widely available and relatively easy to produce.

In the end, the PV harvester is seen as the best candidate for energy harvesting on the human body. The promise of very high outdoor power provision is great and the independence of resonance frequency is a major advantage for reliability. On top of that, KEHs require MEMS production and high voltage tolerant electronics, which makes the device costly to produce and less reliable.

3

Background information on cold start

Starting devices from an energy depleted state (called cold start) is of growing importance to energy harvesting as it guarantees autonomy for energy harvesters. Especially smaller applications in harder to reach locations benefit from this autonomy. The targeted application of a wrist worn device benefits from cold start capability as well. To design an optimal cold start compatible energy harvester, the already existing solutions must be understood and are discussed in this chapter.

The chapter starts with the explanation of cold start circuits and why they are needed. After that, the possible topologies for implementing cold start are examined. Next, each major component of a cold start circuit is examined and the state of the art is given. Lastly, an overview of the components and their specifications is given.

3.1. Introduction

To understand the requirements for cold start, a better understanding of the normal harvester topology is needed. In Figure 3.1, a schematic overview of the harvester circuit is given with its common components visualised. The source is modelled based on the actual energy source and transducer that will be used. A voltage booster is almost always needed, as the voltage from a transducer almost never matches the voltage required on the storage element.

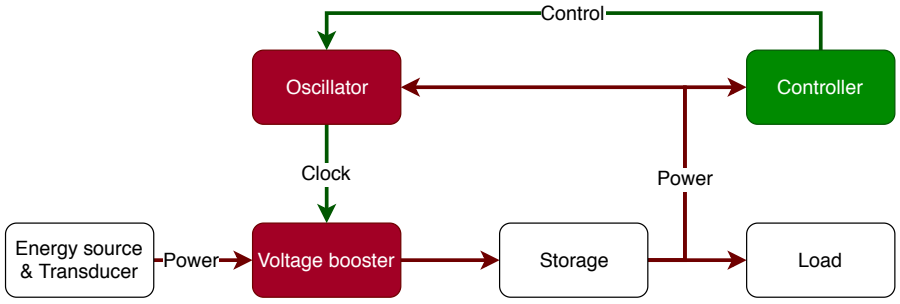

Figure 3.1: Schematic overview of the general components in an energy harvester.

The voltage booster needs to be driven by clock signals provided by the oscillator. The oscillator requires energy to generate this clock signal. However, the oscillator does not operate if there is no energy stored and therefore the booster operates neither. If the booster is not operational, the storage element is not refilled and thus the system is stuck.

3.1.1. Cold start circuit

A cold start circuit is needed to drive the voltage booster with a depleted storage element. The cold start circuit kick-starts the system, after which it can sustain itself. The simplest implementation would be to use the source signal to drive the booster. However, the source often provides too low voltages to drive the booster in the first place. One solution to this is utilising a mechanical switch as presented in [51]. The mechanical

switch is used for the initial cold start and is activated by random motion. From a theoretical point of view a different energy domain (the mechanical domain) is here used for its higher impulse capability. However, after cold start the mechanical switch is still present in the circuit and can inhibit operation. Also, this method only works for inductive boost converters, which are generally not integrated. Lastly, this approach cannot be applied where there is no mechanical energy available.

Other approaches often seek the use of transformers [52–54], having the advantage that high efficiency can be achieved after cold start with the same transformer. However, inductors and transformers form large components that are not compatible with desired form factor and produce magnetic fields that can interfere with other chip components. An interesting solution to this problem is the piezoelectric transformer presented in [5]. Unfortunately, the transformer is still large and not integrated. An integrated inductor could be used, as was done in [55]. Although cold start can now be achieved, the efficiency when out of cold start is severely limited due to the low quality factor of the integrated inductor. A second external inductor would be required for efficient harvesting, raising the question of why the inductor was integrated in the first place. Therefore, the focus is shifted to integrated cold start compatible systems that do not utilise inductors.

The solution lies in the electrostatic domain, using charge pumps and low power oscillators. Charge pumps are switched capacitor circuits that are easily integrated and can provide highly efficient conversion [4, 7, 56]. Charge pumps are examined in more detail later in the chapter. An oscillator is needed to drive the charge pump. Figure 3.2 gives a system enriched with the cold start circuit.

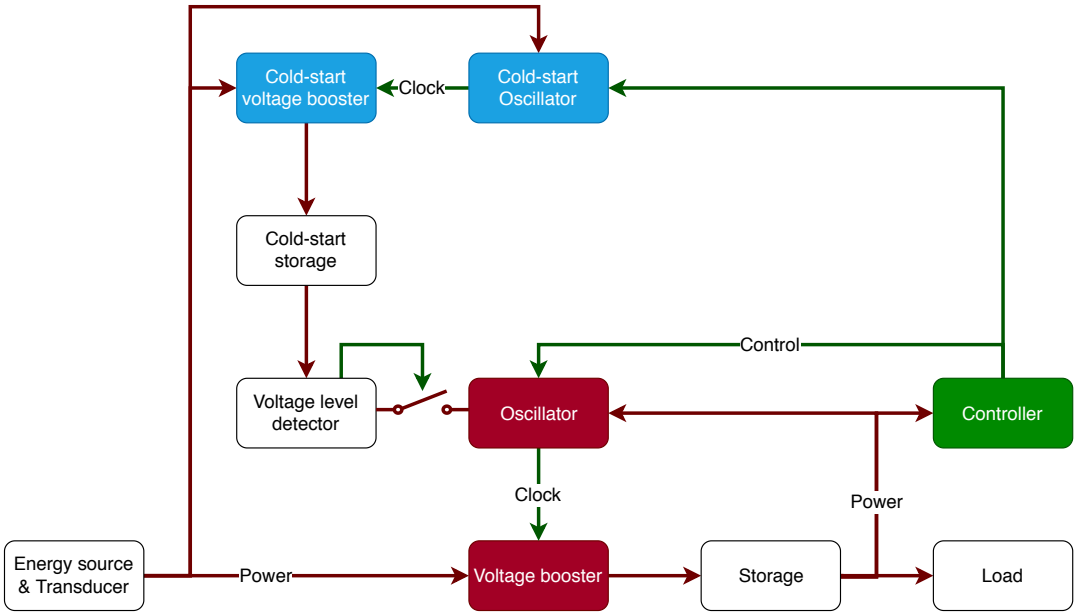

Figure 3.2: Schematic overview of the general components in an energy harvester with cold start circuit.

Most cold start systems do not reach the required reliable output voltages instantly, since the source is unpredictable and cold start conversion often has low efficiency. Therefore an intermediate storage element is used that can store the energy acquired by the cold start circuit. If the main booster is always connected to this storage element it will constantly drain energy from it, thus posing a higher load for the cold start system. Another component is needed for the cold start circuit that determines when there is enough voltage available to reliably start the main booster and prevent leakage before that moment. The component needed is a voltage level detector and a switch. The voltage level detector determines if the correct voltage is reached and the switch prevents energy flow before that point is reached.

With the needed components known, the cold start circuit can be examined in more detail. Based on these findings a suitable system approach can be chosen.

3.2. Topology

The first aspect to decide on is the topology of the top-level for connecting the cold start circuit (CSC). The oscillator and booster of the main harvester can be taken as one block for this purpose. The same is done for the CSC. Similarly, the storage elements and their voltage level detectors are combined in one. At top-

level, six blocks can be distinguished: the source, the main storage element, the cold start storage element, the main harvester, the CSC and the controller. The latter three need to be powered and controlled. The choice of connecting power to these blocks is of importance to their operation and performance. A set of possible topologies that differ on these aspects will now be examined. All major topologies are given in Figure 3.3. Topologies not shown are combinations between the given topologies. Note that the Harvester block is powered from the top arrow and converts energy from left to right.

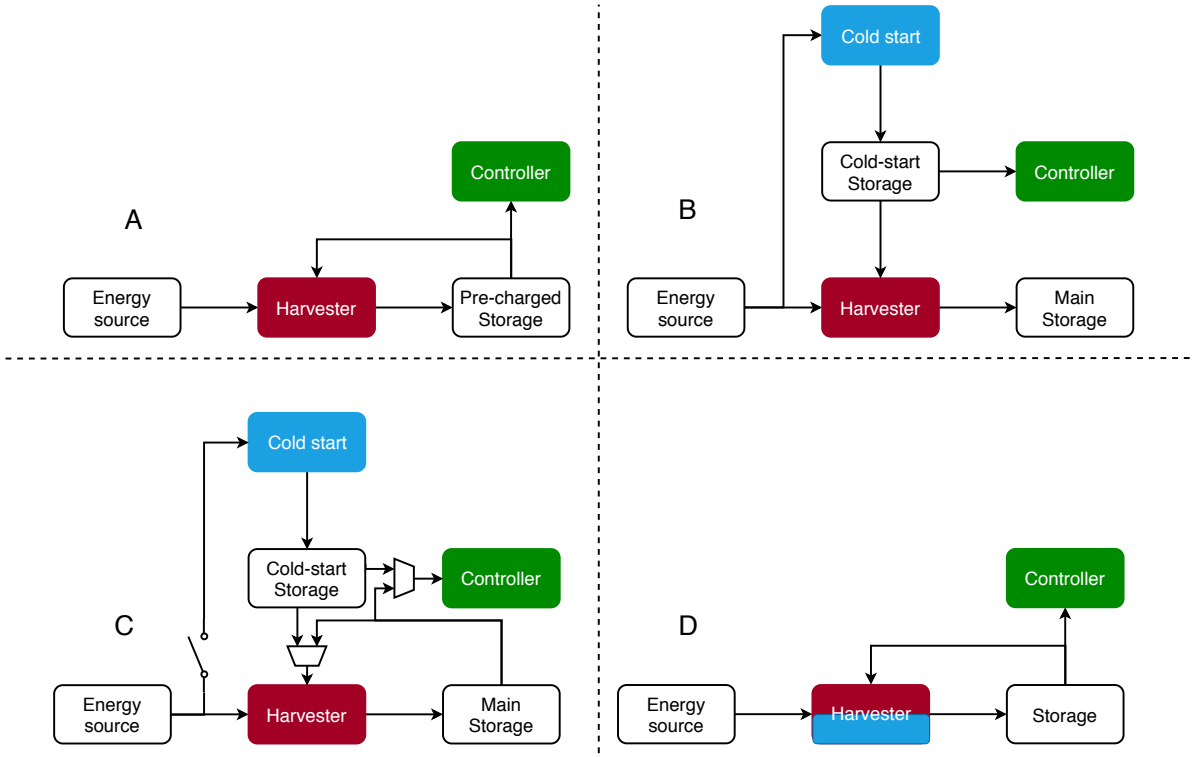

Figure 3.3: Overview of possible cold start topologies. The arrows indicate flow of energy and the trapezoids are multiplexers. The control signals for the multiplexers and switch are not drawn, but are driven by the controller. Note that the harvester block is powered from the top arrow and converts energy from left to right.

3.2.1. Examination of topologies

Topology A Topology A might not seem like a cold start solution, but this topology is actually applied often. The important feature is pre-charging the storage element and assuming it to never run out of energy, due to continuous harvesting. These prerequisites are undesirable, as pre-charging every system induces a new step in production and there is no recovery from having the system depleted. These are the major reasons for having cold start circuits to begin with.

Topology B The next logical step is to introduce the CSC and utilise it to drive the controller and main harvester, as given in topology B. In order to perform cold start that does not rely on the main storage element having energy, the main harvester must be connected to the CSC.

Another advantage is during low power conditions. The main harvester might not be able to effectively harvest any power in low power conditions. Disconnecting the main harvester in this case saves energy of the main storage element. Shutting down the main harvester implies that starting it up again when power levels rise is required. Starting up the main harvester consumes extra power compared to being already running. This effect is especially disadvantageous if the power levels fluctuate around the shut-down point and the harvester is shut down and started up repeatedly. Instead of shutting down the harvester, the CSC can be used to keep the other components in a sleeping mode, where starting up consumes less energy as the system is already energised.

After cold start the CSC is still used to drive the main harvester, which will likely lead to less efficient harvesting and less control possibilities.

A sub-topology would arise by connecting the controller to the main storage element instead, but it would then only operate after cold start. This topology has the advantage of not draining energy by the controller during cold start. On the other hand, having the controller always connected to the storage element drains the storage element even when the controller has nothing to do.

Topology C To take full advantage of the possibility to divert all power through the main harvester in normal operation, a switch to disconnect the CSC from the source is needed. One point of interest is that now the controller must also be powered by the main storage element, since the CSC does not provide any further power when switched off. In this topology the CSC is only utilised during cold start or sleep mode. The main harvester is now also powered by the main storage element after cold start, making more efficient harvesting and more control possible.

The controller must be designed carefully for this topology, as overlap between phases can lock the device. If the controller disables the CSC before connecting itself to the storage element no energy is provided to the controller and the system becomes unstable. An easy solution would be to have the controller only powered by the main storage element and never by the CSC. No control is then possible in cold start.

Topology D In topology D the harvester is adapted to be cold start capable. After cold start the harvester should be altered automatically to support more efficient harvesting. This concept could be realised by changing the topology of the harvester or by combining multiple smaller harvesters. These smaller harvesters can then be designed to operate in cold start when needed, or (partially) combined to form an efficient harvester. With inductive harvesters, applications that share the inductor for cold start and normal operation exist. For electrostatic harvesters this has not been found yet. Cold start compatible charge pumps provide at best half the conversion efficiency that can be achieved with other charge pumps (that are not cold start compatible). Nonetheless, from a system point of view this is a possible topology that simplifies the power path and reduces the size of the system.

This approach requires quite some overhead and a harvester design that is both low-power and power efficient. Especially the latter is an issue, as compromises must be made between efficiency and low-power operation. The CSC and main harvester also share the same storage element, thus simultaneous operation is not possible. The CSC has to store enough energy on the storage element for the main harvester to start before the harvester is converted from cold start operation to normal harvesting. Thus, two different voltage level detectors are needed; the first to activate the main harvester and a second to apply the load once the main harvester is self-sustaining.

3.2.2. Conclusion on topologies

From the given topologies a couple of desired advantages come forward. First there is a need to cold start the system, thus a passive path through the CSC to the main harvester is needed. Secondly, preserving energy on the storage element can be achieved by having the CSC providing power to the other components, especially during low energy situations in which the main harvester is disconnected. Lastly, during normal operation the CSC can be taken out of the energy loop, as the main harvester is more efficient. To do so, the controller must also be powered from the storage element in this mode of operation.

Topology C can provide all these requirements. Connecting the controller solely to the main storage element reduces strain on the CSC and prevent lock-up. The only downside is loss of control during cold start, but since the CSC is only a kick-starting device, efficiency is not of major importance and the loss of control is accepted.

Topology D can provide these desires as well, except for the sleeping mode. A trade-off between area and sleep mode capability is thus made. If a charge pump can be found that is both highly efficient and cold start compatible the area reduction will be a great improvement. Especially for integrated circuits reduction of silicon area is always of interest as it lowers production costs.

3.3. Oscillators

A. Tasic gives the following definition of oscillators: "*An oscillator is a tunable circuit that generates a stable periodic signal, which is in the limit independent of the original conditions* [57]". The 'stable' and 'independent of the original conditions' aspects are most important for cold start applications. A stable signal has sufficient amplitude to drive other components and independence means that an unstable input generated by the source can be handled. The general harvester design requires two oscillators: one that drives the main

booster (main oscillator) and one charge pump dedicated oscillator (cold start oscillator). Both have different design requirements. For the main oscillator, high efficiency and controllability are of essence, since the main booster must achieve maximum efficiency. The cold start oscillator main requirement is starting capability from low voltage and low power consumption.

This section is dedicated to the cold start aspects of oscillators, as the focus of this research is on the cold start circuit. The most important cold start oscillator metrics are: the ability to start from a low and unstable input voltage, low power consumption, sufficient amplitude to drive a charge pump and independence of input signal variation at the limit. Three types of oscillators are examined: LC oscillators, relaxation oscillators and ring oscillators. These are the three main oscillator topologies to date and are second order, first order and nth order oscillators respectively. Many subtypes exist and some are highlighted.

3.3.1. LC oscillators

Inductor capacitor oscillators (LC oscillators) are one of the earliest oscillators to be invented. The design is based on the use of a resonator and a gain producing element providing positive feedback. Due to the gain element the LC oscillator is also known as negative resistance oscillator. The resonator is often created by use of a LC tank that creates an exchange of energy between the inductor and capacitor element. The gain element is needed to compensate for losses in the LC tank, so that there is always energy to continue the oscillation. LC oscillators are second order oscillators, due to their harmonic nature.

The performance of LC oscillators is mainly determined by the quality factors (Q factor) of the inductor and capacitor. Creating these components in IC technologies with high Q factor is difficult and consumes a lot of space. Especially inductors do not scale well. Apart from that, LC oscillators are capable of starting from a low voltage and consume little power. The active (gain) part of the oscillator is often implemented by a transistor. This transistor needs to also operate from low supply voltages and common techniques to lower the switching voltage are thus applied. Some of these techniques are mentioned in Subsection 3.3.3.

Meissner oscillator Certain topologies of LC oscillators allow for properties of interest to cold start. One of these topologies is the Meissner oscillator. The Meissner oscillator allows for an increase in amplitude while still providing oscillation on a small footprint [58]. The Meissner oscillator consists of a transformer and one switch as can be seen in Figure 3.4. The transformer allows for higher voltages to be produced at the secondary side. The primary side forms the actual LC oscillator, together with a capacitor and switch.

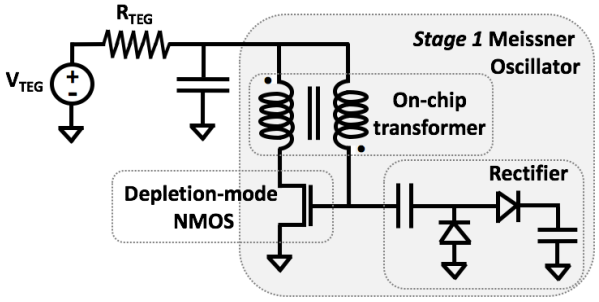

Figure 3.4: General structure of a Meissner oscillator, in this case driven by a thermal energy harvester [55].

The main issue with the Meissner oscillator is the need for a transformer. Transformers do not scale well and are thus either bulky or come with low Q factor. On chip magnetics provide roughly three decades lower inductances than their off-chip counterparts [55]. An alternative to the inductive transformer is proposed by A. Camarda *et al.*, they propose the use of a piezoelectric transformer that achieves a high Q factor at small dimensions (10×30 mm^2) [5]. With such a transformer, input voltages as low as 15 mV are sufficient to start oscillation. Although the size reduction of the piezoelectric transformer is significant, it is still not at an integrated level.

3.3.2. Relaxation oscillators

Relaxation oscillators do not use a resonator, but instead rely on a storage element that is periodically charged and drained by a switch. The waveform produced by such an oscillator is non-sinusoidal, but often triangle or square wave shaped. For the purpose of driving a charge pump this is fine; the square wave is even preferred

as clock signal. Most relaxation oscillators operate at voltages of 600 mV and above, too high for cold start purposes. On top of that, losses in relaxation oscillators with realistic components are often in the micro-watt range, which is barely delivered by the expected harvester. Thus, requiring micro-watts for the oscillator alone reduces the total efficiency of the system severely. The charging and emptying of one element leads these oscillators to be of the first order.

A dual phase current mode relaxation oscillator by S. Dai *et al.* achieves oscillation at 400 mV and consumes 4.2 nW [59]. The design of this oscillator allows for frequency control by means of a voltage, which is used to perform maximum power point tracking. E. Ferro *et al.* tunes the same oscillator design to achieve oscillation at 270 mV for 15.6 pW power consumption [60]. This shows that relaxation oscillators are feasible for cold start applications at voltages around 300 mV, too high for the desired cold start capability. Development of relaxation oscillators might lead to implementations for cold start applications in the future.

3.3.3. Ring oscillators

As technology advanced the cost and size of transistors reduced beyond that of passive components, leading to a different approach to oscillators consisting of only transistors. The most basic design is the ring oscillator. A ring oscillator is based on a line of inverters connected in cascade, where the last inverter is connected to the input of the first inverter, forming a ring. Due to the switching delay of each inverter a periodic signal is generated when an odd number of inverters is used. Each inverter adds one more order to the system and ring oscillators are therefore nth order oscillators, where n is greater than two. A general topology of a ring oscillator and one inverter block is given in Figure 3.5.

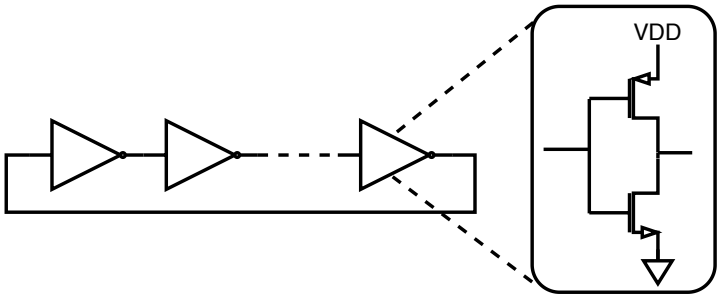

Figure 3.5: General ring oscillator topology with one inverter block given. The number of inverters must be odd for oscillation.

The great advantage of ring oscillators is the absence of any large components; only transistors are needed. The disadvantages are mainly in power consumption. The swing of each inverter is reduced when only low voltages are available. An inverter that is not driven with a full swing leaks current from the top to bottom. Passing the transistor threshold voltages with enough margin ensures low switching losses. Therefore multiple manners of lowering the threshold voltage have been proposed. P. Chen *et al.* uses hot carrier injection in a post-fabrication process to tune the threshold voltage [2]. This method does however lower the yield and increases the cost of production. J. Goeppert and Y. Manoli implement schmitt triggers to lower the required voltage and achieve oscillation from 60 mV [61]. D. Mohammadjavad *et al.* proposes a process invariant inverter that operates in all process corners [62]. This is of interest to low voltage operation as process variation effects can be greater than nominal operation parameters. Lastly, [3] uses forward body biasing to lower the voltage needed to trigger the inverter, but this does come with process variation problems.

Inductive load ring oscillator (ILRO) One adaptation to the ring oscillator can be made by using inductors instead of the PMOS transistor for each stage of the ring oscillator. This technique reduces the required start-up voltage by half and allows the oscillator to boost the voltage above the supply [1]. The topology is given in Figure 3.6.

The lower required start-up voltage and boosting capabilities come at the expense of the need for inductors. A common compromise is to implement a two stage ILRO. The compromise only requires two inductors, but still allows for boosting and reduced start-up voltage. In essence a LC oscillator is made in this case and thus the advantages and disadvantages are the same.

Bootstrapping A relatively simple circuit can be utilised to double the amplitude of a ring oscillator. The circuit is drawn in Figure 3.7 and is a bootstrapping circuit.

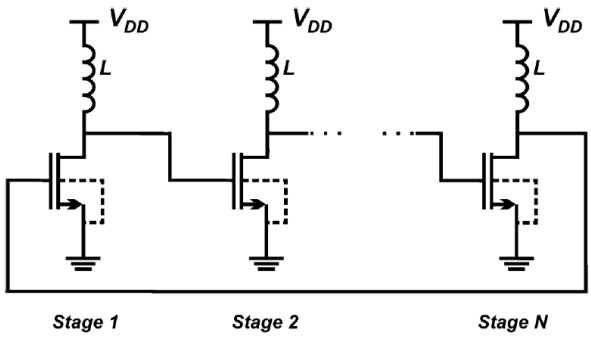

Figure 3.6: Schematic of an Inductive Load Ring Oscillator (ILRO) with N stages [1].

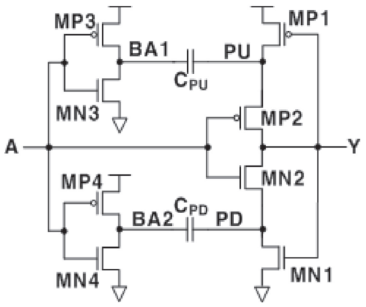

Figure 3.7: Bootstrapped inverter for ring oscillator [63].

The main inverter is formed by MP2 and MN2. MP3 and MN3 form an inverter that boosts the voltage on the upper capacitor together with MP1. The lower capacitor receives a boosted voltage similarly by MP4, MN4 and MN1. The boosted voltage is supplied to the main inverter, which thus operates from twice the supply voltage.

A more compact design is proposed by M. Hasan-Sagha and M. Jalali that uses only one transistor together with a capacitor to provide the boosted supply voltage for the main inverter [64]. Boosting the voltage comes at the cost of an increased leakage current and discharge current of the inverter cells. For cold start purposes the power losses must be weighed against the gained voltage.

3.3.4. Conclusion on oscillators

LC oscillators can achieve oscillation from the lowest supply voltages, capable of operating from 15 mV and up. Next, the ring oscillators operate from voltages of 50 mV and above. Lastly, the relaxation oscillators require at least 270 mV to operate. LC oscillators also allow for higher output voltages than input voltages, which is a huge advantage for cold start applications. In the sense of power consumption all oscillators are within the same league, around pico- to nano-watt consumption.

The required components for LC oscillators are a major drawback, as they are the largest compared to other oscillators. Scaling these components is possible, but comes at great costs in quality. Relaxation oscillators face similar problems. The ring oscillator is the best scalable and requires no passive components, making them desirable for integrated applications. The switching losses of ring oscillators increase with low voltage operation.

3.4. Voltage boosting

Similar issues for fully integrated oscillators are found for fully integrated voltage boosters. Using inductive elements lead to far more efficient boosters with high conversion ratios. However, inductors do not scale well and a fully integrated system using inductive elements is easily out-performed by fully integrated capacitive voltage boosters. Therefore, this work focusses on capacitive voltage boosters, as a design requirement is full integration.

3.4.1. Charge pumps

As the name suggests, a charge pump moves charge around. Pumping charge allows for charge build-up at an end point, which manifests as a higher voltage in the circuit. Energy transducers often present a voltage that is too low to charge a battery with and thus boosting is required. Charge pumps are a sub-family of the switched capacitor circuits. Multiple topologies of charge pumps exist, each with their own advantages and limitations.

The section starts with general switched capacitor networks after which the most basic charge pump is introduced. Next, some modified charge pumps are looked at that solve known issues with charge pumps. After that, the area taken by charge pumps is examined. In the end, the most favourable charge pump for cold start is chosen.

3.4.2. Switched capacitor converters

All switched capacitor converters utilise capacitors, switches and a clock signal to operate. The capacitors are connected in multiple topologies utilising the switches. Two connected capacitor plates distribute their charge equally and can thus be used to move charge around. The simplest example is a voltage doubler given in Figure 3.8.

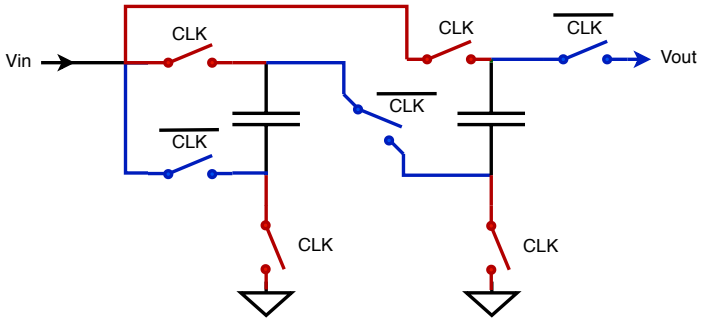

Figure 3.8: Switched capacitor voltage doubler. The charging phase is corresponds with a high *CLK* signal, the boosting phase corresponds with a low *CLK* signal.

Two phases of operation can be distinguished in Figure 3.8, indicated by the red and blue conduction paths. In the charging phase (red path), the clock is high and the capacitors are connected in parallel to the source. Both capacitors are thus charged to V_{in}. When the clock becomes low, the boosting phase starts (blue path). The capacitors are connected in series from the source to the load. The voltage that is present between the capacitor plates is thus stacked and the output voltage is the sum of the stacked capacitor voltage and the input voltage. This operation can be expanded with more capacitors and is also called a series-parallel charge pump.

Many creative designs are possible with this principle. It is easy to combine more capacitors and different switch configurations to enable higher boosting and even modular boosting [56, 65–67]. A common practise is also to create two opposing branches in anti-phase to ensure the output voltage is constant and not a square wave [68].

The major challenge with these devices is producing the correct clock signals and implementing the switches. As can be seen by inspection of Figure 3.8, a short circuit is created when the clock signals overlap. Also leakage through the switches when they are off lowers the efficiency. On the other hand, the on-resistance of the switches must be minimal to ensure low losses from dissipation.

3.4.3. Makowski charge pump

One approach to the series-parallel charge pump of interest is the Makowski charge pump [69, 70]. The same topology is used as before, but the switches are driven by a multiple phase clock signal. The general idea is to not put all capacitors in parallel during the charging phase, but to charge a capacitor by the boosted voltage of its predecessor. The operation of a two stage Makowski charge pump is illustrated in Figure 3.9. The clock signals should be strictly non-overlapping to prevent losses.

More stages can be used to achieve higher conversion ratios. However, each new stage requires one more clock phase to be added. The resulting steady-state output voltage of a Makowski charge pump is:

$$V_{out} = \frac{V_{dd}C}{C + C_{par}} \cdot 2^N - N \cdot \frac{I_L T_{clk}}{C + C_{par}} \tag{3.1}$$

Where V_{dd} is the clock amplitude, C is the capacitance of one stage, C_{par} is the parasitic capacitance of one stage, N is the number of stages, I_L is the load current and T_{clk} is the clock pulse width.

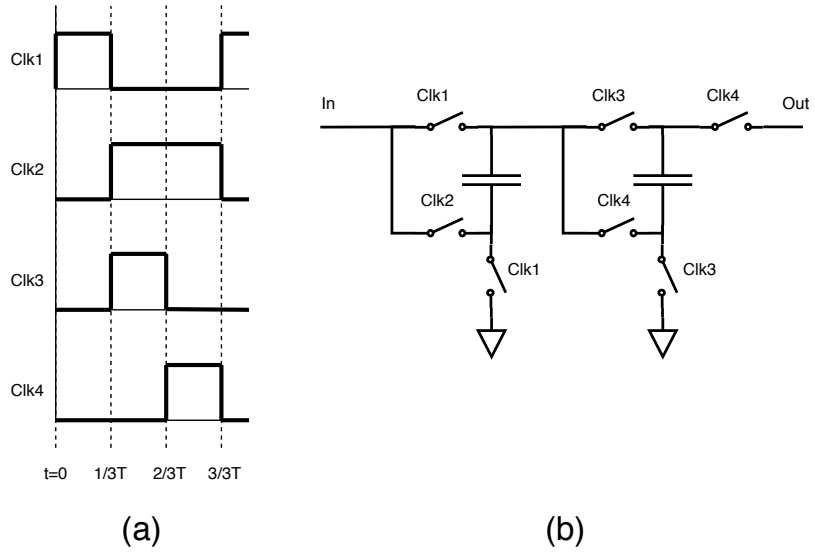

Figure 3.9: (a) Makowski timing scheme for a two-stage converter. (b) Two stage Makowski charge pump schematic.

The Makowski charge pump provides high conversion ratios for a small number of stages due to the exponential dependence of the output voltage on the number of stages. An elaborate oscillator to operate the pump is required, which makes the implementation more challenging. The switches must also be implemented carefully and should be driven with a large swing. The Makowski charge pump offers high efficiency voltage boosting with minimal required stages.

Maximum efficiency Switched capacitor circuits have an inherent maximum achievable efficiency, due to so called switching losses [71]. The maximum is caused by the difference between the ideal output voltage and the maximum voltage that can be obtained by the load. The maximum achievable efficiency is then given by:

$$\eta = \frac{V_{out}}{N \cdot V_{in}} \tag{3.2}$$

Where V_{out} is the maximum load voltage, V_{in} is the input voltage and N is the conversion ratio. So even for a lossless converter the efficiency may not reach 100 percent. Therefore, for a good design the conversion ratio is chosen such that the ideal output voltage and obtainable output voltage match.

3.4.4. Self controlling charge pump

A manner of avoiding active control is utilising a self-regulating switch: the diode. The general structure for a charge pump using diodes is given in Figure 3.10 and is called the Dickson charge pump. The pump works on a two cycle basis. To start, the first capacitor is connected to the source through the first diode and charges up to the same voltage level as the source minus the threshold voltage of the diode. Next, the bottom plate of the capacitor is charged by the clock signal, making the potential at the top plate rise above the source potential. Due to the diodes, the charge from the first capacitor now flows into the second capacitor. This repeats for the second capacitor and on. The final capacitor is simply connected to ground and acts as a buffer for the pump.

The major advantages are the simplicity of the scheme and not requiring active control. It is also easy to control the amount of voltage increase by adjusting the clock amplitude and the amount of stages. The effective voltage gain in the pump is limited by the threshold voltage of the diodes, as given by the following expression:

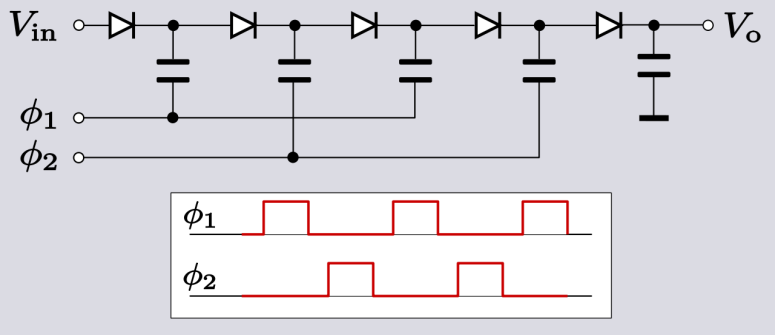

Figure 3.10: Dickson charge pump structure with timing scheme. The last capacitor is an output capacitor and is not part of the pump its [72].

$$V_{out} = V_{in} + N(V_{clk} - V_D) \tag{3.3}$$

Where N is the number of stages, V_D is the diode threshold voltage, V_{clk} is the clock amplitude, all diodes are considered equal and the clock amplitude is equal to the input voltage at V_{in}. The threshold voltage in this equation implies that no current flows below this voltage. However, diodes implement a exponential voltage to current relation and thus a minor current does flow below the threshold voltage. These sub-threshold currents are so low compared to the load current that must be provided that their contribution is neglected with respect to the achievable output voltage.

The major concern with the basic pump is the threshold voltages of the diodes, the leakage current of the diodes and creating the clock signal. The clock signal creation was already covered in Section 3.3 on oscillators. The power delivery in this circuit comes from the clock signals that are often buffered. More details on the diode threshold voltage are given next.

3.4.5. Dickson charge pump aspects

As can be seen from the operation in Figure 3.10 it is essential that the diodes do not leak charge backwards, as this compromises the entire pump. One simple first step is to use diode connected transistors, as they have lower reverse current leakage. Another advantage of not using diodes is avoiding the use of a different masking step for diode creation in fabrication.

The output voltage now depends on the threshold voltage and voltage ripple as given by Equation 3.4 from [73].

$$V_{out} = V_{in} + \sum_{i=1}^{N} \left(\frac{V_{dd} C_i}{C_i + C_{pi}} - \frac{I_{li} T_{clk}}{C_i + C_{pi}} - V_{thni} \right) \tag{3.4}$$

Where V_{thni} is the threshold voltage of the transistor in one stage, V_{dd} is the amplitude of the clock signal, C_i is the capacitance of one stage, C_{pi} is the parasitic capacitance of one stage, I_{li} is the load current per stage and T_{clk} is the clock period. For most standard designs all capacitors and transistors are equal and the clock has the same amplitude as the input voltage. In this case the transfer simplifies to:

$$V_{out} = V_{dd} + N \left(\frac{V_{dd} C}{C + C_p} - \frac{I_l T_{clk}}{C + C_p} - V_{thn} \right) \tag{3.5}$$

The first term between the parentheses is the added voltage for each stage by the clock. The added voltage is reduced slightly by parasitic capacitance, but the other terms are more dominant. The second term within the parentheses represents the voltage ripple at the output, which is reduced for a smaller load current, a larger load capacitor or a faster clock signal.

Transistors also conduct current when in sub-threshold. However, these currents are so small that they are dissipated by small resistances that are normally neglected when designing a circuit. The sub-threshold currents also form a negligible part compared to the load current and are thus not explicitly shown here.

3.4.6. Back bias effect

As can be seen from Equation 3.4 the threshold voltage is a limiting factor for the pump. If the threshold voltage is above the input voltage there will be no pumping to begin with. In the traditional configuration the bulk of the transistors are connected to ground and thus the body effect is observed as described by Equation 3.6, adapted from [73].

$$V_{th} = V_{th0} + \gamma(\sqrt{V_{SB} + 2|\phi_F|} - \sqrt{2|\phi_F|}) \tag{3.6}$$

Here V_{thn0} is the threshold voltage without body effect, γ is the body effect coëfficient, V_{SB} is the source bulk voltage and ϕ_F is the Fermi potential.

The voltage on all terminals but the bulk terminal increase for each stage. The body effect thus grows stronger at later stages, decreasing the efficiency as more stages are used. This effect is known as the back bias effect.

Multiple manners of reducing the body effect have been developed. Starting in 1997, K. Choi *et al.* proposed to use a floating well as the bulk, but undefined nodes in a circuit lead to substrate currents affecting other parts on the chip [74]. K. Choi *et al.* also proposed connecting the source to the bulk. For applying this technique in current day technologies a transistor with a bulk separated from other devices in the substrate is needed. These devices thus take more space. J. Shin *et al.* proposes the use of auxiliary MOSFETs to actively control the bulk voltage [75]. However, the active bulk control can lead to substrate currents, degrading the rest of the chip. Again a separated bulk is needed. H. Lin *et al.* uses four clock phases to reduce the effect, which comes at the cost of having a more complicated and power hungry clock generator [76]. Another scheme that requires a more complex clock generator is proposed in [77], where charge sharing is introduced.

The easiest and most promising technique remains connecting the source to bulk. To this purpose deep N-well transistors are needed, or PMOS transistors must be used, as the latter is always produced with a separate bulk.

3.4.7. Charge transfer switch

An even better output voltage can be reached by completely removing the threshold voltage from Equation 3.5. J. Wu *et al.* introduced charge transfer switches (CTS) to this goal [78]. The charge transfer switch is an additional transistor that is placed in parallel with the diode connected transistor. The gate is connected to the potential of a later stage, where a higher voltage is available. The general structure is given in Figure 3.11. The gate-source voltage can now stay above the threshold voltage, as long as the later stage has high enough potential. The improved gate-source voltage allows for conduction even when the drain voltage reaches the source voltage. The diode connected transistors are still needed to create the initial charge on the later stages that drives the CTS.

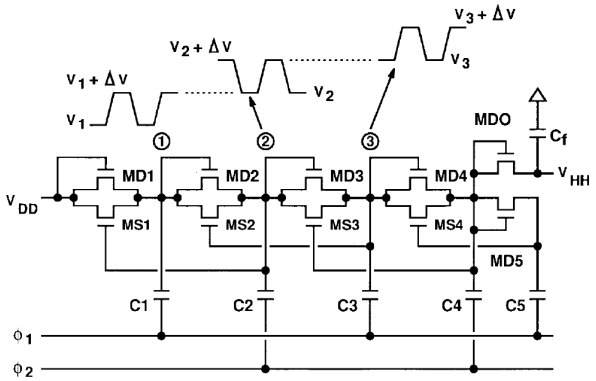

Figure 3.11: General structure of a charge pump using charge transfer switches, with the signals at each node indicated. MDx are the diode connected transistors and MSx are the charge transfer switches [78].

Dynamic Charge Transfer Switch One major drawback in the CTS design is the reverse current leakage, as transistors are bi-directional devices. The ideal gate-source voltage is now at twice the clock amplitude for each stage. The voltage on the gate of the CTS is kept high enough to boost during the first phase, but is not dropped low enough during the second phase. To provide this lower potential dynamic CTS are proposed

[78]. Dynamic CTS build on the previous design, but implement an inverter that connects the gate of the CTS to either the preceding or following stage, depending on the phase. The resulting design is given in Figure 3.12.

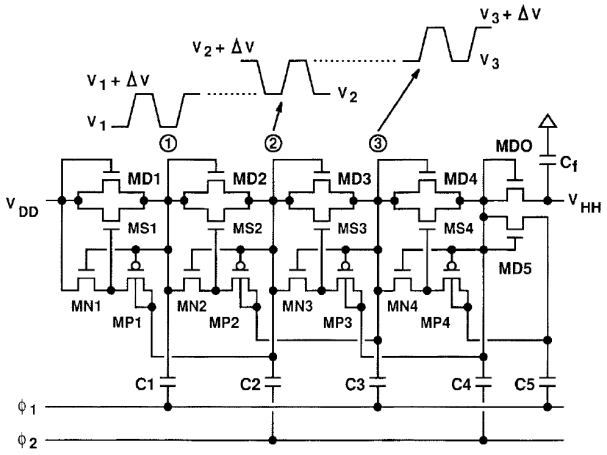

Figure 3.12: Adjusted charge transfer switch charge pump design to incorporate dynamic charge transfer switching [78].

Final stage The last limitation with this charge pump is the last CTS stage that cannot be driven by a higher node, and thus still suffers the back bias problem. A solution would be the use of a cross-coupled CTS as the last stage, as proposed by [79]. The last stage is given in Figure 3.13.

Another solution is expanding the charge pump with one dummy stage that is connected by a simple diode and has a smaller capacitance. The voltage on this capacitor is only used to feed the DCTS of the previous stage and is not fed to the output.

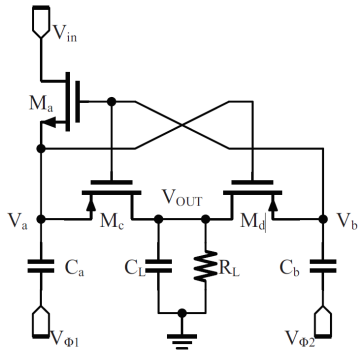

Figure 3.13: Cross coupled charge transfer switch for the last node [79].

Conclusion on Charge Transfer Switches The resulting charge pump works great for efficient pumping, but degrades for very low voltages. Once voltages drop below 100 mV the feedback voltage from the following stages is not sufficient to fully cover for the threshold voltage and the i_{on}/i_{off} ratio drops [11, 62].

Following the idea of borrowing a higher potential from a later stage, it becomes tempting to simply use the output voltage as feedback to achieve an even higher gate-source voltage. However, the gate voltage cannot be lowered enough to deactivate the PMOS in the blocking phase in this case as the inverter is driven by the following stage, which is at a far lower potential compared to the output. Connecting the input of the inverter also to one of the last stages would be a solution to this. But, now the inverter is not able to turn off the NMOS pulling down to the previous node and thus again a large leakage is created. In the end, the connection of neighbouring stages leads to the optimal result.

The presented design can also be made with PMOS implemented diodes. In that case the inverter driving the DCTS connects to an earlier stage to borrow a lower potential and is driven by the following stage. The

first stage cannot borrow from a lower potential without the use of voltages below the ground potential and is thus implemented with a simple diode.

3.4.8. Charge pump sizing

For the modified Dickson charge pumps from Figure 3.11 and Figure 3.12 the input to output relation can be derived from Equation 3.4 by removing V_{thn} (assuming that the later stage voltage is above the threshold voltage) as follows:

$$V_{out} = V_{dd} + N\left(\frac{V_{dd}C}{C+C_p} - \frac{I_l T}{C+C_p}\right) \tag{3.7}$$

Capacitors are the largest components in current IC technologies and determine the silicon area used, as other components can be placed below the capacitors. Thus, the area of a charge pump is almost completely determined by the total capacitance needed. The area of the charge pump can therefore be described by $A_{tot} = kC_{tot}$, where k is a process dependent parameter for the amount of area per capacitance. Using Equation 3.7, the total area of the charge pump can be written as follows:

$$A_{tot} = \frac{N^2 k I_L T}{(1+\alpha)(V_{dd} - V_{out}) + NV_{dd}} \tag{3.8}$$

Where $\alpha = C/C_p$, representing the relative parasitic capacitance caused by a capacitor. To achieve smaller area a reduction in load current and increase in frequency are obvious approaches. However, these are often given by the system design and cannot be altered. Optimising the total area can be done through the number of stages (N). The optimal number of stages is found by taking the derivative and equating to zero, resulting in the optimum number of stages being:

$$N_{opt} = 2(1+\alpha)\left(\frac{V_{out}}{V_{dd}} - 1\right) \tag{3.9}$$

The required capacitance per stage is then given by:

$$C_{opt} = \frac{N_{opt} I_L T}{(1+\alpha)(V_{dd} - V_{out}) + N_{opt} V_{dd}} \tag{3.10}$$

From Equation 3.9 it can be seen that a smaller area can also be achieved through reduction of parasitics and conversion ratio (V_{out}/V_{dd}).

3.4.9. Conclusion on charge pumps

Charge pumps provide a manner of boosting utilising only integrated elements with high achievable efficiency. For cold start a variant is needed that does not require active control. The best conversion ratio for stages used can be achieved using Charge Transfer Switch schemes. For the expected low power and low voltage system the size of the charge pump is large, due to the required capacitors for each stage. Therefore the charge pump size is mainly determined by its capacitors.

3.5. Voltage level detector

In the cold start scenario very small amounts of energy are harvested by the cold start circuit. This energy is stored on an intermediate storage element and is used to drive the more efficient harvester later. If the main harvester is always connected to the intermediate storage element, it is continuously draining the storage element, even if start-up cannot yet be achieved. To prevent leakage, a switch is needed that only connects the main harvester if enough start-up energy is gathered. A switch is easily made in CMOS technology, but detection of the right amount of energy needs more precision. Detection can be done by measuring the voltage stored on a capacitor. The measurement must be converted into a signal that activates the switch at the right voltage level. A device that can achieve this behaviour is the voltage level detector.

This section starts from the ideal voltage level detector (VLD). Next, the most basic designs of VLDs are examined. The section is concluded with the most promising VLD.

3.5.1. Ideal voltage level detector

An ideal voltage detector has a zero output before the detection level is reached and as high as possible voltage level after being triggered [80]. Since the system is energy depleted and only low voltages are available, the output follows the input voltage after triggering. This behaviour is illustrated in Figure 3.14 together with the generic symbol for a level detector.

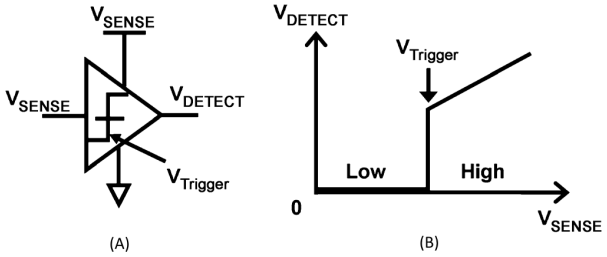

Figure 3.14: Ideal voltage level detector. (A) Symbol and (B) ideal voltage behaviour [80].

Another important aspect with the ideal voltage level detector is low power consumption. Just as for the energy hungry main booster, the voltage level detector should not draw too much energy from the intermediate storage.

3.5.2. Basic voltage level detector

The conventional method of voltage level detection utilises a voltage reference and a comparator. The voltage reference is preferably created by the band gap reference (BGR) for stability. Unfortunately, both the comparator and BGR require a battery voltage to be present, which is not the case in cold start. On top of that, these components burden the cold start circuit during start-up as they also consume power before the trigger point is reached.

3.5.3. Low power voltage level detector

An improvement in terms of power consumption and voltage demands can be made by incorporating the comparator element into the reference generating element. To this goal P. Chen *et al.* propose the use of two cascode transistors [80]. They chose to use two PMOS devices in cascode, as these have less variation. The design is given in Figure 3.15(A).

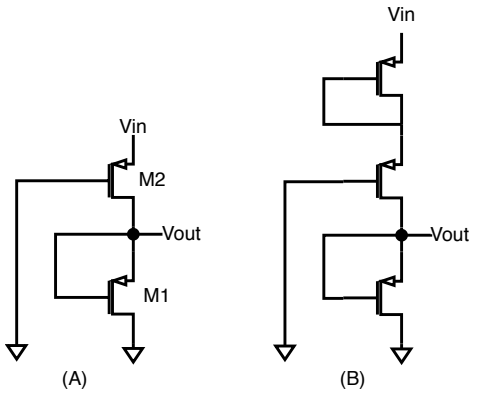

Figure 3.15: Low power voltage level detector. (A) the core design and (B) with the added diode connected transistor [80].

The currents through the transistors determine the output voltage. As both transistors operate in the sub-threshold regime, very little current flows before triggering. The trigger point is found when the pull-up and pull-down currents are equal, which is at an input voltage given by:

$$V_{trigger} = mV_t ln\left(\frac{W_1 * L_2}{W_2 * L_1}\right) \tag{3.11}$$

Where m is the sub-threshold slope coëfficient, V_t is the thermal voltage and W and L are the widths and lengths of the transistors. The trigger voltage is determined by the W/L ratio between M1 and M2. At room

temperature the ratio required for sensible voltages is enormous and not practical to design with. To decrease the ratio, a diode connected transistor is added to the first transistor, adding another gate source voltage to the trigger voltage. The resulting circuit can be seen in Figure 3.15(B). Unfortunately, increasing the trigger level results in a lower output voltage.

Unfortunately, the ratio between the transistors sizes is still large, although not impossible. On top of that, the buffers and low output swing of the detector leads to more power consumption both before and after triggering. The realised maximum power consumption was established at 1.6 nW.

3.5.4. Cross coupled voltage level detector

A new design is proposed by M. Dezyani *et al.* that aims at even lower power dissipation and full output swing [62]. The cross coupled design is given in Figure 3.16.

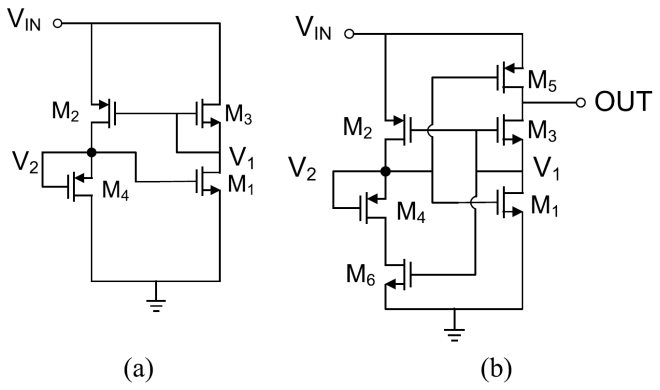

Figure 3.16: Cross coupled voltage level detector. (a) main circuit, (b) implemented version [62].

The design is a combination of two VLDs from Figure 3.15. One is the M1 and M3 branch and the other transistors create a complementary branch. The M1, M3 branch is made using NMOS transistors, creating a positive feedback loop. The positive feedback creates a sharper rising edge when triggered and by that reduce power consumption.

The trigger happens when the currents of the transistors in each brand are equal, so $I_{M3} = I_{M1}$ and $I_{M2} = I_{M4}$. Before triggering, the circuit reduces to that of Figure 3.16(a), as transistors M5 and M6 can be considered ON. In this circuit the gate source voltage of M1 is determined by the opposing branch by:

$$V_{1GS} = \frac{L_4/W_4}{L_4/W_4 + L_2/W_2} * V_{in} = \alpha * V_{in} \tag{3.12}$$

This voltage determines the drain current and thus determines the trigger voltage. The sizing is effectively reduced by a factor $e^{1/\alpha}$. The maximum power consumption during the switching moment is simulated at 14 pW, a major improvement over the previous detector.

3.6. Cold start circuits overview

For a cold start circuit, three components are of essence: an oscillator, a voltage booster and a voltage level detector. These components need to be passively connected to the source for cold start and only connect to the main harvester once the desired amount of energy is stored. After cold start, the cold start circuit can be disconnected from the source by active manners, so that no energy flows in there. Once the input power levels drop, the cold start circuit should be reconnected and cold start can be performed again.

For oscillators the best performance is achieved with off-chip inductors in LC oscillators or inductive load ring oscillators. These allow for the lowest starting voltages and are capable of pushing the generated signal above the supply. Achieving oscillation with only on-chip devices is best done with ring oscillators, which can start from around 60 mV and consume little silicon area. One downside of ring oscillators is the absence of a higher output swing, unless bootstrapping or an inductor is used.

Boosters are also best made using inductors or other off-chip transducers. For a fully integrated deign, charge pumps are the most promising technology. For cold start, the Dickson charge pump topology should be used. A good addition is the use of charge transfer switches.

Lastly, voltage level detectors are essential to ensure power is only transferred if start-up is completed, otherwise the storage is constantly drained and sufficient voltage levels are never reached. Current research has been focussed specifically for low power and low voltage operation VLDs, where the cross-coupled voltage level detector is the best option.

4

System proposal

Now that the choice for the best energy source is made and the basics of energy harvesting with respect to cold start are explored, a system proposal is made. The system is build on existing technologies and aims at extending the possibilities in energy harvester design.

The chapter is started with the new system proposal. After that, each subsystem is explained. The advantages and challenges of each block is examined, followed by novelties and challenges of the system level design.

4.1. System level design

Figure 4.1 gives a graphical representation of the proposed system. The red arrows indicate flow of energy and the green arrows represent flow of information. Information flows are control signals that toggle switches. The source is a solar cell, as it was found to be the preferred energy transducer in Chapter 2. The storage element can be a capacitor or battery, depending on the application. The load will be a low power application fitting the small footprint energy harvester.

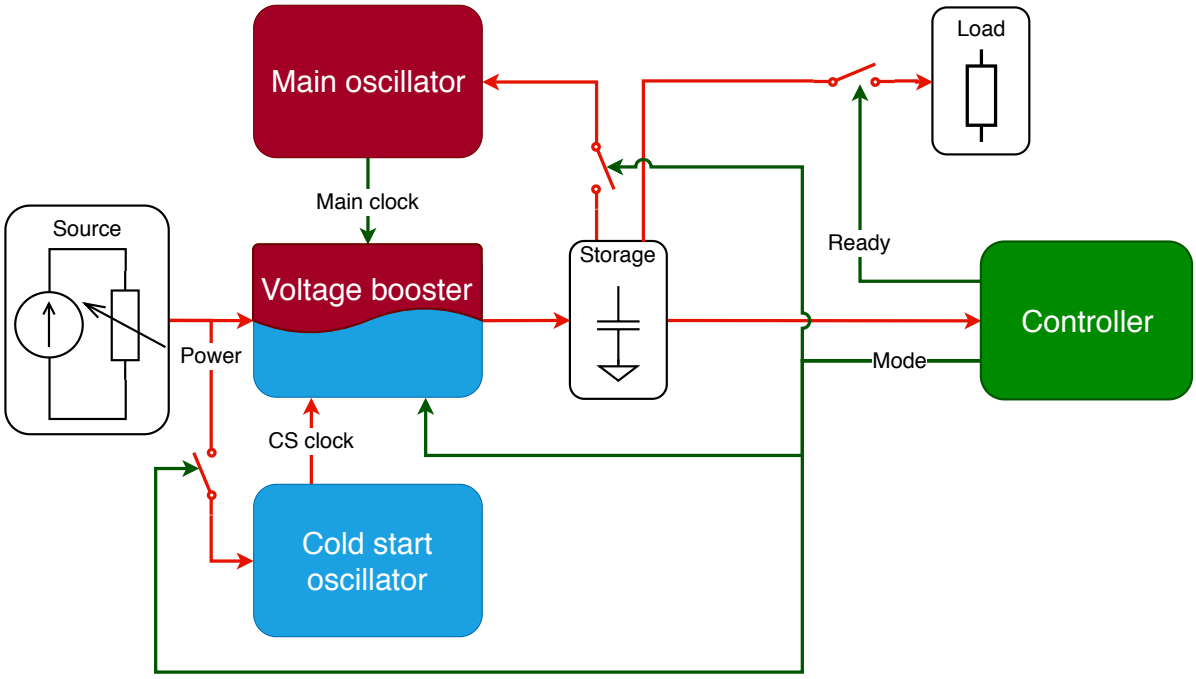

Figure 4.1: Proposed system architecture. The red arrows represent flow of energy and the green arrows indicate flow of information.

4.1.1. Voltage booster

In Chapter 3, a system in which cold start and main voltage boosting are combined was found to be desirable, especially for chip area reduction. To this purpose, a voltage booster is designed that is capable of both cold start and high power conversion efficiency. One topology capable of both would be ideal. However, no booster that is fully integrated within reasonable area, or with desired efficiency exists as explained in Chapter 3. Therefore, the proposed booster adjusts its topology from a cold start capable booster to a high efficiency booster depending on the needs of the circuit. The combined voltage booster is the main innovative step in the system and is therefore the focus of this thesis.

Chapter 3 also explains that the switched capacitor class voltage boosters are the most promising fully integrated voltage boosters. The main advantages of switched capacitor voltage boosters are their high efficiency and small form factor. For cold start, a Dickson type charge pump is the most logical choice. For high efficiency harvesting, a series-parallel type charge pump is the better choice.

4.1.2. Oscillators

Two different oscillators are present in the system as can be seen in Figure 4.1. Due to the expected Dickson type charge pump for cold start, the oscillator drives a heavy load and provides the majority of the power that reaches the storage element. The energy provided by the oscillator to the voltage booster is also indicated in Figure 4.1 with a red arrow for the clock signal from the cold start oscillator.

No stable voltage source is available during cold start to feed the oscillator and thus it is fully powered by the source. The cold start oscillator will be designed to produce at least some sort of oscillation under these circumstances. The efficiency of this oscillator is of less interest, since cold start is a one time operation to begin an efficient manner of harvesting. Operation from low voltage and power inputs are more important aspects for the cold start oscillator. The voltage swing mainly determines the reachable output voltage of the system in cold start. The frequency effects the efficiency, but also the output voltage due to the voltage ripple.

The main oscillator can utilise a stable battery voltage and is designed for high efficiency. Since the main booster is of a series-parallel type, other parameters than for a Dickson charge pump are of interest. The main oscillator requires a stable voltage references and current sources to produce precise clock signals, since non-overlapping clock signals with fast rise and fall times are required to maintain high efficiency. On top of that, there is a need for performing Maximum Power Point Tracking for high efficiency harvesting. Adjusting the oscillator frequency is an often applied and good measure to do so. An oscillator with controllable frequency driven from the source alone would be very challenging to design.

4.1.3. Control

Control must be applied to the system in order to perform cold start and to be capable of high efficiency harvesting. Towards both goals, some subsystems are disabled or adjusted. The controller is a low power system that consists of sensors and logic circuits to implement control. The sensors will be implemented using voltage level detectors.

The controller measures the voltage on the storage element in order to determine what mode the system should operate in. Two modes are distinguished: cold start and normal operation. The general control flow is given in Figure 4.2.

Cold start During cold start, the load and main oscillator should be disconnected so that no energy is drawn from the source by them. The cold start oscillator together with the voltage booster (in cold start mode) are connected to the source. These two subsystems charge the storage element, solely using the source for energy and information flow.

The storage element is charged to a voltage that is sufficient for the main oscillator and voltage booster to start. The cold start will be designed to reach this voltage with a margin that accounts for losses and environmental changes.

During cold start, the controller does not have the energy available to reliably control the switches in the circuit. Therefore, switches that should be active during cold start must be implemented in a manner that does not require active control. The switches are actively controlled in normal operation.

Normal operation Normal operation starts once sufficient voltage is reached. The *Mode* signal becomes high, but the *Ready* signal not yet. In normal operation the main oscillator and voltage booster are activated

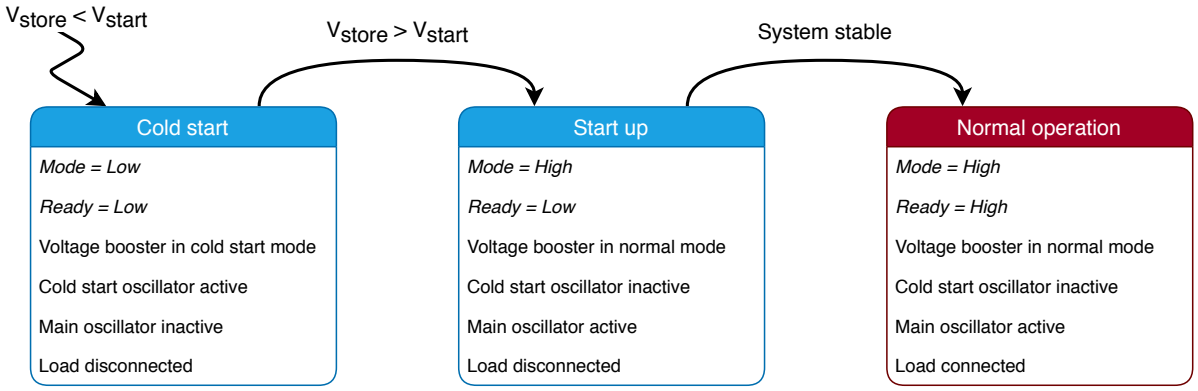

Figure 4.2: Control flow of the proposed system. V_{store} is the voltage on the storage capacitor, V_{start} is the minimum voltage required for start-up.

and convert the energy from the source to the load. A couple of harvesting cycles are needed to stabilise the system after changing the mode of operation. Once the system is stable, the load is connected using the *Ready* signal and cold start has been completed.

During normal operation, the cold start oscillator is turned off to prevent energy leaking from the source into the oscillator.

4.2. Design features and challenges

As previously discussed, the proposed design aims to implement multiple features that are of interest to the field of energy harvesting. The innovative features of the proposal are:

- A voltage booster that is both cold start capable and can achieve high efficiency boosting;
  - The voltage booster has a different topology for both functions, but utilises the same building blocks;
  - The sharing of building blocks reduces the size of the voltage booster compared to having one voltage booster for each mode of operation;
  - The cold start minimal input voltage and power can differ from that for normal operation;
  - The addition of cold start capability has minimal impact on the efficiency of the normal booster;
- The system can be fully integrated;
- Control of the operation mode can be done during cold start;
  - The cold start mode of operation is normally activated;
  - If the storage element is depleted during normal operation, the system returns to cold start passively;
- The cold start oscillator shall not burden the system during normal operation.

The design of the voltage booster is the main challenge, as it is the main innovation of the system. A design combining a Dickson like charge pump and series-parallel charge pump is envisioned. The high efficiency for normal operation will mostly be challenged by added leakages and parasitics. With adequate design, it should be possible to keep the losses at a minimum.

4.3. Conclusion

A design is proposed with the main feature of a voltage booster that is both cold start capable and can provide high efficiency conversion. With this voltage booster, an energy harvesting device can be made that has minimal size, is cold start compatible and can harvest from low power environments with high efficiency.

The exact design of the voltage booster is the most challenging part of the design and is addressed in the next chapter.

5

Capacitor sharing charge pump

In the proposed system, a charge pump capable of both cold start and high efficiency harvesting is taken as the voltage booster. One of the main reasons for this choice is the reduction in silicon area that is used by the charge pump. The combined charge pump is the main innovation of this thesis and is thoroughly explained in this chapter.

In this chapter, the design will be built up, beginning with exploring the possibilities of the known devices discussed in Chapter 3. After the core design is presented, its operation is examined in more detail. Next, adaptations to the core design are presented followed by a section on switch design. Lastly, the chapter is concluded with an overview of the proposed system features.

5.1. Normal charge pump area

The Dickson charge pump is the best choice for a cold start capable charge pump, as was concluded in Chapter 3. One major concern that comes with the use of the Dickson charge pump is the required area. Each stage of the charge pump requires a capacitor, resulting in cold start circuits taking up to a third of the total chip area [4, 60, 62, 67].

The area of a charge pump is determined by the capacitor sizes as the sizes of the involved switches are minor in comparison and often fit under the capacitors. The area of a charge pump is therefore determined by:

$$A_{tot} = k \sum_{i=1}^{N} (1+\alpha) C_i = k C_{tot} \tag{5.1}$$

Where k is a process dependent parameter for capacitor realisation, α is the parasitic capacitance factor and C_i is the capacitance for each stage. In Section 3.4 the optimal amount of stages and the required capacitance per stage is given in Equation 3.8 and Equation 3.9. From these it was concluded that the total area of a charge pump can be reduced by four possible methods:

- Reducing the conversion ratio (V_{out}/V_{in});
- Reducing the parasitics;
- Increasing the oscillator frequency;
- Reducing the load current.

The first two methods shall not be examined further as these are given by the design constraints and technology. The oscillator frequency is determined also by another component, but could be increased. However, in cold start scenarios the oscillation is mainly determined by the source and altering the frequency leads to greater efficiency losses. The load current for a cold start circuit is determined by the power required by the main system to escape cold start and the leakage in the system. The leakage and load current are determined by the system design and can thus be used to possibly reduce the required area.

5.2. Storage capacitor approach

The load current presented in the previous section is a measure for the power required to start up the main system. In all previous calculations, it is assumed that this power is delivered throughout the cold start operation continuously. However, the main harvester can be left disconnected until enough power is stored for start-up. Removing the constant current drawn by the main harvester from the equation for the output voltage of a charge pump (Equation 3.7) leads to the following:

$$V_{out} = V_{dd} + N\frac{V_{dd}C}{C+C_p} = V_{dd} + NV_{dd}\frac{1}{1+\alpha} \tag{5.2}$$

A conversion free of capacitor size is obtained. Nevertheless, the start-up energy still needs to be stored somewhere. The total amount of storage required is exactly the same as the total capacitance that was previously found in the charge pump itself, as the energy demands did not change. The area of the charge pump is thus only placed outside the charge pump internal design.

Leakage is always present in a design and thus capacitors cannot be fully removed from the charge pump.

5.2.1. Storage capacitor sharing

The energy harvester chip does not solely consist of the cold start circuit and thus has other components readily available. In case of a harvesting IC there is also a main booster present, likely designed to charge a large capacitor. The bulky capacitor can be utilised as a storage element for the cold start circuit. Using that capacitor can be done as long as the load capacitor is not leaking more power than is acquired by the charge pump and accepts lower voltages to charge up.

Some harvesting systems rely on batteries instead of capacitors as their major storage element. These can also be used by the cold start system as storage.

A harvesting system does not only contain capacitors used for storage, especially if the voltage booster is of the switched capacitor type. These capacitors may be harder to reach and more elaborate control is needed to utilise these for storage during cold start. Nevertheless, these provide an opportunity to reduce the capacitance (and thus area) needed for a cold start addition to the system.

5.2.2. Capacitance per stage

Equation 5.2 seemingly accepts zero capacitance to operate, but this is only for a static, lossless case. The storage capacitor needs to be charged by the charge pump and leaks energy over time. The larger the capacitance per stage of the charge pump, the more charge can be stored in one cycle and thus the more current can be delivered. As the storage capacitor and charge pump leak energy, the capacitance of the charge pump must not be reduced to zero. Increasing capacitor sizes also improves the start up time of the system, but this is not a focus of the presented work.

The total capacitance used in a charge pump can be arranged in multiple manners. Larger stages can be created by reducing the capacitance of other stages. The number of stages can be changed in this manner as well, as a large capacitor can be build of smaller capacitors. The charge on a capacitor is determined by its capacitance and the voltage difference between its plates by:

$$q = C \cdot V \tag{5.3}$$

Two capacitors that start with a voltage difference between their top plates reach an equal potential when connected due to the redistribution of charge between the capacitor plates. The final voltage is determined by the starting voltages on both capacitors and their capacitances, thus their initial charges. The initial difference between the starting voltage is called ΔV. For Dickson type charge pumps, this difference is created by the oscillator as it controls the bottom plate voltages. The amplitude of the oscillator thus determines ΔV. For two equal capacitors, the final voltage is in the middle of the two starting voltages. The final voltage is $V_{end} = V_{init} + \frac{1}{2}\Delta V$, where V_{init} is the initial voltage on the capacitor being charged. If one of the capacitors is larger, the final voltage ends closer to the starting voltage of this larger capacitor, as a larger capacitor has more charge initially and has thus more influence on the total charge on both capacitors. Therefore, charging a smaller capacitor with a larger capacitor results in a higher voltage on the capacitor being charged, compared to voltage boosting with two equal capacitors (assuming that the initial voltage difference is the same). The final charge on the smaller capacitor is $V_{init} + \frac{1}{2}\Delta V + V_x$, where V_x is the additional voltage due to the difference in capacitance. V_x depends on the first to second capacitor ratio, where a larger ratio results in a higher deviation of the final voltage from ΔV and thus a higher V_x. However, the final charge on the smaller

capacitor is not greater than the final charge on the regular capacitor, as the capacitance in the first scenario is lower and the charge is determined by Equation 5.3. The charge transferred is thus independent of the capacitance, as the capacitance has an inverse relation with the voltage increase and a linear relation with the charge. A reverse scenario also holds: a smaller capacitor that is charged to $V_{init} + \frac{1}{2}\Delta V + V_x$ (as in the previous scenario) can be connected to a new large capacitor in the next stage. Now the larger capacitor pulls the final voltage down with an additional V_x (assuming it has the same capacitance as the first large capacitor) and thus the final voltage is:

$$V_{end} = V_{init} + \frac{1}{2}\Delta V + V_x + \frac{1}{2}\Delta V - V_x = V_{init} + \Delta V \tag{5.4}$$

The same final voltage as for a charge pump with equal capacitors is found. The same ΔV is seen between stages, as the oscillator amplitude is equal for all stages.

Decreasing capacitance charge pump A charge pump with a decreasing capacitance per stage can achieve the same output voltage with a fewer stages compared to a charge pump with equal capacitance per stage. The voltage on the last, smallest capacitor of the decreasing size charge pump is equal to the voltage on the last capacitor of a regular charge pump. The last capacitor of the decreasing size charge pump has less charge, since the capacitance is lower. However, the load capacitor is the same for both charge pumps. Therefore, the last capacitor to load capacitor ratio is greater for the decreasing size charge pump and thus the final voltage delivered to the load capacitor is lower for this charge pump. To achieve the same output voltage on the load capacitor, the voltage on the last capacitor must be increased. This can be achieved by utilising more stages and thus increasing the charge pump size. Ultimately, the total capacitance required for the decreasing capacitance size charge pump equals a regular sized charge pump to achieve the same output voltage on the load capacitor. In the end, a charge pump with decreasing capacitance per stage only alters the number of stages and capacitance per stage, but the delivered output charge and total capacitance remains the same.

The smaller amount of stages in the decreasing capacitance charge pump require fewer connections to the oscillator. However, the larger stages require more power to be driven and thus the power inserted by the oscillator is only rearranged and not decreased or increased. The same can be said for the devices connecting one stage to the next; fewer devices are needed, but the devices for the earlier stages must be made larger as the load capacitance is higher. The oscillator and connecting devices are thus asymmetric. Designing asymmetric devices is more challenging and can lead to mismatching between devices. Therefore, a symmetric charge pump design is preferred.

To summarize, no reduction in total capacitance can be achieved with a charge pump that has a decreasing capacitance per stage. Designing an asymmetric charge pump and its supporting systems is undesired and thus a charge pump with equal capacitance per stage is the preferred charge pump design. A similar case can be made for charge pumps that utilise different capacitance per stage schemes, the same conclusion is found for each scheme.

5.2.3. Control

Due to the shared capacitor between normal operation and cold start, a robust controller is needed that can assure both modes of operation with one capacitor. During cold start the capacitor must be solely connected to the charge pump to ensure minimal leakage through other components. The voltage on the storage capacitor must be monitored to determine when enough energy is build up to perform start-up of the main harvester.

Once this voltage level is reached, the controller directs the energy on the capacitor towards the main harvester. If the start-up succeeds, the capacitor is connected to the load and normal energy harvesting can begin. During normal operation, the cold start circuit must be disabled and the power flow must be monitored to ensure the capacitor is charged by the main harvester.

The controller must thus be able to perform voltage measurement in a cold start scenario and be able to recognise the main harvester being operational after start-up.

5.2.4. Conclusion on storage capacitor sharing

Utilising an already present capacitor reduces the capacitors needed within the charge pump itself, but cannot fully remove them due to leakage and charging time. The time needed to perform start-up is increased, as a storage capacitor must first be charged by a weaker charge pump that outputs less charge per cycle. A robust controller is needed when the storage capacitor is shared between normal operation and cold start.

5.3. Flying capacitor sharing

Since the cold start system still requires capacitors for its own stages, more already present capacitors in the system are used.

The main booster also utilises capacitors, assuming it is of the switched capacitor type. The main booster requires fewer capacitors that are often larger than the capacitors needed in the cold start charge pump, due to the quadratic increase in voltage as function of the number of capacitors. As the main harvester is not active during cold start, the capacitors can be utilised by the cold start circuit during that period.

A method of reliably sharing the flying capacitors between a Dickson charge pump and a series-parallel charge pump are explored in this section. The most basic design is given first, after which adaptations to this design are made.

5.3.1. Building blocks

To build a combined pump, first the existing pumps must be broken down to their most fundamental parts. The fundamental parts are defined by the components used and the connections between these components.

Dickson fundamental blocks The basic Dickson charge pump is given in Figure 5.1. A clear indication is made between the stages in a Dickson charge pump. These stages are separated by the flying capacitors.

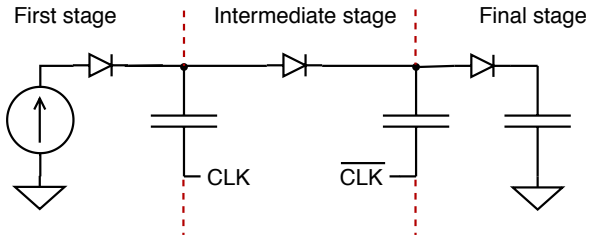

Figure 5.1: Basic Dickson charge pump with its stages indicated.

As can be seen, the Dickson charge pump can be divided into three parts. The intermediate stage can be repeated as many times as needed to acquire the desired conversion ratio and contains connections needed between each flying capacitor pair. The first and last stage are quite similar to the intermediate stage, but have a source and load as their main components, respectively. The fundamental components of the Dickson charge pump are the diodes and capacitors. The diodes are always connected to conduct from source to load and the capacitors are always connected at the top to two diodes and at the bottom to alternating clock signals.

Series-parallel fundamental blocks A similar dissection can be made for the series-parallel pump and is given in Figure 5.2. Again, three stages are distinguished and the intermediate stage can be repeated to increase the conversion ratio.

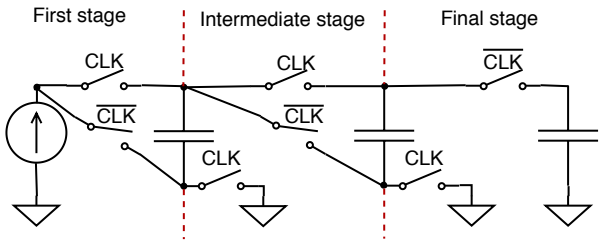

Figure 5.2: Basic switched capacitor pump with its stages indicated.

Fundamental to the series-parallel pump are switches and capacitors, where the function of the diodes in the Dickson charge pump is fulfilled by the switches. Two alternating clock signals are still needed. These must be strictly non-overlapping to prevent a sort circuit of the source. As seen in the figure, the capacitors have specific switch nodes connected to their top and bottom plate that are equal for each intermediate stage.

Both the Dickson and series-parallel pump topologies have fundamental connections to the top and bottom plates of their flying capacitors. These fundamental connections must be adhered for the pumps to operate as desired.

5.3.2. Combinations

Comparing the intermediate stages in both Figure 5.1 and Figure 5.2 shows that the intermediate stage is a four-terminal network, where each capacitor plate is one of the four terminals. Each interconnect design can be flipped over the horizontal and/or vertical axis without changing the operation of the interconnect with respect to the capacitors. Flipping over the vertical axis inverts the direction in which current flows through the complete pump, so the first and final stage should be swapped in this case. Flipping over the horizontal axis reverses the polarity of the voltage on the flying capacitors and thus requires the first and final stage to be flipped over the horizontal axis as well.

Reversing the flow of current in one of the interconnections seems impractical, since the first stage of one pump is then the last stage of the other. The first stage for both pumps must connect to the transducer and the final stage connects to the load capacitor. A wire should thus be run along the length of the pump with switches to correct for the reverse flow. On top of that, the flow during normal boosting is disturbed as the cold start diodes are facing opposite to the desired flow of current and will thus leak current backwards.

Reversing the polarity of the flying capacitors when switching operation mode also poses problems. The final stage must be passively connected to the lower node for the cold start operation, which is connected to a ground node in normal operation. This poses a high risk of shorting the load capacitor.

Therefore, it is chosen to not alter any orientation and the two systems are combined as in Figure 5.3. The first, last and three intermediate stages are given in this figure. The switched capacitor pump is taken as the default and the Dickson charge pump is added with the components highlighted with blue dotted connections. Note that there are two different clocks, one for cold start (*CLKcs* in blue) and one for the normal operation.

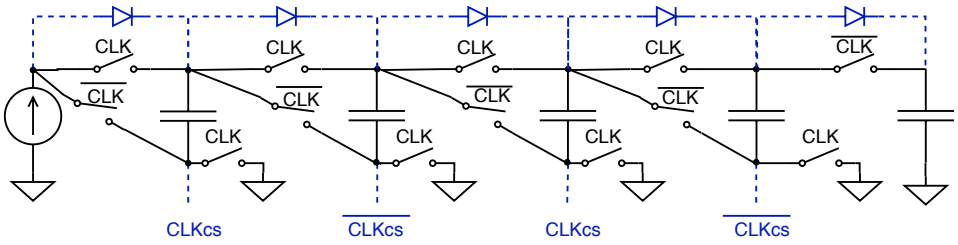

Figure 5.3: Proposed combination of a switched capacitor pump (in black) with a Dickson charge pump (added components in blue).

5.4. Operation analysis

The circuit in Figure 5.3 can now be examined for both cold start and normal operation. Cold start operation refers to the design operating as a Dickson charge pump fed by the auxiliary oscillator and normal operation refers to the circuit operating as a switched capacitor network controlled by the main oscillator.

5.4.1. Cold start operation

The main oscillator is inactive during cold start and thus both the CLK and $CLKb$ signals are low. The low clock signals deactivate all the switches that belong to the normal operation. With these switches deactivated, the system can be simplified to that of Figure 5.4. The cold start operation is that of the regular Dickson charge pump as can be seen in the figure.

The switches that are assumed to be turned off might not fully be disabled and cause an increased current leakage between the capacitors. The switches should be implemented so that maximal impedance is seen across the switch during cold start. A stable battery voltage is available during normal operation to drive these switches. The higher driving voltage in normal operation leads to a high conduction of the switch when activated. The high driving voltage thus allows for a switch implementation that is focussed towards lower leakage during cold start and less focussed towards high conduction during normal operation.

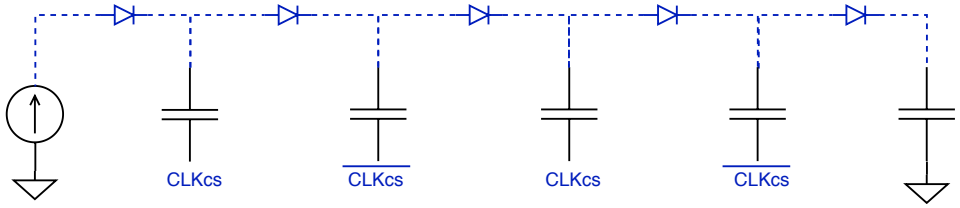

Figure 5.4: Proposed design in cold start operation.

5.4.2. Normal operation

During normal operation, the clock signals of the cold start circuit should not be low potential, but must pose a high impedance. Otherwise, the bottom node of each flying capacitor is connected to the auxiliary oscillator. The charge on the bottom plates would leak through the oscillator and cause major losses for normal operation. The implementation of a high impedance to separate the auxiliary charge oscillator and charge pump is discussed later in Subsection 5.5.1.

With the cold start clock signal removed the circuit is reduced to a switched capacitor pump with added diodes. To illustrate the full operation, both the charging phase and the boosting phase during normal operation are depicted in Figure 5.5. The figure also indicates the voltages present in each node, where $V+$ is the input voltage.

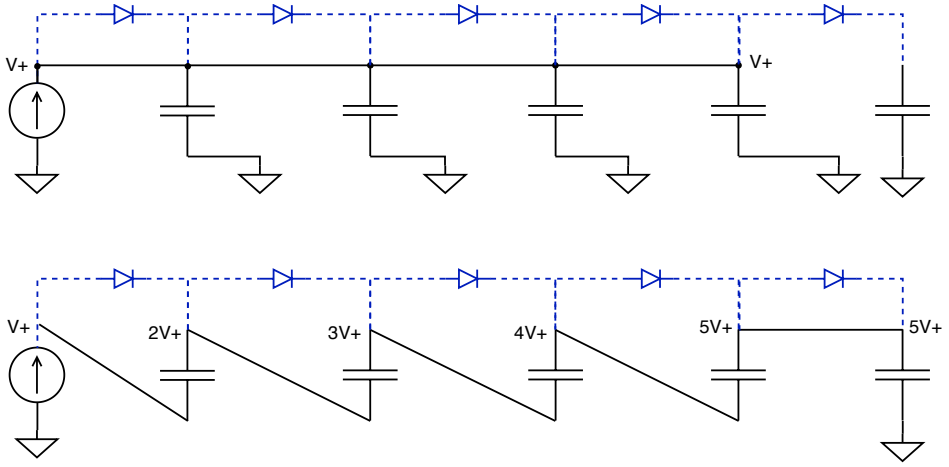

Figure 5.5: Proposed design in normal operation. The top image displays the circuit during the charging phase and the bottom image is during the boosting phase

The diodes are still in the system, but do not cause unwanted conduction paths. Each diode is shorted in the charging phase, except for the final stage diode. The shorted diodes do not interfere with the pump operation, as both terminals of the diode are at the same node. The final diode also poses no problem as the voltage on the load capacitor is assumed to be higher than the input voltage. Even if this were not the case, the diode helps current flow into the load capacitor, which is the ultimate goal of the charge pump.

The last diode is shorted and all other diodes are parallel to the flying capacitors in the boosting phase. The parallel connection is always from a lower voltage to a higher voltage node and thus the diode poses a high impedance as desired.

The diodes in the design are replaced by diode connected MOS transistors at a later stage in design. During normal operation these transistors add parasitic capacitance, thus lowering efficiency. The exact losses due to these parasitics are determined later.

Overall, the normal operation is barely hampered by the addition of the cold start system. Only the auxiliary oscillator connection on the bottom plates of the capacitors might pose an issue.

5.4.3. Mode switching

During cold start, a moment is reached where enough energy has been collected onto the load capacitor to begin normal operation. Switching to normal operation can cause losses if not done correctly. The main risk is at the bottom plate node of the capacitor. If the normal operation switch is conducting, this node becomes

grounded. The cold start oscillator might still connect this node to the source and thus a short circuit is created. It is therefore desired that the cold start clock is first disconnected, before the main oscillator is activated.

The top plates of the capacitors are of interest as well. Charge is still present on these plates at the end of cold start. If the normal operation starts with the charging phase, the built up charge from cold start leaks back to the source, since this is the lowest potential in the chain. Starting in the boosting phase, the charge on the last flying capacitor is transferred to the load. Inevitably, the charging phase follows, in which the charge on all the other capacitors still leaks back to the source. Starting in the boosting phase thus only saves the charge on the last capacitor. The losses due to this back flow is minimal, since it only happens once.

From the previous examination on energy flow back, a question arises as to where this energy goes. If the source is an ideal transducer the energy is converted back to the other energy domain and is likely lost. In other transducers the energy might build up in some component of the transducer itself. The energy is then distributed amongst the transducer and the capacitors and might not get fully lost. The transducer might deteriorate from a large back flow current, depending on the transducer characteristics. Therefore, it is desired to prevent the flow back of energy when changing the mode of operation.

5.4.4. Conclusion on basic operation

The Dickson charge pump can be combined with the topology of a series-parallel type charge pump, as their fundamental building blocks are similar.

The combined design allows for correct operation under the assumptions that the main clock is pulled low during cold start and the cold start oscillator imposes a high impedance during normal operation. Depending on the transducer, the flow back of energy caused by mode switching could degenerate the transducer.

5.5. Adaptations

Now that the basic design is set, additional features can be explored. Some features are necessary to prevent damages and major efficiency losses. Others improve operation of either the Dickson charge pump or series-parallel pump with minimal impact on the other.

5.5.1. Clock disconnection

The first addition is a manner to disconnect the cold start oscillator during normal operation. Creating the high impedance is challenging. The path that must be deactivated during normal operation must provide high conductance during cold start. The energy of cold start flows through the path as the clock signal. Since a clock signal is being conducted, current must be able to flow in both directions and thus a diode cannot be utilised.

The chosen approach is to have a switch present at the output of the oscillator that is active during cold start. The switch is implemented by a pass gate, comprising of one NMOS and one PMOS in parallel. In the pass gate, the PMOS ensures a good pull up from the oscillator and the NMOS ensures the pull down. Conduction by the NMOS is degraded if the gate to source voltage is low, especially below the threshold voltage. Similarly, the conduction of the PMOS is degraded when the source gate voltage is below threshold, which is determined by the clock amplitude. Therefore boosting both these driving signals is desired during low voltage operation, which is expected during cold start.

Switch driving signal boosting Boosting the driving signal that controls the NMOS can be implemented with a small boosting circuit. The driving signal is a static signal during cold start. The load current that the signal must deliver is therefore determined by passive losses and not dynamic losses. Passive losses are a lot smaller and therefore the boosting system does not drive a high load current.

Designing a small voltage booster can be possible due to the low load current that must be delivered. An auxiliary charge pump is utilised that is driven by the already needed cold start oscillator.

This auxiliary charge pump must be disabled once normal operation is started. Disabling the system lowers the power consumption and deactivate the NMOS in the required switch.

Clock boosting The clock signal from the oscillator is a dynamic signal and thus dynamic losses are a major contributor to the load current that must be delivered. On top of that the clock signal is the energy flow during cold start. Boosting an energy flow leads to less efficiency, as dynamic losses increase. Therefore, the clock

signal is not boosted and lower conduction of the PMOS gate has to be accepted. It is expected that most conduction is contributed by the NMOS device.

5.5.2. Charge transfer switches

As described in Section 3.4 on charge pump operation, there is a desire to utilise dynamic charge transfer switches (DCTS) instead of diode connected NMOS diodes in a Dickson charge pump. Especially for sub-threshold operation, this highly boosts the achievable output voltage. Implementing DCTS in the current design poses a problem during normal operation. This situation is illustrated in Figure 5.6, where the boosting phase during normal operation is depicted. Note that the last intermediate and final stage of the Dickson charge pump cannot use a DCTS, since there is no higher clock driven node available. For these stages normal diode connected transistors are used.

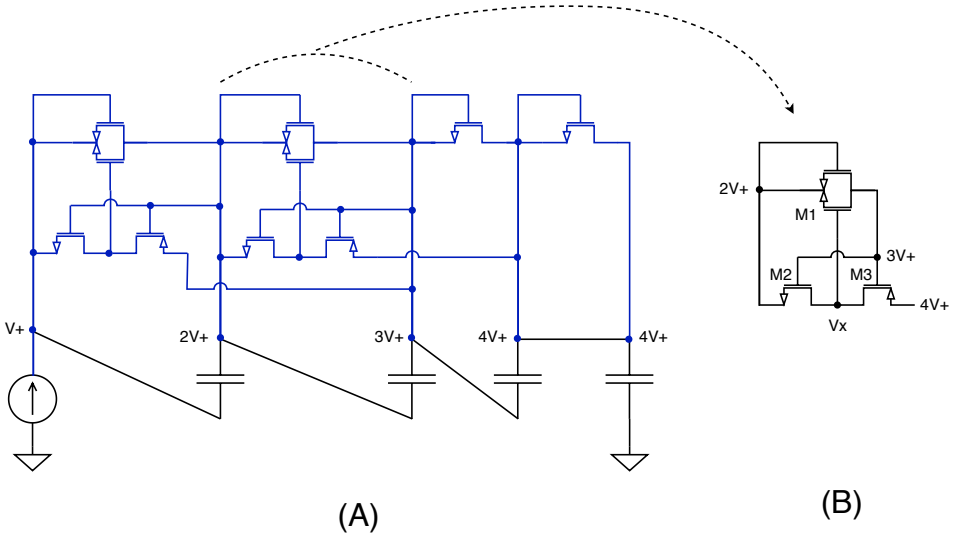

Figure 5.6: (A) Boosting phase during normal operation with DCTS. (B) One DCTS isolated with the voltages at each point indicated

In Figure 5.6(B), one DCTS stage is isolated with the node voltages indicated. The gate potential of M1 (V_X) is controlled by the inverter comprising M2 and M3. The inverter is controlled by the $3V+$ node. Since this node is higher than the left intake of the inverter and lower than the right intake of the inverter, V_X is somewhere between these node voltages. In this example, V_X is around the $3V+$ potential. At this potential, M1 is conducting and thus current flows from right to left, causing later stages to drain to the first stage. The switched capacitor pump does not operate correctly under these circumstances.

Upgrading the inverter to a NAND-gate prevents this leakage current. The NAND-gate must be driven by a control signal and the original signal from the successive capacitor. The control signal is high during normal operation and low during cold start, due to the inverting nature of the gate. The signal from the successive capacitor is always higher than the source voltage of the pull-down branch in normal operation, thus the pull-down branch is already active in normal operation and the control signal is not needed for that branch. The parallel NMOS in the pull-down branch is thus be removed to reduce the gate size slightly.

Final DCTS The final stage of the cold start circuit does not have a succeeding node that can drive the gate and is thus still implemented by a diode. To implement a DCTS for the final stage, an extra diode can be connected after the last stage that is connected to a small capacitor that delivers the control signal. This extra dummy stage capacitor can be kept small, as only one gate is driven by it and not much energy is required to do so.

5.5.3. Conversion ratio orthogonality

A major limitation of the current design is that both pumps utilise the same amount of stages, capacitors and capacitance. The normal operation pump can achieve multiplication of input voltages, whereas the cold start pump can only do addition with each stage. Therefore, the resulting conversion ratios are different for both pumps with the cold start charge pump achieving lower ratios. Especially for higher desired conversion ratios this difference increases.

On top of that, the cold start charge pump is limited by the low available supply voltages that barely surpass the threshold voltages of the DCTS. The lower supply voltages lead to lower conductances and thus less current at the output. As there is always leakage from the storage capacitor, the low output current results in a lower final output voltage reached by the Dickson charge pump.

The final voltage on the load capacitor combined with the capacitance provide the energy needed to start normal operation. On top of that, the final voltage must be high enough to drive the switches during normal operation. For both these reasons a high conversion ratio of the Dickson pump is desired. With the current design, the conversion ratio is limited by the design of the normal operation pump. An orthogonality between the conversion ratios of both pumps is therefore required.

Capacitor splitting As stated before, the capacitors used for normal operation are often larger than the capacitance needed for cold start. This especially holds if the cold start circuit relies on a storage capacitor instead of its stage capacitance to provide enough energy as discussed in Section 5.2. A solution to increasing the conversion ratio of the cold start operation, without altering the capacitance used in normal operation, is by splitting the flying capacitors. A split capacitor can provide more cold start charge pump stages and can be reconnected later to accommodate normal operation.

Assuming that the split capacitor is reconnected by shorting the top plates together and the bottom plates together means that any circuitry between two parts of a split capacitor are shorted as well.

From the previous section it was concluded that DCTS cannot be used without a NAND gate adaptation during normal operation, but if the DCTS is situated within a split capacitor it is shorted during normal operation. Once shorted, there is no issue with leakage as input and output are already at equal potentials. Thus, standard DCTS are used within the split capacitor. Capacitors that are not reconnected during normal operation still require the NAND gate adapted DCTS.

Capacitor splitting improves the cold start conversion operation in two manners, by increasing the number of stages and by allowing the use of standard DCTS.

5.6. Proposed adapted design

Figure 5.7 illustrates the proposed design that utilises split capacitors and DCTS. The blue components are part of the cold start charge pump and the black parts belong to the normal operation pump. The NO signal is a control signal that is high during normal operation and low during cold start. The clock signals for cold start are indicated by $CLKcs$ and for normal operation by $CLKno$. A bar above a signal indicates the inverse signal.

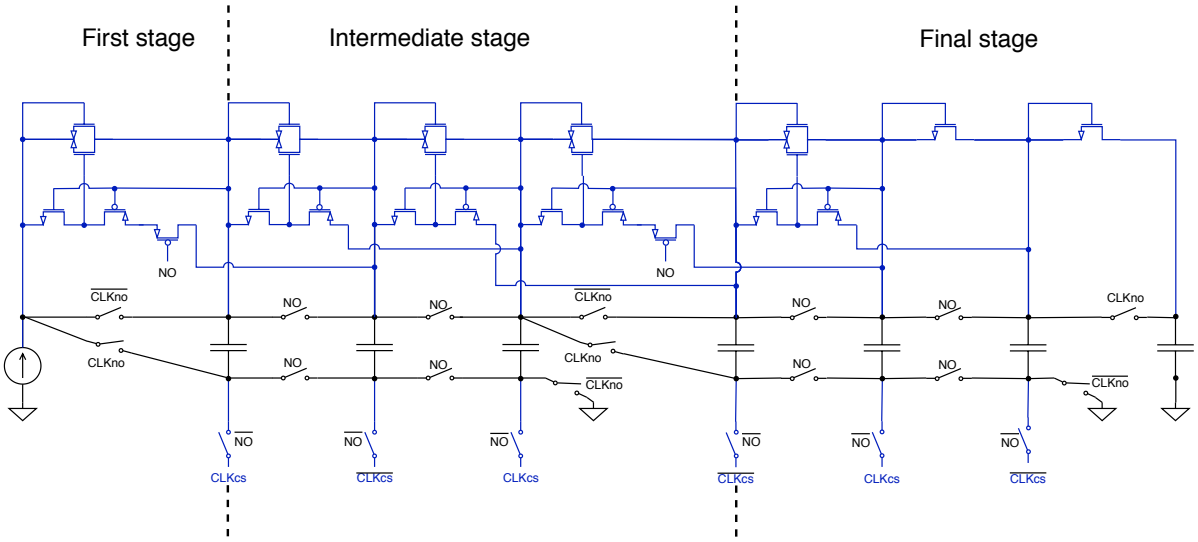

Figure 5.7: Overview of the proposed combined Switched capacitor pump and the Dickson charge pump with dynamic charge transfer switches.

The number of capacitors and the amount of splitting is free to choose in the proposed design. The amount of splitting is called the division ratio. The amount of capacitors determines the number of nor-

mal operation stages. The number of capacitors times the division ratio determine the amount of stages for cold start operation. As was concluded before, the optimal capacitance is reached when distributed equally.

For cold start operation, the last two stages cannot contain DCTS as these have no subsequent clock driven stage for control, in a later design this can be fixed with an additional dummy stage.

5.6.1. Operation analysis

Although the amount of stages and division ratio is free to choose, it is not free of consequences. Splitting the capacitors introduces parasitic capacitance and added resistance during normal operation. The amount of Dickson charge pump stages is equal to:

$$N_{cs} = N_{no} * \gamma \tag{5.5}$$

Where N_{no} is the amount of normal operation stages (thus the amount of flying capacitors) and γ is the division ratio.

The effects of capacitor splitting are examined next for both cold start and normal operation.

5.6.2. Cold start analysis

As with the basic design, the clock signals of normal operation are assumed low during cold start. During cold start, the switches between the capacitors provide a high impedance and thus split the capacitor. The normal operation switches are all deactivated due to the low clock, resulting in a Dickson charge pump with some DCTS and some diode connected NMOS transistors. The output voltage of the cold start operation charge pump is given by:

$$V_{outcs} = V_{in} + \frac{N_{cs} V_{clk} C_{cs}}{C_{cs} + C_p} - 2 \cdot V_{th} - (I_L + I_{leak}) \cdot \frac{N_{cs} T_{clk}}{C_{cs} + C_p} \tag{5.6}$$

Where V_{in} is the input voltage, V_{clk} is the clock amplitude, C_{cs} is the capacitance per cold start stage ($C_{cs} = C_{no}/\gamma$), C_p is the parasitic capacitance per cold start stage ($C_p = \alpha C_{cs}$), V_{th} is the threshold voltage of the transistors, I_L is the load current, T_{clk} is the clock pulse width and I_{leak} is the leakage current.

The first two terms represent the added voltage by the pumping operation, as with the normal Dickson charge pump. The third term refers to the losses imposed by stages that do not utilise DCTS, but rely on diode connected NMOS transistor. The final stage and output diode are the stages that cannot utilise DCTS. Utilising a dummy stage can add DCTS to the final stage, removing one threshold voltage from the third term.

The fourth term also originates from the normal Dickson charge pump and refers to the voltage ripple. The parasitic capacitance is higher compared to a normal Dickson charge pump due to the internal capacitance of the switches for normal operation and splitting switches. The load current and leakage current as seen from the output both add to the voltage ripple.

5.6.3. Normal operation analysis

For normal operation, the cold start oscillator is disconnected and the splitting switches are conducting. Since the DCTS are now shorted, no extra leakage is introduced by these. However, the DCTS, the diode connected NMOS transistor and the splitting NMOS transistor do introduce more parasitic capacitance.

When operating on a two-phase clock the output voltage can be described as follows:

$$V_{outno} = V_{in} + \frac{N_{no} V_{in} C_{no}}{C_{no} + C_{par}} - (I_L + I_{leak}) \cdot \frac{N_{no} T_{clk}}{C_{no} + C_{par}} \tag{5.7}$$

Where C_{no} is the normal operation capacitance, thus the total capacitance of one split capacitor. The resulting output voltage is similar to that of the cold start pump, apart from the threshold voltage losses. The major difference is in the added voltage per stage, the second term in Equation 5.6 and Equation 5.7. During normal operation the added voltage is supplied from the input and not the clock. The flow of power is through the pump and not through the oscillator.

Since the output voltage depends mainly on the input voltage, multiplication is possible. To achieve multiplication, multiple voltage boosters must be placed in cascade. The clock signals must be altered, so that successive pumps utilise the doubled voltage of the first pump.

A more elaborate scheme for achieving multiplication is the Makowski timing scheme as explained in Subsection 3.4.3. The cold start operation is not inhibited by utilisation of the Makowski timing scheme, as the topology does not change. Since a higher conversion ratio with fewer stages can be achieved with the

Makowski scheme, fewer components are needed. Fewer components for normal operation also mean less parasitics during cold start.

5.6.4. Conclusion on adapted design

A transfer gate is required to separate the cold start oscillator from the charge pump during normal operation. The transfer switch requires a higher driving voltage than is available from the source during cold start. Therefore, a small auxiliary charge pump is suggested. The suggested auxiliary charge pump can be small as its load current is small.

With the addition of DCTS, the efficiency and thereby the input to output ratio of the cold start operation is improved. A minor adaptation to the DCTS is needed to ensure there is no leakage during normal operation.

The implementation of capacitor splitting creates orthogonality between the cold start and normal pump design. The amount of stages for each pump is now unaffected by the other. However, extra switches are needed to allow for the splitting.

5.7. Switch design

As can be seen in Figure 5.7, a set of switches is required in the design. Each of these must operate correctly in both modes of operation and still provide optimal conduction, since they are part of the power path. Correct switch implementation is a major contributor to the efficiency of the design.

In this section the important aspects of switch implementations are identified. Three aspects are then discussed in more detail. Lastly a short summary of the aspects is given.

5.7.1. Switch design aspects

For integrated circuit purposes, the switches are implemented using MOS transistors. All switches are meant to conduct power and should thus have high conductivity when active and as little leakage as possible when turned off for the best overall efficiency. The effectiveness of a switch is therefore best expressed by its on/off-resistance ratio.

The on/off-resistance ratio is determined by multiple factors. The major factors that can be adjusted by design are: the gate-source voltage, the sizing of the device and the threshold voltage.

A charge pump operates with lower voltages in earlier stages and closer to the battery level in the later stages. Therefore, switch implementation differs depending on the stage.

5.7.2. Gate-source voltage

The gate-source voltage of a transistor can be called the driving voltage, especially when the transistor is implementing a switch. NMOS devices are passively off, meaning that the off-resistance is observed when a low driving voltage is applied. In duality to this, PMOS devices are passively on and display the on-resistance when a low driving voltage is applied. The resistance, displayed once a high driving voltage is applied, is a function of the driving voltage itself. A higher driving voltage improves the NMOS on-resistance and the PMOS off-resistance. Therefore, a high driving voltage is desired for a high on/off-resistance ratio.

For all switches, the source voltage is determined by the circuit design and cannot be changed without altering the intended circuit operation. The gate voltages are control signals generated from the battery voltage during normal operation and the input voltage during cold start. As the input voltage in cold start is often low, a low driving voltage is observed. The low driving voltage increases the on-resistance for NMOS devices and lowers the off-resistance for PMOS devices. Due to this limitation in cold start, it is desired that switches that are always on during cold start are implemented with PMOS structures and switches that are always off during cold start are implemented with NMOS structures. During normal operation, a stable and high driving voltage is available to drive these switches.

Utilising only PMOS for switches that are active during cold start might not suffice on its own. If the gate-source voltage of the PMOS switch becomes close to zero, the on-resistance is reduced severely. Therefore, pulling nodes to lower potentials is not well supported by PMOS switches. A parallel NMOS is desired to pull the last charge from the higher node. Driving that NMOS switch might not be sufficient by the input voltage alone and requires a boosted voltage.

If the activated NMOS switches are needed for cold start, a small auxiliary charge pump can be used to drive these switches. Since the cold start charge pump does not require clocked switches, the active NMOS switches are not clocked either. This allows for a charge pump that has to deliver minimal power and only a high enough driving voltage, as explained before.

5.7.3. Transistor sizing

The size of a transistor affects both the on- and off-resistance. A balance must be found where the on-resistance is significantly decreased, while the off-resistance is kept maximal. The on-resistance of a general MOS transistor in strong inversion is given by Equation 5.8. With adequate driving voltage and threshold voltage management, the switches operate mostly in the strong inversion regime.

$$r_o = \frac{2L^2}{\lambda \mu C_{ox} W V_{gt}^2} \tag{5.8}$$

Here, L is the length of the transistor, W the width of the transistor, λ is the channel-length modulation parameter, μ is the charge-carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area and V_{gt} is the gate source voltage minus the threshold voltage, also known as the overdrive voltage. Of these parameters λ, μ and C_{ox} are process dependent. The threshold voltage is further discussed in the next subsection.

The W/L ratio is the main parameter that can be used to alter the resistance of the switch. Intuitively, the wider and shorter the material between the drain and source of a transistor is, the more current can flow through and thus the lower the resistance is. The optimal W/L ratio depends on the available driving voltage. If there is a high driving voltage available, the W/L can be lowered to reduce the off-resistance. The high driving voltage still allows for sufficient conductance to be reached. If a high driving voltage cannot be met, a larger W/L ratio is desired to lower the on-resistance.

5.7.4. Threshold voltage

The gate-source voltage to on/off-resistance relation is not linear: an exponential relation is observed for sub-threshold operation, whereas a more quadratic relation is seen above the threshold voltage (as seen in Equation 5.8). Due to the exponential relation, driving the transistor above threshold greatly improves the on/off-resistance ratio. Driving the transistor at even higher voltage levels aids the on/off-resistance ratio, but is not as much of an improvement as for sub-threshold operation.

Generally speaking, a low threshold voltage is desired for high on/off-resistance ratios, due to the lower on-resistance for equal driving voltages. However, the threshold can also become too low. With near zero threshold voltages, the off-resistance of NMOS is lowered so far that the on/off-resistance ratio is not improved any more.

Depending on the available technology, devices come with different threshold voltages. A technology must be chosen that has a low threshold voltage to accompany low voltage applications that still has a high enough NMOS off-resistance.

Body effect Apart from the process dependence of the threshold voltage, the bulk potential is also an important factor. The bulk potential influences the threshold voltage of the device due to the body effect:

$$V_{th} = V_{th0} + \gamma \left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|} \right) \tag{5.9}$$

Where γ is the body effect parameter, V_{th0} is the zero bias threshold voltage, V_{SB} is the source-bulk voltage and $2\phi_F$ is the surface potential. Thus, in order to lower the threshold voltage it is desired that the source to bulk voltage is negative, ideally $V_{SB} = -2\phi_F$. However, creating this negative voltage is not practical. The source voltage is not within our control, as it is determined by the system. Lowering the voltage of the bulk below the ground voltage would lead to unwanted currents in the substrate for most CMOS implementation.

The next best option is equating the bulk voltage to the source voltage. The threshold voltage is not affected by the body effect in this case, as the two terms in the brackets of Equation 5.9 cancel each other out. The simplest manner of equating the bulk voltage to the source voltage is by shorting these terminals. Shorting the bulk to either drain or source creates a diode connection between the source and drain of the transistor. For NMOS devices the diode is from the bulk to the terminals and for PMOS devices the diode is from the terminals to the bulk. This diode connection must be taken into account when designing the bulk connections. Since these switches ultimately lead to equal potential at source and drain when activated, the bulk can be connected to either drain or source to lower the threshold voltage.

5.7.5. Conclusion on switch design

Switch performance can be characterised by the on/off-resistance ratio of the switch. This ratio is determined by three main factors: the gate-source voltage, the sizing of the device and the threshold voltage.

The gate-source voltage can be called the driving voltage and must be as high as possible for good operation. The driving voltage is higher in normal operation and below the threshold voltage in cold start. Therefore, implementing switches that are actively driven in normal operation is more preferred.

The sizes of the transistors must be balanced for optimal on/off-resistance ratio. Increasing the W/L ratio lowers both the on- and off-resistance. Depending on the available driving voltage, a correct W/L ratio must be chosen.

The threshold voltage is determined by both technology and source-bulk voltage. The technology must be chosen carefully. A high on-resistance at low driving voltages is desired, but should not come at the cost of too low off-resistance. The body effect must be negated for better performance. The best approach is to lower the bulk potential below the ground potential. However, this is not practical and equating the bulk to the source or drain potential is more preferred. When connecting the bulk to either the drain or source of the transistor, a diode is created between drain and source. The diode must be taken into account during implementation.

5.8. Conclusion

In this chapter, a cold start capable charge pump that can also provide high efficiency harvesting out of cold start is designed. The main goal is to design this pump with minimal area usage. After examination, a cold start pump that is integrated with the normal operation pump is found to lead to the smallest chip area usage.

A combination between the Dickson charge pump topology and series-parallel topology is chosen. The Dickson charge pump functions as the cold start pump and the series-parallel charge pump functions during normal operation with high efficiency. The operation of the pump is examined and orthogonal operation is found. Utilising the Makowski timing scheme is possible without altering the topology.

Adaptations to the combined topology are made to boost the performance of the cold start operation without affecting the normal operation. The use of DCTS is attained for the cold start operation. Using capacitor splitting leads to orthogonalization between the amount of cold start and normal operation stages. Again, the operation is analysed and deemed sufficient for implementation.

Lastly, special attention is given to the design of the needed switches. Implementation of the switches depends on the available driving voltage and achievable threshold voltage. Possibly a small auxiliary charge pump is needed to drive NMOS switches during cold start. This pump can be designed to be very small as it does not drive clocked gates.

6

Test case

In the previous chapter, an area efficient cold start circuit has been proposed that shares the capacitors with the main harvester. The proposed design is well defined in theory, but still requires proof of operation in a realistic environment. In this chapter, a test case for the design is given.

The chapter starts by explaining the test case. After that, the parameters of the system are given from the test case. The requirements for cold start and normal operation are determined next. Lastly, an overview of the requirements is given.

6.1. Application scenario

To test the design, an existing application is taken and the boundaries of the proposed design are tested to this case. The existing application is an energy harvesting chip designed by Nowi-energy.

The design is implemented in the Cadence Virtuoso simulation environment using model files for an 180 nm technology node. Schematic simulations will be run using Cadence Spectre for varying process corners and temperatures.

6.1.1. Given parameters

The Nowi-energy harvester is designed to boost the voltage of a solar cell from roughly 450 mV to a battery voltage of 1.8 V. Using the Makowski timing scheme, two stages are needed to implement the four times boosting.

The charge pump is fully integrated in 180 nm technology. The fully integrated design allows for a total on-chip capacitance of 1 nF. The maximum available capacitance is based on size desires by Nowi-energy and previous charge pump designs that utilise similar amounts of internal capacitance. For the normal charge pump this means two flying capacitors of 500 pF each. In the chosen technology, both 2V and 5V devices are available. There are also devices with lower threshold voltage available. Triple well NMOS devices are also provided, but not for the lower threshold variants.

There is an interest to push the boundaries of the cold start system. Therefore, it was chosen to perform cold start from 100 mV. For the actual application, where the expected input voltage is around 450 mV, the design should obviously be made more lenient. Choosing a low-voltage start-up tests both the cold start capabilities and the impact on the normal charge pump. 100 mV is chosen as a minimum voltage based on in-house design.

An ideal voltage source is used to emulate the transducer. The cold start circuit is driven by an already designed cold start oscillator by G. Martins based on [10].

6.1.2. Cold start requirements

By the proposed design, it is impossible to have the cold start circuit and the normal operation charge pump active at the same time. Therefore, the cold start circuit has to provide enough energy on the storage capacitor to get the main harvester to start and become self-providing.

An estimation in agreement with Nowi has been made that 1 ms of normal pump operation must be sufficient to be self-providing. The objective of the system in this period is to become self-providing, thus not

all sub-circuits are activated yet. The required circuits and their average current consumption are given in Table 6.1. The system is designed for low power operation and therefore low current draw is expected.

Sub-system	**Current consumption**
Power on reset	5 nA
Current reference	10 nA
Oscillator (at 62kHz)	240 nA
Low drop-out regulator	125 nA
MPPT	228 nA
Charge pump	1400 nA
Total	**2800 nA**

Table 6.1: Sub-systems required during initialisation and their current consumption.

As can be seen from Table 6.1 a mere 2.8 µA is required. Most of these systems operate at 1.8 V, only the MPPT sub-system requires 3V. In the end, 3.62 nJ is required. The storage capacitor must provide this energy on top of being charged to at least 1.8 V. The storage capacitor is taken to be external with a value of 2 µF, as this fits the chosen application by Nowi. To store the required energy, the capacitor should be charged above 1.8 V by 1.004 mV.

6.1.3. Number of cold start stages

The required amount of stages for cold start can be calculated using Equation 5.6. For a first estimation the parasitic capacitance is ignored. The zero bias threshold voltage was found to be around 290 mV for the low threshold devices in the chosen technology. The expected frequency of the cold start oscillator is 20 kHz. The total on-chip capacitance is set to 1 nF. To take the total capacitance into mind, the capacitance per cold start stage can be expressed as $C_{cs} = C_{tot}/N$, with N the number of stages. Neglecting the parasitic capacitance, the output voltage can now be described as:

$$V_{outcs} = V_{in} + N_{cs}V_{clk} - V_{th} - (I_L + I_{leak}) \cdot \frac{N_{cs}^2}{f_{clk}C_{tot}} \tag{6.1}$$

Note that only one threshold voltage is subtracted, as the implementation provides the driving voltage of one additional DCTS. Two parameters are left open: the number of stages N_{cs} and the total load current as seen at the output $(I_L + I_{leak})$. The leakage current is an unknown factor that is influenced by the number of stages. With more stages, more components are required that cause more sources of leakage. On the other hand, more stages also increase the amount of current that can be supplied to the system. The exact relation between increased leakage and increased driving current is not known. Therefore Equation 6.1 is used as is, and a lower number of stages is advised for lower leakage impact. Equation 6.1 can be rewritten to express to the total load current as follows:

$$(I_L + I_{leak}) = \frac{f_{clk}C_{tot}}{N_{cs}^2}(V_{in} + N_{cs}V_{clk} - V_{th} - V_{out}) \tag{6.2}$$

The parasitics introduced by more components for the cold start charge pump also affects the normal operation. Therefore, a low number of stages is desired. However, the total load current that can be driven by the cold start charge pump should also be kept high enough to overcome the leakage in the system. Thus, an optimum between minimal number of stages and output current must be found.

Using Equation 6.2 an optimal number of stages with respect to the load current can be found. For this derivation the leakage current is not taken as a function of the number of stages. The optimal number of stages is found to be:

$$N_{optI} = \frac{2(V_{clk} - V_{th} - V_{out})}{V_{in}} \tag{6.3}$$

Assuming an ideal clock signal equal to the input voltage of 100 mV, an optimum of 40 is found. The desire to use fewer stages to reduce leakage and parasitics in normal operation require finding a lower stage number that still provides an acceptable total load current. A plot of Equation 6.2 is made with respect to the load resistance that can be driven and total output current that can be delivered. The relation can be seen in Figure 6.1.

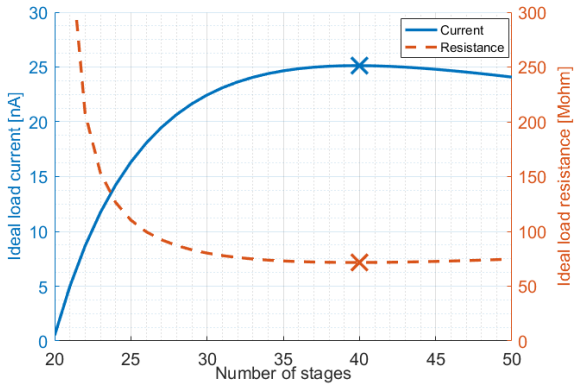

Figure 6.1: Relation between the number of stages and supported load.

In Figure 6.1 the optimum values are indicated by crosses. The supported load current and impedance display a strong decline below 30 stages. As stated a low number of stages is desired. By using 32 stages, a drop of only 1 nA from the optimal value is seen. Therefore, the final number of stages for the cold start is chosen at 32. To achieve the 32 cold start stages, the two normal operation stage capacitors are split into 16 parts. Each part has a capacitance of 31.25 pF.

6.1.4. Subsystems verification

Multiple components of the charge pump must be monitored for correct operation. As the oscillator is not the scope of the thesis, its output is taken as the best case. It is already known that for different operation temperatures and process variations the output frequency can differ and that the clock amplitude is between 90 and 99 percent of the input voltage. Only at a temperature of 85°C in the SF corner the amplitude drops to 70 mV, which is a known flaw of the oscillator.

Two components follow the oscillator before the clock signal is delivered to the flying capacitors: the buffer and the switch separating the cold start oscillator from the charge pump (called the clock switch). Both these components must not deteriorate the clock signal before it reaches the capacitors. The minimum clock amplitude to reach the buffers can be found from Equation 6.2. Setting the minimum output current to 10 nA means a clock amplitude of 78 mV is the bare minimum, assuming no parasitic capacitance and other losses in the charge pump. High losses are expected however, so a more reliable clock amplitude target would be 90 mV.

The clock switch is driven by the auxiliary charge pump. Thus, the performance of the auxiliary charge pump determines the conductance of the switch. The auxiliary charge pump should reach a stable driving voltage at least surpassing the threshold voltage. The threshold voltage for the chosen technology medium threshold devices is around 290 mV. Therefore, a boosted voltage of at least 330 mV is desired to have some headroom.

Once the subsystems reach the specifications mentioned above, the charge pump itself can be validated.

6.2. Overview of criteria

Multiple criteria are mentioned that will verify the design. A first separation is made between the normal operation performance and the performance for cold start. The cold start circuit has a number of sub-systems that must operate correctly before the charge pump itself can be validated. To close this chapter an overview of the specifications is given in Table 6.2.

Table 6.2: Design criteria.

(Sub)system	Specification	Value
Benchmark normal operation	Efficiency	>85.8%
Normal operation charge pump	Efficiency decrease	<10%
auxiliary charge pump	Output voltage	>330 mV
Buffer and clock switch	Clock amplitude	>90 mV
Cold start charge pump	Output voltage	>1.801 V
Cold start charge pump	Output current	>10 nA

7

Charge pump implementation

With the test scenario written out in the previous chapter, an implementation of the proposed design is made to fit the requirements. The implementation takes into account the available technology and criteria given in Table 6.2.

A top-down approach was chosen for the implementation. This chapter follows that top-down approach by first giving the top-level implementation. After that, the sub-systems are described in more detail. Lastly, an overview of the schematic implementation is delivered.

A lay-out of the design is also made and can be seen in Appendix B and is shortly discussed at the end of this chapter.

7.1. Top-level implementation

To achieve the correct conversion ratios, two Makowski charge pump stages and 32 cold start charge pump stages are needed. This results in each Makowski stage having 16 smaller capacitors that are connected by the DCTS and capacitor splitting switches. Both the Makowski stages begin with the normal operation switches (NO switches) and the last stage is ended with one more normal operation switch. The storage capacitor is connected after this last switch. The control is implemented by a voltage level detector (VLD) that is connected to the storage capacitor.

A schematic overview of the top-level is given in Figure 7.1. Note that two parts of the circuit are repeated 15 times. These are the DCTS, Capacitor splitter, capacitor and Cold start Buffer that make up 30 of the 32 cold start stages.

The storage capacitor is connected to the VLD that activates normal operation once enough energy is collected on the storage capacitor. The VLD initiates the normal mode operation by disabling the Cold start Oscillator and Bootstrap circuit. The VLD also signals the Capacitor splitters to re-connect the capacitors. Disabling the Cold start Oscillator and Bootstrap circuit also pulls down the Cold start Mode signal. Other support systems for the charge pump are the cold start oscillator to drive the cold start stages, the main oscillator to drive the normal operation switches and the auxiliary charge pump to drive the cold start switches.

Every cold start stage is driven by a cold start compatible buffer. The buffer ensures that the cold start oscillator has a smaller load to drive and can generate a steady, well-defined clock signal. Similarly, the normal operation switches are driven by buffers that are connected to the main oscillator.

7.2. DCTS

Most details of the DCTS implementation have already been discussed in Subsection 5.5.2. The DCTS above the NO switches must be implemented using an extra gate to prevent leakage during normal operation.

The use of medium threshold voltage devices is desired to lower the on-resistance, which increases the performance. The used technology provides both NMOS and PMOS devices that have roughly half the threshold voltage of the normal devices. There are also near zero threshold voltage devices, but these have an off-resistance that is too low. Therefore, the medium threshold voltage devices are chosen.

Another important aspect is the back bias effect as discussed in Subsection 3.4.6. Ideally, the back bias effect is negated by bringing the bulk potential to the source or drain potential of the device. Unfortunately,

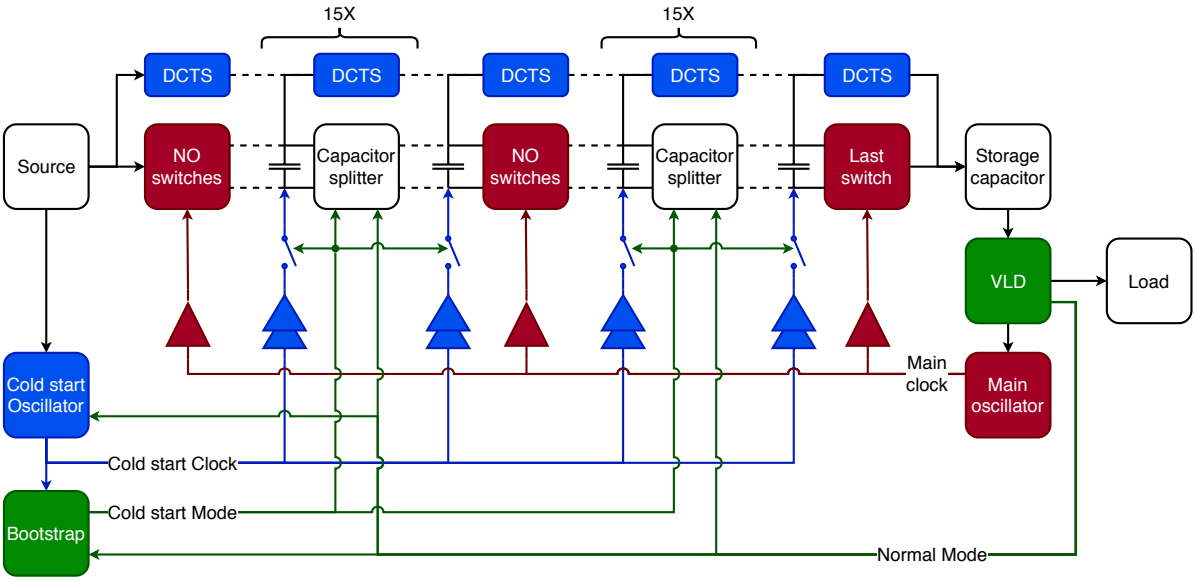

Figure 7.1: Top-level schematic of the implemented design.

the technology does not allow control of the bulk voltage of the medium threshold NMOS devices. Therefore, a PMOS DCTS implementation is applied, as these do come with a bulk that can be controlled.

7.2.1. PMOS DCTS

The duality between NMOS and PMOS devices is also found for DCTS implementation. The DCTS now connects a PMOS gate to an earlier stage, so that a larger source-gate voltage is seen and the PMOS device conducts better in the transfer phase. In the blocking phase, the gate is connected to the source again. A schematic circuit of the PMOS implementation is given in Figure 7.2, where *IN* is connected to the previous stage, *FF* to two stages earlier and *OUT* is connected to the next stage. The *DIS* signal allows for disabling of the DCTS.

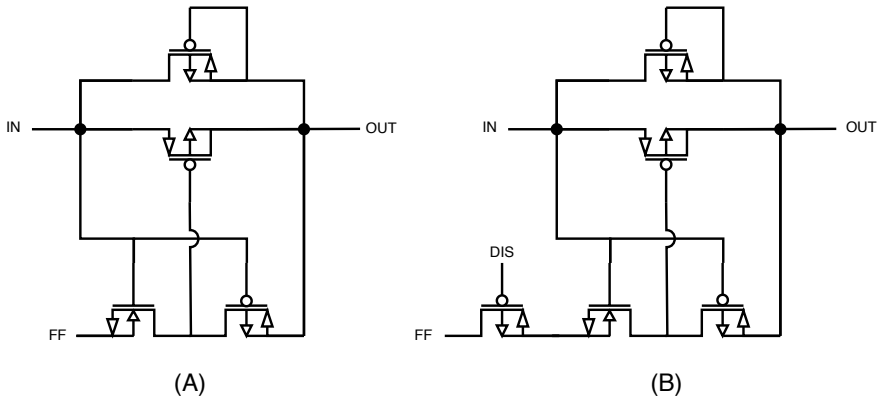

Figure 7.2: PMOS implementation of DCTS. (A) the regular DCTS, (B) DCTS that can be disabled and placed in parallel with normal operation switches.

As can be seen in the figure, there are still NMOS devices in the inverters of which the bulk is connected to the source. This connection reduces the back-bias effect and is needed for later stages to operate. These NMOS transistors are implemented using the deep N-Well devices present in the technology. Unfortunately, the deep N-well devices have a higher threshold voltage. Since the gate of one PMOS is not a large load, the normal threshold devices do not degenerate the operation of the DCTS too much.

The DCTS thus now relies on earlier stages being present. Therefore, the last DCTS stage can be implemented with ease, which was more challenging for a NMOS implementation. However, the first DCTS cannot be made. There is no clocked node available that drops to a low enough voltage. Creating this node with a

dummy stage would seem like a solution. However, this node would be pulled to a negative voltage. Negative voltages on bulk connections can lead to unwanted current flow through the system and is undesired. The first stage is now implemented using a diode connected PMOS.

7.3. Switches

As discussed in Chapter 7, five different switches need to be implemented. Each switch has to operate correctly during cold start and normal operation for the charge pump to work. As explained before, there are no NMOS devices with medium threshold voltage available of which the bulk can be controlled. Thus, a choice must be made for all NMOS implementations, whether bulk control of low zero bias threshold voltage is desired. Using the medium threshold devices can lead to lower on resistance for low driving voltage, as long as the bulk and source potential do not differ too much. If the source-bulk difference becomes too large a normal threshold deep N-well device is more desired, as the bulk voltage can then be controlled.

The switch types are indicated in Figure 7.3, where switches A, B, C belong to the normal operation pump, switches E and F are the capacitor splitters and switches D connect the cold start oscillator to the charge pump. For ease of view, the DCTS are represented by diodes in this figure.

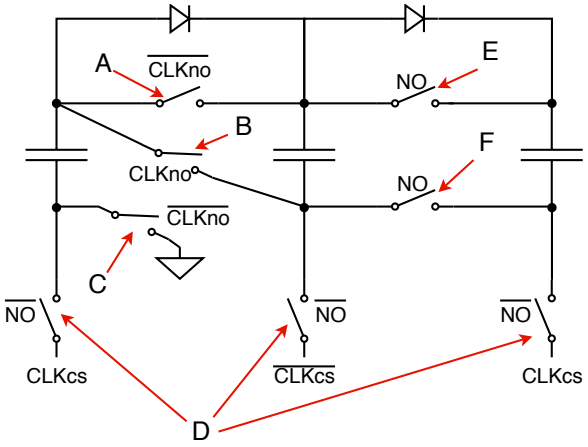

Figure 7.3: Overview of the switches present in the proposed design.

First the normal operation switches are discussed, followed by the clock switch and lastly the capacitor splitting switches are implemented.

7.3.1. Normal operation switches

Three switches separate each normal operation stage: One between the top plates of the capacitors (switch A), one from the top plate of the preceding capacitor to the bottom plate of the next capacitor (switch B) and one switch to connect the bottom plate to the ground (switch C). In normal operation these switches are all driven by a clocked signal and during cold start the switches must be disabled.

All normal operation switches are driven by a stable 1.8 V supply. Therefore, there is no need to use medium threshold devices. This allows for control of the bulk potential and lower leakage in the disabled state during cold start.

Switch A The first switch must push the following node to the potential of preceding one. The gate of this switch is driven by the main oscillator, thus at a higher potential than the input voltage. In earlier stages the source (and following drain) potential is at the input voltage and the main oscillator amplitude provides enough overdrive voltage so that an NMOS implementation suffices. Nominal threshold devices are also desired, as the driving voltage is high enough during normal operation. When the switch is deactivated, the nominal threshold devices ensure lower leakage.

Once the expected voltages at the source and drain terminals come closer to the battery voltage, a PMOS addition is desired. For these higher nodes, a pass gate is used. During cold start the PMOS gate must be driven high. The boosted driving signal from the cold start auxiliary charge pump does not reach the voltages of the later stages in the charge pump. Therefore, the later stages should drive their own PMOS gate to provide higher off-resistance. The self-driving should be inhibited during normal operation when conduction is

desired. Therefore, the PMOS gate is driven by an inverter that pulls to ground or pushes to the succeeding stage controlled by the normal operation clock. The clock must be forced to a low voltage in cold start.

The bulk connection can be made to lower the threshold voltage in any manner that does not create a diode connection from right to left. A diode from left to right is fine, since it is then always in the pumping direction, thus the anode is at the lower potential when the switch is deactivated.

The switch implementations as a function of its location in the charge pump chain is given in Figure 7.4, where (a) can be used for lower potential stages and (b) for the higher potential stages.

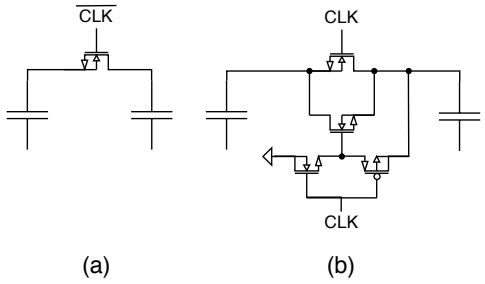

Figure 7.4: Implementation of switch A. (a) For switches where the drain and source voltages are far below the battery voltage minus the threshold voltage. (b) For nodes closer to the battery voltage.

For a Makowski charge pump implementation, the source and drain voltage as a function of the stage number is given by:

$$V_s = V_d = 2^{n-1} V_{in} \tag{7.1}$$

Where n is the stage number. The switch implementation is determined by the source and drain voltages and thus linked to the stage number. Assuming that the charge pump aims to achieve the battery voltage at its output, it follows that the last stage is driven at half the output voltage. Therefore, the first implementation as in Figure 7.4(a) suffices throughout the chain. Only the last switch, which connects the last flying capacitor to the load capacitor, requires the second implementation (Figure 7.4(b)), since this switch conducts the output voltage to the load.

Switch B Switch B is very similar to switch A and the design presented in Figure 7.4(a) is chosen. Only the bulk connection must be adapted. In this case, the diode should be connected from right to left and thus the bulk connection is moved from source to drain.

There is no need for a PMOS addition, since the highest potential seen is half the output voltage, as follows from Equation 7.1.

Switch C This switch pulls a node to ground, just like any pull-down branch in CMOS technology. An NMOS implementation is the logical choice with the bulk connected to the source, which is also the ground in this case. The ground node is always the lowest potential in the system and thus the diode connection does not cause unwanted current flow.

The resulting design of the three normal operation switches is given in Figure 7.5. All devices are normal threshold voltage devices. Switches A and B require a deep N-well to control the bulk potential. Switch C can rely on the ground potential of the substrate for the bulk. As said, only the last switch that connects the charge pump to the output is implemented as in Figure 7.4(b).

7.3.2. Switch D

The clock signal is very weak during cold start. Therefore, switch D is implemented using both NMOS and PMOS transistors. The PMOS transistor gate must be driven high during normal operation and the opposite holds for the NMOS transistor. The NMOS transistor is implemented using a medium threshold device, with its bulk to ground. The bottom plates of the capacitors only reach 100 mV during cold start independently of their position in the chain. The body effect is weak for this low voltage and thus a bulk connection to ground is used.

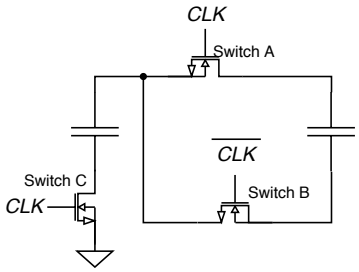

Figure 7.5: Implementation of the normal operation switches.

The PMOS device has its bulk controlled by the capacitor bottom plate voltage, as this node reaches the highest level both during cold start and normal operation. The resulting implementation is given in Figure 7.6. Here the *ModeCS* is the cold start mode signal and *ModeNO* is the normal operation signal.

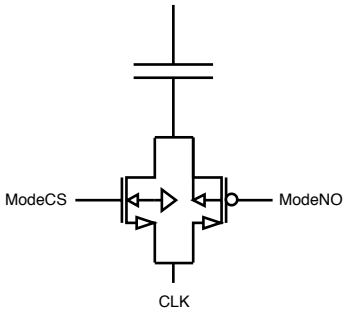

Figure 7.6: Implementation of switch D. *ModeCS* is the cold start control signal and *ModeNO* is the normal operation mode signal.

7.3.3. Splitting switches

The switches that split the capacitors (Switches E and F) are not driven by a clock, but are controlled by the normal operation and cold start mode signals. Both switches are active during normal operation at all time and connect nodes that operate at equal potentials.

Switch E Switch E is identical to switch A for the cold start circuit operation. The only difference during normal operation is at the last flying capacitor, where all the top plates can reach the battery voltage. Therefore, the switches connecting the last flying capacitor plates are all implemented as in Figure 7.4(b). The switches of the first flying capacitor are implemented as in Figure 7.4(a).

Switch F Switch F is implemented by a single NMOS device, as the bottom plate of the last flying capacitor only rises to half the output voltage. One adjustment must be made to the bulk connection. During cold start the drain and source of the transistor are driven by opposite clock phases, thus no diode connection in either direction is allowed. Therefore, the bulk is driven by an inverter that connects either to the source during normal operation or the ground during cold start.

The implementation of the capacitor splitting switches is given in Figure 7.7. For the first Makowski stage the low voltage implementation is used and for the second stage, the high voltage implementation is used.

7.4. Auxiliary charge pump

The auxiliary pump delivers the cold start mode signal. The signal is mainly used to drive the clock switches that separate the cold start buffers from the bottom plates of the flying capacitors. The other use is in the Capacitor splitters, where the signal controls the inverter that sets the gate voltage of switch F.

7.4.1. Design

The load current is minimal, as only gates are driven and there is no dynamic power consumption. As the load current is small, more focus can be put on a small footprint for the charge pump. The use of DCTS is to

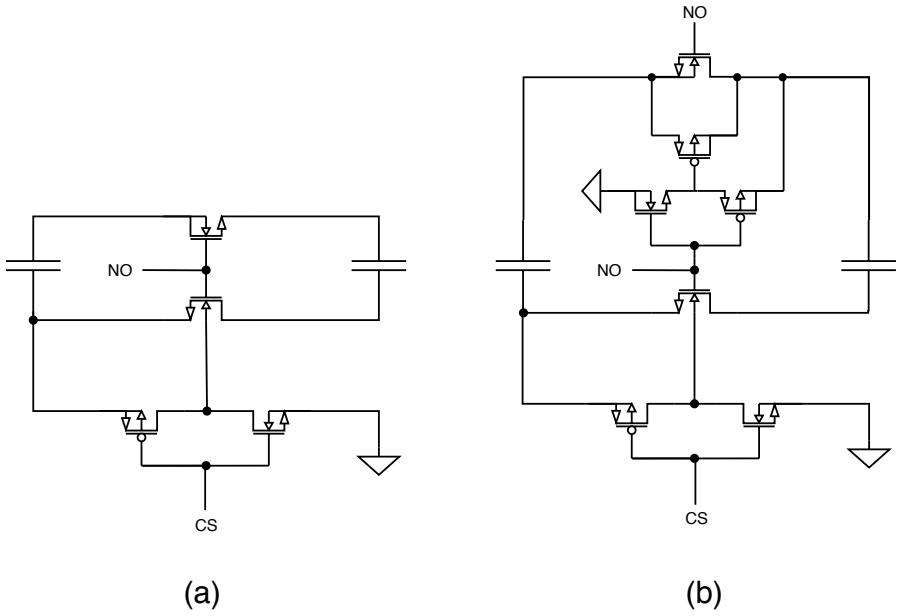

Figure 7.7: Implementation of capacitor splitting switches. (a) for low voltage nodes and (b) for high voltage nodes.

boost the amount of power that can be outputted by a charge pump, but also increases the back leakage of the pump. Therefore, the auxiliary pump does not utilise DCTS. With the small load current that is expected, the threshold voltages of the diode connected devices will not inhibit the operation of the pump. The small current that is delivered in the sub-threshold operation of the diode connected devices is sufficient to deliver the load current.

To achieve the desired output voltage from a 100 mV source, four times boosting is required. This boosting ratio also ensures enough headroom. To implement a four times boosting cold start compatible charge pump, a simple Dickson charge pump is chosen of four stages. The utilised flying capacitors can be made small, as the load does not draw much current. The cold start oscillator should not directly drive the bottom of the flying capacitors in the auxiliary charge pump. Therefore, buffers are utilised in the pump.

Once normal operation starts, the output must be pulled to ground. The cold start oscillator is also stopped, so no extra power is delivered to the charge pump. To ensure the signal goes low, a pull down NMOS transistor is added at the end of the charge pump that is activated by the *Normal Mode* signal.

7.5. Buffers

Three different buffers are used: for the NO switches, the cold start clock and the auxiliary charge pump. The implementation of these buffers is discussed in this section.

7.5.1. Normal operation buffers

During normal operation a steady 1.8 V supply is available. The buffers are driven by the main oscillator and solely have to drive the gates of the NO switches. Therefore, these buffers are implemented with small size devices and low power consumption. Two inverters in cascade are sufficient.

The buffers must output a low potential during cold start, so that the NO switches are all deactivated. The non-inverting nature of the implemented buffer fulfils this purpose, as the main oscillator pulls to ground during cold start.

7.5.2. Auxiliary charge pump buffers

The auxiliary charge pump buffers are active during cold start. The buffers are driven by the cold start oscillator and use the source voltage of 100 mV to operate. The auxiliary charge pump is powered through these buffers, thus they cannot be of minimal size. The size does not have to be too large, since the auxiliary charge pump requires little power to operate.

The buffer is implemented using medium threshold devices to account for the low driving voltage. Two inverters in cascade are sufficient, where the second inverter is three times the size of the first.

A stacked inverter approach is chosen for the cold start oscillator [10]. The stacked inverters allow for a better clock amplitude, but also increase the power consumption of the inverter. The increased power consumption comes from the higher input capacitance and increased leakage, as the paths to ground and VDD are doubled. From tests, it was found that a non stacked inverter was sufficient for the chosen voltage level and achieved lower power consumption. The details of these tests will be discussed in greater detail in Chapter 8.

7.5.3. Cold start buffers

The cold start buffers provide the power to the charge pump during cold start. Therefore, a strong driving power is required. The buffers are supplied with 100 mV and are driven by the cold start oscillator. The load of these buffers is a capacitance of at least 31.25 pF, which are the split flying capacitors. Similar as for the auxiliary charge pump buffers, it was found that the stacked topology did not aid the operation of these buffers and would be a penalty to the power consumption. When attempting to cold start from lower voltages, the stacked topology should be revised.

During normal operation the cold start oscillator is disabled and thus the buffers only have a static leakage current. The output of the buffers is connected to the clock switch and thus not of concern for operation.

To drive the larger load, a tapered buffer design is used. Medium threshold devices are used to account for the low supply voltage.

7.6. Lay-out

The major goal of the combined charge pump is to achieve minimal silicon area use for both a cold start compatible and high efficiency charge pump. The final area usage is determined by the lay-out. As discussed before, the majority of the silicon area is determined by the capacitors used. The total available capacitance of 1 nF is used and thus determines the majority of the area.

The capacitors in the chosen technology are implemented using the fifth and sixth metal layers, with an insulation layer in between. The lower layers are still available below the capacitors. Most sub systems can thus be integrated underneath the capacitors. Only the auxiliary charge pump cannot be placed there, as it has capacitors of its own.

In Appendix B, an image of the lay-out of the system is provided. As can be seen, the lay-out area is almost completely determined by the capacitors.

7.7. Overview

The circuit design is performed with a top-down approach. For the given technology, lower threshold devices are available, but the NMOS device with lower threshold does not allow for bulk potential control. Therefore, the cold start charge pump is implemented using a PMOS DCTS scheme.

The switches used in the proposed design have to operate correctly in both cold start and normal operation. For each switch, a different implementation is chosen. Some switches have multiple implementations, depending on their location in the charge pump. Later stages operate with higher voltages and thus require a different implementation.

An auxiliary charge pump is deemed necessary to aid the NMOS device used in the clock switch. The added area of the auxiliary pump is undesired. Finding a method in which the clock switch can be implemented without the needed higher voltage will be sought in future work. Due to the low loading of the auxiliary charge pump, a small implementation is possible.

A set of buffers is needed to convey the clock signals. These buffers play an important role during cold start, as the power flows through the buffers. Stacked inverters are not used in the current design as the input voltage is not too low. Utilising normal inverters leads to less energy losses in the buffers.

The last step of implementation is the lay-out. The majority of the area is defined by the capacitors and cannot be optimised further. All parts that are not capacitors can be implemented below the flying capacitors and therefore do not add to the total area.

8

Results

Using Cadence Spectre, the implemented system is tested. Five process corners are tested: Fast-Slow (FS), Fast-Fast (FF), Typical (TT), Slow-Slow (SS) and Slow-Fast (SF), where the first symbol stands for the behaviour of the NMOS devices and the second symbol for the PMOS devices behaviour. The system is tested at three different temperatures: −10°C, 27°C and 85°C. With this, a total of 15 test points are obtained that cover the most extreme cases in which the system operates.

This chapter begins with the test set-up that is used to measure the normal operation performance. After that, the results for normal operation of the proposed design are given. Next, the test set-up for cold start verification is given. The operation of the sub-systems for cold start are examined first, followed by the cold start performance itself.

8.1. Normal operation verification

To gauge the normal operation performance, the efficiency is measured. The efficiency is a metric of the energy put into the device and the energy that is delivered at the output. For energy harvesting purposes the efficiency should be as high as possible.

In order to compare the efficiency of the proposed design, a benchmark is first set. The benchmark system is a Makowski charge pump without the cold start capability. The benchmark must be aimed to achieve maximum efficiency for the given input voltage, resistance and the given operation frequency. The proposed charge pump is tested for the same parameters.

As will be later discussed in the set-up, the voltage at the output of the charge pump is fixed by a voltage source. This fixed voltage is lower than the attainable voltage by the charge pump. Due to this, the maximum attainable efficiency is determined by the switch losses, as explained in Section 3.4. The benchmark efficiency should not be lower than 97.5% of the maximum attainable efficiency to ensure the benchmark represents a desirable scenario.

8.1.1. Test set-up

The general test set-up for normal operation is given in Figure 8.1. The input and output currents are indicated by arrows.

In the set-up, an ideal voltage source (Vin) with a series resistor (Rin) models the source. A decoupling capacitor (Cdec) is used to account for the ripple introduced by the switching. At the output the storage capacitor (Cout) of 2 µF and a voltage source (Vout) is present that emulates a battery being present. The output voltage is forced to be below the maximum voltage in the charge pump to emulate a battery that needs charging.

The input power is determined by the current drawn from the source and the output power by the current that runs through the output source. The power provided to the supporting systems must also be taken into account. The current drained from the battery by these supporting systems is isolated in the test set-up for more insight in the power usage. The largest power consumer of the supporting systems would be the normal operation oscillator. To measure the consumption of the oscillator, the clock signal is fed through a buffer. The consumption of the buffer is used as a measure for the power provided by the oscillator to drive the charge pump. The charge pump might pose a different load, once the proposed design is used. The buffer then feeds

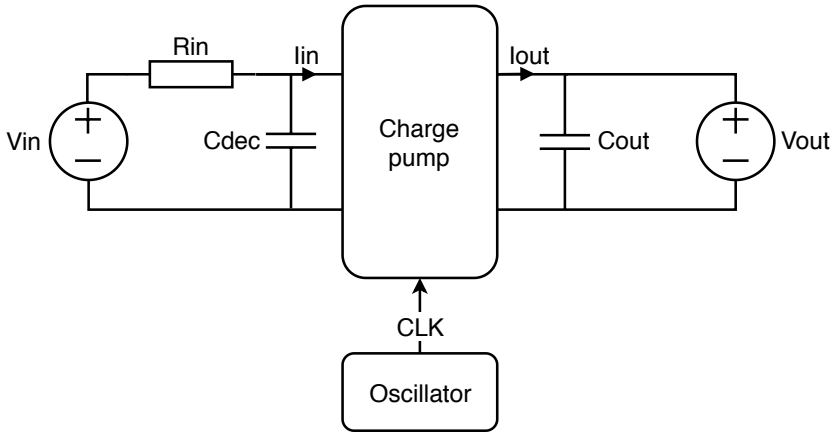

Figure 8.1: Test set-up to measure the efficiency of the charge pump.

this different load and the oscillator does not have to support a different load. The system efficiency can be calculated by:

$$\eta = \frac{I_{out}V_{out}}{I_{in}V_{in} + I_{bat}V_{bat}} \tag{8.1}$$

Where I_{in}, I_{bat} and I_{out} are the input current, battery current and output current respectively and V_{in}, V_{bat} and V_{out} are the input voltage, battery voltage and output voltage, respectively. The battery current is drained by the support systems to drive the charge pump.

The emulated output storage is set to a voltage of 1.6 V, thus 0.2 V below the ideal output of the charge pump. Using Equation 3.2, a maximum attainable efficiency of 88% is found. 97.5% of the optimal efficiency was chosen as the criterion, which leads to a criterion of 85.8% as the minimum efficiency for the benchmark charge pump.

8.1.2. Hypothesis

Introducing new elements into the charge pump inherently lowers the efficiency due to the added parasitics. However, not all parts are equally influential. The capacitor splitters are directly in the power path and conduct the majority of the current during normal operation. Therefore, the capacitor splitters will have the largest influence on the efficiency. The DCTS are in a parallel path and their diode behaviour will likely aid the conduction between parts of a split capacitor, thus reducing the negative impact of their parasitics. The clock switches are away from the power path and will thus only introduce a parasitic capacitor and minimal leakage.

The added parasitics should be minor compared to the used total capacitance. With correct implementation of all switches the efficiency loss is expected to be less than 10 percent. It is expected that the capacitor splitters have the most effect on the efficiency, followed by the DCTS and lastly the clock switches.

8.1.3. Benchmark results

The voltages are set by design and the currents are measured using simulation. The efficiency is calculated from these results using Equation 8.1. The resulting efficiencies for all operating points are given in Table 8.1. For the measurement, a source resistance of 18.1 kΩ was utilised to match the impedance of the charge pump. For all operating points a required input power of 10.9 µW was found.

Table 8.1: Benchmark efficiency of a standard two stage Makowski charge pump.

	−10°C	**27**°C	**85**°C
FS	86.33%	86.44%	86.40%
FF	84.92%	84.93%	84.66%
TT	86.17%	86.34%	86.36%
SS	87.73%	88.01%	87.77%
SF	86.26%	86.56%	86.34%

For the typical case, the resulting efficiency of the charge pump is 86.53%. In Section 8.1 the maximum attainable efficiency was calculated at 88%, making the implemented charge pump 1.5% below optimum.

Capacitor transient A full clock cycle of the charge pump operation is given in Figure 8.2. The top plate voltage of the second stage seems to reach a high voltage during the charging phase of the first capacitor. This is not a correct representation of the charge present on the capacitor, as the bottom plate is floating in this phase.

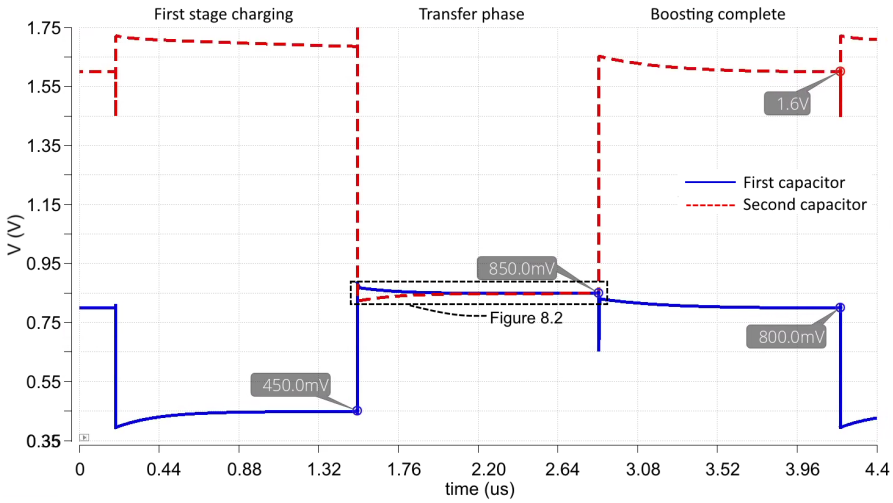

Figure 8.2: Top plate voltages of the first and second Makowski stage during a complete clock cycle. The phases are indicated above the graph. Only the typical case is given.

The performance of the normal operation switches is indicated by the transient voltage during the transfer phase. The transient response of the benchmark can be used to verify the performance of the normal operation switches and capacitor splitters in the proposed design. Figure 8.3 is a zoom in of Figure 8.2 of the transfer phase. In this phase, the charge accumulated on the first capacitor is pushed to a double voltage by connecting the first capacitor in series with the input. At the same time, the second capacitor top plate is connected to the top plate of the first capacitor. The boosted voltage is therefore distributed over the two capacitor top plates. A potential difference of 0.02 mV is seen between the two capacitors at the end of the transfer phase.

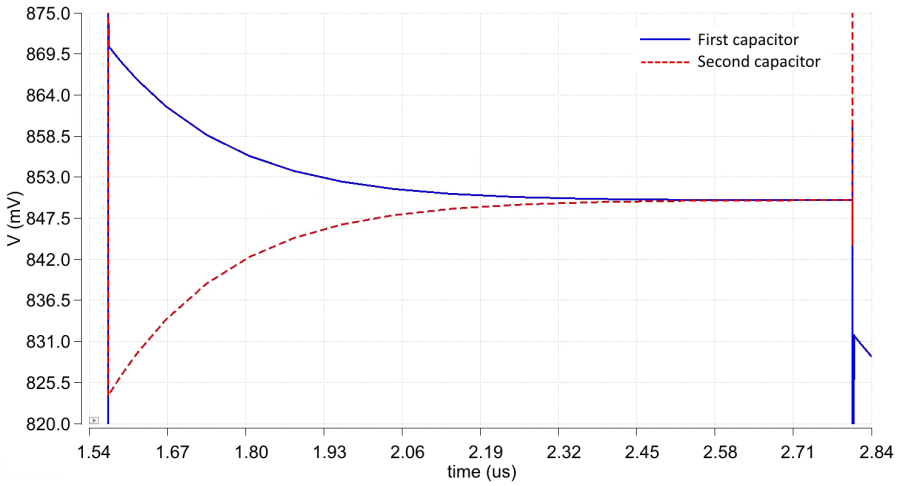

Figure 8.3: Zoom in of Figure 8.2 of the transfer phase, giving the top plate voltages of the first and second Makowski stage. Only the typical case is given.

The voltages on the capacitors require time to reach the final voltage difference between the two capacitors. The voltage on both capacitors follows an asymptotic behaviour, as a smaller voltage difference gener-

ates a smaller current flow between the capacitors. Therefore, the voltages only reach equilibrium at infinity. The settling time is therefore defined as the time required to reach 90% of the final voltage at the end of the transfer phase. For the typical case, a settling time of 459 ns is seen.

The settling times and voltage differences at the end of the transfer phase for all test points are given in Table 8.2.

Table 8.2: Settling times and capacitor voltage difference at the end of the transfer phase of the benchmark charge pump.

	Settling time			**Capacitor voltage difference**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	373 ns	426 ns	514 ns	0.01 mV	0.02 mV	0.06 mV
FF	656 ns	327 ns	395 ns	0.00 mV	0.00 mV	0.01 mV
TT	399 ns	459 ns	553 ns	0.01 mV	0.02 mV	0.11 mV
SS	543 ns	621 ns	718 ns	0.07 mV	0.23 mV	0.71 mV
SF	430 ns	495 ns	589 ns	0.02 mV	0.05 mV	0.20 mV

8.1.4. Proposed design results

The proposed design draws 11 µW in all test points and delivers around 9 µW depending on the efficiency of the operation point. The efficiency is again calculated using Equation 8.1 and the measured currents. The resulting efficiency is given in Table 8.3. In the same table the efficiency loss compared to the benchmark is given.

Table 8.3: Efficiency of the proposed charge pump in normal operation. Efficiency loss compared to a standard Makowski charge pump.

	Efficiency			**Efficiency loss**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	83.57%	82.94%	77.40%	2.77%	3.50%	9.00%
FF	81.86%	81.21%	71.57%	3.06%	3.72%	13.09%
TT	83.57%	83.17%	79.33%	2.60%	3.16%	7.03%
SS	84.29%	83.99%	81.80%	3.44%	4.02%	5.97%
SF	83.51%	83.12%	78.58%	2.75%	3.43%	7.76%

The current flowing through the DCTS and clock switch are also measured during normal operation. The DCTS did not conduct a measurable current during normal operation. The clock switches conducted on average 5 nA.

Capacitor splitters The voltage transient of the split capacitors top plates is simulated to visualise the performance of the capacitor splitters. Figure 8.4 illustrates the voltage on the top plates of the split capacitors during the transfer phase, just as was done for Figure 8.3. The top bundle of voltages represents the first Makowski stage and the lower bundle the second Makowski stage. Within these bundles, the highest line is the first split capacitor and the lowest the last. The other lines represent the other split capacitors in ascending order from top to bottom.

Three aspects of Figure 8.4 are of interest: The settling time, the voltage difference between the first and second capacitor at the end of the transfer phase and the voltage difference within one split capacitor at the end of the transfer phase. The voltage difference between the first and second capacitor follows an asymptotic behaviour over time. Therefore, the final value never reaches zero and the system never fully settles. The settling time is defined as the time it takes the last capacitor to reach the 90% of the final voltage from the beginning of the transfer phase. Each of these three aspects is given in Table 8.4 for all corners. In the table, the stage voltage difference refers to the difference between the first and second Makowski stage. The split voltage difference refers to the largest voltage difference within one split capacitor. The transient behaviour as given in Figure 8.4 of the slowest operation point (SS at −10°C) and fastest operation point (FF at 85°C) in comparison with the typical case are given in Appendix A.

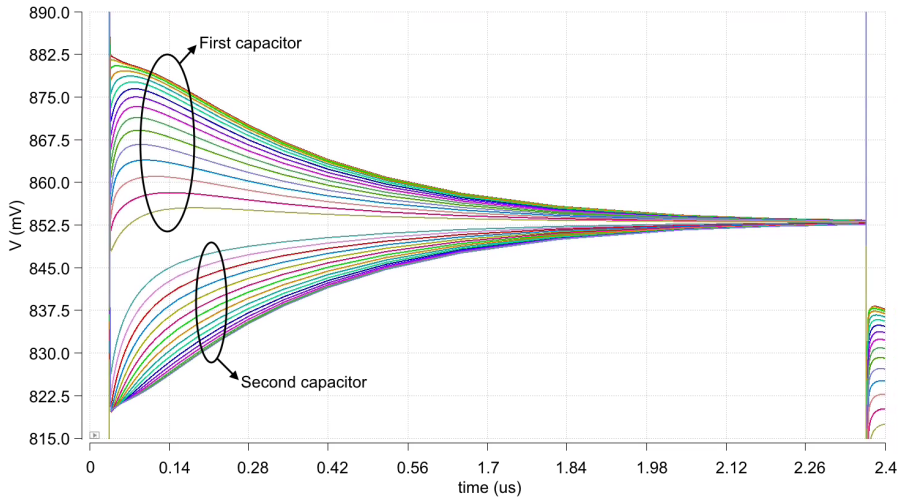

Figure 8.4: Top plates of the split capacitors voltage behaviour during the transfer phase, at the same moment as for Figure 8.3. Only the typical case is given. The top bundle of voltages represents the first Makowski stage and the lower bundle the second Makowski stage.

Table 8.4: Measurements of the split capacitor plates during the transfer phase. The settling time is defined as the time to reach 90% of the final voltage reached in the transfer phase.

	Settling time			**Stage voltage difference**			**Split voltage difference**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	623 ns	703 ns	796 ns	0.02 mV	0.06 mV	0.24 mV	0.06 mV	0.15 mV	0.55 mV
FF	478 ns	546 ns	652 ns	0.00 mV	0.00 mV	0.01 mV	0.00 mV	0.00 mV	0.02 mV
TT	666 ns	741 ns	836 ns	0.03 mV	0.13 mV	0.33 mV	0.07 mV	0.31 mV	0.79 mV
SS	858 ns	915 ns	994 ns	0.34 mV	0.58 mV	1.03 mV	0.80 mV	1.35 mV	2.43 mV
SF	711 ns	775 ns	872 ns	0.10 mV	0.22 mV	0.49 mV	0.23 mV	0.51 mV	1.14 mV

8.2. cold start verification

For the cold start circuit, a test is designed to first determine if the charge pump is operational. Operation is deemed successful once a stable output voltage is seen on the load capacitor of above 1.8 V without a load current present.

Next, the maximum drivable load can be found. A parallel voltage source to the load capacitor emulates the load, quite similar to the normal operation set-up. From Figure 6.1, a total load current of 24 nA should be possible. However, this current includes all losses in the system. The actual current flowing out of the charge pump into the load is thus a lot lower. Cold start systems are often highly inefficient and losing more than three quarters of the input power to losses internally is not unheard off. The final output current that the charge pump can deliver must be positive. A fitting storage capacitor should be sought that has a leakage not higher than the delivered current. For small capacitors that can form an intermediate storage, a leakage of 10 nA is the minimum leakage. Thus, the charge pump must deliver at least 10 nA at the output for implementation to succeed.

8.2.1. Test set-up

The general set-up for the operational test is given in Figure 8.5. An ideal voltage source (Vin) is used to emulate the energy source. The load is emulated by a load capacitor (Cout) and a voltage source (Vout) in parallel. The voltage source is replaced by a resistor when measuring the start-up time. The buffer is of essence in this set-up, since the power in a Dickson charge pump flows through the oscillator. The cold start oscillator is not designed to drive a large load and cannot support the charge pump on its own. A buffer is used that can provide sufficient current to drive the charge pump.

As the cold start circuit implements NMOS switches that must be driven with a higher voltage, an auxiliary charge pump circuit is used. The produced signal by this charge pump must be sufficient to drive the NMOS switch. Measuring the performance of the auxiliary charge pump will be discussed later. The NMOS switch should pose a sufficiently low on-resistance while driven by the signal. The NMOS switch is not driven by a

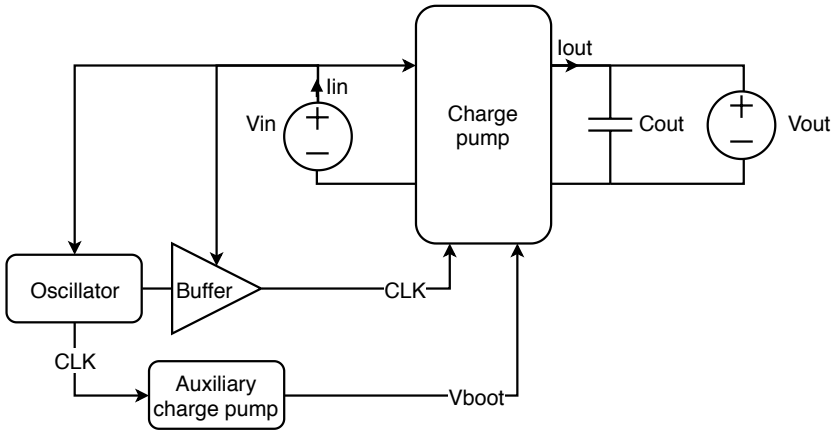

Figure 8.5: Test set-up to assess if cold start can be achieved.

clock signal and simply kept active during cold start. This means that no dynamic power is consumed from the auxiliary charge pump and only static losses are present. Therefore, the auxiliary pump does not have to provide a lot of power and can thus be designed with minimal area occupation.

The efficiency of the charge pump is measured using the current drawn from the source and the current delivered to the load. The total input power is distributed over the oscillator, buffer, bootstrap circuit and charge pump input.

8.3. Cold start oscillator results

Although the design of the cold start oscillator is not part of this work, its results are of importance for evaluating the performance of the blocks driven by the oscillator. Therefore, the oscillator performance is given first.

The used cold start oscillator performs well in all but one corner. The frequencies differ greatly for different test points. The amplitude of the clock signal also differs slightly for all corners. The found frequencies and amplitudes are given in Table 8.5.

Table 8.5: Clock frequencies and amplitudes of the cold start oscillator for different operation corners.

	Clock frequency			**Clock amplitude**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	4.8 kHz	29.6 kHz	220.3 kHz	96.3 mV	94.9 mV	92.1 mV
FF	35.7 kHz	156.5 kHz	802.5 kHz	99.5 mV	98.8 mV	96.8 mV
TT	8.2 kHz	43.6 kHz	286.6 kHz	99.8 mV	99.3 mV	98.3 mV
SS	1.5 kHz	10.1 kHz	88.0 kHz	99.7 mV	99.4 mV	98.6 mV
SF	7.0 kHz	38.4 kHz	258.7 kHz	95.7 mV	89.1 mV	69.9 mV

From Table 8.5 it can be seen that high temperatures and faster operating devices lead to higher frequencies. What also stands out is the typical case (TT at 27°C) has a frequency of 43.6 kHz, which is twice the frequency that was assumed during the implementation phase.

The clock amplitude is above 98% of the input voltage for most corners. For lower temperatures and thus slower test points, a higher amplitude is seen. For the process corners a similar speed to amplitude relation is seen, except for the cross corners (SF and FS). The cross corners also display a different duty cycle upon closer inspection. The SF process corner at 27°C has a clock signal with a duty cycle of 61%.

8.4. Cold start sub-systems results

Multiple supporting systems are present during cold start. The first of these sub-systems are the buffers. The buffers receive the oscillator signal as their input and replicate the oscillation at their outputs. The replicated output is delivered by a larger device and can therefore handle a larger load than the oscillator could.

In this section the results of the buffers are given first. After that, the auxiliary charge pump measurements are given. Lastly, the clock switch performance is given. The section concludes with the final clock amplitude

that reaches the charge pump.

8.4.1. Auxiliary charge pump buffers

The auxiliary charge pump buffers are reviewed first. Table 8.6 gives the amplitude of the clock signal at the output of these buffers for each operating point. The auxiliary charge pump is designed to provide four times boosting of the input voltage. The ideal reachable output voltages with four times boosting from the found clock amplitudes is also given in the table.

Table 8.6: Clock amplitudes after the auxiliary buffers and the maximum reachable output voltage from these amplitudes by four times boosting.

	Clock amplitude			**Ideal boosted voltage**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	94.6 mV	93.3 mV	89.8 mV	378.4 mV	373.2 mV	359.2 mV
FF	97.7 mV	95.8 mV	89.8 mV	390.8 mV	383.2 mV	359.2 mV
TT	98.2 mV	96.9 mV	92.7 mV	392.9 mV	387.6 mV	370.8 mV
SS	98.3 mV	97.3 mV	94.4 mV	393.2 mV	389.2 mV	377.6 mV
SF	86.5 mV	75.3 mV	44.8 mV	346.0 mV	301.2 mV	179.2 mV

All of the operating points achieve a lower voltage after the buffer than before, especially the SF process corner at 85°C shows a low amplitude. What can also be seen is that the SF process corner at 27°C and 85°C do not reach the criterion of 330 mV.

8.4.2. Cold start buffers

Table 8.7 gives the amplitude of the clock signal after the cold start buffer. The losses due to the buffers as a percentage of the oscillator output amplitude are also given. Minor losses are seen in most of the test points. The SF process corner at 85°C displays a significant loss of 61%.

Table 8.7: Clock amplitude and amplitude loss in the cold start buffers.

	Buffer output amplitude			**Buffer loss**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	91.3 mV	91.3 mV	89.5 mV	5%	4%	3%
FF	98.0 mV	95.4 mV	86.0 mV	2%	3%	11%
TT	96.7 mV	96.2 mV	91.1 mV	3%	3%	7%
SS	96.3 mV	95.0 mV	93.1 mV	3%	4%	6%
SF	85.8 mV	75.5 mV	27.2 mV	10%	15%	61%

Stacked inverters The oscillator is build utilising stacked inverters and produces a higher amplitude. To illustrate the difference between a stacked inverter buffer and a regular inverter buffer, two measurements are done. First, the output swing of the second last and last inverter of a regular buffer is measured. Next, a stacked inverter implementation is measured at the same points. The output of the second last inverter is the input of the last inverter. The simulation is run for the TT process corner at 27°C.

The sizes of the inverters are different, since one utilises a stacked topology and the other utilises a regular topology. The tapering throughout the buffer is kept the same for both implementations. The results of the second last inverter output are given in Figure 8.6A and the resulting output of the last inverter is given in Figure 8.6B.

As can be seen in Figure 8.6, the regular inverter has faster rise and fall times, but achieves lower amplitudes in the second last inverter. The output of the stacked inverter buffer is lower than that of the regular inverter.

For the SF process corner at 85°C an increase in amplitude was measured with the stacked implementation. The stacked implementation loses 41% of the amplitude delivered by the oscillator, compared to the 61% loss seen with the chosen implementation. However, all other process corners have an increased amplitude loss with the stacked implementation.

The power consumption of the buffers is measured as well. The second last stage and last stage consumption is separated. The power is measured at the ground node of the inverters in the buffers. The pulling down

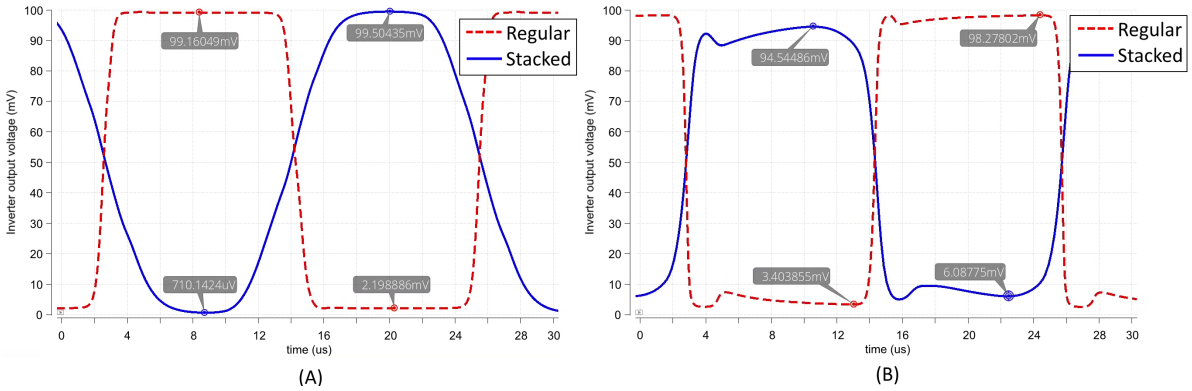

Figure 8.6: Output signal of the inverters in the cold start buffers. (A) The second last inverter output, thus also the input of the last inverter. (B) The output of the buffer. Both a stacked and regular inverter implementation are given.

thus determines the power that is consumed. From the power supply a larger power flow is seen, but this power is also fed to the charge pump and is thus not seen as leakage. The resulting power consumption of the normal buffer is 1.42 nW in the second last stage and 4.25 nW in the last stage. The stacked inverter buffer consumes 2.70 nW in the second last buffer and 13.47 nW in the last stage.

8.4.3. Auxiliary charge pump

The output voltages of the auxiliary charge pump are given in Table 8.8. The losses compared to the ideal output voltages found in Table 8.6 are given as well. These losses can be used as an indication for the leakage in the charge pump. The output voltages are not reached instantly and require a rise time mainly determined by the provided frequency from the cold start oscillator. The rise times are a fraction of cold start output voltage rise time.

Table 8.8: Final output voltage provided by the auxiliary charge pump after settling and the losses compared to the ideal achievable voltage found in Table 8.6.

	Charge pump output			**Difference from ideal**		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	274 mV	348 mV	325 mV	104.4 mV	25.2 mV	34.2 mV
FF	386 mV	365 mV	320 mV	4.8 mV	18.2 mV	39.2 mV
TT	380 mV	375 mV	340 mV	12.9 mV	12.6 mV	30.8 mV
SS	264 mV	359 mV	348 mV	129.2 mV	30.2 mV	29.6 mV
SF	329 mV	276 mV	152 mV	17.0 mV	25.2 mV	27.7 mV

Quite a range of results is obtained. No operating point reaches the optimal 400 mV and all reach a voltage above the input voltage of 100 mV. The FF process corner at −10°C comes closest to the ideal output with 386 mV. The SF process corner at 85°C performs the worst by far.

A ripple is seen in the output voltage that correlates with the oscillation frequency across all test points. The ripple is no more than 5% of the average output voltage for all test points.

The current flow through the auxiliary charge pump is measured as well. An average current of 5.13 pA is flowing out of the charge pump once a steady voltage is reached for the typical case. This output current is the load current imposed by the system. The auxiliary buffers that power the auxiliary charge pump consume 8.67 nA on average in steady state.

8.4.4. Clock switch

The last sub-system is the clock switch that is essential for separation between cold start and normal operation. During normal operation it is deactivated and the losses through the switch during normal operation have already been represented in Subsection 8.1.3. For cold start, the propagation of the clock signal through the switch is given in Table 8.9.

As can be seen from the table, the FF and TT process corners at 27°C cause no measurable drop in amplitude. For all other corners the drop is low as well. Only the SF process corner at 85°C stands out. Here a larger

Table 8.9: Amplitude drop of clock signal when passing the clock switch.

	−10°C	**27**°C	**85**°C
FS	0.11%	0.11%	0.22%
FF	0.08%	0.00%	0.59%
TT	0.10%	0.00%	0.33%
SS	1.56%	0.21%	0.54%
SF	0.38%	1.46%	14.71%

drop of 14.71% is seen.

NMOS and PMOS The clock switch consists of one NMOS and one PMOS device. The transient current flow through these switches is given in Figure 8.7. Four clock phases and thus two pumping cycles are given. The measurement is performed after a stable output voltage is reached for the typical case. Three spikes in current are seen each clock cycle, indicated with three letters.

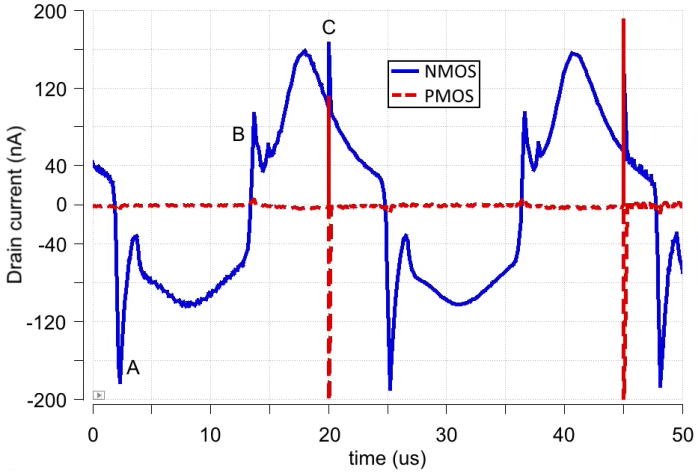

Figure 8.7: Current flow through the NMOS and PMOS drains of the clock switch. Four clock cycles are given for the typical case. Positive current flows from the cold start buffer to the charge pump.

8.4.5. Final clock amplitude

After all sub-systems, the clock signal reaches the bottom plates of the flying capacitors. Here, the clock signal is converted into the boosted voltage by the charge pump. The final clock amplitude seen at the bottom of these capacitor plates is given in Table 8.10.

Table 8.10: Final clock amplitude seen after the cold start support blocks that is applied to the bottom plates of the flying capacitor.

	−10°C	**27**°C	**85**°C
FS	91.2 mV	91.2 mV	89.3 mV
FF	97.9 mV	95.4 mV	85.5 mV
TT	96.6 mV	96.3 mV	90.8 mV
SS	94.8 mV	94.8 mV	92.6 mV
SF	85.5 mV	74.4 mV	23.2 mV

8.5. Cold start operation results

With the results of each sub-system given, the overall performance of the charge pump for cold start can be given. As with the normal operation analysis, the power supplied to the input of the charge pump and the power supplied to the support systems are measured separately.

To give a general indication of the performance, the output voltage over time of charging a load capacitor is given in Figure 8.8. For this test the load capacitor was set to a value of 50 pF to achieve a shorter simulation time. The final output voltage does not change with a different ideal capacitor size as the output voltage is not a function of the load capacitance. Only the rising time of the system changes, as a larger capacitor requires more charge to achieve the same voltage.

In parallel with the ideal capacitor a load resistor of 74.2 MΩ is set to emulate the leakage of a realistic capacitor. The parallel resistor does have a major effect on the output voltage, as it sets the load current. The resistor value was chosen based on the found load current at 1.8 V that will be discussed later. After 90 ms a stable voltage is reached.

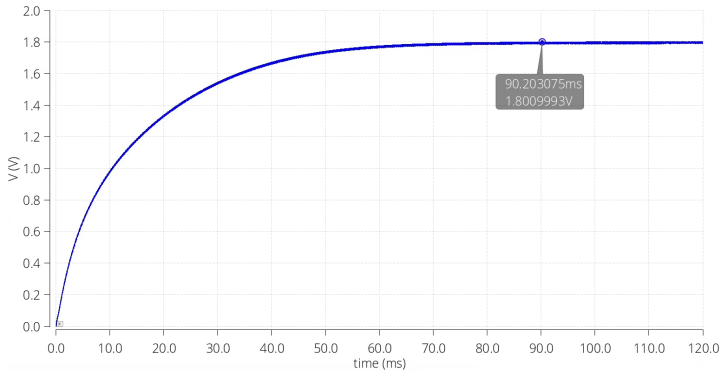

Figure 8.8: Output voltage of the cold start operation charging a load capacitor. The capacitor value is 50 pF and the parallel resistance for this test is set at 74.2 MΩ.

Split capacitor transient Apart from the rising voltage, the voltage on each of the split capacitors is of interest. The transient voltage on the split capacitors is given in Figure 8.9. The figure displays the voltages once a steady output signal is reached. Four clock phases are given that represent two pumping cycles. In total, 32 pumping cycles are needed for charge to reach the output from the input.

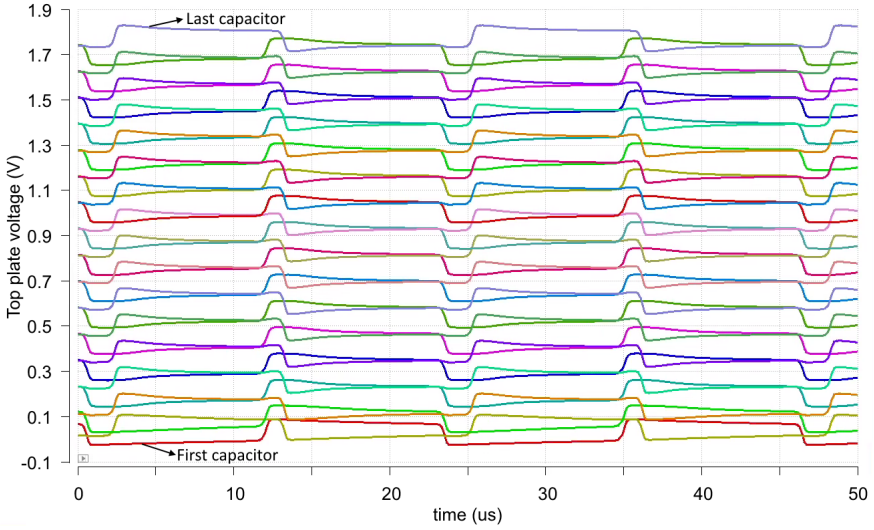

Figure 8.9: Voltage transient of the top plates of the split capacitors in cold start operation once steady state is reached. The first capacitor corresponds with the lowest signal; the second capacitor corresponds with the second lowest signal and so on.

8.5.1. Power and efficiency

Table 8.11 gives the measured input power, output current and efficiency in each operating point for an output voltage of 1.8 V. The SF process corner at 27°C and 85°C cannot support this output voltage and are therefore left out of the table. The efficiency was calculated using Equation 8.1.

Table 8.11: Input power, output current and efficiency of the cold start charge pump for delivering 1.8 V.

	Input power			Output current			Efficiency		
	−10°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C	**−10**°C	**27**°C	**85**°C
FS	53.65 nW	364.99 nW	3.35 µW	2.48 nA	12.39 nA	43.95 nA	8.32%	6.11%	2.36%
FF	271.88 nW	1.50 µW	11.06 µW	25.79 nA	89.74 nA	171.00 nA	17.07%	10.80%	2.78%
TT	63.38 nW	420.75 nW	3.83 µW	5.30 nA	24.27 nA	74.63 nA	15.05%	10.38%	3.51%
SS	10.97 nW	97.60 nW	1.13 µW	0.66 nA	3.91 nA	16.62 nA	10.79%	7.20%	2.64%
SF	95.23 nW	-	-	0.81 nA	-	-	1.52%	-	-

The efficiency drops with increasing temperature as can be seen from the table. For these higher temperatures, higher output currents are also seen. The input power that is consumed by the charge pump for this load is in the high nano-watt to low micro-watt range, fitting to the expected power delivered by a photovoltaic transducer.

Almost all input power flows through the cold start buffers, as expected.

8.5.2. DCTS performance

The effectiveness of the DCTS implementation can be measured by the current flow. The current through both the diode connected transistor and the DCTS is measured to compare the conduction of the devices. The currents are measured for the typical case once a stable output voltage is reached.

The DCTS between the third and fourth split capacitor conducts an average of 23.58 nA. The diode in parallel with this DCTS conducts 1.85 nA. The last DCTS between the last capacitor and the output conducts an average current of 25.74 nA. The diode in parallel with the last DCTS conducts 0.57 nA. The inverters that drive the gates of the DCTS leak an average current of 0.08 nA independent of their position in the chain.

8.5.3. Minimal input voltage

No results are obtained for the SF process corner at 27°C and 85°C, as these corners could not reach the desired output voltage for the given conditions. Since no results are obtained, it is not possible to determine how close to success these corners are. A second simulation is done to provide more insight in the system performance for these test points. The input voltage is incremented in this simulation to determine the minimal input voltage needed to successfully cold start.

The found input voltage and resulting input power, output current and efficiency are given in Table 8.12.

Table 8.12: Minimal input voltage, input power, output current and efficiency of the SF process corner at 27°C and 85°C.

Temperature	Input voltage	Input power	Output current	Efficiency
27°C	110 mV	796 nW	12.13 nA	2.74%
85°C	120 mV	8.20 µW	42.97 nA	0.94%

8.5.4. Leakage

The normal operation switches and capacitor splitters should not conduct current during cold start. The currents that flow through these two components reduce the efficiency of the cold start system. A measurement of the leakage current at the earlier stages and later stages of the charge pump is done, as the voltage levels differ. The leakage current is measured as the average current flowing through one component once a steady output voltage is reached. Current leakage in the pico-ampere range was measured.

8.6. Full system operation

The cold start and normal operation have been tested separately. The complete system is now simulated from cold start into normal operation. The top level implementation as given in Figure 7.1. The main oscillator and VLD are implemented using ideal blocks, as was done for the benchmark simulation. A storage capacitor of 50 pF is used to reduce simulation time, as was done for cold start simulation. The VLD is set to trigger at 1.821 V as this shows the headroom created by the cold start oscillator above the minimal 1.8 V. The load is a 50 MΩ resistor that is connected as the VLD triggers. There is no need for a start-up time for this simulation, since the controller and main oscillator are implemented with ideal blocks for this simulation. The source is

an ideal voltage source that generates 100 mV at the start of the simulation. The voltage source changes to 450 mV as the VLD triggers to accommodate the expected normal operation input voltage. The input voltages differ for normal operation and cold start as the test case was made for a proof of concept, as explained in Chapter 6. The resulting system behaviour is given in Figure 8.10.

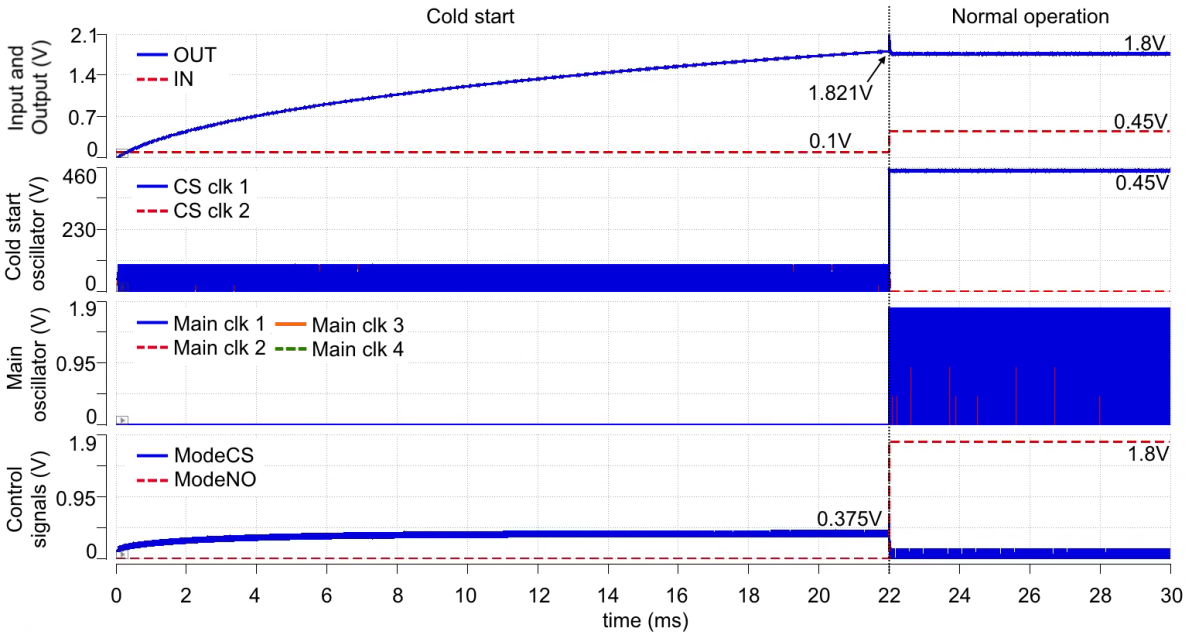

Figure 8.10: System operation from cold start into normal operation.

Cold start is finished after 22 ms, once the output voltage reaches 1.821 V. Four strips are given in Figure 8.10:

1. The input and output voltage of the system;
2. The cold start oscillator output, where the two phases are given;
3. The main oscillator output, where all four phases are given;
4. The control signals, where *ModeCS* is the auxiliary charge pump output and *ModeNO* is the normal mode signal.

The output voltage of the system is defined as the voltage on the storage capacitor. The output voltage is applied to the load resistor during normal operation. The second phase of the cold start oscillator is pulled to the input voltage in normal operation, due to the inverse relation between the first and second phase. The main oscillator produces four phases in total. Only two phases are visible in the figure, as the scale of the figure does not allow for more detail.

9 Discussion

The results of the previous chapter give insight in the proposed design operation. This chapter discusses each of the results and determines the success or failures of all sub-systems. A first bar to pass are the set criteria in Chapter 6. Apart from the minimal required outcomes, the detailed performance of each system is examined.

All simulations are run with a set minimal conductance of 1 pS in order for the simulator to converge. Thus, each node in the circuit is loaded with an additional conductance of 1 pS. Therefore, current cannot be measured accurately below 1 pA, as the added conductance imposes currents in this range. The whole system is thus loaded by the added conductances. Once the system is realised in silicon, these conductances are not present and the system will thus experience lower leakage.

An important point of interest is the total area taken up by the design, which is discussed at the end of the chapter. The results are discussed in the same order as they are presented in the previous chapter.

9.1. Normal operation

First, the normal operation of the charge pump is discussed. The benchmark was set by a normal two stage Makowski charge pump. The proposed design is expected to have higher losses during normal operation, due to the added components. The losses should be kept at a minimum if the capacitor splitters and clock switches are implemented correctly.

9.1.1. Benchmark

The benchmark simulation results shows a stable efficiency across all test points of around 86%, as can be seen in Table 8.1. The FF process corner achieves the lowest efficiency and the SS process corner achieves the highest. The typical and cross corners (SF and FS) barely differ. The achieved efficiencies are within the set criterion of 85.8% for all but the FF process corner. The efficiency in this corner is still high and is thus accepted as a benchmark.

The SS process corner at 27°C exhibits an efficiency on par with the ideal efficiency. Reaching the ideal efficiency should not be possible in a realistic circuit and thus either the simulation is off or the ideal efficiency is incorrect. A difference in the simulation environment is the more plausible explanation. Upon closer inspection, it was found that the charge pump does not perform a full four times boost, but slightly below this due to losses in the SS process corner. The output voltage of the charge pump is thus not exactly at 1.8 V, but slightly closer to the 1.6 V set by the emulated battery. The smaller difference leads to lower switching losses in accordance with Equation 3.2.

The difference between the calculated maximum obtainable efficiency and found efficiencies are a good justification for the benchmark to be used. Theoretical models can be used to estimate the expected efficiency, but only a measurement gives the real case. Utilising the benchmark measurement thus gives a better indication of the losses induced by the proposed design.

Capacitor transient The transient response of the voltage on the capacitor top plates is given in Figure 8.2. The voltage that is boosted by the first stage reaches 850 mV, exactly 50 mV below the expected doubled input, such a precise drop cannot be coincidence. The second stage should ideally reach 1.7 V after pumping the 850 mV. But this is not seen either. 1.6 V is seen instead, as the output of the first stage drops another 50 mV

and the top plate of the second stage does the same. The situation for the full clock cycle is illustrated in Figure 8.2. The losses in voltage seen here are a clear indication of the switching losses.

The transfer phase of Figure 8.2 is of interest for the normal operation switches performance. A closer look at the transfer phase is given in Figure 8.3. The same switch implementation is used for the benchmark as for the proposed design, only with a difference in transistor size. In the ideal scenario, the voltage on both capacitor plates match at the end of the transfer phase, preferably even before the end to have more headroom. The equilibrium is almost reached at the end of the transfer phase and only a minor voltage difference of 0.02 mV is seen.

The voltage difference at the end of the transfer phase does not reach significant values across different test points, as can be seen in Table 8.2. The SS process corner at 85°C is the largest, but still below 1 mV. It can be concluded that the normal operation switches perform well, both from the final efficiency found as from the minor capacitor voltage difference that is found.

The settling times are also given in Table 8.2. The settling time differs with different test points. The slower process corners give the longest settling times. However, lower temperature lowers the settling time. The lower temperature corners resulted in a lower overshoot voltage and thus a starting voltage closer to the final required voltage is found. As the starting voltage is closer to the target voltage, less time is needed to reach the desired value. This effect is also seen for the voltage differences, where the lower temperatures achieve voltages closer to zero.

9.1.2. Proposed design

From Table 8.3, the efficiency drop imposed by the proposed design can be evaluated. The drop is minor in all corners and certainly below the set criterion of 10%. These low losses indicate that the clock switch offers a sufficient off-resistance. On top of that, the capacitor splitters allow for enough current flow, so that the full capacitance of one Makowski stage is utilised.

More losses in faster and higher temperature corners are also observed. In these test points all devices exhibit a lower off-resistance and thus an increased leakage current. Especially the clock switches pose an increased leakage due to this effect. The implementation of the switch minimises the threshold voltage and thereby lowers the off-resistance. Increasing the threshold voltage in normal operation is possible by actively controlling the bulk potential. However, during cold start the active control of a bulk potential is more challenging, especially for the clock switch that already needs an auxiliary charge pump.

The difficulty of bulk control in cold start combined with the minor overall loss seen in the normal operation lead to the conclusion that the clock switches are implemented correctly and do not need adaptation.

Capacitor splitters The capacitor splitter is the other sub-system of importance. Ideally, no voltage drop should be seen between the plates of one split capacitor, indicating that the split capacitor can be treated as one large capacitor. As can be seen in Figure 8.4, a voltage drop does appear. However, at the end of the phase the split capacitor reaches an almost equal potential. The voltage difference within the split capacitors do not exceed 2.5 mV as can be seen from Table 8.4.

The stage voltage difference correlates well with the results seen for the split voltage difference. The SS process corner at 85°C performs the worst, which was also concluded for the benchmark operation. Similarly, the settling time follows the pattern seen for the benchmark case. The reasoning for the difference across test points is thus related as well. The lower temperature corners exhibit a smaller voltage difference to begin with due to the lowered conduction of devices and thus the lower overshoot. Although slower devices allow for a smaller voltage difference to overcome, the process corners indicate that faster devices still reduce the settling time as these allow for greater current to pass.

From the found potential differences, it is concluded that the capacitor splitters benefit from higher conductance and thus lower on-resistance. Lowering the on-resistance by adjusting the device parameters inherently leads to a decrease in off-resistance. With a lower off-resistance, the leakage of a device is higher and thus the performance of the capacitor splitters in cold start is worse. Increasing the driving voltage to lower the on-resistance does not affect the off-resistance during cold start and is thus a preferred method.

The stage voltage differences and split voltages differences are minor in comparison to the voltage being boosted. Therefore, the capacitor splitters and normal operation switches provide sufficient conduction during normal operation.

The DCTS within one split capacitor are still active and could aid the charge distribution across the capacitor. It was found that the current flow through the DCTS during normal operation is too little to be measured.

Thus, the capacitor splitters provide such a high conductance that the DCTS can be considered shorted. The DCTS are no addition to the normal operation, but also pose no major disadvantage.

Conclusion The proposed design inhibits minor losses on the normal operation charge pump. The envisioned implementation is therefore successful for high efficiency boosting.

The size of the capacitor splitters can be used to improve the normal operation efficiency, but at the cost of the efficiency in cold start. Using an increased driving voltage in normal operation is the preferred method to improve the efficiency.

9.2. Cold start oscillator

Although not designed in this work, the performance of the cold start oscillator is of influence on the performance of the cold start charge pump. Therefore, the operation of the cold start oscillator is discussed here.

From Table 8.5 it can be seen that high temperatures and faster operating devices lead to higher frequencies. The opposite effect is seen for the amplitude, where the cross corners (SF and FS) correlate with the lowest amplitudes.

The reason for the difference in frequency will be discussed first in this section. After that, the amplitude differences are examined and lastly, the effects on the cold start charge support systems and pump performance are discussed.

9.2.1. Frequency

The frequency of a ring oscillator is determined by the delay time of each of its elements. For this oscillator the delay elements are implemented by inverters. With a shorter delay of one element, the next can be activated quicker and so the frequency of the oscillator becomes higher. Faster process corners speak for themselves in this regard, as a faster device has a lower delay. With higher temperature the devices also exhibit a faster response due to larger currents as the threshold voltage is lowered.

It is interesting to note that the FS and SF process corners exhibit a frequency lower than that of the typical case. This indicates that the slow response of one type of device is of greater influence on the total average delay.

9.2.2. Amplitude

The slower and colder test points that achieved the lowest frequencies give the highest amplitude. The output voltage of a inverter in steady state is determined by the ratio between the on-resistance of the activated device and the off-resistance of the deactivated device. The steady state voltage also determines the final amplitude that is reached. Due to the low available driving voltage, the on-resistance of activated devices is brought closer to the off-resistance of the deactivated devices and thus the on/off-resistance ratio is reduced. Therefore, the typical case already displays a loss of amplitude.

When moving away from the typical operating point, the on/off-resistance ratio changes as well. For slower test points and lower temperatures, both on- and off-resistance increase. The opposite occurs for faster operating points and higher temperatures. The change of the on-resistance is not equal to the change of the off-resistance for the same device, due to the driving voltage dependence of the on-resistance. From the measured amplitude it is concluded that the off-resistance is lowered more than the on-resistance. With a stronger affected off-resistance the voltage division caused by the on/off-resistance ratio results in a lower voltage and thus in a lower amplitude.

The FS and SF process corners display the lowest amplitudes, especially at 85°C. For matched process corners the pull-up and pull-down networks are in balance and thus an inverter driven with a high potential exhibits the same on/off-resistance ratio as an inverter driven by a low potential. For the cross corners, this balance is broken. Therefore, the on/off-resistance ratio between the inverters is also out of balance. An inverter that is driven such that the slow device is active and the fast device is deactivated produces the lowest on/off-resistance ratio and thus an output voltage far from the rails. This lowered voltage drives the next inverter. Even though that next inverter has a fast active and slow disabled device, the low driving voltage results in a low output voltage as well, since the on-resistance of the activated device depends on the driving voltage. Due to this, the cross corners exhibit the lowest amplitudes.

The amplitude of the clock signal coming from the oscillator is above the 90 mV threshold set in Section 8.2 in all but the SF process corner at 27°C and 85°C. The latter two corners will thus likely not meet the specifications after the buffer and clock switch.

9.2.3. Effects on cold start sub-systems

A fast clock signal requires more effort to be reproduced by a buffer, as the buffer response must be faster for higher frequencies. Fortunately, the process corners of the oscillator are also applied to the buffers. Thus, the buffers response time changes along with the difference in frequency.

The lower amplitudes of some corners are more challenging. The lower driving amplitude results in an input of the buffer close to the switching point, which is already low due to the low input voltage. Especially the SF process corner at 85°C proved difficult to buffer. The oscillator did not degrade the amplitude further as stacked inverters are used there. The chosen buffer implementation does not utilise the stacked topology and this leads to losses in amplitude.

In a later section on the buffer implementation, the severity of the lower amplitude will be further discussed. It will also be decided if a stacked inverter implementation had been better.

9.2.4. Effects on cold start charge pump

From Equation 6.2 in Chapter 6 it can be seen that the oscillation frequency plays a significant role for the load current that can be supplied for a given output voltage. The higher frequencies allow for more cycles within an equal amount of time, increasing the total charge delivered over that time, thus the average output current. Therefore, corners with higher frequency are generally at an advantage.

However, the lower amplitude also affects the resulting drivable load current as can be seen in Equation 6.2. To give an indication of the combined effect of frequency and amplitude on the resulting total load current, Table 9.1 can be used. Table 9.1 was generated using the found frequencies and amplitudes of Table 8.5 with Equation 6.2.

Table 9.1: Maximum attainable total load currents in all corners from the implemented cold start oscillator. The maximum attainable load current includes all leakage losses.

	−10°C	**27**°C	**85**°C
FS	5.1 nA	30.2 nA	205.9 nA
FF	41.6 nA	179.1 nA	868.0 nA
TT	9.6 nA	50.6 nA	323.4 nA
SS	1.7 nA	11.7 nA	100.1 nA
SF	7.4 nA	32.3 nA	62.4 nA

From Table 9.1 it can be seen that the found higher frequencies boost the possible load current. Only the SF process corner does not follow this pattern for higher frequencies. Here, the lowered clock amplitude inhibits the operation more than the higher frequency can boost it. During the design a clock frequency of 20 kHz was adhered. The found frequency for the typical case (TT process corner at 27°C) of 43.6 kHz allows for a higher expected output as seen in Table 9.1. The data sheet of the cold start oscillator that was used, gave the operation frequency around 20 kHz. However, the data sheet was made based on a test where the input voltage was 70 mV. The change in frequency due to the change in input voltage was not accounted for by accident.

9.3. Cold start sub-systems

Now that the input signals from the cold start oscillator are well known, the cold start sub-systems can be examined,. Table 8.5 can be used as a benchmark for the performance of the combined sub-systems. If all sub systems work optimally, the amplitude is not affected before it reaches the charge pump itself. The performance of the sub-systems is therefore best displayed by the amplitude loss of the clock signal.

First, the auxiliary charge pump performance is reviewed. After that, the buffers are discussed and lastly, the clock switch performance is examined. Special attention is given to the cold start buffers, as these caused the most significant degradation of the clock amplitude.

9.3.1. Auxiliary charge pump buffers

The voltage swing at the output of the auxiliary charge pump buffers have a great influence on the performance of the auxiliary charge pump, as the output of the pump also follows the relation of Equation 6.2. The shown amplitudes in Table 8.6 at the output of the buffers are lower than at the input, but possibly not too low yet. The auxiliary buffer will boost the input voltage four times, where only the transistor threshold has to be

passed. This leaves some headroom for the lower input voltage. The headroom can also be seen in Table 8.6 as the ideally reachable voltages.

From the simulations, it became clear that the auxiliary charge pump reaches the desired voltage. Because of this and time constraints, the buffers were not further optimised. More elaboration on possible optimisations for the buffers will be given in the next subsection on cold start buffers, as these are also buffers that have to operate in the cold start scenario. If better buffers are desired, the reasoning given in the next subsection can be applied to the auxiliary charge pump buffers as well.

A conclusion on the amplitude after these buffers is made once the operation of the auxiliary charge pump is further discussed.

9.3.2. Cold start buffers

From Table 8.7 only small losses in amplitude are seen for most test points. Although the percentage loss is small, the effects of a lower clock amplitude are major as seen from Equation 6.2. The clock amplitude loss is seen at every stage in the charge pump and thus the loss is amplified by 32. After discussing the normal operation switches, a final decision based on the criterion of a 90 mV amplitude can be made.

The SF process corner stands out from the others with higher losses. The difference in losses for this process corner indicates that the pull-down network might be too weak compared to the pull-up network. Increasing the pull-down network distributes the amplitude loss more equally between the SF and FS corner. For a next design the NMOS devices should be made slightly larger in comparison to the PMOS devices. The unbalance can already be seen in Figure 8.6(A), for the regular inverter. The voltage difference from the maximum obtainable amplitude is 710 µV for the pull-down network and 495 µV for the pull-up network, a minor difference from the typical case that is escalated in the SF process corner.

SF85 operating point The most disappointing is the SF process corner at 85°C. Here a large drop of 61% in amplitude is seen. The input amplitude in this corner is 70 mV, which likely explains the high losses in the buffer. The lower input voltage swing can barely switch off the pull-up network and only weakly drives the pull-down network. The voltage after the first inverter are even lower and thus the following stage is driven by an even lower voltage. The last inverter, that drives the charge pump, can barely make a full swing and thus a low amplitude is seen at the output.

The implementation of stacked inverters could improve the buffer performance. These inverters are implemented already in the oscillator, so an amplitude larger than 70 mV is still not to be expected. However, it is not possible to implement the stacked inverter topology only for the SF corner, as the process corner is not known before production. Since the other operating points do exhibit good amplitude and consume less current without the stacked inverter implementation, a stacked inverter implementation is not desired.

Stacked inverter To elaborate more on the disadvantage of implementing stacked inverters in the buffer, Figure 8.6 can be used. First off all, it can be seen that the reached output amplitude is lower with the stacked inverter implementation for the typical case. This holds for all process corners, except the SF corner. Thus, what is gained in the SF process corner is lost in others. The power consumption of the stacked implementation is roughly twice that of the regular implementation. The increased power consumption is undesirable during cold start, as little power is available.

The power consumption is determined by the current consumption of the buffer. As can be seen in Figure 8.6(A) the rise and fall times of the stacked implementation are far longer than that for the regular implementation. The most current is drained by an inverter when the input voltage is not at the maximum or minimum, due to both the pull-up and pull-down devices being (semi)activated. A long rise and fall time means that the input voltage is away from the minimum or maximum for a longer time and thus more current is consumed. Therefore, the stacked implementation draws more current.

Current is also drawn once the inverter reaches a steady output voltage, mainly determined by the off-resistance of the deactivated device. Figure 8.6(A) suggests that the regular inverter has a higher static consumption, since the voltage swing is lower and thus the off-resistance is lower than for the stacked case. However, the stacked inverter buffer has a total of three inverters per stage. The two inverters that drive the central inverter cause two static consumption paths through their deactivated devices. Therefore, the total static consumption of one stacked inverter is greater than that of a regular inverter.

The minor improvement of amplitude for one process corner does not justify the loss of amplitude in other corners and increased power consumption. Therefore, the stacked inverter implementation does not

prove a better solution. For lower input voltages, this conclusion should be revisited. At lower input voltages, the difference in achievable amplitude is much higher and also holds for more operating points.

9.3.3. Auxiliary charge pump

The set criterion of 330 mV is met in most of the corners, as seen from Table 8.8. A drop is seen in output voltage for the SS and FS corner at −10°C. The difference from the ideal output voltage indicate that this is caused by losses within the charge pump. PMOS devices have a higher on-resistance in these corners. The charge pump is implemented using diode connected PMOS devices and thus the higher on-resistance is likely the cause of a lower output voltage as less current can be delivered through the higher on-resistance.

An opposite effect is seen for higher temperatures. Here, the difference from the ideal output voltage is slightly above the 27°C case. For higher temperature the on-resistance of the diode connected PMOS devices is lower and thus higher conduction is achieved. However, the off-resistance is also reduced and thus more flow-back current through the diodes is seen.

The SF process corner at 85°C has a small drop from the ideally reachable voltage. Thus, the charge pump works well in this corner. Only the buffers cannot produce a large enough clock amplitude to support the charge pump.

The charge pump drives a load of 5.13 pA. The small load current was expected during design and led to a small charge pump implementation. The current consumption of the auxiliary charge pump buffer of 8.67 nA is higher than expected. A more power conservative buffer design is desired for the auxiliary buffers.

Conclusion From the results it can be concluded that the auxiliary charge pump is successful in most corners. Only at the SF corner at 85°C, the pump certainly fails. The results from the clock switch will determine success or failure of the other test points that are below the 330 mV criterion. The auxiliary charge pump is successful for these test points if the losses due to the switch at these points are acceptable.

Once the auxiliary charge pump has been deemed successful, the auxiliary charge pump buffers are also considered sufficient.

9.3.4. Clock switches

The final sub-system that the clock signal has to pass is the clock switch. Table 8.9 depicts a miniature loss that is acceptable and can be neglected compared to the losses caused by the buffer. The clock switch implementation is therefore successful.

Only the SF process corner at 85°C has a large drop, although still not significant compared to the losses of the buffer. Here, a drop of 4 mV is seen. The most plausible explanation is the low driving voltage of only 152 mV delivered by the auxiliary charge pump.

The low losses due to the clock switch also indicate that the supplied driving voltage by the auxiliary charge pump is sufficient and thus the auxiliary pump buffers perform well.

NMOS and PMOS The switch is implemented using one NMOS transistor in parallel with a PMOS transistor. Figure 8.7 gives the current flowing through both devices in the clock switch. The majority of conduction is clearly through the NMOS device. These findings fit the expected behaviour during the design and implementation phase. The PMOS device source to gate voltage is 100 mV at best, which is below the threshold voltage of the device and thus leads to a high on-resistance. The gate voltage of the NMOS device is provided by the auxiliary charge pump and the resulting gate to source voltage is above the threshold voltage of the device. Therefore, the on-resistance of the NMOS devices is a lot smaller than that of the PMOS device.

The addition of the PMOS device was not needed for the current implementation. The PMOS implementation will prove more useful for higher input voltage implementations, as the source to gate voltage is then raised.

Figure 8.7 also shows three current spikes occurring each clock cycle. When viewing Figure 8.9, an overlap between the clock phases can be seen. Current spikes A and B correlate with these overlapping moments. Both spikes are thus the first rush-in current that occurs when both clock phases have switched and the top plates of the capacitors are set to a new voltage. Spike C correlates with the switching moment of the DCTS. When the DCTS is activated or deactivated, a current rushes through the inverter controlling the DCTS. This current rush is seen in spike C. Only one spike is seen each clock cycle as the capacitor connected to a clock switch only delivers the current during the high phase of the clock signal.

9.3.5. Conclusion on sub-systems

The final clock amplitude that reaches the bottom plates of the flying capacitors is given in Table 8.10. The majority of test points reach the criterion of 90 mV, only the SF process corner and two corners at 85°C do not make it. Of the latter two, the FS corner still reaches close to the set criterion and might be sufficient due to the headroom that was taken.

A more clear conclusion can be drawn by making a new version of Table 9.1. The final clock amplitude after the clock switches is used and Table 9.2 is formed, giving the expected maximum achievable load current of the cold start system.

Table 9.2: Maximum achievable output current of the cold start charge pump for each operating point. The values are determined using the available amplitude at the bottom plates of the capacitors and the oscillation frequency.

	−10°C	**27**°C	**85**°C
FS	4.36 nA	26.83 nA	186.65 nA
FF	39.85 nA	162.43 nA	584.63 nA
TT	8.78 nA	46.48 nA	256.26 nA
SS	1.50 nA	10.24 nA	83.62 nA
SF	5.11 nA	14.64 nA	0.00 nA

The first thing to note is the loss of operation in the SF process corner at 85°C. As has been seen throughout this chapter, the SF85 operating point was always under-performing, starting already with the oscillator output. Therefore, the loss does not come as a surprise and is the combined result of the support systems failing in this operating point.

The other test points display a wide range of possible load currents. A strong dependency on temperature is seen, where higher temperatures lead to the best results. This is mostly linked with the high frequencies at these temperatures. The design was made based on the typical expected case and for this case the output current can still meet the set criterion of 10 nA. Of course, there are still leakage losses to account for. These leakages are expected to be higher for higher temperatures, since a lower off-resistance and more dynamic losses occur at these temperatures. The operating points that achieve a calculated load current already below the criterion will almost certainly not make it.

9.4. Cold start operation

The first criterion that was set is to reach the envisioned output voltage of 1.8008 V. From Figure 8.8 it can be seen that the criterion is met. A major part of the final voltage that is reached is determined by the load current that can be supplied. In the set-up, a parallel resistor of 74.2 MΩ is used. Increasing or decreasing this load influences the load current and thus the stable voltage that is reached. With all test points a different suiting load is found that achieves the desired output.

From Figure 8.9 the operation of the DCTS can be gauged. At the end of the boosting phase for one capacitor, the following capacitor should have reached the same potential. The conduction through the DCTS determines if this equilibrium is reached within the clock pulse duration. From the Figure 8.9, it can be seen that the voltages reach the desired equilibria at the end of each cycle. Upon closer inspection, 4.2 mV difference is found between two capacitors at the end of the boosting phase. Thus, a small loss is seen. This loss results in a lower output voltage or a lower output current for the same voltage.

The difference in voltage is caused by a combination of three currents:

- Forward current flow through the DCTS between the capacitors;
- Reverse current flow through all DCTS in the chain;
- Leakage current flow through parasitic junctions.

The forward current flow must be maximal to achieve the lowest potential difference at the end of a boosting phase. This current flow is determined by the on-resistance of the DCTS when activated. The opposing force is the reverse current, that is dictated by the off-resistance of the deactivated DCTS. The leakage current due to parasitic resistance is barely within the control of the designer and is not discussed.

Both the on- and off-resistance of the DCTS are determined by the sizes of the devices and the driving voltage. Increasing the W/L ratio of the devices decreases the on-resistance and thus lead to a higher forward current. However, the off-resistance is also decreased by increasing the W/L ratio. A compromise must be

found between these two resistances that leads to the minimal voltage difference between the capacitor plates at the end of a boosting cycle.

After some iterations of the design, the presented results were obtained. Adjusting the W/L ratio of the devices further did not yield improvements and thus a fitting balance is established.

9.4.1. Load current

The achieved load currents given in Table 8.11 differ greatly throughout the test points. The found load currents are an indication of the maximum current that can be delivered for a load at 1.8 V. Achieving higher output voltages is possible by lowering the load current. Vice versa, higher load currents can be achieved for a lower output voltage. The test points that achieve the highest output current at 1.8 V, can achieve the highest output voltages for a lower load current.

Comparing the results with the total available load current calculated in Table 9.2 leads to the conclusion that there are many losses at 27°C and 85°C. These losses are also represented in the found efficiency. The higher temperature corners do allow for a higher total current, but also have an increase in leakage current. Especially the reverse current flow through the DCTS is increased. The higher leakage current is caused by a lower off-resistance, which in turn is caused by higher temperatures.

The lower temperature corners achieve the lowest absolute currents. The leakage is less in these corners due to the increased off-resistance of the devices. However, the on-resistance of the devices is decreased as well. The forward current flow through the DCTS is lowered and thus less current can be delivered to the output. At 27°C, a balance is found where the reverse leakage current is less than for the higher temperature case and the forward current is greater than for the lower temperature case. Thus, the standard operation temperature achieves the best balance between the on- and off-resistance for these devices. This balance indicates that the chosen device sizes are sufficient.

The typical case reaches the load current criterion of 10 nA. The FS and FF process corners also reach the desired output at 27°C. For −10°C, only the FF process corner can meet the demands. For the other corners, a storage element with a leakage below 10 nA is thus needed. A large external capacitor will likely not meet the low leakage demands. One possible approach to providing a storage element with smaller leakage is the use of a smaller external capacitor for cold start. The smaller capacitor can be connected to a larger capacitor bank, once normal operation is achieved. It must also be noted that the charge pump is now designed for a low input voltage and this results in a lower load current as well. If the energy source can provide a higher voltage, the output current is increased and thus a larger storage capacitor can be used.

9.4.2. Minimal input voltage

The SF process corner at 27°C and 85°C cannot reach an output voltage of 1.8 V, since the losses are too great. With an increased input voltage, these test points can provide the desired output load. The required input voltages and resulting performance of these test points is given in Table 8.12. At 27°C, a small increase of only 10 mV was sufficient and at 85°C a still minor increase of 20 mV is needed. Thus, a minor input voltage increase of only 20 mV is sufficient to have the system operational in all corners. The small increase also indicates that the system is close to being operational at 100 mV, otherwise the test points would still fail at 120 mV. The system will operate in the majority of real life cases. The test points presented here represent the worst case scenarios and a small deviation from these points will lead to success.

Comparing Table 8.12 with Table 8.11 shows that similar input power, output current and efficiencies are achieved with the increased voltages for these test points.

9.4.3. Power and efficiency

The achieved load current alone cannot determine if the system can be implemented reliably. Another important aspect is the required power at the input and the efficiency of the system.

Table 8.11 shows that the required input power is in the high nano-watt to low micro-watt range. In Chapter 2 it was concluded that PV harvesting systems can provide micro-watts of power. With the lower desired voltage, solar cells can be connected in parallel to achieve a higher output current if needed. Since the system is designed to cold start from 100 mV, more current can be drawn from the solar cell. For the typical case, a solar cell of 400 mm^2 in bright indoor lighting suffices.

The low achieved efficiencies given in Table 8.11 are expected for cold start operation. As was concluded from the available load current, the largest losses are found for higher temperatures. The test points that achieve efficiencies close to 1% cause concern for reliable operation. The input power supplied for these

corners should be made higher than was found in Table 8.11 to have more headroom. However, these results look at a worst case scenario and the expected temperature of the chip will not be at 85°C for long periods.

9.4.4. DCTS performance

The difference in current flow through the DCTS and the parallel diode connected transistor indicate the added value of the DCTS. 93% of the current between two cold start stages flows through the DCTS early in the chain. At the last DCTS, 98% of the current flows though the DCTS. The addition of the DCTS clearly increases the forward conduction throughout the cold start charge pump. The inverters driving the DCTS create a minor current leakage backwards through the pump. The minor backwards current flow is 0.08 nA, which is a fraction of the forward current provided by the diode connected transistor, let alone the forward current provided by the DCTS.

The major forward conductance provided by the DCTS improves the charge pump operation significantly. The minor losses induced by the inverters needed to drive the DCTS can be neglected with respect to the forward current provided.

9.4.5. Leakage

The normal operation switches and capacitor splitters should not conduct current during cold start. The small current that is conducted by these components are a loss during cold start and is thus considered leakage. The current measured is within the pico-ampere range. It cannot be said with certainty that this current flow is caused by the mentioned components or by the added conductance of 1 pS for simulation convergence. Therefore, the current leakage through the components is certainly small enough to be neglected. The leakage current is certainly eight times smaller than the leakage through the DCTS inverters, which in itself is a fraction of the current being conveyed through the charge pump.

It can be concluded that the normal operation switches and capacitor splitters provide a high enough impedance during cold start.

9.5. Full system operation

The combined operation of the cold start system and normal operation system is given in Figure 8.10. The cold start system successfully builds up the voltage on the storage capacitor (*OUT*) to 1.821 V. Once the trigger voltage is reached, the VLD pulls the normal operation signal (*ModeNO*) to the output voltage and sets the input voltage (*IN*) to 450 mV. The main oscillator is activated as well.

The normal operation signal does a number of things. First, the cold start control signal (*ModeCS*) is pulled down and the auxiliary charge pump is deactivated. With the cold start control signal down, the clock switches are deactivated and the cold start oscillator is isolated from the charge pump. The normal operation signal also deactivates the cold start oscillator, as can be seen from the second strip. The first clock phase (*CS clk 1*) is pulled to the input voltage of 450 mV, due to the inverting relation between the two cold start clock phases. The capacitor splitters are switched as well, so that the split capacitors are joined together. Lastly, the normal operation signal deactivates the DCTS situated in parallel with the normal operation switches.

A steady output voltage of 1.8 V is seen at the output during normal operation and thus the system has successfully reached a high efficiency harvesting operation from an energy depleted state.

A small spike in the output voltage is seen when the normal mode starts. The spike is caused by the sudden increase in input voltage and the start of the main oscillator. The voltage spike is quite high, due to the storage capacitor being relatively small. A larger storage capacitor will be used in the final implementation and reduce this peak significantly.

9.6. Footprint

The complete lay-out is given in Appendix B. The system minus the auxiliary charge pump is 1026.26 µm by 635.1 µm in size. The auxiliary charge pump adds an area of 43.6 µm by 43.6 µm. As can be seen by comparing Figure B.1 and Figure B.2, the size of the system is determined almost solely by the capacitors. This highlights the significance of capacitor sharing to reduce silicon area. The auxiliary charge pump stands out as an unwanted sub-system. It cannot be placed underneath the capacitors of the main charge pump and thus increases the total area.

Twice the total area would be needed for a high efficiency charge pump next to a cold start capable charge pump, assuming that the same total capacitance is used for each pump. A comparison of other cold start

systems that are fully integrated and their required silicon area is given in Table 9.3. Most systems are produced using a 180 nm technology. The third entry ([61]) uses a 130 nm node. The first entry uses a 180 nm technology for the charge pump and system, but utilises a separate 600 nm process to create the on-chip coil that must be connected to the charge pump and other sub-systems in post-processing.

Table 9.3: Comparison of other cold start systems and their required silicon area. V_{in} is the minimal input voltage required for start-up, V_{out} is the output voltage provided by the cold start circuit and C_{tot} is the total capacitance used by the cold start system. *voltage provided to the inductive booster preceding the charge pump.

Source	Silicon area	V_{in}	V_{out}	Stages	Load	C_{tot}	Method
[55]	12.71 µm^2	25 mV*	1.2 V	4	N.A.	400 pF	On-chip magnetics & negative Vth devices
[11]	1.56 µm^2	55 mV	840 mV	20	N.A.	400 pF	Cross-Coupled CP & gate boosting
[61]	0.60 µm^2	70 mV	600 mV	24	10 pA	46.08 pF	Super schmitt triggers & Pelliconi CP
[60]	1.575 µm^2	170 mV	1.1 V	8	N.A.	N.A.	Pelliconi CP
Nowi-energy	1.046 µm^2	70 mV	1 V	44	1-10 nA	1263 pF	DCTS Dickson CP
This work	0.652 µm^2	100 mV	1.8 V	32	24.27 nA	1000 pF	DCTS Dickson CP

The first entry ([55]) requires two different technology nodes to be produced and post processing to combine the chips together, greatly increasing the cost of production. The coil is used for a meissner oscillator that provides a first boosting stage, after which the charge pump is utilised to further boost the voltage. The exact voltage at the output of the messner oscillator is not given. From the fact that four charge pump stages are used and an output voltage of 1.2 V is reached, the output voltage of the meissner oscillator must be at least above 300 mV. This system also utilises negative threshold transistors, which requires special processing as well. The fourth entry ([60]) and the proposed system are the only systems where both the cold start and the main harvesting system are fully integrated, all others utilise an external component for normal operation or do not have high efficiency harvesting system included.

From Table 9.3, it can be seen that the proposed design does not achieve the lowest minimal input voltage. This was not a goal for the current design, but might be desired for later implementation. Either the device size has to increase or the load current needs to be lowered in this case. The achieved output voltage of the design is higher than other systems and indicates that the conversion ratio is comparable with the other works presented.

9.6.1. Total capacitance and supported load

The total capacitance is a direct measure of the load current that can be supplied, as has been shown in Subsection 6.1.3. This relation between capacitance and load current is also seen in Table 9.3.

The first entry does not give a specification of the load that can be supported. It is assumed that an open circuit measurement is performed, judging by the mentioned test set-up. The open circuit measurement poses a minimal load and thus a small capacitance is sufficient. The third entry ([61]) utilises a very low total capacitance and can only support a load of 10 pA. The second entry does not specify the exact current supplied by the cold start system, but drives a similar load as the third entry. Like the third entry, the second entry only kick-starts the normal operation by activating one switch. Therefore, the expected load current of the second entry is low as well. The proposed design utilises far more capacitance, but also achieves an output current of 24.27 nA. The measurements of the Nowi-energy cold start system are not fully complete yet, but a load in the range of nano-amperes can be driven. As can be seen, the latter two entries achieve a far higher load current as a higher total capacitance is utilised.

9.6.2. Total system area

Even though a larger capacitance is used and a larger load current can be delivered, the proposed system requires less or equal silicon area compared to the second and third systems. These other systems require more supporting subsystems to achieve cold start or drive the main harvester and thus have a larger total area. The proposed system uses the flying capacitors and storage capacitor of the main harvester and therefore requires minimal additional silicon area. If the other systems are adjusted to provide higher load currents, a larger total capacitance would be needed and the silicon area usage would be even greater.

The Nowi-energy system and the first entry system ([55]) only consist of a cold start system and tells the other side of the story. In this case, a lot more silicon area is required to accommodate a main harvester next to the cold start circuit. The proposed system already includes the main harvester and the cold start circuit in the used silicon area.

The fourth entry ([60]) does not specify the capacitance used for cold start and the cold start load current that is supported. It does specify the total area required and contains a fully integrated cold start system as well as a fully integrated main harvester. The system requires more than double the required silicon area as the proposed system, indicating the silicon area reduction that is achieved with the proposed design.

The proposed design achieves a significant reduction in required silicon area for a charge pump that is both cold start compatible and can achieve high efficiency harvesting. Systems that only provide cold start (Nowi-energy system and [55]) require comparable silicon area, but do not provide a main booster. Systems that have both cold start and the main booster in one system cannot provide high load currents with the cold start system and can only activate a switch. The proposed design can provide high load currents that can start fully integrated energy harvesting systems or systems that utilise external components.

10 Conclusions

In this concluding chapter, an overview of the presented work is first given, starting with the design goals set in the introduction. The success of the work with respect to these goals is concluded on next. Lastly, the contributions of the presented work are given and future work is mentioned.

10.1. Goals

In the introduction, a set of goals was formulated for designing the energy harvester. The energy harvester must be a wrist worn device that utilises ambient energy sources that can provide power in the micro-watt range to charge a battery or other storage element. The system must be capable of cold start and high efficiency energy harvesting out of cold start. The entire system, except the transducer and storage element, must be fully integrated into one IC package and require as little silicon area as possible.

10.2. Overview

First, the optimal energy source for energy harvesting on the human body was determined. A comparison was made on the aspects of power, voltage and sizing for multiple ambient sources and their transducers. In the end, a photovoltaic cell was chosen as it performed best on all three aspects. A solar cell is chosen that will fit on a wrist worn device. The desired power range of micro-watts can be achieved with this photovoltaic cell. The energy delivered by a solar cell depends heavily on the environment, where sunlight provides large amounts of energy and indoor lighting barely provides enough. The voltage provided by the solar cell is below the voltage level of a battery and thus voltage boosting is needed.

With the energy source determined, a theoretical background on voltage boosting for energy harvesting based on literature was given. Special attention was given to the cold start scenario, where no energy is stored in the system. In the cold start scenario, high efficiency harvesting is inhibited. For a fully integrated system the Dickson charge pump was chosen as the best cold start capable charge pump. Utilising dynamic charge transfer switches can greatly increase the performance of the Dickson charge pump. On the aspect of high efficiency harvesting, the Makowski charge pump outperforms other designs. For both charge pumps, the occupied silicon area is mainly determined by the total capacitance used.

With the background complete, a new system is proposed to fulfil the goals set in the introduction. To this effort, a charge pump combining the Dickson topology and Makowski topology was chosen. The proposed design greatly reduces the total silicon area required, as the capacitance is shared between the cold start and normal operation. Of course, the design of a combined charge pump came with new challenges. An implementation of dynamic charge transfer switches for the cold start operation was made with small adjustments. Also, a manner of splitting the capacitor was designed. With the capacitor split, the cold start charge pump can have many more stages than are set by the normal charge pump design. Separating the cold start from the normal operation is done with switches. Special attention to the design of these switches was given, as they are a integral part of the charge pump.

After that, a test case was set and the system was implemented. The test case represents a realistic harvesting scenario for normal operation. The test case contains a more challenging cold start scenario to test the boundaries of the proposed design for cold start operation. An implementation of the proposed design

was made in Cadence Virtuoso. Simulations were done over different process corners at different temperatures to acquire a complete picture of the system performance. A lay-out of the design was also made to determine the needed silicon area for the design. A set of specifications was made to justify the working of the proposed design.

10.3. Results

From the measurements, it can be concluded that the design imposes minor losses for normal operation. These losses are acceptable and the charge pump is thus capable of high efficiency harvesting. The voltage booster can successfully reach battery level voltages of 1.8 V from an input of 450 mV, making the design suitable for solar cell transducers. The power drawn by the converter is in the micro-watt range, which also suits the chosen ambient energy source and transducer. In the end, the proposed design loses around 5% in efficiency compared to a comparable system without cold start capability.

For the cold start operation, slightly lesser results were found. Almost all the test points did achieve a successful start-up and met specifications. However, the SF process corner at 85°C fails certainly, mainly due to losses in the clock buffers. The proposed design is capable of cold start from an input voltage of 100 mV in most situations. For slightly higher voltages of around 120 mV, the design certainly reaches the desired output voltage for all test points. The cold start system can deliver a load current in the nano-ampere range. The buffers should be improved if the desire arises to achieve lower start-up voltages, as the most power losses are seen in the buffers. The set input voltage is below that of the expected output of a solar cell, so the results give a worst case scenario. The system still manages to perform cold start for this low input voltage and is thus proven successful. The required input power is within the range that can be delivered by the solar cell. Low efficiency was achieved as expected. Since the cold start operation is only required once to start the system, the low efficiency is acceptable. The cold start operation is successfully implemented in the proposed design for almost all explored scenarios. The loss of operation in one point is not critical and can be accepted for now. If the need arises, the operation in this process corner will be improved in future work. Utilising stacked inverters will then be of interest.

The achieved silicon area occupied by the proposed design meets that of other works on the aspect of cold start. However, these works do not provide high efficiency harvesting within the same area. A chip that has both a cold start system and high efficiency boosting system requires about twice the size compared to the proposed design. Currently, a small auxiliary charge pump is still needed. This auxiliary charge pump is unwanted in the design and manners of removing this charge pump are desired. The small auxiliary charge pump did not increase the total silicon area significantly compared to other systems. Therefore, it can be concluded that the proposed design achieves close to minimal area usage. The reduction of silicon area usage is one of the major advancements achieved with the proposed design.

It is concluded that the goals set in the introduction are met. The optimal energy source is found and a minimal silicon area, fully integrated energy harvesting system is provided that can achieve both cold start and high efficiency harvesting.

10.4. Contributions

This work provides multiple contributions to the engineering field of energy harvesting. A list of these contributions is given below:

- An overview of literature on ambient energy sources and their suitability for energy harvesting is provided;
- An overview of literature on available voltage boosting techniques suitable for energy harvesting is given, with special attention to cold start scenarios;
- A new design is proposed that combines a cold start compatible and high efficiency charge pump;
  - The proposed design can utilise dynamic charge transfer switches to achieve higher performance in cold start;
  - The proposed design can have a different number of stages for cold start and normal operation using capacitor splitting;
  - The proposed design achieves high efficiency voltage boosting when out of cold start;

- The proposed design can achieve cold start from a voltage of 100 mV;
- The proposed design is suited for small size photovoltaic energy harvesters;
- The proposed design is fully integrated;
- The proposed design can reduce the silicon area twofold.

10.5. Future work

The lay-out of the design is completed at the moment that this work is presented. At the moment of writing, the final post-layout circuit simulations are being performed and the system is being prepared for tape-out. The proposed design will be manufactured in the coming three months. With the design on silicon, the system will be tested in a real life application and a final confirmation of its performance is made. After that, the device will be tailored to a designated application and will be implemented for end-user products. The failing of the SF process corner will be reviewed and it will be decided if adjustments are necessary.

The system also seems suitable for implanted devices and can reduce the chip area for these devices as well. After the wearable device is successful with the proposed system, an implantable device can be outfitted with the proposed system.

The proposed design utilises a small auxiliary buffer to drive one type of switch. To truly achieve minimal silicon area, this auxiliary charge pump should be removed. A manner of switch implementation that can provide a high impedance during normal operation and a low impedance during cold start is sought. Another option would be implementing the auxiliary charge pump under the capacitors of the main charge pump. A possibility lies in using lower metal layer capacitors or substrate capacitors.

New questions and research directions arise from the presented work. First, a major improvement to the cold start system could be made with better design of the buffers. The buffers could not achieve the full voltage swing and are the bottleneck for the cold start operation. A suggestion for achieving a better buffer can be found in stacked buffer design, although issues are also found with this type of buffer as mentioned in Chapter 9.

Another point of interest lies within the oscillator design. For cold start, all power flows through the oscillator and both achievable cold start levels and efficiency depend heavily on the oscillator performance. An oscillator that can achieve higher frequencies and amplitudes in cold start could be a major improvement for cold start applications. With the charge pump optimised, the oscillator is the next logical choice to improve the performance for cold start systems.

A

Capacitor top plate transients

The transient voltage behaviour of the top capacitor plates during the transfer phase is given in Figure A.1 for three test points. First the typical case is given, followed by the fastest test point and lastly, the slowest test point.

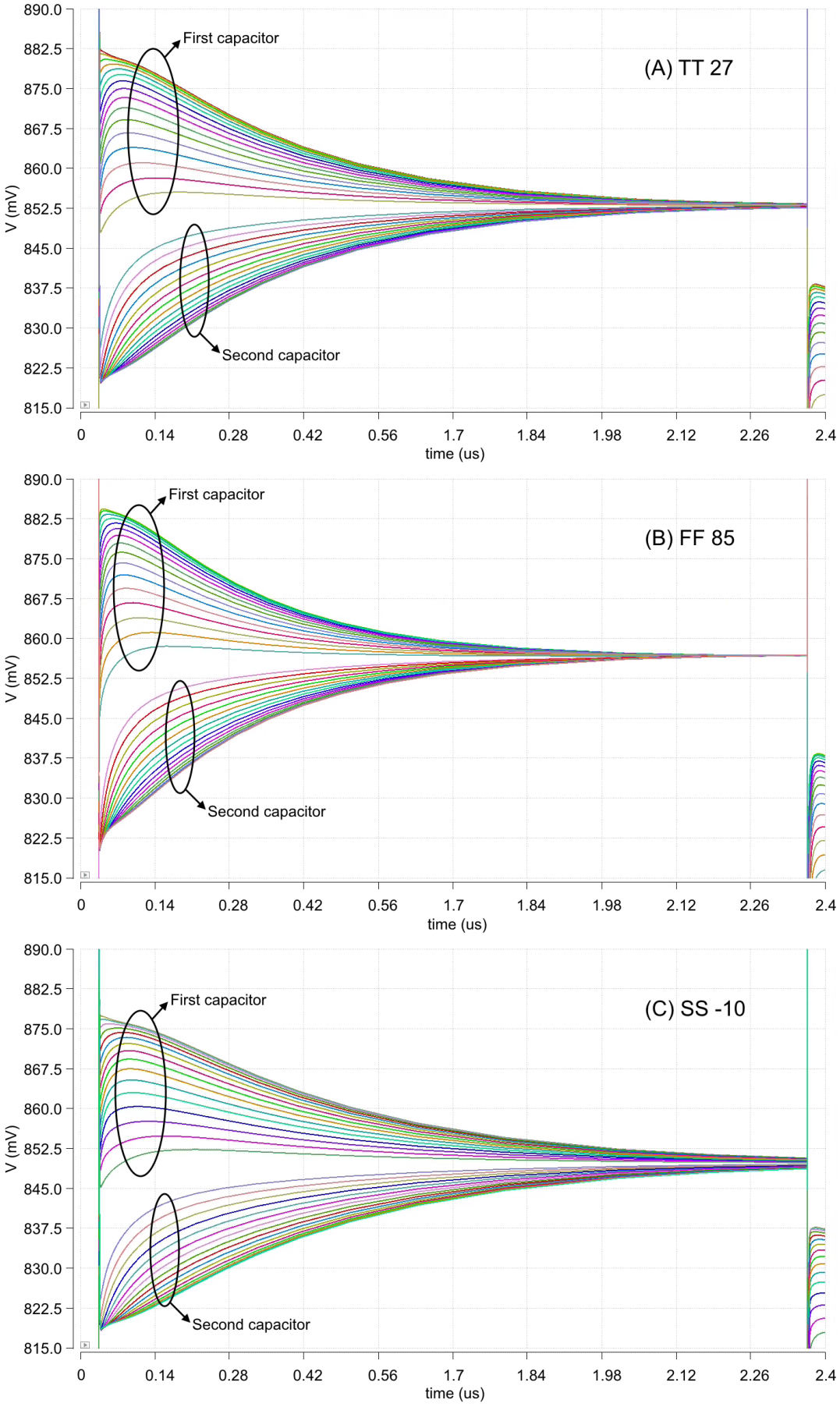

Figure A.1: Top plates of the split capacitors voltage behaviour during the transfer phase. (A) Typical process corner at 27°C. (B) FF process corner at 85°C. (C) SS process corner at −10°C.

B

Lay out

The top-level lay-out is depicted in Figure B.1. The same lay-out is given in Figure B.2, but with the capacitor layers hidden to show the underlying systems. In the second figure, the oscillator can be seen more clearly and it can be seen that most of the system is underneath the capacitors.

The system minus the auxiliary charge pump is 1026.26 µm by 635.1 µm. The auxiliary charge pump adds an area of 43.6 µm by 43.6 µm.

Figure B.1: Top level lay-out of the proposed design. The small square on the left is the auxiliary charge pump. One split capacitor is outlined in red to indicate the size of one stage.

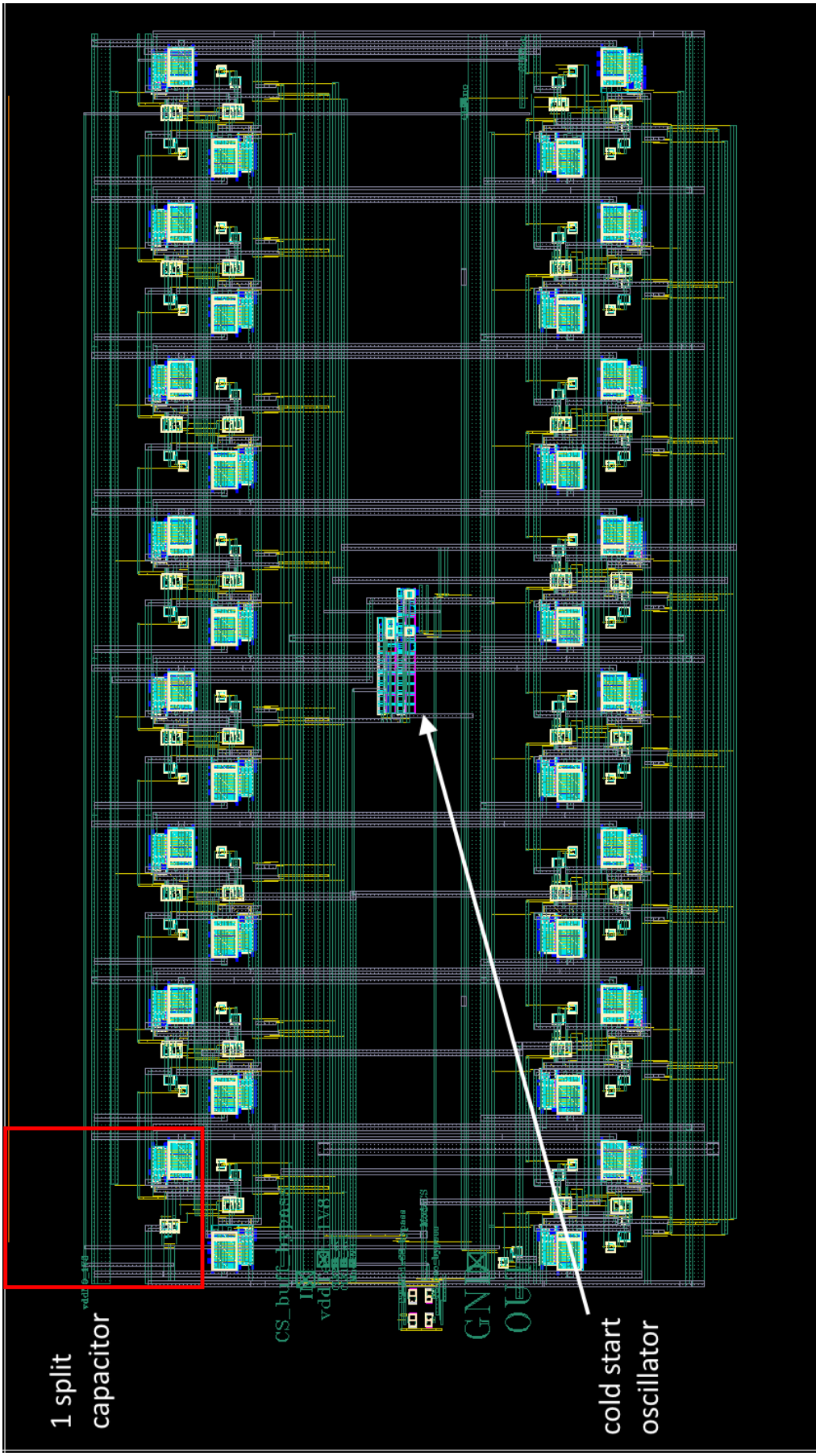

Figure B.2: Top level lay-out of the proposed design without the capacitors to show the underlying system.

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