

# A Zoom ADC for Dynamic Signals

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# A Zoom ADC for Dynamic Signals

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# Abstract

Analog-to-digital converters (ADCs) are one of the most critical blocks of the electronic systems, usually employed at the front-end of the signal chain to convert analog signals into digital domain to be processed by digital signal processing (DSP) algorithms, saved into digital volatile or non-volatile memories, or transmitted through digital communication channels.

ADCs usually are designed to meet the application driven specifications such as dynamic range (DR), signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR), spurious free dynamic range (SFDR), integral and differential nonlinearities (INL and DNL). They should be as much energy efficient as possible when meeting these requirements. Thus, the focus of the ADC design was improved energy efficiency lately. Although low-to-medium resolution ADCs have been improved, high resolution ADCs still lag behind.

This thesis presents an energy efficient high-resolution ADC, i.e. zoom ADC, for audio applications achieving 102dB DR 97dB SNR and 92dB SNDR while consuming only 2.07mW. While showing state-of-the-art energy efficiency the ADC occupies only 0.16mm<sup>2</sup> area, which is smallest reported for similar resolution and bandwidth.

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# 1. Introduction

We are living in the age of electronics. This is mostly because of the power of signal processing, which was never available before in any other domain than electronics. The electronic gadgets we have such as laptop computers, smart phones and music players etc. possess enormous signal processing power. Even the beasts of mechanics like cars, planes or trains are likely to have the most complicated electronics embedded at their very hearts.

The world surround us is analog. Any physical signal should be acquired by analog sensors into electrical domain. It can then be processed by analog electronics. However, analog signal processing is known to have unwanted effects on the signal such as increased noise, and distortion. Furthermore, an analog signal cannot be accurately memorized for a long period of time, or cannot be transferred without added noise or distortion [1]. From the early days of analog electronics, engineers and scientists tried to deal with these problems. Especially in the area of communications, digitization of analog signals was a popular topic due to the need of noise immune communication channels. The first widely used electronic communication tool, the telegraph, was actually digital. However, the successor telephone had serious noise problems. This bring analog to digital conversion into question, without distorting the signal with minimum effort. The reader is referred to [2] for a detailed early history of data conversion.

There was a rise of digital electronics with the introduction of the modern CMOS technology. Due to ever reducing feature size of CMOS, much complex and efficient digital signal processing algorithms have become possible, and it continues to improve. However, we are still struggling to represent the analog signals in digital domain accurately with minimum effort, or in other words minimum energy. Today, analog-to-digital converters (ADCs) still is far from theoretical limits of energy efficiency. Especially very high resolution (16-20 bits) ADCs lag behind the competition compared to low to medium resolution ADCs.

This work is describes an energy efficient high resolution ADC, a zoom ADC, for audio applications. For high-performance digital audio systems, SNR should be higher than 96dB (CD quality), and bandwidth is usually defined between 20Hz-20kHz. In the context of this work, it is most beneficial to first understand the different definitions of energy efficiency, or in other words figure-of-merit (FoM), in the literature.

## 1. 1. ADC Figure-of-Merits (FoM)

It is a challenging task to compare the performance of different ADCs which might be designed and optimized for different applications, implemented in different architectures or technologies and so on. Thus, a figure-of-merit (FoM) should be defined to make this compassion possible. There are two different FoM definitions accepted in the literature, Walden FoM [3] and Schreier FoM [4], both of which try to reflect the trade-off between power, bandwidth and resolution.

### 1.1.1. Walden FoM

Walden [3] assumed that doubling the resolution requires as much power as doubling the bandwidth. This empirical trade-off is expressed as:

$$FoM_w = \frac{P}{f_s \cdot 2^{ENOB}} \quad [\text{J / conv.}] \quad 1)$$

The Walden FoM ( $FoM_w$ ) is seen to fit to quantization noise limited ADCs [5].

### 1.1.2. Schreier FoM

Assuming a theoretical case that the only noise source of an ADC is its sample and hold circuit, the maximum SNR is:

$$SNR = 20 \cdot \log_{10} \left( \frac{V_{FS}}{\sqrt{\frac{kT}{C}}} \right) \quad 2)$$

where  $V_{FS}$  is full scale input voltage, and  $C$  is the sampling capacitance.  $C$  needs to be quadrupled in order to double the resolution (i.e. 6.02dB increase in SNR). The power requirements also increase with the same amount for the same bandwidth, leading to  $FoM_s$  [4]:

$$FoM_s = DR + 10 \cdot \log_{10} \frac{f_{bw}}{P} \quad [\text{dB}] \quad 3)$$

where  $DR$  is the dynamic-range in dB.  $FoM_s$  is more suitable for thermal noise limited ADCs, especially over-sampled ADCs [5]. However it ignores distortion, and the circuits which are usually not thermal noise limited such as biasing circuits and digitals.

## 1. 2. Energy vs resolution

It is hard to estimate the relationship between power and resolution. Some of circuit elements are not thermal noise limited (e.g. digital circuits, biasing blocks), and some ADCs are matching limited. So, it is most useful to compare the energy consumption ( $P/f_s$ ) of ADCs with respect to their resolution (SNDR) rather than by estimating the relationship between power and resolution [5]. Fig. 1.1 shows this relationship for different ADC architectures described in the literature [6]. For reference the 10 and 100 fJ/conv. lines are also shown. It may be seen that SAR ADCs display good energy efficiency at low to medium resolutions (30-70dB SNDR), while for medium to high resolutions (60-80dB SNDR) pipeline and  $\Sigma\Delta$  ADCs compete. However, for very high resolutions (80-110dB SNDR)  $\Sigma\Delta$  stand alone.

## 1. 3. Motivation of this work

Note that in the low and medium resolution regions, ADCs are pushing towards the 10fJ/conv. However, high resolution designs are still quite far away from the 100fJ/conv. border. This performance gap is the main motivation of this work, which is to implement a very high resolution ADCs with state-of-the-art energy efficiency. Before that, the operation of the two best candidates,  $\Sigma\Delta$  ADCs and SAR ADCs will be discussed briefly.



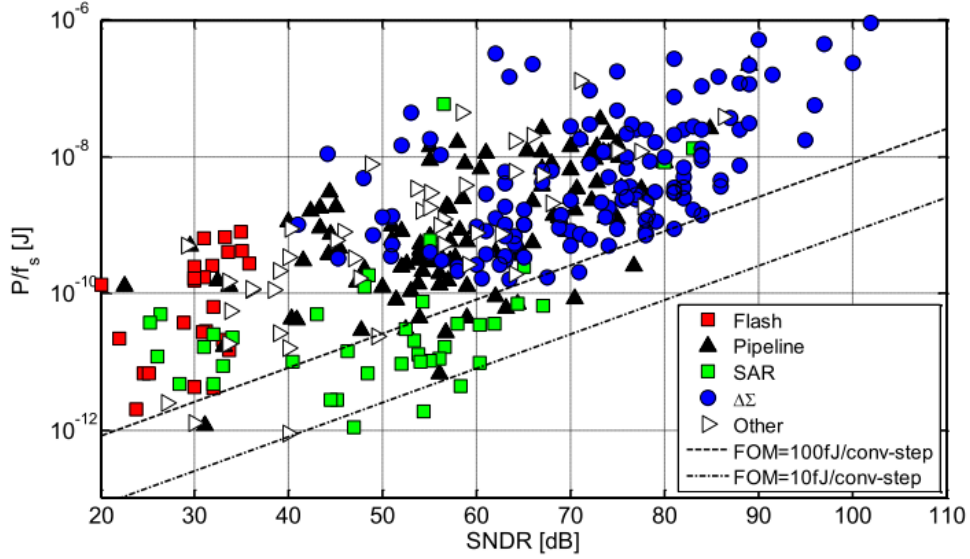


Figure 1.1. Energy vs. SNDR of ADCs reported between 1997-2012 (From [6])

#### 1. 4. Overview of the thesis and the main objectives

This thesis is organized as follows. Chapter 2 discusses oversampled ADCs and SAR ADCs to establish the theoretical background of the zoom ADC, emphasizing on the energy efficiency of the architecture. It also provides a previous zoom ADC design [7] for pseudo-DC signals, and discusses the challenges of implementing a zoom ADC for dynamic signals. Chapter 3 determines the system level considerations, and choices made for the targeted specifications. Chapter 4 discusses the transistor-level design and physical implementation of the prototype chip, supported with simulation results. Chapter 5 presents the design considerations of the measurement setup, and the measurement results of the fabricated prototype chip together with the conclusion.

The main objectives of this work are to:

- Study the feasibility of zoom ADC as an energy-efficient high-resolution ADC for dynamic signals
- Discuss the challenges, critical design aspects and optimization points
- Implement a prototype chip which achieves state-of-the-art energy efficiency to proof the concept on silicon
- Present the silicon measurement results

## 2. System Level Overview of Zoom ADC

### 2. 1. Nyquist-rate and oversampled ADCs

Nyquist-rate is the lowest possible sampling rate which does not introduce aliasing problems, which is defined as the twice the bandwidth of interest ( $f_s = 2 \cdot f_{bw}$ ). The ADCs sample their inputs at this rate is referred as Nyquist-rate ADCs. Oversampled ADCs sample the input signal faster than the Nyquist-rate with an oversampling ratio (OSR). OSR can be defined as the ratio between sampling frequency  $f_s$  and the Nyquist-rate, which is twice the signal bandwidth  $f_{bw}$ :

$$OSR = \frac{f_s}{2 \cdot f_{bw}} \quad 4)$$

The total power of the quantization noise introduced by an ADC is only dependent on the number of quantization levels and not by its sampling rate [1, 8]. However, the frequency range over which quantization noise is spread, i.e. the Nyquist bandwidth of the ADC, increases with sampling frequency.

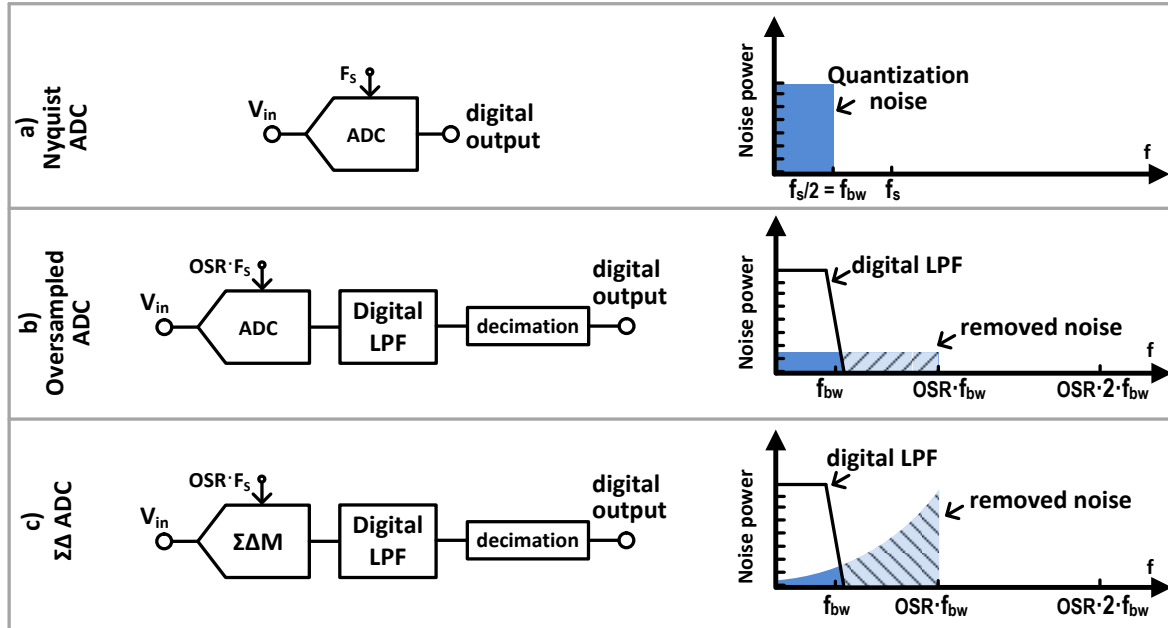


Figure 2.1. Example in-band quantization noise spectrums for (a) Nyquist, (b) oversampled, and (c)  $\Sigma\Delta$  ADCs (From [2])

Output quantization noise spectrums of a Nyquist-rate ADC run at  $f_s = 2 \cdot f_{bw}$ , and the same ADC with an over-sampled clock ( $OSR \cdot 2 \cdot f_{bw}$ ) are shown in Fig. 2.1-a and Fig. 2.1-b respectively. The latter has the same total quantization noise power in its Nyquist bandwidth of  $OSR \cdot f_{bw}$  with the first one, which is spread over a wider bandwidth assuming that the noise spectral density of quantization noise is white. Thus, the integrated noise power in the bandwidth of the Nyquist ADC, i.e.  $f_{bw}$ , is reduced by OSR. This

results in an increased signal-to-quantization noise ratio (SQNR) compared to a Nyquist-rate converter, which is given by:

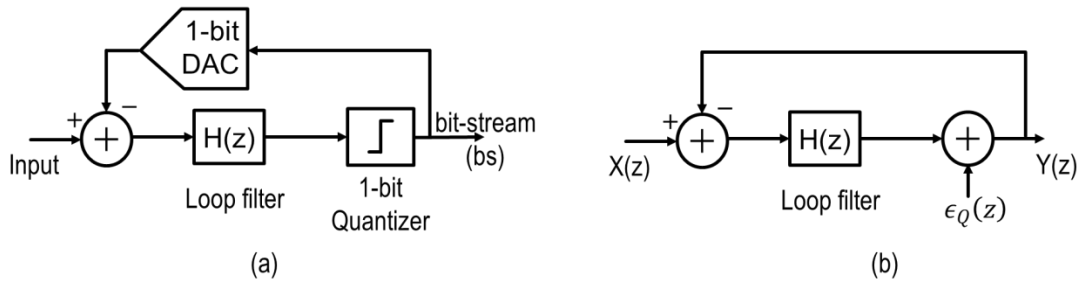
$$SQNR = 1.76 + 6.02 N + 10 \log(OSR) \quad [8] \quad (5)$$

The out-of-band noise can be removed by post-filtering, and the output rate can be reduced to  $f_s = 2 \cdot f_{bw}$ , i.e. Nyquist ADC's output rate, by decimation. However, these requires additional digital hardware.

Although, SQNR can be increased by 0.5 bit/octave with oversampling it is required to increase the sampling rates which yields to more energy consumption per conversion. Since the ADC's bandwidth is higher than the bandwidth of interest, the quantization noise power spectrum can also be shaped to move most noise power out of the signal band as shown in Fig. 2.1-c, which results even lower in-band SQNR levels. This is referred as  $\Sigma\Delta$  modulation. Oversampled ADCs which consist of  $\Sigma\Delta$  modulator, digital post-filtering, and decimation filter are referred as  $\Sigma\Delta$  ADCs.

## 2.2. Noise shaping ( $\Sigma\Delta$ modulation)

Sigma-delta ( $\Sigma\Delta$ ) modulation shapes the quantization noise spectrum of oversampling converters to have a better SQNR over the bandwidth of interest [4]. The simplest  $\Sigma\Delta$  modulator is shown in Fig. 2.2-a. It consists of a loop filter  $H(z)$ , a 1-bit quantizer and a 1-bit digital-to-analog converter (DAC). The filter output is quantized, thus introducing an quantization error  $\epsilon_Q$ . This error is the difference between the quantizer input signal and its quantized representation at the output of the DAC. The quantization error is suppressed by oversampling and shaping of the noise by the loop filter, as explained in the following.



**Figure 2.2. a) Block diagram of a 1-bit 1<sup>st</sup> order  $\Sigma\Delta$  modulator. b) its linear model**

By modelling the non-linear quantizer with a linear gain of 1 and a summation of quantization noise (Fig. 2.2-b), we can calculate two different transfer functions: the signal transfer function (STF), and the noise transfer function (NTF), where [4]:

$$STF(z) = \left. \frac{Y(z)}{X(z)} \right|_{\epsilon_Q(z)=0} \quad (6)$$

$$NTF(z) = \left. \frac{Y(z)}{\epsilon_Q(z)} \right|_{X(z)=0} \quad (7)$$

From the transfer functions above, the output can then be expressed as:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot \epsilon_Q(z) \quad (8)$$

where STF and NTF are:

$$STF(z) = \frac{H(z)}{1 + H(z)} \quad (9)$$

$$NTF(z) = \frac{1}{1 + H(z)} \quad (10)$$

If  $H(z)$  has a large DC gain with a low-pass behavior, the following approximations hold:

$$NTF(z)|_{f \ll f_s} \cong \frac{1}{H(z)}, \quad STF(z)|_{f \ll f_s} = 1 \quad (11)$$

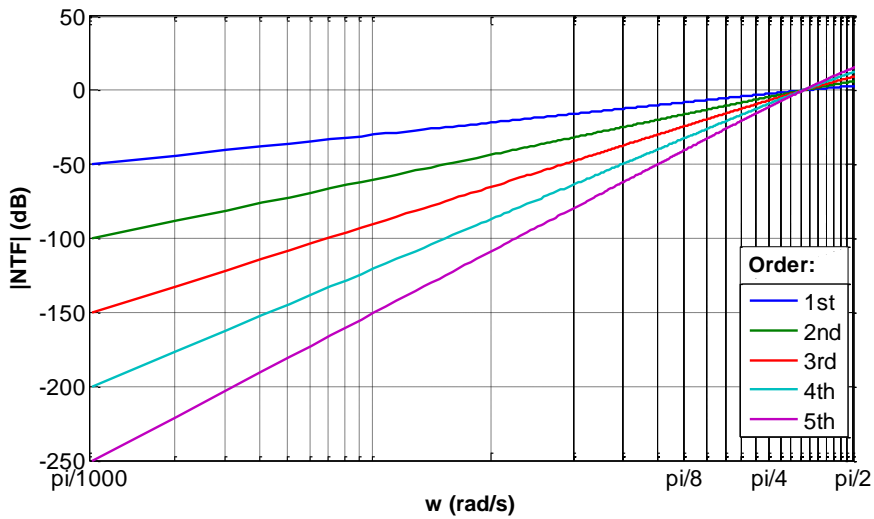
It can be concluded that  $\Sigma\Delta$  modulator has a high-pass  $NTF$  that suppresses the noise in the signal bandwidth and a unity  $STF$  that preserves the signal. Using a discrete integrator for loop filter  $H(z)$ :

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (12)$$

Then, the output becomes:

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot \epsilon_Q(z) \quad (13)$$

From (12) it is clear that the signal is transferred to the output by only a delay, but the quantization noise is high-pass shaped. It should be noted that the quantizer can have more quantization levels and that the order of the loop filter can be greater than 1. A quantizer with higher resolution introduces less quantization noise in the loop, i.e. a lower  $\epsilon_Q(z)$ . A higher-order loop filter suppresses more quantization noise in the signal bandwidth, thus resulting in higher SQNR for a given OSR [4].



**Figure 2.3. NTFs of different order 1-bit  $\Sigma\Delta$  modulators**

As an example, Fig. 2.3 shows noise shaping functions for different filter orders, as given by:

$$NTF(z) = (1 - z^{-1})^n \quad 14)$$

It is clear that higher order loop filters achieve higher SQNR. It should be noted, however, that a higher order system is prone to instability. Hence, some kind of compensation is needed to keep the system stable, which usually reduces the SQNR improvement.

### 2.2.1. Multi-bit quantization

The quantizer and the DAC of  $\Sigma\Delta$  ADC can both be multi-bit implementations (Fig. 2.4), which confers benefits such as increased SQNR without increasing noise-shaping order or over-sampling ratio, increased stability and so on [4].

A multi-bit quantizer is usually implemented as a flash ADC, which requires  $2^N$  comparators for N-bits. This means that the complexity of the quantizer exponentially increases which leads to increased power consumption and area. The linearity of the quantizer together with the linearity of the multi-bit DAC are important factors in determining the linearity of the overall  $\Sigma\Delta$  ADC. There are several techniques such as dynamic element matching (DEM), calibration and trimming to increase the linearity of the DAC. DEM is usually the preferred method due to its compatibility with the operation of over-sampled ADCs [4]. This will be explained later in more detail.

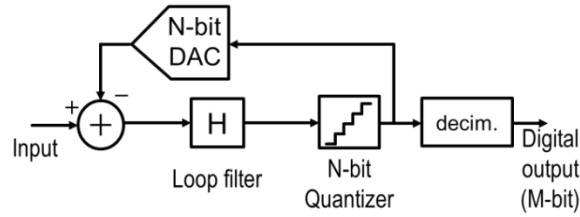


Figure 2.4. Block diagram of a multi-bit  $\Sigma\Delta$  ADC

## 2. 3. SAR ADC

Successive approximation (SAR) ADCs use a binary search algorithm to iteratively find the digital code corresponding to a given input signal. A typical SAR ADC consists of a comparator, a DAC and a successive approximation (binary search) logic, as shown in Fig. 2.5. In the last years, this architecture gain popularity due to its energy efficiency. It can be implemented easily in nanometer-scale CMOS technologies, in which even better energy efficiency can be achieved due to the reduction in minimum capacitor sizes. The most energy efficient ADCs reported on the literature are SAR [9-15].

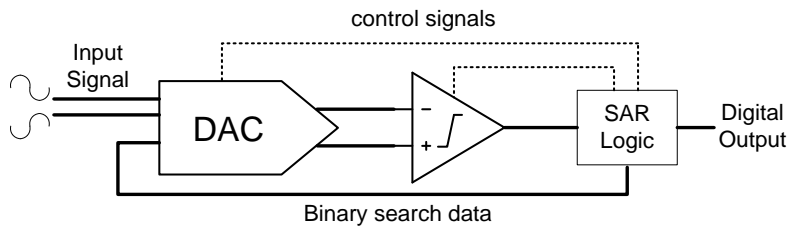


Figure 2.5. SAR ADC

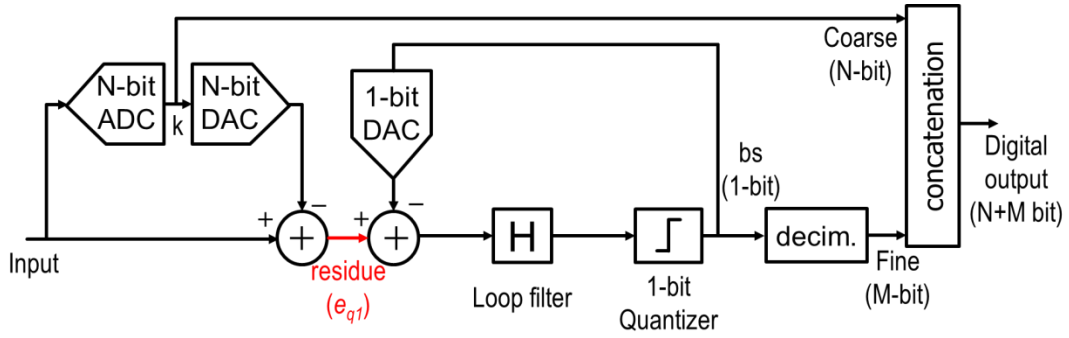
A SAR ADC's linearity and resolution are determined by the linearity and resolution of its DAC. Typically, 12-bit linearity can be achieved without trimming in typical CMOS processes [12]. If higher linearity and resolution are required,  $\Sigma\Delta$  ADCs are preferred.

## 2.4. Zoom ADC

### 2.4.1. System overview

So far, we have discussed two different ADC architectures: a high-resolution one ( $\Sigma\Delta$ ) and an energy efficient, but low-resolution, one (SAR). In order to combine the advantages of both SAR ADCs and  $\Sigma\Delta$  ADCs in a single architecture, the Zoom ADC architecture has been proposed to combine a coarse SAR ADC with a fine  $\Sigma\Delta$  ADC in a two-step fashion [7].

Multi-bit  $\Sigma\Delta$  ADCs are usually used in order to achieve very high resolution. However, the main disadvantage of it is that a multi-bit quantizer is required, which leads to an exponential increase in power consumption, circuit complexity and area. For high energy efficiency and low circuit complexity, it is desirable to retain a one-bit quantizer (which is just a comparator) in the  $\Sigma\Delta$  loop but somehow to benefit from a multi-bit quantization, which does not necessarily need to be in the loop. A two-step ADC in which the coarse ADC has a low resolution but the fine 1-bit  $\Sigma\Delta$  modulator performs a high-resolution conversion on the residual quantization error of the coarse step, appears to be a viable way to go.



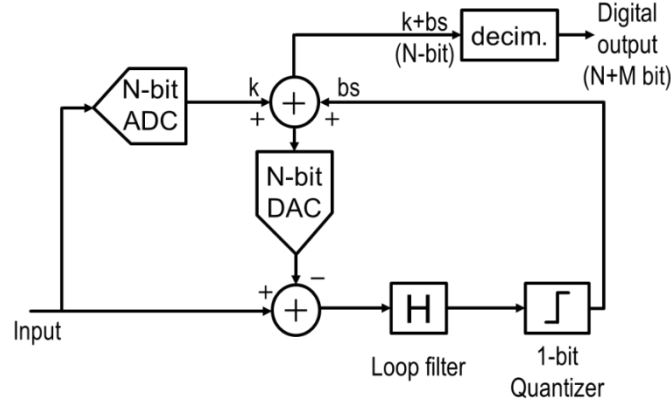
**Figure 2.6. A two-step ADC**

The block diagram of such a two-step ADC is shown in Fig. 2.6. If the N-bit coarse ADC and the N-bit DAC are ideal, there will be no error due to the combination of coarse and fine conversion results. However, it is not possible to realize an ideal coarse ADC, or an ideal N-bit DAC. The residue of the coarse ADC ( $e_{q1}$ ) will have nonlinearity and offset errors due to mismatch and circuit non-idealities. These errors have a bigger effect than the errors added by the  $\Sigma\Delta$  ADC because the coarse conversion will determine the MSBs of the combined digital output. The linearity of the N-bit ADC and the DAC should be better than N+M bits (e.g. 16 to 20-bits), which makes it very hard to implement such a coarse ADC without using some kind of trimming or calibration technique.

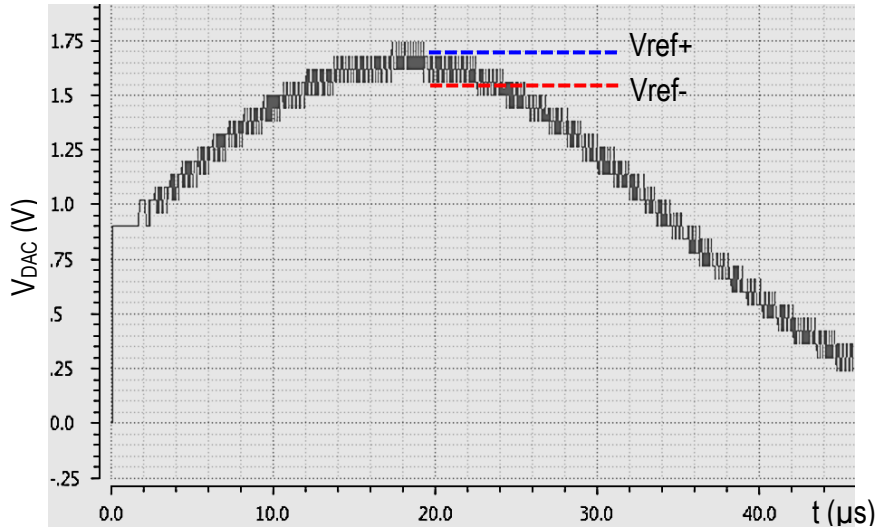
The block diagram of a zoom ADC is shown in Fig. 2.7. In order to address the errors added by the DAC, the two separate DACs may be combined into a single N-bit DAC, and the N-bit digital coarse result  $k$  and 1-bit bit-stream  $bs$  can be summed to create an N-bit (ignoring the carry-out) digital feedback data for the DAC. Thus, an additional subtraction node to calculate the residue  $e_{q1}$  is removed. Now, the multi-bit DAC has the same linearity, offset and noise constraints as the DAC of a multi-bit  $\Sigma\Delta$  ADC. This

means, techniques like dynamic element matching can be applied to the DAC in order to achieve high linearity.

The N-bit ADC is preferably a SAR ADC, due to its energy efficiency. However, its linearity still needs to be at the level of the final N+M bit (e.g. 20-bits) even it is a low-resolution ADC (e.g. 4-6 bits). This linearity requirement should be addressed and relaxed, as will be explained in the Chapter 3.



**Figure 2.7. Zoom ADC block diagram**



**Figure 2.8. DAC output of an example zoom ADC**

Intuitively the zoom ADC can be seen as a 1-bit  $\Sigma\Delta$  ADC, whose DAC is tracking the signal, in other words the DAC zooms-in to a small region around the signal, such that the signal is always in between the positive and the negative references of the DAC. Fig. 2.8 shows the output voltage of the DAC of a zoom ADC versus time for a sinusoidal input. The input signal is tracked roughly by the coarse ADC (5-bits in this example), and a 1-bit  $\Sigma\Delta$  modulation is done on top the coarse quantization steps which after decimation accurately corresponds to the input signal. Since the fine converter zooms-in to a smaller region of the input range, the internal signal swings of the  $\Sigma\Delta$  ADC are reduced. This leads to relaxed requirements on circuit performance and thus lower power dissipation.

### 2.4.2. Energy Efficiency

It can be intuitively understood that zoom ADCs can achieve high energy efficiency. As was mentioned before,  $\Sigma\Delta$  ADCs are generally not as energy efficient as the other architectures. On the other hand, low resolution SAR ADCs require orders of magnitude less energy. If we combine both as described previously, then we can increase the overall resolution without any significant energy penalty. For example, if one wants to achieve 110 dB SNDR, a 5-bit SAR ADC might be used to provide 30 dB SNDR and a  $\Sigma\Delta$  ADC for the remaining 80 dB SNDR. As shown in Fig. 2.9, the SAR ADC would then require 3 orders of magnitude less energy than the  $\Sigma\Delta$ , which is negligible in terms of the overall energy per conversion. Thus, 110 dB SNDR can be achieved with a conversion energy practically equal to that of an 80-dB SNDR  $\Sigma\Delta$  ADC, thus outperforming other high resolution converters.

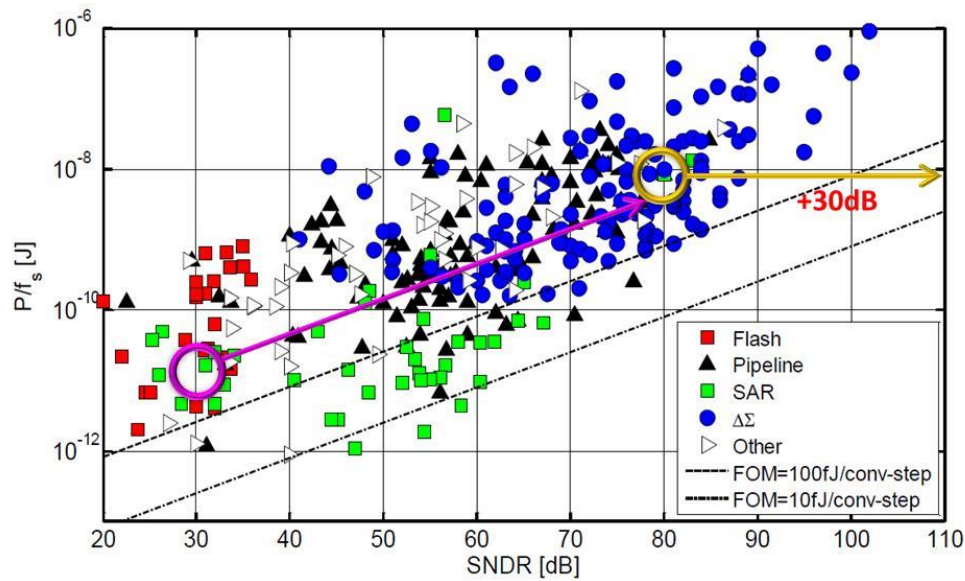


Figure 2.9. Energy vs SNDR plot emphasizing zoom ADC's energy efficiency (Redrawn [6])

### 2.4.3. Comparison to multi-bit $\Sigma\Delta$ ADCs

A zoom ADC has essentially the same hardware (a loop filter, a multi-bit DAC, a quantizer) as a multi-bit  $\Sigma\Delta$  ADC. So, it is fair to compare the two architectures. Both architectures share some common properties: they both benefit from a reduced signal swing at the input of the loop filter; DEM can be applied to the multi-bit DAC to improve its linearity; both of them exhibit a wider stable input range compared to 1-bit  $\Sigma\Delta$  ADCs.

On the system level, the most obvious difference is that a zoom ADC places the multi-bit quantizer outside the  $\Sigma\Delta$  loop while a multi-bit  $\Sigma\Delta$  ADC employs it after the loop-filter. Placing the quantizer outside the loop makes it possible to optimize it for energy efficiency rather than low delay. It also immediately provides the zoom ADC with the resolution of the SAR ADC right at the beginning of the signal chain, which can be beneficial for some applications. For example, a battery-powered wireless sensor node might stay in stand-by mode for a long time until some activity is detected, (by the zoom ADC's energy efficient coarse converter). Once activity is detected, a high-energy high-resolution conversion could then be performed.



The linearity of a zoom ADC is determined only by the accuracy of the multi-bit DAC. This relaxes the constraints on the multi-bit quantizer. This is unlike conventional multi-bit  $\Sigma\Delta$  ADCs' whose quantizers require careful design [16].

Depending on the design of its loop filter, the STF of a  $\Sigma\Delta$  ADCs is often not flat, but may have a "peaking" gain of couple of dB on the higher frequencies. In a zoom ADC, however, the coarsely quantized signal is fed-forward to the DAC with only one delay, which suppresses STF peaking. A similar behavior is exhibited by multi-bit  $\Sigma\Delta$  ADCs that have a signal feed-forward path to the quantizer input [16].

A disadvantage of the zoom ADC is its limited bandwidth. Basically, the  $\Sigma\Delta$  ADC can only operate properly as long as the coarse ADC can track the input signal. Since the tracking performance drops with increased signal frequency, the performance also degrades quite dramatically. However, this can be avoided by placing a simple RC filter in front of the ADC to limit the signal bandwidth seen by the coarse ADC.

#### 2.4.4. Error Sources

Although there is no residue calculation error or residue amplification error, the SAR ADC used in a simple implementation of a zoom ADC would still need to achieve linearity at the level of the final resolution. Since the quantization steps of the SAR ADC may be different than that of the  $\Sigma\Delta$  ADC's DAC, alignment of the quantization steps to a good precision is necessary.

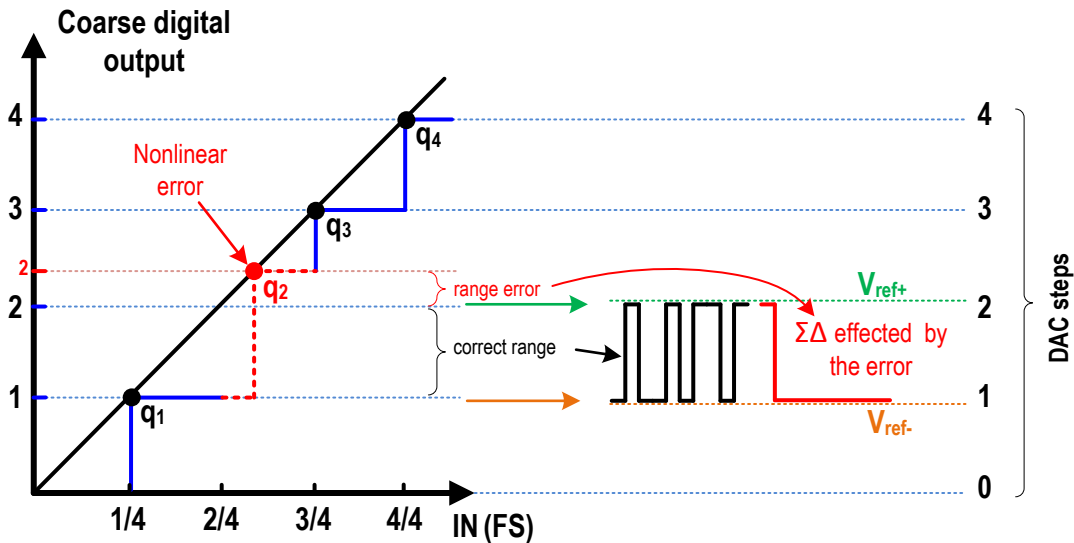


Figure 2.10. Nonlinear error of the coarse ADC

If there is a nonlinear error in the quantization steps of the SAR ADC, then it might cause the  $\Sigma\Delta$  ADC to zoom-in to an incorrect range as shown in Fig. 2.10 in an example 2-bit coarse case. In this example the 2<sup>nd</sup> quantization step of the SAR ADC  $q_2$  is in a wrong place (shown in red). Because of the transfer function of the SAR ADC is nonlinear (dashed red lines are the nonlinear part of the transfer function). Assuming the output of the SAR ADC is considered as the negative reference by the  $\Sigma\Delta$  ADC and the positive reference is 1-LSB higher than the negative one; if the signal is between the ideal and the non-ideal positions of the quantization level  $q_2$ , the  $\Sigma\Delta$  ADC uses incorrect references (1 and 2, instead of 2 and 3). There could be a problem even if the SAR ADC's quantization levels are perfect. Assume that

the input signal is very close to quantization step  $q_1$  in Fig. 2.10. The signal will be too close to the negative reference  $V_{ref-}$  of the  $\Sigma\Delta$  ADC. This usually causes instability of the  $\Sigma\Delta$  ADC [4]. In addition to these, thermal noise may cause  $\pm 1$ -LSB uncertainty in the SAR ADC, especially when the signal is close to the quantization thresholds. This would cause the  $\Sigma\Delta$  modulator to select the wrong references.

Tolerance to these errors can be increased by methods similar to the ones used in two-step or pipeline ADCs against stage gain errors. One method is to design the second ADC to use a range larger than the first ADC's quantization levels i.e. 1.5 or 2 bits instead of 1-bit. In this work, this method is referred as over-ranging. For the same example in Fig. 2.11, we now use 2-LSB<sub>coarse</sub> ranges in the  $\Sigma\Delta$  ADC instead of 1-LSB<sub>coarse</sub> such that the negative reference is chosen by the SAR ADC output code (i.e.  $k$ ) and the positive reference by  $k+2$ . This case is shown in Fig. 2.11. It is clear that even if there is a relatively big quantization step error on the SAR ADC, the  $\Sigma\Delta$  ADC still work properly.

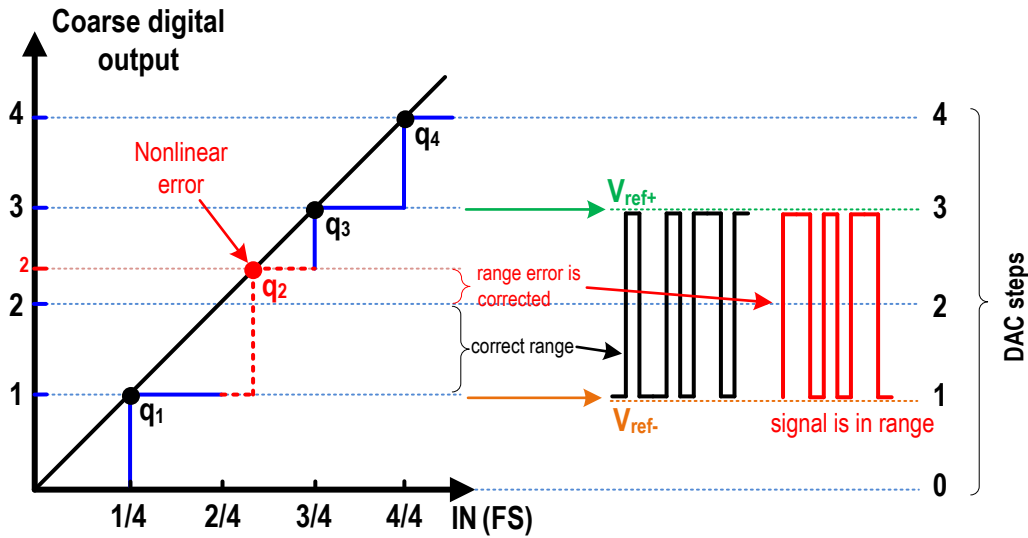


Figure 2.11. Over-ranging

Now the successive ranges are overlapping in such a way that the SAR ADC's quantization step points are shared between both possible ranges. All valid DAC reference ranges (the codes corresponding to the low and the high references) of the previous example are shown in Fig. 2.12. For instance, if the input is close to the coarse quantization level  $q_1$ , the SAR ADC's output would be either 0 or 1, which corresponds to the ranges 0-2 and 1-3 respectively in Fig. 2.12. For the signals higher than  $q_1$  both of the reference ranges are valid, but if the signal is actually just below  $q_1$  the range 1-3 would not be correct. Optimization of the over-ranging in order to solve these kinds of problems will be discussed later.

The total error introduced by the coarse ADC needs to be lower than half of the over-ranging factor (e.g. for 2-LSB over-ranging, the total error should be lower than 1-LSB) to provide an accurate representation of the input for fine ADC's references. If a  $\Sigma\Delta$  ADC is considered, the input sampling network should be linear to the wanted level (e.g. 20-bit) and the noise introduced by sampling should be lower than the signal with a certain ratio, i.e. signal-to-noise ratio (SNR). Assuming an ideally linear sampling operation, the DAC component matching is the main limit of the linearity of the fine converter. As it discussed, DEM can be used to improve the linearity of multi-bit DACs. Errors introduced by the quantizer is suppressed by the filter gain like all  $\Sigma\Delta$  ADCs. However, the loop filter's performance is

important to determine the final performance of the whole system. This will be discussed in detail later in Chapter 3.

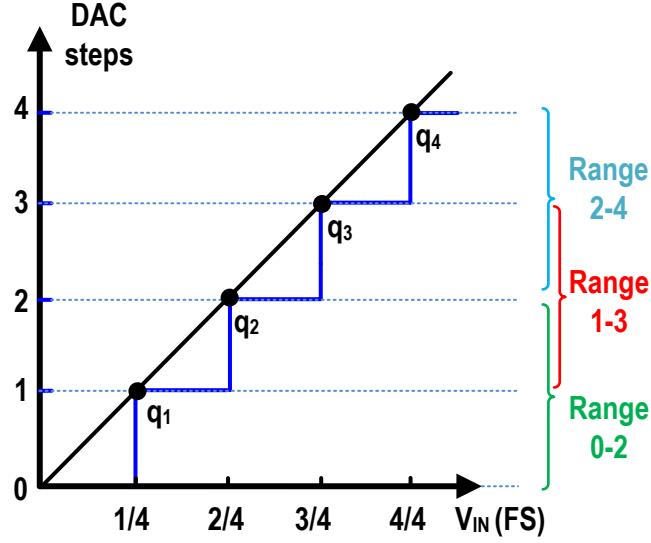


Figure 2.12. Reference ranges of the  $\Sigma\Delta$  ADC for 2-bit coarse quantization

## 2. 5. Incremental Zoom ADC (previous design)

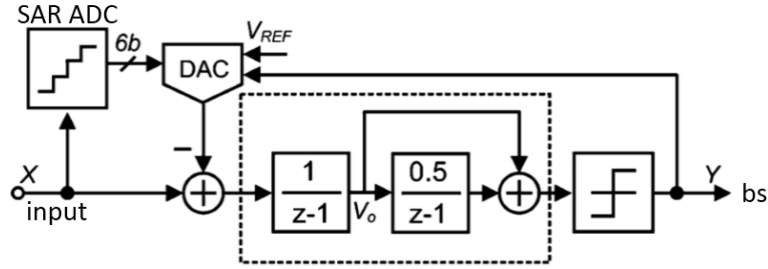


Figure 2.13. Block diagram of the incremental zoom ADC (From [7])

In previous works, two incremental zoom-ADCs have been proposed. The first one [17] is used in a temperature sensor as a proof of concept. The second work [7] aimed to demonstrate the energy efficiency of the zoom ADC concept. Both of them used a coarse SAR ADC in conjunction with a fine  $\Sigma\Delta$  ADC (Fig. 2.13). Two step conversion is performed sequentially: first, the SAR ADC determines a coarse approximation of the input signal, and then the coarse result is used to adjust the references of the  $\Sigma\Delta$  ADC to zoom into a small range around the signal (Fig. 2.14).

The sequential operation allows the SAR and the  $\Sigma\Delta$  ADCs to share the same hardware. During the coarse conversion, a 6-bit DAC and a comparator are used together with SAR logic. In the succeeding fine conversion phase, a 2<sup>nd</sup>-order incremental  $\Sigma\Delta$  ADC uses the same 6-bit DAC and the comparator with a second order feed-forward loop filter. Thus, mismatches between the coarse and the fine phases are minimized. The loop filter employs inverter based pseudo-differential integrators for a good energy efficiency. DEM is applied on the DAC in the fine conversion phase. A system-level low frequency chopping, which is chopping the whole ADC for two successive conversions and averaging the results, is used to reduce the offset as shown in Fig. 2.14.

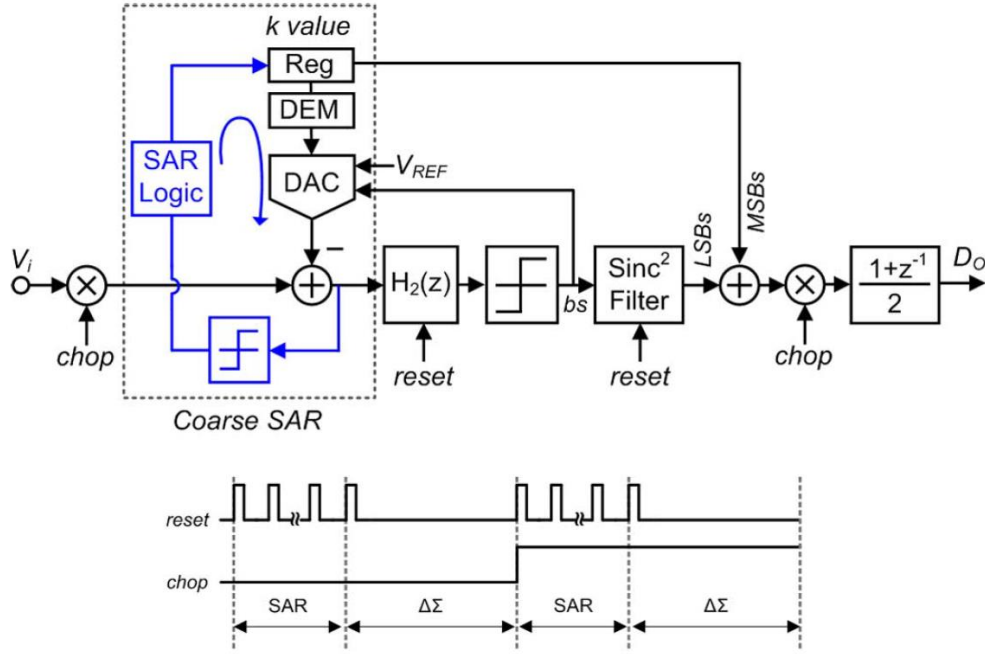


Figure 2.14. Incremental zoom ADC timing diagram (From [7])

The prototype chip was taped-out in 0.16 $\mu$ m CMOS process. It consumes 6.3 $\mu$ W power while achieving 20-bit resolution, 6-ppm INL and 1 $\mu$ V offset in a conversion time of 40ms. The ADC achieves the state-of-the-art 182.7dB FoMs which is the highest reported so far. Although the previous ADC achieves the state-of-the-art energy efficiency, its bandwidth is limited to pseudo-DC signals (12.5Hz BW) because of the sequential architecture. Thus, it was not suitable for dynamic signals.

## 2. 6. This work

The aim of this work is to increase the bandwidth of the zoom ADC to 20kHz (1600x increase), have an SNDR higher than 110dB while keeping the same energy efficiency, i.e. FoM. It is required to increase coarse ADC's sampling frequency as much as possible to increase the bandwidth as it will be explained in Chapter 3. For this purpose, the system is designed to have a coarse ADC that runs in parallel with the  $\Sigma\Delta$  ADC. In this way, it will be possible to update the references of the free-running  $\Sigma\Delta$  ADC without interrupting the conversion. It also provides the flexibility to optimize the coarse ADC's sampling frequency independent of the zoom ADC's output rate.

### 3. System Level Design and Optimization

A system-level diagram of a zoom-ADC is illustrated in Fig. 3.1. It consists of an  $L^{\text{th}}$ -order  $\Sigma\Delta$  modulator sampled at a sampling frequency  $F_s$ , an  $N$ -bit SAR ADC sampling at  $F_s/N$ , a DEM circuit, and a decimation filter. The system level parameters need to be optimized for the target specifications. In this work, the zoom-ADC is designed for audio applications, i.e.  $>110\text{dB}$  SNDR and  $20\text{kHz}$  bandwidth, by optimizing the following system level parameters: the number of coarse bits ( $N$ ), the sampling frequency ( $F_s$ ), over-ranging width ( $M$ ), and the order of the  $\Sigma\Delta$  modulator ( $L$ ). A DEM algorithm for the desired SNDR level should be implemented also.

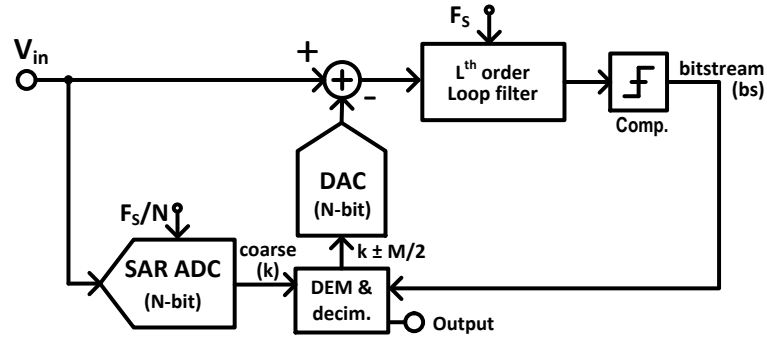
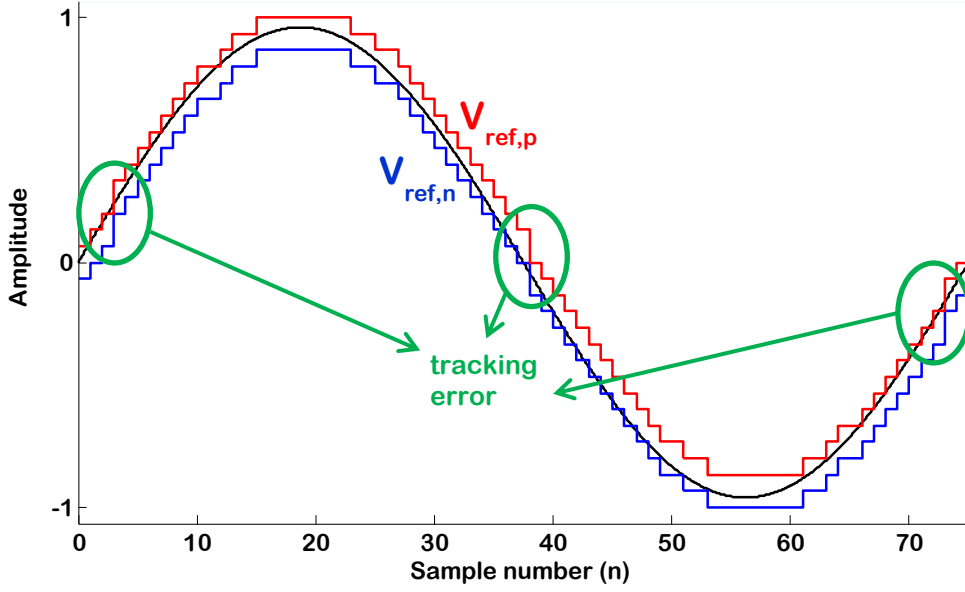


Figure 3.1. Block diagram of a zoom ADC

Increasing the SAR ADC's resolution lowers the amplitude of the signal processed by the  $\Sigma\Delta$  ADC. This is desirable because it reduces the signal swing at the input of the  $\Sigma\Delta$  ADC and thus relaxes the requirements on the dynamic range of the loop filter. So it might seem advantageous to increase the SAR ADC's resolution. However, this will increase the length of the SAR conversion (which takes  $N/F_s$ ), and more importantly, will decrease the maximum allowed input signal slope. This is because if the coarse output (and consequently the  $\Sigma\Delta$  references) is not updated frequently enough, the input signal may move out of the modulator's stable input range. This in turn, corresponds to a reduction in the zoom-ADC's large-signal bandwidth. An example of faulty tracking is illustrated in Fig. 3.2. The negative reference of the  $\Sigma\Delta$  is the conversion result of the SAR ADC ( $k \cdot V_{\text{LSB,SAR}}$ ) and the positive reference is 2 LSB higher than the negative one ( $(k+2) \cdot V_{\text{LSB,SAR}}$ ), corresponding to over-ranging factor ( $M$ ) of 2. Ideally, the signal should at least be between these two references in order to keep the  $\Sigma\Delta$  modulator stable. However, especially around the zero-crossing points of the signal the references are not at the correct levels.



**Figure 3.2. Tracking error of the coarse ADC**

The slope ( $S$ ) of the signal is maximum around the zero-crossings of a full-scale amplitude sinusoid with a frequency equal to the target bandwidth:

$$S_{max} = V_{FS} \cdot 2\pi \cdot f_{in,max} \quad (15)$$

The change in signal level should be smaller than the stable input range of the  $\Sigma\Delta$  modulator over one sampling period of the SAR ADC. An  $L^{\text{th}}$   $\Sigma\Delta$  order modulator has a stable input region which is a fraction ( $\alpha$ ) of its full-scale inputs. In the case of a zoom ADC, the full-scale inputs of the  $\Sigma\Delta$  modulator can be defined as  $M \cdot \text{LSB}_{\text{SAR}}$ ;

$$V_{FS,\Sigma\Delta} = M \cdot \frac{V_{FS}}{2^N} \quad (16)$$

The condition for proper operation can be formulated as:

$$V_{FS} \cdot 2\pi \cdot f_{in,max} < \alpha \cdot \frac{V_{FS} \cdot M}{2^N} \cdot \frac{1}{f_s/N} \quad (17)$$

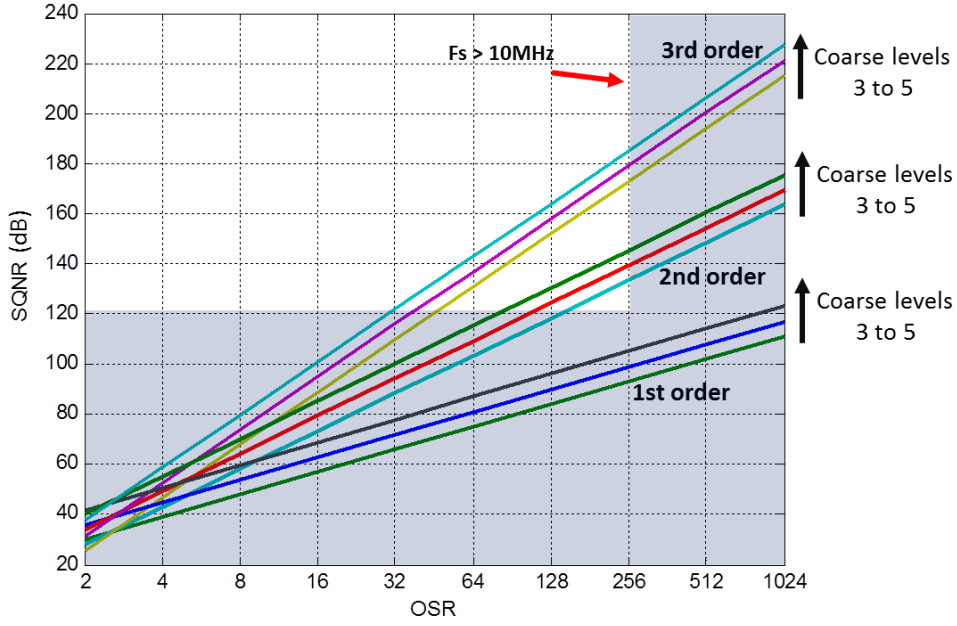
The maximum input signal frequency the zoom ADC can handle is then found as:

$$f_{in,max} < \frac{\alpha \cdot M \cdot f_s}{N \cdot \pi \cdot 2^{N+1}} \quad (18)$$

It is clear that the bandwidth of the zoom ADC is limited by the number of coarse bits, but can be improved by increasing the sampling frequency ( $f_s$ ) and the over-ranging width ( $M$ ). However, increasing the sampling frequency results in increased power consumption in the digital backend. On the other hand, low  $f_s$  gives rise to a low over-sampling ratio (OSR), which, depending on their filter order ( $L$ ), usually means lower SQNR for  $\Sigma\Delta$  modulators. It is possible to increase the loop filter order for lower OSR designs in order to improve the maximum SQNR at the expense of circuit complexity. In fact for very low

OSR, the benefit of using higher order loop filters becomes even less, which leads to lower energy efficiency.

Using the linear model, Fig. 3.3 shows the theoretical maximum SQNR vs. the OSR for different loop-filter orders ( $L$ ) and coarse levels ( $N$ ). For the chosen process,  $f_s$  is chosen to be 10MHz in order to keep the digital power consumption at a reasonable level, which translates into an OSR of 250. With this determined, the order of the  $\Sigma\Delta$  modulator required to obtain more than 120dB SQNR can be chosen from Fig. 3.3 as 2 or 3. Note that the data shown is derived from the linear model, which is much too optimistic. The 2<sup>nd</sup> order  $\Sigma\Delta$  modulator just barely achieves the required SQNR level, and so in a real implementation this does not leave any margin for non-idealities. Thus, a 3<sup>rd</sup> order loop filter was chosen.



**Figure 3.3. OSR vs  $SQNR_{max}$  for different orders of noise shaping and coarse levels**

Since the sampling frequency ( $f_s$ ) and the order of the loop filter ( $L$ ) have now been determined, only the coarse resolution ( $N$ ) and the over-ranging width ( $M$ ) are left. Basically, the highest possible coarse resolution is wanted to maximize energy efficiency. However, high  $N$  means lower bandwidth (recalling Eq. 18). This can be improved by increasing  $M$ , which also relaxes the SAR ADC design since it reduces the zoom ADC's sensitivity to the SAR ADC's noise, linearity and offset.

In Fig. 3.4 the trade-off between the number of coarse bits ( $N$ ), over-ranging width ( $M$ ) and maximum input frequency  $f_{in,max}$  described by Eq. 4 is illustrated for  $f_s=10\text{MHz}$  and  $\alpha=0.5$  (estimated for 3<sup>rd</sup> order  $\Sigma\Delta$  modulator). For bandwidths greater than 20kHz, the maximum number of coarse bits  **$N=5$**  (provided that  $M>4$ ). In order to relax the matching requirements of the SAR ADC's DAC elements,  **$M$  is chosen as 5**. This means that for a the SAR ADC output of  $k$ , the positive reference is  $k+3$  and the negative reference is  $k-2$ .

So, this work consists of a 5-bit SAR ADC and a 3<sup>rd</sup> order  $\Sigma\Delta$  modulator operating at a sampling frequency of 10MHz and employing 5-LSB over-ranging.

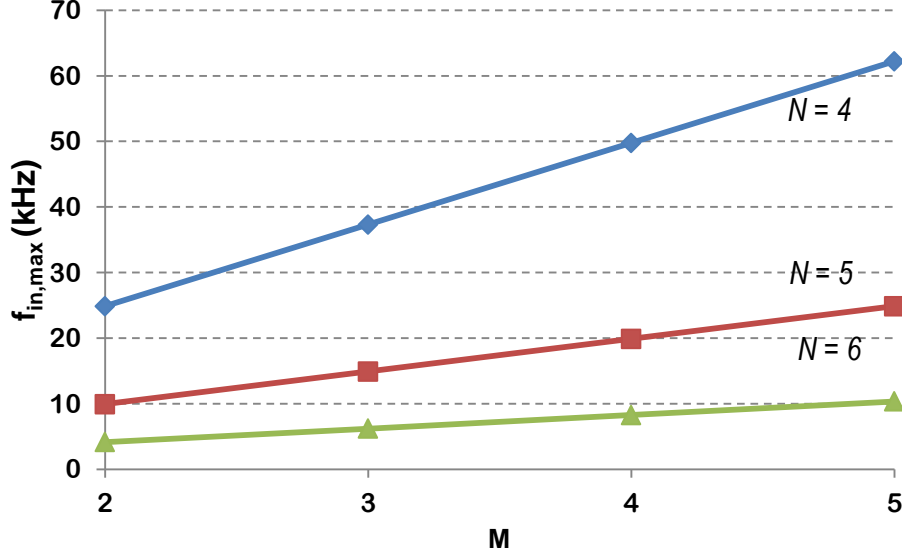


Figure 3.4. Coarse resolution (N), over-ranging width (M) and maximum frequency trade-off

### 3. 1. System-level design of the $\Sigma\Delta$ modulator ( $\Sigma\Delta$ M)

The zoom ADC can be implemented with a continuous-time  $\Sigma\Delta$ M. However, DEM is needed for the required SNDR levels, which requires an additional processing time between quantization instances and the time DAC feedback is applied. It is usually not an problem for a discrete-time  $\Sigma\Delta$ M but the increased loop-delay for a continuous-time  $\Sigma\Delta$ M is undesirable because of the excess loop delay sensitivity. Thus, DEM circuit implementation is much harder for a continuous-time  $\Sigma\Delta$ M [16]. Another disadvantage of the continuous-time approach is the sensitivity to clock jitter. The jitter sensitivity is needs to be relaxed, at least to the level of practical low-cost oscillator's jitter performance (e.g.  $\sim 1$ ps) for this work. Moreover, some sort of  $1/f$  noise cancellation is required considering desired high SNR level. While auto-zeroing can be applied easily for a discrete-time  $\Sigma\Delta$ M, chopping is required for continuous-time  $\Sigma\Delta$ M. However, chopping at  $f_s/2$  might be problematic due to the risk of fold-back of the shaped quantization noise to the baseband. It is also required to calibrate the coefficients of the continuous-time  $\Sigma\Delta$ Ms due to large spread of the absolute values of the circuit parameters determining the loop coefficients. However, discrete-time  $\Sigma\Delta$ Ms are usually implemented as switched-capacitor circuits which rely on relative values of the capacitors, which is much accurate without any sort of calibration.

Due to the reasons listed above, a discrete-time  $\Sigma\Delta$  modulator implementation is chosen for this work.

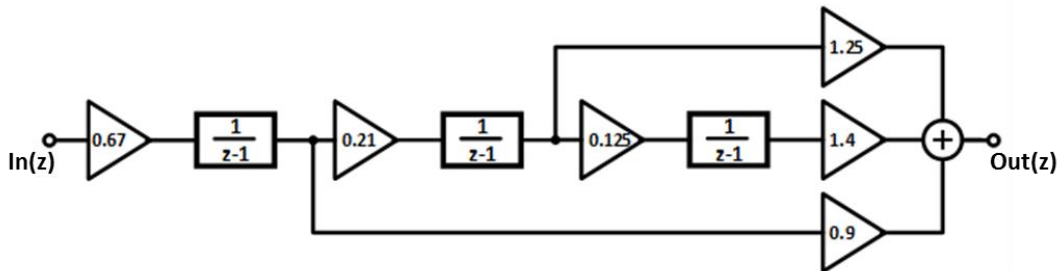


Figure 3.5. The loop-filter with the coefficients



The coefficients of the  $\Sigma\Delta$  modulator are obtained using the Delta-Sigma Toolbox [18] for a non-aggressive noise shaping, since the OSR is already high enough. The transfer function is then mapped to a cascade-of-integrators with feed-forward (CIFF) loop filter as shown in Fig. 3.5. The simulated spectrum of the 1-bit  $\Sigma\Delta$  modulator with a sample sinusoidal input is shown in Fig. 3.6. SQNR vs input amplitude of the modulator is shown in Fig. 3.7.

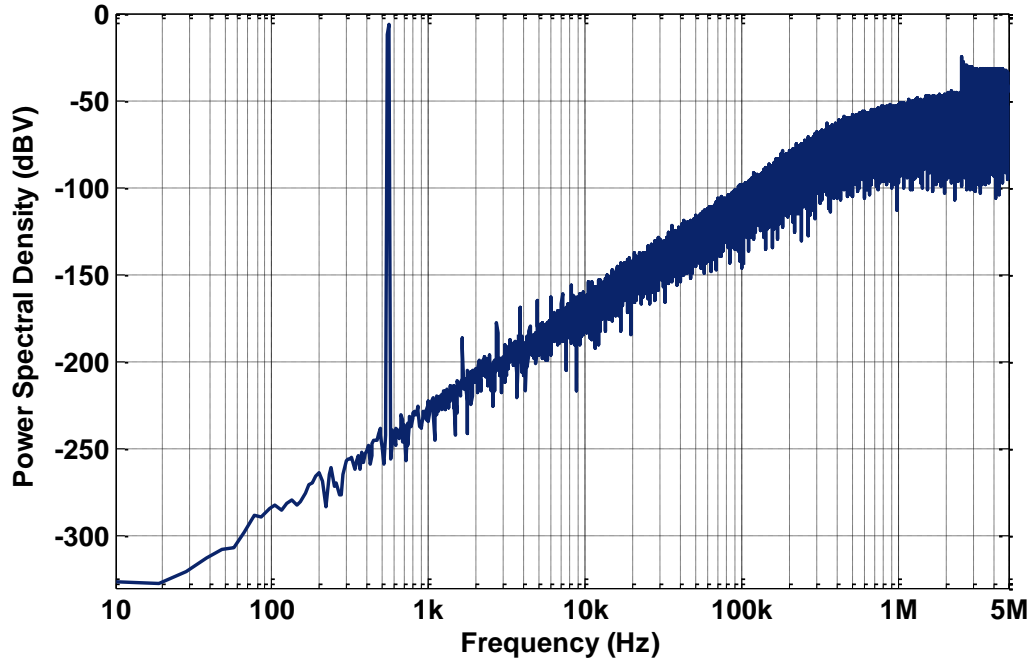


Figure 3.6. Simulated Spectrum of the 1-bit  $\Sigma\Delta$  modulator

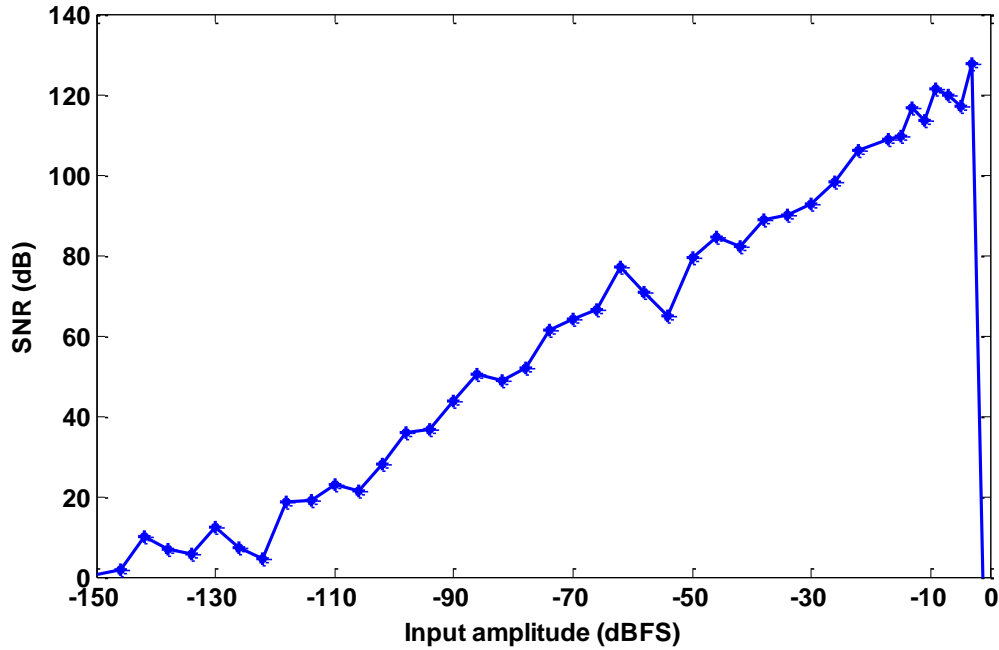


Figure 3.7. Simulated SQNR vs input amplitude for the 1-bit  $\Sigma\Delta$  modulator ( $\text{SQNR}_{\max} = 127\text{dB}$ )

The block diagram of the designed zoom ADC is given in Fig. 3.8. It consists of a 5-bit SAR ADC, and a third order  $\Sigma\Delta$  modulator and a  $\text{sinc}^3$  decimation filter. The  $\Sigma\Delta$  modulator consists of a 3<sup>rd</sup> order feed-forward loop filter, a 1-bit quantizer, and a 5-bit DAC with DEM.

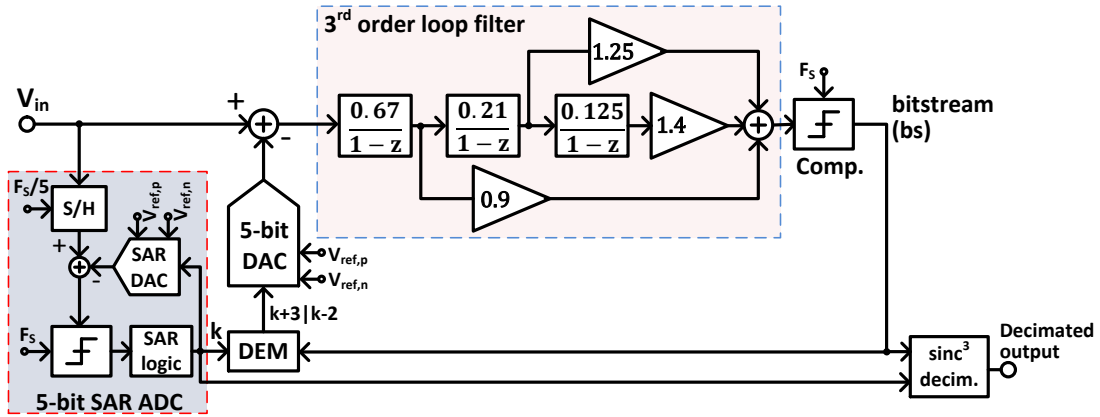


Figure 3.8. The block diagram of the designed zoom ADC

A behavioral model of the zoom ADC (including the error sources which will be discussed later), was built in Simulink. A simulated output spectrum of the zoom ADC is shown in Fig. 3.9 for  $f_{in}=18\text{kHz}$ . The SNR is calculated as 120.44dB, and is DEM mismatch noise limited. The output swings of the integrators shown in Fig. 3.10 (normalized to 1V full-scale). The integrators' output swings are low as expected.

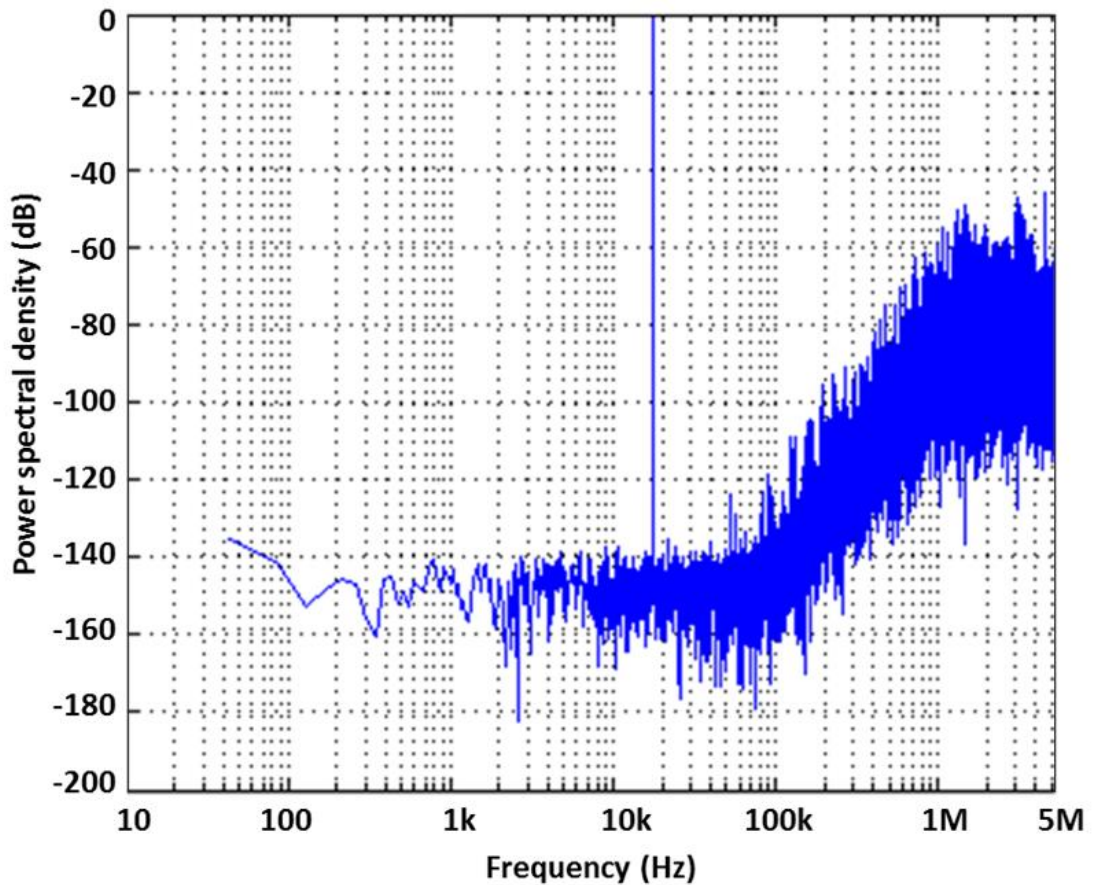


Figure 3.9. A simulated output spectrum of the zoom ADC

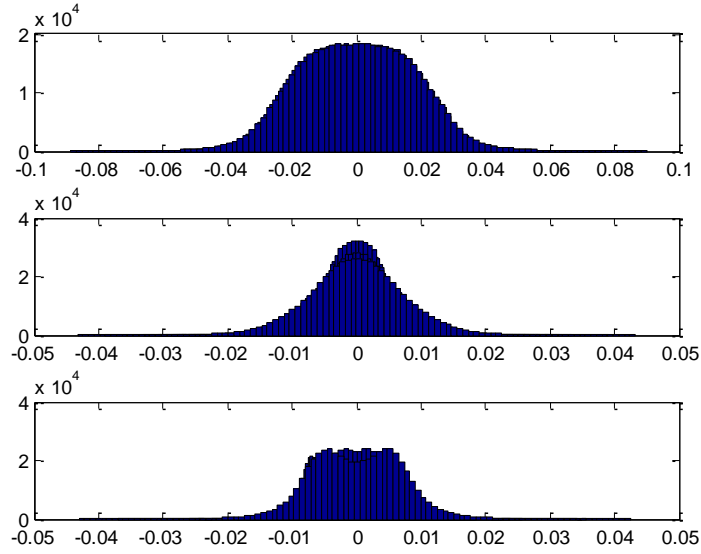


Figure 3.10. 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> integrator swings respectively, normalized to 1V full-scale

### 3. 2. Error sources of the system

So far it has been assumed that every block of the system is ideal. However, a real system suffers from several non-idealities. The gain and bandwidth of the circuit elements are usually limited by the power budget, which may limit the settling time and accuracy of the switched-capacitor analog circuits. The values of the circuit elements spreads due to production tolerances, which, in turn, leads to offset, gain errors and non-linearity. Also all the noise sources should be taken into account, as they should limit the desired SNR.

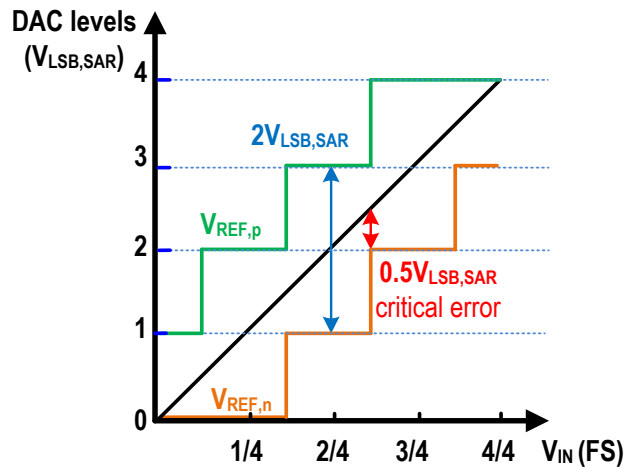


Figure 3.11. Critical error point for the case  $M=2$

#### 3.2.1. Matching requirements of the SAR ADC

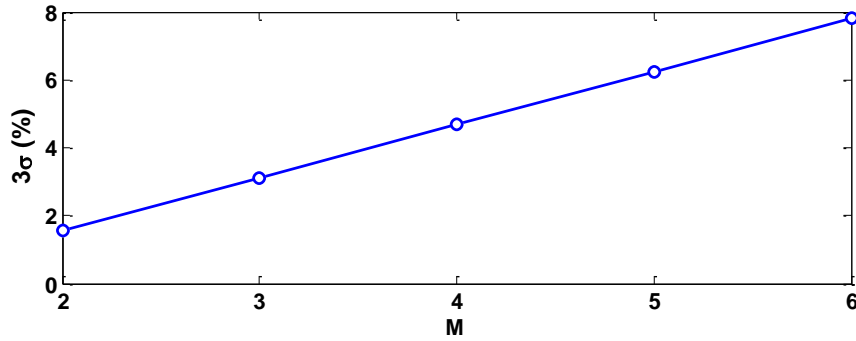
A sequential zoom ADC like [7] can use the same DAC and the same comparator for the coarse and the fine conversions, thus ensuring that the relative matching of the quantization levels of coarse and the fine converters is perfect. However, the SAR ADC of a dynamic zoom ADC needs to employ its own

DAC and comparator in order to perform the coarse conversion in parallel to the fine conversion. This immediately makes the system vulnerable to any offset error between the SAR comparators and the  $\Sigma\Delta$  DAC, and integral-nonlinearity (INL) error between the two DACs. In fact, the SAR ADC now needs to have an INL better than the final aim. For example if the zoom ADC needs to have 20-bit linearity, the SAR ADC should have better than 20-bit INL. However, designing a SAR ADC at that level of accuracy is neither easy nor desirable [19].

In order to relax the matching requirements of the coarse and fine paths, the over-ranging width  $M$  can be increased. If the range of the  $\Sigma\Delta$  modulator is 2 coarse LSB wide ( $M=2$ ), the INL requirement of the SAR ADC relaxes because there is an overlap of  $1-V_{LSB,SAR}$  between the  $\Sigma\Delta$  DAC output ranges. As shown in Fig. 3.11, the maximum error which can be tolerated is  $0.5V_{LSB,SAR}$ . For higher levels of over-ranging, the requirements relaxes more. In fact, the maximum error, expressed as three times the standard deviation of the random error, can be formulated as:

$$3\sigma_{err} < \frac{M-1}{2^{N+1}} \quad 19)$$

Apart from the unit element matching of two different DACs, the offset between coarse and the fine path is also important. So the total tolerable error budget should be divided between comparator offset and DAC unit element mismatch. The comparator is usually the dominant offset source of SAR ADCs, but for a  $\Sigma\Delta$  modulator the offset of the comparator is divided by the loop-filter gain. However, the offset of the  $\Sigma\Delta$  modulator is dominated by the DAC's offset.



**Figure 3.12. Matching requirement of the SAR ADC vs.  $M$**

$\sigma_{err}$  versus  $M$  is shown in Fig. 3.12. Since  $M=5$  is already chosen, the unit element mismatch requirement on the DAC and comparator offset error combined is only 2% ( $1\sigma$ ). Since both error sources are uncorrelated:

$$\sigma_{err} = \sqrt{\sigma_{ofst}^2 + \sigma_{C,DAC}^2} \quad 20)$$

Assuming the error sources equal, each of them should have  $\sigma = 1.4\%$ . The maximum INL error on a binary weighted DAC occurs at the MSB-1 crossing point. For a 5-bit DAC it is:

$$\sigma_{C,tot} = \sqrt{\sigma_{1C}^2 + \sigma_{2C}^2 + \sigma_{4C}^2 + \sigma_{8C}^2 + \sigma_{16C}^2} \quad 21)$$

Total standard deviation of the DAC can be found as:

$$\sigma_{C,tot} = \sqrt{31} \cdot \sigma_{1C} \quad (22)$$

The minimum unit capacitance size then can be determined for the given process considering  $\sigma_{C,tot} < \sigma_{C,DAC}$ :

$$\begin{aligned} \sigma_{1C} &< \frac{\sigma_{C,DAC}}{\sqrt{31}} \\ \sigma_{1C} &< 0.25\% \end{aligned} \quad (23)$$

The DAC of the SAR ADC should have roughly 8-bit unit element matching.

### 3.2.2. $\Sigma\Delta$ modulator DAC matching requirements and DEM

In order to meet the target specifications, the DAC of the  $\Sigma\Delta$  modulator should achieve 20-bit matching. . This is, however, quite impractical for standard CMOS technologies [20]. There are a number of techniques to improve the linearity such as trimming, background or foreground calibration and dynamic element matching (DEM) [1, 4, 8]. Oversampled data converters benefit most from the latter, because it does not increase production costs like trimming, nor does it need to interrupt the conversion like in foreground calibration, and finally it does not need complex digital logic as in background calibration.

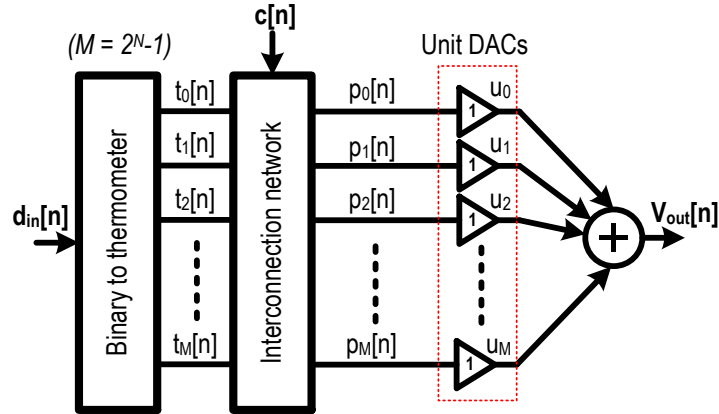


Figure 3.1. Block diagram of a DAC with DEM

DEM selects a different set of elements of a unary DAC at each period, even for the same DAC input code, in order to average the matching errors [4]. An example block diagram of a DAC employing DEM is shown in Fig. 3.13. First of all, the binary data is transformed into a thermometric (unary) form in order to be able to use and select unary elements such that the sum of the unary code is equal to the binary value:

$$d_{in} = t_0 + t_1 + t_2 + \dots + t_M \quad (24)$$

Then the thermometric code is passed through an interconnection network which connects the thermometric code inputs to the unit DAC with the starting pointer  $C[n]$  such that on each period a different set of unit elements are selected while keeping the same sum equal to the binary input:

$$d_{in} = p_0 + p_1 + p_2 + \dots + p_M \quad 25)$$

Finally, the output of the unit DACs are summed in analog domain. There are several known DEM algorithms such as random selection, barrel-shifting or mismatch-shaping. The difference between these algorithms is in how they determine the unit selection pointer  $C[n]$ .

### 3.2.2.1. Randomizing DEM

If the active unit DACs are selected randomly during each sampling period, their mismatch is then modulated by that random distribution [4]. This ensures that the mismatch between codes is zero on average and that the spectral power density of the nonlinearity due to mismatch is spread over the Nyquist bandwidth. This means that the harmonic components are suppressed at the expense of increased noise power.

### 3.2.2.2. Barrel-shift DEM

Barrel-shifting DEM uses a barrel-shift register pointer to track the first unit element to be selected, such that at each cycle the DAC starts from the element next to the first element selected in the previous cycle (Fig. 3.14). This DEM scheme is known to generate a tone at  $f_s/(2^N-1)$  for an N-bit DAC because it repeats the averaging process with this period.

Cycle	DAC	Pointer	DAC elements				
1	2	0					
2	1	1					
3	3	2					
4	2	3					
5	3	4					

**Figure 3.1. Barrel-shift DEM for a 5-unit DAC**

The residual error after k cycles of barrel-shifter DEM for an N-bit DAC is [7];

$$\sigma_{tot} = \frac{\sqrt{2^N - 1}}{k} \cdot \sigma_{unit} \quad 26)$$

### 3.2.2.3. Mismatch shaping

Since the pointer  $C[n]$  can be an arbitrary function, it is possible to realize a so-called mismatch shaping function which essentially shapes the residual mismatch noise to have a lower power in the bandwidth of interest.

A very practical and hardware efficient realization of first order mismatch shaping is so-called data weighted averaging (DWA). It uses the previous output code of the DAC to shift the starting pointer such that:

$$C[n] = \text{mod}_M( C[n - 1] + d_{in}[n - 1] ) \quad (27)$$

In this way at each clock cycle the DAC output starts from an unused unit of the previous cycle as shown in Fig. 3.15. This is effectively a 1<sup>st</sup> order  $\Sigma\Delta$  modulator which shapes the mismatch noise [4]. It is also possible to realize higher order mismatch shaping.

Cycle	DAC	Pointer	DAC elements					
1	2	0	■	■				
2	1	2			■			
3	3	3				■	■	■
4	2	0	■	■				
5	3	2			■	■	■	

Figure 3.2. DWA for a 5-unit DAC

In this work, barrel-shifter and DWA algorithms are implemented on-chip in order to improve linearity of the DAC of the  $\Sigma\Delta$  modulator.

### 3.2.3. Finite DC gain, bandwidth and slew-rate and thermal noise of the OTAs

In the designed Simulink model, circuit non-idealities have been included in order to find the required specifications for DC gain and unity gain bandwidth (UGBW) of the OTAs of the three integrator. The integrator model used in the Simulink simulations is shown in Fig. 3.16. Finite unity gain bandwidth (UGBW) of the OTAs limits the settling time and cause an integrator gain error ( $\beta$ ):

$$\beta = 1 - e^{-\frac{T_s}{2\pi \cdot \text{UGBW}}} \quad (28)$$

The finite DC gain of the OTA causes the unity gain error:

$$\alpha = 1 - \frac{1}{A_{DC}} \quad (29)$$

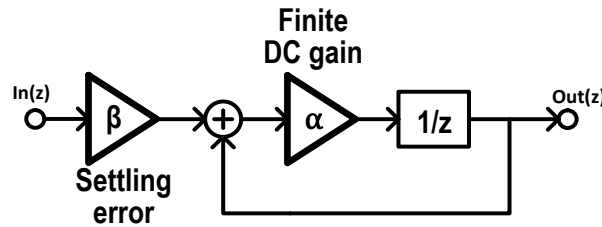


Figure 3.3. Discrete integrator model with settling error and finite DC gain

DC gain of a real integrator is limited by the finite gain of the OTA. It also shifts the zeros of the NTF from their ideal positions and usually the following criteria should be met [8]:

$$\pi \cdot A_{DC} \gg OSR$$

30)

Finite slew-rate might be problematic because it would affect the linearity of the integrator, especially if a large swing is required. However, for a zoom ADC the integrators do not require to handle large swinging signals. So, the slew rate becomes less of a problem with zooming. This relaxes the unity gain bandwidth requirement because the time for exponential settling is now higher.

It is known that the error introduced by the 2<sup>nd</sup> and 3<sup>rd</sup> integrators are shaped by the loop filter. Thus the performance of the first integrator is the most critical for the overall performance of the  $\Sigma\Delta$  modulator. Thus the succeeding integrators are less of a problem because of the noise shaping. In order to keep the achievable quantization noise in 20kHz bandwidth low enough for 110dB, the specifications required for the OTAs are given in Table 1. The SNR mentioned is the input referred signal-to-thermal noise ratio for an input signal with a full-scale amplitude.

OTA	DC gain	Slew rate	UGBW	SNR	Output swing
1 <sup>st</sup>	60 dB	15 V/us	30 MHz	116dB	400 mV <sub>pp</sub>
2 <sup>nd</sup>	40 dB	10 V/us	20 MHz	66dB	200 mV <sub>pp</sub>
3 <sup>rd</sup>	40 dB	10 V/us	20 MHz	26dB	200 mV <sub>pp</sub>

**Table 1. Circuit specifications for the OTAs**

Any error (finite gain, finite UGBW, offset, and noise) introduced by the 1<sup>st</sup> OTA will be right in the front of the loop filter and will not be suppressed by any gain. However, the errors introduced by the 2<sup>nd</sup> and the 3<sup>rd</sup> OTAs are suppressed by the gains of the preceding stages. For this reason, the 1<sup>st</sup> OTA needs to have the highest gain and UGBW, as well as the lowest noise and offset.



## 4. Circuit Implementation

In this chapter, circuit design details will be discussed. The prototype chip is implemented in SSMC 0.16 $\mu$ m 1P5M CMOS process.

### 4. 1. Inverter-based $\Sigma\Delta$ ADC

Fig. 4.1 shows the block diagram of the designed zoom ADC with simplified schematics of the capacitive DAC and the 1<sup>st</sup> integrator of the  $\Sigma\Delta$  modulator. Inverter-based pseudo-differential operational transconductance amplifiers (OTAs) are used to implement the integrators of the  $\Sigma\Delta$  modulator. In this chapter, the design details of each circuit block will be discussed.

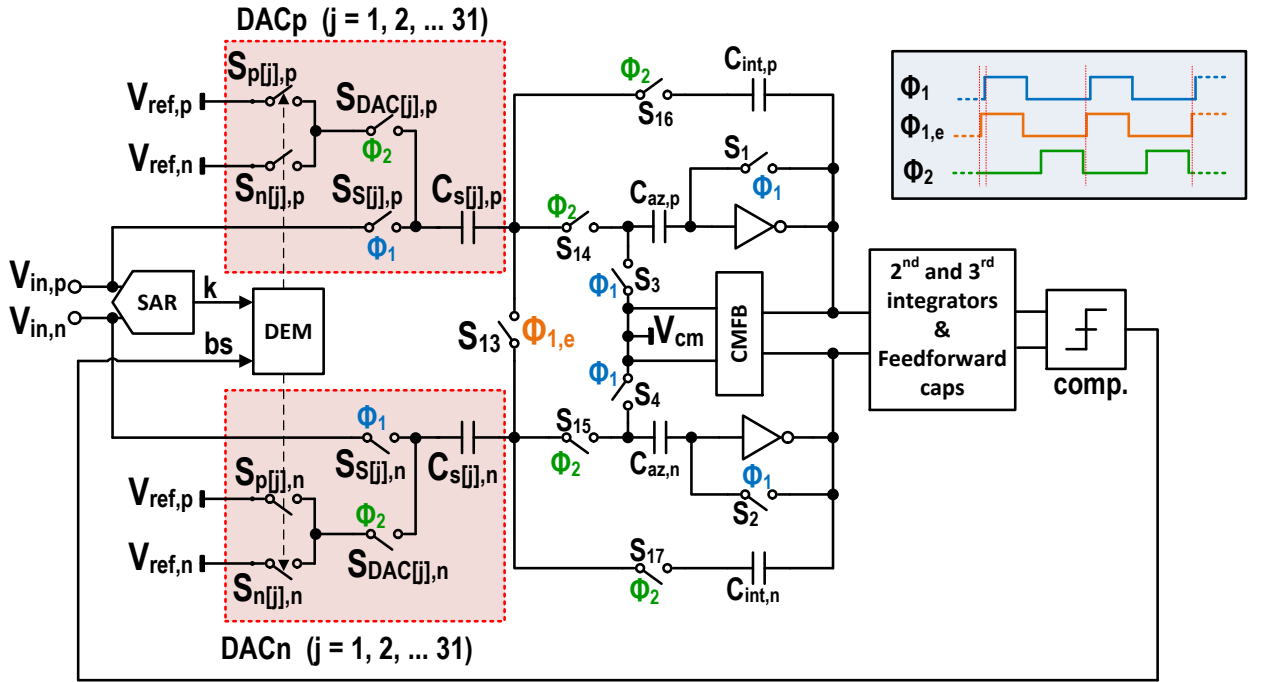


Figure 4.1. Block diagram showing the simplified schematic of the  $\Sigma\Delta$  modulator

### 4. 2. The sampling network

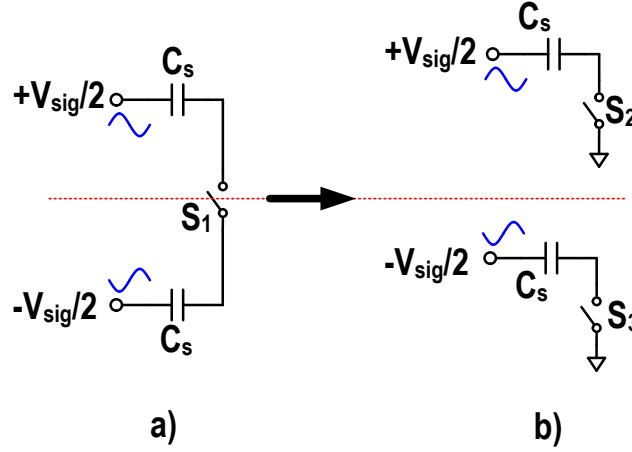
The sampling network consists of the capacitive DACs ( $DAC_{p,n}$ ) and the switch  $S_{13}$  In Fig. 4.1. The DACs are formed by splitting the sampling capacitances to 30 unit elements. During the sampling phase  $\Phi_1$ , the differential input is sampled by all unit elements  $C_{s[0-30],p}$  and  $C_{s[0-30],n}$ . In the following phase  $\Phi_2$  the DACs either add or subtract fixed amount of charges depending on the SAR ADC's output  $k$ , and the bit-stream  $bs$  in order to form the subtraction node at the  $\Sigma\Delta$  modulator's input. Before diving into the details of the DAC, the noise and the offset requirements of the sampling network will be discussed first.

#### 4.2.1. Input referred noise

In this work, the SAR ADC's noise is not critical because an over-ranging level of 5-LSB is used, as discussed in chapter 2. For the  $\Sigma\Delta$  modulator, the total noise budget can be determined for 116dB SNR, for 3.5V full-scale differential input it corresponds to an integrated noise of;

$$v_n = \frac{3.5/2\sqrt{2}}{10^{\left(\frac{116}{20}\right)}} = 3.9\mu V_{rms}$$

To achieve the target SNR level, the input referred noise budget can be divided between  $kT/C$  noise and the other noise sources preceding the sampling action. For a  $\Sigma\Delta$  modulator this is dominated by the input-referred noise of the first integrator since the noise sources of the succeeding integrators in the loop-filter is suppressed by the gain of the first integrator. Assuming that half of the noise budget is reserved for the loop filter's input referred noise, it should be lower than  $2.75\mu V_{rms}$ . So, the first integrator's OTA should be designed to meet this specification. To mitigate its low-frequency noise, a dynamic noise and offset reduction technique such as chopping or auto-zeroing is desirable.



**Figure 4.2. a- The implemented sampling circuit, b- Split version of the sampling circuit**

The other half of the noise budget is for the  $kT/C$  noise. The sampled thermal noise power, or  $kT/C$  noise in other words, is given by:

$$\overline{v_n^2} = \frac{1}{OSR} \cdot \frac{kT}{C_s} \quad 31)$$

Where OSR is the over-sampling ratio,  $C_s$  is total sampling capacitance,  $k$  is Boltzmann constant and  $T$  is temperature in  $^{\circ}K$ . The sampling scheme used in this design is shown in Fig. 4.2-a. It can be split into two equal parts as in Fig. 4.2-b. The differential noise power is:

$$\overline{v_n^2} = \frac{kT}{OSR} \cdot \left( \frac{1}{C_s} + \frac{1}{C_s} \right) = \frac{2kT}{OSR \cdot C_s} < (2.75\mu V)^2$$

The minimum sampling capacitor size for 110dB SNR can be found with  $OSR = 250$  and full-scale input amplitude  $V_{sig} = 3.5V$  at room temperature ( $T = 300^{\circ}K$ ) as  $C_s > 4.37pF$  ( $C_{s,n}$  and  $C_{s,p}$  in Fig. 4.1 are equal to  $C_s$ ).

#### 4.2.2. Input referred offset

The ADC's input offset is mainly determined by the charge injection mismatch of the sampling switch  $S_1$ , the first integrator's switches  $S_{16,17}$  and the input offset of the 1<sup>st</sup>-integrator's OTA. The phases in Fig. 4.1 are simplified to  $\Phi_1$  and  $\Phi_2$  for the sake of clarity. In the implementation, there are early, normal and delayed versions of each clock phase and their complementary versions. These multiple phases are used to perform bottom-plate sampling, and reduce the charge-injection effects of the switches on any sampling instance.

As shown in Fig. 4.1, sampling is done by opening one switch ( $S_{13}$ ) in an early phase of  $\Phi_{1,e}$ . If  $C_{s,n}$  and  $C_{s,p}$  are the same, charge-injection of  $S_{13}$  will be ideally differential and result a zero offset. However, the mismatch of the of sampling capacitors  $C_{s,n}$  and  $C_{s,p}$  gives rise to a mismatched effect of the charge-injection, resulting an offset voltage. A minimum size transistor ( $W=0.768\mu\text{m}$ ,  $L=0.16\mu\text{m}$ ) driven by 1.8V has about 1.5fC of channel charge. Assuming the channel charge is injected equally to  $C_{s,n}$  and  $C_{s,p}$ , if they are equal to 4pF (due to the noise reasons discussed before), with 1% mismatch the offset voltage would be 2.4 $\mu\text{V}$ . At the end of the integration phase  $\Phi_2$ , the charge-injection of  $S_{16,17}$  also results in an offset voltage on the integration capacitors  $C_{\text{int},n-p}$  due to the mismatches of the switches and the capacitances which can be expected to be in the same order of magnitude as the offset calculated before.

The input-referred offset of the implemented zoom ADC is dominated by the input-referred offset of the OTA, which is auto-zeroed for low offset. In previous work, low-frequency chopping (at 25Hz) was applied to further reduce the offset of an incremental zoom ADC to 1 $\mu\text{V}$  level [7]. However, low-frequency chopping is not used in this work because for audio applications the chopping frequency should be higher than 20kHz, which would probably not result in significantly less offset than with auto-zeroing.

#### 4.3. The DAC

The sampling capacitor is split in multiple units that can be used as a capacitive feedback DAC during the 1<sup>st</sup>-integrator's integration phase. The single-ended schematic of the unary capacitive DAC is given in Fig. 4.3. It consists of 31 unit elements, each consisting of a unit capacitor and 4 switches. During the tracking phase  $\Phi_1$ , the input is sampled by all unit elements  $C_{0-30}$ , which in total form the sampling capacitances. The unit capacitance is chosen to be 160fF, corresponding to a 4.96pF total sampling capacitance, as required to meet the  $kT/C$  noise requirements.

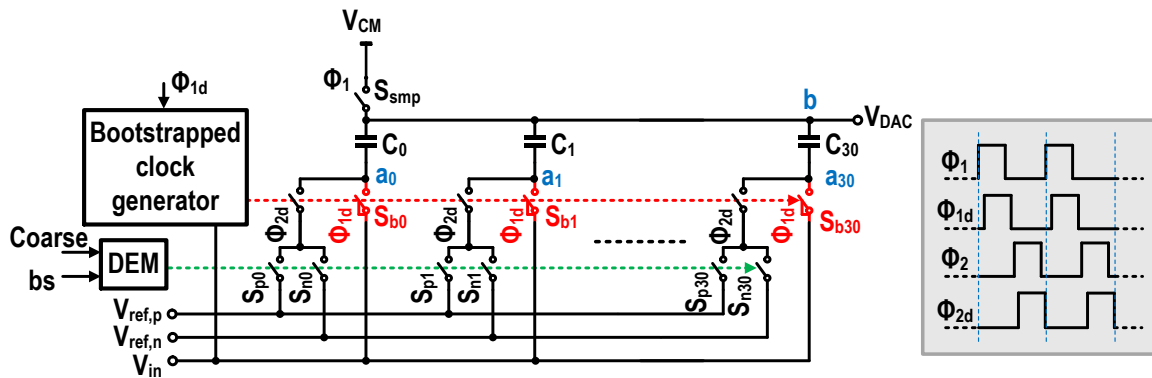


Figure 4.3. The DAC (single ended)

A bootstrapped clock generator is shared by the sampling switches  $S_{b,0-30}$ . During the integration phase  $\Phi_2$ , the units of the DAC are connected to either the positive or the negative references,  $V_{ref,p}$  and  $V_{ref,n}$  respectively, depending on the bitstream output of the modulator, and the output of the DEM logic.

In Fig. 4.4, a representative layout of the capacitor array, which is a modified version of the DAC used in a previous work [7], is shown. Metal fringe capacitors (using the metal layers from metal<sub>1</sub> to metal<sub>4</sub>) are used to implement the DAC because of their good linearity and matching. Since the node  $b$  in Fig. 4.3 is common for all the units, it is shared by all the fringes in the layout. The relative mismatch error of the unit elements was measured to be below 0.05% for a similar 6-bit DAC with the same unit capacitor size and layout (Fig. 4.5). The units on the edge of the layout have a larger error, up to 0.3%, probably because of edge effects. In the new layout, 10 dummy units are placed on each side of the capacitance array to reduce the edge effects.

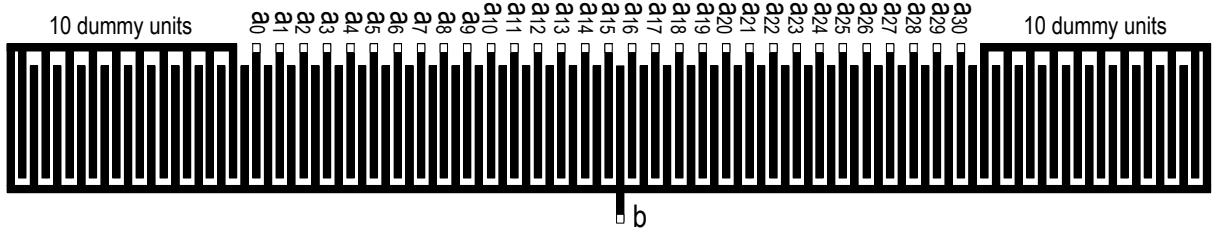


Figure 4.4. Sample layout of the DAC

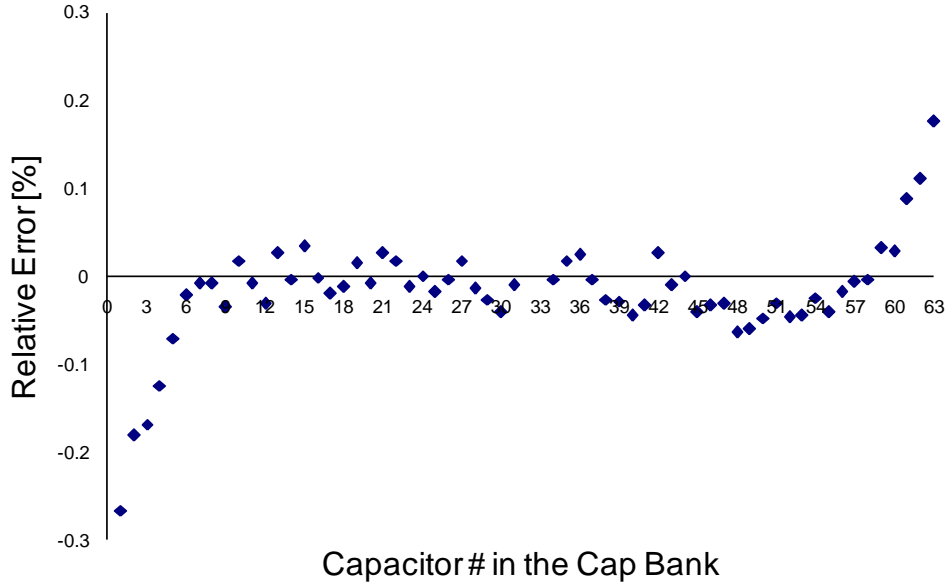


Figure 4.5. Relative matching of the unit fringe capacitances of a 6-bit DAC (courtesy of Y. Chae)

#### 4. 4. Bootstrapped switches

To implement the sampling switches  $S_{b,0-30}$  in Fig. 4.3 the CMOS pass-gate switch shown in Fig. 4.3 was initially used. However, its simulated third order distortion (HD3) was approximately -70dB. Thus, bootstrapped switches are needed to achieve the required linearity of >110dB. The bootstrap voltage generator circuit schematic is shown in Fig. 4.7 [21].

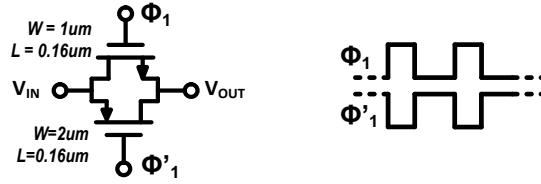


Figure 4.6. CMOS pass-gate switch

The circuit's operation is as follows. When  $\Phi_1$  is low,  $INV_1$  and  $M_2$  charges  $C_{boost}$  to  $V_{boost}=V_{DD}$ . When  $\Phi_1$  is high, the gate voltage of the bootstrapped switches  $M_{s[1..31]}$ ,  $V_{SW}$ , becomes  $V_{DD}+V_{IN}$ . Voltage stress on transistors  $M_5$  and  $M_7$  is avoided by  $M_3$  and  $M_6$ .  $C_{boost}$  is implemented as a 5pF MOS capacitor.

Only two bootstrap voltage generator circuits are used for the negative and the positive DACs. The simulated HD3 was better than -117dB HD3, and was the dominant distortion component in all corners while sampling 20kHz signals on a 5pF sampling capacitance, thus meeting the linearity specification.

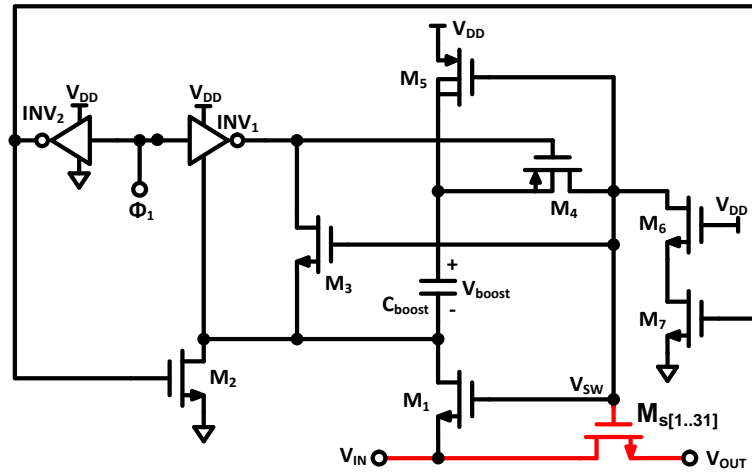


Figure 4.7. Bootstrap circuit [21]

## 4. 5. Inverter based OTA

### 4.5.1.Previous work

The inverter is one of the most basic CMOS amplifier structure. However, its biasing current and output common-mode voltage are signal dependent. In order to bias an inverter-based OTA, a dynamic biasing scheme combined with auto-zeroing was proposed in a previous work [7]. Since the operation of switched-capacitor integrators is usually divided into two phases; one for sampling and the other for integration, the two-step nature of auto-zeroing makes it a perfect fit.

An inverter-based OTA with cascode transistors for higher DC gain is shown in Fig. 4.8. In order to bias the cascoded inverter during the auto-zero phase, a floating current source might be used. By diode-connecting the input devices, the correct biasing voltages can be stored on the auto-zeroing capacitances  $C_{az}$  during the auto-zero phase. During this phase, the cascode devices' bias voltages must be generated by a bias generator circuit. Although this is relatively simple to do, the floating current source must be de-activated or disconnected during the subsequent integration phase..

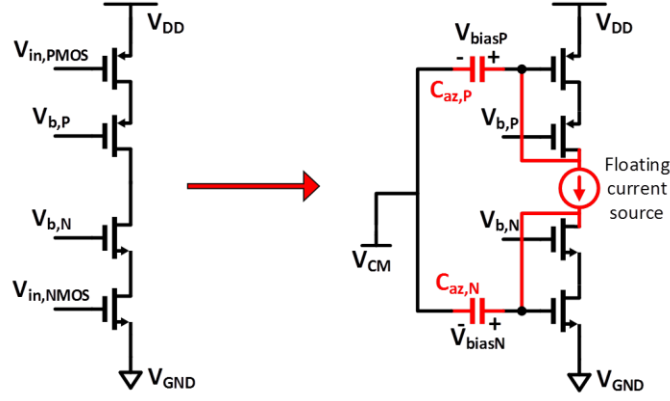


Figure 4.8. Inverter-based SC integrator

In previous work, the dynamic biasing scheme shown in Fig. 4.9 was used [7]. In the auto-zeroing phase, a floating current source ( $M_{7,8}$ ) is used to fix the current in  $M_1$  and  $M_2$ . During the amplification phase, the floating current source is disconnected and the output is connected to the input devices via the cascode transistors. The cascode transistors  $M_{3,6}$  are thus used to switch currents between the two branches. However, this approach has the downside that at the end of every period the biasing circuit needs to charge the gate capacitance of the cascode transistors  $M_{3,6}$  to the bias voltages  $V_{b0,1}$  in a relatively small fraction of the period. Since the cascodes are not minimum-size devices, since they have to carry enough current and provide enough output impedance, this requires a very low impedance biasing circuit. Although the noise introduced by the cascode transistors  $M_{5,6}$  is usually negligible, another disadvantage of this method is that their  $1/f$  noise is not cancelled because different sets of cascode transistors are used during auto-zeroing and amplification phases. As a result, the circuit's  $1/f$  noise performance suffers somewhat.

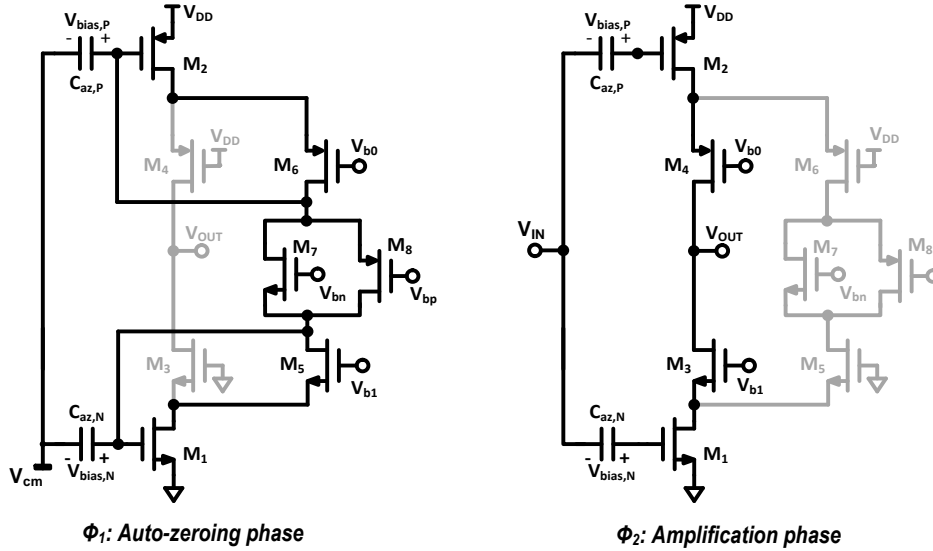


Figure 4.9. Inverter-based OTA proposed in [7].

#### 4.5.2. Proposed OTA

A novel biasing scheme for inverter-based OTAs is proposed in order to tackle the aforementioned problems. A schematic of the proposed pseudo-differential inverter-based OTA is shown

in Fig. 4.10, where the common-mode feedback (CMFB) circuit is not shown for the sake of simplicity. During the auto-zeroing phase  $\Phi_1$ , diode connections are formed through the switches  $S_{1,2}$  and  $S_{5,6}$  as in previous work. However, during the amplification phase  $\Phi_2$ , low-ohmic switches  $S_3$  and  $S_4$  are used to bypass the floating current sources ( $M_{9-12}$ ). Note that the cascode transistors  $M_{5-8}$  are never turned-off. Since the bypass switches  $S_3$  and  $S_4$  need to be driven by logic levels, the requirement on the output impedance of the biasing circuit is now removed. These switches can be implemented with devices much smaller than the cascodes since it is designed only for low on-resistance and it can have almost minimum size. Moreover, due to the removed cascode transistors, the area is reduced compared to the previous topology.

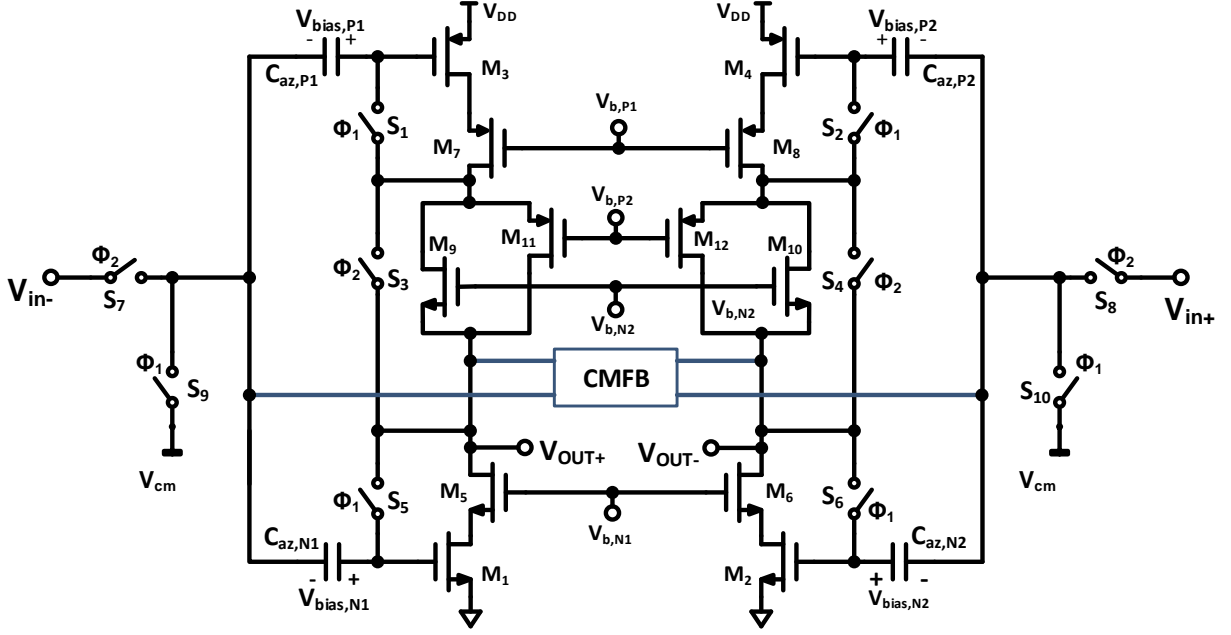


Figure 4.10. The proposed pseudo-differential inverter-based OTA

#### 4.5.3. Pseudo-differential integrator with common-mode feedback (CMFB)

In Fig. 4.11, a pseudo-differential implementation of the inverter-based SC integrator with a SC common-mode feedback (CMFB) circuit is shown. Ignoring the CMFB, during auto-zeroing phase  $\Phi_1$  of the inverter, the inputs are sampled to the capacitances  $C_{s,p-n}$ . Note that the integration capacitances  $C_{int,p-n}$  are disconnected from the virtual ground during this phase. During  $\Phi_2$ ,  $C_{int,p-n}$  are connected to the virtual ground and the charges sampled on sampling capacitances are transferred to integration capacitances yielding the integrator transfer function:

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_{s,p-n}}{C_{int,p-n}} \cdot \frac{z^{-1/2}}{1 - (1 - \beta)z^{-1}} \quad (32)$$

where  $\beta$  is the pole-error because of the switch parasitic capacitance  $C_p$  shown in Fig. 4.11:

$$\beta = \frac{C_p}{C_p + C_{int}} \quad (33)$$

Although reducing  $C_{cmfb}$  seems desirable to reduce amplifier loading, it also reduces  $A_{CMFB}$  which is for practical implementations already very low (1 - 2dB) [22]. So this CMFB circuit can only control output common-mode drift but cannot effectively cancel the effect of input common-mode voltages on the output common-mode voltage. If the input of the ADC has a large common-mode range, this



common-mode will be passed through all of the stages of the  $\Sigma\Delta$  modulator, and, as a result, the OTAs will drift from their desired operation point. Thus, the ADC's input common-mode range is limited.

#### 4. 6. CM range improvement

To improve the common-mode range of the ADC, an input common-mode cancellation technique is proposed for the sampling network by introducing switches  $S_{1-3}$  as shown in Fig. 4.12. During  $\Phi_1$  the differential inputs are applied to the input node of the sampling capacitances, but the nodes  $x_p$  and  $x_n$  are shorted through the switch  $S_1$ . Switches  $S_{2-3}$  are used to isolate the input from the virtual ground node during  $\Phi_1$ . Note that because of the parasitic capacitances  $C_{para,p-n}$  the nominal voltages on the nodes  $x_p$  and  $x_n$  are settled to  $V_{cm}$  in one clock cycle. As a result, the sampled voltages on the sampling capacitors are:

$$\begin{aligned} V_{s,p} &= (V_{in,p} - V_{cm}) \\ V_{s,n} &= (V_{in,n} - V_{cm}) \end{aligned} \quad (35)$$

Thus the common mode voltage of the input is effectively cancelled.

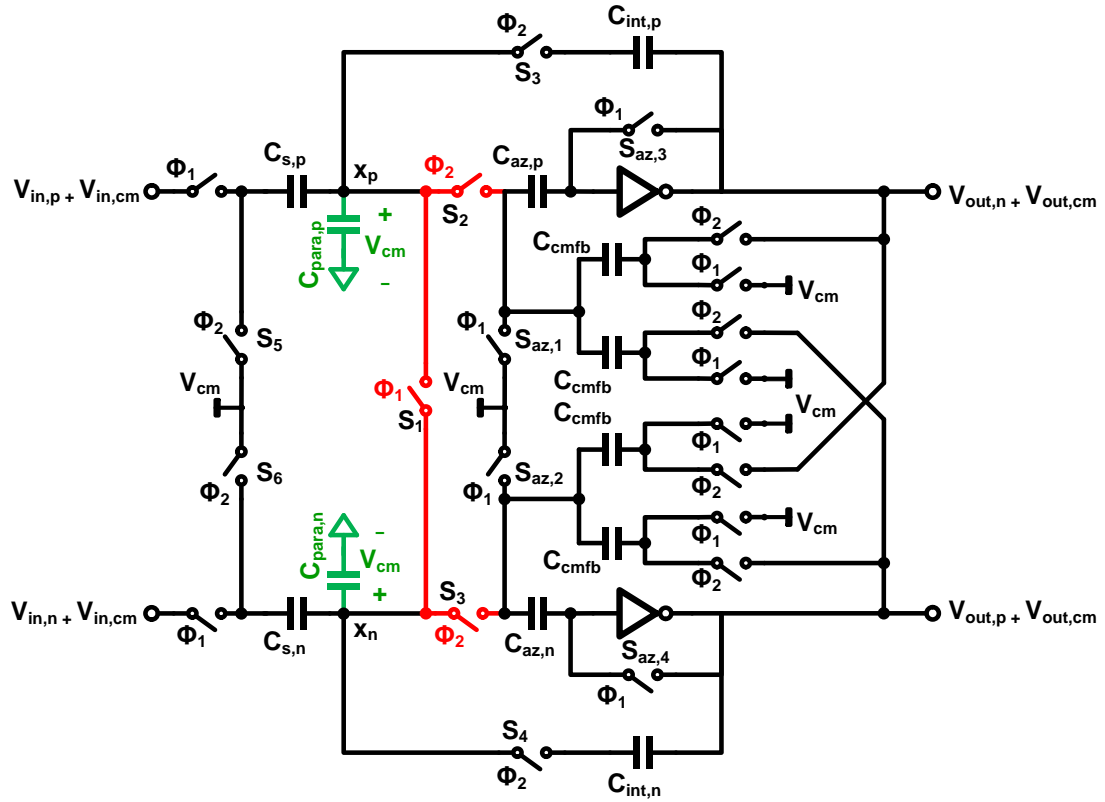


Figure 4.12. Input CM range improvement

During  $\Phi_2$  the integration is performed with respect to  $V_{cm}$ , the integrated differential voltage is:

$$\begin{aligned}
V_{int,diff} &= \frac{C_{int}}{C_s} \cdot ((V_{s,p} + V_{cm}) - (V_{in,n} + V_{cm})) \\
&= \frac{C_{int}}{C_s} \cdot V_{in,diff}
\end{aligned} \tag{36}$$

However, the CMRR of this sampling scheme is limited due to the relative mismatch ( $\delta_{C_s}$ ) of the sampling capacitances  $C_{S,p-n}$ :

$$CMRR = \delta_{C_s} \tag{37}$$

#### 4. 7. The 1<sup>st</sup> Integrator's OTA

The 1<sup>st</sup> integrator in the signal path is the most critical for noise, offset, gain and bandwidth aspects, because non-idealities of the succeeding integrators are attenuated by the gain of the first integrator. It is designed to provide the required performance when driving an integration capacitance of 3.3pF ( $C_{int,p-n}$  in Fig. 4.12). In order to keep the capacitive loading low, 280fF common-mode feedback capacitances ( $C_{cmfb}$ ) are used providing 1.4dB common-mode gain ( $A_{CC}$ ).

The simulated gain vs. frequency plot of the designed 1<sup>st</sup> OTA is given in Fig. 4.13 during the integration phase for 10pF capacitive load. From Fig. 4.13 it is seen that the auto-zeroed offset voltage is leaking through the switches' ( $S_{az1,2}$  in Fig. 4.12) off resistance. This leakage affects the transfer function at frequencies lower than 1 kHz, which indicates that the auto-zeroing frequency of the implemented OTA should be higher than this.

The worst-case performance of the OTA over process, voltage (1.6V-2V) and temperature (0°C - 85°C) corners are listed in Table 2.

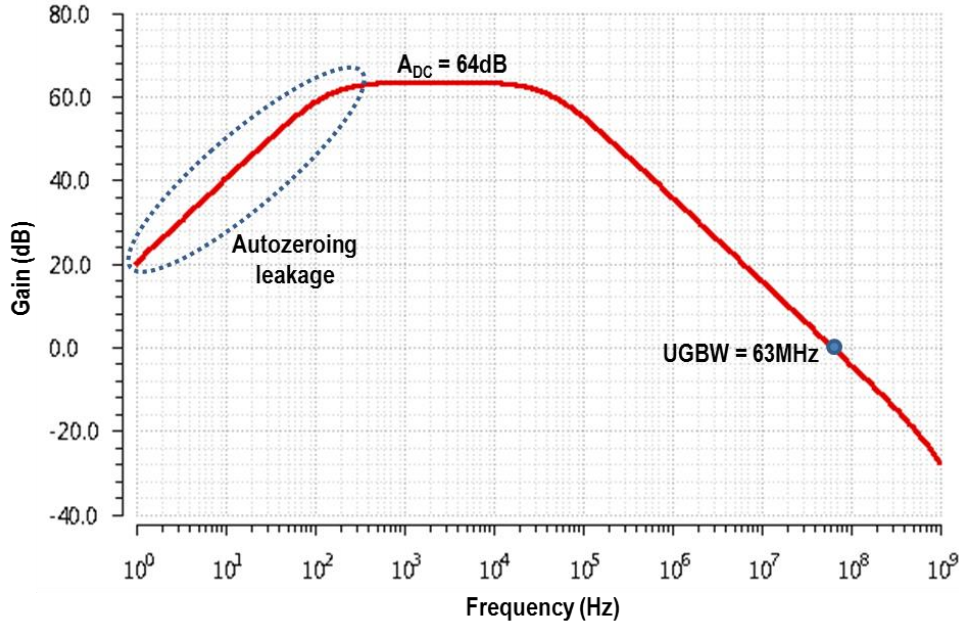


Figure 4.13. Gain vs frequency of the designed OTA for 10pF capacitive load in nominal corner

DC gain	Slew rate	GBW	Output swing	Power
---------	-----------	-----	--------------	-------

Target	60 dB	15 V/us	30 MHz	400 mV <sub>pp</sub>	-
Simulation	62 dB	20 V/us	52 MHz	800 mV <sub>pp</sub>	0.45mW

**Table 2. Targeted and simulated specifications of the 1<sup>st</sup> OTA**

#### 4.7.1. Noise and offset

As mentioned before, the input referred noise of the ADC is dominated by the sampled thermal noise ( $kT/C$ ) and the first OTA's noise. In order to suppress  $1/f$  noise together with the input referred offset of the first OTA, auto-zeroing is used. However, auto-zeroing increases baseband white noise since the whole noise bandwidth is under-sampled [24]. So, the white noise power increases to  $kT/C_{az}$  just like the input sampling network's noise. Thus, the auto-zeroing capacitor should be sized for the required noise level. For this reason, the auto-zeroing capacitors ( $C_{az,n1,2-p1,2}$  in Fig. 4.10) are 1.65pF each.

The simulated input referred noise power spectrum is shown in Fig. 4.14 which includes the first OTA's noise and the  $kT/C$  noise of the sampling network. The baseband noise power spectral density is  $33\text{nV}/\sqrt{\text{Hz}}$ . The presence of  $1/f$  noise increases this to  $49\text{nV}/\sqrt{\text{Hz}}$  at 1Hz. The total integrated noise in 20Hz-20kHz bandwidth is  $4.1\mu\text{V}_{\text{rms}}$  which corresponds to 109.5dB SNR for a 3.5V<sub>pp</sub> full scale input.

The major contributor to the OTA's offset is the charge-injection mismatch of the auto-zeroing switches  $S_{az,1-2}$  on capacitors  $C_{az,p-n}$ . Because  $S_{az,1-2}$  opens before  $S_{az,3-4}$ , the charge injection of  $S_{az,3-4}$  has no effect on the charge of the auto-zeroing capacitances. The next largest offset contributor is the charge-injection mismatch of the auto-zeroing switches  $S_{az,1-2}$  on capacitors  $C_{az,p-n}$ . In order to find the expected offset, a 100-run Monte-Carlo simulation is run on each PVT corner, yielding  $\sigma_{\text{offset}} = 85\mu\text{V}$ .

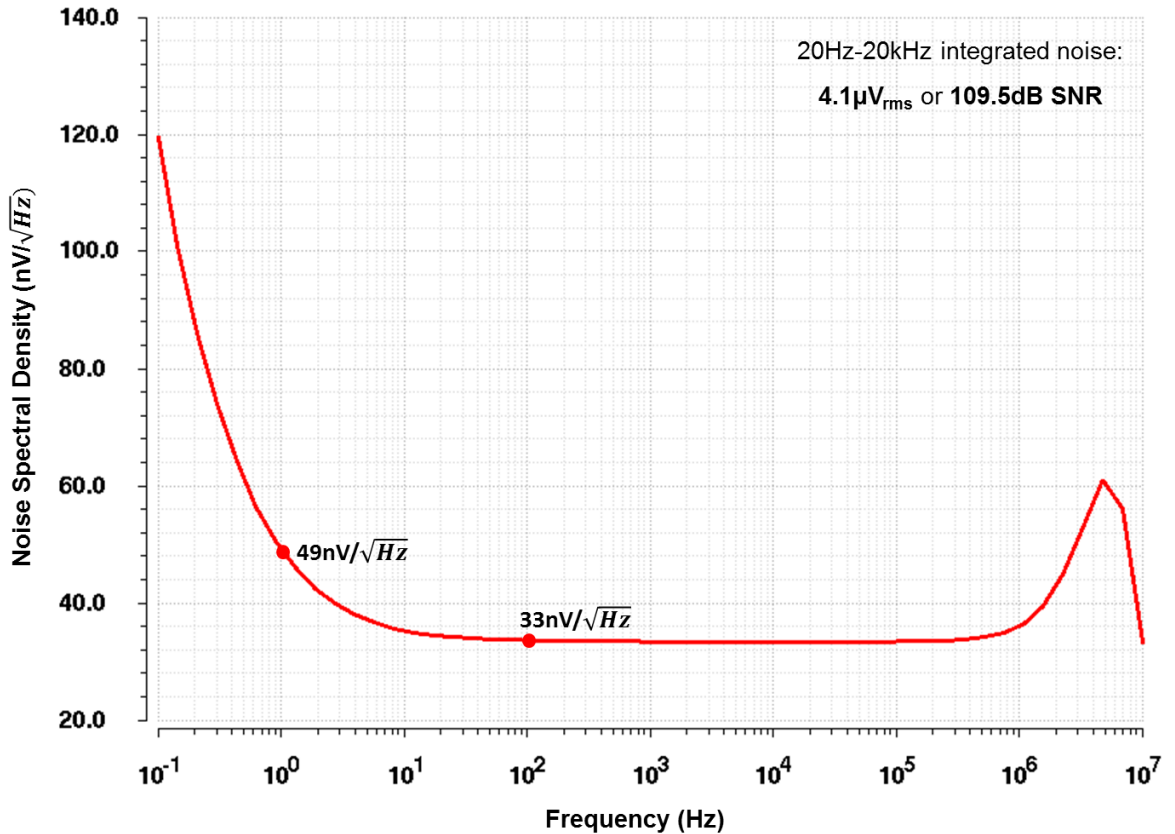


Figure 4.14. Simulated input referred noise

#### 4. 8. Scaling of the OTA powers

Since the errors introduced after the first integrator are attenuated by its gain, the performance requirements of the 2<sup>nd</sup> and the 3<sup>rd</sup> integrators are relaxed. For that reason, a lower power OTA drawing 50 $\mu$ A was designed for these integrators. It provides a minimum 46dB gain and 25MHz unity-gain bandwidth across all process, voltage and temperature (PVT) corners.

#### 4. 9. Bias generator circuit

The circuit used to generate constant transconductance ( $g_m$ ) bias voltages over temperature is shown in Fig. 4.15 [25]. Ideally, the temperature coefficient of the resistor  $R_1$  should be zero. Because it has the lowest temperature coefficient available in the chosen process, an n-doped poly-silicon resistor is used. A start-up circuit ( $M_{s,1-4}$ ) is used which is only active during the start-up, and turns-off once a proper operation point is established. When  $V_{dd}$  is rising from zero to its nominal value,  $M_{s3}$  and  $M_{s1}$  rises the gate voltage of  $M_{s4}$  which eventually sinks current and turns-on  $M_3$ . Because of the positive feed-back, the bias generation loop ( $M_{1-4}$ ) starts and stabilizes on a desired point quickly. When the gate voltage of  $M_{s2}$  rises the start-up circuit 'turns-off'. In that mode, it only draws a very low leakage current from the power supply.

The bias voltages  $V_{b,p1-2}$  and  $V_{b,n1-2}$  are obtained by biasing diode connected transistors with a copy of the bias current. As discussed before, they should have low impedance in order to regulate kick-back charges due to the switching behavior of the OTAs. Thus, the currents of each branch has been chosen to adjust the output impedance of the corresponding diode-connected transistor for their capacitive loads. Total current consumption of the bias generator circuit is 60 $\mu$ A.

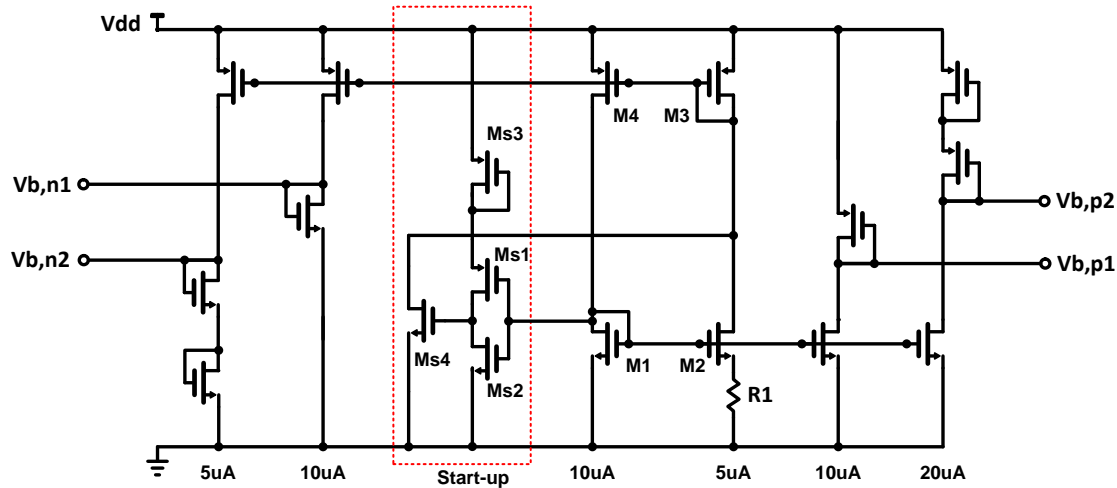


Figure 4.15. The bias generator circuit

#### 4. 10. The comparator

The comparators used in the  $\Sigma\Delta$  modulator and the SAR ADC are exactly the same, and consist of a preamplifier and a clocked SR-latch. The schematic of the comparator is shown in Fig. 4.16. It works as follows. When the clock (CLK) is low, the dynamic latch ( $M_{6-15}$ ) is reset through switches  $M_{6,7,15}$ . The

preamplifier ( $M_{1-5}$ ) amplifies the signal with a moderate gain of  $\sim 12\text{dB}$ . The amplified signal is mirrored to the dynamic latch by  $M_{4,5,10,11}$  to generate an imbalanced current on two branches of the dynamic latch ( $M_{6-15}$ ). However, this is only possible with the rising edge of the clock (CLK) when  $M_{6,7,15}$  turn-off and  $M_{8,9}$  turn-on to establish the latch with cross connected inverters ( $M_{12-15}$ ). Because of the imbalanced current, the positive feedback of the latch drives two outputs of the comparator to two different rails (Vdd or ground) in a short amount of time, generating CMOS logic output levels.

In the previous chapter, it was found that the standard deviation of the error due to the offset should be lower than 1.4% of the full-scale for the SAR ADC's comparator. For the technology used, the full scale input is 3.6V. So, the offset error of the comparator should be:

$$V_{ofst,max} < 3\sigma_{ofst} \cdot V_{FS}$$

$$V_{ofst,max} < 152\text{mV} \quad (38)$$

The input referred offset is 3.5mV ( $1\sigma$ ) for the designed comparator which satisfies the requirement. Another criteria for the comparator is the speed. It should be faster than the half period of the clock, which is 50ns (for 10MHz clock). Although the decision time can be quite high for very low signals due to meta-stability, for an input of 1mV the comparator's maximum decision time is simulated as 4ns on all PVT corners. The comparator draws only 6 $\mu\text{A}$  from the 1.8V supply.

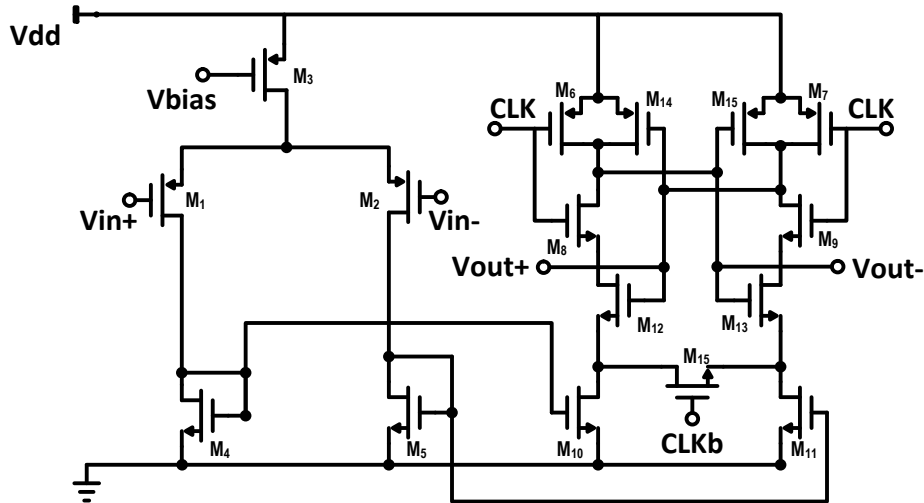


Figure 4.16. The comparator

#### 4. 11. The SAR ADC

A single ended schematic of the SAR ADC is given in Fig. 4.17. It samples the input signal to the capacitor DAC array every 5 clock cycles using phase  $\Phi_{\text{SAR}}$ . During  $\Phi_2$ , the DAC units are connected to the positive or the negative references,  $V_{\text{ref},p}$  and  $V_{\text{ref},n}$  respectively. The comparator, which is the same as the one described before, is triggered by the clock  $\Phi_{\text{CMP}}$  before the end of the phase  $\Phi_2$ . The SAR logic then processes the result to determine the next DAC output before the next  $\Phi_2$  rising edge.

The capacitive DAC is implemented with metal fringe capacitors (metal<sub>1</sub> to metal<sub>4</sub>). The unit capacitor  $C$  is 11fF resulting in a total DAC capacitance of 352fF. The analog power consumption is 11 $\mu\text{W}$  (only the comparator power).

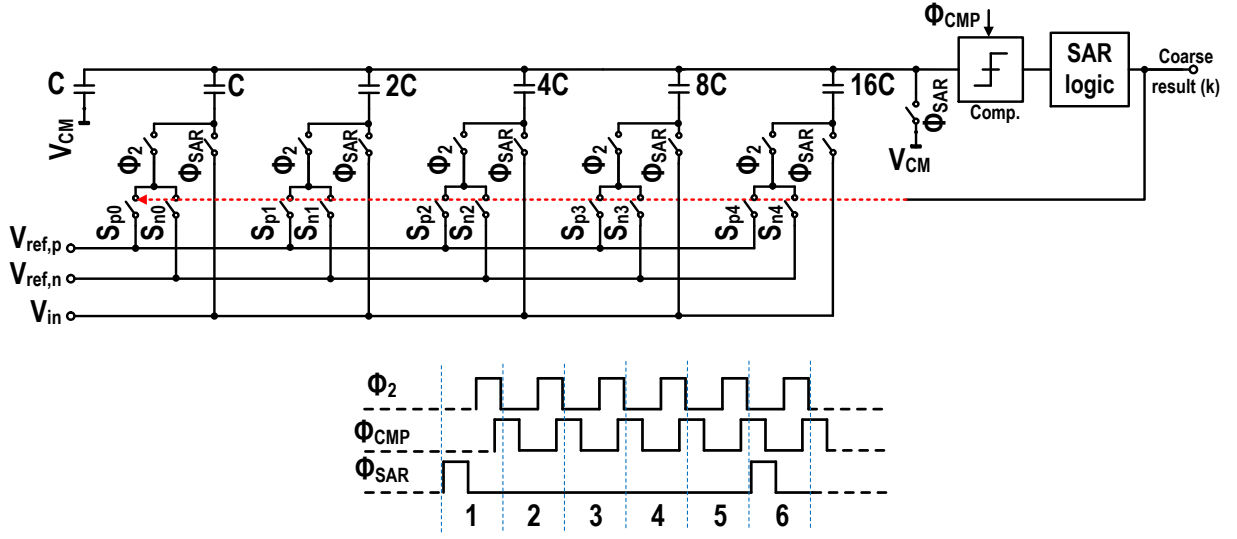


Figure 4.17. The SAR ADC

## 4.12. Digital circuits

The digital circuits on-chip includes a non-overlapping clock generator, SAR logic and two DEM algorithms: barrel-shift DEM and DWA.

### 4.12.1. Clock generator

The circuit used to generate two non-overlapping clocks ( $\Phi_1$  and  $\Phi_2$  and their complements  $\Phi'_1$  and  $\Phi'_2$ ) with their 3 slightly different phase-delayed versions (early, normal, and delayed) and a large delayed comparator clock ( $\Phi_{\text{comparator}}$ ) is shown in Fig. 4.18. Note that complementary clocks are not shown in the representative timing diagram. The  $\Phi_{\text{comparator}}$  should be in the middle of the phase  $\Phi_2$ , which requires a large delay. In order to achieve that, a standard RC delay cell is used (Fig. 4.18). The nominal delay of RC delay cell is 5ns.

Monte-Carlo simulation is performed on all PVT corners in order to ensure the correct clocking in any condition. Since the input signal is sampled by the clocks  $\Phi_{1,\text{early}}$  and  $\Phi'_{1,\text{early}}$ , their jitter performance is important. Clock jitter causes a non-uniform sampling which gives rise to a sampling error. Assuming a clock jitter with a standard deviation of  $\sigma_{jit}$ , the in-band error due to the jitter is [1]:

$$\varepsilon_{\Delta t} = \frac{V_{ref}^2}{8} \cdot \frac{2\pi \cdot f_s \cdot \sigma_{jit}}{OSR} \quad (39)$$

The SNR due to the jitter is:

$$SNR = 20 \cdot \log_{10} \left( \frac{OSR}{2\pi \cdot f_s \cdot \sigma_{jit}} \right) \quad (40)$$

The maximum tolerable sampling jitter for 10MHz clock and 117dB SNR is calculated as **5.6ps**. As seen from Fig. 4.18 these two clock signals are derived from the external clock after a NAND gate and two inverters. A transient noise analysis is performed to check these blocks' jitter contribution. Results are

shown in Fig. 4.19 as histograms. The clock  $\Phi_{1,\text{early}}$  has an added jitter of  $\sigma_{\text{jit},1e} = 106\text{fs}$  and  $\Phi_{1',\text{early}}$  has  $\sigma_{\text{jit},1eb} = 121\text{fs}$  on top of an ideal clock. These results show that, in order to be not effected by the clock jitter, the external clock  $\text{CLK}_{\text{in}}$  should have a jitter performance better than **5.6ps**.

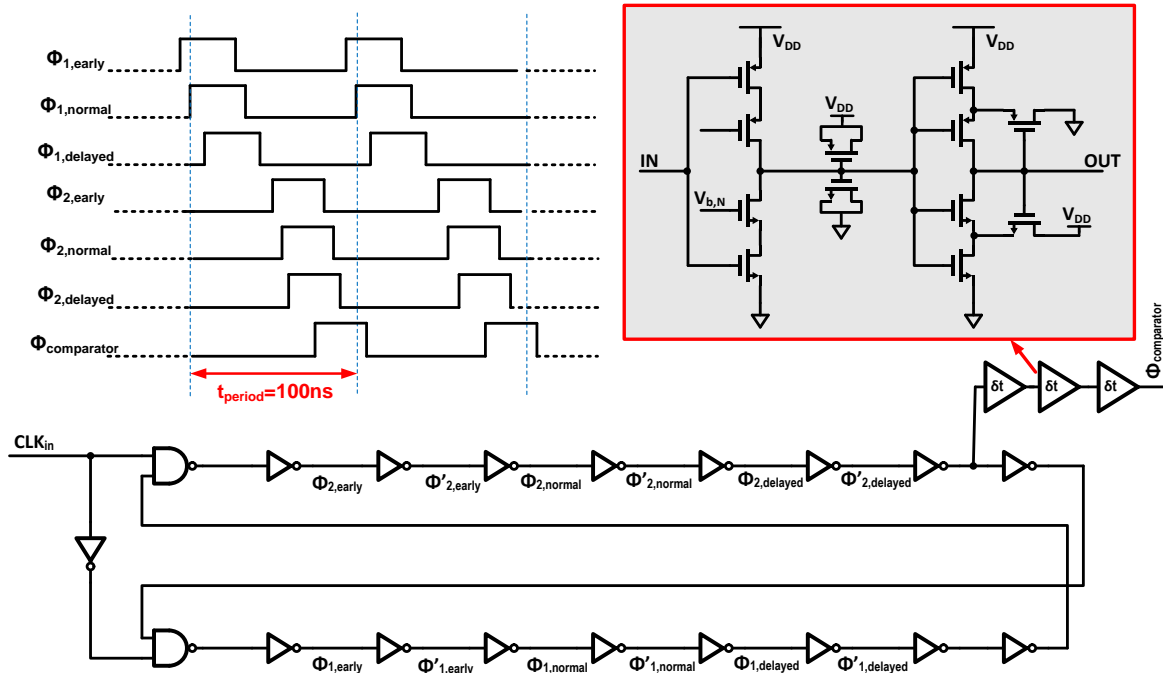


Figure 4.18. The non-overlapping clock generator circuit

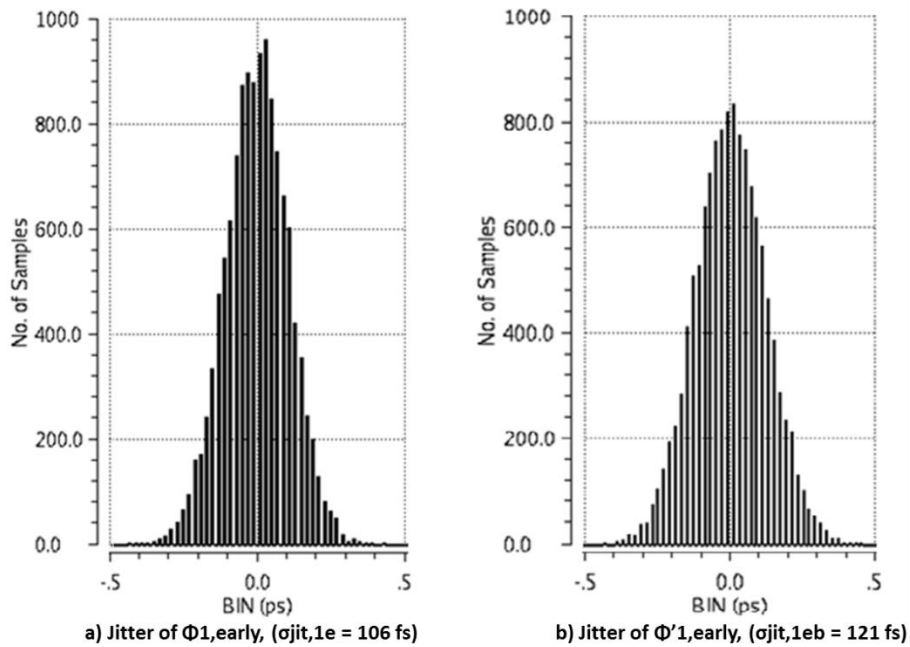


Figure 4.19. Jitter performance of the sampling clocks

#### 4.12.2. SAR logic

SAR logic is synthesized on-chip by using Cadence RTL compiler. A flow-chart of the algorithm is given in Fig. 4.20. It gives two 5-bit results at the end of 5-cycle binary search;  $k-2$  and  $k+3$  for low and high references of the DAC respectively. The outputs are saved on the registers to be kept for the next 5-cycles.

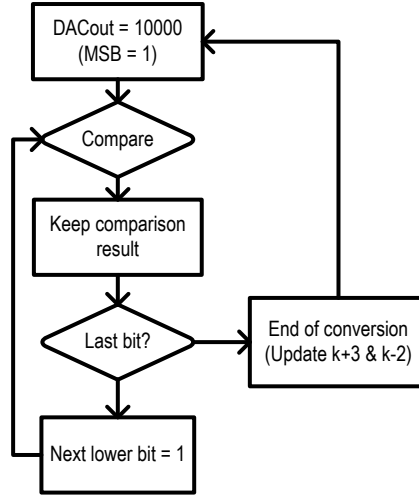


Figure 4.20. SAR logic flow-chart

#### 4.12.3. DEM

There are two different DEM algorithms implemented on-chip: barrel-shift DEM and DWA. An RTL code including both algorithms is written in Verilog and synthesized by using Cadence RTL compiler. It is possible to not use any DEM algorithm in order to measure the nonlinearity without such techniques. An external logic mode is implemented to have a direct access to the DAC by 31 pins in order to have a possibility to try different DEM algorithms.

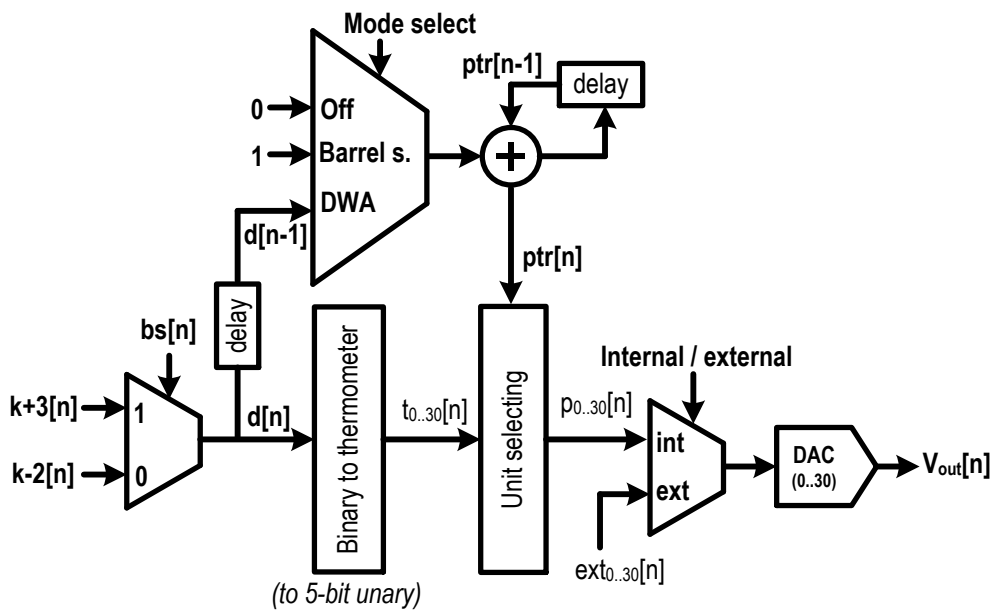


Figure 4.21. DEM logic block diagram



A block diagram of the DEM logic is shown in Fig. 4.21. The inputs of the DEM block are the registers keeping  $k-2[n]$  and  $k+3[n]$  for low and high references of the DAC respectively from the previous SAR ADC conversion result. Depending on the bit-stream output of the  $\Sigma\Delta$  modulator  $bs[n]$ , the DAC's input word  $d[n]$  is determined. This 5-bit binary code is then converted to thermometric (unary) code  $t_{0-31}[n]$ . Unit selecting logic gets the thermometric code as input and determines the active DAC units depending on the pointer  $ptr[n]$  as shown in Fig. 4.22.

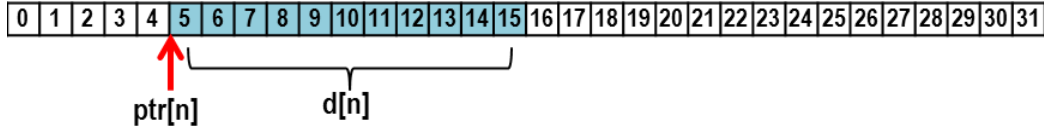


Figure 4.22. Unit selecting

A 3-bit shift-register is used to program the ADC for different DEM modes (DEM off, barrel-shifter, and DWA). For all DEM algorithms the same 5-bit pointer register  $ptr[n]$  is used to determine the first active unit in the array. If the ADC is programmed for “DEM off” mode, the pointer does not change, i.e. always the same unit elements are used for the same DAC input code  $d[n]$ . For the “barrel-shifter” mode,  $ptr[n]$  is increased by 1 on each conversion cycle. Thus, the first unit element is shifted by 1 every time. The “DWA” mode uses the previous output of the DAC, i.e.  $d[n-1]$ , to shift the pointer.

#### 4. 13. Simulation results

A transient simulation performed on transistor level analog circuits and the clock generator, and behavioral digital circuits. The output spectrum of the zoom ADC on nominal process corner with 1.8V ideal power supply at 27°C temperature before decimation for a 15kHz sinusoidal input with 3.5V peak-to-peak amplitude is shown in Fig. 4.23. For this simulation, external source impedance is chosen as 10Ω. SQNR is calculated as 119.5dB. Note that this simulation does not include thermal noise or mismatch. Thus, the overall SNR is expected to be limited by thermal noise to 109.5dB. The total power consumption is 1.37mW (including all analog circuits and the clock generator). The digital power is estimated as 0.5mW by the synthesizer, resulting 1.87mW of total power consumption. The expected  $FoM_s$  is 180.3dB.

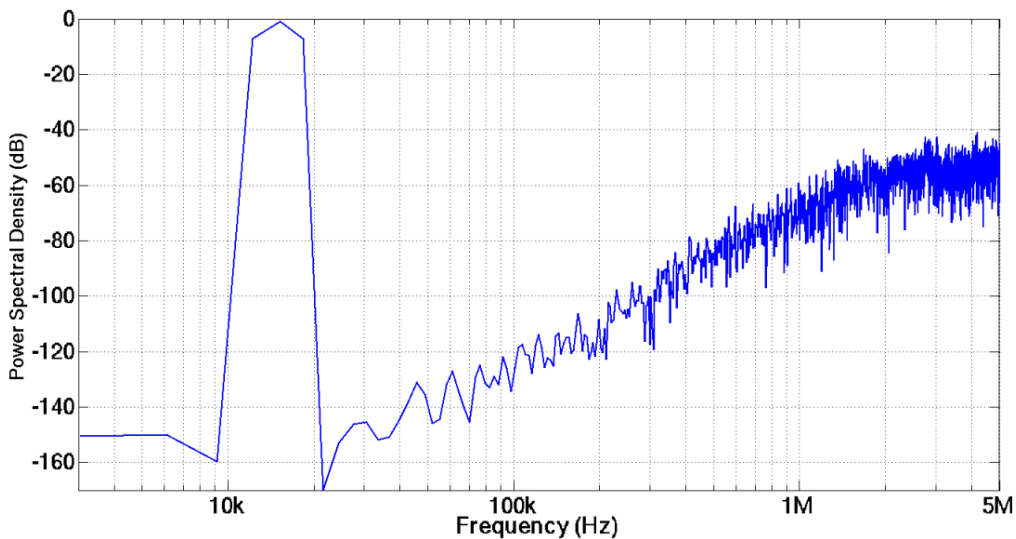


Figure 4.23. Transistor level simulation result of the designed zoom ADC

#### 4. 14. Layout

The layout of the active area of the designed chip shown in Fig. 4.24. It only occupies 0.16mm<sup>2</sup> die area. The definitions of the numbered sub-blocks are given in Table 3.

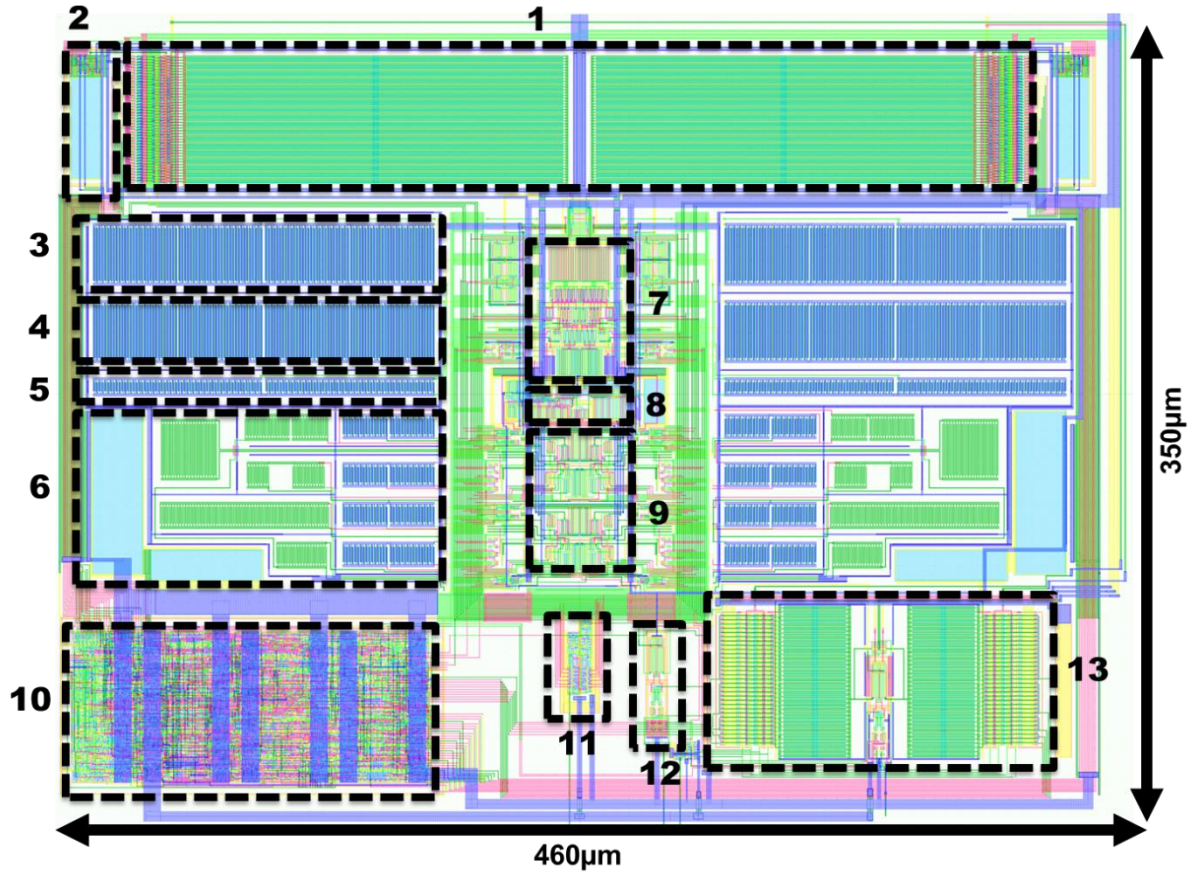


Figure 4.24. The layout of the designed zoom ADC

Number	Description	Area ( $\mu\text{m}^2$ )	Area (%)
1	Capacitive DAC	20235	13
2	Bootstrapped clock generator	1792	1
3	Auto-zeroing capacitances of the first OTA	8640	5
4	Integration capacitances of the first integrator	8640	5
5	CMFB capacitors of the first OTA	3456	2
6	2 <sup>nd</sup> & 3 <sup>rd</sup> integrators' capacitors and feed-forward coefficient capacitors	20160	13
7	1 <sup>st</sup> OTA	2700	2
8	biasing circuit	1080	1
9	2 <sup>nd</sup> and the 3 <sup>rd</sup> OTAs	2700	2
10	Synthesized digitals	10800	7
11	Non-overlapping clock and phase generator.	320	-
12	Comparator of the $\Sigma\Delta$ modulator.	360	-
13	SAR ADC.	9000	6

Table 3. Descriptions of the blocks in the layout

The layout plan is done considering symmetry as a matter of the utmost importance. The sampling capacitances (the capacitive DACs) are placed at the very front of the signal path. Then the 1<sup>st</sup> integrator laid-out by placing the 1<sup>st</sup> OTA in the center of the line of symmetry, and the switches and the capacitors on the both sides of the OTA. All of the capacitors are shielded with so-called “side-walls” consisting of stack of metals and vias from substrate to metal-5. These shields are connected to the analog ground in a star-connection fashion.

Between 1<sup>st</sup> and the 2<sup>nd</sup> OTA, the biasing circuit is placed in order to keep the interconnections short for low resistance, thus a low voltage-drop. The 2<sup>nd</sup> and the 3<sup>rd</sup> integrators are laid-out with the same considerations as of the 1<sup>st</sup>.

The SAR ADC is placed in a considerably distant place than the front-end in order to reduce any signal depended kick-back effects which might cause quantization noise fold-back. The SAR ADC and the  $\Sigma\Delta$  modulator shares the same positive reference voltage.

The non-overlapping clock and phase generator circuit is placed in the center of the line of symmetry since the equality of the delays for the same clocks, e.g. clock signals of the auto-zeroing switches of the positive and the negative inverter counterparts of the OTA, are quite important for switched-capacitor circuits. Thus, any clock has the same delay with its counterparts if there is any. All clock signals are shielded with a metal layer below which is connected to the digital ground. The comparator is placed just beside the clock generator.

The synthesized digitals are kept away from the input of the  $\Sigma\Delta$  modulator, and the SAR ADC. A 20 $\mu\text{m}$  distance between the 3<sup>rd</sup> integrator's capacitances and the digitals is used for shielding, again from substrate to metal-5. The digital circuits generate the DACs' input code, which are routed around the core area in a shielded “box”. The signals are routed on metal-2, metal-3 and metal-4 layers, and metal-1 and metal-5 are used for the grounded shield. These two shield planes are connected through stacked vias around the signal lines, forming a closed-box as shown in Fig. 4.25 with a sample cross-section. These shielding lines are connected to the digital ground directly at the pad, forming a star-ground connection.

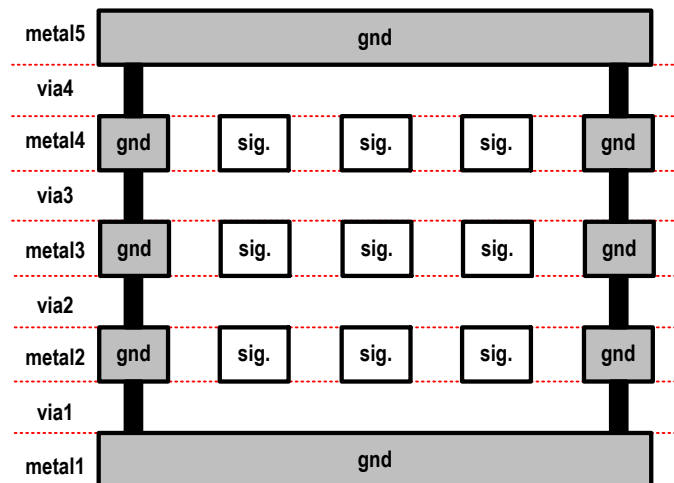
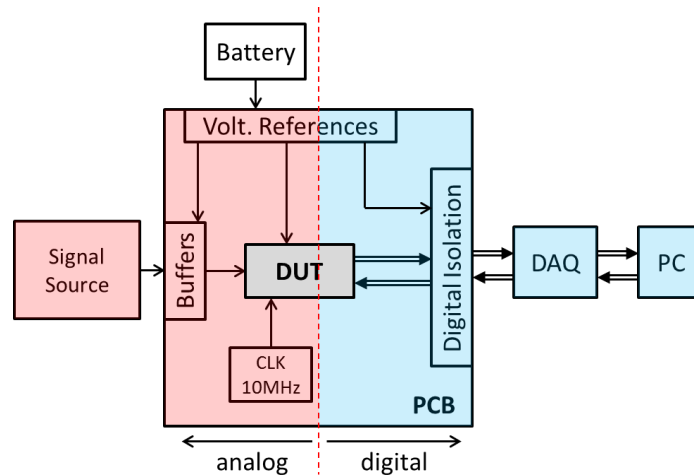


Figure 4.25. Cross-section of the shielded digital signal lines

## 5. Measurement Setup and Results

### 5.1. Measurement setup

The measurement setup should be carefully designed in order to achieve targeted low-level noise and linearity in this work ( $\text{SNR} \ \& \ \text{SNDR} > 110\text{dB}$ ). A block diagram of the measurement setup is shown in Fig. 5.1. A test PCB is designed employing the prototype chip and the necessary discrete components such as voltage references, analog signal buffers, an oscillator for clock generation, digital isolators and decoupling capacitors. A battery is chosen as power source in order to minimize power source noise and interference. A low-noise high linearity signal generator is used as analog signal source. The isolated digital inputs and outputs of the PCB are connected to a PC via a high speed digital data acquisition (DAQ) device.



**Figure 5.1. Block diagram of the measurement setup**

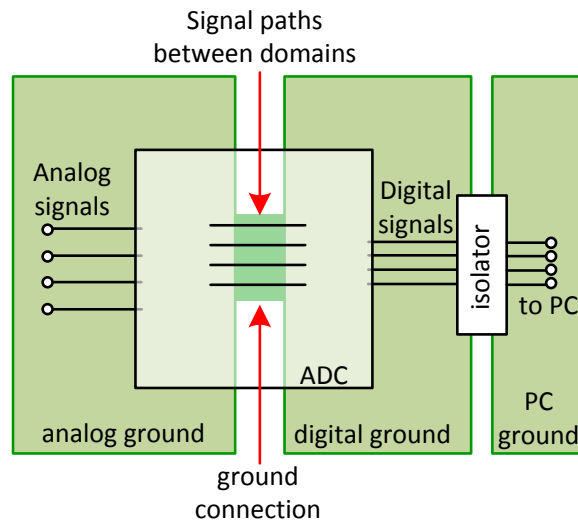
All of the elements shown are critical for the measurement setup performance. The noise of the signal source and the signal buffers should be considerably lower than the ADC's input referred noise, and the linearity of the signal applied to the ADC should be better than the desired level of measurement. The PCB should be carefully laid-out in order to reduce interference and coupling. These design aspects will be discussed in the following sections.

#### 5.1.1. PCB ground separation

Any current returns to its source, via the lowest impedance path. Long current return paths are source of magnetic coupling [26]. Usually, a ground plane parallel to the signal lines needed to shorten the physical length of the current return path, thus reducing coupling.

The ADC under test is a mixed-signal integrated circuit with a low noise analog input and rather high speed digital signals on the back-end. Separate analog and digital power and ground domains are necessary to minimize coupling between sensitive analog part and the digitals. Thus, the PCB is divided into two power domains by placing the test chip as the center of the domain separation. For a mixed-signal PCB, connecting analog and digital grounds without increasing current return paths is also one of the most critical points of the design [26].

The analog and the digital grounds are connected just under the chip, allowing any signals between domains to have the shortest return path as shown in Fig. 5.2. Any coupling possibility is minimized because the PCB has no digital or analog signal crossing the separation line. Moreover, all digital signal lines are designed as  $50\Omega$  transmission lines with termination. The PC ground is isolated from the PCB ground via a digital isolator, as shown in Fig. 5.2.



**Figure 5.2. Ground domains of the designed PCB**

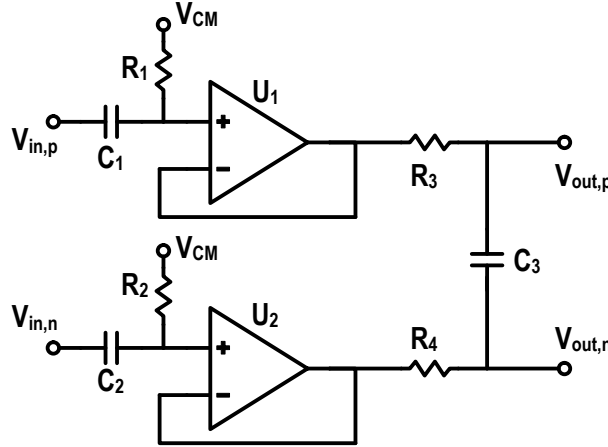
### 5.1.2.Noise

The ADC under test has an input referred thermal noise of  $4.1\mu\text{V-rms}$  in 20Hz-20kHz bandwidth. Thus, the signal source and the signal buffers shown in Fig. 5.1 should have lower noise power in this bandwidth. A signal source, Rohde & Schwarz UPD, with a  $2\mu\text{V-rms}$  nominal noise in 20Hz-20kHz bandwidth is used as the signal generator. Thus, the maximum achievable SNR is limited by the ADC.

Since the signal source should drive a switched-capacitor sample and hold circuit, a buffer is usually desired for high resolution ADCs. A buffer topology shown in Fig. 5.2 is used. The buffer OPAMPs' noise contributes to total input referred noise of the measurement system. Thus, a very low noise OPAMP (LME49990) is used. The noise spectral density is specified as  $1.4\text{nV}/\sqrt{\text{Hz}}$  at 10Hz, and  $0.9\text{nV}/\sqrt{\text{Hz}}$  above resulting  $127\text{nV-rms}$  integrated noise in 20Hz-20kHz bandwidth. Hence, the buffer noise is negligible compared to the signal generator's and the ADC's input referred noise.

The buffer inputs are AC coupled, in order to get rid of low frequency noise and common-mode voltage drift of the signal source. The input common-mode voltage is defined with a precision voltage source on the PCB ( $V_{\text{CM}}$ ). The pole frequency of the AC coupling high-pass filter is 8Hz. Unity gain buffer OPAMPs are used to drive an RC low-pass filter ( $R_{3,4}$  and  $C_3$ ). The filter helps to reduce the high

frequency noise of the signal source and the buffer OPAMPs. Choosing a large  $C_3$  is preferable since it acts as a charge-reserve for the sample and hold circuit of the ADC. It is chosen as 10nF. The pole frequency of the low-pass filter is chosen as 30 kHz, since this helps the SAR ADC's high-frequency tracking problem by attenuating high frequency signals. It is possible to by-pass the AC coupling, the buffers, and the RC filter via jumpers on the PCB.



**Figure 5.3. Input signal buffer circuit**

Voltage reference of the ADC has a direct effect on the maximum achievable SNR. For this reason, the noise of the reference should be much lower than the ADC's input referred noise. A low-noise 2V voltage reference (LTC6655) is used for this purpose. Noise-bandwidth of the reference is reduced to less than 10Hz with passive filtering, resulting a 160nV-rms noise. Hence, the voltage reference noise is negligible.

### 5.1.3. Linearity

For the proposed measurement setup, the signal source is capable of >110dB THD for the input range of the ADC (3.5 V-pp). The buffer OPAMPs are also highly linear, providing 130dB THD for the used signal range. However, even the passive elements might limit the linearity of the system. Thus, the passive components are chosen for low dependence of voltage, frequency and temperature.

### 5.1.4. Clock jitter

The sampling clock's jitter might limit the maximum achievable SNR. For this work, maximum 5.6ps-rms period jitter might be tolerated as found before. For this reason, a Si501 MEMS oscillator with 1.6ps-rms max period jitter is used to generate 10MHz sampling clock. 50Ω series termination is used in order to avoid reflection.

### 5.1.5. Data acquisition and post-processing

Digital outputs of the ADC consists of SAR ADC's comparator output, sampling flag of the SAR ADC (which becomes active once in each 5-cycles), bit-stream output of  $\Sigma\Delta$  modulator and a clock synchronized to all these three outputs. The digital inputs of the ADC are reset, shift register data input and shift register clock input. These signals should be driven or acquired by a PC, in order to simplify the



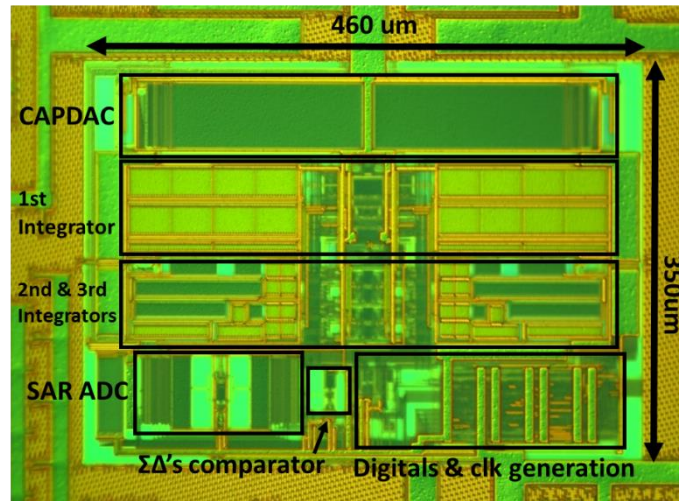
controls and post-processing. For this reason, a high speed data acquisition card (DAQ) is employed on the PC. However, this requires to connect the ground of the PCB to the PC's ground which might be noisy. In order to isolate the grounds, inductive digital isolators (Si8660 and Si8663) are used between the PCB and the DAQ which supports up to 150 Mbps, satisfying the speed requirement of maximum 10Mbps output of the ADC.

## 5. 2. Measurement results

### 5.2.1. Power, offset, CMRR, PSRR

The prototype chip has been fabricated in SSMC 0.16 $\mu$ m 1P5M CMOS process. Fig. 5.4 shows the die micrograph. It draws 1.1mA from 1.8V supply resulting 2.07mW power consumption. The analog part consumes 1.1mW (55%) while all the digitals including the clock generator consume 1mW (45%).

Its CMRR is 63dB for DC signals and stays greater than 60dB up to 100kHz, which is limited by the sampling and integration capacitance mismatches. PSRR is measured as 84dB at DC and 50Hz, which shows the effectiveness of dynamic-biasing technique. The input referred offset of the ADC is maximum 0.5mV for 10 samples. The flicker noise corner is below 2Hz.



**Figure 5.4. The micrograph of the prototype chip**

Fig. 5.5 shows SNR and SNDR vs input amplitude. Maximum SNR is measured 97dB at 0dBFS input (3.5V-pp) and maximum SNDR is 92dB at -2dBFS input. With DWA off, the SNDR is 72dB and is limited by DAC mismatch. DWA and barrel-shifter DEM did not show a difference in SNDR. Dynamic range of the ADC is 102dB. Sample output spectra of the ADC for zero input and -2dBFS at 1kHz input are shown in Fig. 5.6. Note that the “fur” on the noise-shaped region when a large signal is present is due to the DWA. There is a strong (-30dB) tone at 2MHz, i.e.  $F_s/5$ , which is due to the sampling of the SAR ADC occurring at that frequency.

Fig. 5.7 shows full-scale input signal frequency vs. integrated noise in 20kHz bandwidth with and without an first order RC 30kHz LPF at the ADC's input. Due to the SAR ADC's inability to track full-scale signals faster than 24kHz, the  $\Sigma\Delta$  modulator cannot work properly. Thus, the in-band SNR settles to 40dB level. With a simple RC filter with a pole frequency of 30kHz at the input, this can be

mitigated considerably. The resulting FoM<sub>s</sub> is 172dB, which is on par with state-of-the-art high-resolution (>15b) ADCs with similar bandwidth while the area is more than 2x smaller as Table 4 shows.

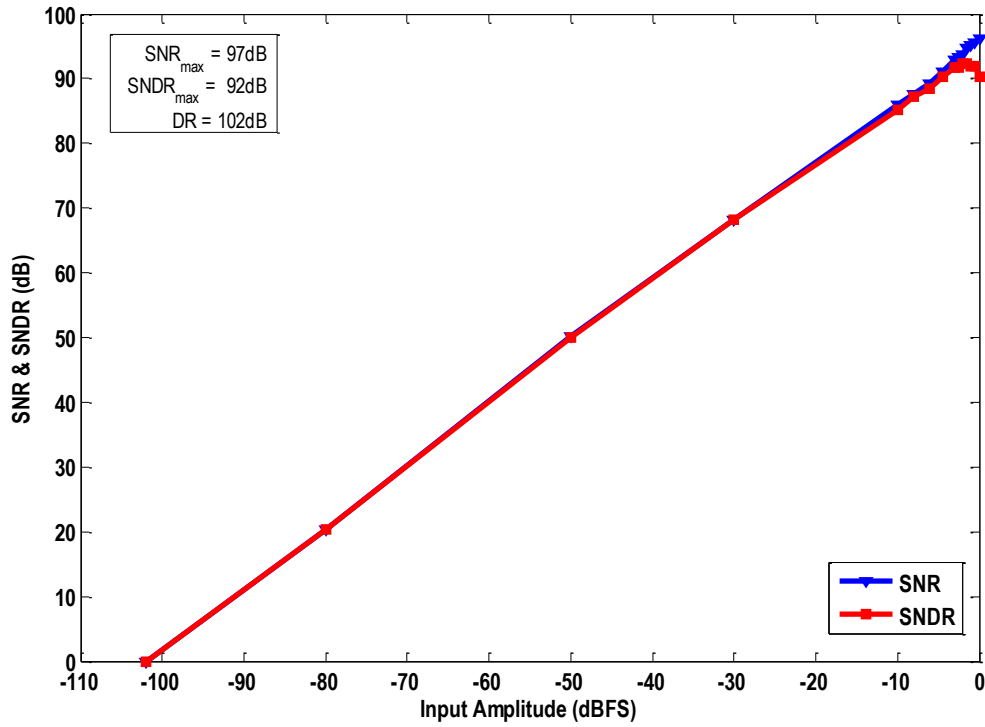


Figure 5.5. SNR & SNDR vs input amplitude

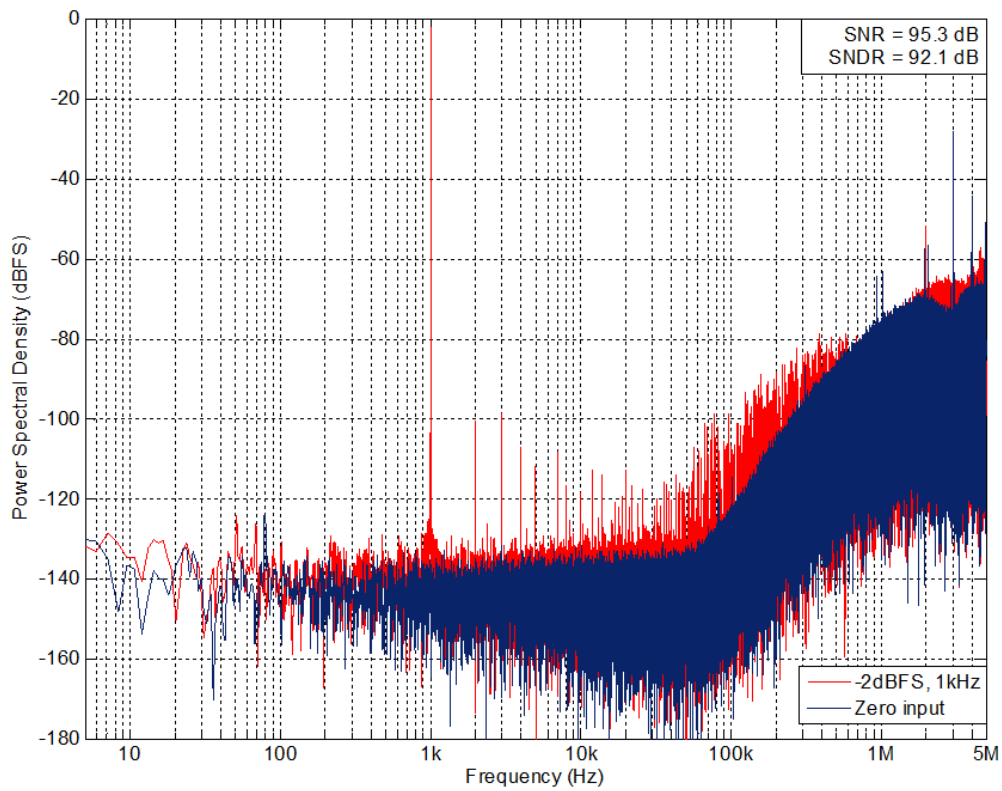
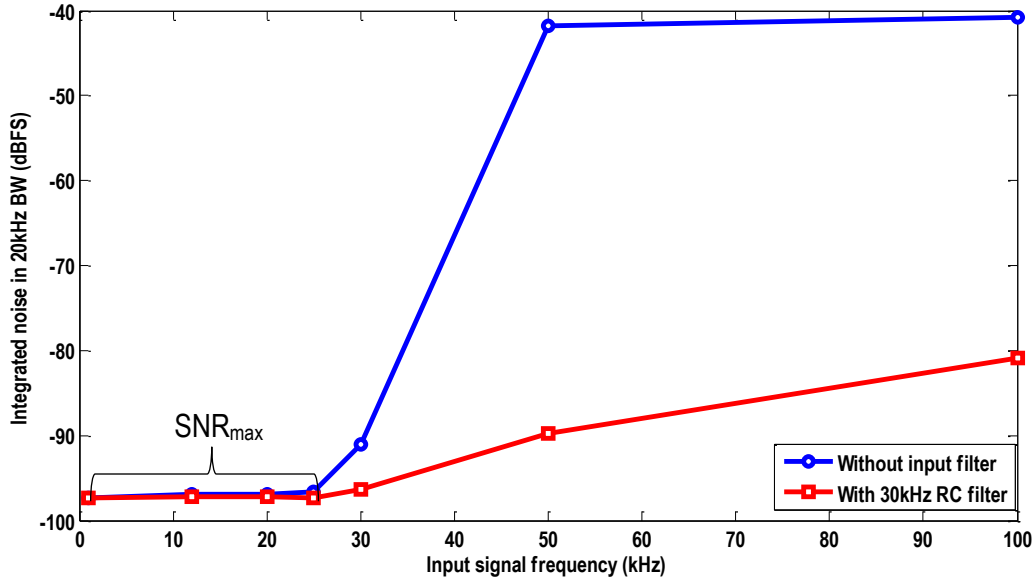


Figure 5.6. Measured output spectrum of the zoom-ADC (SAR-ADC output combined with  $\Sigma\Delta$ -ADC output before decimation; Hanning window;  $2^{23}$  samples).





**Figure 5.7. Full-scale input signal frequency vs. integrated noise in 20kHz BW (dBFS) with and without an first order RC 30kHz LPF at the ADC's input.**

	Unit	This work	[21]	[27]	[28]	[29]	[30]	[31]	[32]
Year	-	2014	2009	2008	2005	2004	2014	2012	2011
Tech.	$\mu\text{m}$	0.16	0.18	0.35	0.35	0.35	0.18	0.18	0.065
Die Area	$\text{mm}^2$	0.16	2.16	14.8 (2 ch.)	0.82	9.6	1.25	0.38	0.41
Supply voltage	V	1.8	0.7	5 (A) 2.5 (D)	-	5 (A) 1.8 (D)	1.8	5 (A) 1.8 (D)	1
Power	mW	2.07	0.87	165	18	150	0.28	1.1	0.371
Sampling frequency	MHz	10	5	6.144	5.12	6.144	6.144	2.5	3.072
Input range	$V_{pp}$	3.5	1.4	5.7	5.7	-	3.6	4.9	-
BW	kHz	20	25	20	20	20	24	20	24
Peak SNR	dB	97	100	-	106 <sup>†</sup>	-	99	99	96
Peak SNDR	dB	92	95	111	99	110	98	99	95
DR	dB	102	100	124 <sup>†</sup>	106 <sup>†</sup>	120 <sup>†</sup>	103	101	96
FOMs <sup>††</sup>	dB	172	175	175 <sup>†</sup>	166 <sup>†</sup>	171 <sup>†</sup>	182.3	173.6	174.5

<sup>†</sup> A-weighted, <sup>††</sup> FOMs=DR+10log(Signal bandwidth/Power)

**Table 4. Performance summary and benchmarking**

## 6. Conclusion and Future Work

### 6. 1. Conclusion

In this thesis, a zoom ADC for dynamic (audio) signals is proposed, system-level and transistor-level implementation details are discussed, and measurement results are provided. A reliable low-noise and low-distortion measurement setup is designed and used.

The implemented prototype's energy efficiency is on par with state-of-the-art ADCs with similar resolution and bandwidth. Thus, zoom ADC is promoted from being a "promising" concept to "proven" energy efficient architecture for high-resolution dynamic signals. Moreover, the prototype chip showed an unrepresented area advantage increasing the attractiveness of the zoom ADC.

### 6. 2. Future work

The prototype chip is designed for 110dB SNR and SNDR, and 180dB FoM<sub>s</sub>. Although simulations satisfied the expectations, the measurement results did not. The source of the lost SNR should be investigated on measurement and simulation further. The linearity after DEM is also, not on the level with the expectations. The source of nonlinearity should be tracked.

The effect of SAR ADC's sampling frequency tone on the spectrum should be investigated. This is a suspect of quantization noise fold-back to the baseband. This requires layout simulation in time domain, which is quite time consuming. Thus, new simulation strategies might be required.

Digital power consumption of the designed zoom ADC is 45% of the total power. This should be improved, either with a more careful digital design or with the investigation of an energy-efficient DEM algorithm for zoom ADC.



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