Graphene-based microfabricated platform technologies for multimodal neural interfaces

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GRAPHENE-BASED MICROFABRICATED PLATFORM TECHNOLOGIES FOR MULTIMODAL NEURAL INTERFACES

TRANSFER-FREE MULTILAYER GRAPHENE NEURAL INTERFACE

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TRANSFER-FREE MULTILAYER GRAPHENE NEURAL INTERFACE

Dissertation

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My heart was never deprived of acquiring knowledge
There are not many mysteries that I have not noticed
For seventy-two years I contemplated day and night
It has become known to me that I know nothing

Umar Khayyam

CONTENTS

SUMMARY

Technologies that are employed to record and modulate neural activities are rapidly advancing. This advancement could bring breakthroughs in our understanding of brain function and enable scientists to diagnose and treat neural diseases and disorders. Combining multiple modalities to study brain function, from single cells to large networks, offers insights beyond those offered by a single-modal platform using only electrical recording or modulation. However, the tools to enable such studies are yet to be developed and still face significant challenges that remain to be resolved to allow multimodal measurement without any of the modalities interfering with one another.

Recently, graphene-based neural electrodes have shown great promise for combining optical and electrical modalities in a single device. However, their complicated fabrication process, high impedance, and low charge storage capacity currently limit their application. In addition, their compatibility with the magnetic domain remains to be proven.

In this thesis, graphene-based microfabricated platform technology is introduced for the manufacturing of multimodal neural interfaces. First, a transfer-free fabrication process is demonstrated to fabricate multilayer graphene electrodes on parylene-C substrates. Full electrochemical characterization is performed on these graphene electrodes and a comparison is made with conventional metal-based electrodes. Second, a nanoparticle printing technique, spark ablation, is leveraged to print platinum nanoparticles on the graphene electrode surface to enhance its electrochemical characteristics even further without compromising its optical transparency. Third, a hybrid encapsulation stack is fabricated and validated that includes parylene C and PDMS with thin ceramic interlayers to be employed as the encapsulation layer on the final neural-interface device.

The multimodal platform technology introduced in this thesis can be used as a tool in multimodal measurements combining electrical, optical, and magnetic domains. The fabricated multilayer graphene electrodes show the highest charge storage capacity among all CVD graphene electrodes to date. They show no optical and MRI artifacts. Moreover, the fabricated electrodes and encapsulation stack both reveal the high optical transparency required for optical measurements. Local platinum nanoparticle printing can improve the impedance, charge storage, and charge injection capacity by 4.5, 15, and 3.6 times, respectively.

SAMENVATTING

Technologieën die worden gebruikt om neurale activiteit vast te leggen en te moduleren maken een stormachtige ontwikkeling door. Deze vooruitgang zou doorbraken kunnen opleveren in ons begrip van het functioneren van de hersenen en wetenschappers in staat stellen neurale ziekten en stoornissen te diagnosticeren en te behandelen. Het combineren van meerdere modaliteiten om de hersenfunctie te bestuderen, van enkele cellen tot grote netwerken, biedt inzichten die verder reiken dan geboden worden door een uni-modaal platform dat alleen elektrische opname of modulatie biedt. De instrumenten om dergelijk onderzoek mogelijk te maken moeten echter nog worden ontwikkeld en worden nog steeds geconfronteerd met aanzienlijke uitdagingen die nog moeten worden opgelost om multimodale metingen mogelijk te maken zonder dat de modaliteiten elkaar storen.

Op grafeen gebaseerde neurale elektroden toonden zich onlangs veelbelovend voor het combineren van elektrische en elektrische modaliteiten in één apparaat. Echter, hun ingewikkelde fabricageproces, hoge impedantie, en geringe ladingsopslagcapaciteit beperken momenteel hun toepassing. Bovendien dient hun compatibiliteit met het magnetische domein nog aangetoond te worden.

In dit proefschrift wordt een op grafeen gebaseerde microgefabriceerde platformtechnologie geïntroduceerd voor de vervaardiging van multimodale neurale interfaces. Eerst wordt een transfervrij fabricageproces om meerlaagse grafeenelektroden op paryleen-C substraten te vervaardigen gedemonstreerd. Een complete elektro-chemische karakterisatie wordt uitgevoerd op deze grafeenelektroden en er wordt een vergelijking gemaakt met conventionele op metaal gebaseerde elektroden. Ten tweede wordt gebruik gemaakt van een techniek om nanodeeltjes te printen, vonkablatie, om platina nanodeeltjes op het oppervlak van de grafeenelektrode te printen om de elektrochemische eigenschappen nog verder te verbeteren zonder compromissen ten aanzien van de optische transparantie. Ten derde wordt een hybride inkapselingsstapel vervaardigd en gevalideerd die paryleen C en PDMS met dunne keramische tussenlagen bevat als de inkapselingslaag op het uiteindelijke neurale interface-apparaat.

De in dit proefschrift geïntroduceerde platformtechnologie kan worden gebruikt als hulpmiddel in multimodale metingen die de elektrische, optische en magnetische domeinen combineren. De gefabriceerde elektroden met lage impedantie en hoge ladingsopslagcapaciteit vertonen geen optische en MRI artefacten. Bovendien tonen de gefabriceerde elektroden en de inkapselingsstapel beide de hoge optische transparantie aan die is vereist voor optische metingen. Het lokaal printen van platina-nanodeeltjes kan de impedantie, de ladingsopslag, en de ladingsinjectiecapaciteit verbeteren met respectievelijk 4,5, 15 en 3,6 keer.

1

INTRODUCTION

1.1. BIOELECTRONIC MEDICINE

Bioelectronic medicine is an innovative and growing healthcare field that focuses on developing methods to advance the diagnosis and treatment of a wide range of diseases and neural disorders using electrical signals instead of chemical drugs.

All neurons in our nervous system communicate with each other by means of electrical signals. It is possible to manipulate these neurons to restore their activity by stimulating or inhibiting the malfunctioning pathways using an implantable device. Such implants are already widely used for several conditions, such as deep-brain stimulation (DBS) to treat Parkinson's disease, neural stimulation to treat epilepsy or paralysis, and retinal prosthetic devices to treat blindness or vision loss. Depending on the application, stimulating, inhibiting, and recording the electrical activity, or a combination of these functionalities might be employed.

To achieve such therapies with bioelectronic medicine, devices and neural interfaces (interfacing between the biological tissue and the electronics) are used as a tool to interact with the nervous system and uncover the hidden world of neurons.

These devices must be placed close to the targeted nerves and, therefore, miniaturization is necessary to reduce their form factor in the human body and minimize the damage to the surrounding soft tissue. An ideal neural interface should be also biocompatible to prevent a host-induced inflammatory reaction. These reactions might lead to the formation of an encapsulation region around the device, subsequently decreasing the signal-to-noise ratio and stimulation efficiency. Conventional neural interfaces consist of metal electrodes for electrical signal transfer. Therefore, the electrode should have a high electrical conductivity and a high charge transfer capability.

Moreover, the envisioned therapy delivered in the field of bioelectronic medicine is personalized, meaning that it can be tailored to the person's condition. This can be achieved by integrating electronic circuitry in the implantable device (leading to so-called active implantable devices) which can allow for bidirectional communication between the neural tissue and the outside world. The electronic components can be implanted inside the body close to the targeted neurons. Hence, protecting the electronic

components from the harsh environment of the human body is of paramount importance for the lifetime of the device to prevent early failure. Therefore, encapsulation of the implantable device using soft encapsulation is an important aspect of designing such devices.

Despite the enormous development of implantable devices and their wide use in clinical applications, the interaction of the neural interface with the neurons has not been fully understood. This makes the further development of such devices difficult. Besides, only relying on electrical recording and stimulation might not be enough to decipher neural connectivity due to the low spatiotemporal resolution achieved by these methods. Therefore, combining multiple recording and stimulation methods in a synergistic way may enable scientists to decipher such complicated neural connections from small neurons to neural networks and populations.

The main challenges for achieving such multimodality are the required tools and methodologies. The neural interfaces should be designed such that minimum interference between different modalities is ensured. Therefore, specific requirements should be considered for selecting the electrode material.

Another important aspect of designing such a neural interface is the soft encapsulation that facilitates the protection of electronic components and at the same time fulfills the requirements for a multimodal platform, such as a high optical transparency required for the optical domain.

1.2. RESEARCH OBJECTIVES

The research presented in this thesis was supported by the POSITION-II project funded by the ECSEL Joint Undertaking (JU) under grant number Ecsel-783132-Position-II- 2017-IA. The objective of this project was to develop devices for the field of medical devices. The fabrication of the electrodes for neural interfacing was carried out at the Else Kooi Laboratory (EKL) of Delft University of Technology and a nanoparticle printer from VSPARTICLE B.V. was used to print nanoparticles on graphene.

The goal of the research presented in this thesis was to develop a set of enabling microfabricated technologies for electrodes and the development of an encapsulation stack that facilitates the use of multiple modalities which results in a multimodal platform technology for neural interfaces. Microfabrication provides the tool to achieve a miniaturized neural electrode by using photolithography techniques. The envisioned platform technology provides the possibility of combining different modalities such as electrical recording, electrical stimulation, optogenetics, optical imaging, and magnetic resonance imaging (MRI) for neural recording and stimulation on a small and large scale.

To achieve this, several critical aspects of this goal have been investigated. First, a fabrication process was introduced for graphene electrodes combined with polymer substrates using a wafer-scale transfer-free fabrication process. Then, a full assessment of the electrochemical characteristics of the fabricated graphene electrodes was performed and compared to those of conventional metal electrodes with the same size and geometry to demonstrate the possible substitution of such electrodes with the graphene electrodes for the applications of electrical recording and stimulation.

Moreover, the multimodality of the graphene-based electrodes for neural interfacing was demonstrated to show the potential combination of electrical, optical, and mag-

netic modalities with minimal interference between them. The optical transparency of the fabricated graphene electrodes was evaluated to ensure their compatibility with optical imaging and optogenetics. Furthermore, optical-induced artifacts in the electrical domain and magnetic-induced artifacts due to a potential magnetic susceptibility difference between the electrode and the tissue were assessed to prevent any interference from one modality to the other.

Platinum nanoparticle (Pt NP) printing was employed using the spark ablation method as a surface-modification technique on the graphene electrode surface to further improve the graphene electrodes' electrochemical characteristics. However, careful consideration was taken into account to ensure that the method used for electrochemical performance improvement does not compromise the optical transparency of the electrode.

Finally, an optically transparent encapsulation stack was introduced that could contribute to a longer lifetime of the device.

1.3. OUTLINE OF THIS THESIS

In this thesis, a number of microfabricated technologies have been developed to enable a platform technology for multimodal neural interfacing. Several aspects of the design, fabrication, and characterization of the neural interface, and its soft encapsulation have been investigated.

In Chapter 2, an overview of the existing methods for neural recording and modulation has been provided. Then, the neural interfaces and their challenges for combining multiple modalities in one single platform are explained. Next, the state-of-the-art optically transparent electrodes are introduced. Additionally, with more focus on graphene electrodes, the existing fabrication methods for graphene-based neural interfaces and their characterization are discussed. Then, surface modification techniques are introduced as a method to enhance the electrochemical characteristics of an electrode. Finally, the state-of-the-art encapsulation techniques, specifically soft encapsulation, are discussed.

Chapter 3 focuses on the fabrication process of multilayer graphene neural electrodes using a wafer-scale transfer-free process. This method allows for the fabrication of high-temperature graphene growth with a polymer substrate without using any additional graphene transfer. Moreover, it allows for the substitution of a non-biocompatible copper (Cu) catalyst, commonly used for graphene growth, with molybdenum (Mo). The proposed fabrication process allows for the combination of graphene electrodes with various polymers with different ranges of mechanical properties that can be tuned based on the final application and its required polymer properties. Full electrochemical characterization of the multilayer graphene electrodes is performed. The multilayer graphene electrodes fabricated in this work are compared with conventional electrodes with the same size and geometry. Moreover, optical transparency and photo-induced artifact tests are performed to demonstrate the possibility of using such electrodes for multimodal electrical-optical platforms. MRI- compatibility of the electrodes is also studied and compared with conventional metal electrodes.

Chapter 4 presents the surface modification of graphene electrodes using Pt NPs to enhance their electrochemical characteristics. The spark-ablation method is used as a

post-process step to print Pt NPs on the graphene surface. Then, full characterization and comparison of the electrodes with and without coatings is performed to confirm the electrochemical improvement after adding the NPs to the graphene surface. Electrochemical and mechanical stability tests are also performed to ensure that long-term improvement in the electrode performance is achieved.

In Chapter 5, a soft encapsulation stack for encapsulating the final device is introduced. Thin ceramic layers are integrated between two polymers to enhance their adhesion and at the same time act as barrier layers against water vapor. The proposed method is fully characterized to ensure a sufficient water vapor barrier and suitable adhesion between polymers.

The general conclusions of this thesis, contributions to the field of microfabrication, and recommendations for future research are collected in Chapter 6.

1.4. LIST OF ORIGINAL PUBLICATIONS

JOURNAL ARTICLES

- **N. Bakhshaee Babaroud**, S. J. Rice, M. C. Perez, W. Serdijn, S. Vollebregt and V. Giagka. "Surface modification of multilayer graphene electrodes by local printing of platinum nanoparticles using spark ablation for neural interfacing". Nanoscale. 2024.

- **N. Bakhshaee Babaroud**, M. Palmar, A. I. Velea, C. Coletti, S. Weingärtner, F. Vos, W. Serdijn, S. Vollebregt and V. Giagka. "Multilayer CVD Graphene electrodes using a transfer-free process for the next generation of optically transparent and MRI-compatible neural interfaces". Microsystems & Nanoengineering- Springer Nature. Sep. 2022 (Selected as a featured article on the journal website).

CONFERENCE CONTRIBUTIONS

- **N. Bakhshaee Babaroud**, R. Dekker, O. Holk, U. Tiringer, P. Taheri, D. Horvath, T. Nanasi, I. Ulbert, W. Serdijn, and V. Giagka. "Investigation of the long-term adhesion and barrier properties of a PDMS-Parylene stack with PECVD ceramic interlayers for the conformal encapsulation of neural implants". In: 2021 23rd European Micro-electronics and Packaging Conference and Exhibition (EMPC). IEEE. 2021, pp. 1–7.

- A. Velea, J. Wilson, A. Pak, M. Seckel, S. Schmidt, S. Kosmider, **N. Bakhshaee**, W. Serdijn, and V. Giagka. "UV and IR laser-patterning for high-density thin-film neural interfaces". In: IEEE 2021 23rd European Microelectronics and Packaging Conference (EMPC) 2021, Online, September 2021.

- **N. Bakhshaee Babaroud**, R. Dekker, W. Serdijn, and V. Giagka. "PDMS-Parylene Adhesion Improvement via Ceramic Interlayers to Strengthen the Encapsulation of Active Neural Implants". In: 2020 42nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC). IEEE. 2020, pp. 3399–3402. 11.

- **N. Bakhshaee Babaroud**, M. Kluba, R. Dekker, W. Serdijn, and V. Giagka. "Towards a semi-flexible parylene-based platform technology for active implantable medical devices", In Book of Abstracts, SAFE 2019, Delft, the Netherlands, July 4-5 2019.
- **N. Bakhshaee Babaroud**, M. Kluba, R. Dekker, W. Serdijn, and V. Giagka. "Towards a semi-flexible parylene-based platform technology for active implantable medical devices", In Book of Abstracts, 2019 International Winterschool on Bioelectronics Conference (BioEl 2019), Kirchberg, Tirol, Austria, 16-23 March 2019.
- **N. Bakhshaee Babaroud**, M. Kluba, R. Dekker, W. Serdijn, and V. Giagka. "Towards a semi-flexible parylene-based platform technology for active implantable medical devices", In Book of Abstracts, 7th Dutch Biomedical Engineering Conf. (BME) 2019, Jan. 24-25 2019.

CO-SUPERVISED MASTER THESES

- Merlin Palmar, "Improving electrical characteristics of graphene neural electrode with nanoparticles and doping," Master thesis, 2021.
- Abdul Tawab Karim, "Monolithically fabricated flexible graphene-based active implant," Master thesis, 2022.
- Samantha Rice, "Graphene with Platinum nanoparticles for neural recording and stimulation,", Master thesis, 2023.

2

STATE-OF-THE-ART MULTIMODAL NEURAL INTERFACES

This chapter discusses state-of-the-art multimodal neural interfaces. Specifically, neural interfaces that could enable the possibility to combine different modalities such as electrical, optical, and magnetic are studied and discussed in this chapter to understand the required design specifications for a multimodal platform technology. First, a brief introduction is given to the methods used to interact with the nervous system. Then, their challenges are investigated, and the requirements for designing a new platform technology for multimodal neural interfaces are introduced. Then, the electrode material, its electrochemical characteristics, and its requirements in terms of compatibility with other activation and monitoring modalities are discussed. Next, current state-of-the-art methods for electrode surface modification with the aim of electrochemical characteristics improvement are studied. Finally, the encapsulation methods, the current state-of-the-art, and their challenges are introduced.

2.1. INTERACTING WITH THE NERVOUS SYSTEM

There are billions of neurons with different types and shapes in our nervous system. Each neuron has complicated connections with the surrounding neurons by means of electrical and chemical signals. The electrical signals are carried via the membrane of the neural cells. Neural cells are depicted in Fig. 2.1 (a). The membrane potential is about -70 mV at the resting state. Excitation of a neural cell triggers an action potential (AP) (as shown in detail in Fig. 2.1 (b)), also called "units" or "spikes", which propagate along the axon and result in the release of chemical neurotransmitters at synapses. The neurotransmitters influence the behavior of other neurons and cause the adjacent neurons to generate APs. This mechanism is the basis of neural communication [1].

In addition to APs, small ionic currents cause the membrane potential to deviate from its resting state. These small potential deviations last longer than an AP. The mea-

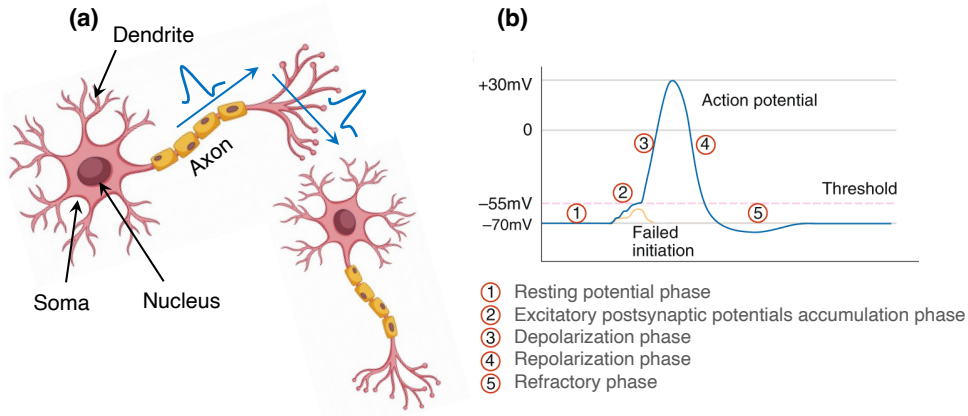

Figure 2.1: (a) A schematic of a neural cell (Adapted and modified from https://www.freepik.com/free-photos-vectors/neuron-cell); (b) Waveform of a typical action potential (AP) of a neuron: 1) A neuron in the resting state has a potential of around −70 mV compared to the outside of the membrane. 2) The neuron generates an AP if a sufficient excitatory potential increases the membrane potential above the threshold value. 3) The voltage between the inside and outside of the membrane changes to a positive value due to the inflow of Sodium (Na) ions during the depolarization phase. 4) The voltage decreases due to the closing of the Na channels and opening of Pottasium (K) channels during the repolarization phase. 5) The voltage drops and returns to the initial resting potential after the refractory phase [1].

sured extracellular potential is always the superposition of all ionic processes and is called the local field potential (LFP) when recorded on the cortical surface [2].

To understand the connection between neural circuit activity and certain functions and behavior in our nervous system, it is necessary to record and manipulate the neural activity [3]. There are various methods for recording and modulating the neural activity. These methods include multiple modalities, such as electrical, optical, magnetic, acoustic, and, etc. This thesis only focuses on the electrical, optical, and magnetic domains, however, in this chapter, a list of the various approaches for neural recording and modulation is outlined to give an overview of some of the main modalities for interacting with the nervous system and to provide context for the methods explored in this thesis.

2.1.1. ELECTRICAL

RECORDING

Electrical recording has been the most powerful method for neural recording due to its wide range of neural applications, capturing neural signals from individual neurons to neural populations. Macroscopically, electroencephalography (EEG) is the most widely used non-invasive method of recording the LFPs from a population of neurons by using patch electrodes attached to the surface of the scalp [4]. The recorded signals only contain the largest neural signals since they must travel through the brain fluid and skull before being recorded by the electrode and capture mostly low-frequency content due to low-pass filtering of the skull [5].

To collect neural signals with higher resolution and with a wider range of frequency content, electrocorticography (ECoG) is employed using electrode grids or strips placed

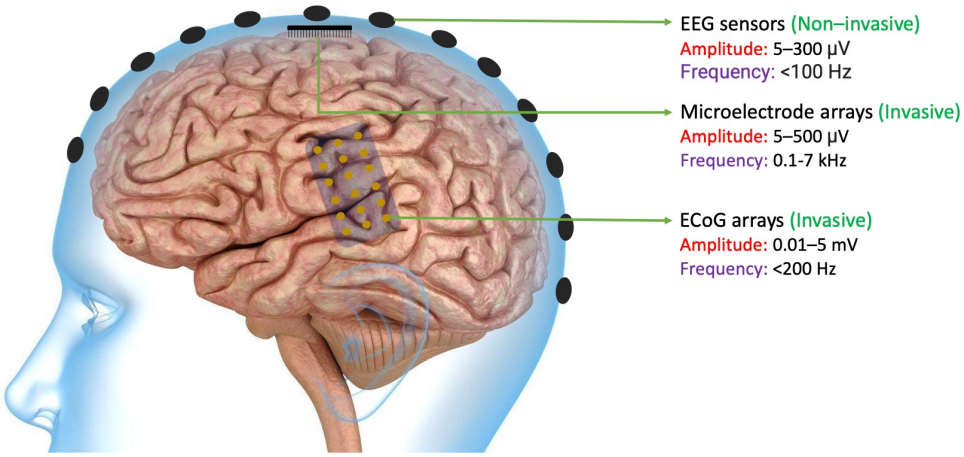

Figure 2.2: Existing electrical recording methods including EEG, ECoG, and microelectrode arrays with their acquired signal characteristics (Adapted from [6]).

subdurally onto the surface of the brain [2].

Additionally, microelectrode arrays offer the highest spatial and temporal resolution in electrical recording. Microelectrode arrays can be divided into micro-wire electrode arrays and microfabricated electrode arrays. Micro-wire electrodes consist of conductive wires coated with an insulation layer except at the tip of the micro-wire, where the recording contact is located. These electrodes are used as penetrating electrodes collecting neural signals in a certain depth of the brain. Microfabricated electrode arrays typically include surface micro-ECoG (μECoG) arrays and penetrating electrode arrays. μECoG arrays consist of thin metal films patterned through photolithography on polymer substrates and are conformally placed on the surface of the brain. Penetrating electrode arrays are typically fabricated on rigid silicon substrates, with multiple electrode contacts along the length of the shank to enable recording neural activity at multiple depths into the brain [2].

An overview of all these methods together with their acquired signal characteristics is shown in Fig. 2.2.

STIMULATION

The first demonstration of neuromodulation was realized by Luigi Galvani in the late 18^{th} century to stimulate the sciatic nerve of a frog [7]. To stimulate neurons, electrical signals are sent through stimulating electrodes to the targeted regions. Electrical stimulation induces charge redistribution at the electrode-neural interfaces which can lead to the depolarization (activation) or hyperpolarization (inhibition) of neurons [3]. Electrical stimulation has shown a reduction of motor symptoms in patients suffering from Parkinson's disease [8, 9] and a reduction of seizure rates in those suffering from epilepsy [10, 11]. Electrical stimulation also enabled the development of brain-computer interfaces (BCIs) which can restore lost sensory or motor functions. Restoration of vision with retina implants [12], and gaining sensory feedback from prostheses by using implanted

thin-film electrodes [13] are some examples of such developments.

Although neural activity can be modulated by electrical stimulation, there are still several major challenges to be addressed. First, single-cell stimulation has not been possible so far because the induced electric field by the electrode affects all adjacent neural cells (within the electrode radius). Second, electrical stimulation does not have neuron-type specificity; and third, repeated stimulations might cause irreversible chemical reactions at the electrode-tissue interface resulting in decreased stimulation efficiency [3, 7, 14].

2.1.2. OPTICAL

RECORDING

Optical recording refers to optical monitoring or imaging of neural activity. It works based on the basic concept that light absorption and scattering are responsive to functional changes in neural tissue [15]. Since water and hemoglobin on the brain tissue absorb much of the light only a narrow wavelength range from 680 to 1000 nm can be used for optical imaging. Optical imaging technique makes it possible to image brain activity with a subcentimeter spatial resolution and millisecond-level temporal resolution [16]. Optical imaging approaches are divided into two main categories. The first category includes those based on the identification of neuro-dynamics that are molecular-selective using fluorescent [17, 18] and voltage-sensitive dyes [19]. The second category of optical imaging consists of methods analyzing scattering and oxygenated condensation changes in brain tissue such as optical coherence tomography (OCT) [20] and diffuse optical tomography (DOT) [21].

Calcium imaging is a sensitive method for monitoring neural activity. Fluctuations in intracellular Calcium ion (Ca^{2+}) concentration in response to cell activity can be observed using fluorescent indicators. These indicators show a change in fluorescent properties when bound with free Ca^{2+}. Chemical indicator dyes provide large signal-to-noise ratios, however, it is difficult to load them into cells and keep them there over a longer recording time. Genetically encoded Ca^{2+} indicators have the advantage of genetic targeting cell-type specificity. The main disadvantage of calcium imaging is that fluctuation in Ca^{2+} concentration is an indirect measure of neural activity. One of the other key limitations of this technique is their limited temporal resolution due to Ca^{2+} binding and unbinding kinetics from the fluorescent indicators and the limited speed of the imaging instrumentation. Other challenges include limitation to image at high resolution across a broad field of view and difficulty in imaging deep structures due to light scattering in tissue [22, 23, 24].

Voltage-sensitive dye imaging measures neural activity by using specific molecules that can modify electric charges from neural cells into fluorescence of emitted light. Therefore, it enables a more direct measure of neural activity compared to calcium imaging. Since this method provides only the surface activity of the brain in two dimensions, it is difficult to monitor deep brain activity. However, the importance of this approach compared to electrical recording lies in the neural activity measurement from many cells or multiple sites simultaneously, such as in the nerves or brain. However, achieving fast acquisition speeds while maintaining a large field of view is significantly challenging. The speed of image acquisition must be fast to be able to sample APs. However, voltage

indicators do not have sufficient time to deliver photons to the imaging detector, making each measurement noisy.

STIMULATION

Light can be also used to manipulate neurons. One of the attempts to stimulate neurons optically was to use a femtosecond laser. The femtosecond laser has a high spatial selectivity as it triggers neural activities only at a focal point. However, it suffers possible cell death due to reactive oxygen species (ROS) produced during the stimulation. Another optical stimulation technique is infrared neural stimulation (INS) which modulates neural activities by shining a pulsed infrared light. This method suffers from accumulated heat in the tissue due to the high water absorption [25].

Neuroscience research has been recently revolutionized by optogenetics. Optogenetics is a powerful technique that uses light to stimulate neurons. It requires genetic modification of neural cells to make them susceptible to light [26, 27]. Genes encoding light-activated ion channels, called opsins, are expressed in specific types of cells. Therefore, unlike electrical stimulation, it can provide cell-type specificity. Shining the light with the correct wavelength to the neuron opens the ion channels and allows the inflow of Na^+ or Cl^-, leading to the depolarization (activation) or hyperpolarization (inhibition) of neurons depending on the light wavelength [28, 29]. The cell-type specificity in optogenetics made it possible to unravel the contributions of specific cell types to neural circuits since activation and inhibition of those specific cells can reveal the impact they have on the generation of behaviors and pathologies [2].

Optogenetics can enable millisecond-scale neural modulation in behaving animals and has greatly advanced our understanding of neural circuit function. Translational research studies towards human applications and treatments focus on optical cochlea implants [30, 31] and most recently also on the restoration of vision [32]. One of the main challenges in optogenetics is the scattering and absorption of visible light by neural tissue. Thus, methods of light delivery to the brain including implantable optical fibers [33], implantable probes with integrated optical waveguides [34] or micro-light emitting diodes (μ-LEDs) [35] have recently attracted great attention.

2.1.3. MAGNETIC

RECORDING

Due to the low magnetic susceptibility of biological tissues, magnetic fields can reach deep tissues with minimal signal attenuation [36]. Functional magnetic resonance imaging (fMRI) is a non-invasive method that allows imaging of the whole brain. fMRI works based on the differences between the magnetic properties of oxygenated and deoxygenated hemoglobin and measures the blood flow increase that accompanies neural activity [37]. Therefore, it has an indirect correlation to neural activity. It has a limited spatial resolution which is defined by the voxel size and is on the order of 1 mm^3 [38]. The temporal resolution is on the order of 1 s, and it is limited both by the image sampling rate and the slow hemodynamic response time [39]. Despite its relatively poor spatiotemporal resolution, fMRI has enabled many insights into the functions of specific regions in the human brain and their contributions to different cognitive processes [2].

STIMULATION

The activation of neurons via magnetism has been greatly investigated. Magnetic stimulation does not require contact with the targeted neurons since magnetic fields easily pass through biological tissues. Transcranial magnetic stimulation (TMS) is a non-invasive technique that uses magnetic fields with frequencies below 1 kHz and amplitudes above 1 T to modulate brain activity through the skull. In this method, a high-amplitude current pulse passing through a coil produces a transient magnetic field which can induce an electric field in the tissue and consequently modulate neurons [40]. The spatial resolution achieved by this method is limited to 1 cm.

Magnetic stimulation can be also performed locally using an implantable micro-coil [41]. The shape of the coil can be changed and lead to an anisotropic shaping of the electric field which can consequently increase precision by stimulating neurons of a particular orientation [42].

Another method for using magnetic fields to achieve neuromodulation is the use of magnetic nanoparticles (MNPs) as transducers. MNPs use two mechanisms of magneto-thermal [43] and magneto-mechanical [44] to transduce magnetic fields into neural activation. The use of these magnetic transducers allows modulation on the microscale, as well as cell-type specific targeting.

2.1.4. ACOUSTIC

RECORDING

Ultrasound (US) is a form of acoustic energy that can penetrate several centimeters deep into the soft tissues at wavelengths on the order of 100 µm [45]. Furthermore, sound waves propagate at speeds of 1.5 km/s in soft tissue, which gives temporal precision below 1 ms for US [2]. The US has been used as a technique to image soft tissues throughout the body. US imaging works based on the transmission of US pulses into tissue and recording the backscattered echoes from the objects and interfaces in the tissue [45]. Although US is strongly attenuated by bone, brain imaging is possible through the intact skull in mice, and through cranial windows in other species. Functional US imaging (fUSI) can image cerebral blood flow with a high temporal resolution in awake, behaving subjects by fixing a miniaturized US probe onto their skull [44].

STIMULATION

The US can be used for neural stimulation as a non-invasive method that can target cm-deep brain areas with high spatial resolution. Since US waves only need to travel in one direction (backscattering is no longer used for neural stimulation) lower frequencies can be used as they travel easily through the skull [45]. Studies showed that targeted regions of a rat's brain could be both stimulated and suppressed using focused ultrasound (FUS) [46]. In awake non-human primates and humans, FUS applied to the brain has been shown to modify perception, behavior, and other neurophysiological responses [47]. The exact mechanisms by which FUS achieves its neuromodulatory effects are not fully understood, but it is believed to act through mechanical force on neurons, transduced by mechanosensitive ion channels [48].

2.1.5. MULTIMODAL NEURAL INTERFACING

CHALLENGES OF HYBRID OPTICAL-ELECTRICAL MODALITIES

As mentioned, there are various modalities for stimulating or recording neural signals, and each has its own advantages and disadvantages. Thus, simultaneously integrating multiple modalities on a single device for recording and stimulation can provide more possibilities for the analysis of neural functions [49, 50, 51, 52].

In particular, a hybrid of optical and electrical approaches maximizes the synergism of the resolution of the two methods, while at the same time compensates for the weaknesses of each approach [53, 54, 55, 56]. This multimodality can pave the way towards studying the connectivity between the neurons, the function of neural circuits, and understanding the underlying mechanism [57, 58, 59].

Optogenetic stimulation combined with simultaneous electrophysiology enables the mapping of the dynamics of stimulated neurons at the network level [60, 61]. Simultaneous electrophysiology and optical imaging of neural structure and function could be also advantageous. Conventional neural recording electrodes offer a high temporal resolution. However, they lack the spatial resolution that optical methods provide. Optical imaging can reveal the finest spatial intricacies in brain tissue though they are still catching up in recording fast neural activities [62]. Combining these two modalities, in a single, hybrid platform could lead to complementary and powerful new ways to explore the brain and has recently gained great attention in neuroscience and neural engineering research [63, 64].

Therefore, the main idea of combining multiple modalities in one platform is to exploit the advantages of all and minimize the weaknesses of each approach. Therefore, careful consideration in designing such platforms should be taken into account to prevent data interference between these methodologies and to generate diagnostic or therapeutic synergies with them. Recent studies have revealed that opaque electrodes based on conventional metals, such as gold or platinum, pose several challenges in the integration of electrical and optical modalities including photoelectric artifacts, optical image blocking, and light transmittance efficiency as illustrated in Fig. 2.3.

The photoelectric effect refers to a phenomenon in which light with a specific frequency is emitted on a metal electrode causing a current flow at the surface of the electrode and consequently creating a potential difference in the electrode as shown in Fig. 2.3 [66, 67]. As this phenomenon occurs inside the saline body solution, it is also called the photoelectrochemical effect. The metal-based microelectrode has a high probability of causing photoelectric effects due to the overlap between their conduction and valence bands which can result in much easier photoexcitation of metal electrons compared to those of other materials [65]. This effect might also lead to an accumulation of charge on the electrode [68, 66, 67].

The photoelectric effect can result in so-called photoelectric artifacts. When the electrophysiological signal generated by optogenetics is being recorded, the signal created due to the photoelectric effect is the main source of data contamination. If an increase in the amplitude of the recorded signal is observed at the start of light irradiation, it can be considered noise caused by the light source. This noise can be minimized by using filtering or linear regression of the trace of the signal. However, for the signal that follows, it is unclear whether it is noise caused by photoelectric artifacts or a biological signal from an experimental model. To overcome this issue, optical stimulation was

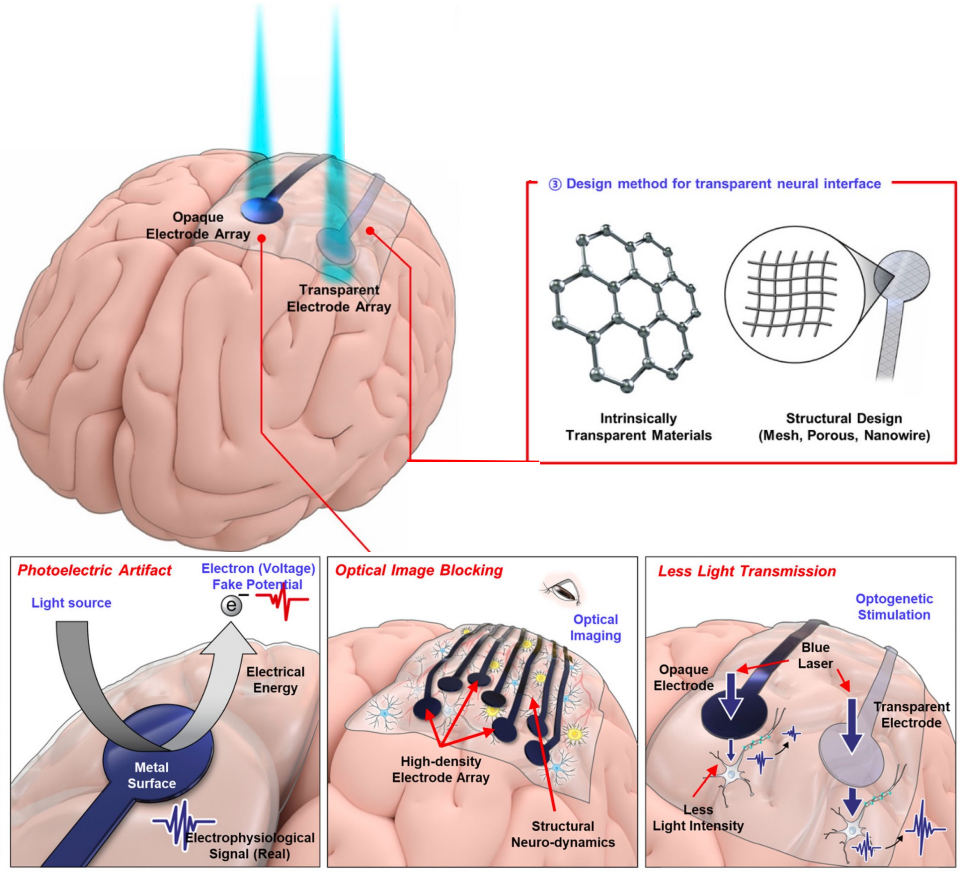

Figure 2.3: Schematic illustration of the conventional neural electrodes challenges when combining electrical and optical modalities (Adapted and modified from [65]).

only performed using low-frequency or long-rise time waves to reduce light-induced artifacts. This approach limits the possibility of treating neurological diseases that require high-frequency light stimulation. In conclusion, to enable light stimulation in a wide frequency band without interference by artifacts, it is necessary to select an electrode material that barely generates a photoelectric effect [65].

Another issue attributed to the use of opaque electrodes for neural interfaces is the block of the field of view by the electrodes [69, 70, 71]. Optical imaging provides a high spatial resolution of the activated tissue. To ensure that neuro-dynamic information can be obtained with a high temporal resolution, integration of electrophysiological approaches is significantly important. The use of opaque electrodes in such a dual-modality platform blocks the field of view exactly underneath the recording electrode as illustrated in Fig. 2.3.

A similar issue can be observed when electrical stimulation and optical imaging are combined in one single platform. As shown in Fig 2.4 (a,b), the peak response of the neurons using fluorescence imaging is blocked by the Pt electrodes used for neural stimulation. The opaque electrodes make it difficult to observe vascular changes and the dynamic activity of nerves during stimulation. This issue limits the use of such a multimodal platform and the potential expected synergism impact. This problem deteriorates for high-density electrode arrays as the number of channels and connections required per electrode increases.

Finally, optical stimulation of the neurons is affected by frequency and light intensity in optogenetic applications. Therefore, it is necessary that the neural interface used between the brain and the light source should not interfere with the light to reach the neurons. Recent research investigated the light transmission efficiency of a transparent gold nano-network electrode in comparison with a think-film gold electrode and showed that the opaque electrode absorbs most of the light causing the failure of stimulation on a transgenic mouse while a gold nano-network electrode array showed the propagation of high-amplitude potential from the same stimulation site to the surrounding tissue, suggesting the possibility of increasing the light transmission efficiency with the same material [66]. Thus, the most ideal approach to overcome this problem is to use optically transparent electrode materials or design electrodes by engineering materials and structures to minimize energy loss of the light.

CHALLENGES OF HYBRID MAGNETIC-ELECTRICAL MODALITIES

As mentioned before, the therapeutic mechanisms of electrical stimulation of neurons are poorly understood. Electrical stimulation of brain tissue may initiate neural responses at both the local and global levels. However, using the electrical recording to record these responses, due to its low spatial resolution, does not provide the bigger picture as it might only give insights into local changes.

Magnetic resonance imaging (MRI), and specifically functional MRI (fMRI), represents a powerful tool for mapping brain activity with a higher spatial resolution. Therefore, simultaneous electrical stimulation and magnetic imaging could provide valuable insights into brain function, connectivity patterns, and therapeutic mechanisms of electrical stimulation in various neurological disorders [73, 74, 75, 76].

MRI can also be beneficial in clinical applications during or after device implantation, including verification of implanted electrode placement (specifically DBS elec-

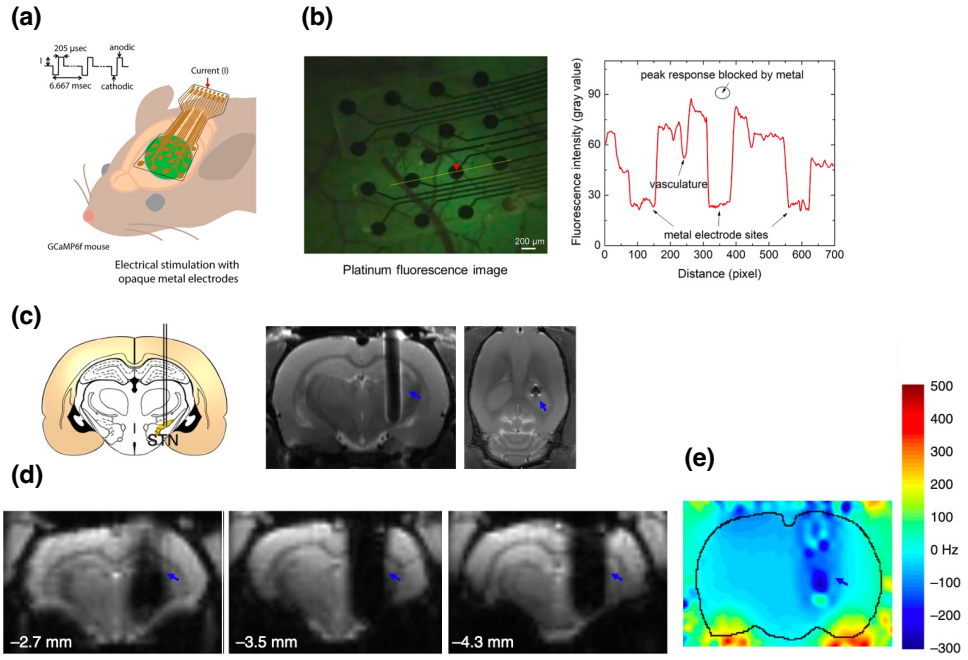

Figure 2.4: (a) Electrical stimulation of the cortex through a Pt electrode and corresponding neural activity using fluorescence imaging in GCaMP6f mice; (b) Fluorescence intensity over platinum electrodes with an artifact from the electrode sites (Adapted from [70]); (c) A schematic of a PtIr electrode inside a rat brain and coronal (left) and horizontal (right) sections of the MRI T2-images of a rat brain with an implanted electrode; (d) Three serial coronal scans of EPI images from rat brains indicating the MRI artifact from the electrodes; (e) B0 field distortion map. The blue arrow points to the PtIr implant (Adapted from [72]).

trodes), and its stability [77], and long-term epilepsy monitoring that needs repeated signal recording and anatomical/functional neuro-imaging [78].

However, using conventional metal electrodes in MRI studies may produce an image artifacts or blind spots around the electrodes in MRI as shown in Fig 2.4 (c,d). These artifacts are caused by the induced severe field distortions (as shown in Fig 2.4 (e)) around the PtIr electrode implanted in a rat's brain due to a mismatch of the magnetic susceptibility between the metal and the surrounding tissue. Such artifacts may interfere with anatomical and functional MRI studies. Therefore, specific design requirements and material selection should be taken into account to ensure artifact-free measurement using a combination of electrical and magnetic recording and stimulation.

2.2. NEURAL ELECTRODES REQUIREMENTS

2.2.1. ELECTRODE REQUIREMENTS FOR MULTIMODAL NEURAL INTERFACES

Neural interfaces provide a bridge between the nervous system and the outside world. These devices are the most applied tools in neural activity recording and also provide therapy, when integrated with required electronic circuitry, for neurological disorders, such as Parkinson's disease with DBS electrodes [79].

The design and fabrication of neural interfaces are guided by some universal principles. The key element in the neural interface design is the electrode surface as it is the main physical contact between the biological tissue and the outside world. An ideal electrode monitors signals accurately while minimizing its own influence on the recorded information. In the case of a stimulation electrode, the injected pulses must reach the cell membrane, therefore, a transition from electronic to ionic signal should take place [80].

Electrode impedance is an important electrode characteristic that increases as the size of an electrode is reduced. Therefore, it becomes a significant challenge when electrodes are miniaturized. Achieving a low impedance is key for recording low-noise signals, as well as for efficient delivery of charge to the tissue for stimulation to limit the voltage drop across the electrode. Thus, choosing electrode materials with low impedance is a primary consideration for implantable electrodes.

Charge storage capacity (CSC) and charge injection capacity (CIC) are also of great importance for stimulation electrodes. CSC indicates how much charge an electrode can inject into the tissue. The stimulation efficiency of an electrode is determined by its charge injection capacity (CIC), which is the amount of charge that can be injected into the tissue without inducing any irreversible chemical reactions at the surface of the stimulating electrode [3]. More explanation on impedance, CSC, and CIC and how to measure these values will be discussed in the next section.

Another key challenge for implantable interfaces is the chemical stability of the electrode and insulation materials in the harsh environment of the body. The electrode material must be resilient to swelling, delamination, dissolution, and corrosion over the lifetime of the implant. If the electrodes are used to deliver electrical stimulation, electrochemical corrosion during charge injection cycles should be avoided. The insulation materials must withstand cracking and delamination as this leads to current leakage and degradation of the underlying conductive layers [81].

Recent investigations into the long-term performance of implanted neural electrodes have shown that the quality of signals transduced across the electrode-tissue interface decays over time [82]. One of the main reasons that limit the lifetime of implanted electrodes is the mismatch in mechanical properties between the implantable device materials (Young's moduli around 100 GPa) and the surrounding soft tissues (Young's moduli around 10 kPa). As a result, a glial scar is formed around the implant after the implantation which can be transformed into a chronic foreign body response over time. This biological response forms an insulating layer around the implanted electrode and limits ionic exchange between the electrode and surrounding tissue. The most effective approach for improving the long-term performance of implanted electrodes focuses on making electrodes smaller and softer to minimize the foreign body response.

Additionally, since the aim of this thesis is to design a microfabricated platform technology that can allow a combination of multiple modalities to be used for neural activity monitoring and neural stimulation it is of paramount importance to set additional electrode design and material selection requirements.

The neural interface is required to allow simultaneous measurements in the optical and electrical domains. Commonly used materials for implantable neural electrodes, metal electrodes, including platinum-iridium (PtIr), tungsten (W), gold (Au), and stainless steel are not optically transparent and might produce photoelectric artifacts and block the field of view in optical imaging. Therefore, the main requirements of the electrode material apart from the previously mentioned requirements are the broadband-wavelength optical transparency from infrared (IR) to ultraviolet (UV) to accommodate both optical imaging and optogenetics [83, 84, 85, 86]. In addition, the encapsulation layer should also provide such optical transparency.

As mentioned previously, using conventional electrodes in the combination of electrical modalities with the magnetic domain might generate artifacts, which may interfere with anatomical and functional MRI studies. Therefore, the main requirement for such electrodes is comparable magnetic susceptibility to those of soft tissue and consequently MRI-compatibility.

2.2.2. ELECTRODE-TISSUE INTERFACE

The implanted electrode in the body is surrounded by extracellular fluid creating an electrochemical cell. The electrode-tissue (electrolyte) interface is usually modeled using an equivalent circuit model, the so-called Randle model, as shown in Fig. 2.5 (a,b). Two main types of processes can occur at the electrode-electrolyte interface.

First, a non-Faradaic reaction in which the electrode behaves almost as an ideal capacitor and no electrons are transferred between the electrode and electrolyte due to the local arrangement of the charges at the electrode-electrolyte interface. The surface of the electrode with electrons forms the inner plate of a capacitance called a double-layer (C_{dl}) or Helmholtz capacitance, while the first layer of self-organized solubilized ions in the electrolyte forms the outer plane. Using a constant-phase-angle impedance, Z_{CPA}, instead of C_{dl} results in a better agreement of the model with the measurements [87]. This capacitance contributes more at low frequencies, introducing a phase shift and attenuating the signal [80]. The effect of the double-layer capacitance is directly proportional to the contact area of the electrode with the electrolyte solution.

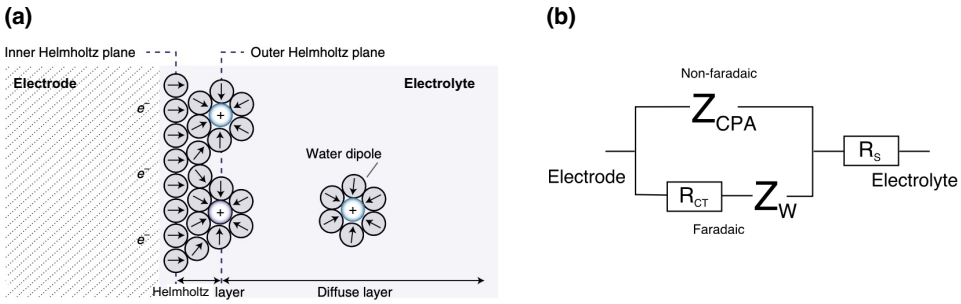

Figure 2.5: (a) Electrode-electrolyte interface (Adapted from [80]), (b) Commonly used equivalent circuit model of the electrode-electrolyte interface (Adapted from [88]).

Second, a Faradaic reaction in which electron exchange between the electrode and electrolyte is performed through oxidation and reduction. In oxidation, an electron is removed from the electrode that is driven positive while in reduction an electron is added at the electrode driven negative. These reactions result in the formation of some products that either stay on the electrode surface (reversible reaction) or diffuse away from it into the solution (irreversible reaction). This phenomenon can be modeled as a charge-transfer resistance, R_{CT}. The Warburg impedance, denoted Z_W, takes into account that ions, produced on the surface of the electrode, need to diffuse away. This impedance is negligible for large charge-transfer resistances. Lastly, the equivalent circuit model is completed with solution resistance, Rs, which shows a frequency-independent behavior [88].

ELECTROCHEMICAL IMPEDANCE

The electrochemical impedance is one of the important properties of the electrode-electrolyte interface. Electrochemical impedance spectroscopy (EIS) measures the electrochemical impedance and phase angle obtained with sinusoidal voltage or current excitation of the electrode. The amplitude of the excitation signal (usually between 10 and 100 mV) should be small to ensure that a linear current-voltage response is obtained. The measurement is made over a broad frequency range (typically within the 0.01 Hz–1 MHz interval) resulting in a spectrum that is called a Bode plot.

EIS is typically measured in a so-called three-electrode setup, as illustrated in Fig. 2.6 (a). A phosphate-buffered saline (PBS) solution is used to mimic the ionic liquid environment of the body. The working electrode (WE), the electrode under test, is immersed in a PBS solution together with a large-area counter electrode (CE) that closes back the electrical circuit. Due to the large surface area of the counter electrode, its impact on the electrochemical impedance is negligible. The setup is completed with a non-current-bearing reference electrode (RE), against which all voltage measurements are taken.

EIS is used broadly for benchmarking the performance of recording and stimulating electrodes. For neural electrodes, it is common to report the impedance magnitude at 1 kHz, as this is around the frequency where the information content in an action potential occurs [80].

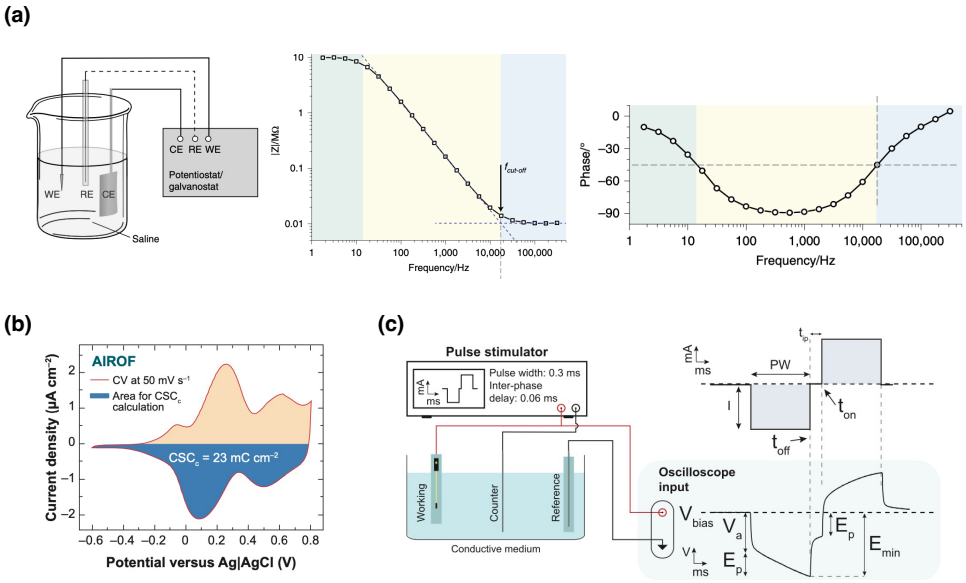

Figure 2.6: (a) A schematic diagram of a three-electrode setup with WE, CE, RE, and the Bode plot (impedance magnitude and phase angle) of a sample electrode over frequencies from 1 Hz to 100kHz (Adapted from [80]), (b) CV curve of activated iridium oxide film (AIROF) electrode. The blue region depicted in the voltammogram shows the time integral of the negative current, representing the cathodic CSC (Adapted from [89]), (c) Schematic diagram of a three-electrode setup for voltage transient measurements, applied stimulation waveform (top) and a polarization measurement of a sample electrode (bottom) (Adapted from [90]).

CHARGE STORAGE CAPACITY

Charge storage capacity (CSC) is an important characteristic of stimulation electrodes. CSC is a measure of the total charge available from an electrode for delivering stimulation. It is evaluated using slow-scan-rate cyclic voltammetry (CV) in PBS over a potential range that is within the water electrolysis window for the given electrode. It has become common practice to characterize stimulation electrodes by their cathodic CSC which is the time integral of the cathodic current during the CV scan as depicted in Fig. 2.6 (b) in blue. However, it is important to note that only a fraction of the charge enclosed by the CV is typically available for injection during a short pulse. In practice, only the most superficial layers of the electrode will be actively involved in charge transfer during short stimulation pulses, and the CSC therefore overestimates the charge available [80]

CHARGE INJECTION CAPACITY

Stimulating electrodes allow the exchange of charge carriers in the biological medium. However, this process should not induce irreversible reactions that alter the electrode material.

As mentioned previously, faradaic reactions at the electrode interface can corrode or degrade the electrode. However, reactions where the products remain bound to the surface have a high degree of reversibility. Water electrolysis is one irreversible faradaic reaction that can be generated by any electrode. This reaction results in the formation of oxygen or hydrogen gas and local pH changes, which may damage the electrode and are harmful to the surrounding tissue. Hence, stimulation electrodes are often characterized by their water window. Therefore, maximum charge injection capacity (CIC) is defined as the maximum charge per pulse that can be injected before water electrolysis occurs under either the cathodic or anodic phase.

As shown in Fig. 2.6 (c), a biphasic current pulse is delivered through the working electrode while the voltage at the electrode interface is monitored. The access voltage (Va) is the instantaneous voltage change due to the applied current pulse and it is related to the interface impedance. The maximum cathodic voltage or transient potential (Emc) is measured at the termination of Va in the cathodic phase, where the transient potential begins to decay towards the open circuit voltage. The CIC is then defined as the total injected charge (current multiplied by pulse width) at which Emc reaches the water window limit [80].

2.2.3. OPTICALLY TRANSPARENT CONDUCTIVE MATERIALS

As mentioned, high electrically conductive materials with broadband optical transparency are needed to allow the combination of optical and electrical modalities. There are two categories of conductive transparent electrodes. The first group of materials consists of intrinsically transparent materials and the second group includes non-transparent materials that could be deposited in an ultra-thin film or designed in a specific structure and provide high optical transparency. Some of the materials and methods used for this purpose are discussed in this section.

INTRINSICALLY TRANSPARENT MATERIALS

Indium tin oxide (ITO) is widely used in optoelectronic devices due to its relatively high optical transmittance and very good electrical conductivity. A transparent ITO electrode

array fabricated on a parylene C substrate and integrated with μ-LEDs showed a successful recording of light-evoked signals from the rat visual cortex [91]. However, ITO electrodes suffer from decreased performance under mechanical deformation because of the brittle nature of ITO [3]. Its brittleness might cause microscopic crack formation even under very low tensile strains [92, 93]. Nevertheless, there has been an attempt to create hybrid conductive transparent electrodes combining ITO with graphene to improve its sheet resistance and mechanical stability during bending tests compared to the original ITO electrode [94].

Conductive polymers prepared by solution processes are an emerging material for optoelectronic applications. Polystyrene sulfonate-doped poly(3,4-ethylene dioxythiophene) (PEDOT:PSS) with remarkable flexibility, high CSC, and excellent optical transparency is commonly used as a coating on an electrode site. However, PEDOT is sensitive to oxidizing agents, resulting in electrode performance degradation [95]. It has been observed that the impedance magnitude increases significantly after a high-temperature accelerated aging test due to mechanical delamination of PEDOT from the underlying substrate or electrode [96, 95]. These issues might affect electrode performance in long-term implantable devices.

Carbon-based materials such as carbon nanotubes (CNTs), graphene, and their relatives are also considered intrinsically transparent conductive materials. CNT with high electrical and thermal conductivity, high electron mobility, and excellent mechanical strength has been used as an electrode material itself and also as a coating on electrode sites. Its large surface area leads to improved impedance [97, 98] and CIC [99], which are both important for neural recording and stimulation, respectively. However, there has been significant concern about its cytotoxicity [100, 101].

Among all transparent carbon-based electrodes, graphene is the most attractive material due to its high thermal/electrical conductivity, broad-spectrum transparency, and flexibility [102]. The majority of research on graphene and graphene-related materials concerns graphene-oxide (GO) and reduced-graphene-oxide (rGO) materials. However, due to the electrically insulating properties of GO, its combination with other conductive materials, such as conductive polymers and metals, is necessary to fabricate electrodes. rGO's large effective surface area leads to low impedance and high charge injection capacity [103]. However, its electrical conductivity does not reach that of pristine graphene [104]. More importantly, cytotoxicity concerns towards different types of cells using GO and rGO have been raised recently [105]. Park et al. fabricated a transparent ECoG electrode array that was composed of four stacked graphene monolayers [106]. This electrode exhibited a light transmittance of approximately 90%, which enabled effective stimulation of opsin-expressing neurons underneath the graphene electrodes. Thunemann et al. further developed a graphene micro-electrode array with no light-induced artifact by using residue- and contamination-free single-layer graphene as the electrode material [107].

OPTICALLY TRANSPARENT STRUCTURES

Metal films with high electrical conductivity have been widely employed as electrodes. However, their high optical absorption excludes them as a potential candidate for transparent conductive electrodes. Recently, transparent metallic electrodes with a specific

design such as mesh or grid have been developed for simultaneous optogenetic stimulation and electrical recording. The large voids in these mesh- and grid-type metallic electrodes allow efficient light transmission, leading to the high optical transparency of the electrodes. Qiang et al. fabricated a transparent mesh electrode by patterning gold electrodes and connection lines with polystyrene spheres [108]. The mesh-type gold electrodes showed no artifact under optical stimulation, enabling low-noise electrical recordings of light-evoked activities in an awake mouse.

Metal nanowires [109, 110] and metal nanomeshes [111] prepared by a solution process have also shown high optical transmittance and excellent mechanical stability under thousands of bending cycles. However, their poor adhesion to the substrates, due to the mismatched surface energies, makes the morphology rough and discontinuous, resulting in discrete islands, and consequently a reduction in their optical transmittance and electrical conductivity over time. Therefore, recent research has been focusing on physical and chemical modification of the substrate to improve the adhesion [112].

2.2.4. MRI-COMPATIBLE CONDUCTIVE MATERIALS

As mentioned previously, specific material properties must be taken into account to achieve an MRI-compatible neural interface. There are several potential risks in the presence of metal electrodes in an MRI scanner. First, the applied force from the magnetic field on the ferromagnetic metal electrodes might cause movement and consequently injuries to the surrounding tissue. Moreover, the time-varying radio frequency (RF) field induces an eddy current in the conductive electrode which might lead to undesired neural stimulation or a temperature increase causing a risk to the tissue. Furthermore, the magnetic field distortion caused by the presence of the implant might result in artifacts in MRI images and obstruction of the field of view [113].

To achieve MRI-compatible neural interfaces, several strategies have been introduced including limiting the use of ferromagnetic materials, designing circuits to compensate for the interference of MRI gradient noise during electrical recording, and optimization of MRI parameters [113].

There have been also several methods that can be used in the design of the electrode to ensure MRI compatibility. It has been shown that minimizing the size of implants could cause less magnetic field distortion [114]. However, minimizing the size of implants increases the electrode impedance and consequently reduce the quality of the recorded electrical signal.

There has been also a focus on selecting MRI-compatible materials to reduce MRI artifacts. The formation of MRI artifacts around the implants is due to the magnetic field distortion due to the differences in the magnetic susceptibility of the electrode material and the surrounding tissue. The magnetic susceptibility of a material is its capability to undergo magnetization when placed in an external magnetic field. The absolute value of the magnetic susceptibility of a material is correlated with the distortion to the external magnetic field. Soft tissues such as the brain (−9.2 to −8.8 ppm) [115] have a magnetic susceptibility that is close to that of water (−9.05 ppm). Therefore, neural implants with a magnetic susceptibility that is greatly different from that of tissue cause distortions in the magnetic field that consequently lead to signal loss.

Copper (Cu) has a magnetic susceptibility that is the closest to the one of tissue

(−9.6 ppm) among metals, but it is not a biocompatible material due to its biotoxicity. Since graphite and nano-structured carbon materials can be MRI-compatible, recently, graphene was used to encapsulate a Cu microwire (100 µm G-Cu) to reduce its cytotoxicity. The size of artifacts in T2*-weighted MRI image under 7.0 T magnetic field in a rat's brain was approximately 150 µm which is considered negligible [116].

Graphene fiber (GF) electrodes (with a diameter of 0.17 mm) with excellent electrochemical properties, showed an MRI artifact of 0.7 mm in diameter in echo-planar imaging (EPI) in a 9.4 T scanner while this value for PtIr electrodes was 3 mm. This large artifact around the PtIr electrode resulted in a signal dropout from a significant portion of the rat brain, resulting in a loss of functional response visualization during MRI scans. EPI images are highly sensitive to susceptibility mismatch and the difference in the artifact size in such images can be directly attributed to the differences in magnetic susceptibility [72]. CNT yarn electrodes (with a diameter of 1.3 mm) showed an excellent electrochemical performance and less image artifact compared to the one of a Pt-Ir electrode [117]. A magnetic susceptibility (−5.9 ppm) close to the one of tissue was reported for a CNT forest prepared by means of a CNT templated microfabrication technique, and the MRI image of electrodes in vitro demonstrated a small distortion in the magnetic field [118]. Furthermore, microfabricated glassy carbon (GC) electrodes on flexible polymer substrates demonstrated less MRI artifact in comparison with a Pt electrode in a phantom experiment [119].

Conductive polymers are also considered to be potential candidate materials for neural electrodes, although their exact values of magnetic susceptibility are unknown. An example could be a PEDOT:PSS transparent and MRI-compatible stimulation electrode on a polyimide substrate which exhibited MRI compatibility in a 3 T MRI scanner and also X-ray imaging compatibility [120].

2.3. GRAPHENE AND ITS APPLICATION FOR NEURAL ELECTRODES

2.3.1. GRAPHENE AS AN ELECTRODE MATERIAL

Graphene is chosen as an electrode material for neural interfaces as it shows potential compatibility with MRI and high optical transparency for optical applications in addition to other advantages compared to the other materials mentioned previously. Graphene consists of a two-dimensional (2D) hexagonal network of sp^2 hybridized carbon atoms in a honeycomb lattice as shown in Fig. 2.7 (a). The valence and conduction bands are symmetrically distributed (with respect to the Fermi level) with the intersection at their extremities, forming Dirac cones as shown in Fig. 2.7 (b). This makes graphene a zero band-gap semiconductor, with high electron mobility due to the linear energy dispersion for both electrons in the conduction band and holes in the valence band [121]. Moreover, graphene is mechanically robust and flexible due to the hexagonal bonding of carbon atoms.

A few layers of graphene have high optical transparency of more than 90% in the UV to IR light spectrum required for optogenetic stimulation and optical imaging [122]. Moreover, its optical transmittance is higher than those of ITO (~ 80%) and ultra-thin metals (~ 60%) [106]. In contrast to ITO optical transmittance, graphene has a very flat transmittance spectrum, which makes it suitable for both optogenetics experiments in

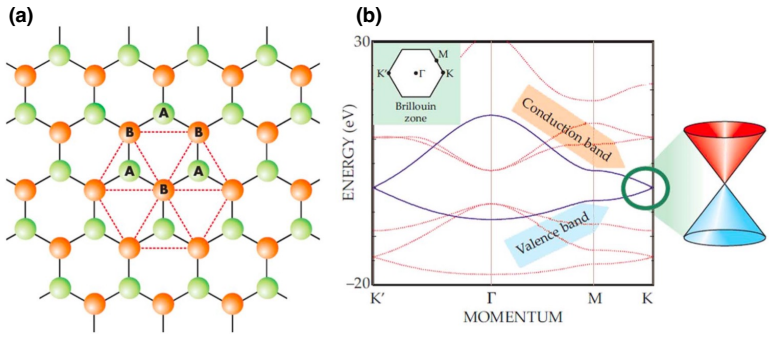

Figure 2.7: (a) Honeycomb lattice of single-layer graphene; (b) Band dispersion of graphene showing the valence and conduction bands touching one another at the K point and the Dirac cone approximation [126]

the blue spectrum and multi-photon imaging in the IR [69]. Recent research presented 1200 µm deep two-photon imaging and artifact-free electrophysiology combined with optogenetic stimulation with a graphene electrode [107].

In addition, there have been various studies on the biocompatibility of graphene demonstrating enhanced adhesion and good viability for neural cells cultured on graphene substrates [123, 124, 125].

Considering both optical transparency and MRI compatibility for the electrode material in addition to other requirements, such as biocompatibility and flexibility, graphene is selected as the electrode material in this thesis.

2.3.2. FABRICATION PROCESS OF GRAPHENE-BASED ELECTRODES

There are various methods to fabricate graphene. Monolayer graphene was discovered in 2004 by means of mechanical exfoliation of graphite using the scotch tape method due to the weak Van der Waals forces between graphene layers [127]. Other techniques, such as epitaxial growth, and chemical oxidation-reduction of graphite have been also developed [128]. Another method as mentioned previously is the CVD process.

CVD enables graphene growth on a catalyst material. Various metals in the form of foils and thin films such as Copper (Cu), Nickel (Ni), and Molybdenum (Mo) have been used as a catalyst [129]. The CVD process starts with the catalyst exposure to high temperatures, ranging from 800 to 1200 ° C, in a vacuum environment. Then, a gas flow with carbon atoms (usually CH_4) is introduced inside the chamber. The carbon atoms are absorbed by the metal catalyst. Then, the temperature drops rapidly, causing the carbon atoms to be pushed from the bulk of the metal to its surface, creating a layer of graphene on top of the catalyst. This method is called precipitation and is shown in Fig. 2.8 [130, 131, 132].

Another possible method for graphene growth in a CVD process is the isothermal method. In this method, graphene can be formed on the catalyst surface due to its supersaturation caused by continuous exposure to hydrocarbon at a constant temperature [133].

Several parameters affect the graphene layer. A higher temperature has been shown

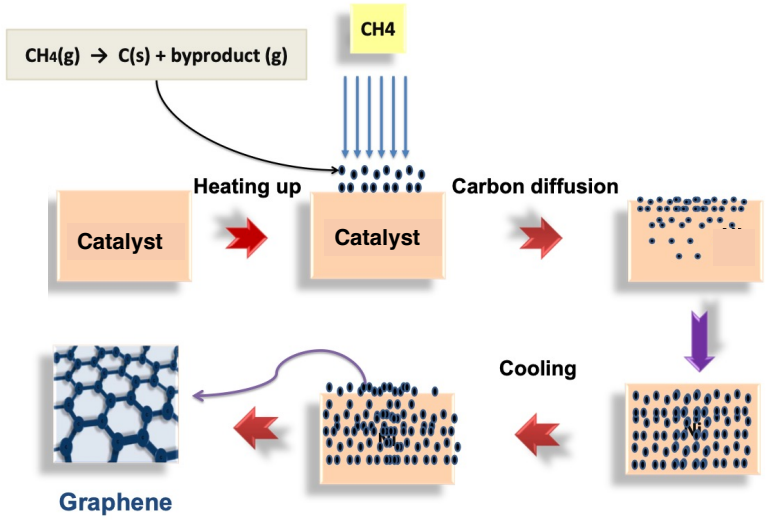

Figure 2.8: Graphene growth process on a catalyst layer, according to the precipitation method (Adapted from [132]).

to grow graphene with lower defect density [129]. The parameters that affect the thickness of graphene are the precursor pressure, catalyst thickness, and exposure time. Furthermore, carbon solubility and diffusibility of the catalyst affect the growth [133].

After graphene growth, it is usually separated from the metal catalyst and transferred onto the desired substrate using a supporting layer as shown in Fig. 2.9. Polymethyl methacrylate (PMMA) is typically coated on top of graphene as a support layer for the transfer process. Then, the metal is etched and the PMMA/graphene film is transferred to the target substrate. Finally, PMMA is removed with acetone [130].

Graphene has been used as an electrode material in a variety of neural interfaces. Graphene electrodes were made of a large graphene piece on PDMS [134, 135]. Recently, the electrodes were fabricated by using a microfabrication process on Borofloat [136,

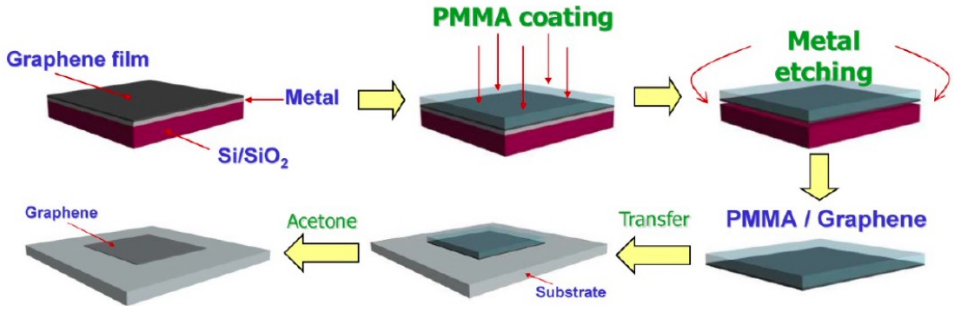

Figure 2.9: Graphene transfer process using PMMA as a supporting layer [130]

137, 138], polyimide [139, 140], parylene-C [106, 69, 70, 141], and polyethylene terephthalate (PET) substrates [107, 54]. Since microfabrication steps are employed, electrodes can be made in a specific design for different applications.

Current state-of-the-art graphene electrode fabrication has been mostly focusing on graphene transfer processes, where graphene is grown on a copper (Cu) catalyst, and subsequently transferred to the required polymer substrate used for the soft implant [139, 141, 138, 70]. The current state-of-the-art fabrication processes and the fabricated electrodes are summarized in Fig. 2.10. The required high temperature (usually ≥ 900 °C) for graphene growth prevents direct graphene growth on Si wafers with already present polymers, a fundamental component of flexible implants. As mentioned previously, polymer supporting layers, such as PMMA, facilitate the transfer process. This method, despite its popularity, has reliability and scaling issues [142] regarding preserving the quality of the material after the transfer, polymer residues from the supporting layer, or an additional cleaning process to remove any polymer residues [107]. Finally, metallic particles from the non-biocompatible Cu catalyst layer can impact the implant's biocompatibility. Apart from that, in such processes, the first polymer layer is present before the graphene transfer. This could limit the electrode post-processing options that have the potential to e.g. improve the conductivity [143].

Other recent techniques employed to fabricate porous graphene electrodes are direct laser pyrolysis of porous graphene on a polyimide substrate [144], or laser carbonization of parylene-C to create graphitic carbon as a coating on metal electrodes [145]. These methods create devices with promising properties for neural stimulation. However, to date, laser pyrolysis fabrication has been successfully used only for devices with relatively large electrodes (200–700 μm diameter). The main limitation of this technology is the laser resolution (i.e., the limited spot size of the laser and the resolution of the software that drives the laser head [144]), in comparison to the resolution achieved by photolithographic methods, crucial for miniaturization and the formation of high-density arrays.

2.3.3. GRAPHENE-BASED ELECTROCHEMICAL CHARACTERISTICS

One of the main problems of graphene-based microelectrodes is their low CSC and large impedance that restricts effective neural stimulation and recording. The CSC can be increased by increasing the number of graphene layers [70] or increasing the porosity of the graphene [144]. The CIC of the porous graphene was reported to reach up to 3.1 mC/cm^2.

However, as mentioned previously, using laser pyrolysis to fabricate porous graphene electrodes has some drawbacks. Apart from laser resolution, low-quality carbon-based electrodes are not highly optically transparent and suffer from reproducibility issues. Furthermore, it is incompatible with CMOS-based technology fabrication processes.

The large electrode impedance of graphene could be attributed to the small quantum capacitance at the interface between the graphene and electrolyte. The quantum capacitance is considered in series to the double-layer capacitance. Metal electrodes have a high quantum capacitance due to the large electronic density of states at the Fermi level. As a result, its contribution to the total capacitance is negligible. However, the quantum capacitance dominates the total capacitance for the monolayer graphene due to the low

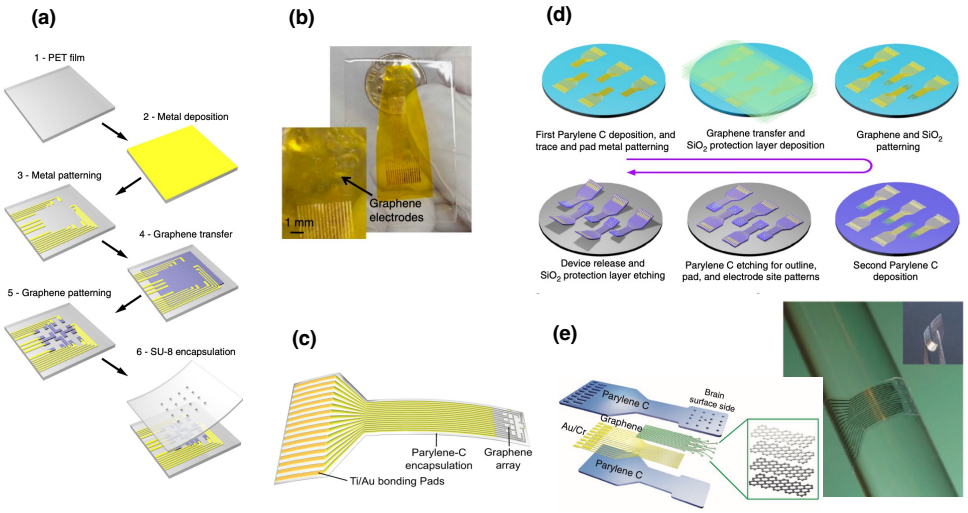

Figure 2.10: (a) Fabrication process used for monolayer graphene electrodes based on transfer process of graphene on PET substrate [107]; (b) Monolayer graphene electrodes fabricated with the same method on polyimide substrate [139]; (c) Two stacked monolayer graphene electrode using transfer process on a parylene substrate [141]; (d) Fabrication process used for four stacked monolayer graphene electrode on parylene substrate [69]; (e) Four stacked monolayer graphene electrode with parylene substrate fabricated with the same fabrication process [106].

electronic density of states at the fermi level [146, 147]. This leads to the dominance of small quantum capacitance, and hence a large electrode impedance. However, it has been shown that the impedance can be drastically decreased if graphene is doped with nitric acid or its surface is modified with carbon nanotubes (CNTs), PtNPs, or PEDOT:PSS [107, 54, 148, 149, 150].

The electrochemical characteristics of the current state-of-the-art graphene electrodes are also summarized in Table. 2.1.

2.4. SURFACE MODIFICATION

As mentioned previously, monolayer CVD graphene with high optical transparency has shown compatibility with optical imaging and optogenetics [107]. However, it suffers from low sheet conductivity in an undoped state [151], large impedance caused by the low electronic density of the state of graphene, and a low CSC due to the dominance of its small quantum capacitance [147]. Stacked four monolayer graphene neural electrodes have demonstrated better electrochemical characteristics than monolayer graphene [106]. However, the electrical characteristics of these graphene electrodes are still not comparable to conventional metal electrodes.

High CSC materials can deliver a higher amount of charge per area of the electrodes to the surrounding tissue for neural stimulation. In addition, low-impedance electrodes are desired to achieve a low-noise recording of neurons according to the thermal (Johnson-Nyquist) noise Eq. 4.1:

Table 2.1: Current state-of-the-art graphene electrodes

Electrodes	Catalyst	Substrate	Calculation	CSC (μC/cm²)					Electrode surface area (μm²)	Water window	CIC (μC/cm²)	Impedance at 1 kHz (kΩ)	Area-normalized impedance (Ω.cm²)	Optical transmittance (%) @550nm	Reference
				1V/s	0.6V/s	0.5V/s	0.2V/s	0.1V/s							
Monolayer graphene	Cu	PDMS	Only CV curve						590,000	-0.3 to 0.6		117 kΩ	690.3		C. H. Chen, 2011
Monolayer graphene	Cu	SU8/PDMS							13,500			5.4 kΩ mm^{-2}			C. H. Chen, 2013
Monolayer graphene	Cu	Quartz							314			170 ± 11.1	0.53 ± 0.035		X. Du, 2015
Monolayer graphene	Cu	Polyimide							314			100 ± 50	0.314 ± 0.157		D. Kireev, 2016
Monolayer graphene	Cu	Si/SiO_2 Borofloat							75			3500 ± 500	2.62 ± 0.38		D. Kireev, 2017
Monolayer graphene (Doped with HNO_3)	Cu	Polyimide	Total					1953	2,500	-0.8 to 0.8		541	13.5	60	D. Kuzum, 2014
Monolayer graphene	Cu	PET	Only CV curve						10,000	-0.6 to 0.8		963	96.3	83	Martin Thunemann, 2018
Porous graphene	-	Polyimide	Cathodic					50,000	62,500	-1.3 to 0.8	3200	5 ± 3	3.125 ± 1.9		Y. Lu, 2016
Monolayer graphene	Cu	Borofloat							310,000		800	10 ± 0.2	31 ± 0.62		B. Koerbitzer, 2016
Few-layer graphene	Cu	Borofloat	Total	910 ± 130					700	-1.6 to 1.4	150 ± 50	2650 ± 260	18.73		B. Koerbitzer, 2019
Two stacked Monolayer graphene (Doped with HNO_3)	Cu	Parylene C	Cathodic			64.44			2,500	-0.8 to 0.8		908 ± 488	22.7 ± 12.2	90	N. Driscoll, 2020
Four stacked monolayer graphene	Cu	Parylene C	Cathodic	87.8					7,854 17,671 31,416	-0.6 to 0.8	57.13	286.4 ± 92.6 248.7 ± 125.0 215.7 ± 120.4	22.5 ± 7.27 43.95 ± 22.09 67.76 ± 37.8	90	D. W Park, 2018
Four stacked monolayer graphene	Cu	Parylene C							17,671- 31,416	-0.6 to 0.8		50-600		90	D. W Park, 2016
Four stacked monolayer graphene	Cu	Parylene C	Only CV curve						31,416	-0.6 to 0.8		243.5±5.9	76.5 ± 1.85	90	D. W Park, 2014
Four stacked monolayer graphene	Cu	SU8/PET							15,394			161	24.8	85	J. Park, 2021
Monolayer graphene (HNO3 doped)	Cu	Si/SiO_2	Only CV curve						2,500	-0.2 to 0.6 in KCl		1500 ± 200	37.5 ± 5	97.7	S. K. Rastogi, 2018

$$\text{Vnoise} = \sqrt{4\text{kTRe(Z)}\Delta\text{f}} \tag{2.1}$$

Where k is Boltzmann's constant, T is the temperature, Re(Z) is the real part of the impedance, and Δf is the frequency band of interest [152, 153].

Moreover, to selectively record signals from the neurons, scaling down the electrodes is necessary which leads to an increase in their impedance. Thus, to obtain low impedance with small-size electrodes, increasing the effective surface area of the electrode using surface modification techniques is of paramount importance. In addition, these techniques should be advantageous for improving the charge transfer properties at the electrode and tissue interface.

Various materials have been applied to modify the surfaces of electrodes, including materials with three-dimensional (3D) topography such as nanoparticles (NPs) [54], CNTs [154], and conductive polymers such as PEDOT [155, 150]. However, as mentioned previously, CNT and PEDOT have their drawbacks such as cytotoxicity and degradation, respectively. This makes them unsuitable for implantable medical devices.

2.4.1. SURFACE MODIFICATION USING NANOPARTICLES

NPs have a larger surface-to-volume ratio compared to bulk material and their surface-to-volume ratio is inversely proportional to the diameter of the NPs. Therefore, deposition of NPs on electrodes can change the effective surface area which leads to lower impedance [156].

Au NPs have been proven to be non-toxic, highly conductive, and biocompatible materials [157]. Therefore, they are widely used in the field of biosensors, multielectrode arrays, and microelectrodes. Graphene with Au NPs has been fabricated by doping graphene surface with $AuCl_3$ [158]. This method showed a greater reduction in sheet resistance than HNO_3 doping, while optical transmittances were similar.

Electrodeposition of Pt NPs on reduced graphene oxide (rGO) [159, 160], and functionalized graphene sheet [161] have been shown to enhance the electroactivity in fuel cell and biochemical sensor applications. Recently, monolayer graphene neural electrodes with electrodeposited Pt NPs showed a reduction in impedance and optical transmittance, and an increase in CSC with increased Pt deposition time [54].

Current techniques mostly used for surface modification of electrodes with NPs require the use of wet chemical processes. The extra steps that are added to the fabrication process of certain electrodes cannot easily be applied to other types of electrodes. Furthermore, single-electrode surface modification is usually not possible and the process does not attain localized deposition. Finally, good control over the size of the NPs is not possible. Therefore, to address these issues, the spark ablation method is used in this thesis to print NPs on the graphene surface. This will be discussed in details in chapter 4.

2.5. STATE-OF-THE-ART ENCAPSULATION METHODS

As mentioned previously, neural interfaces are used to interact with the nervous system, to record, stimulate or block electrical activity. For this purpose, they are implanted close to the targeted region in the wet environment of the human body. To prevent water and

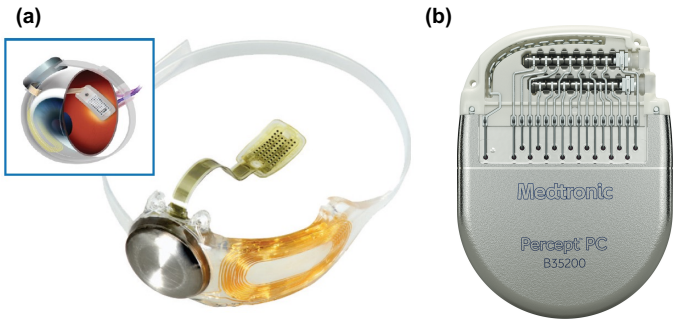

Figure 2.11: (a) Argus II Retinal Implant using a silver case [163]; (b) Medtronic DBS [164].

ion ingress into the implanted electronics, and avoid diffusion of corrosion products to the tissue, it is necessary to protect the implantable device using a biocompatible protective barrier material [162]. Therefore, a long-term reliable packaging or encapsulation technology is needed given that the implants are expected to remain stable, safe, and functional over a certain amount of time.

Inorganic enclosures made of metallic (commonly titanium) or ceramic materials have been employed for the protection of neural implants due to their good hermeticity against water and ions. Two examples of implants with metallic enclosures are shown in Fig. 2.11 [163, 164]. It is of paramount importance to remove any water vapor from inside the enclosure prior to implantation (using heating and vacuum processes) [165]. Any water vapor inside the enclosure might condense to liquid water and cause early failure of the electronics.

The hermeticity of such enclosures is important and can be evaluated using a helium (He) leak test. Consequently, the expected lifetime of the device can be predicted. It should be noted that the tolerable leak rate depends on the desired lifetime of the device and the volume of the enclosure case. However, this measurement method can be challenging for two reasons: First, for many implantable devices, the leak rates are beyond the detection limit. Second, the long-life predictability of small packages with volumes smaller than 1 mm^3 is lost, as slower leaks may not be detectable using the current method of mass spectrometry [166]. Therefore, this conventional packaging method based on titanium or ceramic is not a suitable encapsulation approach for microfabricated neural implants due to their incompatibility with microfabrication processes and difficulties with miniaturization.

Moreover, as neural implants are further miniaturized, targeting millimeter sizes, packaging becomes the limiting factor. Therefore, to ensure that the internal volume available for the enclosed electronics will not be decreased for smaller implants, the packaging thickness must be reduced. While thinner metal cases may maintain sufficient barrier properties, thin-film deposited metals are fragile and prone to micro-cracks causing reliability issues and mechanical strength problems.

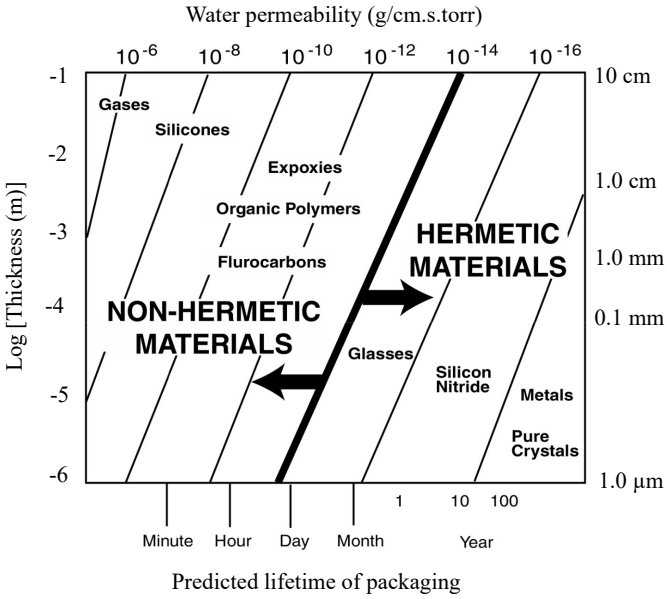

Figure 2.12: Water permeability of different packaging materials ([167])

2.5.1. CONFORMAL ENCAPSULATION

Recent research has been investigating other options based on conformal encapsulation to pave the way toward miniaturization. Conformal encapsulation can be based on organic or inorganic materials or a combination of both. Inorganic materials, such as ceramic/metallic thin films, could provide sufficient hermetic tightness due to their high intrinsic atomic density. However, they tend to form pinholes and cracks on non-uniform substrates. On the other hand, polymeric thin films have proven to be pinhole-free at the micrometer scale but have a lower tightness at the molecular level. A comparison between the water permeability of organic and inorganic materials is shown in Fig. 2.12 [167].

Organic coatings are promising because they contribute to a reduction of the foreign body response. Biocompatible polymers have been selected for soft encapsulation and have shown promising results such as PDMS-coated sacral nerve roots stimulators (Finetech Medical) [168]. Alpha-AMS is a commercially available retinal prosthesis that employs a polymeric encapsulation for a micro-photodiode array. The estimated lifetime of this device, based on clinical results, is 3.3 years [169].

This encapsulation approach relies on achieving good adhesion between the encapsulant and the substrate material and it is, therefore, dependent on process control. Since polymers are permeable to water vapor, water vapor diffuses through the polymers and reaches the interface. Therefore, any contamination site or voids at the interface must be prevented as they might act as a potential failure point, initiate the condensation of water vapor to liquid water, and cause early failure of the device [166].

A hybrid encapsulation approach that aims to exploit the advantages of both cate-

gories of materials is based on the combination of organic and inorganic materials. This method offers the possibility of improving the encapsulation by having one layer compensate for any weakness of the other layer. The thin and still flexible ceramic layers are incorporated between layers of polymers and act as moisture barriers [170, 171]. This approach is mostly based on an attempt to delay failure and to ensure the long-term reliability of the encapsulation [172].

Several materials including inorganic thin-film layers of alumina (Al_2O_3), hafnia (HfO_2), SiO_2, and silicon carbide (SiC), as well as organic polymers such as polyimide (PI), parylene, liquid crystal polymer (LCP), and silicone elastomer, have been used for this reason.

Recently, plasma-assisted atomic layer deposited (ALD) alumina was explored as a moisture barrier layer for encapsulation. Alumina provides a conformal coating with a good water barrier property. However, it suffers from hydrolysis in direct contact with water [173]. Therefore, polymers such as parylene have been used to compensate for the relatively high dissolution rate of alumina. Xie et al. conducted accelerated aging tests at different temperatures on electrodes and interdigitated comb structures (IDC) encapsulated with parylene and parylene-alumina bilayer. The result showed the enhanced lifetime of the alumina/ parylene bilayer (180 days) compared to parylene-only encapsulation (35 days) in an 80 °C saline solution [174, 175, 171, 176]. However, this bilayer encapsulation has not been tested for long-term chronic implants.

ALD-deposited hafnia coating also provides a conformal and pinhole-free coating. The addition of ALD hafnia layers between PI-ALD alumina bilayers (PI/ HfO_2/ Al_2O_3/ HfO_2/ PI) improved the water vapor transmission rate (WVTR) of the PI-only films from 4300 mg/(cm^2·day) to a value below the detection limit of the WVTR measurement tool (0.5 mg/(cm^2·day)), determined by the Mocon method [177, 170, 178].

A bilayer coating of 100 nm thin ALD HfO_2/ PDMS on IDC structure was evaluated in PBS for 450 days at room temperature [179]. Impedance monitoring of ALD-only coated IDCs showed a slight drop, indicating water diffusion through the defects in the ALD layer. However, a stable impedance was observed for the HfO_2/ PDMS encapsulated samples due to the low viscosity of PDMS filling the defects of the ALD layer.

ALD-deposited hafnia and a hybrid parylene-ALD multilayer (Al_2O_3/ TiO_2) stack were both employed for the coating of LCP-based flexible implants with a silicone finish in both cases in comparison with only LCP samples. The accelerated aging test at 60 °C under a 14V DC bias for more than 16 months showed a stable impedance for the first group of samples. The results showed that the adhesion of the coating to the substrate materials plays a key role in maintaining a stable interface and thus longer lifetimes [180].

Recently, aluminium (Al) IDCs coated with different passivation layers (SiO_x, SiO_xN_y, SiO_xN_y + SiC) using plasma-enhanced chemical vapor deposition (PECVD) were encapsulated in medical grade silicones. No silicone delamination, passivation dissolution, or metal corrosion was observed for (SiO_xN_y + SiC)/silicone samples during aging in PBS at 67°C for up to 694 days under a 5 V biphasic waveform. However, a resistance reduction by an order of magnitude was observed for SiO_x/ silicone samples due to the hydration of SiO_x. These results demonstrate that silicone encapsulation offers excellent protection to thin-film conducting tracks when combined with appropriate inorganic thin films [181].

In fact, SiO_2 is known to slowly dissolve by hydrolysis in a saline solution with varying

dissolution rates depending on the deposition method. Accelerated aging of the thermally grown SiO_2 at different temperatures (~ 1100 °C) showed dissolution rates of 80 nm/day at 90 °C, which can be extrapolated to a few decades of a lifetime at body temperature with a 1 µm-thick film [182]. Additionally, thin layers of SiO_2 have been used in combination with pinhole-free and stress-releasing parylene-C. These layers were deposited in a single-chamber process, combining CVD and PECVD technologies. The adapted calcium mirror test revealed that the use of parylene-C layers containing three SiO_x interlayers leads to a considerably lower liquid water permeation as compared to pure parylene layers having the same thicknesses [172].

Silicon carbide (SiC) deposited by sputtering or PECVD has good barrier properties against diffusion and dissolution in saline. An accelerated aging test of SiC films deposited by PECVD (at 200 to 400 °C) in 90 °C in PBS showed a dissolution rate of 0.1 nm/h, which was ten times less than that of SiO_2 (1 nm/h) and Si_3N_4 (2 nm/h) under the same aging conditions. Moreover, aging the SiC layer at 37 °C over 40 weeks did not result in any thickness reduction [183].

So far, the hybrid encapsulation method showed promising soak test results. However, other characterization such as the long-term reliability tests under DC bias and chronic in vivo test has to be studied to further evaluate such encapsulation methods.

2.5.2. ENCAPSULATION REQUIREMENTS

The optical transparency and MRI compatibility should also be investigated for the encapsulation layer. The optical transparency of the encapsulation layer is of paramount importance for optogenetics and optical imaging methods. Therefore, high optical transparency to wavelengths ranging from 450 nm to 850 nm is aimed for.

Regarding MRI compatibility, Matthias C. Waplera et al. measured the magnetic susceptibility of a large collection of polymers and glasses, providing a useful reference for selecting materials applied in MRI-compatible devices. According to the authors, polymethylmethacrylate (PMMA) (−7.609 to −7.59 ppm) and PI (−5.57 ppm) are recommended as MRI-compatible materials as well as two elastomers which are polyurethane (PU) (−8.35 ppm) and PDMS, whereas some of the materials widely used in neural implants, such as parylene-C, were not mentioned in the article [184].

2.6. SUMMARY AND CONCLUSIONS

In conclusion, the proposed platform technology for multimodal neural interfaces should provide high optical transparency over a broad wavelength spectrum and MRI compatibility. This allows combining different stimulation and recording modalities with a lower risk of artifacts and interference. The material used for electrodes should meet the requirements that have been detailed in this chapter. The electrode should have high electrical conductivity, high optical transparency, and MRI compatibility. Graphene has been shown to be a potential candidate for the electrodes. However, there are some problems regarding the current fabrication process used for graphene-based neural interfaces and their electrochemical characteristics. Besides, a comparison between graphene electrodes with the current state-of-the-art conventional metal electrodes is missing.

Moreover, an encapsulation material needs to be introduced for such multimodal

platform technology that can be fabricated on a miniaturized device, has high optical transparency, and ensures the long-term performance of the device.

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3

TRANSFER-FREE MULTILAYER GRAPHENE NEURAL INTERFACE

Parts of this chapter have been published in [1].

This chapter discusses a multimodal platform technology for graphene-based neural interfaces and presents the proposed wafer-scale transfer-free fabrication process and the results regarding the electrode characterization. The following sections are based on a published article in the Journal of Microsystems and Nanoengineering, therefore, repetitions are unavoidable. Additional information that might be useful for a better understanding of the fabrication process and characterization, which was not included in the article, is added at the end of this chapter.

3.1. MULTIMODAL GRAPHENE-BASED NEURAL INTERFACES

Abstract: Multi-modal platforms combining electrical neural recording and stimulation, optogenetics, optical and magnetic resonance (MRI) imaging are emerging as a promising platform to enhance the depth of characterization in neuroscientific research. Electrically conductive, optically-transparent, and MRI-compatible electrodes can optimally combine all modalities. Graphene as a suitable electrode candidate material can be grown via chemical vapor deposition (CVD) processes and sandwiched between transparent biocompatible polymers. However, due to the high graphene growth temperature ($\geq 900\,^{\circ}C$) and the presence of polymers, fabrication is commonly based on a manual transfer process of pre-grown graphene sheets, which causes reliability issues. In this paper, we present CVD-based multilayer graphene electrodes fabricated using a wafer-scale transfer-free process for use in optically transparent and MRI-compatible neural interfaces. Our fabricated electrodes feature very low impedances which are comparable to those of noble metal electrodes of the same size and geometry. They also exhibit the highest charge storage capacity (CSC) reported to date among all previously fabricated CVD graphene electrodes. Our graphene electrodes did not reveal any photo-induced artifact during 10-Hz light pulse illumination. Additionally, we show here, for the first time, that CVD graphene electrodes do not cause any image artifact in a 3T MRI scanner. These results demonstrate that multilayer graphene electrodes are excellent candidates for the next generation of neural interfaces and can substitute the standard conventional metal electrodes. Our fabricated graphene electrodes enable multi-modal neural recording, electrical and optogenetic stimulation, while allowing for optical imaging, as well as, artifact-free MRI studies.

3.2. INTRODUCTION

Neural interfaces are tools that enable bidirectional interactions with the human nervous system. To allow for personalised therapies, which is the ultimate goal of bioelectronic medicine, the functional neural behaviour has to be well understood. Conventional neural recording and stimulation methods provide insufficient spatio-temporal resolution for neuro-scientific research [2]. In addition, it is of paramount importance to monitor neural activity systematically to uncover the interconnections between the neurons and neural clusters. In recent years, several methods such as optical imaging (e.g. calcium or fluorescence imaging) [3, 4], optogenetics [4, 5], and magnetic resonance imaging (MRI) [6, 7] have emerged to assist neuroscientists to decipher the neural structure and function. These, combined with electrical neural recording and stimulation in a multi-modal fashion, can pave the way towards a much deeper understanding

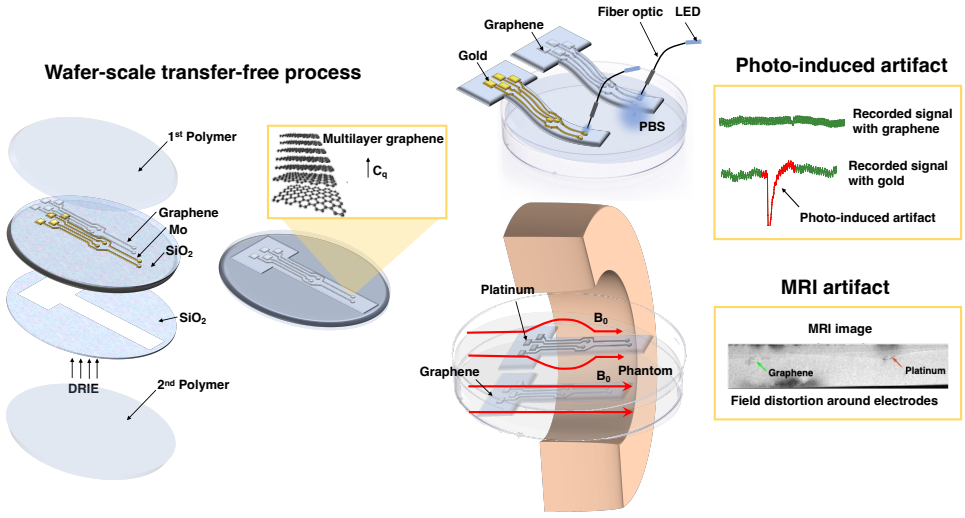


Figure 3.1: Graphical abstract

and mapping of the nervous system [4, 5, 8].

Conventional noble metal electrodes, such as gold (Au) or platinum (Pt), are the most common tools for recording neural activity and stimulating neurons due to their good electrical performance, high biocompatibility, and chemical stability. However, due to their opaque nature, they prevent any *in vivo* optical imaging at the site of stimulation (underneath the electrodes). In addition, due to photoelectrochemical effects, Au electrodes might produce photo-induced artifacts when used for electrophysiology in optogenetic devices [9, 10]. Platinum-iridium (Pt-Ir) alloy electrodes, on the other hand, cause image artifacts in MRI due to the magnetic susceptibility of Pt being different from that of the surrounding tissue [11, 12].

Therefore, there is a need for optically transparent and MRI-compatible electrodes. Indium-Tin-Oxide (ITO) and carbon-based electrodes are the most commonly used transparent conductive electrodes. However, ITO cannot be used in flexible devices due to its brittleness that might cause crack formation [13, 14, 15]. Among all transparent carbon-based electrodes, graphene is the most attractive material due to its high thermal/electrical conductivity, broad-spectrum transparency, and flexibility [16]. In addition, graphene-coated copper wires [17] and graphene-fibre electrodes made of graphite oxide [18] have been proven to be MRI compatible due to their magnetic susceptibilities being close to that of tissue. Therefore, graphene has the potential to be the ideal electrode material candidate for the next generation of optically transparent, and MRI-compatible multimodal neural interfaces.

The majority of research on graphene-related materials concerns graphene-oxide (GO) and reduced-graphene-oxide (rGO) materials. However, due to the electrically insulating properties of GO, its combination with other conducting materials, such as conductive polymers and metals, is necessary to fabricate electrodes. rGO's large effective surface area leads to low impedance and high charge-injection capacity (CIC) that are

both important for neural recording and stimulation [19]. However, its electrical conductivity does not reach that of pristine graphene [20]. More importantly, a cytotoxicity concern towards different types of cells using GO and rGO has been raised recently [21].

The most common fabrication method for growing graphene is chemical vapor deposition (CVD) which has the advantage of simplicity and the possibility to create high-quality graphene on a metal catalyst that can span a large surface area [22]. However, the required high graphene growth temperature (usually $\geq 900\,^{\circ}C$) prevents direct graphene growth on wafers with already present polymers, a fundamental component of flexible implants. Therefore, current state-of-the-art graphene electrode fabrication has been mostly focusing on graphene transfer processes, where graphene is grown on a copper (Cu) catalyst, and subsequently transferred to the required polymer used for the implant [23, 24, 25, 26]. Sacrificial polymer supporting layers, such as polymethylmethacrylate (PMMA), facilitate the transfer process. This method, despite its popularity, has reliability and scaling issues [27] regarding preserving the quality of the material after transfer, polymer residues from the supporting layer, or an additional cleaning process to remove any polymer residues [28]. Finally, metallic particles from the, typically, non-biocompatible Cu catalyst layer can impact the implant's biocompatibility. Apart from that, in such processes the first polymer layer is present before the graphene transfer. This limits the electrode post-processing options that have the potential to e.g. improve the conductivity [29].

Other techniques to fabricate graphene electrodes, such as direct laser pyrolysis of porous graphene on a polyimide substrate [30], or laser carbonization of parylene-C to create graphitic carbon as a coating on metal electrodes [31], have also been reported. However, to date, laser pyrolysis fabrication has been successfully used only for devices with relatively large electrodes (200–700 μm diameter). The main limitation of this technology is the laser resolution, in comparison with the resolution achieved by photolithographic methods, crucial for miniaturization and the formation of high-density arrays. In addition, these low-quality carbon-based electrodes are not highly optically transparent and suffer from reproducibility issues.

Therefore, using CVD graphene is, so far, the best approach for developing neural electrodes. CVD graphene itself can be created as a monolayer or multilayer, depending on the metal catalyst and the process parameters used [32]. Although monolayer graphene has shown compatibility with neuro-imaging and optogenetics [28], previously reported works suggest that monolayer graphene in an undoped state suffers from low sheet conductivity [33]. This prevents the use of graphene instead of long metal tracks, reducing the total implant transparency. Moreover, graphene made of fewer layers is more prone to damage during the fabrication and implantation processes.

On the other hand, increasing the number of graphene layers reduces the sheet resistance but also reduces the optical transparency [34, 35]. Recent research in the field of supercapacitors showed that multilayering of graphene (up to a threshold of 4 to 6 layers) could result in higher electrochemical capacitance [36], and previously reported stacked four monolayer graphene neural electrodes have demonstrated good electrochemical characteristics [37]. However, literature suggests that adding graphene layers in a transfer-based process requires more transfer steps, which, in turn, leads to more polymer residues between layers and therefore lower optical transparency [35].

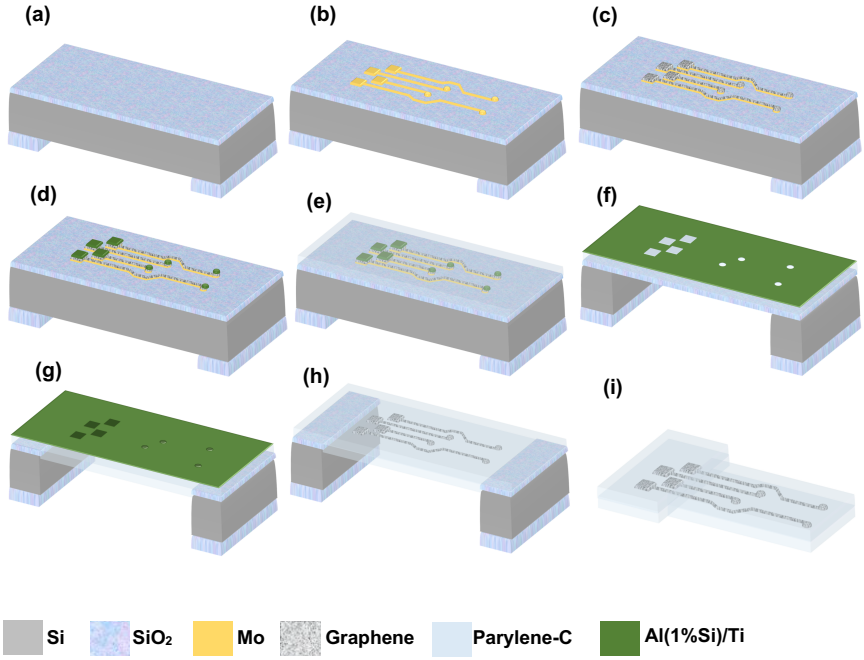


Figure 3.2: Fabrication process steps (a) Oxide deposited on both sides of a DSP Si wafer, patterned and etched on the backside, (b) Mo deposition and pattern, (c) Graphene growth, (d) Al (1%Si)/Ti deposition and pattern on the electrodes and contact pads, (e) Parylene-C deposition, (f) Al/Ti hard mask deposition and pattern for parylene etching followed by a DRIE process, (g) Front-side oxide removal followed by Mo wet etching, second parylene deposition on the back side, and parylene etching on the front side, (h) Hard mask wet etching, (i) Cutting the sample

The aim of the current study is to use CVD multilayer graphene to create fully-transparent and MRI-compatible neural electrodes with better electrochemical performance. To prevent the presence of polymer residues caused by the transfer process, but also, to make the process more compatible with conventional wafer-scale fabrication and post-processing technologies, we have adapted the process reported in [38], which uses a transfer-free method to grow graphene on a Molybdenum (Mo) catalyst [39], to create the neural electrodes. This method enables the fabrication of a multilayer graphene electrode without any transfer involved. The electrodes' impedance, charge storage capacity (CSC), and CIC are assessed and compared to Pt and Au electrodes with the same size and geometry. In addition, the developed electrodes were assessed for compatibility with optogenetic stimulation and MRI, versus Au and Pt electrodes, respectively.

3.3. METHODS

3.3.1. FABRICATION PROCESS

SUSPENDED GRAPHENE ELECTRODE

Multilayer graphene neural electrodes were fabricated as illustrated in Fig. 3.2.

First, 2 µm and 4 µm plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited on the front-and backside of a double-sided polished (DSP) 100 mm silicon (Si) wafer (Fig. 3.2 (a)). The backside oxide is patterned and etched to define the area for a subsequent deep reactive ion etching (DRIE) step. Next, 50 nm molybdenum (Mo) is sputter-deposited at 50 °C on the frontside of the wafer, which serves as the catalyst metal layer for graphene growth. After Mo deposition, lithography steps are employed to define the final design of the electrode array and tracks (Fig. 3.2 (b)). Etching of the Mo layer is then performed at 25 °C using an ICP etcher with 50 W RF power, 500 W ICP power, 5 mTorr pressure, and 30 and 5 sccm Cl_2 and O_2 gas flows, respectively. Graphene is selectively grown on Mo as shown in Fig. 3.2 (c) using a CVD process (Aixtron Black Magic Pro tool) at temperatures of about 935 °C using 960, 40, and 25 sccm of Ar, H_2, and CH_4 gas flows, respectively, at 25 mbar pressure for 20 min and cooled to room temperature under an Ar atmosphere.

The flexible, polymeric-based encapsulation is added in the next step and subsequently the electrodes and contact pads are exposed. A layer of aluminium (Al) is needed to prevent damaging the graphene layer while etching the polymer over the electrodes and contact pads. However, since the adhesion of Al to graphene is poor, an additional titanium (Ti) layer, due to a better microstructure of the film [40], is needed to act as an adhesion promoter. Hence, prior to polymer deposition, the Al (1%Si)/Ti stack (100 nm of Ti, followed by 675 nm of Al) is sputtered at 50 °C on top of the existing graphene layer and photolithographically patterned (wet etching performed using a 0.55% hydrofluoric acid (HF) solution) to cover the graphene features (Fig. 3.2 (d)).

Then, 10 µm of parylene-C is CVD deposited at room temperature (using a SCS PDS 2010 parylene coater) (Fig. 3.2 (e)). Next, in preparation for the upcoming polymer etching step, a hard mask of 500 nm/100 nm Al (1%Si)/Ti is sputter-deposited (at 1 kW, 25 °C) and patterned (dry etched at 25 °C using an ICP etcher with 50 W RF power, 500 W ICP power, 5 mTorr pressure, and 30 and 40 sccm Cl_2 and HBr gas flows, respectively, with a long over-etching time with 15 and 30 sccm Cl_2 and HBr gas flows, respectively, to remove potential Al particles from the polymer layer) (Fig. 3.2 (f)). The hard mask deposition temperature is intentionally kept low to prevent exceeding the parylene glass transition temperature and avoid crack formation.

Finally, a DRIE process on the backside of the wafer lands on the frontside oxide (Fig. 3.2 (g)), which is then plasma-etched (using an AMS110 etcher (Alcatel) with 300 W RF power, and 17, 150, and 18 sccm C_4F_8, He, and CH_4 gas flows, respectively). Mo is removed at this stage by wet etching in hydrogen peroxide (H_2O_2). Graphene will not be accidentally removed in this step as it has already adhered well to the top polymer. Subsequently, the second parylene layer is deposited on both sides of the wafer encapsulating the implant.

To remove the second deposited parylene layer on the frontside and expose the electrodes and contact pads, the frontside parylene is plasma-etched (using the AMS110 etcher (Alcatel) with 40 W LF power, 15 sccm of SF_6 and 185 sccm of O_2), landing on the Al protective layer, which is then, together with the hard mask, removed in 0.55% HF (Fig. 3.2 (h)). At this point, the graphene layer sandwiched between two layers of parylene-C with exposed graphene on the electrodes and contact pads is ready to be cut out of the Si frame (Fig. 3.2 (i)).

Details of the mask design used for the electrode arrays can be found in Fig. S1.

GRAPHENE, PT AND AU ELECTRODES ON SI

For rapid prototyping and to investigate and compare the electrode properties of graphene with those of Pt and Au of similar size and geometry, non-suspended devices were fabricated. For this version, parylene insulation is substituted by photoresist to simplify the processing. The fabrication process for these devices is shown in Fig. S2 and Fig. S3, for graphene and metal (Pt and Au) electrodes, respectively. To contact the electrodes, stainless steel wires are attached to the contact pads using silver (Ag) ink, subsequently covered with a drop of polydimethylsiloxane (PDMS) to enhance the mechanical stability.

For the graphene variant, the devices are at this point placed inside a H_2O_2 bath to remove Mo only on the electrodes. The Mo is kept on the contact pads to make a better contact with the attached metal wire.

3.3.2. ELECTRODE CHARACTERIZATION

SHEET RESISTANCE AND OPTICAL TRANSMITTANCE

Different growth times (20, 40, and 60 min) were used to create graphene with various thicknesses. Longer growth times result in a larger number of layers. To compare these, both their sheet resistance and optical transmittance are measured. For the sheet resistance, Van der Pauw structures were made, and four-point probe measurements were performed with a Cascade Microtech probe station (see Fig. S4 for more details).

To evaluate the optical transmittance, graphene sheets were grown and transferred to a glass microscope slide (details on the transfer method can be found in Fig. S5). The optical transmittance measurement was conducted using a Perkin Elmer Lambda 950 UV/Vis spectrophotometer (PerkinElmer, Waltham, Massachusetts). The wavelength range for the measurement was from 300 nm to 900 nm. Reference measurements were also performed for only the glass slide. The number of graphene layers can be calculated from the optical transmittance by calculating the total absorbance of the multilayer graphene and comparing it with 2.3% absorbance of a monolayer graphene [41, 42].

To evaluate the quality of a transparent conductive film, a figure of merit (FOM) is used; it is calculated for all graphene thicknesses based on the optical transmittance (T) at 550 nm wavelength and the sheet resistance (R_{sh}) and can be found in the Supplementary Notes.

ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY

Electrochemical impedance spectroscopy (EIS) was used to assess the electrochemical properties of the electrodes. The measurements were performed in phosphate-buffered saline (PBS) in a three-electrode set-up with a Pt electrode (3 mm diameter (BASI Inc.)) as a counter electrode (CE), a leakless miniature silver/silver chloride (Ag/AgCl) (eDAQ) as a reference electrode (RE), and the graphene, Au and Pt electrodes fabricated in this work as the working electrodes (WE). The setup was kept inside a Faraday cage during the measurements. All the electrodes were connected to a potentiostat (Autolab PGSTAT302N) that applied a 10 mV RMS sinusoidal voltage between the WE and the RE and measured the current between the WE and the CE [43]. Finally, the impedance magnitude and phase were plotted over frequencies ranging from 1 Hz to 100 kHz.

CYCLIC VOLTAMMETRY

Cyclic Voltammetry (CV) is frequently used to calculate the amount of charge that an electrode can inject into the tissue [44]. This measurement was also performed using the same three-electrode setup. The water window for graphene was chosen from -0.8 V to 0.6 V and used as the CV potential range. As the charge storage capacity (CSC) highly depends on the scan rate, the measurements were performed with various scan rates (0.1 V/s, 0.2 V/s, 0.6 V/s, and 1 V/s). Both the total and cathodic CSC were calculated.

VOLTAGE-TRANSIENT MEASUREMENTS

Voltage-transient measurements are used to estimate the maximum charge that can be injected by means of a constant current stimulation pulse [43, 44, 45]. The voltage transient was recorded in the same three-electrode configuration by applying a cathodic-first biphasic symmetric current pulse between the WE and CE (1 ms pulse width, 100 µs interphase delay) in the PBS solution. In the voltage transients between the WE and the RE, an immediate resistive potential drop (access potential (Va)) is observed at the onset of the cathodic pulse followed by a gradual potential decrease due to the capacitive charging of the electrode-tissue interface. The potential reaches its minimum value at the end of this pulse. The interface polarization (Ep) is evaluated by eliminating the resistive potential drop from this minimum potential (Ep = Emin - Va). Next, the applied current amplitude is increased until the interface polarization reaches the cathodic water window extracted from the CV measurement. It should be noted that the anodic interface polarization must also not exceed the anodic water window. Finally, the maximum cathodic CIC of the electrode is calculated based on the maximum current amplitude multiplied by the pulse width and divided by the electrode surface area [45].

PHOTO-INDUCED ARTIFACT TEST

When shining light on the metal electrode, electrons from the metal surface might be ejected and a small transient potential is created that could interfere with the recorded signal from the neurons. This signal is created due to the photoelectrochemical effect and is called a photo-induced artifact [9, 10].

Here, we tested our multilayer graphene in comparison with gold electrodes using an optical fiber coupled with an 470 nm LED. The setup used for this test is shown in Fig. S6. A safe range of light stimulation intensity for *in vivo* experiments is up to ~75 mW/mm^2 for short pulses from 0.5 to 50 ms [46]. In this experiment, rhythmic rectangular pulse stimulation with 10 ms pulse duration at 10 Hz and 50 mW/mm^2 light intensity was applied to both graphene and the Au electrodes while immersed in a PBS solution. The power spectrum of the recorded signal was investigated for light-induced artifacts. In addition, this test was performed for three different graphene thicknesses to compare the effect of thickness on the produced artifact.

MRI COMPATIBILITY TEST

To investigate the MRI compatibility of multilayer graphene and Pt electrodes, samples were prepared as follows. To simulate a brain-tissue environment, a phantom was prepared by dissolving 1 g agarose in 100 ml PBS in a Petri dish, where the suspended graphene (Fig. 3.2) and Pt electrodes were subsequently immersed, and any bubbles were removed using a Q-tip. Finally, the phantom was solidified and placed in a water

bath to mitigate the effect of susceptibility artifacts at the edge of the phantom caused by the phantom-air interface to be able to detect potential artifacts from the electrodes.

An image artifact is usually detected as a specific signal dropout that clearly obstructs a portion of the image around the electrodes and prevents visualization of brain structures where neural signals are recorded, or electrical stimulation is applied. The MR images of the phantom were acquired with a clinical 3 T scanner (Philips Ingenia, Best, The Netherlands). The following sequences were used to acquire MRI images: (1) High resolution 3D T2*-weighted dual-echo gradient recalled echo (GRE) sequence; (2) Multi-slice GRE sequence with single-shot EPI (echo-planar imaging) readout; (3) Low resolution T2* mapping performed with a multi-echo GRE sequence; (4) Ultra high resolution B_0 mapping based on multi-echo GRE phase imaging.

B_0 maps are analyzed to quantitatively assess B_0 field distortion introduced by the electrodes. A region-of-interest (ROI) is defined to detect the field shifts induced by the electrodes. Then, a background field removal (BFR) method is performed using a high-pass or Gaussian filter with a standard deviation of 23 to remove the field distortions originating from outside of the ROI. The sequences and their corresponding parameters to acquire the MRI images are provided in detail in Table. S1.

3.4. RESULTS

3.4.1. FABRICATED DEVICES

The final suspended graphene electrode with parylene substrate is shown in (Fig. 3.3 (a)). The polymer layer can also be substituted with PDMS based on the application and its required mechanical properties. The suspended graphene electrode with a larger number of electrodes and contact pads with PDMS substrate is shown in (Fig. 3.3 (b)).

Optical images of the 340 µm diameter electrodes before and after Mo removal are shown in Fig. 3.3 (c). The holes on the electrode surface are related to the mask design leaving the device with a surface area of 68320 μm^2 as explained in Fig. S1.

Raman spectroscopy using a laser with a 633 nm wavelength on the electrode surface was performed after Mo removal to confirm the presence of graphene on the electrode surface. As shown in Fig. 3.3 (d), three distinct peaks can be observed: a D peak (grey) at 1337 cm^{-1} with a full-width at half maximum (FWHM) of 61.02 cm^{-1}, a G peak (green) at 1586 cm^{-1} related to the sp^2 C-C bonds forming the graphene lattice and having a FWHM of 33.32 cm^{-1}, and a 2D peak (yellow) around 2670 cm^{-1} with a FWHM of 62.20 cm^{-1}. The ratio between the intensities of the D and the G peaks (I_D/I_G = 0.38) indicates the defects in the graphene layer, which in this case indicates a low number of defects after Mo removal. This ratio matches with the reported values for graphene on Mo for gas sensing applications [47]. The ratio between the intensities of the 2D and the G peaks (I_{2D}/I_G = 0.74) confirms the presence of multilayer graphene as the ratio is less than 1 [41]. In addition, from the shape of the single-peaked 2D band, it can be postulated that the graphene is turbostratic [48, 49].

3.4.2. SHEET RESISTANCE AND OPTICAL TRANSMITTANCE

The sheet resistance (R_{sh}) was measured on 27 Van der Pauw structures for different graphene growth times. The average (plus sign) values for R_{sh} are depicted in the box

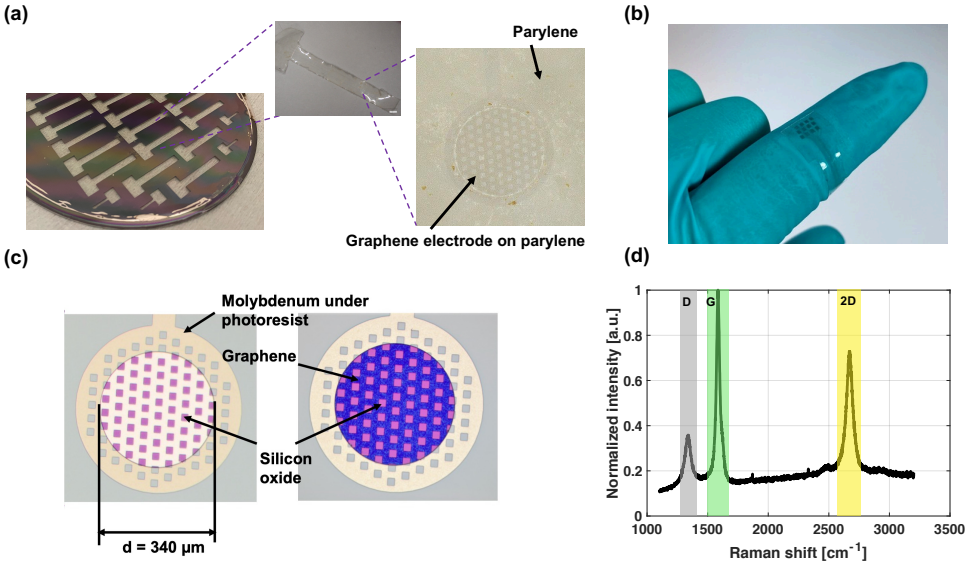


Figure 3.3: (a) Suspended graphene electrodes with parylene-C substrate, (b) Suspended graphene electrode with PDMS substrate, (c) Optical image of the electrode before (yellow) and after (blue) Mo removal, (d) Raman Spectroscopy on graphene electrodes

plot in Fig. 3.4 (a) and reported in the Table. 3.1 for 20, 40, and 60 min graphene growth times. There was a strong correlation between the R_{sh} and the location on the wafer for all conditions. The structures in the centre of the wafer showed the lowest R_{sh}, and the structures towards the edge showed higher R_{sh}. This is possibly due to the single zone heating element in the chamber causing a higher temperature close to the centre of the wafer, which results in thicker graphene with a lower defect density.

Furthermore, the average R_{sh} was lower for a longer growth time. The variation of the R_{sh} over the wafer was smaller for the graphene with a longer growth time. That could be explained by the isothermal growth process of graphene, which indicates that with the increased thickness of graphene, the growth rate is slower as carbon has to diffuse through a thicker carbon layer. It has recently been shown for graphene grown on a Nickel (Ni) catalyst that the rate of isothermal graphite growth slows down with increasing exposure time, which might be due to the increased coverage of the catalyst surface with graphite that blocks the precursor supply from the Ni catalyst [50]. Another explanation is the low solubility of Mo (0.0026 weight % at 1000 °C) for carbon atoms. Mo will be saturated faster in the middle, and thus the thickness will not increase further. Therefore, we postulate that with a longer growth time, the thickness of the graphene on the edges of the wafer becomes more similar to the thickness in the centre.

Optical transmittance measurements performed on graphene grown 20, 40, and 60 min after removing the contribution of the glass slide are shown in Fig. 3.4 (b). The optical transmittances for graphene at 550 nm are presented in Table. 3.1. The optical transmittance at 550 nm is typically used for the calculation of graphene number of layers [42]. According to these measurements, 20, 40, and 60 min graphene growth times lead

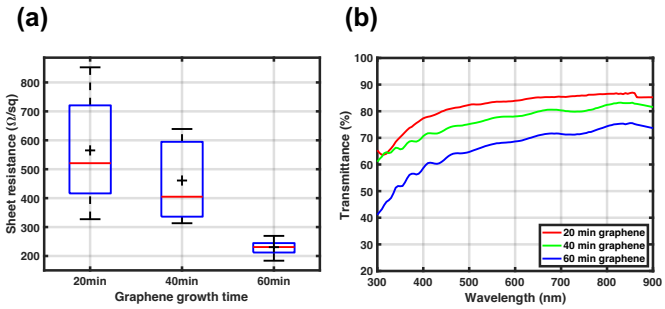


Figure 3.4: (a) Sheet resistance of three different graphene recipes (growth time: 20, 40 and 60 mins) showing the maximum, upper quartile, median (red line), average (plus sign), lower quartile, and minimum values, (b) Optical transmittance measurements for different graphene growth times (the effect of the glass substrate is removed).

Table 3.1: Graphene with 3 different growth times with measured optical transmittance, calculated number of layers, sheet resistance, and FOM

Growth time	T (%) @ 550 nm*	No. of layers	R_{sh} (Ω/sq)	FOM
20 min	83.5	7	565	3.53
40 min	77.6	10	461	3
60 min	67.5	17	230.5	3.76

* These values were calculated for only graphene layers after removing the contribution of the glass layer.

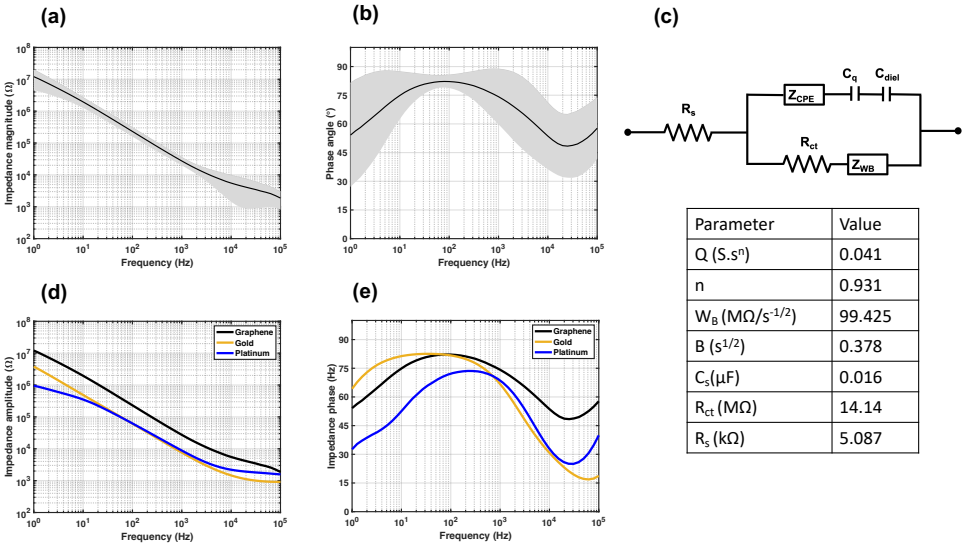
to ~ 7, 10, and 17 graphene layers, respectively. These confirm that increasing the growth time increases the thicknesses of graphene and reduces the optical transmittance.

The calculated FOM is reported in Table. 3.1 for three different growth times. These values are comparable with the result reported for CVD graphene [51] and also higher than the theoretical value of (2.55) calculated from the same equation for an undoped monolayer graphene in [52]. Finally, a 20 min graphene growth time was chosen for the final electrode to achieve a higher optical transparency.

3.4.3. ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY

EIS measurements were performed on 15 graphene electrodes with 20 min growth time, and the obtained graphs can be found in Fig. 3.5 (a,b).

In the Bode plots, the deviation from the average impedance and phase is shown in the shaded grey area. This could be related to slight variations of graphene growth over the Si wafer. EIS measurements were performed for 3 graphene electrodes with 40 min growth time and 3 electrodes with 60 min growth time as shown in Fig. S7. To be able to draw a conclusion a larger number of samples is needed as there are noticeable variations in the impedance at 1 kHz.



Parameter	Value
Q (S.s^n)	0.041
n	0.931
W_B (MΩ/s$^{-1/2}$)	99.425
B (s$^{1/2}$)	0.378
C_s(μF)	0.016
R_{ct} (MΩ)	14.14
R_s (kΩ)	5.087

Figure 3.5: (a) Average impedance magnitude and (b) Phase angle plots (± standard deviation shaded in grey) for fifteen graphene electrodes, (c) Proposed equivalent circuit model for the multilayer graphene electrode and the average values of the parameters used in the equivalent circuit model, (d) Impedance magnitude and (e) Phase angle plots for fifteen graphene electrodes in black (average values), Au electrodes in orange, and Pt electrodes in blue. All electrodes are of the same size and geometry.

The proposed equivalent circuit model for multilayer graphene electrodes is shown in Fig. 3.5 (c). In this model, R_s is the resistance of the solution, Z_{CPE} is the constant phase element representing the Helmholtz double layer capacitance. R_{ct} is the charge-transfer resistance used to simulate Faradaic reactions and Z_{WB} is the bounded Warburg impedance used to simulate the diffusion process.

It was found that the double layer capacitance for graphene is in series with the quantum capacitance (C_q) caused by the limited electronic density of states (DOS) [36, 53]. C_q is relatively small for monolayer graphene and therefore dominant at low frequencies. Recent research shows that, by increasing the number of graphene layers, C_q is increased and its effect on total capacitance becomes less dominant [36]. It has also been shown that for multilayer graphene another capacitance is added in series with C_q, which is called the dielectric capacitance (C_{diel}). This capacitance is caused by a shielding effect inside the electrode due to a generated electric field. By increasing the number of graphene layers, this shielding region expands leading to a reduction in C_{diel} [54].

The equivalent circuit model was fitted to the Bode plots for all fifteen graphene electrodes (20 min growth time) using the equations presented in the Supplementary Notes. Then the averages for all parameters were calculated and are presented in the table reported in Fig. 3.5 (c). C_s is the series equivalent capacitance of C_{diel} and C_q. n is a constant in the range between 0 to 1 and equals 0.931, which shows the highly capacitive behavior of the constant phase element. Moreover, the high value of R_{ct} proves that the electric behavior is mainly capacitive and thus there is little Faradaic current at the electrode-electrolyte interface.

Table 3.2: Total and cathodic CSC, impedance at 1kHz, area-normalized impedance, charge injection capacity, water window of graphene, Pt, and Au electrodes, and a comparison with the state of the art CVD graphene neural electrodes

Electrodes	CSC (μC/cm²)					Electrode surface area (μm²)	Water window	CIC (μC/cm²)	Impedance at 1 kHz (kΩ)	Area-normalized impedance (Ω.cm²)	Reference
		1V/s	0.6V/s	0.2V/s	0.1V/s						
Graphene (20 min)	Total	972	1298	2425	3549	68320	-0.8 to 0.6	44	27.4 ± 7.5	18.72 ± 5.1	This work
	Cathodic	631	812	1453	2151						
Platinum (Pt)	Total	940	1131	1611	2012		-0.6 to 0.8	67.33	8.7	5.94	
	Cathodic	726	919	1396	1765						
Gold (Au)	Total	597	757	1272	1663		-0.8 to 0.6	11.7	7.5	5.1	
	Cathodic	454	594	993	1343						
Monolayer graphene (Doped with HNO_3)	Total				1953	2500	-0.8 to 0.8		541	13.5	[23]
Two stacked Monolayer graphene (Doped with HNO_3)	Cathodic		22.4 @0.5V/s scan rate			2500	-0.8 to 0.8		908 ± 488	22.7 ± 12.2	[24]
Few layers graphene	Total	910				707	-1.6 to 1.4	150	2650 ± 260	18.73 ± 1.84	[25]
Four stacked monolayer graphene	Cathodic	87.8				31416	-0.6 to 0.8	57.13	215.7± 120.4	67.76 ± 37.8	[26]

EIS measurements were performed on Au and Pt electrodes with the same dimensions (Fig. 3.5 (d, e)). The average impedances at 1 kHz, which are typically reported for neural electrodes, are approximately 7.5, 8.7, and 27.4 kΩ for the Au, Pt, and graphene electrodes, respectively. Furthermore, all electrodes exhibit capacitive behaviour at low frequencies. The comparison between the impedance at 1 kHz of the graphene electrodes fabricated in this work and the CVD graphene electrodes fabricated in other works can be found in Table 3.2. The impedance is normalized to the electrode surface area to ease the comparison.

3.4.4. CYCLIC VOLTAMMETRY

Cyclic voltammetry was performed on the same 15 graphene electrodes. The CV curves for graphene (20 min growth time), Au, and Pt are shown in Fig. 3.6 (a) at different scan rates. The CSC values were calculated based on the time integral of the CV curve and are reported in Table 3.2. The CSC calculated for Au is a lot lower than Pt and graphene. On the other hand, the CSC for graphene is comparable to that of Pt. However, the CSC values for graphene are higher at slower scan rates than those of Pt. This could be related to the high average surface roughness (6.75 nm) measured for 20 min graphene based on atomic force microscopy (AFM) measurements as shown in Fig. S8. At a high scan rate, for electrodes with a high surface roughness, only a fraction of the pores on the electrode surface are accessible for the electrochemical processes. On the other hand, a slower scan rate leads to a slower reactant flux, and therefore, increased accessibility to the electrode surface [55].

The comparison between the CSC calculated for graphene electrodes with different thicknesses was inconclusive as the variation between the CSC of the electrodes is insignificant. Therefore, a larger number of samples is needed for 40 min and 60 min graphene growth to be able to study the impact of thickness on the CSC.

Furthermore, as shown in Table 3.2, the CSC of our graphene electrodes is 1.8, 36, and 7 times higher compared with the graphene electrodes made from doped monolayer, two stacked monolayer, and four stacked monolayers, respectively [23, 24, 26]. More-

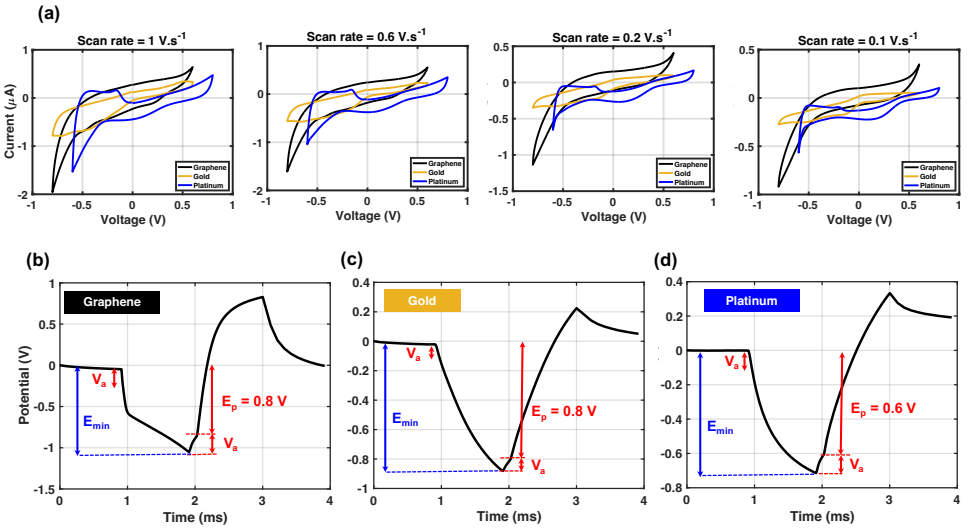


Figure 3.6: (a) CV curves for graphene, Pt, and Au electrodes with scan rates 1 V/s , 0.6 V/s, 0.2 V/s, and 0.1 V/s from left to right, respectively, (b) Voltage transient measurements for graphene, (c) Au, and (d) Pt electrodes.

over, the graphene electrodes reported in [25] show a high CSC at 1.0 V/s scan rate but still lower than the one reported in this work. Such a high CSC for the graphene electrode reported in [25] was related to the larger potential window used for the CV measurement.

3.4.5. VOLTAGE-TRANSIENT MEASUREMENTS

The results of voltage-transient measurements for graphene, Au, and Pt are shown in Fig. 3.6 (b-d). The maximum current amplitude that could be applied to the electrodes before exceeding the safe potential window are 30 μA, 8 μA, and 46 μA, for graphene, Au, and Pt, respectively. The calculated CICs are 44, 11.7, and 67.33 μC/cm^2 for graphene, Au, and Pt electrodes, respectively. It should be emphasized that by reducing the current pulse width, the current amplitude could be increased to ensure that the current is high enough to elicit neural activation, as pulse widths shorter than 0.6 ms are generally employed in neural stimulation [44]. However, this result still can be used as an indication of the CIC for neural stimulation.

3.4.6. PHOTO-INDUCED ARTIFACT TEST

The power spectra of the recorded signals for Au and graphene electrodes while shining 10 Hz light pulses on their surface are shown in Fig. 3.7. The spectra are normalized to the first harmonic of Au electrode. No artifact was detected in the power spectrum of graphene electrodes. On the other hand, for Au electrodes, the fundamental frequency component, but also harmonic components at 20, 30, 40, 50 Hz, etc., are observed. The measurement was repeated for graphene grown with different thicknesses and no artifacts were revealed.

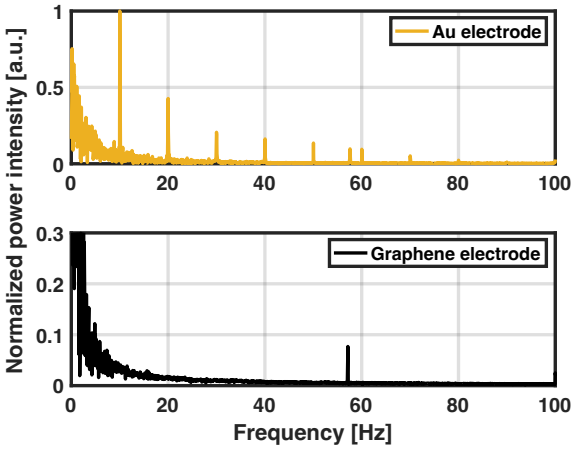


Figure 3.7: Normalized power spectrum of the recorded signal from Au and graphene electrodes (zoomed-in) after shining light with 10 Hz frequency.

3.4.7. MRI COMPATIBILITY TEST

As shown in Fig. 3.8 (a), an MRI compatibility test was performed for graphene and Pt electrodes in a 3 T MRI scanner. In this test, the eventual introduction of susceptibility artifacts that would then lead to signal dropout was investigated. To do this, T2*-weighted images were acquired because they accentuate local susceptibility effects. However, no electrode-related image artifact was detected in these images (Fig. 3.8 (b)). Therefore, EPI images, which are even more sensitive to B_0 inhomogeneity and then actual T2* maps were acquired. No image artifact was detected around the electrodes in the T2*-weighted image shown in Fig. 3.8 (c) as well. The T2* maps represented in Fig. 3.8 (d) also did not reveal any artifact around the electrodes. The lack of any artifact around the Pt electrode could be related to the very small thickness (100 nm) of the Pt electrodes.

However, the B_0 map acquired at a high resolution in a sagittal view shows a differential field response around Pt and graphene electrodes (Fig. 3.8 (e)). The field shifts induced by the electrodes are much smaller than the spatial inhomogeneity of the main magnetic field. Therefore, the field distortions originating from outside the ROI need to be removed using BFR. Then, the field distortion introduced by the electrodes becomes vaguely visible, and it is apparent that the effect is much stronger for Pt than for graphene. The mean value of the field distortion around Pt and graphene was averaged over fifteen repetitions resulting in 63.33±67.02 and 3.4±5.42 Hz variations around the main magnetic field value (B_0 = 3 T), respectively. This shows that the Pt electrode causes about 18.6 times higher magnetic field distortion than the graphene electrode due to its higher magnetic susceptibility than the surrounding tissue.

3.5. DISCUSSION

Multilayer graphene electrodes were fabricated using a wafer-scale transfer-free process. The use of CVD processes for graphene synthesis gives the opportunity of developing

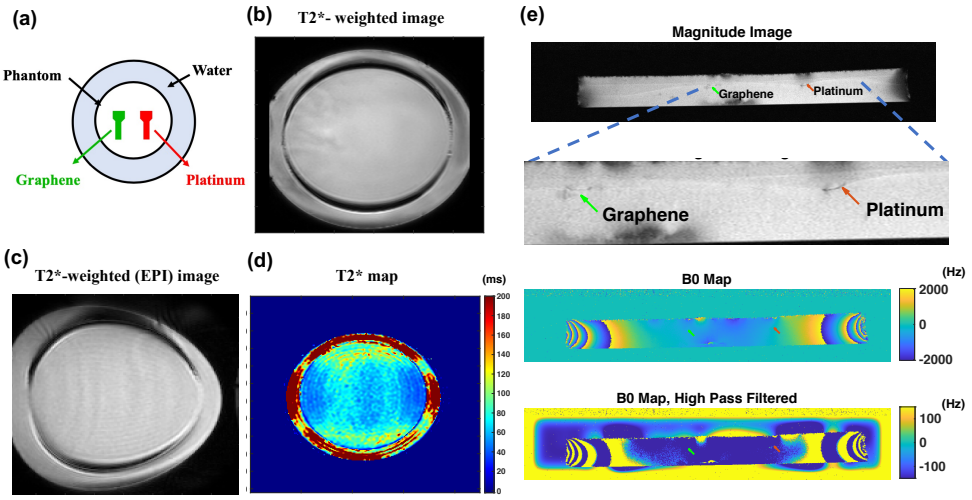


Figure 3.8: (a) Immersed Pt and graphene electrodes in a phantom, (b) T2*-weighted image with no artifact from the electrodes, (c) T2*-weighted image acquired with EPI readout resulting in an artifact-free imaging, (d) T2* maps of the electrodes without any artifact, (e) Baseline magnitude image, B_0 maps, and the high pass filtered image of the B_0 maps of the electrodes.

graphene layers only over desired areas, since the catalyst used can be patterned before graphene growth. Mo is chosen as a catalyst layer due to the possibility of growing thin and uniform layers of graphene because of its extremely low carbon solubility, thus creating a self-limiting growth process [56]. Moreover, the thermal expansion coefficient (CTE) of Mo in comparison with Cu and Ni is much closer to the one of Si, hence, Mo is less prone to wrinkle creation during high temperature graphene growth [57, 58]. Additionally, catalyst residues are an important concern in an implantable device. Cu has shown toxicity after histopathological evaluation in the cerebral cortex and categorized as a toxic material for the human body [59, 60]. Mo has shown biocompatibility [61]and biodegradability [62, 63] and therefore, is a great substitute for Cu as a catalyst material for biomedical applications. In addition, energy dispersive X-ray (EDX) analysis performed on our graphene electrode after Mo removal revealed only 0.03% weight percentage of Mo residue on the electrode surface as shown in Fig. S9.

The use of a transfer-free process adds significant advantages to the fabrication process. The graphene transfer method is a complicated process and the graphene layer is prone to crack formation, polymer contamination, catalyst residues, wrinkling, and folding [27]. Therefore, the resulting graphene implant performance might have a variation from device-to-device and wafer-to-wafer.

However, due to the transfer-free process used in this work, less defects and misalignment are expected in a graphene layer compared to transferred graphene. Subsequently, the absence of any polymer residues results in high optical transparency. More importantly, the transfer-free process is more compatible with conventional wafer-scale fabrication processes and results in a higher yield, as shown by the authors in [64]. This could provide the possibility of monolithic integration of active circuitry to the device

prior to graphene growth. The proposed fabrication process can be also an advantageous method for the fabrication of optoelectronic devices.

The process also allows for the addition of arbitrary polymers at the end of the fabrication process based on their mechanical characteristics and the application requirements. [65] and [66] also show the use of a multilayer stack for the encapsulation. In these cases, the mechanical properties of the device can be tuned by changing the thickness of each layer based on the application.

Multilayer graphene could cause a lower sheet resistance for graphene tracks compared to monolayer graphene as the sheet resistance is inversely proportional to the thickness of the film. Moreover, having multiple graphene layers provides additional transport paths for the charge carriers, which increases the conductivity of graphene. Recent research shows that increasing the number of layers to reduce the sheet resistance in a transfer process leads to optical transmittance reduction not only due to the added layers but also due to the polymer residues on each layer from the transfer process. Furthermore, since the transfer process can induce defects in the graphene lattice, for the same number of layers, fewer transfers show lower sheet resistance [34].

The results obtained by the sheet resistance and optical transmittance measurements in this work show sheet resistance and optical transparency reductions by increasing the graphene growth time. Besides, the additional layers are expected to enhance the mechanical and electrical reliability [67]. Therefore, 20 min graphene growth was chosen to make graphene-based devices that are optically transparent enough to be used for modern neuroscientific research such as optogenetics and *in vivo* optical imaging. It should be noted that doping could decrease the sheet resistance even further but this was not the focus of this work.

A thorough characterization of the properties of the graphene electrodes presented here was conducted and results are summarized in Table 3.2.

A comparison between our multilayer graphene with Au and Pt electrodes showed only 3-4 times higher impedance (1 kHz) for graphene electrodes. The multilayer graphene electrodes fabricated in this work showed a lower area-normalized impedance compared to other undoped CVD-based graphene electrodes.

CV measurements showed that our graphene electrodes are comparable to Pt electrodes in terms of CSC. Graphene electrodes outperform Pt electrodes when using slower scan rates for CV measurements. This could be related to the high graphene surface roughness that could be more accessible for ion fluxes at lower frequencies. The CSC at different scan rates was measured to be able to compare the result with state-of-the-art graphene electrodes. It was shown that our multilayer graphene has the highest CSC reported so far for CVD graphene electrodes.

The significant improvement in CSC for the multilayer graphene compared to monolayer graphene could be explained by the effect of the quantum capacitance in series with the double layer capacitance. By increasing the number of graphene layers, the quantum capacitance is increased. Therefore, this capacitance is no longer dominant for multilayer graphene and the total capacitance will be increased.

On the other hand, voltage-transient measurements showed comparable CIC for both graphene and Pt. However, to substitute conventional metal electrodes, the CIC could be further improved using chemical dopants or surface functionalization methods to give

graphene the possibility to compete with Pt electrodes. In fact, other transparent materials such as poly (3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) and carbon nanotube (CNT) with great CIC (up to 15 mC/cm^2 and 1.6 mC/cm^2, respectively) and low impedance due to their high surface area are other electrode candidates [44]. These have been added as coating materials on graphene to improve its characteristics [68, 69].

The graphene electrodes in [25] appear to be capable of higher CIC than what we achieved. This is probably related to the unusually large potential window used in the CV measurement in [25]. A detailed study on the safe potential limit used for CV measurement for graphene material is hence necessary to further appreciate the capabilities of graphene as a stimulation electrode.

Regarding photo-induced artifacts, a previous report for a monolayer graphene electrode tested with a 470 nm light emitting diode (LED) light source did not show any artifact [28]. However, a photo-induced artifact was observed with stacked 4-layer graphene tested using blue laser diodes [26]. Therefore, it was uncertain whether the artifact was induced due to a larger thickness of graphene or due to the different light sources used for this test.

The photo-induced artifact test performed in this work using an LED light source, showed no artifact on the power spectrum of the recorded signal picked up from the graphene electrode. However, visible peaks were observed using the Au electrode. The same measurement with different thicknesses of graphene still did not show any artifact. This could prove the lack of dependence of photoelectrochemical effect on the graphene thickness. However, to be able to conclusively argue about such independence, additional characterisation would be needed. More importantly, LEDs were used as the light source in this test. It is possible that when a coherent light source, i.e. a laser diode, is used instead, photo-induced artifacts will be generated [10].

Moreover, it should be noted that for a thorough investigation of the photo-induced artifact, this test must be performed in an *in vivo* condition as the light scattering and absorption in tissue differs from that in a simple PBS environment. However, this PBS test is a good first indicator and can additionally provide information about the effect of increased thickness on any generated artifact.

The MRI compatibility of graphene encapsulated Cu wires [17] and graphene fibers [18] has been recently confirmed. The MRI test performed in this work shows that CVD graphene electrodes encapsulated with parylene-C can be considered MRI compatible. This could be due to the small difference between the magnetic susceptibility of graphene and the human body. The exact value of magnetic susceptibility of graphene is unknown. However, carbon (C) in graphite form is reported to have a highly anisotropic diamagnetic susceptibility (−8.5ppm) [70], which is very close to that of brain tissue (−9.2 to −8.8 ppm) [71].

On the other hand, Pt electrodes were expected to show image artifact in MRI. However no artifact was detected. Therefore, using Pt electrodes with a larger thickness or in an MRI scanner with a higher magnetic field strength (7 T or more) might generate even higher magnetic field distortion leading to more image artifacts.

No substantial heating was detected with a room temperature IR thermometer. However, the use of a phantom instead of real tissue might lead to a different temperature

distribution and thus a different degree of image artifacts. Therefore, an *in vivo* MRI test with graphene electrodes implanted would be advantageous.

Apart from a magnetic susceptibility difference, the material conductivity and the eddy currents induced in the material by gradient switching and the RF field might cause MRI artifacts. However, the eddy current induced artifact was assumed to be negligible.

3.6. CONCLUSIONS

We presented the development and characterization of fully transparent CVD-based multilayer graphene electrodes using a wafer-scale transfer-free process for the next generation of optically transparent and MRI-compatible neural interfaces. The electrodes were fabricated directly on a patterned Mo catalyst resulting in a multilayer graphene electrode.

The electrode showed low impedance (27.4 kΩ) at 1 kHz that is quite comparable to those of Au and Pt electrodes with the same size and geometry. A 3.5 mC/cm^2 CSC was achieved based on CV measurements for graphene at a 100 mV/s scan rate that is the highest value reported for CVD graphene electrodes to date. The CIC was also calculated for graphene electrodes (44 µC/cm^2) using voltage-transient measurements. Our graphene electrodes illuminated with light pulses with a repetition rate of 10 Hz did not reveal any photo-inducted artifacts for all thicknesses measured. Moreover, the fully transparent electrodes did not show any image artifact in a 3 T MRI scanner. These results show that graphene multilayer electrodes with a high CSC and a low impedance could be used for the next generation of neural interfaces, enable multimodal electrical and optical recording and stimulation, and substitute the current standard metal electrodes, to additionally allow for MRI studies of the nervous system.

3.7. SUPPLEMENTARY NOTES

3.7.1. MASK DESIGN

The masks used for this project shown in Fig. S1/Fig. 3.9 were previously designed [72].

In the Mo/graphene mask, holes are designed to promote better adhesion of the metal layer (Al (1%Si) / Ti) that will be applied on top of graphene with the layer underneath (SiO_x). In the Al/metal mask, the metal layer on top of the electrode is smaller such that it can easily be removed from graphene when needed. Moreover, once the metal is removed, the graphene electrode area should not be fully exposed but protected against possible delamination, at its outermost ring, by the polymer on top (smaller opening in the polymer opening mask for the electrodes). The metal layer on the contact pads of graphene is slightly larger than graphene contact pads. The reason is the adhesion needed to keep the metal layer on top of the graphene until the final steps of the microfabrication process.

Additionally, in the polymer opening mask, the dimensions of the openings for the contact pads are the same as for the graphene pads, to ensure that graphene pads are completely covered by the metal layer. This Al metal layer on the contact pad was also designed for soldering wires to the contact pads. However, the openings for the electrodes are smaller than the metal to avoid damaging the graphene layer in case of misalignment of the mask during the lithography steps.

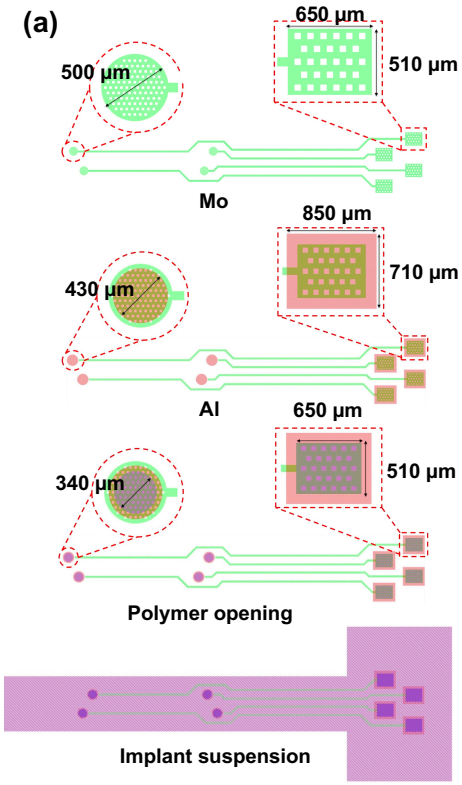


Figure 3.9: Masks used for the microfabrication of full implant devices. The electrode diameter is 340 µm which leads to an area of 90792 µm2. However, the total surface area after subtraction of the holes is 68320 µm2.

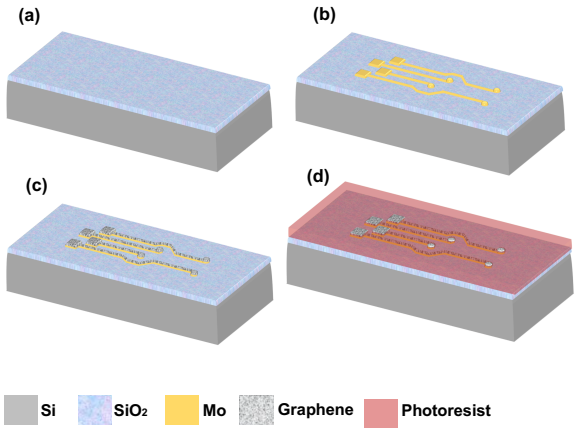


Figure 3.10: Fabrication process steps for graphene electrodes on Si. (a) 300 nm wet thermal oxide grown on the front side of a single-sided polished (SSP) Si wafer, (b) Mo deposition and pattern, (c) Graphene growth, (d) 4µm photoresist coating as an insulation layer. The photoresist is finally patterned and etched only on the electrodes and contact pads.

3.7.2. GRAPHENE, PT, AND AU ELECTRODES ON SI

For rapid prototyping and for enabling the investigation and comparison of graphene electrodes with those of Pt and Au of similar size and geometry, non-suspended devices were fabricated. For these test structures, parylene insulation is substituted by photoresist to simplify the processing. The fabrication process for these devices is described as following:

GRAPHENE ELECTRODES ON SI

Fabrication process steps for graphene electrode creation on Si substrate are shown in Fig. S2/Fig. 3.10. 300 nm wet thermal oxide is grown on the front side of a single-sided polished (SSP) Si wafer followed by Mo deposition, pattern, and etch. Then, Graphene is grown on the pre-patterned Mo. Finally, 4 µm photoresist is coated on the wafer as an insulation layer. The photoresist is finally patterned and etched only on the electrodes and contact pads.

PT AND AU ELECTRODES ON SI

Fabrication process steps for both Pt and Au electrodes on Si start with 300 nm wet thermal oxide deposition on the front side of an SSP Si wafer as shown in Fig. S3/Fig. 3.11. Next, a photoresist layer is spin-coated and patterned. Then, 100 nm thick Pt or Au is deposited using an e-beam vapor-deposition technique on a 10 nm Ti adhesion promoter. A lift-off process followed by photoresist removal in an ultrasonic bath creates electrodes and tracks made of metals. Photoresist serves as the final insulation layer between the electrodes.

3.7.3. SHEET RESISTANCE MEASUREMENT

Four-point probe measurements were performed with a Cascade Microtech probe station. The four probes were positioned on the Ag ink dots on the extremities of the Van der

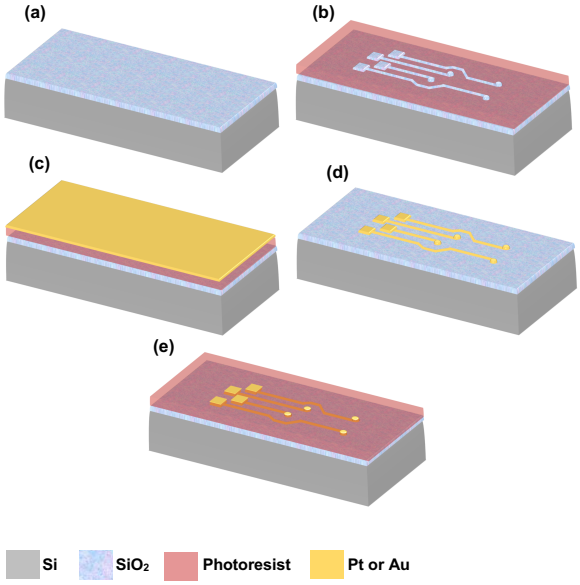


Figure 3.11: Fabrication process steps for Pt and Au electrodes on Si. (a) 300 nm wet thermal oxide deposited on the front side of an SSP Si wafer, (b) Photoresist spin-coating and pattern, (c) 100 nm thick Pt or Au e-beam vapor-deposited on a 10 nm Ti adhesion promoter (d) Lift-off process and removing the remaining photoresist layer in an ultrasonic bath (e) Photoresist coating and pattern.

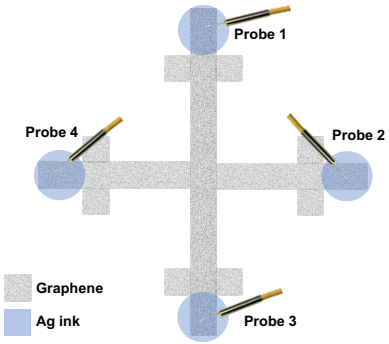


Figure 3.12: Van der Pauw structures used for measuring the sheet resistance of graphene layers with different growth times (20, 40, and 60 min). Contact pads were covered with a drop of silver (Ag) ink to prevent any damage caused by the measurement probes on the graphene.

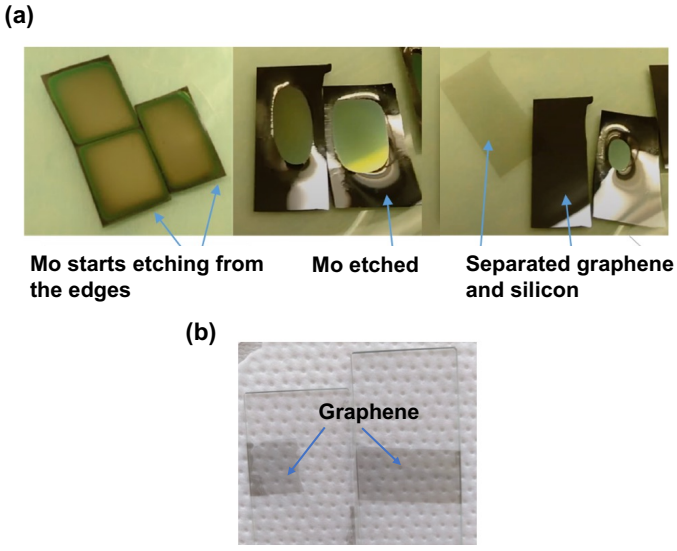


Figure 3.13: Sample preparation for optical transmittance measurement, (a) graphene transfer process to glass slides, (b) graphene with 20 min growth time transferred to a glass slide

Pauw structures as shown in Fig. S4/Fig. 3.12. The current was forced between Probes 1 and 2 ($I_{1,2}$), by setting the Probe 1 potential from -1 V to 1 V with 8 mV steps and Probe 2 acting as ground. The voltage was measured between Probes 3 and 4 ($V_{3,4}$). The sheet resistance (R_{sh}) was calculated using the equation below for each point in Ω/sq unit, which were then averaged, excluding the values around I = 0.

$$R_{sh} = \frac{V_{3,4}}{I_{1,2}} \times \frac{\pi}{\ln 2} \tag{3.1}$$

3.7.4. GRAPHENE TRANSFER PROCESS

The method used for graphene transfer started with a full wafer with graphene grown on non-patterned Mo. The wafer was then manually diced into roughly 2 cm^2 pieces. These were then placed in a beaker where H_2O_2 was added just until the height of the Si piece with graphene. Mo then started to etch from the sides towards the center, as illustrated in Fig. S5 (a)/Fig. 3.13 (a). After all the Mo was etched, the graphene was separated from the silicon piece and floated on the surface of the liquid while the silicon fell to the bottom of the beaker. DI water was then added very gently with a pipette until the level of the liquid rose about 2 cm. The floating graphene was then scooped on the glass slide. One drop of Triton X100 was added to 1 liter of DI water and 50 ml of triton-water solution was added to the H_2O_2 in the beaker to reduce surface tension. The resulting glass slides with transferred graphene are shown in Fig. S5 (b)/Fig. 3.13 (b).

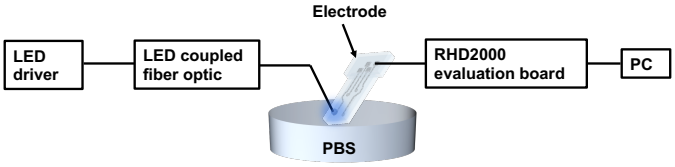


Figure 3.14: Setup used for photo-induced artifact test including an Intan RHD2000 Evaluation System, a 200 µm diameter fiber, and a blue light LED.

3.7.5. FIGURE OF MERIT (FOM)

To evaluate the quality of a transparent conductive film (TCF), the figure of merit (FOM) is calculated based on optical transmittance (T) at 550 nm wavelength and sheet resistance (R_{sh}). Films with low R_{sh} at high optical transmittance show higher performance as a TCF, therefore, a higher FOM corresponds with better TCF performance. The most widely used FOM is defined as follows:

$$\mathrm{FOM} = \frac{188.5\sqrt{\mathrm{T}}}{\mathrm{R_{sh}}(1-\sqrt{\mathrm{T}})} \tag{3.2}$$

The FOM calculated based on this equation can be used to evaluate all films with different thicknesses, synthesized from different methods and materials. The reported values in this work are comparable with the result from graphene electrodes manufactured using a CVD process and also higher than the theoretical value (2.55) calculated by the same equation for undoped monolayer graphene. However, the calculated FOM is as expected a lot lower than the one of ITO (60 for 40 nm).

3.7.6. PHOTO-INDUCED ARTIFACT

The setup used for the photo-induced artifact test is shown in Fig.S6/Fig. 3.14. A 200 µm diameter fiber was used to shine the light from an LED (M470F1, Thorlabs) with a blue light on an electrode site soaked in a PBS solution. The LED driver (DC2200, Thorlabs) was used to drive the LED.

The electrode was connected to an RHD2000-series amplifier evaluation system (Intan Technologies, LLC) for data acquisition. This system consists of a headstage that includes the RHD2000-series amplifier chip and can be connected to the electrode contact pad. The headstage is then connected to the USB interface evaluation board via a serial peripheral interface (SPI) cable. The evaluation board is then connected to a computer and a multi-platform graphical user interface (GUI) controls the operation of the amplifiers. The electrode and the RHD headstage were both kept inside a Faraday cage to prevent any interference.

3.7.7. MRI SEQUENCES AND PARAMETERS

MRI sequences and parameters used to acquire each image are shown in detail in Table.S1/Table. 3.3

Table 3.3: MRI sequences and parameters used to acquire each image

Sequence	Acquired images	Acquired resolution (mm^3)	Field of view (FOV) (mm^2)	Nr. slices	Nr. echos	T_R (Repetition time) (ms)	T_E (Echo time) (ms)	Flip angle (°)	Sense
Dual-echo GRE	T2*-weighted	0.7×0.7×0.7	150×131	70	2	22	T_{E1} = 6.2, T_{E2} = 15.2	15	-
SSh GRE EPI	T2*-weighted	1.4×1.4×1	150×150	30	1	3681	50	90	-
Multi-echo GRE	T2*-weighted, T2* maps	1.8×1.8×2	200×200	10	15	19	T_{E1} = 1.96, ΔT_E = 1.1	25	Factor = 2
Spoiled GRE	T2*-weighted, B_0 maps	0.2×0.2×7	110×28	1	2	2400	T_{E1} = 15, T_{E2} = 25	70	-

3.7.8. ELECTRICAL IMPEDANCE SPECTROSCOPY (EIS)

The EIS data for graphene electrodes using 40- and 60-min graphene growth recipes are shown in Fig. S6 (a, b)/Fig. 3.15 (a, b), respectively. The impedance of three 40-min graphene electrodes at 1kHz are 13.1, 47.4, and 56.4 kΩ and the impedance of three 60-min graphene electrodes are 18.2, 23.8, and 47.8 kΩ. Therefore, to be able to draw a conclusion about the influence of graphene's number of layers on impedance larger number of samples is required as there are noticeable variations in the impedance for different samples.

3.7.9. EQUIVALENT CIRCUIT MODEL

The equation used for Z_{CPE} in the equivalent circuit model is:

$$Z_{CPE} = \frac{1}{Q(j\omega)^n} \tag{3.3}$$

where j is the unit imaginary number for which it holds that $j^2 = -1$, ω is the angular frequency being 2π times the frequency of the AC signal ($\omega = 2\pi f$), Q is a measure of the magnitude of Z_{CPE}, and n is a constant in the range between 0 to 1. When n = 1, Z_{CPE} is a purely capacitive impedance element, and Q is capacitance; when n = 0, Z_{CPE} is a purely resistive element, and Q is its conductance, the reciprocal of its resistance. For practical electrode-electrolyte interfaces, the Z_{CPE} is used instead of a pure capacitance, accounting for the non-ideal capacitive behavior of the electrochemical double layer.

The equation used for Z_{WB} in the equivalent circuit model is:

$$Z_{WB} = \frac{W_B}{\sqrt{j\omega}} \times \tanh\left(\frac{\sqrt{j\omega}}{B}\right) \tag{3.4}$$

Where W_B is the finite-length Warburg coefficient and B is:

$$B = \frac{\sqrt{D}}{\delta} \tag{3.5}$$

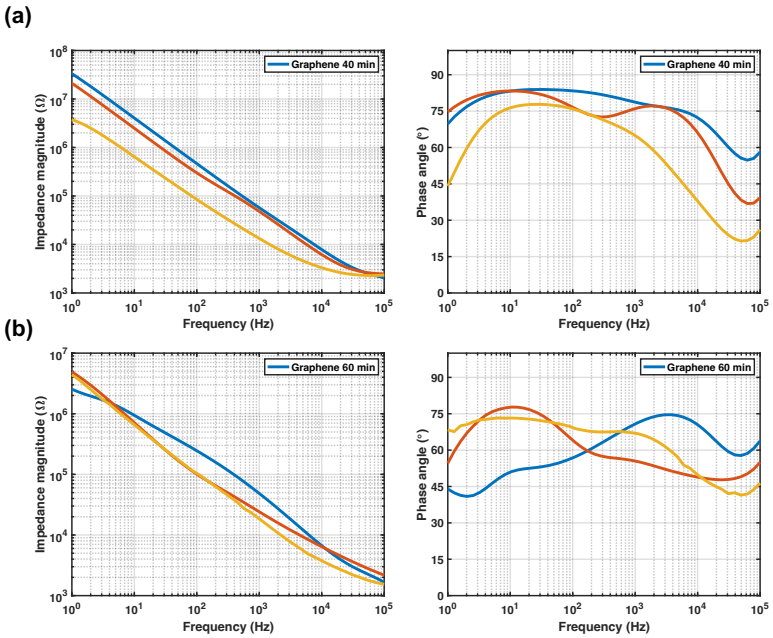


Figure 3.15: Average impedance magnitude and phase angle plots (with standard deviation shaded in grey) for (a) three graphene electrodes using 40 min graphene growth, and (b) three graphene electrodes using 60 min graphene growth.

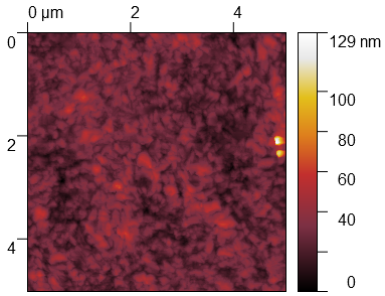


Figure 3.16: AFM image of the graphene electrode surface

Where D is the diffusion coefficient and δ is the thickness of the diffusion layer.

3.7.10. CYCLIC VOLTAMMETRY (CV)

The CV scan performed in this chapter for each electrode started at 0 V, then the potential increased until the upper limit. Next, the potential decreased to the lower limit and after that returned back to 0 V. The scan was repeated 3 times to stabilize the signal, and the third scan was used in the calculation of the CSC. The CSC is calculated based on the time integral of the CV curve. The calculated charge was then divided by the electrode surface area (68320µm^2) to obtain the charge density. Finally, the CSC was expressed in µC/cm^2.

3.7.11. ATOMIC FORCE MICROSCOPY (AFM)

Since any surface roughness greatly increases the CSC due to an increase in the electrochemical surface area of the electrode, the prepared graphene samples were characterized by atomic force microscopy (AFM) as shown in Fig. S8/Fig. 3.16. AFM was conducted using an NTEGRA Spectra system at ambient conditions. The morphology was captured in the tapping mode with a NSG01 probe. The surface roughness was measured across the 50 × 50 µm^2 areas, calculated as the root-mean-square of the height distributions, and then averaged. The phase lag of the AFM probes was measured simultaneously with the topography to achieve better contrast of small topographic features. High-quality images were processed in the standard way using Gwyddion, applying polynomial correction of the background. Then, surface characterization was used to determine the surface roughness.

3.7.12. EDX MEASUREMENT

EDX measurement is performed on the electrode surface to investigate if there are any Mo residues after the fabrication process. For this measurement, Mo is deposited on a Si wafer with a pre-deposited SiO_2 layer. Next, graphene is grown on a Mo catalyst. Then, Mo is etched using a simple wet etching process (using H_2O_2) as was also used in the paper. To verify that there is no Mo residue energy dispersive X-ray (EDX) (FEI XL30 SFEG, w. EDAX Octane Plus detector) analysis was performed. During the EDX measurement, the electrode surface after Mo removal was focused using a 15 kV electron beam and a

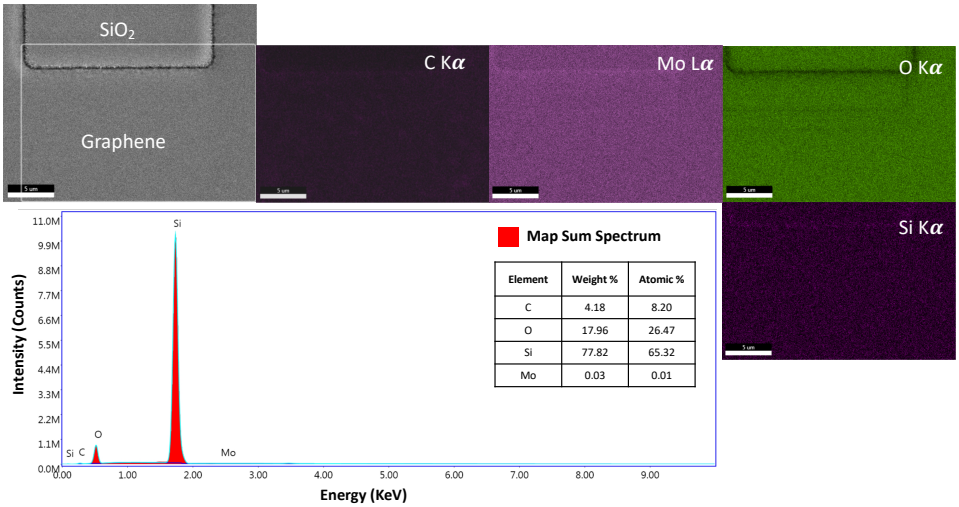


Figure 3.17: SEM image, EDX elemental mapping, and the map spectrum of the graphene electrode after Mo removal

spot size of 6. The elemental mapping results acquired after 92 minutes represented in Fig. S9/Fig. 4.8 show the presence of Si, O, C, and Mo and the corresponding spectrum. The indicated areas with graphene and without graphene in the SEM image match the C map. Details of the atomic and weight percent of each element are listed in the inset Table represented on the right side of the diagram. At the location where normally the Mo peak is found (2.293 eV), no clear feature can be distinguished above the noise floor. Upon manually selecting Mo as the element, 0.03 weight and 0.01 atomic percentages are attributed to this element. However, the thin layer of graphene is still present and EDX was able to distinguish it.

3.8. ADDITIONAL INFORMATION

3.8.1. FABRICATION PROCESS: BACKSIDE AND FRONT SIDE OXIDE ETCH

Additional information regarding some of the fabrication process steps is added in this section. One of the challenging steps in the fabrication process of graphene-based neural electrodes is the oxide etch step. As mentioned before, 2 µm and 4 µm PECVD oxide is deposited on the front and back sides of a DSP si wafer. The backside oxide is patterned and etched for the subsequent DRIE process steps. Fig. 3.18 shows the wafer after SiO_2 etch step.

After the DRIE step, the Si substrate is etched and the front-side oxide is reached from the backside of the wafer. This 2 µm oxide needs to be removed before the removal of the Mo layer. BHF is usually used as a solution to etch oxide. However, the Al layer present on the front side of the wafer (as a metal hard mask for the polymer etch step) is also etched in BHF. To protect this Al layer, a dedicated wafer holder is used as shown in Fig.3.19 (a). This wafer holder protects the front side of the wafer by covering it using a

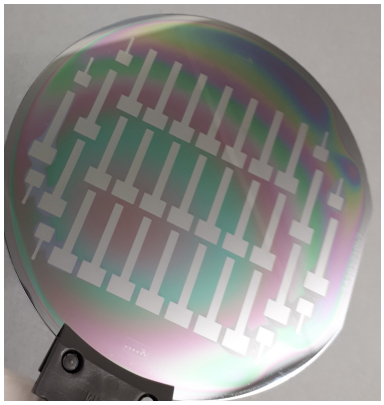


Figure 3.18: Backside oxide is patterned and etched for the subsequent DRIE step.

lid (this lid is tightened up by six screws), while the back side of the wafer is exposed to BHF solution.

There are some challenges in using the wet etching process. First, this process is not uniform as shown in Fig. 3.19 (b). Therefore, some structures still have oxide while the oxide is completely removed from the other structures. Second, even though the wafer holder is tight and no BHF can touch the Al layer on the front side, BHF can still diffuse through the polymer and reach the Al layer on top of the electrodes and contact pads and cause delamination as shown in Fig. 3.19(c).

To overcome these problems, one could increase the polymer thickness. This might delay the diffusion of BHF through the polymer. However, a thicker polymer layer is not of interest considering the application of thin and miniaturized devices. Moreover, having thicker polymer on the electrodes and contact pads might create challenges regarding polymer etching (due to longer etching time) as will be explained later.

Another solution to this problem might be to reduce the thickness of the oxide to ensure a shorter wet etching process. However, thinning the front side oxide should be accompanied by thinner backside oxide to prevent crack formation along the wafer. Reducing the backside oxide thickness is not possible in this flow because the oxide is needed to protect Si from etching during the DRIE process step (oxide is also etched with a slower etch rate in a DRIE process).

The final method to overcome these problems is to use a dry etching method to etch SiO_2. The recipe used to etch oxide used a low RF power with a slow etch rate (20nm/min) to ensure a soft landing on Mo without damaging it (using an AMS110 etcher (Alcatel) with 300 W RF power, and 17, 150, and 18 sccm C_4F_8, He, and CH_4 gas flows, respectively).

3.8.2. FABRICATION PROCESS: POLYMER REMOVAL

Polymers used as an insulation layer for the electrodes in this work are parylene C and PDMS. To remove these polymers from the electrodes and contact pads, several methods were investigated in this thesis.

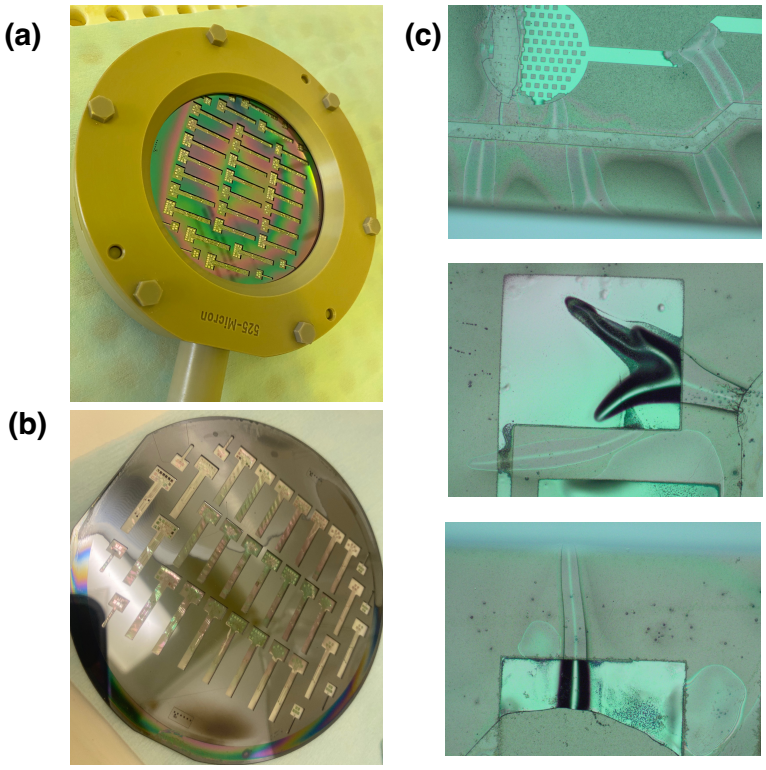


Figure 3.19: Wet etching of frontside oxide, (a) Dedicated wafer holder for single-side wet etching, (b) Non-uniform etching of oxide from the back side of the wafer, (c) Delamination of Al layer on the front side due to BHF diffusion through polymer.

In the case of parylene, due to its chemical inertness, chemical etching is limited to dry etching and it is quite challenging [73]. So far, plasma etching has shown great promise for the achievement of defined micrometer patterns in parylene C films [73]. However, it is hard to achieve a fast etching rate, lack of residues, and high aspect ratios (especially for thick layers) due to its crystalline structure [74].

Polymers are etched using a photoresist or a metal hard mask followed by a dry etching process. Since parylene is an inert material, its etching rate is quite slow (between 0.1 and 1 µm/min as reported in [74]). Therefore, the photoresist used as a mask layer usually etches faster than the polymer, resulting in poor selectivity. It should be mentioned that if the parylene layer is thin enough using the photoresist layer as a mask should be still possible. Positive photoresist AZ ECI 3025 is reported to be used as a mask for thin layers of parylene during etching [75]. To etch thicker parylene, AZ40XT photoresist was recently used as it can be patterned in thick layers. However, since it is based on diazonaphthoquinone chemistry, it quickly overheats in the plasma chamber, and within minutes forms cracks and bubbles on its surface [76].

In this thesis, AZ12XT photoresist was used primarily as a mask layer on 10 µm parylene during the plasma etching process. As expected based on previous research, cracks and bubbles started appearing on the photoresist compromising the process. Therefore, this method was not further investigated for parylene removal, hence alternative methods based on using a metal hard mask for parylene etching process were sought.

In addition, laser cutting could be another option to remove the polymer layer from the electrodes. This method might be used for cutting large samples but is reported to leave debris on the openings in micro-level structures [77].

In this thesis, two methods are mainly discussed for polymer removal from the electrode surface: (1) plasma etching with a metal hard mask and (2) laser patterning. To test plasma etching, PDMS and parylene samples were used. A more complicated etching process is expected for PDMS samples as electrodes with PDMS have larger thicknesses compared to parylene electrodes, and consequently, a longer polymer etching time is expected for PDMS-encapsulated electrodes. Therefore, more focus is put on the plasma etching of PDMS. To study the laser patterning method, parylene samples were made since parylene has a lower glass transition temperature compared to PDMS and it is assumed that its laser patterning might create more challenges.

PLASMA ETCHING USING A METAL HARD MASK

To perform the polymer etching using a plasma etch, a metal hard mask is used. The main challenge regarding the use of polymer etching is related to the metal hard mask. Most metal layers do not have good adhesion to the polymers. Another challenge is that the metal deposition at a slightly high temperature above the glass temperature of the polymer might cause degassing and crack formation in the polymer. Therefore, the deposition temperature should be kept low (in this work 25 °C) to prevent this issue.

Additionally, metal particles can penetrate the polymer during the deposition process. These metal particles might act as micro-masks during the subsequent etching step and leave some fur-like structures as shown previously in [78]. Thus, the deposition power should be kept as low as possible (in this work 1 kW) to prevent metal particles from penetrating deep into the polymer layer.

Even by reducing the deposition power, some metal particles might still penetrate the polymer. To ensure the removal of these metal particles, a long over-etching step was used after etching the metal layer from the electrodes and contact pads. This method was proposed previously to remove the fur-like residues after dry etching of polyimide [78].

These considerations help to reduce the risk of crack formation in the polymer layer and fur-like structures on the exposed areas after the etching steps. However, the re-deposition of the metal mask also occurs during the etching step, specifically for thicker polymers with a long etching time.

PLASMA ETCHING OF PDMS

To create test samples for plasma etching of PDMS, samples with graphene electrodes were covered with a layer of Al (1%Si). Next, PDMS was spin-coated as an encapsulation layer. Then, the metal hard mask of 500 nm Al (1%Si) was sputter-deposited on the PDMS layer.

PDMS cannot be etched with only oxygen plasma unlike most polymeric materials due to the presence of the Si-O group which needs a fluorine environment to be etched. An etching recipe (50, 20, and 20 sccm SF_6, O_2, and C_4F_8, respectively with 2000W ICP power, and 100 W RF power) with an etch rate of 2 µm/min was used to etch PDMS on the test samples using AMS110 etcher (Alcatel). The photoresist used to pattern Al was left on the wafer after Al etching to protect the Al mask at least at the beginning of the etching. The photoresist was removed later during the etching process due to the presence of an oxygen plasma. After almost 10 minutes of etching, the Al layer started changing color and becoming rough. Based on the literature, this might be due to the re-deposition of the metal mask [79].

The recipe was optimized by reducing the RF power from 100 to 40 W to decrease the ionic bombardment effect. The etch rate is much lower and the Al re-deposition seems to be much less. However, after 40 minutes of etching, the electrodes and contact pads could not be etched further. The optical image of the electrode is shown in Fig. 3.20 (a). The SEM images of the contact pads are also shown in Fig. 3.20 (b). The electrode and contact pad surface are covered with fur-like structures.

The recipe was changed again by lowering the RF power and increasing the gas flows (100 SF_6, 40 O_2, and 20 C_4F_8, 2000W ICP power, 10W RF power). The result is shown for both the electrode and the contact pad in Fig. 3.20 (c). The polymer layer on the electrode and contact pad started to be removed. However, this etching recipe is very slow and time-consuming. If any fur-like structure remains on the electrode it can be easily removed in the next step of Al removal to expose the underlying graphene.

PLASMA ETCHING OF PARYLENE

The plasma etching of polymer using a metal hard mask was also tested to etch parylene. The process is similar to PDMS etching, however, some slight changes are worth mentioning. To do this, test samples with gold electrodes encapsulated with parylene were created. It should be noted that Al (1%Si) cannot be used as a hard mask for parylene etching as Al does not adhere well to parylene. Therefore, 500 nm/ 100 nm Al (1%Si)/ Ti is sputter-deposited on parylene as a hard mask. The same plasma etcher was used (AMS110 etcher (Alcatel)) to etch parylene. The recipe used 40 W LF power, 15 sccm of

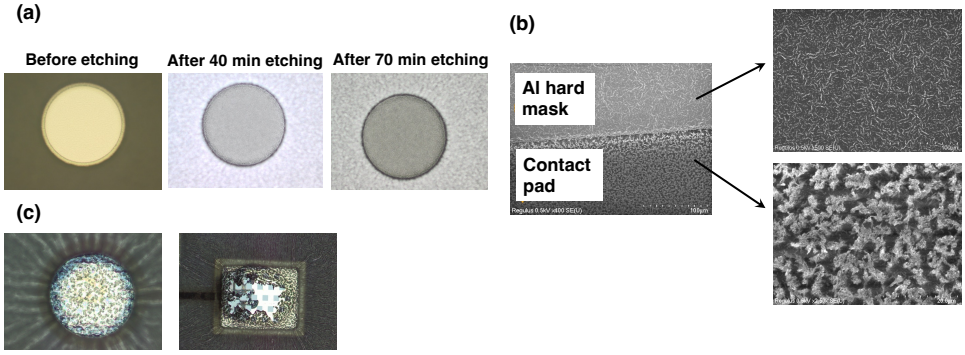


Figure 3.20: Optical image of the electrode (a) before and after etching, (b) SEM image of the contact pad after keeping the photoresist and decreasing the RF power and increasing the gas flows, (c) optical image of the electrode after using lower RF power to reduce the amount of Al re-deposition during the etching step.

SF_6, and 185 sccm of O_2. The SF_6 was added to the oxygen plasma as it was proven to have a significant effect on removing the fur-like structures from the surface [80]. It was reported that SF_6 could be excited to fluorine-free radicals during the process, consequently turning the metallic particles into metal fluoride resulting in their removal. As shown in Fig. 3.21 (a), parylene-Au structures are observed after the full fabrication process. The parylene layer is etched on the electrode as shown in Fig. 3.21 (b). The 10 µm parylene etch from the contact pad is also shown in Fig. 3.21 (c).

LASER PATTERNING OF PARYLENE

As mentioned previously, another possibility to remove polymer from the electrode and contact pad is laser patterning. The advantage of this method is that for any change in the design or electrode size, re-fabricating new masks is not necessary. Moreover, it is a faster method compared to polymer plasma etching. Therefore, laser patterning could provide a cheaper method compared to photolithography specifically for fast prototyping.

To use a laser for patterning polymers, the metal hard mask is not needed. The test samples used for this experiment include samples with different thicknesses (675 nm and 1475 nm) of Al(1%Si) encapsulated with parylene. A metal layer (Al) on top of graphene in the final design is required as the direct contact of the laser with graphene might cause damage. Therefore, different thicknesses are tested here for Al(1%Si).

For this study, a pulsed picosecond laser (Schmoll Picodrill) with a frequency range from 200 kHz up to 1 MHz was used. The laser uses two separate beam paths, IR and UV. The IR beam was chosen for this experiment due to the lower absorption coefficient of metals (Au and Al) in the IR spectrum which results in a higher uniformity of the exposed electrode [81].

The IR beam with a 1064 nm wavelength has a maximum power of 50 W and a minimum beam diameter of around 40 µm, when focused. Two different drilling modes "punched" and "hatched" are available with this laser. The pulsed laser, in the punched mode, directs its energy to a fixed location creating small vias with the diameter of the

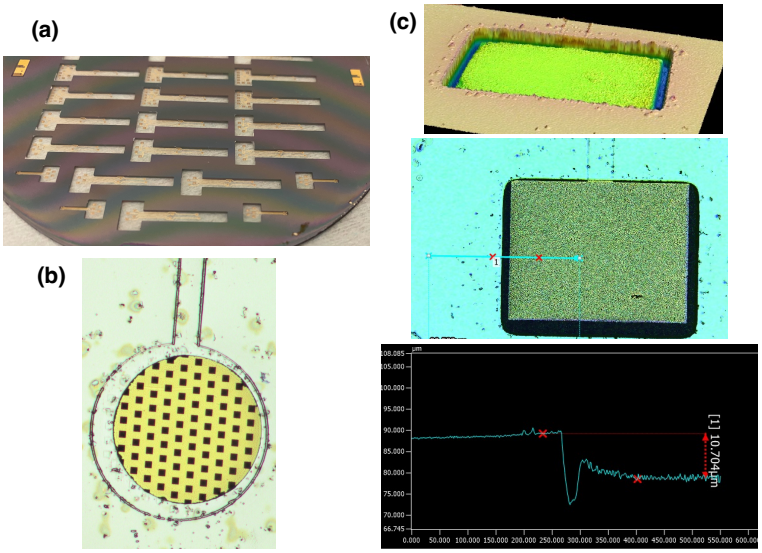


Figure 3.21: a) Parylene-gold structures, (b) Parylene removal from the gold electrode, (c) 10 µm parylene removal from contact pad

laser beam. On the other hand, the "hatched" mode is used when larger openings are desired. Since the electrode surface area and the required openings in this work are larger than the diameter of the laser beam, the hatched mode was selected.

Multiple rings of different diameters had to be hatched to ensure the opening of such large electrodes. The number of rings and the distance between them is dependent on the diameter of the beam. The reason is that overlap is needed to ensure the complete removal of the material.

The parameters that can be changed to remove polymer using a laser were power, the number of repetitions (how many times the laser hatched the same area), and the cut speed. The cut speed determines how much is hatched in one second. This parameter can be correlated with the amount of energy concentrated in one location. It can be increased to avoid having too much energy concentrated in one location for a longer period. This might generally avoid damaging the electrode surface.

The parylene layer removal from 675 nm Al(1%Si) with different process parameters is shown in Fig.3.22. Red circles show parylene residues and the white circles show the removal of Al reaching underlying oxide. As shown in Fig.3.22 (a), the Al layer is removed probably due to too much applied average power. It might be also that the Al layer is too thin and is easily damaged and delaminated. Decreasing the number of repetitions or power could lead to less damage on the surface. However, it might result in more parylene residues on the electrode.

To overcome the issue of damage on the electrode surface, the Al layer thickness was increased to 1475nm. The result after laser patterning is shown in Fig.3.23. As shown in Fig.3.23 (a), the parylene layer was not completely removed (the brown areas shown

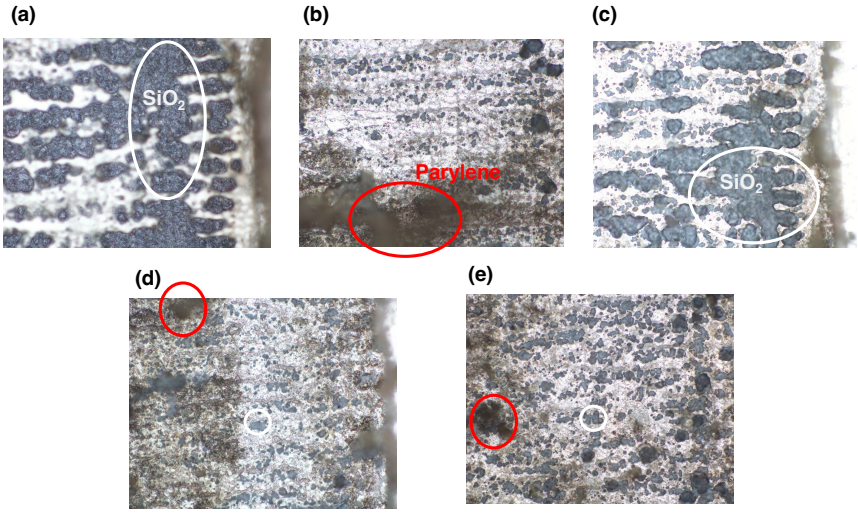


Figure 3.22: Parylene removal from 675 nm Al (1%Si) electrodes with different power, repetition, and cut speeds (a) Using 1 W, 3 repetitions, 2000 mm/s cut speed, (b) Using 1 W, 2 repetitions, 2000 mm/s cut speed, (c) 1 W, 2 repetitions, 1500 mm/s cut speed, (d) Using 1 W, 2 repetitions, 1100 mm/s cut speed, (e) Using 0.8 W, 1 repetition, 1000 mm/s cut speed

by the red circle). The grey areas in black circles are the areas where Parylene was removed and the metal exposed. In Fig.3.23 (b), parylene is significantly removed. Some small parylene residues remained (where the red circles are). Probing the wafer with a multimeter indicated that the openings were made. The metal layer seems a bit rough probably due to the laser hatching process.

Although the laser patterning of polymer deposited on a thicker metal layer resulted in better removal of parylene, the deposition of thicker Al on graphene resulted in delamination and cracks appearing on the tracks, electrodes, and contact pads as shown in Fig. 3.24. Therefore, 1475 nm thickness was the maximum Al thickness that could be achieved without any cracks.

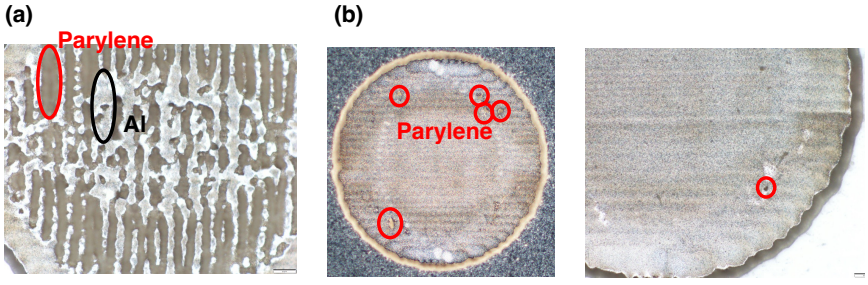


Figure 3.23: Parylene removal from 1475 nm Al (1%Si) electrodes with different power, repetition, and cut speeds (a) Using 0.3 W, 1 repetition, 1200 mm/s cut speed, (b) Using 0.3 W, 1 repetition, 800 mm/s cut speed

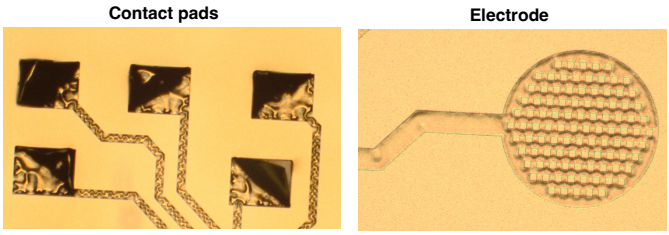


Figure 3.24: Delamination of thicker Al from graphene tracks

To conclude, two methods of plasma etching using a hard mask and laser patterning can be used to remove the polymer encapsulation layer from the electrode and contact pads. The plasma etching method is more complicated considering the challenges related to metal hard masks. However, based on the results of this work, it is recommended for thinner polymer layers (less than 10 µm). Choosing the right etching recipe can also help to minimize the metal hard mask deposition. In addition, having the Al(1%Si) on top of graphene helps to remove the fur-like residues from the electrode surface later in the fabrication process. On the other hand, laser patterning is more straightforward compared to plasma etching and it is recommended for the thicker polymer layers. Both methods should be optimized by changing the process parameters to ensure proper polymer removal from the electrodes.

3.8.3. CHARACTERIZATION: X-RAY PHOTOELECTRON SPECTROSCOPY (XPS)

XPS was used to evaluate any potential Mo residues under the graphene electrode after Mo removal. Two electrode samples were used for this experiment as shown in Fig. 3.25 (a). Mo was removed from one sample using H_2O_2 etching for 5 minutes. Mo on the other sample was not etched to make a comparison between the XPS measurement results. The stack of layers in each sample before and after Mo removal are shown in Fig. 3.25 (b). The optical image of the sample with Mo and with etched Mo are shown in Fig. 3.25 (c,d), respectively. The electrode looks shiny and yellow before Mo removal. The graphene electrode after Mo removal is observed before and after Ar backscattering. This is to remove graphene and reach the interface to investigate any potential residues left from Mo.

The XPS analysis was carried out in a vacuum (10^{-9} mbar) using an AXIS SUPRA (EMPC: PHI-TFA) XPS spectrometer, equipped with an Al-monochromatic X-ray source. The analyzed area was 110 µm in diameter and the analysis depth was approximately 10 nm. The survey spectra were collected from 0 to 1400 eV. Next, high-resolution multiplex scans of the measured peaks were recorded. The collected spectra were analyzed using Multipak v8.0 (Physical Electronics Inc.). To reach the interface and remove any potential contaminants, the surface was rastered using a 5 keV Ar ion beam.

Subsequent XPS measurements were conducted after 270 seconds of sputtering. The survey spectrum of the sample with Mo shown in Fig. 3.26 (a) indicates the presence of Oxygen (O1s), Molybdenum (Mo3d), Carbon (C1s), and Silicon (Si2s and Si2p). The wide scan spectrum of the sample without Mo is also shown in Fig. 3.26 (b, c) for before and

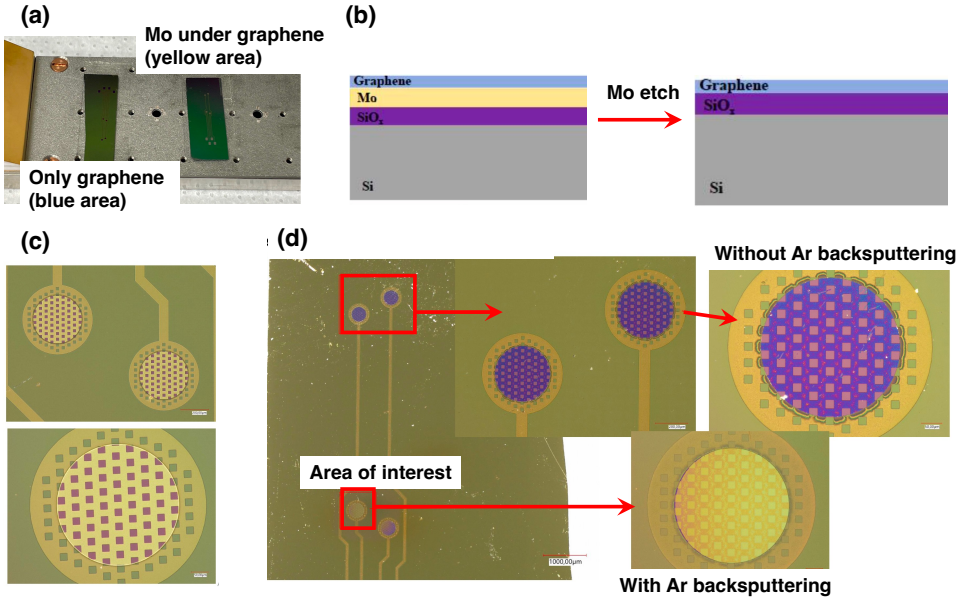


Figure 3.25: (a) Two samples used for XPS analysis one with graphene on Mo and the other one with only graphene after Mo etch, (b) Stacks of layers before and after Mo etch, (c) Optical image of graphene electrodes on Mo catalyst, (d) optical image of graphene electrodes after Mo etch with and without Ar backscattering.

after Ar backscattering, respectively.

There is a reduction in C1s peak and an increase in O1s peak after Ar sputtering due to the removal of graphene and reaching the underlying SiO_2 layer, however, no indication of Mo is detected. The high-resolution XPS spectra for these samples, shown in Fig. 3.27, indicate the same result with more details. The high-resolution spectra are also evaluated for the potential Mo peak, however, no peak could be detected above the noise level.

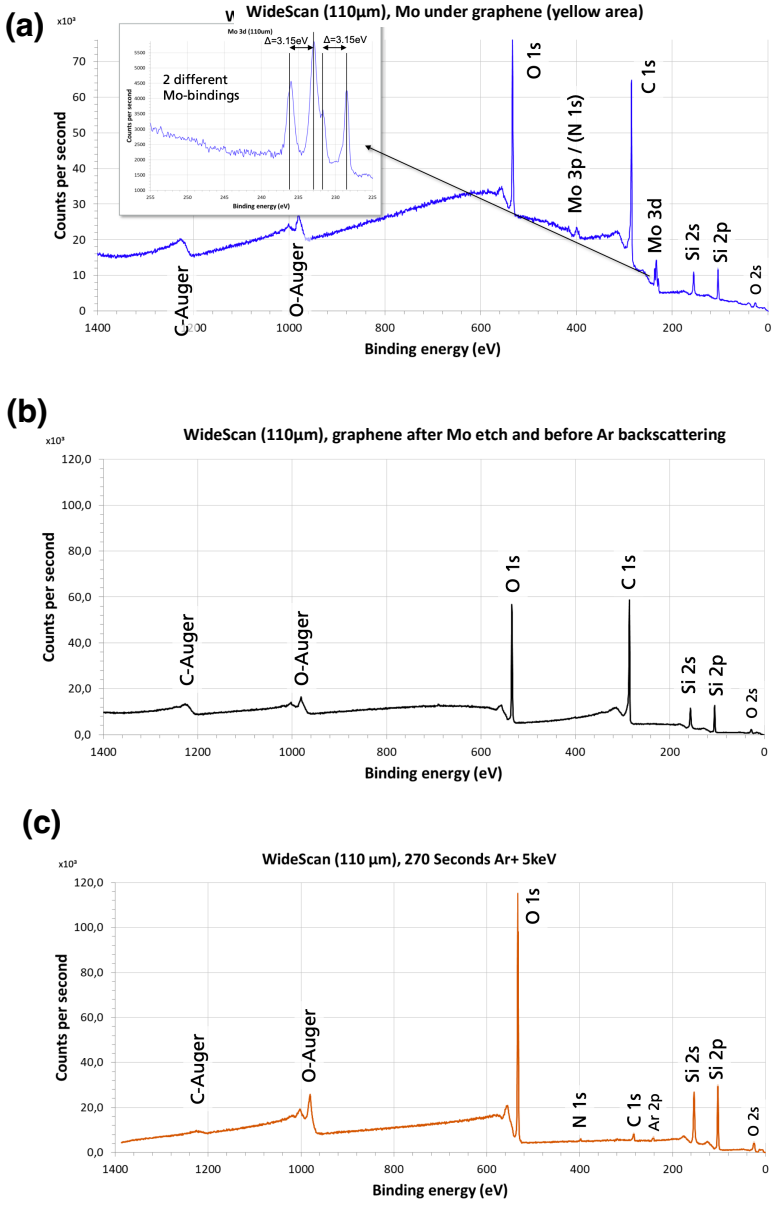


Figure 3.26: (a) Wide scan spectrum of the sample with Mo, (b) Wide scan spectrum of the graphene sample after Mo etch and before Ar backscattering, (c) Wide scan spectrum of the graphene sample after Mo etch and after Ar backscattering.

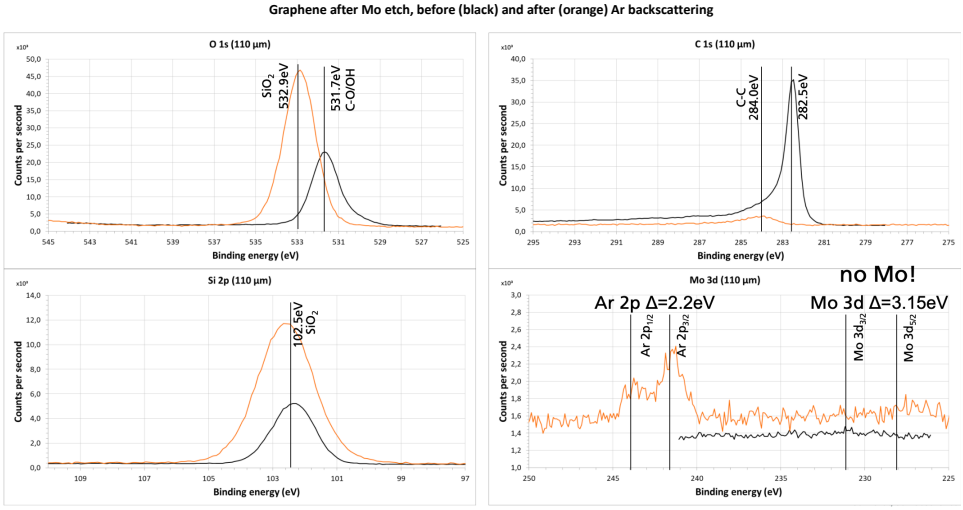


Figure 3.27: (a) High-resolution spectra of O1s, C 1s, Si 2p, and Mo 3d before (black) and after Ar backscattering (orange).

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4

GRAPHENE SURFACE MODIFICATION WITH NANOPARTICLES

This chapter has been published in [1].

This chapter discusses graphene surface modification with platinum nanoparticles using the spark ablation method. First, a brief introduction is given on electrode surface modification and why it is needed. Then, the method used in this thesis is explained. Later, graphene electrodes without and with coatings are electrochemically characterized and compared. Finally, the electrochemical and mechanical stability of the printed nanoparticles are discussed. The following sections are based on a published article in the Journal of NanoScale, therefore, repetitions are unavoidable.

4.1. SURFACE MODIFICATION OF GRAPHENE NEURAL ELECTRODES

Abstract: In this paper, we present the surface modification of multilayer graphene electrodes with platinum (Pt) nanoparticles (NPs) using spark ablation. This method yields an individually selective local printing of NPs on an electrode surface at room temperature in a dry process. NP printing is performed as a post-process step to enhance the electrochemical characteristics of graphene electrodes. The NP-printed electrode shows significant improvements in impedance, charge storage capacity (CSC), and charge injection capacity (CIC), versus the equivalent electrodes without NPs. Specifically, electrodes with 40% NP surface density demonstrate 4.5 times lower impedance, 15 times higher CSC, and 4 times better CIC. Electrochemical stability, assessed via continuous cyclic voltammetry (CV) and voltage transient (VT) tests, indicated minimal deviations from the initial performance, while mechanical stability, assessed via ultrasonic vibration, is also improved after the NP printing. Importantly, NP surface densities up to 40% maintain the electrode optical transparency required for compatibility with optical imaging and optogenetics. These results demonstrate selective NP deposition and local modification of electrochemical properties in graphene electrodes for the first time, enabling the cohabitation of graphene electrodes with different electrochemical and optical characteristics on the same substrate for neural interfacing.

4.2. INTRODUCTION

In recent years, the combination of complementary methods such as optical and electrical neural recording and stimulation has enabled a deeper understanding of the brain and deciphering neural behavior to advance the treatments and therapies for disorders and diseases related to the nervous system.

Optical imaging [2, 3] together with electrophysiology, the method used for neural activity recording, have been employed to target specific biological structures and identify cell types. The combination of optogenetics with electrophysiology has also attracted great attention in neuroscientific research in recent years to pave the way towards a much deeper understanding of the nervous system [4, 3, 5].

However, conventional metal-based electrodes, mostly used in neural interface devices, are not the best candidates to combine electrical and optical neural measurement methods. Such electrodes obstruct the field of view in optical imaging due to metal opacity. Moreover, light illumination on the metal electrode surface might generate photo-induced artifacts that can interfere with the recorded electrical signal [6, 7]. Therefore, the development of transparent conductive materials has increased rapidly to substitute metal electrodes.

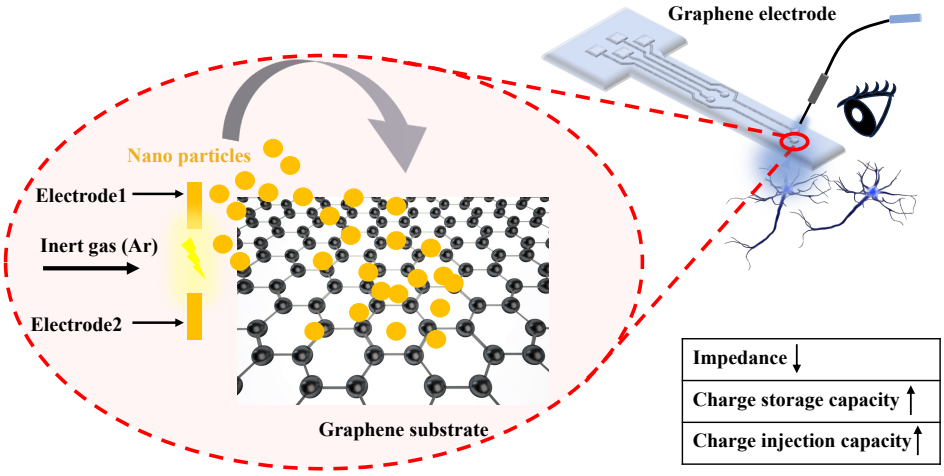

Figure 4.1: Graphical abstract

Graphene with a high thermal/electrical conductivity and broad-spectrum transparency [8] could be grown using a chemical vapor deposition (CVD) technique which is compatible with micro-fabrication process steps. Monolayer CVD graphene with high optical transparency has shown compatibility with optical imaging and optogenetics [9]. However, undoped monolayer graphene suffers from low sheet conductivity [10] and a low charge storage capacity (CSC) due to the dominance of its small quantum capacitance [11].

Recently developed multilayer CVD graphene electrodes, using a transfer-free fabrication process, reported an increase in CSC and impedance reduction due to an increase in the quantum capacitance as a result of using multiple graphene layers [12, 13]. However, increasing the number of layers has only impact on the quantum capacitance up to a threshold of 6 layers [11], while each added layer reduces the graphene's optical transparency [14, 12].

Moreover, scaling down the electrode size is necessary to selectively record signals from targeted neurons [15, 16]. However, a size reduction is accompanied by an increase in impedance, which causes an increase in the amount of noise (voltage) from the electrodes:

$$\text{Vnoise} = \sqrt{4\text{kTRe}(\text{Z})\Delta\text{f}} \tag{4.1}$$

where k is Boltzmann's constant, T is the temperature, Z is the electrode impedance, and Δf is the frequency band of interest [17, 18].

Thus, to obtain a low impedance with small-size electrodes, various strategies have been investigated. The surface modification techniques, used in the literature, mostly rely on increasing the surface roughness or improving the impedance and CSC by additional electrochemical means [19].

Various materials have been applied to modify the graphene electrode surface, including nanoparticles (NPs) [20], carbon nanotubes (CNTs) [21, 22], and conductive polymers such as poly(3,4-ethylene dioxythiophene) (PEDOT) [23, 24]. NPs, specifically, have a larger surface-to-volume ratio compared to bulk materials. Therefore, the deposition of NPs on electrodes has been shown to lower the impedance [25]. Furthermore, the surface topography of electrodes can improve the cell adhesion to the electrode surface and, therefore, improve signal quality [26].

Graphene doped with $AuCl_3$ (Au NPs) resulted in a greater reduction in sheet resistance compared to HNO_3 doping with similar optical transmittances [27]. Electrodeposition of platinum (Pt) NPs on reduced graphene oxide (rGO) [28, 29], and on functionalized graphene sheet [30] has been shown to enhance their electroactivity. Recently, graphene neural electrodes with electrodeposited Pt NPs showed a reduction in the impedance and a CV enlargement for an increased Pt deposition time [20]. It has been suggested that creating an alternative conduction path with Pt NPs at the electrode-electrolyte interface could increase the small quantum capacitance [20]. Moreover, the amount of faradaic charge transfer over the electrode-electrolyte interface increases due to the high charge injection capability of Pt which increases the CSC [20].

The current techniques used for surface modification of the electrodes with NPs are mostly based on electrochemical depositions. The NP coating formation by these methods is highly time-consuming and hard to control, which results in limited reproducibility and mass production [31]. Moreover, the NP coating process step optimised and integrated into the fabrication process of specific electrodes may not easily be applicable to other types (material and electrode size) of electrodes [19]. Furthermore, single (individual) electrode surface modification is not always possible and usually comes at a high cost and process complexity. On the other hand, the spark ablation method provides the possibility of NP printing at room temperature and in a dry process. Due to the use of ultra-pure carrier gas and electrode material(s), the printed NPs are highly pure and residue-free unlike the NPs produced by the electrochemical deposition in which contain residues and contamination associated with the liquid [32].

The aim of this paper is the direct surface modification of multilayer graphene electrodes with Pt NPs using the spark ablation method to enhance the electrochemical performance of the electrode. This versatile method is based on gas-phase electro-deposition, which prevents the exposure of the electrodes to any chemicals. It is capable of single-step local NP impaction printing and is compatible with the existing microfabrication process as a post-processing step. Due to its local nature, this technique opens up new possibilities in neural interface design for multimodal tissue interaction. For instance, it enables the coexistence of smaller size electrodes, which need better electrochemical characteristics, with larger electrodes, requiring higher optical transparency, on the same substrate.

4.3. METHODS

4.3.1. SAMPLE PREPARATION

FABRICATION PROCESS

The multilayer graphene electrodes have been fabricated using a previously reported fabrication process [12]. The fabrication process, shown in Fig. 4.2(a), starts with an oxide growth on the front side of a silicon (Si) wafer followed by a molybdenum (Mo) deposition and patterning. Then, graphene is selectively grown on pre-patterned Mo. Next, an aluminum (Al) / titanium (Ti) stack is sputtered and photolithographically patterned. These steps are added to the previously reported fabrication process flow to allow for wire bonding on the contact pads. Next, the photoresist (PR) is spin-coated as an insulation layer and patterned on the electrodes and contact pads. Finally, Mo underneath the graphene electrodes is etched, leaving the graphene in the exact same location as defined by the catalyst. This is shown in the cross-sectional view of the graphene electrode before and after etching Mo in Fig. 4.2(a). The fabrication process is explained in detail in the supplementary notes. The optical image of the final device with four electrodes is shown in Fig. 4.2(b). The electrode diameter is 340 µm which leads to 68320 μm^2 surface area after subtracting the holes' surface area (these holes are considered in the mask design as explained in [12]).

At the end of the fabrication process, the Si wafer is diced and an epoxy die adhesive is used to attach one device to a printed circuit board (PCB) for further testing (Fig. 4.2(c)). Next, the Al contact pads are Au wire-bonded to the PCB pads. The contact pad and the attached wire are both covered with a drop of Polydimethylsiloxane (PDMS) for mechanical protection. At this stage, some preliminary measurements are performed to characterize the graphene electrodes (pre-NP measurements). Next, the electrodes are ready for NP printing and post-NP measurements.

NP PRINTING

A spark ablation method is employed to print NPs on the electrodes. The process consists of three steps: generation, particle processing, and deposition as illustrated in Fig. 4.3. A generator (VSP-G1) is connected to a prototype nanostructured material printer (VSP-P0) (VSPARTICLE BV, the Netherlands). The generator initiates periodic electrical discharges between two metal rod electrodes of a desired conductive material and an inert gas flow (Nitrogen (N_2)) carries the NPs to the substrate in the deposition chamber.

The substrate is mounted on the stage in the vacuum chamber perpendicular to a 3D-printed converging nozzle with a 0.35 mm diameter as shown in Fig. 4.3. This nozzle is connected to motors that can navigate in the x,y, and z directions, creating a local printing process. The nozzle aerodynamically focuses the NPs and deposits them on the substrate by impaction [33]. In this work, Pt (99.9% purity) rod electrodes with diameters of 3 mm are used to create Pt NP coating on graphene electrodes.

OPTIMISATION OF NP PRINTING SETTINGS

The printer settings are optimised to get three different surface densities of NPs, namely 15%, 30%, and 40%. The spark is generated with 1 kV and 3 mA current and the printings are performed under ambient pressure with nitrogen (99.995% purity) as a carrier gas at a flow rate of 1.5 l/min.

First, NP printing is performed on silicon dies from a nozzle height of 0.5 mm in single-line patterns by varying printing speeds. Then, the Si dies are inspected by scanning electron microscopy (SEM), and the corresponding images are analyzed to calculate

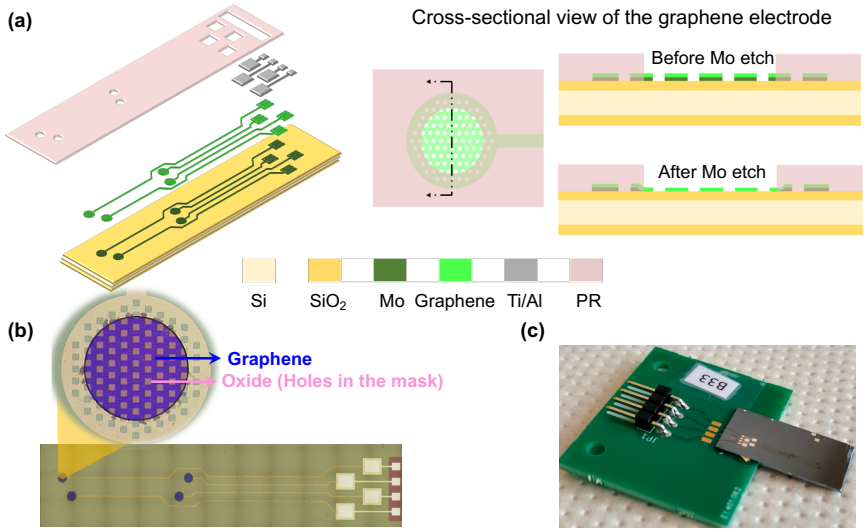

Figure 4.2: (a) Fabrication process steps of graphene electrodes on a Si substrate. First, the oxide is deposited on the front side of a Si wafer followed by Mo deposition and patterning. Then, graphene is grown on a Mo catalyst. Next, Al/Ti is deposited and patterned on the contact pads. Finally, PR is spin-coated and patterned as an insulation layer and Mo is removed from the electrode sites, leaving graphene contacts (as shown in the cross-sectional view of the graphene electrode). (b) Optical image of the final device with four electrodes. (c) The final device attached and wire-bonded to a PCB.

the obtained NP densities per each printing speed. Finally, the printing speed to achieve the required NP density is chosen.

For each printer setting, the resulting NP density is determined by averaging the surface density of three SEM images from the same deposition batch. These images are taken with a 2 kV electron beam and 50000x magnification (using a Hitachi Regulus 8230). First, the grey-scale SEM images are converted to black and white (binary) images using MATLAB R2019b (of MathWorks). The pixels whose value is above a certain threshold are replaced with white, representing the area covered with NPs, and the pixels with values below the threshold are considered black. Otsu's method [34] is used to determine the optimal threshold to convert the grey-scale images into binary images. The percentage of white pixels out of all pixels is considered the density of the NPs.

To ensure that the width of the printed NP line is sufficient to cover the electrode surface, it is necessary to measure the line width. SEM images taken at low magnification (x50) at a 2kV accelerating voltage are used for this purpose. The grey-scale images are converted to binary images through Otsu's thresholding method. The data matrix includes columns of 0s and 1s and the longest series of 1s across a column is considered the width. The average length of that data matrix is then used as the width of the printed line. This value is subsequently converted to millimeters using ImageJ (an image analysis program developed at the National Institute of Health [35]).

It should be noted that the printed line should not conduct electricity to prevent enlarging the circular electrode surface area into an extended line. To ensure low conduc-

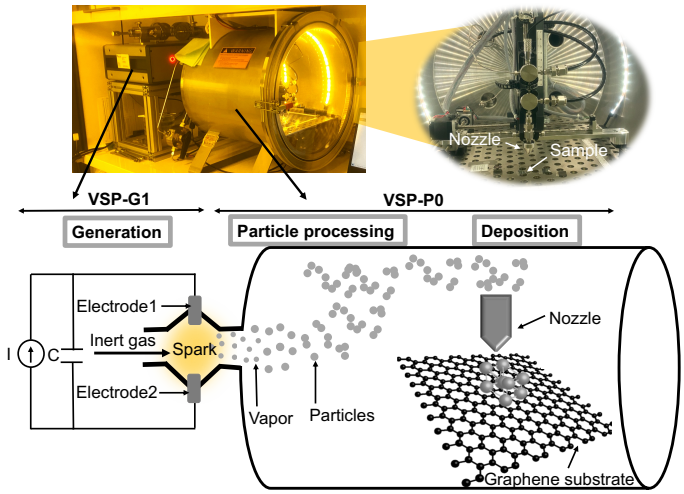

Figure 4.3: Schematic view of the spark ablation method system (VSPARTICLE BV, the Netherlands) used for NP printing.

tivity of the printed NP lines, a conductivity measurement is performed using a four-point probe (Cascade Microtech probe station) on gold Van der Pauw structures covered with an NP line with the same density printed over them.

4.3.2. ELECTRODE CHARACTERIZATION

ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY

Electrochemical impedance spectroscopy (EIS) is employed to assess the electrochemical properties of the graphene electrodes with and without NP coating. The measurements are performed in a phosphate-buffered saline (PBS) solution in a three-electrode configuration set-up using a potentiostat (Autolab PG-STAT302N). A Pt electrode (3 mm diameter (BASI Inc.)) is used as a counter electrode, a leakless miniature silver/silver chloride (Ag/AgCl) (eDAQ) as a reference electrode, and the graphene electrodes(with and without NPs) fabricated in this work as the working electrodes. A 10-mV RMS sinusoidal voltage is applied between the working and reference electrodes and the current between the working and counter electrodes is measured [36]. Finally, the impedance magnitude and phase angles are plotted as a function of frequency ranging from 1 Hz to 100 kHz.

CYCLIC VOLTAMMETRY

Cyclic Voltammetry (CV) is an electrochemical surface analysis technique used for investigating charge transfer reactions of an electrode surface. CSC is calculated as the time integral of the CV curve and is reported as charge per electrode surface area. This value estimates the total charge transferred to the electrode and has been used as a common practice to compare stimulation electrodes [37, 36]. CV measurement is performed using the same three-electrode setup. To ensure a safe measurement for both materials (Pt and graphene) and facilitate the comparison between pre-NP and post-NP measure-

ments, the overlap (-0.6 V to 0.6 V) between the previously used water window ranges for graphene (-0.8 V to 0.6 V) and Pt (-0.6 V to 0.8 V) is chosen [12]. The measurements are performed at various scan rates (0.1 V/s, 0.2 V/s, 0.6 V/s, and 1 V/s) 3 times to ensure that the third stabilized cycle is used for the calculation of the CSC. Both the total and cathodic CSC are calculated and expressed in $\mu C/cm^2$ after dividing the calculated charge (based on the third scan) by the electrode surface area.

VOLTAGE-TRANSIENT MEASUREMENTS

Voltage-transient (VT) measurements are used to estimate the maximum charge that can be injected by an electrode by applying a constant-current stimulation pulse [36, 37, 38]. This measurement is performed in the same three-electrode setup as well. A cathodic-first biphasic symmetric current pulse (1 ms pulse width, 100 µs interphase delay) is applied between the working and counter electrodes in the PBS solution. The voltage between the working electrode and the reference electrode is then evaluated. This voltage consists of a resistive voltage drop at the beginning of the cathodic pulse followed by a gradual voltage decrease due to the capacitive charging of the electrode-electrolyte interface. The interface polarization of the electrode is evaluated by eliminating the resistive voltage drop from the minimum voltage. The interface polarization should not exceed the water window extracted from CV. The maximum cathodic-current amplitude is the maximum current in which the interface polarization reaches the cathodic water window. Finally, the maximum charge-injection capacity (CIC) of the electrode is calculated based on the maximum current amplitude multiplied by the pulse width and divided by the electrode surface area [38].

4.3.3. STABILITY ASSESSMENTS

Printing NPs on the graphene electrode surfaces is performed to reduce the electrode impedance and increase the CSC. This electrochemical improvement should remain stable for the lifetime of the device. Coating stability includes both electrochemical and mechanical stability, meaning the electrode should maintain its electrochemical improvement and the coating should not delaminate from the electrode surface. Therefore, the electrochemical and mechanical stability of the NPs must be verified prior to any electrode implantation in the body.

To this aim, continuous CV and VT tests are performed to ensure the electrochemical stability of the electrodes. Finally, an ultrasonic vibration test is performed to evaluate the mechanical stability of the NP coating.

CONTINUOUS CV MEASUREMENT

Continuous CV measurements are commonly used to evaluate the electrochemical stability of the electrodes [39]. Three samples per each electrode type are subjected to 500 CV scanning cycles at a fast scan rate of 1 V/s. EIS measurements are then performed to evaluate any changes in the impedance. The impedance of the electrodes at 1 kHz is reported before and after this test. To additionally investigate whether the Pt NPs are present on the electrode surface after 500 CV cycles, energy-dispersive X-ray spectroscopy (EDX) measurement is performed on the electrode with NP coatings.

CONTINUOUS VT MEASUREMENT

A continuous VT test is performed by applying cathodic-first biphasic current pulses to the electrode. A current amplitude of 2.5 µA with a 1 ms pulse width and 1 µs interphase delay with a frequency of 333 Hz is applied. The number of cycles is kept at 500,000 as the Mo layer underneath the graphene tracks started to corrode. The test is conducted for two electrodes: one graphene electrode without any NP coating and one graphene electrode with 40% NP coating. The characterization of the electrodes is performed before and after the continuous VT test by performing Raman spectroscopy, EIS, and CV measurements.

ULTRASONIC TEST

The stability of the NPs on the electrode surface is additionally tested by ultrasonic vibration using a digital ultrasonic cleaner (HBM Machines). Four electrodes, two graphene electrodes without any coatings, and two graphene electrodes with 40% Pt NPs are submerged in a water bath of 250 ml at 30 W power, 22 kHz frequency for 2 minutes. Optical images of the electrode surface are taken before and after this test. EIS measurements are also performed as any changes in the impedance might reveal a change in the surface properties and the delamination of NPs from the electrode surface.

4.4. RESULTS

4.4.1. NP PRINTING

Fig. 4.4(a) shows the SEM images of NPs printed on Si dies with the required surface densities. The corresponding binary image of 40% Pt NPs is also depicted. The settings and parameters used for Pt NP printing are shown in Table S1 in the supplementary notes. The resulting printed line width, calculated from the binary images for the various NP densities, is also reported in this table. In all cases, the lines are wide enough to ensure that NPs are printed on the entire electrode surface with a diameter of 340 µm.

Furthermore, the results of the conductivity measurement can be found in Fig. S1 in the supplementary notes. The measurement on the printed Pt NP lines over gold Van der Pauw structures shows a significant current flow for NP surface densities of 50%. Therefore, the NP surface density is kept below 40% for this study to prevent any potential extension of the graphene electrode surface to the printed line, as this would influence the electrochemical tests. Conductivity measurements for these lower densities, discussed in the supplementary notes, indicated this has not been the case.

Fig. 4.4(b) shows the optical images of a graphene electrode before and after 15% Pt NP printing. NPs can be seen in the zoomed-in image and an obvious color change in the electrode surface is observed as a result of the presence of NPs.

The Raman spectrum of the graphene with and without Pt NPs is displayed in Fig. 4.4(c). The spectrum of graphene with 40% Pt NPs is shown in green and the spectrum before printing NPs on graphene is displayed in black as a reference. Three distinct peaks can be observed for both spectra: a D peak at 1354 cm^{-1}, a G peak at 1582 cm^{-1} related to the sp2 C-C bonds forming the graphene lattice, and a 2D peak around 2709 cm^{-1}. No differences are observed in the average intensity ratio of the D to G peaks (I(D)/I(G)) after NP printing (0.19 for graphene and 0.17 for graphene with Pt NPs), implying that Pt NPs did not affect the defect density of graphene. A possible explanation is that nanoparticles

are small and sparsely distributed over the surface and they do not have sufficient kinetic energy to cause defects. The mechanism of printing NPs probably results in physically adsorbed clusters causing NPs to have minimal interaction with the graphene lattice.

The optical transmission of multiple surface densities of Pt NP on a glass slide (after removing the effect of the glass slide) versus the wavelength is shown in Fig. 4.4(d). The optical transmittance measurement was not directly performed for 40% NP surface density. The result shown in the graph is the interpolation of the optical transmittance of 30% and 50% (not shown) NP densities. As shown in the graph, the optical transmittance of the NPs with 40% surface density is still above 92% over a wide range of wavelengths.

The surface roughness measurement on the printed Pt NPs on Si dies is performed for five samples per surface density. The average and standard deviation of RMS and mean surface roughness for each NP surface density are reported in Table S2 in the supplementary notes. The reported values show a higher average for both RMS and mean roughness by increasing the NP surface density from 15 to 40% (from 9 to 14.67 nm for RMS and from 7.1 to 12 nm for mean surface roughness). An increase in the standard deviation of both RMS and mean surface roughness by increasing the NP density confirms the non-uniformity of printed NPs over the surface. It should be noted that the surface roughness of multilayer graphene electrodes with the same growth condition was reported to be 6.75 nm [12] which is smaller than the surface roughness of printed Pt NPs.

More information on the measurement methods for Raman spectroscopy, optical transmittance, and surface roughness measurements can be found in the supplementary notes.

4.4.2. ELECTRODE CHARACTERIZATION

ELECTRODE IMPEDANCE SPECTROSCOPY

EIS measurements are performed for graphene electrodes without and with NP coatings with various surface densities. The average impedance magnitude and phase angle of 7 graphene electrodes without any Pt NP coatings and 5 graphene electrodes with Pt NPs per each set of NP surface density (5 electrodes with 15% Pt NPs, 5 electrodes with 30% Pt NPs, and 5 electrodes with 40% Pt NPs) are shown in Fig. 4.5(a). A 2-times reduction in the impedance magnitude at 1 kHz is observed after adding the NPs with 15% surface density to the graphene-electrode surface. The graphene-electrode impedance decreased even further by printing 40% NPs from 31.45 kΩ to 7.26 kΩ (leading to a 4.5 times impedance reduction). The average impedance and the area-normalized impedance of the electrodes at 1 kHz before and after NP printing for various NP surface densities are represented in Table 4.1.

CYCLIC VOLTAMMETRY

The CV curves of the median sample of each sample group including graphene electrodes with and without NP coatings for various scan rates are shown in Fig. 4.5(b). An enlargement of the CV curve is clearly observed after increasing the surface density of the NPs. In addition, oxide reduction peaks at 0.1 V and hydrogen adsorption peaks at −0.4 V indicate the engagement of Pt NPs in the charge-transfer process at the electrode/electrolyte interface [37]. The calculated total and cathodic CSC of each electrode

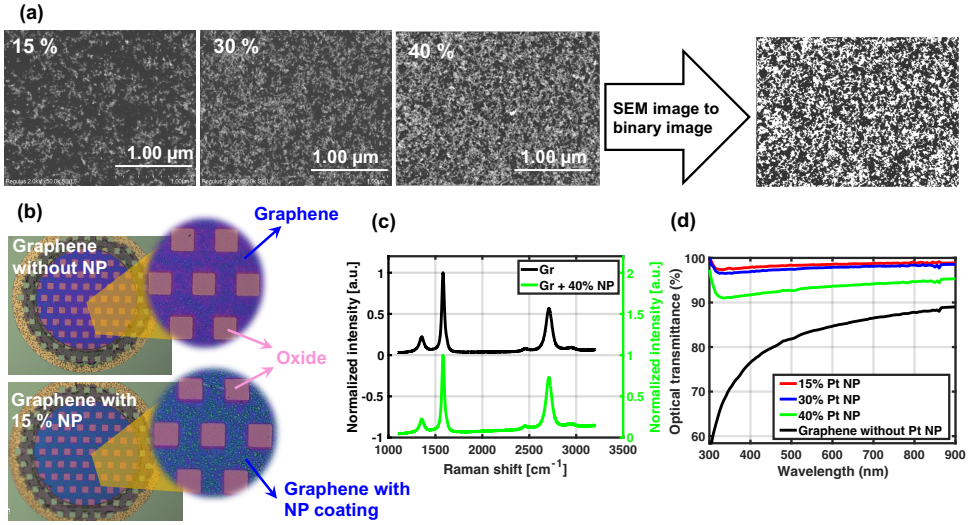

Figure 4.4: (a) The original grey-scale SEM images after calculating the surface density of NPs, with the corresponding binary image of 40% NP density, (b) The optical image of graphene electrode before and after 15% NP printing, (c) Raman spectroscopy measurement of graphene without and with 40% Pt NPs, (d) Optical transmittance of multiple densities of Pt NPs (15, 30, and 40%) on glass slide are shown after removing the effect of the glass (the optical transmittance of 40% Pt NP is interpolated from 30% and 50% NP densities). Optical transmittance of graphene without Pt NP coating (after removing glass contribution) is added as a reference.

Table 4.1: Impedance, CSC, and CIC of graphene, without and with Pt NPs with surface densities of 15%, 30%, and 40%.

Measurement results			Graphene	Graphene + 15% Pt NPs	Graphene + 30% Pt NPs	Graphene + 40% Pt NPs
Impedance at 1 kHz (kΩ)			31.45 ± 5.88	14.29 ± 0.95	9.32 ± 0.80	7.26 ± 0.90
Area-normalized impedance (Ω.cm^2)			21.49 ± 4	9.8 ± 0.6	6.4 ± 0.5	4.96 ± 0.6
CSC (µC/cm^2)	Total	1V/s	248 ± 185	551 ± 73	745 ± 91	954 ± 103
		0.6V/s	349 ± 272	778 ± 109	959 ± 159	1199 ± 99
		0.2V/s	817 ± 666	1887 ± 268	1960 ± 504	2444 ± 368
		0.1V/s	1566 ± 1277	3497 ± 495	3399 ± 1062	4365 ± 821
	Cathodic	1V/s	78 ± 52	345 ± 84	469 ± 73	651 ± 45
		0.6V/s	95 ± 63	496 ± 146	625 ± 118	878 ± 88
		0.2V/s	159 ± 102	1211 ± 439	1327 ± 367	1993 ± 429
		0.1V/s	233 ± 146	2197 ± 849	2207 ± 746	3614 ± 892
Max. current amplitude (µA)			5.7 ± 1.5	8.6 ± 1.3	12.5 ± 1.5	20.9 ± 1.2
CIC (µC/cm^2)			8.4 ± 2.1	12.6 ± 1.9	18.3 ± 2.2	30.6 ± 1.8

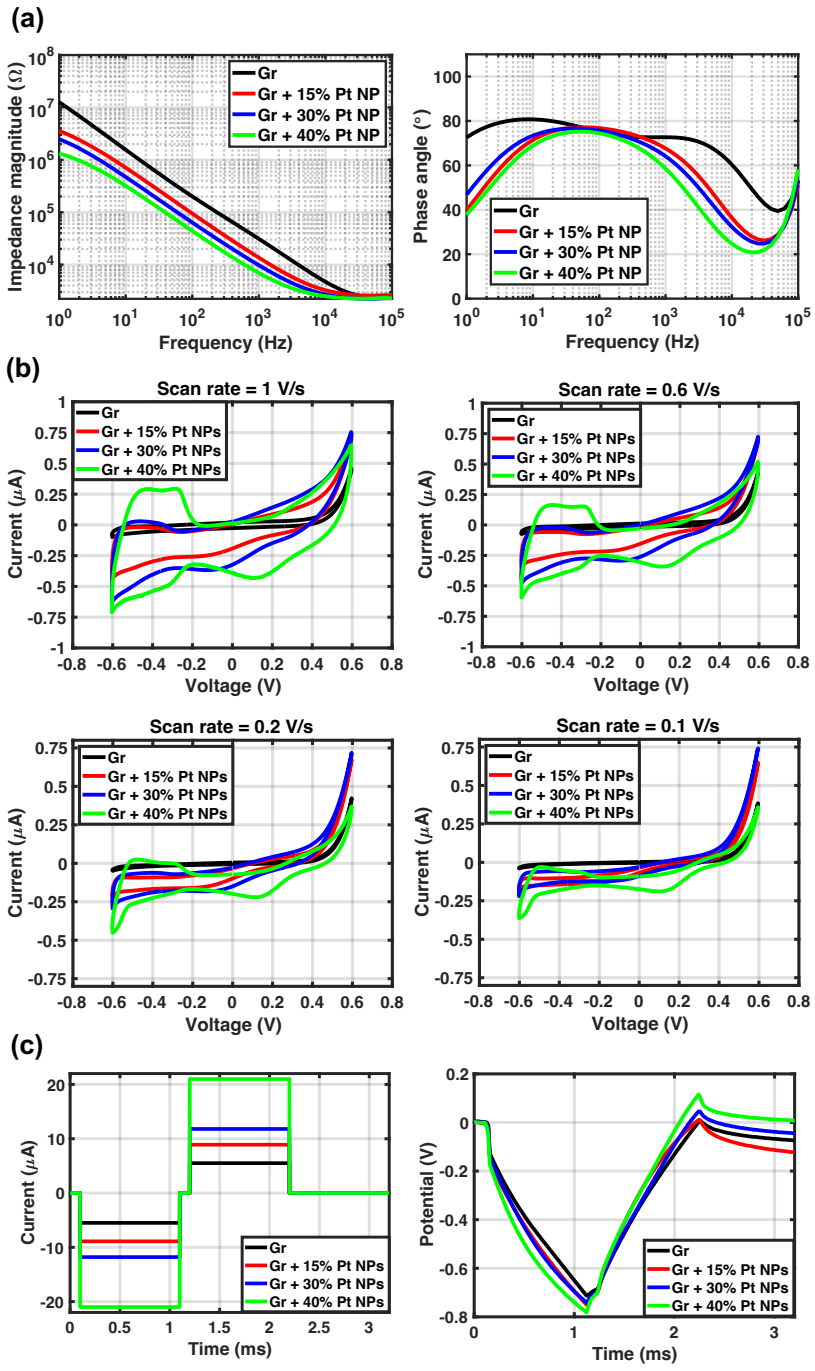

Figure 4.5: (a) Average EIS results of 7 samples per graphene without Pt NPs and 5 samples per each set of NP surface densities, (b) CV curves of the median sample of each category of graphene without and with NPs with different surface densities, (c) The median of the maximum-amplitude current pulse applied to 5 electrodes per each category of different NP densities with the corresponding VT measurement.

are represented in Table 4.1. As shown, a CSC increase correlates with an increase in the surface density of NPs on the electrode surface, and a 40% NP coating improves the CSC 15 times compared to that without NPs (from 233 μC/cm^2 to 3614 μC/cm^2).

VOLTAGE-TRANSIENT MEASUREMENTS

The maximum current amplitudes and measured voltages for the median samples of each sample group with respect to the (Ag/AgCl) reference electrode are shown in Fig. 4.5(c). An increase is observed in the maximum current pulse amplitude applied to the electrode by increasing the NP surface density, consequently resulting in an increase in the calculated maximum CIC of up to 3.5 times, as shown in Table 4.1.

4.4.3. STABILITY ASSESSMENT

CONTINUOUS CV MEASUREMENT

Continuous CV tests are performed for graphene electrodes with and without NPs for three electrodes per each type for 500 cycles. The CV curves of one representative graphene electrode without NP and one with 40% Pt NP after 3, 250, and 500 CV cycles are shown in Fig. 4.6(a). A slight increase in the area of the CV curve (4.7% increase in total CSC) of graphene electrodes without coating is observed. The corresponding EIS measurement before and after 500 cycles of CV are also shown for these electrodes in Fig. 4.6(a). A small reduction (only 3%) in the impedance of the graphene electrode is observed which might be related to surface cleaning and contamination removal of the electrode surface.

A CV enlargement is observed for 7 out of 9 graphene electrodes with Pt NP coating after 500 cycles of CV (shown in Table S3 in the supplementary notes). A shoulder at 0.25 V is observed that corresponds to oxide formation, and a peak at 0.10 V is attributed to the oxide reduction. Peaks for hydrogen adsorption and desorption were also observed around -0.40 V as reported previously [37]. Comparing the CV curves after 250 and 500 cycles shows that the CV curve seems to be stabilized and no significant change is observed after 250 cycles. Although the CV enlargement is observed for graphene electrodes with various Pt NP densities after 500 CV cycles, the electrodes with 40% NPs show the largest increase in CSC of around 16.9%. This can be related to more oxidation and reduction as a result of more Pt NPs and, therefore, higher peaks in CV. The CV curve reduction of 2 out of 9 electrodes is inconclusive and cannot be attributed to the delamination of Pt NPs. To draw any conclusions, more samples should be tested and the number of CV cycles should be also increased.

The impedance of 7 out of 9 graphene electrodes with Pt NPs shows an average of 15% increase. This increase could be attributed to Pt NP delamination which could increase the impedance. However, if there is any delamination of NPs the CSC is expected to decrease. It might be argued that the appearance of the peaks related to oxidation and reduction compensates for the NP delamination. However, if this were the case, the delamination is expected to continue even after 250 CV cycles.

Finally, the EDX measurement on the electrode surface after a continuous CV test (shown in Fig. S2 in the supplementary notes) confirms the presence of the coating by showing Pt peaks corresponding to Pt NPs.

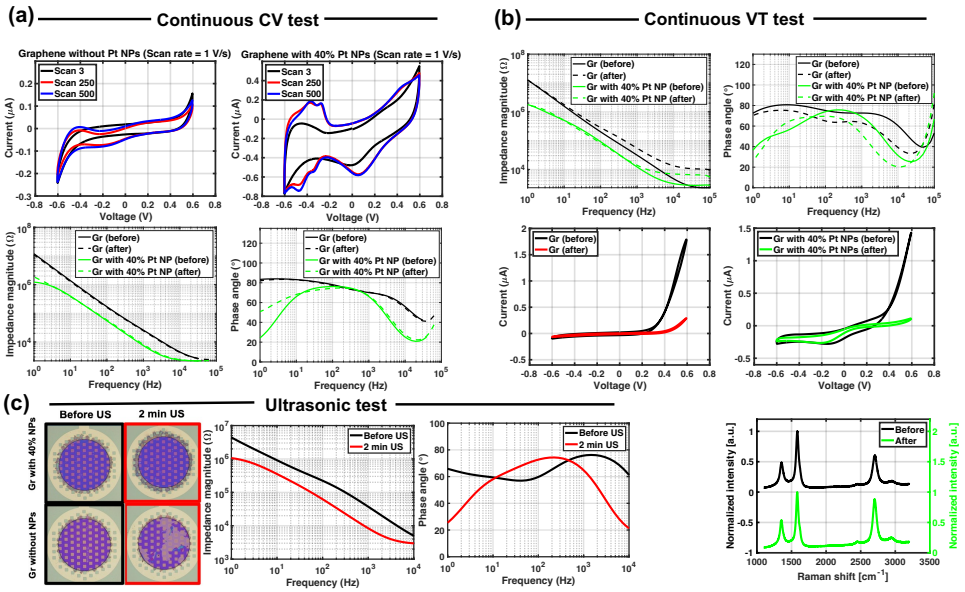

Figure 4.6: Stability assessment results. (a) Continuous-CV test results: CV curves of graphene without NP and graphene with 40% NP after 3, 250, and 500 cycles, and impedance magnitude and phase plot of graphene without NP and with 40% NP before and after 500 cycles of CV, (b) Continuous VT test results: impedance magnitude and phase plot of graphene electrodes without and with 40% NP coatings before and after 500,000 cycles of VT test, CV curves of graphene electrodes without and with 40% Pt NP coatings before and after continuous VT test, and Raman spectra of a graphene electrode with 40% NP coatings before and after continuous VT test, (c) Ultrasonic test results: an optical image of graphene electrodes with and without NPs before and after 2 minutes of ultrasonication, and impedance magnitude and phase plot of graphene electrode with 40% NP density before and after 2 minutes of ultrasonication.

CONTINUOUS-VT MEASUREMENT

EIS plots of graphene without and with 40% Pt NPs are shown in Fig. 4.6(b) before and after this test. An increase in the impedance at 1kHz (from 34.53 kΩ to 54.88 kΩ) is observed for the graphene electrode without NP coating which could be related to the small delamination of graphene from underlying oxide. This delamination could be responsible for the slight increase also observed in the impedance at 1 kHz for graphene with 40% NP coatings (from 6.7 kΩ to 9.75 kΩ). A significant delamination of NP from the graphene layer is unlikely to be occurring, as the impedance curve remains about an order of magnitude lower for the NP-coated electrodes throughout the frequency spectrum. An impedance increase at high frequencies could be attributed to the corrosion of Mo underneath the graphene tracks.

CV curves for graphene electrodes without and with 40% NP coating are shown in Fig. 4.6(b). In both cases a reduction in the CV area is observed after 500,000 cycles of the VT test, indicating some electrochemical change in the graphene electrode. However, the CSC for the NP-coated electrodes remains higher than the one of graphene only, further suggesting the presence of NP still after the continuous-VT test.

The Raman spectra acquired on the graphene electrode with 40% NP coating be-

fore and after this test show three graphene characteristics, confirming the presence of graphene after the continuous-VT test as shown in Fig. 4.6(b). However, the I(D)/I(G) ratio slightly increased from 0.2 to 0.35 probably due to the defects induced into the graphene lattice. This ratio did not change for the graphene electrode without any coatings.

ULTRASONIC TEST

Some of the samples are additionally subjected to ultrasonic treatment to investigate its effect on the NP adhesion to the electrode surface. However, the test samples are not optimized for this test, hence the test could not be performed for long durations due to the delamination of graphene from the underlying oxide layer on the test samples (shown in Fig. 4.6(c)). Nevertheless, the samples with NPs remain stable after 2 minutes of ultrasonic treatment as shown in Fig. 4.6(c). The impedance magnitude of the graphene sample with NPs (Fig. 4.6 (c)) shows a decrease after 2 minutes of ultrasonication. Graphene delamination from the underlying oxide starts after 2 mins, however, for NP-coated electrodes which presented higher mechanical stability, the treatment was continued. EIS measurements after 10 minutes of ultrasonication indicate that there is only a 4 kΩ increase in the impedance despite the substantial delamination of graphene, which confirms the presence of Pt NPs even after longer ultrasonication (as shown in Fig. S3 in the supplementary notes).

4.5. DISCUSSION

The multilayer graphene electrode surface is modified with Pt NPs to enhance its electrochemical characteristics. A spark ablation method is used to print NPs locally on the electrodes. This single-step process can be performed at room temperature in a dry environment. The surface modification practically enables the use of smaller electrodes with higher selectivity for neural recordings and allows the transfer of more charge via the electrode-tissue interface for neural stimulation under electrochemically safe conditions. Furthermore, the NP deposition at room temperature enables a stress-free NP coating deposition, which does not involve thermally introduced strain forces to the electrode [19].

The highest NP surface density used in this work is 40% which still has an optical absorbance below 8%. The optical transmittance of graphene with the same growth condition was previously reported to be above 80% [12]. This confirms the potential use of graphene electrodes coated with NPs for future neuroscientific research such as optogenetics and optical imaging, as adding NPs on the graphene electrode surface is not expected to have a significant impact on the electrode's optical transparency.

The results reported in this work demonstrate an improvement of the electrochemical characteristics of graphene electrodes by adding printed Pt NP coatings. The electrochemical performance is further improved for higher NP surface densities. This improvement is likely a result of the electrode surface area increase due to the presence of NPs and the fact that Pt NPs create a parallel conduction path in the electrode-electrolyte interface, overcoming the quantum capacitance of graphene[20]. CSC values are also known to be influenced by factors such as surface roughness, electrochemical surface area, and charge transfer mechanisms of the coating [37]. Previously reported mono-

layer graphene electrodes with electrodeposited Pt NP coatings with 15% density have a similar area-normalized impedance with the one reported in our work with the same NP density [20]. Concerning CSC and CIC for neural stimulation applications, no comparison can be made with the previous work which focuses only on neural recording measurements. The results from CV and VT measurements demonstrate 15 times higher CSC, and 4 times better CIC after Pt NP printing on the graphene surface. Unfortunately, in the aforementioned work, the stability of the coating on graphene was also not investigated. In this work, three different tests were used to assess the coating stability, electrochemically and mechanically.

Continuous CV tests show that the electrodes with printed Pt NPs are electrochemically stable. Examination of the electrode surface after continuous CV measurements did not reveal any delamination or cracks on the graphene samples with NP coating. To further investigate the electrochemical stability of the electrodes, a larger number of CV cycles could be used.

Continuous VT tests do not suggest substantial delamination of the Pt NP coating from the graphene electrode surface. Similar impedance and CSC changes are observed for the graphene electrode without any coating which could be attributed to graphene delamination from the oxide layer. The reported impedance of the electrode with coating after 500,000 VT cycles is still lower than the impedance of graphene electrodes without any coating. This test should be repeated for the final implantable device as this device will not have a Mo layer underneath graphene which restricted this test due to Mo corrosion. The presence of the Mo layer probably had a negative impact on the results.

Ultrasonic treatment has been applied to the coated electrodes to assess the mechanical stability of the coating. Results from this test do not suggest NP delamination after the treatment, as indicated by optical inspection and impedance measurements. Surprisingly, graphene electrodes coated with NPs remain adherent to the underlying oxide layer, while graphene electrodes alone delaminate from it during the treatment. Ultrasonication has been used in literature to test the mechanical stability and adhesion of other coatings, such as PEDOT:PSS, on various electrode materials[40]. However, the ultrasonic vibration applied by this test to the electrodes is quite intense and harsh, and not representative of what an electrode will encounter in the body environment.

Nevertheless, the electrochemical and mechanical stability of the Pt NP coating of graphene electrodes suggest that printed NPs are quite stable. It is not clear whether the stability of printed NPs is because of the printing method, the multilayer nature of our graphene, or some other factor. It would certainly be interesting to compare the stability of the NP deposited with other deposition techniques and/or single-layer graphene, but unfortunately, these results are lacking in the literature.

The test samples used for the stability assessment of the Pt NP coating on graphene in this work have not been optimised for these tests. In particular, the samples have been fabricated on a Si substrate where graphene sits on a silicon oxide layer, from which it delaminates during the continuous VT and ultrasonic treatments. This fact limited the intensity or duration of the treatment. In a practical application scenario of a neural interface, the oxide layer underneath the graphene electrodes is removed and substituted with parylene, as shown in [12]. Therefore, to ensure a more conclusive result the stability and adhesion tests should be repeated and extended for the final device. The delami-

nation of the NP coating leads to the deterioration of the electrochemical characteristics over time, which consequently results in functionality loss. Moreover, the detached NPs may undergo biodispersion inside the body after implantation and can become toxic to the tissue. Additional treatments, such as prolonged immersion in a PBS solution, or dipping in an agarose gel [39], could be added to the current suite, to further assess the long-term adhesion and stability of the coating for potential chronic applications.

If necessary, roughening the electrode surface prior to NP printing could be investigated in the future as a means to enhance the NP adhesion to the electrode surface. Previously, roughening the electrode surface of metal electrodes prior to PEDOT:PSS coating resulted in an increase in mechanical bonding between the electrode and its coating, thereby resulting in higher stability [40].

The NP deposition technique presented in this paper yields a selective local modification of graphene electrodes. This opens up interesting possibilities when arrays of electrodes of various sizes are required during multimodal interaction with neural tissue. NP coatings come at the expense of less transparency, therefore could only be applied locally, only at e.g., very small electrodes, to enhance their recording performance, while larger electrodes on the same device can remain uncoated. Besides their effect on electrochemical characteristics, Pt NPs can be employed for local biosensing. This localization is not possible with electrodeposition techniques, where all electrodes on a device will be coated simultaneously. Besides, but crucially, the proposed technique is performed at room temperature and via a dry process, as a post-processing step. It is thus compatible with polymer substrates, an integral component of neural implants, as well as with a range of other processes and materials of the final device. These characteristics render this approach a unique tool for the enhancement of the performance of flexible neural implants.

Finally, the Pt NP coating on graphene electrodes used in this paper shows that significant improvement in the electrochemical characteristics of multilayer graphene while maintaining a large degree of transparency is possible per electrode. It demonstrates a reduction in the impedance and a significant increase in CSC and CIC, quantities that are essential for efficient neural tissue interaction. The stability of the Pt NPs on the graphene surface was also assessed, for the first time, in scenarios relevant and tailored to their use during neural interfacing.

4.6. CONCLUSIONS

To conclude, we present multilayer graphene electrode surface modification with Pt NPs using a spark ablation method. This method yields the local printing of NPs on an electrode surface without using a high temperature or wet processing. NP printing can be performed as a post-processing step to enhance the electrochemical characteristics of graphene electrodes further. The electrode showed 4.5 times lower impedance at 1 kHz after 40% NP coating on the surface (from 31.45 to 7.26 kΩ). The charge storage capacity (CSC), calculated based on a cyclic voltammetry (CV) test, was improved up to 15 times with 40% NP coating (from 233 μC/cm^2 to 3614 μC/cm^2). The maximum charge injection capacity (CIC), obtained by voltage transient (VT) measurements, also increased from 8.4 μC/cm^2 for graphene electrodes to 30.6 μC/cm^2 for graphene-coated electrodes with 40% surface density of NPs. NPs printed using this method yield electro-

Table 4.2: Nanoparticle printing setting.

Nominal NP surface density (%)	Calculated surface density (%)	Printing speed (mm/s)	Line width (µm)	Voltage (kV)	Current (mA)	Carrier gas flow (L/min)	Nozzle height (mm)	Nozzle diameter (mm)
15	17.55	137.0	526	1	3	N_2 (1.5)	0.5	0.35
30	30.30	67.0	554					
40	39.90	38.3	637					

chemical stability over 500 cycles of continuous CV measurements and 500,000 cycles of continuous VT tests. In addition, ultrasonic vibration of electrodes with NP coating shows better mechanical stability compared to graphene electrodes without any NPs. These results demonstrate selective NP deposition and local modification of electrochemical properties in graphene electrodes for the first time, enabling the cohabitation of graphene electrodes with different electrochemical and optical characteristics on the same substrate for neural interfacing.

4.7. SUPPLEMENTARY NOTES

4.7.1. FABRICATION PROCESS STEPS

The fabrication process of the multilayer graphene electrode, as shown in Fig.4.2, starts with 300 nm thermal wet oxide growth on the front side of a silicon (Si) wafer at 1000 °C. Next, 50 nm molybdenum (Mo) is sputter-deposited at 50 °C on the oxide layer. The Mo layer is then patterned and etched to serve as the catalyst layer for the following graphene growth. Mo etch is performed using an inductively coupled plasma (ICP) etcher with 50 W RF power, 500 W ICP power, 5 mTorr pressure, 25 °C temperature, and 30 and 5 sccm Cl_2 and O_2 gas flows, respectively. Then, graphene is selectively grown on pre-patterned Mo using a chemical vapor deposition (CVD) process (using an Aixtron Black Magic Pro tool) at temperatures of 935 °C, 25 mbar pressure, and using 960, 40, and 25 sccm of Ar, H_2, and CH_4 gas flows, respectively, and cooled to room temperature under an Ar atmosphere. The growth time is 20 minutes which results in 7 graphene layers as shown in [12].

Then, an aluminum (Al) / titanium (Ti) stack is sputtered and photolithographically patterned to allow for wire bonding on the contact pads. The Al/Ti layer is then etched in a 0.55% concentration of hydrofluoric acid (HF) to remove this layer from the whole wafer except the contact pads. Next, the photoresist (PR) is spin-coated as an insulation layer and patterned on the electrodes and contact pads. Finally, Mo underneath the graphene electrodes is etched using wet etching in hydrogen peroxide (H_2O_2), leaving the graphene in the exact same location as defined by the catalyst. This is shown in the cross-sectional view of the graphene electrode before and after etching Mo in Fig.4.2 (a).

4.7.2. NANOPARTICLE PRINTING SETTING

For ease of comparison, 17.55% NP surface density was considered 15% in the text (as shown in Table.S1/4.2).

4.7.3. CONDUCTIVITY MEASUREMENT

Since the Pt NPs were printed as a line that goes from the insulating layer to the exposed electrode, the printed line may create a conducting path. To better understand this behavior, a four-point probe measurement test was performed. A line pattern was printed over vertical metal tracks (100 nm gold with 10 nm chromium) on the samples. The measurement was performed by passing a current through two outer probes and measuring the voltage between two inner probes as shown in Fig. S1/ 4.7 (a). The test was conducted twice for each printed line (with surface densities of 15, 30, 40, and 50%) at different locations. However, the distance between the inner probes was kept constant at 25 µm. The measurement was conducted from -500 mV to 500 mV with 8 mV steps.

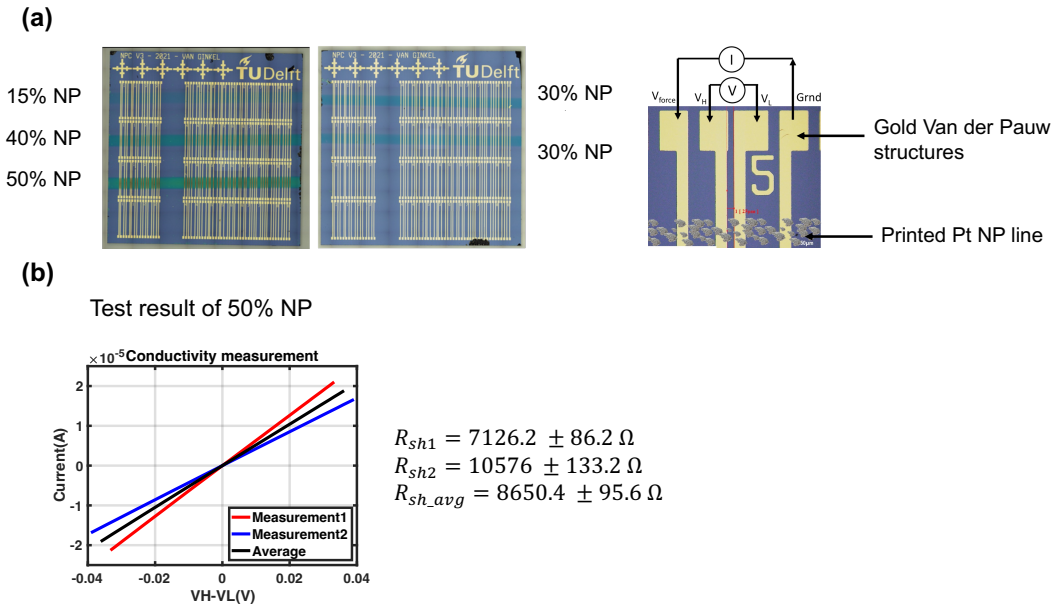

Figure 4.7: Conductivity measurement (a) Samples with Pt NP lines with the corresponding printing speed printed over gold Van der Pauw structures for the four-point probe measurement, (b) Results of the four-point probe measurements of 50% NP surface density printed lines.

Out of the eight measurement attempts (2 tests for each line sample), only 2 samples showed a current above the noise floor of the instrument. Hence, there is a conducting path along those measured areas. Two tests for the print sample of 50% NP show a conductive circuit. Presented in Fig. S1/ 4.7 (b) are the current-voltage curves measured for these closed circuits. The sheet resistance for these printed lines is calculated based on Equation (4.2) and are shown in Fig. S1/ 4.7 (b). R_{sh1} and R_{sh2} represent the sheet resistance of the printed line for the two measurement tests and R_{shavg} is the average of the sheet resistance from these two measurements. Additionally, the 40% NP line did not have any current flowing on both tests, and the height difference between the exposed graphene electrode and the insulating layer (3 µm) on the final electrode samples likely severs any connecting path for print speeds of 40% NP and lower. Although, this is likely

not the case for the 50% NP printed line with stable linear current-voltage characteristic curves. Therefore, the electrodes with 50% NP were removed from further characterization.

$$R_{sh} = \frac{\pi}{Ln2} \cdot \frac{V_H - V_L}{I_{force}} \tag{4.2}$$

4.7.4. RAMAN SPECTROSCOPY, OPTICAL TRANSMITTANCE, AND SURFACE ROUGHNESS MEASUREMENTS

As explained in the manuscript, Raman spectroscopy, surface roughness, and optical transmittance measurements are performed for the electrodes. The details of each measurement can be found below:

Raman spectroscopy is used to investigate the effect of NP printing on the graphene lattice structure. For the Raman characterization, a Renishaw inVia system with a red HeNe laser of 633 nm is used. Raman spectroscopy is performed before and after NP printing on the electrode surface.

The NP surface density can only indicate the 2D distribution of the NPs. To indicate a 3D NP distribution over the electrode surface, surface roughness measurements are performed. A high surface roughness has been shown to increase the CSC due to an increase in the electrochemical surface area of the electrode [38]. The surface topography of the Pt NPs printed with multiple surface densities is investigated through atomic force microscopy (AFM; Ntegra). Samples are prepared by printing Pt NP lines on a silicon die. The topography of these samples is tested at a frequency of 0.50 Hz in semi-contact mode with a scan size of 10 µm by 10 µm. This measurement is performed 5 times for each sample at different locations throughout the printed NP lines but as far as possible from the line edges. The AFM data is further processed using Gwyddion applying polynomial correction of the background [41].

The optical transparency of different NP surface densities is assessed for wavelengths in the range of 300 nm to 900 nm (using a Perkin Elmer Lambda 950 UV/Vis spectrophotometer, Waltham, Massachusetts). NPs are printed directly on glass slides (1 sample per surface density). To create a sufficiently large area covered with NPs for this measurement, the printer's nozzle follows a laddered path, i.e., a line is printed along the x-direction followed by a step in the y-direction. Since the line width for each NP density is determined through the method discussed previously, a logical step at the y-direction is considered for each NP density to minimize the chance of overlapping with the previous line.

4.7.5. ATOMIC FORCE MICROSCOPY (AFM)

RMS and mean surface roughness of the Pt NPs with various surface densities printed on si wafer is shown in Table S2/4.3.

4.7.6. CONTINUOUS CV TEST

The impedance and CSC before and after continuous CV tests for three electrodes per group of graphene electrodes without and with various Pt NP surface densities are shown in Table S3/4.4.

Table 4.3: Table S2. RMS and mean surface roughness.

Nominal NP surface density (%)	RMS surface roughness (nm)	Mean surface roughness (nm)
15	9.00 ± 0.87	7.11 ± 0.72
30	9.41 ± 1.37	6.96 ± 0.20
40	14.66 ± 7.31	12.03 ± 6.36

Table 4.4: Table S3. The results of continuous CV test for three electrodes per each group.

Electrodes	Z at 1 kHz (kΩ) Before	Z at 1 kHz (kΩ) After	Z change (%)	CSC (μC/cm²)					
				Total			Cathodic		
				Before	After	Change (%)	Before	After	Change (%)
Graphene	26.98	25.66	-4.9	148	164	10.8	97	117	20.6
	34.60	33.61	-2.8	99	101	2.0	48	56	16.7
	36.64	36.17	-1.3	198	201	1.5	76	106	39.5
Graphene + 15% Pt NPs	17.19	19.83	15.4	738	675	-8.5	596	548	-8.0
	17.23	21.22	23.1	656	694	5.8	589	635	7.8
	18.03	17.99	-0.3	767	834	8.7	646	703	8.8
Graphene + 30% Pt NPs	12.69	16.23	27.9	928	924	-0.4	731	757	3.5
	10.90	13.33	22.3	797	789	-1.0	678	659	-2.8
	11.27	12.15	7.8	813	829	2.0	669	658	-1.6
Graphene + 40% Pt NPs	7.87	8.62	9.5	879	1004	14.2	727	780	7.3
	7.62	8.53	12.0	952	1112	16.8	755	812	7.5
	9.22	8.80	-4.6	917	1097	19.6	709	827	16.6

4.7.7. EDX RESULT

Optical microscopy and SEM images of the electrode after the continuous CV are shown in Fig.S2/4.8 (a). The zoomed-in optical image shows the dendritic pattern created by Na and Cl residues on the electrode surface. EDX map spectrum and table of the present elements are also shown in Fig.S2/4.8 (b).

4.7.8. ULTRASONIC TEST

The graphene electrodes without NPs showed partial to complete delamination of the layer after only 2 minutes of the ultrasonic test as shown in Fig. S3/4.9 (a). This is due to the poor adhesion of graphene to the underlying oxide. Samples with NP coatings were able to sustain ultrasonication longer than samples without NPs.

After 5 minutes of ultrasonication, there was visible delamination of the graphene layer on samples with NPs. However, the impedance (at 1 kHz) of the electrode (as shown in Fig. S3/4.9 (b)) is 13 kΩ which is still much lower than the average impedance of the graphene (34 kΩ), thus implying that there are still Pt NPs on the electrode surface. However, the Pt NP surface density after this duration is unknown. The impedance value is still low (26.25 kΩ) after the 7 minutes of ultrasonication and increases (38.7 kΩ) after 10 minutes. Despite the substantial delamination of the graphene layer, the impedance only increased by about 4 kΩ. This suggests that there may still be some Pt NPs on what is left of the graphene layer. There was also a color change on the graphene after 12 minutes, possibly caused by substantial delamination of the Pt NPs.

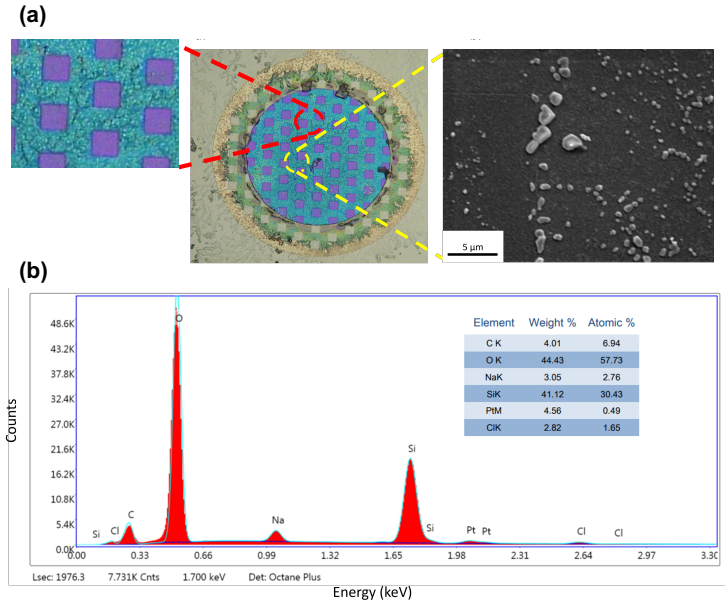

Figure 4.8: Fig. S2. EDX result (a) Microscopy and SEM image of the electrode after the continuous CV (The zoomed-in optical image shows the dendritic pattern created by Na and Cl residues on the electrode surface), (b) EDX map spectrum and table of the present elements.

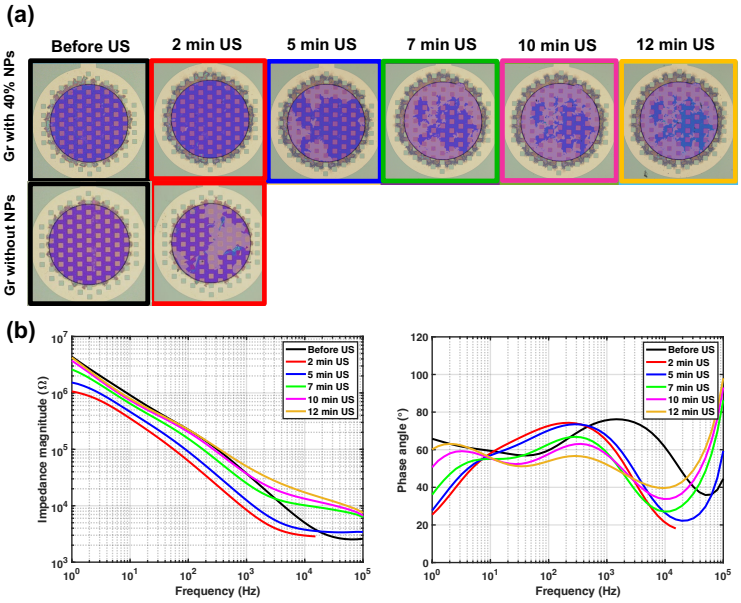

Figure 4.9: Fig. S3. Ultrasonic test (a) optical image of graphene electrodes with and without NPs before and after 12 minutes of ultrasonication, (b) Impedance magnitude and phase plot of graphene electrodes with 40% NPs before and after 12 minutes of ultrasonication.

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5

PDMS-Parylene C ENCAPSULATION

Parts of this chapter have been published in 42nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC) **324**, 289 (2020) [1] and 23rd European Microelectronics and Packaging Conference (EMPC) **324**, 289 (2021) [2].

This chapter discusses soft encapsulation for active neural implants, presents the proposed encapsulation stack based on using thin-film ceramic interlayers (SiC and SiO_2) between polydimethylsiloxane (PDMS) and parylene C and the results regarding the adhesion strength and moisture barrier property.

5.1. PDMS-PARYLENE C ENCAPSULATION

Abstract: Parylene C has been used as a substrate and encapsulation material for many implantable medical devices. However, to ensure the flexibility required in some applications, minimize tissue reaction, and protect parylene from degradation in vivo, an additional outmost layer of polydimethylsiloxane (PDMS) is desired. In such a scenario, the adhesion of PDMS to parylene is of critical importance to prevent early failure caused by delamination in the harsh environment of the human body. Towards this goal, a method based on using intermediate ceramic layers as adhesion promoters between PDMS and parylene are proposed.

To evaluate this concept, three different sets of samples with PDMS on parylene without and with oxygen plasma treatment (the most commonly employed method to increase adhesion), and samples with our proposed ceramic intermediate layers of silicon carbide (SiC) and silicon dioxide (SiO_2) are prepared. To investigate the adhesion property, cross-cut tape tests, and peel tests are performed. The results show a significant improvement in the adhesion in the proposed encapsulation stack compared with PDMS on parylene and PDMS on plasma-treated parylene. In addition, the X-ray photoelectron spectroscopy (XPS) analysis at the interface between SiC and parylene C shows different peaks for the interface compared to the reference spectra, which could be an indication of a chemical bond.

The long-term adhesion strength of the proposed encapsulation stack is also investigated. Samples with thin ceramic interlayers are soaked in a phosphate-buffered saline (PBS) solution at 67 °C to accelerate the aging process. Two samples are also implanted, subcutaneously, on the left and right subscapular regions of a rat. The optical inspection and peel tests performed after two months of aging confirm the preliminary findings and show a significant improvement of the adhesion in the proposed encapsulation stack compared to the case of PDMS on parylene C with or without pre-treatment.

Finally, water vapor transmission rate (WVTR) tests are performed to investigate the barrier property of the proposed encapsulation stack against water vapor transmission. The results demonstrate that the proposed stack acts as a significantly (two orders of magnitude) higher barrier against moisture compared to only parylene C and PDMS encapsulation layers.

The proposed method yields a fully transparent encapsulation stack over a broad wavelength spectrum that can be used for the conformal encapsulation of flexible devices, thus, making them compatible with techniques such as optical imaging and optogenetics.

5.2. MATERIAL SELECTION

Various organic and inorganic materials have been proposed as alternative encapsulation methods for miniaturized microfabricated neural implants as they exhibit mechan-

ical flexibility, compatibility with the microelectromechanical system (MEMS) process, good electrical insulation, conformal encapsulation of complex topography, and biocompatibility. The purpose and application of an implant dictate the material selection for its encapsulation. As an example, considering the optogenetics and optical imaging applications for the proposed graphene-based platform in this work, the encapsulation layer has to be chosen among all soft and flexible materials which exhibit optical transparency across the 450 nm to 850 nm wavelength range. Polyimide, a material commonly used in flexible electrode arrays [3, 4], is not preferred for such applications due to its absorption peak around 450 nm, overlapping with the wavelength of interest and considerably blocking blue light as shown in [5]. Parylene (poly-para-xylylene (PPX)) C and PDMS (Polydimethylsiloxane) have shown high optical transparency and could be selected for the encapsulation stack.

5.3. PARYLENE C

Parylene C has the advantage of low-stress and pinhole-free layers, flexibility, easy deposition and etching processes, and high biocompatibility, categorized in the USP class VI group which is the highest biocompatibility rating for plastics [6]. Moreover, its high optical transparency and good ionic barrier property (one of the lowest water vapor transmission rates among polymeric materials [7]) make it a very promising material both for the substrate as well as the encapsulation layer of the implant.

Due to the molecular level deposition process used for parylene C (chemical vapor deposition (CVD) processes at room temperature), a uniform and conformal film can be formed over complex surface topographies such as sharp edges [8, 9]. Moreover, it is considered to be a suitable candidate for insulating high-density conductive tracks in many implantable medical devices [10, 11, 9]. However, its high Young's modulus (~2.7 GPa) makes it still relatively stiff compared to the tissue (Fig. 5.1) [12]. This stiffness might be tolerated in some applications and even be beneficial, such as protecting thin-film metal tracks from the longitudinal stress and strain applied during implantation. However, it might be completely unsuitable in others, where softer elastomers such as PDMS are necessary to avoid tissue damage [13].

Recent research showed damage in parylene C itself, due to *in vivo* exposure [14, 15]. Also, degradation of the parylene encapsulation layer itself caused by oxidation and chlorine abstraction of the parylene C surface was reported after 3.25 years of implantation [16]. As a consequence, an additional outmost encapsulation layer with similar mechanical properties to the tissue is desired.

5.4. PDMS

PDMS is the most commonly used silicone elastomer, with a Si–O backbone, in micro- and nano-scale soft lithography in biomedical applications. This is due to its advantageous properties such as high elasticity, optical transparency, adjustable surface composition, and biocompatibility. However, it does not provide the required mechanical stability for the thin film metal tracks.

Furthermore, high permeability to water vapor may limit its application for encapsulation purposes if there is a loss of adhesion to its substrate and the substrate is not a

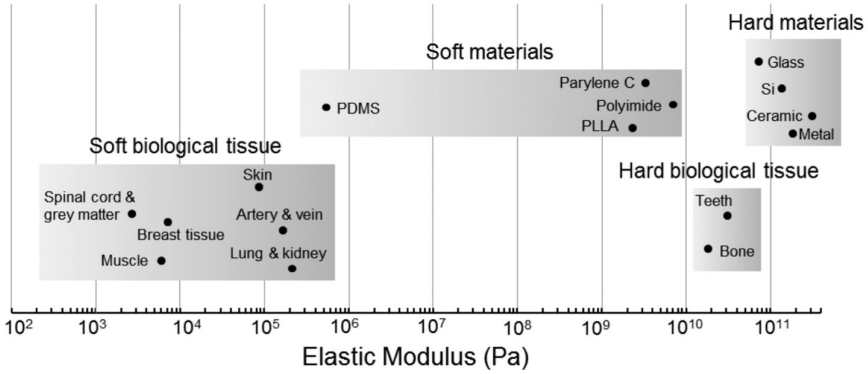

Figure 5.1: Logarithmic plot of Young's modulus for various biological tissues and common materials used for neural interfaces ([12])

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good water vapor barrier.

However, this high water permeability can be further improved by combining PDMS with other materials such as glass [17] and parylene C [18, 19]. Therefore, despite the inadequate barrier properties of PDMS, given its mechanical properties, it could be useful as a secondary coating material . Due to its low Young's modulus as shown in Fig. 5.1 [12] its mechanical properties are more similar to those of soft biological tissue, creating a better interface between the implant and the human body.

5.5. PDMS-PARYLENE C ADHESION

The combination of parylene C and PDMS is advantageous to achieve the required flexibility, reduce tissue damage, protect thin-film tracks against breakage, and prevent degradation of the parylene C *in vivo*.

However, to ensure long-term stability of the implant during chronic *in vivo* experiments, a strong adhesion of PDMS to parylene C is of paramount importance. Implantable devices operate in harsh environments, and their reliability should, therefore, be considered and evaluated in non-standard dedicated representative tests. The long-term stability of the conformal coating is mainly affected by (a) the adhesion between all interfaces, as well as by (b) the water vapor and ionic barrier properties that the respective coatings can offer. Therefore, in this chapter, a thorough evaluation of the aforementioned properties will be presented under conditions that better match the environment that the implant will encounter when inside the body [20].

Due to the different polymeric backbones of parylene C and PDMS, as shown in Fig. 5.2, and their hydrophobicity [21], adhesion between them is often based on physical bonds, which are relatively weak, rendering the layers prone to delamination, especially when water is present at the interface [22].

To create a stronger bond between the two materials, one approach could be plasma surface treatment. It has been reported that oxygen plasma treatment of polymer surfaces is an excellent method to increase their wettability and their surface energy enabling a strong bonding of two polymers [23]. In [24], the authors achieved a selec-

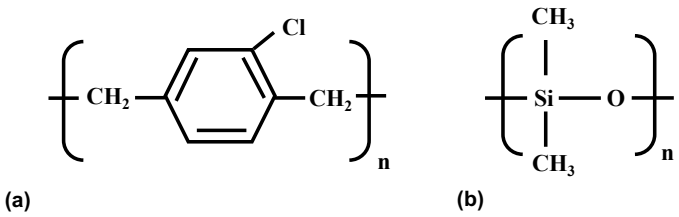


Figure 5.2: (a) Parylene C, and (b) PDMS chemical formulas ([21])

tive bond between PDMS and parylene C after nitrogen and oxygen plasma treatments. Techniques such as X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy energy-dispersive X-ray spectroscopy (TEM-EDS) were used for the interface analysis and a covalent bond was reported. However, the measured force during T-peel test for all the test variations did not exceed 0.3 N. This is in contrast with the fact that according to the ASTM D3359 tape test, an adhesion force above 7 N is classified as 5B and indicates strong adhesion. It was also claimed that these 3D soft and flexible structures could be used in implantable biomedical applications, however, no long-term investigation was reported on the adhesion strength.

A number of different plasma treatments (Nitrogen (N_2), SF_6, and O_2) has been also proposed to enhance the bonding of PDMS-parylene for microfluidic applications [21]. The authors showed that samples created by this method were able to withstand high burst pressures, however, no long-term adhesion evaluation was performed.

Another method to improve the adhesion between layers is to add a thin-film interlayer as an interface. The advantage of using this method is the improvement in water-vapor barrier property in addition to adhesion. Related to this approach, thin ceramic intermediate layers were employed to make a chemical bond between PDMS and polyimide [22]. A thin layer of SiC and SiO_2 was deposited in a vacuum chamber on polyimide using the plasma-enhanced chemical vapor deposition (PECVD) technique. The low-pressure deposition process allowed the creation of a covalent bond between sp2-bonding carbon in polyimide towards the sp3-bonding in SiC, continuing to SiO_2 providing a strong adhesion with PDMS. The samples were subjected to accelerated aging at 125°C and 130 kPa in a PBS solution for 96 hours. The reference samples without ceramic layers failed after 30 minutes while no failure was detected on the samples with ceramic layers over 96 hours.

5.6. THE PROPOSED SOLUTION

Inspired by the above approach based on using thin ceramic layers as interlayers between PDMS and polyimide, we propose the use of intermediate thin films, namely SiC and SiO_2, to create strong bonds between parylene C and PDMS, as illustrated in Fig. 5.3. These thin film ceramic layers (SiC and SiO_2) are tight at the molecular level. Therefore, apart from adhesion improvement, they might lead to total water permeation reduction through the encapsulation stack.

To achieve an encapsulation stack with a long lifetime, a strong adhesion between all the interfaces is required. PDMS is known to have a strong adhesion to SiO_2 due to

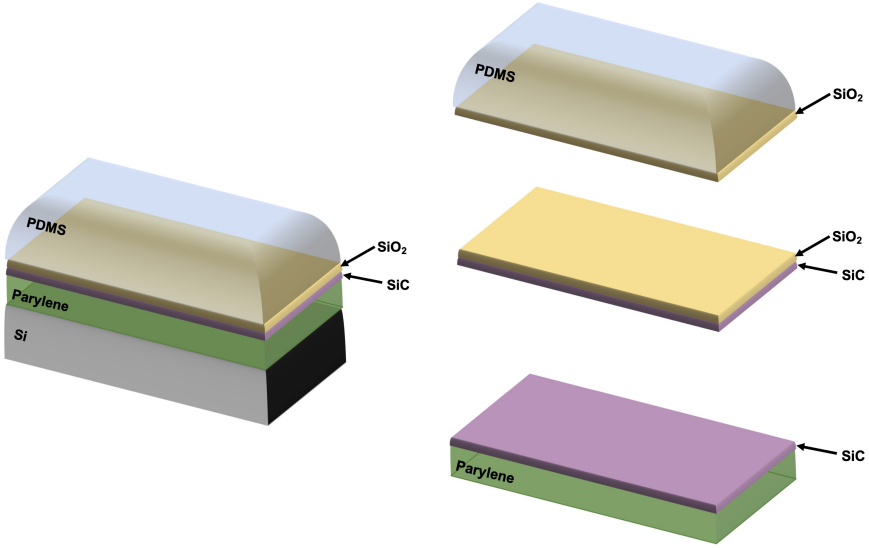


Figure 5.3: The proposed encapsulation stack including PDMS on parylene and the thin ceramic interlayers with all the existing interfaces

the presence of hydroxyl groups at the interface between the two materials. Due to its wide use in MEMS, Si bond formation between SiO_2 and SiC has also been studied well [22]. It is assumed that a C-C chemical bond can be created between SiC and parylene. Therefore, the interface created between SiC and parylene C needs further investigation.

Adhesion tests such as the cross-cut tape test, the 180 °-peel test, and the T-peel test have been employed to characterize the adhesion strength, between the layers in the proposed encapsulation stack. To characterize the adhesion strength relevant test structures including only PDMS on parylene, PDMS on oxygen plasma-treated parylene, and PDMS-parylene with the thin film interlayers (SiC and SiO_2) were created. Their preparation is explained in the following section.

5.6.1. SAMPLE FABRICATION

SI-BASED SAMPLES

To evaluate the proposed concept, relevant test structures were fabricated, as illustrated in Fig. 5.4.

A 400nm SiO_2 layer was deposited at 400 °C on a single-sided polished (SSP) Si wafer as an isolation layer by using a plasma-enhanced chemical vapor deposition (PECVD) technique. A 5-µm parylene layer was deposited using a chemical vapor deposition (CVD) technique at room temperature (using an SCS PDS 2010 parylene coater), followed by applying an A-174 adhesion promoter. A monolayer of this adhesion promoter should be applied inside the chamber before parylene deposition. To create samples with and without oxygen plasma treatment as shown in Fig. 5.4 (a), PDMS (Dow Corning Sylgard 184) was mixed with a curing agent at a 10:1 ratio, spin-coated at 1250 rpm di-

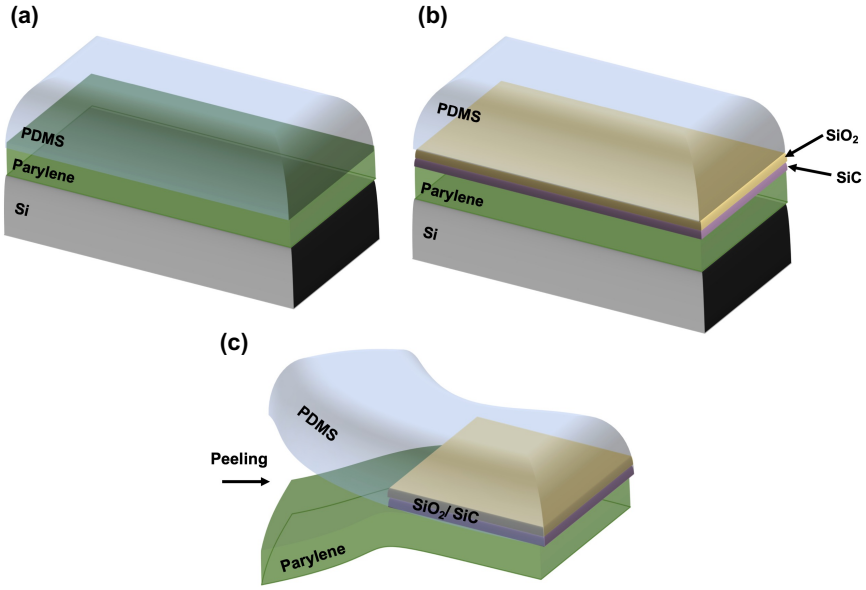


Figure 5.4: Prepared samples for adhesion tests, (a) Samples with and without oxygen plasma treatment, (b) Full encapsulation stack with thin ceramic interlayers, and (c) Free standing membrane prepared for the adhesion test

rectly on parylene, and cured at 75 °C for 3 hours. This resulted in a 50-µm thick layer. The curing temperature was kept low to ensure the temperature does not exceed the glass transition temperature of parylene (90 °C) and cause its oxidation [25]. For the samples with oxygen plasma treatment, an oxygen plasma treatment (50 sccm of oxygen flow, 60 W, 0.25 mTorr, Diener electronic GmbH Germany) was applied on the parylene surface for 1 min before PDMS coating to increase the surface activation energy in order to improve the adhesion.

The proposed SiC-SiO_2 stack of Fig. 5.4 (b) was created as follows: 25 nm SiC is PECVD deposited (Elettrorava Amor) on parylene at 180 °C temperature using three different recipes (R1, R2, and R3), which will be discussed more in the following section. Then 25 nm SiO_2 is deposited in the same chamber and at the same temperature using deposition parameters of 1 sccm SiH_4, 20 sccm CO_2, 1.4 mbar pressure, and 20 W power. The SiC-SiO_2 stack deposition temperature was kept low to ensure it is below the parylene melting temperature (290 °C) [25]. The deposition temperature is already above the parylene glass transition temperature because the deposition is performed under a vacuum preventing the effects of oxidation (browning, wrinkling, and becoming brittle)[25]. Finally, the PDMS layer is spin-coated on top.

FREE-STANDING MEMBRANE

Free-standing test structures were developed for the needs of the peel test described in Section 5.6.4. For these, the Si/SiO_2 substrates were removed to create free-standing parylene-PDMS stacks with all the flavors of Fig. 5.4 (a, b). To ease the release of the fi-

Table 5.1: Recipes used for SiC deposition

Recipe		Deposition parameter				
		SiH_4 (sccm)	CH_4 (sccm)	H_2 (sccm)	Power (W)	Pressure (mbar)
Non-silane starving mode	R_1	20	45	0	4	0.7
	R_2	1.6	3.7	200	6	2.6
Silane starving mode	R_3	2	10	90	30	2

nal structures from the Si wafers, a de-adhesive material from Sigma-Aldrich (Trichloro (1H,1H,2H,2H-perfluorooctyl) silane was first coated on a clean silicon wafer in a vacuum environment created inside a desiccator. To evaluate the influence of the ceramic layers on the adhesion between PDMS and parylene C, the proposed layers were deposited only on half of the wafer (using metal masks to cover the other half during deposition) to be able to initiate the peeling as shown in Fig. 5.4 (c). It should be noted that no plasma treatment was performed before PDMS spin coating on the sample.

5.6.2. COMPARISON OF THE THREE SiC RECIPES

In addition to adhesion improvement, ceramic layers also act as a barrier layer against moisture. A pinhole-free layer is expected to be an excellent moisture barrier. However, depositing the SiC and SiO_2 layer at low temperatures (due to the presence of parylene) might not result in a layer with high Si-C and Si-O bond densities, respectively. Therefore, SiC and SiO_2 deposition recipes at the desired temperatures are needed. Multiple deposition recipes were created for only SiC as the interface between SiC and parylene is the interface under investigation in this work. Moreover, the recipe mentioned in the previous section for SiO_2 deposition was previously developed at EKL (Else Kooi Lab).

Recent research on SiC deposition at low temperatures showed that using a high concentration of hydrogen (H_2) as a dilution gas can compensate for the low deposition temperature and result in a high Si-C bond density. In addition, a lower silane (SiH_4) flow can also result in a higher Si-C bond density [26]. Therefore, based on this work, two gas flow modes were used for SiC deposition: silane starving mode (R_3) and a non-silane starving mode (R_1 and R_2) [26]. The silane starving and non-silane starving modes refer to the specific precursor ratio shown in Equation (5.1).

$$\frac{SiH_4}{(SiH_4 + CH_4)} = \begin{cases} 0.17 & \text{Silane starving mode} \\ 0.3 & \text{Non-silane starving mode} \end{cases} \tag{5.1}$$

All these recipes are shown in Table. 5.1. As shown, the H_2 flow is also different in each recipe. Stress measurement and Fourier transform infrared spectroscopy (FTIR) was performed for each recipe with respect to a bare Si wafer. For the R_1, R_2, and R_3 recipes, this resulted in 205, 585, and 530 MPa compressive stress, respectively.

The FTIR diagram is shown in Fig. 5.5 for all three recipes (all waveforms are normalized to the maximum peak). As shown in this figure, the following peaks are expected:

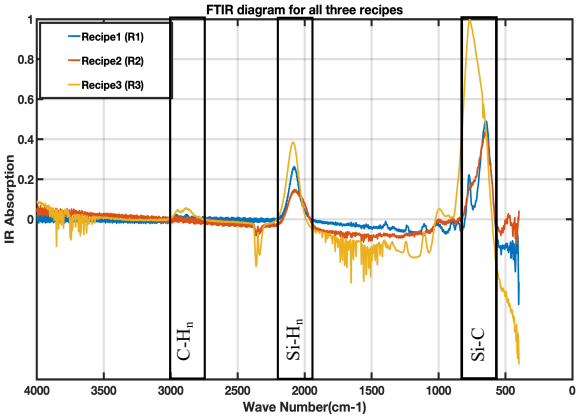


Figure 5.5: FTIR spectra for three different SiC deposition recipes.

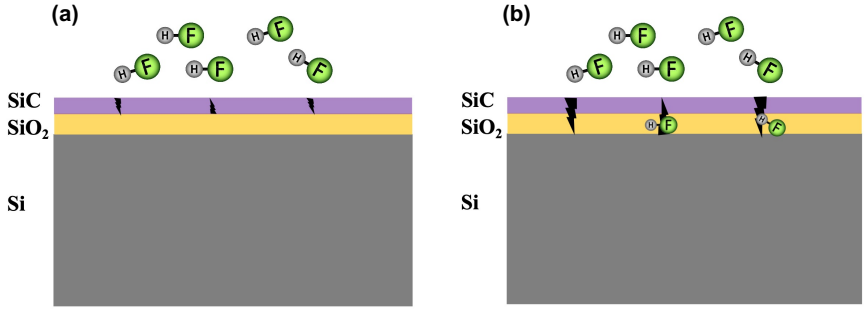


Figure 5.6: (a) Soaked samples in BHF, (b) BHF diffiuses through pinholes and etches SiO_2

(1) a peak at a wavenumber between 720 and 780 cm^{-1}, corresponding to Si-C stretching bonds, (2) a peak at a wavenumber around 2000 cm^{-1} related to Si-H_n bonds, and (3) a peak at the wavenumbers between 2800 and 3000 cm^{-1} for C-H_n bonds [26]. To gain insight into the Si-C bond density of each recipe, a comparison was performed between the Si-C peaks. From these results we observe that R_3 has the highest Si-C peak. However, it also has the highest peaks for Si-H_n and C-H_n.

To compare the different SiC recipes in terms of the number of pinholes, new samples were made. For these samples, silicon wafers with 400 nm PECVD SiO_2 were protected with SiC layer. Three different recipes of SiC were used for the top layer deposition. Then, the samples were placed inside Buffered HydroFluoric acid (BHF) 1:7 for 10 minutes. BHF can penetrate through the pinholes in SiC to reach SiO_2 and etch it (as shown in Fig. 5.6), which can be detected optically.

It was found that there are more pinholes in R_1 (without hydrogen dilution gas) compared to R_2 and R_3. Recipe R_1 also showed the lowest Si-C bond density in the FTIR. This can be explained by the fact that H_2 was not used in this recipe, resulting in a layer with a lower Si-C bond density and a higher number of pinholes which also causes less stress.

The presence of the pinholes depends on the chemistry used for deposition and also the cleanliness of the surface. The characterizations for three different SiC layers show fewer pinholes in the recipes with higher amounts of hydrogen dilution gas (R_2 and R_3).

It has been suggested that C-H_n groups terminate the Si-C network structure and form micro-voids [26]. The higher infrared absorption that occurs for wavenumbers between 2800 and 3000 cm^{-1} in FTIR indicates a higher presence of C-H_n groups, and thus a more porous film. Therefore, R_3 exhibits a higher C-H_n peak resulting in a porous layer. Based on a comparison between the three different recipes, R_2 was selected to be used for SiC deposition for the final encapsulation stack as it has the lowest amount of voids and offers a reasonable trade-off between the number of pinholes and the measured stress.

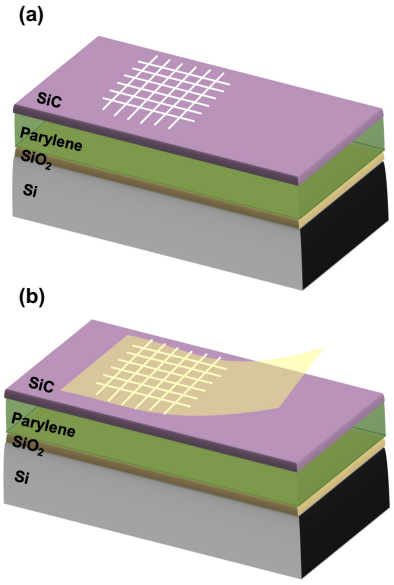
5.7. ADHESION STRENGTH

5.7.1. TAPE TEST

As explained previously, strong adhesion between each layer in the full encapsulation stack is required to ensure the long-term performance of the final device. Among all the interfaces, the SiC-parylene interface is the most critical one. To investigate this interface, a tape test was performed based on the ASTM D3359 standard test method. To do this test, several samples with SiC only (deposited using the three recipes of Table. 5.1) on parylene were created. Next, certified pressure-sensitive tapes, with an adhesive force of 4.3 N/cm and 7.6 N/cm, were applied on the grid pattern created previously on the film by scribing the coating to the substrate with a sharp blade is shown in Fig. 5.7 (a) and peeled from the sample at a 180 degree (Fig. 5.7 (b)). The grid pattern was optically evaluated before and after the test. The adhesion is graded according to the ASTM classification based on the number of entirely or partially peeled-off squares of the layer as shown in Fig. 5.7 (c).

The result of the tape tests for all three recipes are shown in Fig. 5.8 (a). Optical images of the sample before and after the tape test are shown in Fig. 5.8 (b, c). Some parts of the layer peeled off from the substrate after the tape test. However, detailed inspection revealed that the delamination happened between parylene and its SiO_2 substrate (Fig. 5.8 (c)), leaving the parylene-SiC layers still firmly attached to each other. Some residues of parylene C are left on the substrate shown in Fig. 5.8 (c). This result shows that the adhesion of SiC to parylene is stronger than the adhesion of parylene to SiO_2 (which was confirmed by a separate test) as the SiC layer was firmly attached to parylene.

Large stress can cause local delamination from the substrate if the level of adhesion is not strong enough. To investigate this, especially in a humid environment that mimics the human body, samples with different recipes for the SiC layer were deposited on parylene C and placed in soak (PBS solution) and investigated after 12 and 60 days using a tape test. No differences were observed between the three recipes. The result showed that the adhesion was so strong that there was no delamination even for those recipes with a high amount of compressive stress (R_2 and R_3).



(c)

Classification of adhesion test results		
Classification	Percent area removed	Surface of cross cut area from which flaking has occurred for six parallel cuts and adhesion range by percent
5B	0% None	
4B	Less than 5 %	
3B	5 - 15%	
2B	15 - 35%	
1B	35 – 65%	
0B	Greater than 65%	

Figure 5.7: (a) Grid pattern created on the sample prior to tape test; (b) Tape test on the sample; (c) Classification of adhesion test results

(a)

Adhesion force (N/cm) / Deposition recipes	Tape1 (4.3)	Tape2 (7.6)
Recipe1	2B → 0B	2B → 0B
Recipe2	5B → 2B	5B → 1B
Recipe3	5B → 2B	5B → 1B

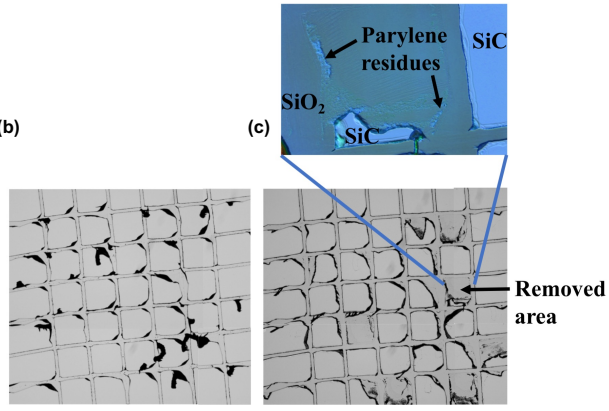


Figure 5.8: (a) Crosscut tape test result for three recipes with two different tapes, (b) Optical image of the sample before performing the tape test, and (c) after performing the tape test with the specified removed area

5.7.2. XPS

XPS was used to further study the SiC-parylene C interface. Two samples comprising 10 µm parylene C on a Si wafer and 0.5 µm SiC on a Si wafer were considered as reference samples. A model sample (test sample) customized for XPS analysis was prepared by depositing less than 25 nm of SiC on parylene C. The XPS analysis was carried out in vacuum (10^{-9} mbar) using a PHI-TFA XPS spectrometer (Physical Electronic Inc.), equipped with an Al-monochromatic X-ray source. The analysed area was 0.7 mm in diameter and the analysis depth was approximately 10 nm. The survey spectra were collected from 0 to 1000 eV. Next, high-resolution multiplex scans of the measured peaks were recorded using a pass energy of 23.5 eV with a step size of 0.1 eV at a take-off angle of 45 ° with respect to the sample surface. The collected spectra were analysed using Multipak v8.0 (Physical Electronics Inc.).

To reach the interface and remove any potential carbon contaminants, the surface was rastered using a 2 keV Ar ion beam over an area of 4 × 4 mm^2. The emission current was 20 mA, and the Ar pressure was 10 mPa. Subsequent XPS measurements were conducted after 1, 4, 8 and 15 minutes of sputtering. SiC and parylene C can be recognised and distinguished by detecting the Si and chlorine (Cl) peaks, respectively.

The survey spectrum of the test sample, shown in Fig. 5.9 (a), indicates the presence of O, C, Cl, and Si elements in 53.1%, 34.4%, 1.1%, and 11.4% atomic concentrations. The high-resolution XPS spectra for the SiC and parylene C reference samples, shown in Fig. 5.9 (b, c), indicate a Si $2p_{3/2}$ peak at 99.4 eV and a Cl $2p_{3/2}$ peak at 202 eV (dashed line). Moreover, a C1s peak at 285 eV and an O1s peak at ~ 533 eV for both samples were observed. The high-resolution spectra for the test sample are shown for Si$2p_{3/2}$, Si2s, C1s, O1s, and Cl2p in Fig. 5.9 (d, e, f, g, h). The presence of the Cl peak is strongly related to the presence of parylene C as shown in its chemical formula (Fig. 5.2).

After sputtering for 1, 4 and 8 minutes, an increase in this peak was observed. A strong Cl peak appeared after 15 minutes of sputtering, which originates from parylene C. High-resolution spectra for O1s and Cl2p for both the reference and test samples showed the same results. In the C1s spectrum, both the reference and test samples contained a peak at 285 eV arisen from the C-C bond, as shown in Fig. 5.9 (f). At the interface, a new peak at 286.5 eV appeared, indicating either a C-O or a C-Cl bond formation. However, after longer sputtering times, this peak was not visible anymore. The high-resolution spectra of Si $2p_{3/2}$ shown in Fig. 5.9 (d) also indicate the presence of another peak close to the Si-O peak, which could be a characteristic of a Si-based bond at the interface [27]. This peak, however, is still present after sputtering, indicating that it is not related to contamination. Compared to the reference, the different peaks observed on the test sample could be an indication that different chemical bonds are being formed between the two materials under investigation. However, more characterization such as analysis of the sample cross-section by transmission electron microscopy (TEM) with energy dispersive X-ray spectroscopy (EDS) is necessary to be able to define the nature as well as the properties of such chemical bonds. This method could provide the possibility of investigating the distribution of atoms at the interface.

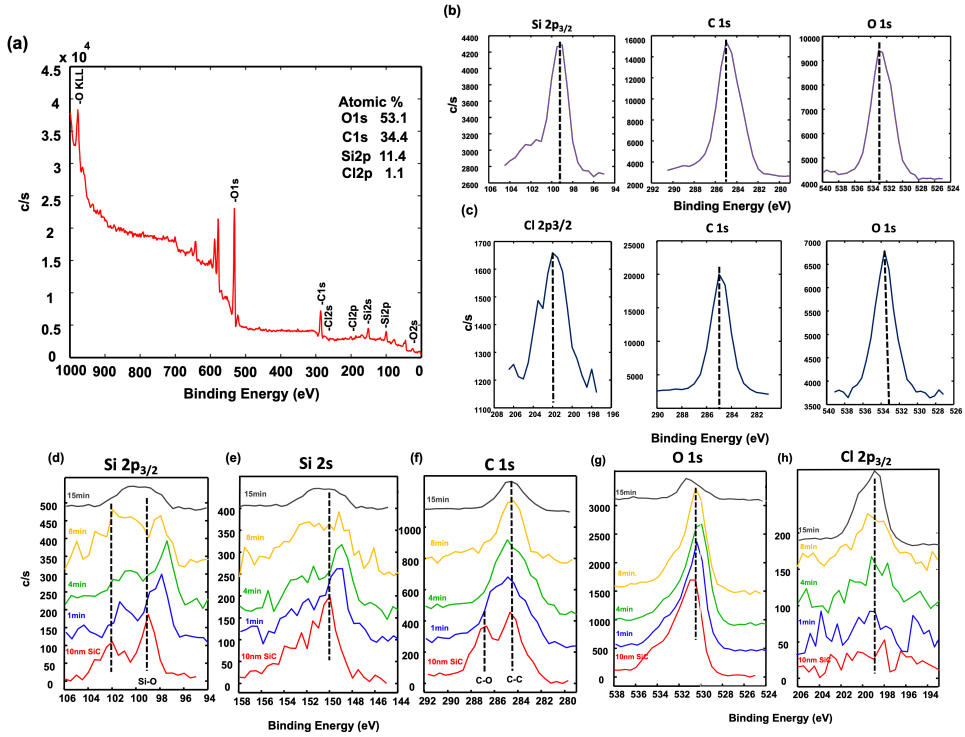


Figure 5.9: XPS results (a) Survey spectra of the test sample, (b) Si2p, C1s, and O1s peaks for the SiC reference sample, (c) Cl2p, C1s, and O1s peaks for the parylene C sample, (d) Si2p, (e) Si2s, (f) C1s, (g) O1s, and (h) Cl2p high-resolution spectra for the test sample.

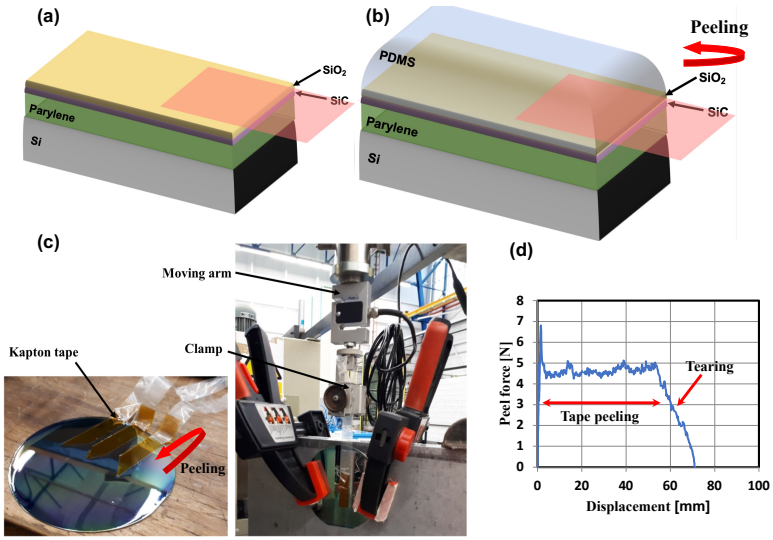


Figure 5.10: (a) Kapton tape applied on the thin-film ceramic layers, (b) PDMS spin coated on the sample and the kapton tape, (c) before and after installation in the peel test machine, (d) tearing failure curve for the encapsulation stack with ceramic layers.

5.7.3. 180 °-PEEL TEST

To be able to assess the strength of the adhesion between the layers used in the proposed encapsulation method, several adhesion tests have been used such as the 180 °-peel test and the T-peel test. To do the 180 °-peel test, one of the layers is clamped and remains fixed in position while the other layer (which is attached onto a moving arm of the testing tool, here a Zwick 1455 tensile testing machine, Fig. 5.10 (b)) is pulled on at a constant speed and at an 180-degree angle.

For this test, samples with the same encapsulation stacks as in Section 5.5.1 were prepared. A Kapton tape was applied on the sample before PDMS coating to create a clamping point for the tool and initiate the peeling (see Fig. 5.10 (a)). The peel test was performed by pulling on the PDMS layer at 500 µm/s and a load of 10 N via the attached Kapton tape. The samples that had PDMS on parylene with and without oxygen plasma were easily peeled.

On the other hand, no peeling was observed on samples that included the whole stack. The adhesion was so strong that the peel test caused the Si wafer to break and the PDMS layer to tear apart before peeling started. The result shown in Fig. 5.10 (d) shows that the peeling was possible on the area covered with the tape and an average peeling force of 4.5 N was measured for the tape peeling but peeling the layer further was not possible. Efforts to strengthen the PDMS layer by making it thicker (80 µm) lead to the same result. Literature shows that no peel during the peeling process is categorized as a common failure mechanism (tearing failure) in a peel test [28]. Tearing failure occurs due to a high adhesion strength (close to the breaking strength of the film) between the film and the substrate which results in a torn film.

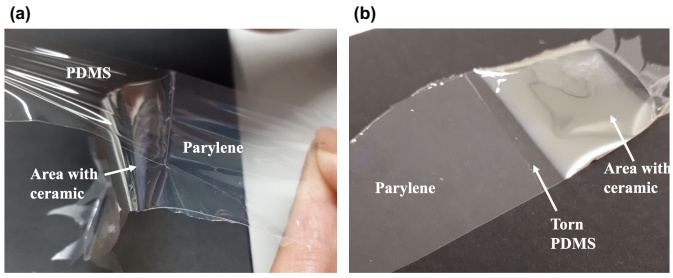


Figure 5.11: Flexible sample including parylene, ceramic layers (on only half of the sample) and PDMS (a) during peeling, (b) torn PDMS after peeling

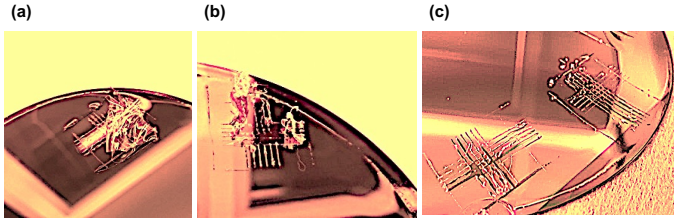


Figure 5.12: (a) PDMS-parylene sample shows delamination before soak test, (b) PDMS-plasma-treated-parylene sample shows delamination before soak test, (c) PDMS-parylene with ceramic layers before soak test

5.7.4. T-PEEL TEST

The test structures shown in Fig. 5.10 allow only for the evaluation of the adhesion of PDMS to the layer underneath. Hence, for the samples shown in Fig. 5.4 (b) only the adhesion of PDMS to SiO_2 can be evaluated. To evaluate the adhesion among the remaining layers the free-standing membranes of Fig. 5.4 (c) were created to allow peeling from both the parylene and the PDMS sides. For the flexible test structures, peeling was performed manually. As shown in Fig. 5.11 (a), peeling of the PDMS layer was very easy on the areas without ceramic layers. However, when the peeling reached the region with the ceramic layer, it was not possible to peel further anymore and PDMS was torn at the edge of this region, as can be seen from Fig. 5.11 (b). This can prove the improvement in adhesion strength in the areas with ceramic layers.

5.7.5. PBS SOAK TEST

To simulate oxidizing and ionic conditions inside the human body, samples with a pre-patterned grid were soaked in a 1X PBS solution at room temperature for 60 days. All samples were monitored optically and a tape test was performed after 12 and 60 days. As expected, for those samples that had PDMS on parylene with and without oxygen plasma, delamination of PDMS happened directly after creating the grid patterns on the film and even before a tape test. For those samples that included the interlayers between PDMS and parylene, tape tests performed after 12 and 60 days revealed no delamination.

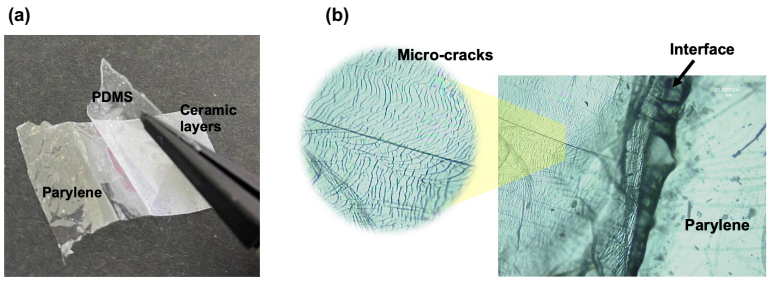


Figure 5.13: (a) Delamination of PDMS from parylene after a two-month soak test, (b) Micro-cracks appearing on the sample caused by the force applied during the peel test after two months soak test at 67 °C

5.7.6. ACCELERATED AGING TEST

Studying the long lifetime of implant material in the human body is not feasible. The conventional way of overcoming this problem is to subject materials to elevated temperatures, known as the "accelerated aging test". To evaluate the long-term performance of our encapsulation stack, samples, soaked in a PBS solution, were exposed to elevated temperatures to accelerate the aging. The 10-degree rule states that increasing the temperature by about 10 °C roughly doubles the rate of polymer reactions [29]. The acceleration factor is calculated by Equation (5.2). T_1 is the test temperature with respect to body temperature T_2. Therefore, maintaining a polymer at 67 °C for 2 months is equivalent to aging it for 16 months at 37 °C. The assumption underlying accelerated aging is that the degradation of a polymer follows first-order kinetics and that the elevated temperature does not induce any chemical changes or phase transitions that would not have occurred at 37 °C [29].

$$\text{Acceleration factor} = 2^{(T_1 - T_2)/10} \tag{5.2}$$

After two months, the samples were optically inspected, and peel tests were performed to evaluate the adhesion strength. The peel test revealed no delamination for the samples having ceramic interlayers. As shown in Fig. 5.13 (a), PDMS was peeled off from parylene C only over the region with no ceramic layers. This test was also performed for a similar sample without SiC and delamination was observed after the peel test proving the effect of this layer on the adhesion improvement. As depicted in the optical microscopy image shown in Fig. 5.13 (b), the presence of micro-cracks on the ceramic layers is related to the force applied during the peel test. These observations are in accordance with our previous findings in which a strong adhesion for the proposed encapsulation layer was demonstrated and prove that even a two-month soak test at 67 °C does not lead to a deterioration of the adhesion strength.

5.7.7. *In vivo* EXPERIMENTS

It is important to notice that no soak test can completely mimic the conditions in the human body. Soak tests are only intended to ensure that there are no obvious hazards before a material is incorporated into a device for a clinical trial. Therefore, to study the longer-term adhesion strength of our proposed encapsulation stack, *in vivo* exper-

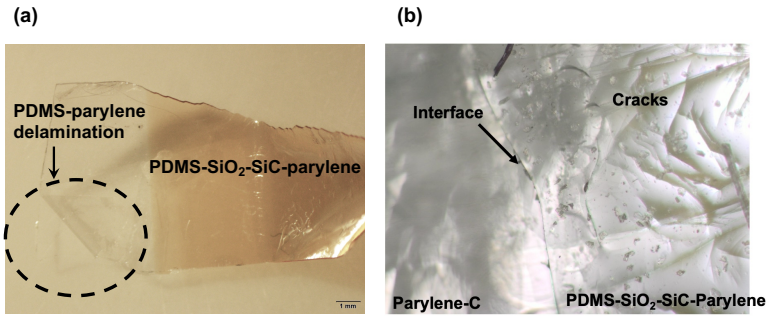


Figure 5.14: Optical image of the sample after a two-month implantation, (a) PDMS delamination from parylene C on the region without ceramic layers, (b) sample after the peel test

iments were performed for two months. The results of the experiments could, potentially, provide a more realistic evaluation compared to the aforementioned accelerated aging study because the samples are subjected to an environment similar to what an implantable device would encounter inside the body.

The samples presented in Fig. 5.4 (c) were disinfected with isopropyl alcohol (IPA) and rinsed with distilled water before implantation. Next, two samples were implanted subcutaneously, on the left and right subscapular regions of a rat, and the wounds were later closed by using two sutures and a vet bond. The samples were optically inspected after explantation, followed by a peel test to evaluate the adhesion.

Fig. 5.14 (a) illustrates the optical microscopy results from the explanted samples after a two-month implantation period. Delamination of PDMS from parylene C was observed in the region without ceramic layers and no delamination was observed for the area with PDMS-SiO_2-SiC-parylene C multilayers. However, it seems that there is some discoloration suggesting some changes in the full encapsulation stack. It has not been possible to identify the nature of these changes. However, this could suggest that reactions that lead to discolouration are different in the body compared to the PBS solution since no color change was observed after the soak test even at a high temperature. However, to be able to make such a claim that longer soak tests in PBS are required. It has been suggested that silicone storage in water for over 6 months resulted in an increase in cross-link density and consequently the modulus of silicone and also color change [30]. This effect might be also relevant for PDMS. However, the discoloration might be related to changes in the ceramic layers or parylene.

The peel tests were performed manually for the explanted samples. As shown in Fig. 5.14 (b), the PDMS layer could easily be peeled off from the areas with no ceramic interlayers. However, once the ceramic interlayers were reached, peeling was not possible anymore, and the PDMS layer was torn at the edge of this region. The cracks that appeared on the area with ceramic layers were due to the force applied during the peel test.

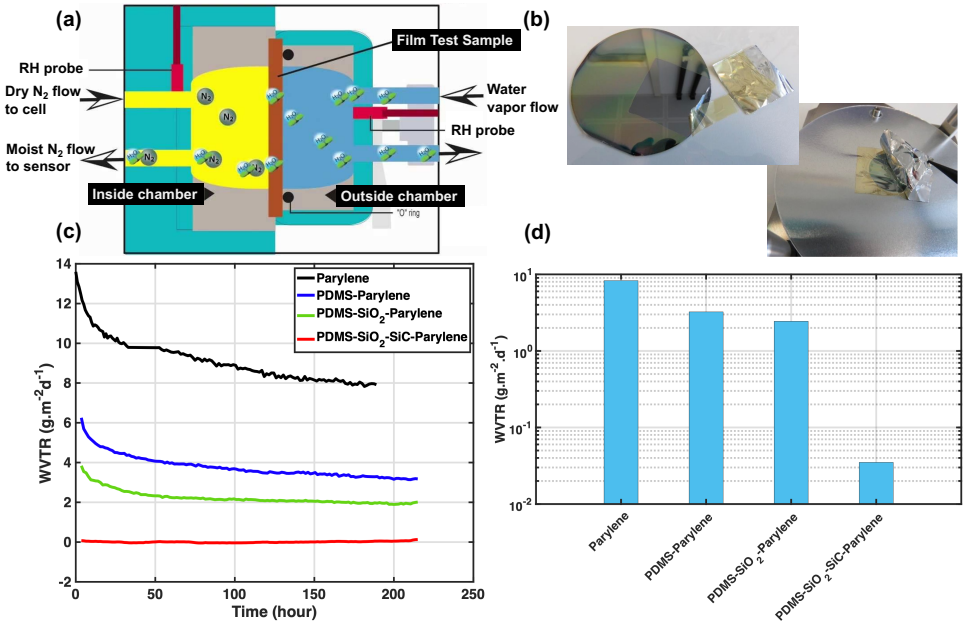


Figure 5.15: (a) WVTR tool schematic (courtesy Mocon), (b) Method used to transfer the flexible encapsulation layer first to an Al foil and then install it in the tool, (c) WVTR result comparing different encapsulation stacks, and (d) WVTR results comparing different encapsulation stacks after 100 hours stabilization

5.8. MOISTURE BARRIER PROPERTY

Apart from improving the adhesion between PDMS and parylene C, the proposed ceramic layers also act as barrier layers against moisture. Since this also depends on the composition of ceramic layers, the three different recipes of SiC were evaluated in terms of the number of pinholes. Then, the SiC layer with fewer pinholes was chosen for the full encapsulation stack. Next, a water vapor transmission rate (WVTR) test was performed to evaluate the overall water vapor permeability of the full encapsulation stack.

5.8.1. WVTR TEST

WVTR test was performed using Permatran-W 3/33 from MOCON Inc. The encapsulation film is placed between two chambers, one filled with water vapor and the other one with nitrogen carrier gas as shown in Fig. 5.15 (a). The amount of water vapor permeation from one chamber to the other, through the encapsulation layer, is measured with the units of $gm^{-2}day^{-1}$.

The evaluation was performed for different flexible samples, including parylene C alone, PDMS-parylene C bi-layer stacks, PDMS-SiO_2-parylene C stacks, as well as PDMS-SiO_2-SiC-parylene C stacks. The samples were transferred to the WVTR test tool using an Al foil as shown in Fig. 5.15 (b). Then, the Al foil was removed and the encapsulation film separated a chamber with 100 % relative humidity (RH) at 38 °C from the dry nitrogen flow, which was analysed for moisture content and flow rate.

The conducted WVTR tests showed a clear improvement of the barrier property when ceramic layers are present at the interface between PDMS and parylene C. The WVTR was calculated based on measurements conducted for 100 hours after which a steady state was considered to be established (Fig. 5.15 (c)). Comparing the results obtained for parylene C alone versus the PDMS-parylene C stack, it can be concluded that the combination of materials leads to a lower WVTR. As indicated in Fig. 5.15 (d), adding barrier layers to the encapsulation stack can lead to an increase in the barrier efficiency by orders of magnitude. However, since the value is close to the upper limit of the investigation equipment, it might be difficult to accurately determine the WVTR for better barriers.

5.8.2. OPTICAL TRANSPARENCY

The optical transparency of the encapsulation layer is of paramount importance for techniques that play a significant role in modern neuroscientific studies, including optogenetics and *in vivo* optical imaging methods (e.g., calcium imaging or fluorescence imaging). Therefore, high optical transparency for wavelengths ranging from 450 nm to 850 nm is expected.

A quantitative evaluation of the optical transparency of our proposed multilayer encapsulation stack was conducted using a Perkin Elmer Lambda 950 UV/Vis (PerkinElmer, Waltham, Massachusetts). The wavelengths used for the measurement ranged from 300 nm to 1200 nm. The optical transmittance measurements are shown in Fig. 5.16 for parylene C alone, the PDMS-parylene C stack and the PDMS-SiO_2-parylene C stack show more than 80% transmittance over a broad wavelength spectrum, from 300 to 1200 nm, and specifically above 85% for the 470nm (blue light) wavelength that is mainly used in optogenetics applications. Adding SiC to the encapsulation stack shows that the optical transmittance for wavelengths higher than 600 nm is greater than 70%, which is acceptable for optical imaging. However, the optical transmittance drops to 48% for a 470 nm wavelength. This could be further improved by depositing thinner SiC layers.

5.9. DISCUSSION

To improve the adhesion of PDMS to parylene, SiC and SiO_2 are used as intermediate adhesion layers. The adhesion of SiC to parylene was initially evaluated with a tape test. The result of this test revealed a strong adhesion between the two layers under test, however, it must be noted that such a test is not ideal for investigating thin ceramic layers, as peeling them at a 180-degree angle may induce damage in the thin layer. In addition, the tape test can only give a qualitative evaluation of the adhesion strength.

This test is a reliable method for ranking the effectiveness of adhesion promoters or for quality control measurements. However, it is hard to reproduce the result. Moreover, many factors can significantly affect the results, such as the adhesion of the tape to the top layer and the peel rate applied by the user. Thus, without even considering the coating and substrate properties, there is already a considerable degree of complexity introduced just by the properties of the tape alone [31].

The peel test can give a more quantitative evaluation, as the force at which each layer is peeled from its substrate can be recorded. Here, such a test showed that the adhesion

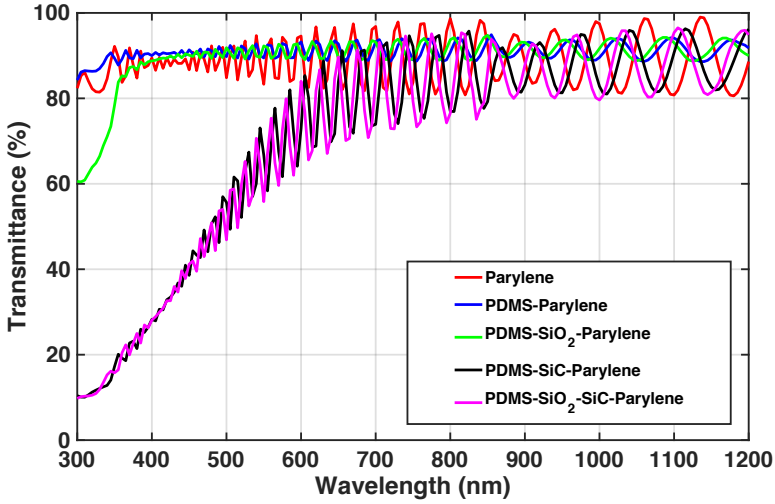


Figure 5.16: Optical transmittance measurement for different encapsulation stacks

for the stack that includes ceramic layers was much stronger than for the other two variants. However, peeling of PDMS was not possible for the sample with ceramic layers since the PDMS layer was torn before peeling. Therefore, no quantitative result was reported. The peel test also revealed no difference in the adhesion between plasma-treated and non-treated samples.

Moreover, the XPS results also confirmed these findings by indicating different peaks at the interface between SiC and parylene C compared to reference materials.

Adhesion evaluation has to be performed under similar conditions as the human body. One approach consists of soaking the samples under test at 67 °C, which accelerates the aging process and could cause an early failure of the adhesion. This temperature was also chosen to make the result comparable to other works in the literature.

However, [29, 32], suggest that the accelerated temperature should not be so high as to initiate physical or chemical processes that are unlikely to be involved in normal aging. Therefore, changes in the structure of the material cannot be excluded at this temperature. Nevertheless, no delamination was observed when performing the experiments for two months. Although the PBS solution commonly used for these types of tests can resemble the environment that an implant will see in the human body, it still lacks the complexity of the targeted *in vivo* scenario. Therefore, it is possible that the failure mechanisms usually observed during the *in vivo* experiments are neither accurately nor fully captured by such tests [16].

Nevertheless, during the *in vivo* experiments presented here, neither delamination nor peeling was observed for our proposed encapsulation stack after explantation. However, it should be noted that a longer *in vivo* experiment might reveal different results as it seems after this two-month study there is some discoloration in the explanted samples with ceramic interlayers suggesting some changes in the layers.

As mentioned before, it is expected that ceramic layers can also act as a barrier layer

against moisture, which is important especially when the adhesion is not achieved. The soak tests at room temperature revealed no difference in the performance of the three different recipes of SiC, despite their different characteristics in terms of pinhole density and stress, as adhesion was never compromised throughout the soaking period.

To better understand the resulting barrier properties of the proposed stack, a water vapor transmission rate test was employed. The results have shown that by stacking two polymer layers, the WVTR is reduced. However, adding ceramic interlayers (SiC and SiO_2) between the two polymers leads to a significant (two orders of magnitude) improvement in the moisture barrier property of the encapsulation layer.

Conformal encapsulation has the potential to solve important miniaturization challenges in the field of active neural interfaces and become the enabling factor for the realization of mm-sized implants for bioelectronic medicine [33]. The proposed encapsulation stack should also meet the other requirements needed in this work.

Finally, the proposed method allows for a gradual adjustment of the mechanical properties of the encapsulation, from a relatively rigid (parylene C) layer to a softer one (PDMS), with properties similar to those of soft tissues, while yielding a fully transparent encapsulation stack over a broad wavelength spectrum. Therefore, the proposed solution can be used for the conformal protection of a variety of flexible devices and even be combined with transparent conductors, making the device suitable for optical imaging such as calcium imaging and optogenetic applications.

5.10. SUMMARY AND CONCLUSIONS

In conclusion, in this chapter the effect of using thin ceramic layers to improve the adhesion of PDMS to parylene for the encapsulation of implantable devices was investigated. Results show that the adhesion of PDMS to parylene after using intermediate SiO_2 and SiC is so strong that no delamination was observed after 60 days soak test at room temperature. In comparison, PDMS-on-parylene and PDMS-on-plasma treated parylene delaminated easily by hand during the same test. The improvement in adhesion strength was also confirmed by XPS analysis which showed different peaks at the interface of SiC-parylene C compared to reference samples.

The proposed ceramic layers have a dual function, acting at the same time as a barrier layers against water permeation. In this work, three different SiC recipes were evaluated with respect to the number of pinholes present in each layer. The result shows that the non-silane starving mode with high amount of hydrogen leads to less pinholes in the layer. The WVTR test results have shown an improvement of about two orders of magnitude for the full stack compared to only using polymers without any additional ceramic layers.

The long-term effect of thin ceramic interlayers (SiO_2, SiC) used to improve the PDMS-to-parylene C adhesion for the encapsulation of implantable devices was also investigated in this chapter. The results show that the adhesion of PDMS to parylene C after using intermediate SiO_2 and SiC layers is significantly improved, as no delamination was observed after two months of accelerated aging, for which the samples were soaked at 67 °C. Similarly, this multilayer stack adhesion was not compromised even after *in vivo* validation, where the samples were subcutaneously implanted for two months.

As a recommendation for future work, for a better and more complete comparison

between samples with ceramic layers and samples with oxygen plasma treatment, the effects of different power, pressure, and oxygen-flow parameters during the plasma treatment process could also be investigated. However, the assumption is that the encapsulation stack with the ceramic layer will still outperform the samples with oxygen plasma treatment.

Moreover, to understand the nature of the bonds created between the SiC and parylene, more analysis is needed such as TEM/EDS to gain more understanding of the interface and the distribution of the atoms.

Furthermore, further investigation of the adhesion strength under the effect of bias voltages at elevated temperatures could shine more light on the adhesion strength and mimic the condition in implantable medical devices more realistically. It is expected that such experiments may reveal failure mechanisms that cannot be observed when passive tests are performed. Eventually, the proposed encapsulation stack can be employed as a packaging of bare silicon chips on active implants [34].

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6

CONCLUSIONS AND RECOMMENDATIONS

This chapter summarizes the conclusions of this thesis and discusses the impact and contribution of this work. In the end, recommendations are provided on how to proceed with this project.

6.1. CONCLUSIONS

This thesis presents graphene-based microfabricated platform technology for multimodal neural interfaces. It demonstrates the development of fully transparent CVD-based multilayer graphene electrodes using a wafer-scale transfer-free process for the next generation of optically transparent and MRI-compatible neural interfaces. The full electrochemical characterization of the graphene electrodes performed in this work demonstrates low impedance, high CSC, and high CIC characteristics for the fabricated electrodes and provides a favorable comparison with conventional metal electrodes fabricated with the same size and geometry and tested in a similar condition.

Multilayer graphene electrode surfaces were then modified with Pt NPs using a spark-ablation method to enhance their electrochemical characteristics without compromising their optical transparency. The electrochemical characterization suggests improvement in the impedance, CSC, and CIC of the electrodes. Moreover, long-term electrochemical stability testing of the electrodes demonstrated the stability of the printed Pt NPs on the graphene electrode surface with a minor compromise of the electrochemical properties of the electrodes.

Finally, a hybrid encapsulation stack including parylene C and PDMS with thin ceramic interlayers was fabricated and validated to be employed as the encapsulation layer on the final neural-interface device. The encapsulation stack offers a suitable water barrier property and high optical transparency, both needed for the final multimodal graphene-based platform.

To demonstrate the possibility of using the graphene electrodes fabricated in this

work for multimodal neural interfacing, photo-induced artifacts in the electrical domain and MRI artifacts due to the potential magnetic susceptibility differences of the electrode and the surrounding tissue were tested. The fabricated graphene electrodes show no optical artifact or MRI interference. The multimodal platform technology introduced in this thesis can be used as a tool in multimodal measurements combining electrical, optical, and magnetic domains. Moreover, the fabricated electrodes and encapsulation stack both reveal the high optical transparency required for optical measurements.

6.2. CONTRIBUTIONS

The multilayer graphene electrodes developed in this work were fabricated using a wafer-scale transfer-free process. The fabrication process used in this thesis provides several advantages. First, the CVD process used for graphene growth provides the possibility of developing graphene layers only over desired areas patterned on the catalyst layer. Using Mo as a catalyst layer allows the creation of graphene with fewer wrinkles at a high-temperature growth process compared to graphene grown on other catalyst layers. Moreover, Mo is biocompatible and biodegradable, and potential residues left from the catalyst on the final device do not pose any risk to the surrounding tissue as compared to other catalyst materials such as Cu.

Second, the transfer-free process does not have the complexity of the transfer process of graphene such as crack formation in graphene, polymer contamination, catalyst residues, wrinkling, and folding, and as a result, prevents graphene-implant performance variation from device- to- device and wafer- to- wafer.

Lastly, the transfer-free process allows for the addition of arbitrary polymers at the end of the fabrication process after all the high-temperature process steps have been performed. The required polymer can be selected based on, e.g., its mechanical characteristics that should be matched to the application requirements. The proposed encapsulation stack of PDMS-parylene with ceramic interlayers could be also applied at this step.

Multilayer graphene instead of monolayer graphene is used in this work to reduce the sheet resistance for graphene tracks, lower the total impedance, and enhance mechanical and electrical reliability. Furthermore, the increase in the number of graphene layers did not compromise the optical transparency, and the obtained optical transparency was confirmed to be sufficient for modern neuroscientific research such as optogenetics and *in vivo* optical imaging.

The multilayer graphene electrodes fabricated in this work showed a lower area-normalized impedance compared to other undoped CVD-based graphene electrodes. The obtained impedance was comparable to those of Au and Pt electrodes with the same size and geometry. The graphene electrodes fabricated in this work demonstrate the highest CSC reported so far among all CVD graphene electrodes.

To demonstrate the possibility of using the graphene electrodes fabricated in this work for multimodal neural interfacing, photo-induced and MRI artifact tests were performed and compared to the results acquired using conventional metal electrodes. Light illumination via an LED showed no artifact on the power spectrum of the recorded signal picked up from the graphene electrode. However, visible peaks were observed using the Au electrode. Moreover, the graphene electrodes did not show any image artifact in a 3

T MRI scanner. These results show that graphene multilayer electrodes with a high CSC and a low impedance could be used for the next generation of neural interfaces, enable multimodal electrical and optical recording and stimulation, and substitute the current standard metal electrodes, to additionally allow for MRI studies of the nervous system.

In the next section of this thesis, the graphene surface is modified with Pt NPs to enhance its electrochemical characteristics. A spark-ablation method is used to print NPs locally on the electrodes. This single-step process can be performed at room temperature in a dry environment. The NP deposition at room temperature enables a stress-free NP coating deposition, which does not involve thermally introduced strain forces to the electrode [1]. The surface modification practically enables the use of smaller electrodes with higher selectivity for neural recordings and allows the transfer of more charge via the electrode-tissue interface for neural stimulation under electrochemically safe conditions.

The NP deposition technique presented in this thesis yields a selective local modification of graphene neural electrodes. This opens up interesting possibilities when arrays of electrodes of various sizes are required during multimodal interaction with neural tissue. NP coatings come at the expense of less transparency and, therefore could only be applied locally, only at e.g., very small electrodes, to enhance their recording performance, while larger electrodes on the same device can remain uncoated. Besides their effect on electrochemical characteristics, Pt NPs can be employed for local biosensing. This local surface modification is not possible with electrodeposition techniques, in which all electrodes on a device will be coated simultaneously. Besides, but crucially, the proposed technique is performed at room temperature and via a dry process, as a post-processing step. It is thus compatible with polymer substrates, an integral component of future neural implants, as well as with a range of other processes and materials of the final device. These characteristics render this approach a unique tool for the enhancement of the performance of flexible neural implants.

The highest NP surface density used in this work is 40% which still has an optical absorbance below 8%. The optical transmittance of the graphene used in this work is reported to be above 80% [2]. This confirms the potential use of graphene electrodes coated with NPs for future neuroscientific research such as optogenetics and optical imaging, as adding NPs on the graphene electrode surface is not expected to have a significant impact on the electrode's optical transparency.

The results reported in this work demonstrate an improvement in the electrochemical characteristics of graphene electrodes by adding printed Pt NP coatings. This improvement is likely a result of the electrode surface area increase due to the presence of NPs. Continuous CV and VT tests were performed and showed the electrodes' electrochemical stability with printed Pt NPs. Examination of the electrode surface after continuous CV measurements did not reveal any delamination or cracks on the graphene samples with NP coating. Moreover, ultrasonic treatment has been applied to the coated electrodes to assess the mechanical stability of the coating. Results from this test do not suggest NP delamination after the treatment, as indicated by optical inspection and impedance measurements.

The last section of this thesis focuses on the soft encapsulation of implantable devices. In particular, it focuses on the effect of using thin ceramic layers to improve the

adhesion of PDMS to parylene for the encapsulation of implantable devices. Results show that the adhesion of PDMS to parylene after using intermediate SiO_2 and SiC is so strong that no delamination was observed after 60 days of soak test at room temperature. In comparison, PDMS- on- parylene and PDMS- on- plasma- treated parylene were delaminated manually during the same test.

The proposed ceramic layers have a dual function, acting at the same time as a barrier layer against water permeation. In this work, three different SiC recipes were evaluated concerning the number of pinholes present in each layer. The result shows that the non-silane starving mode with a high amount of hydrogen leads to fewer pinholes in the layer. The WVTR test results have shown an improvement of about two orders of magnitude for the full stack compared to only using polymers without any additional ceramic layers.

The long-term effect of thin ceramic interlayers (SiO_2, SiC) used to improve the PDMS-to-parylene-C adhesion for the encapsulation of implantable devices was also investigated in this work. The results show that the adhesion of PDMS to parylene C after using intermediate SiO_2 and SiC layers is significantly improved, as no delamination was observed after two months of accelerated aging, for which the samples were soaked at 67 °C. Similarly, this multilayer stack adhesion was not compromised even after *in vivo* validation, where the samples were subcutaneously implanted for two months.

6

6.3. RECOMMENDATIONS

6.3.1. GRAPHENE ELECTRODES FABRICATION AND CHARACTERIZATION

The transfer-free fabrication process used in this thesis is more compatible than the graphene transfer process with conventional wafer-scale fabrication processes. This could provide the possibility of monolithic integration of active circuitry to the device. This possibility can open up new doors to make neural interfaces with integrated electronic circuitry and also optrodes with integrated LEDs. The proposed fabrication process can be also an advantageous method for the fabrication of optoelectronic devices.

Regarding the characterization methods, there were some differences between the water windows used for graphene CV tests in the literature. The water window chosen in this work is on the conservative side. However, a detailed study on the safe potential limit used for CV measurement for graphene material is necessary to further appreciate the capabilities of graphene as a stimulation electrode.

Regarding photo-induced artifacts, a previous report for a monolayer graphene electrode tested with a 470 nm LED did not show any artifact [3]. However, a photo-induced artifact was observed with stacked 4-layer graphene tested using blue laser diodes [4]. Therefore, it was uncertain whether the artifact was induced due to the larger thickness of graphene, different light sources used for this test, or yet another reason, such as electrical crosstalk. The artifact-free result in this work was obtained with multilayer graphene using an LED light source with a wavelength of 470 nm. The same measurement with different thicknesses of graphene still did not show any artifact. This could prove the lack of dependence of the photoelectrochemical effect on the graphene thickness. However, to be able to conclusively argue about such independence, additional characterization would be needed. It is possible that when a coherent light source, i.e.

a laser diode, is used instead, photo-induced artifacts will be generated [5]. Moreover, it should be noted that for a thorough investigation of the photo-induced artifact, this test must be performed in an *in vivo* condition as the light scattering and absorption in tissue differs from that in a simple PBS environment. However, this PBS test is a good first indicator and can additionally provide information about the effect of increased thickness on any generated artifact.

Regarding the MRI-compatibility test, the use of a phantom instead of real tissue might lead to a different temperature distribution and thus a different degree of image artifacts. Therefore, an *in vivo* MRI test with graphene electrodes implanted would be advantageous.

6.3.2. GRAPHENE ELECTRODES WITH PT NPS

Regarding the electrochemical stability assessment performed for graphene electrodes with Pt NP coatings, continuous CV tests were performed only for 500 cycles. To further investigate the electrochemical stability of the electrodes, a larger number of CV cycles (above 100,000) could be used.

The test samples used for the stability assessment of the Pt NP coating on graphene in this work have not been optimized for these tests. In particular, the samples have been fabricated on a Si substrate where graphene sits on a silicon-oxide layer, from which it delaminates during the continuous VT and ultrasonic treatments. This fact limited the intensity and duration of the treatment. In a practical application scenario of a neural interface, the oxide layer underneath the graphene electrodes is removed and substituted with parylene, as shown in [2]. Therefore, to ensure a more conclusive result the stability tests should be repeated and extended for the final device. The long-term VT test should also be repeated for the final implantable device as this device will not have a Mo layer underneath graphene which restricted this test due to Mo corrosion. The presence of the Mo layer probably had a negative impact on the results.

Nevertheless, the electrochemical and mechanical stability of the Pt NP coating of graphene electrodes suggest that printed NPs are quite stable. It is not clear whether the stability of printed NPs is because of the printing method, the multilayer nature of our graphene, or some other factor. It would certainly be interesting to compare the stability of the NPs deposited with other deposition techniques and/or single-layer graphene, but unfortunately, these results are lacking in the literature.

Furthermore, the delamination of the NP coating leads to the deterioration of the electrochemical characteristics over time, which consequently results in functionality loss. Moreover, the detached NPs may undergo biodispersion inside the body after implantation with the risk of becoming toxic to the tissue. Additional treatments, such as prolonged immersion in a PBS solution, or dipping in an agarose gel [6], could be added to the current suite, to further assess the long-term adhesion and stability of the coating for potential chronic applications.

If necessary, roughening the electrode surface before NP printing could be investigated in the future as a means to enhance the NP adhesion to the electrode surface. Previously, roughening the electrode surface of metal electrodes before PEDOT:PSS coating increased the mechanical bonding between the electrode and its coating, thereby resulting in higher stability [7].

Finally, other NPs such as gold, Irridium oxide, or a combination of materials can be used as a coating on the graphene electrodes to observe if synergic impact of various materials can improve the electrochemical properties of the graphene electrodes even further. Different NP materials can be also printed on different electrodes on the same device. This could have some potential in biosensing applications.

6.3.3. SOFT ENCAPSULATION

Regarding the last section of this thesis, for a better and more complete comparison between samples with ceramic layers and samples with oxygen-plasma treatment, the effects of different power, pressure, and oxygen-flow parameters during the plasma treatment process could also be investigated. However, the expectation is that the encapsulation stack with the ceramic layer will still outperform the samples with oxygen-plasma treatment.

Moreover, to understand the nature of the bonds created between the SiC and parylene, more analysis such as TEM/EDS is needed to gain more insights into the interface and the distribution of the atoms.

Furthermore, further investigation of the adhesion strength under the effect of bias voltages at elevated temperatures could shine more light on the adhesion strength and mimic the condition in implantable medical devices more realistically. It is expected that such experiments may reveal failure mechanisms that cannot be observed when passive tests are performed. Eventually, the proposed encapsulation stack can be employed as a packaging to encapsulate chips that are used in the active implants [8].

In general, the graphene-based neural interface fabricated in this work could be used for multimodal measurements in neuroscientific research. It would be interesting to see whether the graphene electrode can substitute the conventional metal electrodes in real experiments. Therefore, in vivo experiments using graphene electrodes for electrical neural recording and stimulation combined with optical imaging, optogenetics, and MRI measurements could add other perspectives to this work.

Moreover, it would be interesting to expand the capability of this multimodal platform by adding the opportunity for measurements in other domains. The printed Pt NPs, for example, can be used for biosensing. The spark ablation method provides the opportunity to have graphene electrodes without and with NPs with various surface densities and even different materials in a single device. This could offer the advantages of monitoring different biomolecules using different NP coatings on the electrode.

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A

APPENDIX A

A.1. GRAPHENE ELECTRODE WITH POLYMER SUBSTRATE FABRICATION PROCESS FLOW

This chapter includes the process flow used to fabricate the graphene electrodes encapsulated with two different types of polymers (parylene and PDMS). The initial fabrication process flow is similar to before the polymer deposition. After this step, the procedure should be followed based on the material used for the encapsulation.

A.1.1. STARTING MATERIAL

Use 10 double-sided polished Si wafers (p-type) with a diameter of 100mm and a thickness of 500 µm.

A.1.2. PART1: CREATION OF ZERO LAYERS: FRONTSIDE COATING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of the following steps:

1. A treatment with hexamethyldisilazane (HMDS) vapor, with nitrogen as a carrier gas, to improve resist adhesion to the wafer.
2. Spin coating of Shipley SPR3012 positive photoresist, dispensed by a pump.
3. A soft bake (a.k.a. pre-bake) at 95 °C for 90 seconds.
4. An automatic Edge Bead Removal (EBR) with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use the default program: '1 - Co - zero layer' (with a resist thickness of 1.400 µm), which has a larger EBR than the standard program.

A

ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose the mask called 'COMURK' with the job 'litho/Zefwam'. Use the correct exposure energy (check the energy table (120mJ/cm2)). This results in stepper alignment markers and verniers for wafers.

DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of the following steps:

1. A post-exposure bake at 115 °C for 90 seconds, to prevent standing waves on the sidewalls of the resist structures.
2. Developing with Shipley MF322 with a single puddle process.
3. A hard bake (a.k.a. post-bake) at 100 °C for 90 seconds.

Always follow the instructions for this equipment. Use the program 'program Dev - SP'.

INSPECTION

Visually inspect the wafers by using a microscope. Check if the correct mask is exposed and whether there are any resist residues (resist residues are not allowed in the lab).

Check the line width of the structures and the overlay of the exposed pattern (if the mask was aligned to a previous pattern on the wafer).

WAFER NUMBERING

Use the glass pen in the lithography room to mark the wafers with the 'batch' and 'wafer' numbers. Write the numbers in the photoresist, just above the wafer flat. Always do this after exposure and development. It is NOT allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

PLASMA ETCHING: ALIGNMENT MARKERS (URK'S) INTO SILICON

Use the Trikon Ω 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and durations from the etch recipe.

Use sequence 'URK-NPD' (with a platen temperature of 20 °C) to etch 120 nm deep ASM URK's into the Si.

Check the depth that you etched by using Dektak. The target is 120 nm.

PHOTORESIST STRIPPING

Use the Tepla Plasma 300 system to remove the photoresist from the wafers in an oxygen plasma environment. Follow the instructions specified for the Tepla resist stripper, and use the quartz carrier to load the wafers.

Use program 1 which uses 1000 watts of power, an automatic endpoint detection, and an additional 2 minutes of over-etching.

CLEANING

The cleaning procedure consists of the following steps:

1. Clean the wafers for 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench 'HNO_3 99% (Si)' and the carrier with the white dot.

2. Rinse in the Quick Dump Rinser (QDR) with the standard program until the resistivity is 5 MΩ.

3. Clean the wafers for 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use the wet bench "HNO_3 69,5% 110 °C (Si)" and the carrier with the white dot.

4. Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

5. Use the 'Avenger Ultra-Pure 6' rinser/dryer with the standard program, and the white carrier with a red dot to dry the wafers.

A.1.3. PART1: CREATION OF ZERO LAYERS: BACKSIDE

COATING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of the following steps:

1. A treatment with HMDS vapor, with nitrogen as a carrier gas, to improve resist adhesion to the wafer.

2. Spin coating of Shipley SPR3012 positive photoresist, dispensed by a pump.

3. A soft bake (a.k.a. pre-bake) at 95 °C for 90 seconds.

4. An automatic EBR with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use the default program: '1 - Co - zero layer' (with a resist thickness of 1.400 µm), which has a larger EBR than the standard program.

ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose the mask called 'COMURK' with the job 'litho/Zefwam'. Use the correct exposure energy (check the energy table (120mJ/cm2)). This results in stepper alignment markers and verniers for wafers.

A

DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of the following steps:

1. A post-exposure bake at 115 °C for 90 seconds, to prevent standing waves on the sidewalls of the resist structures.
2. Developing with Shipley MF322 with a single puddle process.
3. A hard bake (a.k.a. post-bake) at 100 °C for 90 seconds.

Always follow the instructions for this equipment. Use the program 'program Dev - SP'.

INSPECTION

Visually inspect the wafers by using a microscope. Check if the correct mask is exposed and whether there are any resist residues (resist residues are not allowed in the lab).

Check the line width of the structures and the overlay of the exposed pattern (if the mask was aligned to a previous pattern on the wafer).

PLASMA ETCHING: ALIGNMENT MARKERS (URK'S) INTO SILICON

Use the Trikon Ω 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe.

Use sequence 'URK-NPD' (with a platen temperature of 20 °C) to etch 120 nm deep ASM URK's into the Si.

Check the depth that you etched by using Dektak. The target is 120 nm.

PHOTORESIST STRIPPING

Use the Tepla Plasma 300 system to remove the photoresist from the wafers in an oxygen plasma environment. Follow the instructions specified for the Tepla resist stripper, and use the quartz carrier to load the wafers.

Use program 1 which uses 1000 watts of power, an automatic endpoint detection, and an additional 2 minutes of over-etching.

CLEANING

The cleaning procedure consists of the following steps:

1. Clean the wafers for 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench 'HNO_3 99% (Si)' and the carrier with the white dot.
2. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.
3. Clean the wafers for 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use the wet bench "HNO_3 69,5% 110 °C (Si)" and the carrier with the white dot.

4. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.

5. Use the 'Avenger Ultra-Pure 6' rinser/dryer with the standard program, and the white carrier with a red dot to dry the wafers.

A.1.4. PART2: DRIE PREPARATION

BACKSIDE STANDARD (STD) OXIDE DEPOSITION

Use the Novellus to deposit 5 µm of PECVD oxide on the backside of the wafer.

For oxide deposition use reipe 'xxxstdteos at 350 °C' (check Novellus logbook for the required deposition time).

FRONTSIDE STD OXIDE DEPOSITION

Use the Novellus to deposit 2 µm of PECVD oxide on the front side of the wafer.

For oxide deposition use reipe 'xxxstdteos at 350 °C' (check Novellus logbook for the deposition time).

OXIDE THICKNESS MEASUREMENT

Use the Leitz MPV-SP measurement system to measure the oxide thickness. Use the recipe program: 'Th. SiO2 on Si larger than 50nm auto5pts'.

Wollam ellipsometer can be also used for this measurement.

COATING AND BAKING FOR THE BACKSIDE

Use the EVG 120 wafer track to coat the wafers with photoresist, and follow the instructions specified for this equipment. The process consists of treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with AZ ECI 3027 positive photoresist, and a soft bake at 95 °C for 90 seconds.

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use the coating recipe of 'Co –3027 – 3,1um – noEBR' (resist thickness: 3.100 µm).

ALIGNMENT AND EXPOSURE

Use the SUSS MicroTec MA/BA8 mask aligner to expose the photoresist. Use mask 'device BE2325', layer DRIE.

Calculate the exposure time by consulting the contact aligner exposure energy data log.

DEVELOPMENT

Use the EVG 120 wafer track to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

Use the development program 'Dev – SP'.

INSPECTION

Visually inspect the wafers by using a microscope, and check the openings in the resist.

PLASMA ETCHING OF BACKSIDE OXIDE

Use the Drytek 384T plasma etcher and follow the operating instructions from the manual when using this machine. The process conditions of the etch program should not be changed.

Use the program 'StdOxide' with the etch rate of 8-10 nm/s and change the time to 11 min. Try this recipe first on a test wafer to ensure the etch rate is as before.

CLEANING PROCEDURE

Plasma strip:

Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier to load the wafers. Use program 4 (not only for photoresist stripping)

Wet cleaning:

The cleaning procedure consists of the following steps:

1. Clean the wafers for 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench 'HNO_3 99% (Si)' and the carrier with the white dot.
2. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.
3. Clean the wafers for 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use the wet bench "HNO_3 69,5% 110 °C (Si)" and the carrier with the white dot.
4. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.
5. Use the 'Avenger Ultra-Pure 6' rinser/dryer with the standard program, and the white carrier with a red dot to dry the wafers.

A.1.5. PART3: MOLYBDENUM (MO) CATALYST AND GRAPHENE GROWTH

MO DEPOSITION: 50NM

Use the TRIKON SIGMA sputter coater for the deposition of the catalyst metal Mo layer on the process and test wafers. Follow the operating instructions from the manual when using this machine.

If necessary perform a target clean with recipe '-Trgt-Cln-Mo-50 °C'.

Use recipe 'Mo-50nm-50 °C' for Mo deposition.

For visual inspection, note that the metal layer must look shiny.

COATING AND BAKING

Use the EVG 120 wafer track to coat the wafers with photoresist, and follow the instructions specified for this equipment. The process consists of treatment with HMDS vapor with nitrogen as a carrier gas, spin coating with AZ ECI 3027 positive photoresist, and a soft bake at 95 °C for 90 seconds. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating 'Co –3012 – 1.4um' (resist thickness: 1.400 µm). A recipe with a 2.1 µm resist thickness is also possible.

ALIGNMENT AND EXPOSURE

Use the SUSS MicroTec MA/BA8 mask aligner to expose the photoresist. Use mask for device 'BE2325', layer 'GRAPHENE'.

Calculate the exposure time by consulting the contact aligner exposure energy data log.

DEVELOPMENT

Use the EVG 120 wafer track to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds. Always check the temperature of the hotplates first.

Use development 'program Dev – SP'.

For Visual inspection, check the wafers through a microscope for the openings designed in the mask.

PLASMA ETCHING OF MO

Use the Trikon Ω 201 plasma etcher.

Follow the operating instructions from the manual when using this machine.

Use sequence 'Mo-TEST2' and set the etching time to 30s.

Note that this etching time should be first confirmed on a test wafer.

CLEANING PROCEDURE

Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 1 and in case there is a problem with Tepla, use N-Methyl-2-pyrrolidone (NMP) in SAL in an ultrasonic bath for 5-10 min.

For visual inspection, note that the metal layer must look shiny.

GRAPHENE GROWTH

Use the AIXTRON BlackMagic Pro to grow graphene using LPCVD at 935 °C.

Use recipe 'Mo-NEW-935 °C-toph 1050 °C-20min-CH4-20minpre-annealing'.

Before proceeding with the processing, the presence of graphene should be confirmed on the first wafer using Raman spectroscopy.

Note: The process wafers are now considered Cu-contaminated. Beware of which tweezers to use when handling the wafers. Put the wafers in a process box dedicated to Cu-contaminated processes.

A.1.6. PART4: METAL DEPOSITION AND PATTERNING

METAL DEPOSITION

Use the TRIKON SIGMA sputter coater for the deposition of the metal interface Ti+Al(1%Si) layer on the process and test wafers.

Use the dedicated transport wafers and the cassette for contaminated wafers.

Follow the operating instructions from the manual when using this machine.

If necessary perform a target clean with recipes '-Trgt-ClnTi-50 °C' and '-Trgt-Cln-AlSi-50 °C'.

Use recipe 'Ti100nmAl675-50 °C' for the metal deposition.

For the visual inspection, note that the metal layer must look shiny.

COATING AND BAKING

MANUAL COATING should be performed using a Brewer manual spinner as the wafers are contaminated.

Use contaminated chuck and contaminated hotplate for contaminated wafers.

1. 10 minutes of treatment with HMDS vapor with nitrogen as a carrier gas should be performed before photoresist coating.
2. AZ-ECI-3027 positive photoresist spin coating (2.1 µm) using the recipe 'AZ-ECI-3027-2100nm'.
3. A soft bake at 95 °C for 1 minute.

ALIGNMENT AND EXPOSURE

Use the SUSS MicroTec MA/BA8 mask aligner to expose the photoresist. Use mask for device 'BE2325', layer 'METAL'.

Calculate the exposure time by consulting the contact aligner exposure energy data log.

Use contaminated chuck for contaminated wafers.

DEVELOPMENT

A manual development step should be performed as follows:

1. Post-exposure baking at 115 °C for 1 minute.
2. Photoresist development using Shipley MF322 developer for 1 minute.
3. Visual inspection of the wafers by using a microscope, and checking the openings.
4. Hard baking at 100 °C for 1 minute.

Use contaminated chuck for dryer and hotplate for contaminated wafers.

ETCHING OF TI+AL (1%SI)

An extra baking step of 30 minutes at 115 °C for the photoresist is needed before the etching step to prevent photoresist delamination during the wet etch process.

Perform a wet etching step using HF 0.55%. (SAL lab).

The etching time should be first confirmed on a test wafer.

CLEANING PROCEDURE

Use 5 minutes of exposure to Acetone followed by 5 minutes of isopropanol alcohol (IPA) to remove the remaining photoresist. Then rinse the wafer in DI water for 5 minutes.

Note that the contaminated rinser/dryer should be used for contaminated wafers.

A.1.7. PART5: POLYMER ENCAPSULATION-FIRST LAYER

In this step, parylene or PDMS should be deposited/spin-coated on the wafers.

PARYLENE DEPOSITION

Deposit 10 µm parylene on the wafers using parylene SCS LabCoater in the MEMS lab. For this purpose, use 20 g of dimer. Follow the instructions for parylene deposition. Also, use the A-174 Silane adhesion promoter before deposition. Do not forget to use the contaminated carrier and carrier wafers. Use one dummy wafer to check the etch rate later on. Note that parylene is deposited on both the front and back sides of the wafer if no carrier wafer is used. Therefore, carrier wafers can be attached to the process wafers to prevent parylene deposition on the other side of the wafer.

PDMS SPIN COATING

Mix Sylgard 184 elastomer and curing agent with a ratio of 10/1 using 6 grams of elastomer per wafer. Mix and degas the solution in Thinky are-250 mixer.

Use the Brewer Science Manual Spinner to spin coat the PDMS solution on the wafer. Make sure to cover the spinner with aluminum foil to prevent PDMS residues everywhere on the tool.

Use program 'x-PDMS-50u' for spin coating. Bake the wafer in the Memmert oven for 60 minutes at 90°C to ensure full curing of the PDMS layer.

Use contaminated chuck and wafer carrier for contaminated wafers.

A.1.8. PART6: METAL MASK FOR POLYMER ETCHING

The metal layer used for polymer etch differs for each polymer. Al(1%Si) can be used as the hard mask for PDMS etch. However, Al does not have a proper adhesion to parylene. Therefore, to etch parylene, the hard mask should also have Ti as the adhesion promoter.

METAL DEPOSITION

Before depositing metal on top of the polymer layer it is important to check the outgassing of the polymer layer. Perform a leak-up rate (LUR) test for the polymer layer. There is a special protocol in the logbook.

Use the TRIKON SIGMA sputter coater for the deposition of the metal layer on the polymer.

Al(1%Si)/Ti metal layer is used as a hard mask for parylene etching and Al(1%Si) is used as a hard mask for PDMS etching.

Follow the operating instructions from the manual when using this machine.

Use the dedicated transport wafers and the cassette for contaminated wafers.

If necessary, perform a target clean with recipes '-Trgt-Cln-Ti-25' and '-Trgt-Cln-AlSi-25-LP' for parylene-based devices and use '-Trgt-Cln-AlSi-25-LP' for PDMS-based devices.

For metal deposition, use recipe 'Ti100nm-AlSi500nm-Org' for parylene-based devices and use recipe 'AlSi-500nm-1kW-25C' for PDMS-based devices.

For visual inspection, note that the metal layer must look shiny.

COATING AND BAKING

The manual coating is used for this step using Brewer manual spinner.

Use contaminated chuck and hotplate for contaminated wafers.

1. 10 minutes of treatment with HMDS vapor with nitrogen as a carrier gas should be performed before photoresist coating.

2. AZ-ECI-3027 positive photoresist spin coating (4.0 µm) using the recipe 'AZ-ECI-3027-4000nm'.

3. A soft bake at 85-90 °C for 1.5 minute.

Note: Lower the soft bake temperature to below 90 °C and increase the time to make sure it is not causing any problems in parylene as the glass transition temperature of Parylene is around 90 °C.

ALIGNMENT AND EXPOSURE

Use the SUSS MicroTec MA/BA8 mask aligner to expose the photoresist. Use mask for device BE2325, layer PDMS. Use preset3 in the contact aligner and try to align the alignment marks on the backside of the wafer to the alignment marks on the front. Calculate the exposure time by consulting the contact aligner exposure energy data log.

Use contaminated chuck for contaminated wafers.

DEVELOPMENT

Manual development can be performed as followed:

1. Post-exposure baking at 115 °C for 1 minute.

2. Photoresist development using Shipley MF322 developer for 1 minute.

3. Visual inspection of the wafers by using a microscope, and checking the openings.

4. Hard baking at 85-90 °C (Reduce the temperature to about 80 °C and extend the baking time to around 1 hour).

Use contaminated chuck for dryer and hotplate for contaminated wafers
Visually inspect the wafers through a microscope, and check openings.

ETCHING OF AL (1%SI)

An extra baking step of 30 minutes at 115 °C for the photoresist is needed before the etching step to prevent photoresist delamination during the wet etch process.

Perform a wet etching step using HF 0.55%. (SAL lab).
The etching time should be first confirmed on a test wafer.

CLEANING PROCEDURE

Use Acetone followed by IPA to remove the photoresist.

A.1.9. PART7: DEEP REACTIVE ION ETCHING (DRIE)

DRIE

Use AMS110 to etch Si. Recipe: winope-single- -10 °C

A lower temperature than 0 °C is used to prevent polymer burning. It is best to do the etching in several intervals to prevent the temperature increase of the polymer.

A.1.10. PART8: OXIDE ETCHING AND MO REMOVAL

OXIDE REMOVAL

Dry etch of the oxide layer: Use AMS110, and the recipe 'oxide-Etsen-slow' to etch SiO_2.

In case, you want to use the wet process instead of dry etch, you need to use dedicated holders to protect the frontside Al. If you see any leakage on the front side and any Al damage, you can cover the front side with a photoresist layer just for more protection followed by a long baking step.

MO REMOVAL

Use Peroxide (create your bath) for about 5 minutes to remove the Mo layer.

Note that at this point, graphene-on-polymer suspended structures should be visible (graphene has a grey color).

A.1.11. PART9: POLYMER ENCAPSULATION-SECOND LAYER

Parylene deposition or PDMS spin-coating can be performed following similar steps as explained before.

Use carrier wafers to ensure sufficient mechanical support for the fragile membrane during spinning in the PDMS spin-coating step.

A.1.12. PART10: POLYMER ETCHING

POLYMER ETCH

Use AMS110 to etch parylene using 'Par-etch' recipe.

Use AMS110 to etch PDMS using 'PDMS-etch' recipe.

The polymer etch should be done until the Al layer underneath is visible.

Use test wafers to calculate the etch rate of each recipe.

AL (1%SI) REMOVAL

Use BHF 7:1 (create your bath) to remove the Aluminum and titanium (in the case of parylene-based devices) mask.

B

APPENDIX B

B.1. FABRICATION PROCESS FLOW OF GOLD AND PLATINUM ELECTRODES ON SI SUBSTRATE

The current process flow aims to develop gold (Au) and platinum (Pt) electrodes encapsulated with parylene on a Si substrate. Au and Pt are being deposited using a lift-off process.

B.1.1. STARTING MATERIAL

Use 10 single-sided polished Si wafers (p-type) with a diameter of 100mm and a thickness of 500 µm.

B.1.2. PART1: CREATION OF ZERO LAYER

COATING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of the following steps:

1. A treatment with HMDS vapor, with nitrogen as a carrier gas, to improve resist adhesion to the wafer.
2. Spin coating of Shipley SPR3012 positive photoresist, dispensed by a pump.
3. A soft bake (a.k.a. pre-bake) at 95 °C for 90 seconds.
4. An automatic EBR with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating, and follow the instructions for this equipment.

Use the default program: '1 - Co - zero layer' (with a resist thickness of 1.400 µm), which has a larger EBR than the standard program.

ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Expose the mask called 'COMURK' with the job 'litho/Zefwam'. Use the correct exposure energy (check the energy table (120mJ/cm2)). This results in stepper alignment markers and verniers for wafers.

DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of the following steps:

1. A post-exposure bake at 115 °C for 90 seconds, to prevent standing waves on the sidewalls of the resist structures.
2. Developing with Shipley MF322 with a single puddle process.
3. A hard bake (a.k.a. post-bake) at 100 °C for 90 seconds.

Always follow the instructions for this equipment. Use the program 'program Dev - SP'.

INSPECTION

Visually inspect the wafers by using a microscope. Check if the correct mask is exposed and whether there are any resist residues (resist residues are not allowed in the lab).

Check the line width of the structures and the overlay of the exposed pattern (if the mask was aligned to a previous pattern on the wafer).

WAFER NUMBERING

Use the glass pen in the lithography room to mark the wafers with the 'batch' and 'wafer' numbers. Write the numbers in the photoresist, just above the wafer flat. Always do this after exposure and development. It is NOT allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

PLASMA ETCHING: ALIGNMENT MARKERS (URK'S) INTO SILICON

Use the Trikon Ω 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe.

Use sequence 'URK-NPD' (with a platen temperature of 20 °C) to etch 120 nm deep ASM URK's into the Si.

Check the depth that you etched by using Dektak. The target is 120 nm.

PHOTORESIST STRIPPING

Use the Tepla Plasma 300 system to remove the photoresist from the wafers in an oxygen plasma environment. Follow the instructions specified for the Tepla resist stripper, and use the quartz carrier to load the wafers.

Use program 1 which uses 1000 watts of power and an automatic endpoint detection and an additional 2 minutes of over-etching.

CLEANING

The cleaning procedure consists of the following steps:

1. Clean the wafers for 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench 'HNO_3 99% (Si)' and the carrier with the white dot.

2. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.

3. Clean the wafers for 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use the wet bench "HNO_3 69,5% 110 °C (Si)" and the carrier with the white dot.

4. Rinse in the QDR with the standard program until the resistivity is 5 MΩ.

5. Use the 'Avenger Ultra-Pure 6' rinser/dryer with the standard program, and the white carrier with a red dot to dry the wafers.

B.1.3. PART2: OXIDE DEPOSITION

WET OXIDATION

Use the C1 furnace tube to grow 300 nm of wet thermal oxide on the wafer. Use the program 'wet1000'. Use an online oxide growth calculator to calculate the time needed to reach the desired thickness. Then, measure the oxide thickness using Leitz MPV-SP measurement system. Use the recipe program: 'Th. SiO2 on Si larger than 50nm auto5pts'.

B.1.4. PART3: METAL DEPOSITION

CLEANING

The cleaning procedure consists of the following steps:

1. Clean the wafers for 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench 'HNO_3 99% (Si)' and the carrier with the white dot.

2. Rinse in the Quick Dump Rinser (QDR) with the standard program until the resistivity is 5 MΩ.

3. Clean the wafers for 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use the wet bench "HNO_3 69,5% 110 °C (Si)" and the carrier with the white dot.

4. Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

5. Use the 'Avenger Ultra-Pure 6' rinser/dryer with the standard program, and the white carrier with a red dot to dry the wafers.

COATING AND BAKING FOR METAL LIFT-OFF

Use the EVG 120 wafer track to coat the wafers with photoresist, and follow the instructions specified for this equipment.

The process consists of treatment with HMDS vapor with nitrogen as a carrier gas, followed by spin coating with AZ NLOF2020 negative photoresist, and a soft bake at 95 °C for 90 seconds.

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating 'Co –nlof2020 – 3.5um – no EBR' (resist thickness: 3.500 µm).

ALIGNMENT AND EXPOSURE

Processing will be performed on the SUSS MicroTec mask aligner and follow the operating instructions from the manual when using this machine.

Mask: Graphene

Exposure time: check logbook (55 mJ equivalent)

DEVELOPMENT

Use the EVG 120 wafer track to develop the wafers, and follow the instructions specified for this equipment.

The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds.

Always check the temperature of the hotplates first.

Use the development program 'Dev – Only X-link Bake'

Use the development program 'xDens-Dev-Lift-Off'

Visually inspect the wafers by using a microscope, and check openings.

AU OR PT DEPOSITION

Use the CHA evaporator in CR10000 to deposit 10/100 nm of Ti/Au or 10/100 nm of Ti/Pt.

Note that for visual inspection, the metal layer must look shiny.

The process wafers are now considered Au- or Pt-contaminated. Beware of which tweezers to use when handling the wafers. Put the wafers in a process box dedicated to Au- or Pt-contaminated processes.

LIFT-OFF PROCESS

Perform lift-off in SAL using NMP heated bain-marie to 70 °C in an ultrasonic bath. Apply ultrasonic till all Au or Pt is removed from the areas it should be lifted off. Rinse in DI water for 5 min and dry the wafers using the contaminated chuck.

Use dedicated beakers for lift-off.

Note that for visual inspection, the metal layer (protected by the photoresist) must look shiny.

B.1.5. PART4: PARYLENE DEPOSITION

Deposit 10 µm parylene on the wafers in parylene SCS LabCoater in the MEMS lab. For this purpose, use 20 g of dimer. Follow the instructions for parylene deposition. Also, use the A-174 Silane adhesion promoter before deposition. Do not forget to use the contaminated carrier and carrier wafers. Use one dummy wafer to check the etch rate later on. Note that parylene is deposited on both the front and back sides of the wafer if no carrier wafer is used. Therefore, carrier wafers can be attached to the process wafers to prevent parylene deposition on the other side of the wafer.

B.1.6. PART5: METAL MASK FOR PARELENE ETCHING

METAL DEPOSITION

Before depositing metal on top of the polymer layer it is important to check the outgassing of the polymer layer. Perform a leak-up rate (LUR) test for the polymer layer. There is a special protocol in the logbook.

Use the TRIKON SIGMA sputter coater for the deposition of the metal layer on the polymer.

Al(1%Si)/Ti metal layer is used as a hard mask for parylene etching.

Follow the operating instructions from the manual when using this machine.

Use the dedicated transport wafers and the cassette for contaminated wafers.

If necessary, perform a target clean with recipes '-Trgt-Cln-Ti-25' and '-Trgt-Cln-AlSi-25-LP'.

Use recipe 'Ti100nm-AlSi500nm-Org'.

COATING AND BAKING

The manual coating is used for this step using Brewer manual spinner.

Use contaminated chuck for contaminated wafers and hotplate for contaminated wafers.

1. 10 minutes of treatment with HMDS vapor with nitrogen as a carrier gas should be performed before photoresist coating.

2. AZ-ECI-3027 positive photoresist spin coating (4.0 µm) using the recipe 'AZ-ECI-3027-4000nm'.

3. A soft bake at 85-90 °C for 1.5 minute.

Lower the soft bake temperature to below 90 °C and increase the time to make sure it is not causing any problems in parylene as the glass transition temperature of Parylene is around 90 °C.

ALIGNMENT AND EXPOSURE

Use the SUSS MicroTec MA/BA8 mask aligner to expose the photoresist. Use mask for device BE2325, layer PDMS. Use preset3 in the contact aligner and try to align the alignment marks on the backside of the wafer to the alignment marks on the front. Calculate the exposure time by consulting the contact aligner exposure energy data log.

Use contaminated chuck for contaminated wafers.

DEVELOPMENT

Manual development can be performed as follows.

1. Post-exposure baking at 115 °C for 1 minute.
2. Photoresist development using Shipley MF322 developer for 1 minute.
3. Visual inspection of the wafers by using a microscope, and checking the openings.
4. Hard baking at 85-90 °C (Reduce the temperature to about 80 °C and extend the baking time to around 1 hour).

Use contaminated chuck for dryer and hotplate for contaminated wafers
Visually inspect the wafers through a microscope, and check openings.

ETCHING OF AL (1%SI)

This step can be done using a wet etching process in SAL lab. Use BHF 7:1 (create your bath) to remove the Aluminum and titanium mask.

CLEANING PROCEDURE

Use Acetone followed by IPA to remove the photoresist.

B.1.7. PART6: PARELENE ETCHING

Use AMS110 to etch parylene using 'Par-etch' recipe.

CURRICULUM VITÆ

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EDUCATION

2006–2011	Bachelor's degree in Electrical Engineering University of Tehran, Tehran, Iran
2011–2014	Master's degree in Electronics Engineering Field of study: Semiconductor Devices University of Tehran, Tehran, Iran
2018–2024	Ph.D. degree in Bioelectronics Delft University of Technology, The Netherlands
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SHORT BIO:

Nasim Bakhshaee Babaroud obtained her M.Sc. degree in Electronics engineering in the field of semiconductor devices and her bachelor's degree in Electrical engineering from the University of Tehran in 2014 and 2011, respectively. During her master's studies, Nasim joined the TFL (Thin Film Laboratory) of the University of Tehran to work on her Master's project. During this period, she developed a strong proficiency in the design and microfabrication of silicon-based electrodes and their characterization for the field of neural interfaces and gained knowledge and experience in the field of microfabrication. In 2018, she started her research on flexible and implantable biomedical devices at the Department of Microelectronics (TU Delft, The Netherlands). Her doctoral research focused on the microfabricated graphene electrodes for multimodal neural interfaces used in biomedical applications. Nasim is currently an application engineer in imaging/focus competency at ASML. She is involved in new product introduction for DUV scanners and handles imaging/focus-related escalations from first-leading semiconductor industry customers. Her main research interests include Bioelectronics, MEMS microfabrication, Semiconductor devices and modeling, and process control.

List of Publications

Journal articles

- **N. Bakhshaee Babaroud**, S. J. Rice, M. C. Perez, W. Serdijn, S. Vollebregt and V. Giagka. “Surface modification of multilayer graphene electrodes by local printing of platinum nanoparticles using spark ablation for neural interfacing”. Nanoscale. 2024.

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