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Protection of Shipboard DC systems

From capacitors to ultrafast devices

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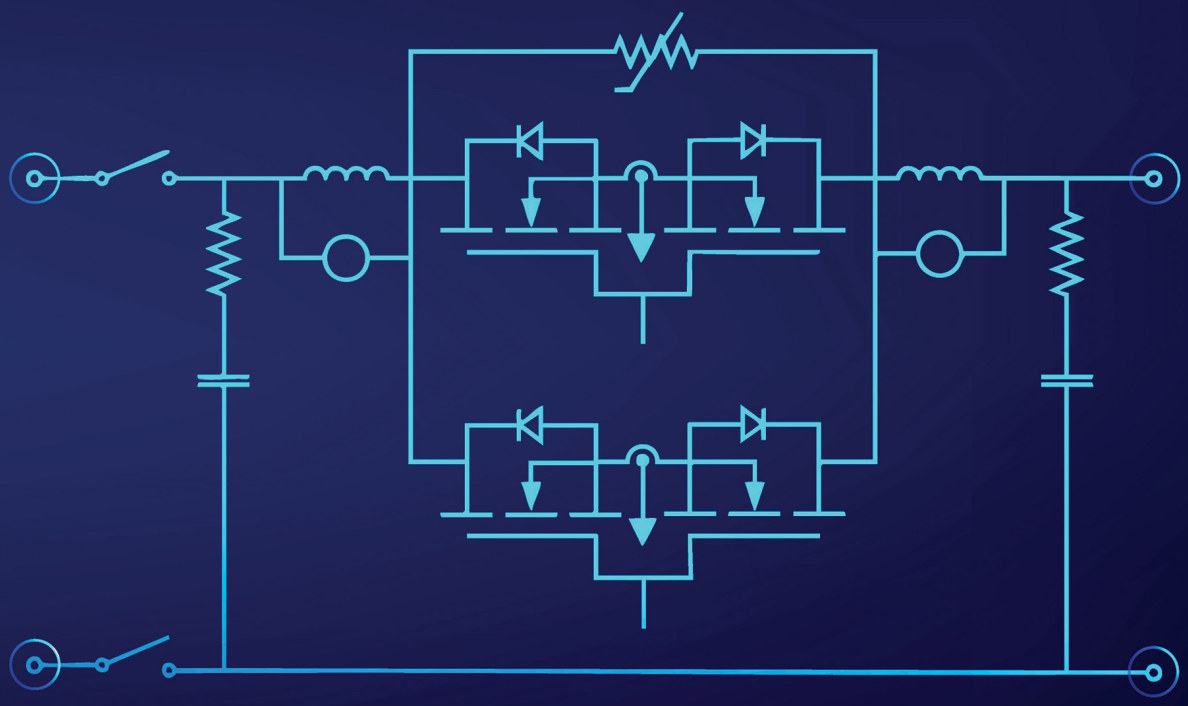

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Proefschrift

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aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op donderdag 4 december 2025 om 17:30 uur

door

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You have no responsibility to live up to what other people think you ought to accomplish. I have no responsibility to be like they expect me to be. It's their mistake, not my failing.

Richard P. Feynman

Contents

Summary

The development of shipboard DC power systems promises significant operational and economic benefits but faces major challenges in primary distribution, protection, and power scalability. As DC technology continues to mature, many aspects of shipboard implementation remain insufficiently defined to guarantee both safety and efficiency. Current regulatory standards are incomplete, and protection strategies often rely on outdated or inadequate frameworks. Unipolar and bipolar bus architectures each offer application-specific advantages, and the strategic placement of power electronics opens new possibilities for centralized and distributed switchboard designs. However, protection architectures still face limitations: breaker-based approaches rely on slow fuses, mechanical circuit breakers, or emerging solid-state circuit breakers, while power electronics–based protection, embedding protective functions within converters, remains underdeveloped. Furthermore, the low production rate of vessels and the varied power demands across applications often force designers to employ commercial off-the-shelf converters, raising challenges in modular topologies, scalability, and overall protection strategy.

This research addresses protection challenges through a multi-stage investigation into shipboard DC systems and power electronics for DC protection. First, a use case–based categorization of short-circuit events in primary DC systems is proposed. A detailed fault inventory is compiled using a reference 5 MW superyacht model, providing simulation-based short-circuit data for diverse operational scenarios. The study contributes: (1) a comprehensive short-circuit inventory, (2) a qualitative fault categorization, and (3) design recommendations for power converters in shipboard DC systems. This work emphasizes that systematic fault classification is critical to understanding the impact of different short circuits and to guiding both protective device design and regulatory evolution.

In parallel, the thesis advances the state of the art in DC fault protection hardware. A high-speed solid-state circuit breaker (SSCB) is developed, integrating a latching current limiter to prevent unnecessary tripping during transient overcurrents. Supported by a custom gate driver and controller, the SSCB prototype achieves a clearing time of approximately 200 ns, substantially reducing system stress during faults. Both SPICE simulations and experimental tests confirm its capability to properly operate under diverse fault conditions while requiring low-complexity upgrades.

Finally, a proof-of-concept DC–DC converter with embedded protection is demonstrated. The proposed protection module, based on the electronic capacitor concept,

is integrated into a 10 kW bidirectional LLC converter. Placed in series with the DC-link capacitor, the module significantly reduces processed power and conduction losses compared to conventional series-breaker configurations. Experimental validation confirms that the approach is compatible with fuse-based selectivity strategies while offering rapid fault isolation and reduced design complexity.

Collectively, this thesis provides a comprehensive framework, from system-level fault categorization to device-level protection design, supporting the safe and scalable adoption of shipboard DC systems. The proposed solutions and prototypes contribute to addressing essential protection challenges, favoring the widespread adoption of DC systems in various applications, by offering more efficient, compact, and safe DC systems, which ultimately play an important role in the transition of energy for transportation in general.

Samenvatting

De ontwikkeling van DC-voedingssystemen aan boord van schepen belooft aanzienlijke operationele en economische voordelen, maar kent grote uitdagingen op het gebied van primaire distributie, beveiliging en schaalbaarheid. Terwijl DC-technologie zich verder ontwikkelt, blijven veel aspecten van de implementatie aan boord van schepen onvoldoende gedefinieerd om zowel veiligheid als efficiëntie te garanderen. De huidige regelgeving is onvolledig en beveiligingsstrategieën zijn vaak gebaseerd op verouderde of ontoereikende kaders. Unipolaire en bipolaire busarchitecturen bieden elk applicatiespecifieke voordelen en de strategische plaatsing van vermogenselektronica opent nieuwe mogelijkheden voor gecentraliseerde en gedistribueerde schakelbordontwerpen. Beveiligingsarchitecturen kampen echter nog steeds met beperkingen. Op stroomonderbrekers gebaseerde benaderingen zijn afhankelijk van trage zekeringen, mechanische stroomonderbrekers of opkomende solid-state stroomonderbrekers. Op vermogenselektronica gebaseerde beveiliging, waarbij beveiligingsfuncties in omvormers worden ingebouwd, is nog onderontwikkeld. Bovendien dwingen de lage productiesnelheid van schepen en de uiteenlopende stroomvereisten per toepassing ontwerpers vaak om kant-en-klare omvormers te gebruiken, wat uitdagingen oplevert op het gebied van modulaire topologieën, schaalbaarheid en de algehele beveiligingsstrategie.

Dit onderzoek pakt beveiligingsuitdagingen aan door middel van een onderzoek op verschillende niveaus naar DC-systemen aan boord van schepen en vermogenselektronica voor DC-beveiliging. Ten eerste wordt een use case-gebaseerde categorisering van kortsluitingen in primaire gelijkstroomsystemen voorgesteld. Een gedetailleerde fouteninventarisatie wordt samengesteld met behulp van een referentiemodel van een superjacht van 5 MW, dat simulatiegebaseerde kortsluitgegevens voor diverse operationele scenario's levert. De studie levert de volgende bijdragen: (1) een uitgebreide kortsluitinventarisatie, (2) een kwalitatieve foutcategorisering en (3) ontwerpaanbevelingen voor vermogensomvormers in gelijkstroomsystemen aan boord van schepen. Dit werk benadrukt dat systematische foutclassificatie cruciaal is om de impact van verschillende kortsluitingen te begrijpen en om zowel het ontwerp van beveiligingsapparatuur als de evolutie van de regelgeving te sturen.

Daarnaast bevordert het proefschrift de stand van zaken op het gebied van hardware voor DC-foutbeveiliging. Er wordt een snelle solid-state circuit breaker (SSCB) ontwikkeld, die een latching current limiter integreert om onnodige uitschakeling tijdens transiënte overstromen te voorkomen. Ondersteund door een aangepaste gate driver en controller, bereikt het SSCB-prototype een uitschakeltijd van ongeveer 200 ns, wat de systeembelasting tijdens fouten aanzienlijk vermindert. Zowel

SPICE-simulaties als experimentele tests bevestigen dat de module onder diverse foutcondities goed functioneert, terwijl upgrades met lage complexiteit nodig zijn.

Ten slotte wordt een proof-of-concept DC-DC-omvormer met ingebouwde beveiliging gedemonstreerd. De voorgestelde beveiligingsmodule, gebaseerd op het elektronische condensatorconcept, is geïntegreerd in een 10 kW bidirectionele LLC-omvormer. In serie geplaatst met de DC-linkcondensator, vermindert de module het verwerkte vermogen en de geleidingsverliezen aanzienlijk in vergelijking met conventionele configuraties met serieschakelaars. Experimentele validatie bevestigt dat de aanpak compatibel is met selectiviteitsstrategieën op basis van zekeringen, terwijl het snelle foutisolatie en een verminderde ontwerpcomplexiteit biedt.

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Gecombineerd biedt dit proefschrift een uitgebreid raamwerk, van foutcategorisering op systeemniveau tot beschermingsontwerp op componentniveau, ter ondersteuning van de veilige en schaalbare implementatie van DC-systemen aan boord van schepen. De voorgestelde oplossingen en prototypes dragen bij aan het aanpakken van essentiële beveiligingsuitdagingen en bevorderen de brede acceptatie van DC-systemen in diverse toepassingen door efficiëntere, compactere en veiligere DCsystemen te bieden. Uiteindelijk spelen die een belangrijke rol in de energietransitie voor transport in het algemeen.

1

Introduction

Photo by Wesley Fernandes on Unsplash

The jaguar, roaming from the dense Amazon to the forests of Central America, is a masterful hunter, both on land and in water. More than a solitary predator, it is a keystone of balance: by regulating prey populations, it shapes the very fabric of the ecosystem, its silent steps carrying the weight of a landscape that depends on its presence.

1

Ships have played a vital role throughout human history, supporting everything from basic survival to leisure and trade [1]. To sustain these diverse activities, a wide range of vessels and technologies is required. However, many of the technologies commonly used on ships today are harmful to the environment [2]. The rapid pace of industrial and technological progress often comes at the cost of pollution and habitat destruction, key drivers of climate change. These effects endanger not only ecosystems and wildlife but also the long-term survival of humanity. Reducing the negative impact of our activities is no longer optional, it is a matter of urgency [3].

In response to the growing threat of climate change, some governments and regulatory bodies have begun enforcing policies to accelerate energy transition. One example is the European Commission's push for a 40% reduction in maritime emissions by 2030 [3]. This regulatory momentum has spurred research and development across the shipping industry, with a focus on improving emissions and sustainability, without sacrificing economic viability. In this framework, three main innovation fronts have emerged:

1. The enhancement of internal combustion engines by optimizing their operation and employing alternative fuels [4].

2. The hybridization and electrification of shipboard systems, which include the integration of new energy sources and storage solutions and the improvement of the power grid [5].

3. A generalized improvement in load efficiency (see Fig. 1.1).

This book mainly promotes the understanding and development of ship electrification, since several improvements are based on it. However, this research can be considered transversal as it influences, and it is influenced by the other fronts.

Ship electrification aims to use electricity to power as many onboard systems and services as possible. Once this transition is underway, the ship's power plant can then be decarbonized or upgraded to reduce fossil fuel consumption [6]. These upgrades typically involve replacing some or all combustion engines with energy storage systems or alternative energy sources, such as battery packs and fuel cells. Regardless of the exact configuration, electrification requires advanced onboard power grids capable of integrating a wide range of sources, loads, and support systems [7]. This work focuses on the part of the electrical system that integrates generation, storage, and key consumers such as propulsion systems and large onboard loads, commonly referred to as the *primary system*. The *secondary system* is generally described as the onboard distribution system and is usually not directly connected to large sources and loads, therefore, it is out of the scope of this thesis.

Modern shipboard systems are increasingly transitioning from legacy AC systems to DC systems. One key reason for this shift is that DC systems do not impose fixed-speed constraints on engines, allowing engines to run at optimal speeds for longer periods, improving efficiency [8]. Unlike AC systems, which operate at a set frequency (e.g., 50 Hz), DC systems deliver current directly to the load without periodic oscillations. Another advantage of DC systems is their simpler integration with modern energy storage and alternative energy sources like fuel cells, which

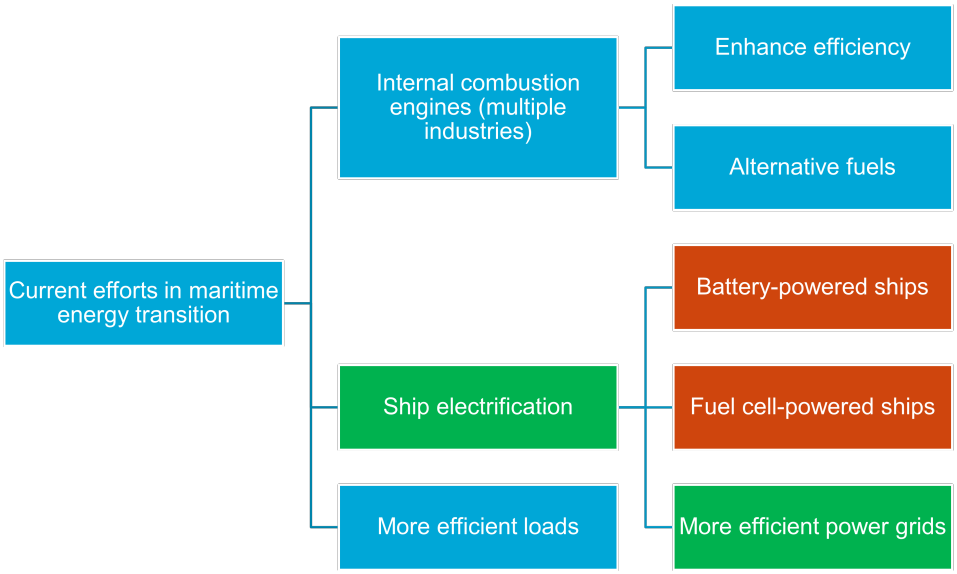

Figure 1.1: Overview of current efforts boosting energy transition in the maritime sector. *Blue:* General topics, *brown:* topics related to this research, *green:* research core topics.

typically operate within narrow voltage ranges [9]. In some cases, these can be connected directly to the DC grid. By contrast, AC systems often require additional components such as three-phase inverters, which, while robust and widely used, add complexity to the system.

Despite their advantages, DC systems are not universally applicable. Their feasibility depends on the specific vessel type (application-specific) and operational requirements [10]. For example, sea-going cargo ships have relatively small power systems because they commonly use mechanical propulsion. In this case, a highly controllable and efficient DC system is difficult to justify both technically and economically. In contrast, a battery-powered, full electric ferry can use a DC system for most of the power system, allowing for low complexity and good economics. Moreover, new challenges arise with DC implementation, particularly in areas like protection, scalability, stability, architecture, electromagnetic compatibility, and power electronics [5]. Details on these topics are covered in Chapter 2).

To better understand these challenges and expand the applicability of DC systems to various ship types, this book uses a superyacht as a case study. Superyachts are not considered sustainable and do not offer benefits to society beyond the employment of personnel for their design, construction, and maintenance. However, they have become popular development platforms for more complex ship types that actively contribute to our society. Through this lens, the book explores key technical topics such as protective devices, power electronics, and fault mechanisms in DC power systems.

Given the growing interest in DC systems for ship electrification, and the complexity they introduce, it becomes essential to identify and prioritize the most pressing challenges in order to guide meaningful research and development. Hence, the remainder of this chapter explores the identified research opportunities (Section 1.1), expanding on the problem they represent, which later produce the research questions of this work (Section 1.2) and the contributions that this thesis provides in answering the research questions (Section 1.3). The structure of the chapter, summarized in Fig. 1.2, and the context of the book were built on Chapter 2. Lastly, the book outline is summarized in Section 1.4.

1.1. Research opportunities

One of the first hurdles in advancing shipboard DC systems is determining which challenges to address first, especially given the wide-ranging and interconnected nature of the issues involved. To guide the research presented in this book, an extensive literature review was conducted (*see Chapter 2*). This review revealed a critical gap: standardized design guidelines for DC ship systems lag significantly behind what is already being implemented in advanced vessels. While this may appear to be a procedural shortfall, it actually points to a deeper issue: the lack of comprehensive technical understanding of DC systems in the maritime sector.

This gap in understanding of protection in DC systems deserves immediate attention. In response, the research outlined in this book focuses on analyzing the intrinsic behavior of DC systems with the aim of developing more effective protection solutions.

When the broader problem is broken down, three key research opportunities emerge as the foundational building blocks of this thesis.

1. **Fault identification and characterization:** There is insufficient clarity around the types, characteristics, and consequences of potential faults that shipboard DC systems must be designed to withstand.

2. **Protection device limitations:** Existing DC protection devices face significant trade-offs in terms of efficiency, performance, market availability, and cost, all of which restrict their practical deployment.

3. **Converter oversizing and vulnerability:** The power electronics (converters) used to interface energy sources and loads in primary DC systems are often oversized to meet design margins, resulting in chronically underutilized components. Furthermore, they are not equipped to protect themselves from short circuits, which can motivate further oversizing.

These blocks lead to research questions and a research objective, detailed in Section 1.2, and to research contributions, summarized in Section 1.3, as illustrated in Fig. 1.2. The background and context of these three problem areas are detailed in the following subsections.

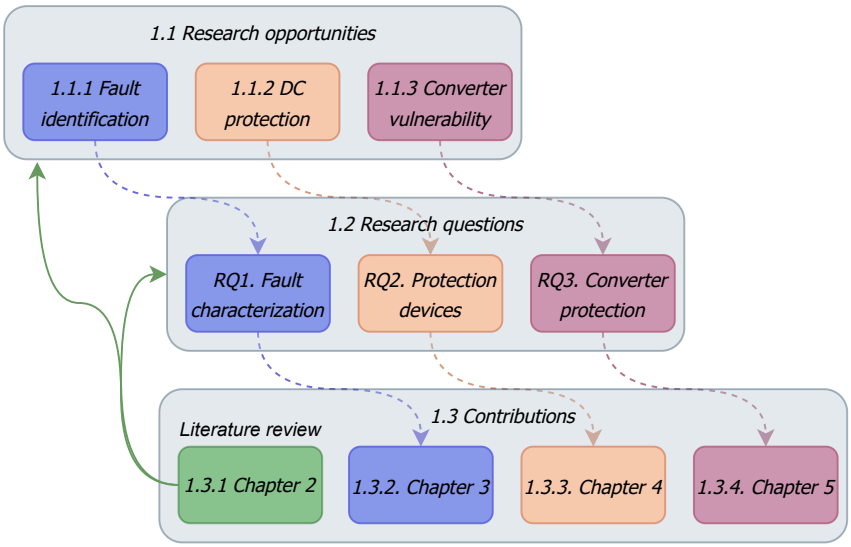

Figure 1.2: Structure of the research opportunities 1.1, the research questions 1.2 and the contributions 1.3, of this thesis. *Chapter 2* is the platform of the complete work.

1.1.1. Fault identification and characterization

To understand the risks and behavior of shipboard DC systems, it is essential to examine how faults, especially short circuits, manifest in these environments. In both AC and DC circuit analysis, faults are generally categorized into two types: open circuit faults and short circuit faults.

An open circuit occurs when part of the electrical path is suddenly disconnected, interrupting the current flow. This can destabilize the system, potentially shutting down other loads or subsystems. A short circuit, on the other hand, behaves like a highly conductive connection between two circuit nodes. It effectively creates an unintended low-resistance path that diverts a large portion of the system's available power to the short circuit location. This concentrated energy transfer can overheat components and lead to severe damage, particularly in DC systems.

Shipboard DC systems are relatively complex systems that could be simplified as in the circuits depicted in Fig. 1.3. Generators, converters, passive components, cables and switches are fundamental components in a generic DC system. Figure 1.3 includes short-term energy storage elements, such as capacitors, commonly used to minimize voltage ripple and support stable dynamic performance. These capacitors, often referred to as DC-link or DC bus capacitors, help maintain voltage stability by releasing energy rapidly during transients and recharging in a controlled cycle. From a design perspective, larger capacitors are often favored to achieve better voltage ripple attenuation.

Two key parameters govern the behavior of a short circuit in a DC system, the

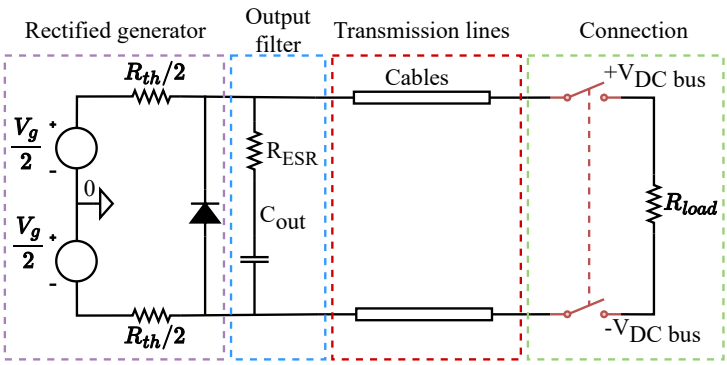

Figure 1.3: Simplification of the feeder of a shipboard DC system.

stored energy and the time constant. The energy in a capacitor E_{cap} depends on its capacitance C (component-related) and the square of the voltage V (system-related) (1.1).

$$E_{\text{cap}} = \frac{1}{2}\text{C}V^2 \tag{1.1}$$

The time constant τ indicates roughly how quickly the capacitor can partially charge or discharge depending on the circuit resistance R (system-related) and the capacitance C (component-related) (1.2).

$$\tau = R\text{C} \tag{1.2}$$

In the event of a short circuit, the system resistance R drops drastically, from several ohms to just a few microohms, resulting in a very short time constant τ. This rapid transition causes the capacitor to release a significant portion of its stored energy E_{cap} into the fault location almost instantaneously.

As a result, a short circuit in a DC system can release tens of kilojoules of energy within microseconds, creating intense thermal and electrical stress that may severely damage or destroy nearby components. Understanding this behavior is crucial for designing reliable protection systems and ensuring the safe operation of modern, more electric vessels.

The problem

Although the complexity of shipboard DC systems is widely acknowledged, the lack of a unified framework for protection performance means short circuit studies are often missing or undisclosed. As a result, manufacturers and stakeholders develop independent solutions aligned with their own interests and specific solutions. This leads to inconsistencies across the industry and leaves key concepts unaddressed or undisclosed. Short circuit calculation and propagation studies are necessary to understand onboard fault behavior. They can then support hardware development and help identify critical components and procedures.

1.1.2. Protection device limitations

Given the unique characteristics of DC systems and their lack of zero-crossings, their protection technologies have evolved differently from legacy AC approaches. Traditional AC protection relies on current zero-crossings to achieve arc-free protection using reclosers, relays, fuses, and mechanical circuit breakers, two of which (fuses and breakers) have been adapted for DC applications and are now standard in shipboard DC systems. However, these devices have significant performance limitations, exacerbated by the absence of zero-crossing in DC systems. Fuses require relatively long melting times and can only be used once. Similarly, mechanical circuit breakers adapted for DC systems are slow to respond, which limits their effectiveness in fast fault scenarios.

To overcome these time limitations, some hardware designers have developed solid-state circuit breakers. These semiconductor-based devices operate without moving parts and are controlled by small currents, allowing much faster response times. Solid-state circuit breakers offer arc-free, enhanced protection performance for DC systems and can be scaled to handle high current levels.

The problem

The trade-off with solid-state circuit breakers lies in efficiency and power density. Unlike mechanical breakers that use efficient metallic conductors, solid-state counterpart rely on semiconductors, which inherently have higher conduction losses. This often makes them less attractive for applications where efficiency is critical. Additionally, they require supporting components, such as gate drivers, forced cooling, and embedded controllers, that add size, weight, and cost. As a result, solid-state circuit breakers remain expensive, are produced by a limited number of manufacturers, and are typically used only in high-end or tightly regulated vessels where protection performance outweighs cost.

Compounding the issue is a common misconception: solid-state circuit breakers are often designed as simple replacements for AC circuit breakers. This overlooks their full potential, making them generally underutilized. Unlike mechanical switches, semiconductors can enable advanced protection functions, such as current limiting, voltage balancing, and improved fault selectivity. Unlocking and demonstrating these features could improve their cost-effectiveness, making SSCBs viable for broader use and encouraging more suppliers to enter the market.

1.1.3. Converter oversizing and vulnerability

DC power systems depend on power converters to regulate the energy flow between sources and loads. These converters must meet strict design criteria, as maritime regulations demand high power availability even under adverse conditions. However, due to the high cost of design and certification, manufacturers often pursue broadly certifiable multipurpose solutions that maximize profitability.

The problem

As a result, the final products are often suboptimal for maritime use and frequently underutilized. Moreover, many commercial converters lack built-in short-circuit protection and reconfiguration capabilities, limiting their fault tolerance.

From a research standpoint, power electronics-based protection is perceived as costly and low-performing, though current empirical support for these claims is limited. Terminology also adds confusion, "power electronics-based protection" is often used interchangeably with "breakerless protection", despite important differences. Power electronics-based protection implies that the protection functionality relies mainly on the power converter and does not necessarily require the removal of the circuit breaker. In contrast, breakerless counterparts make this requirement explicit. Although breakerless strategies can address certain fault types, they are generally ineffective against short circuits.

To overcome these limitations, modern protection schemes that extend converter topologies to embed the protection components are needed. These could improve not only system protection but also power density and overall efficiency, simplifying system design and enhancing reliability.

1.2. Objective and research questions

Building on the aforementioned challenges and opportunities in DC protection technologies, the main objective of this work is:

- *To enhance protection effectiveness of shipboard DC systems by improving the capabilities of circuit breakers and DC-DC converters.*

This research goal is achieved by addressing the identified research opportunities, which come together like pieces of a puzzle. These opportunities then translate into specific research objectives, each forming a part of the overarching research aim. The storyline of this research is illustrated in Fig. 1.4.

Each objective is presented as a research question, and from each of these questions, several sub-questions arise. Answering these sub-questions will help accomplish the main objective. The remainder of this section introduces the primary research questions along with brief explanations of their requirements, studies, and anticipated outcomes.

RQ1: *What are the characteristics of short circuits in shipboard DC systems?* A simplification of the procedure is shown in Fig. 1.5, with the following subsequent questions.

- Which system configurations could be used to represent state-of-the-art DC ships?
- How can faults be categorized based on their relative impact on the system?
- Which components or sub-components require protection based on fault severity?

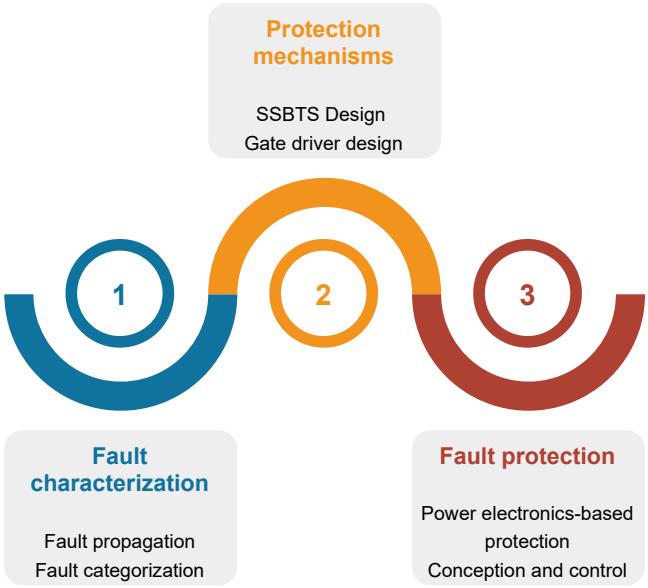

Figure 1.4: Overview of specific research objectives

- What type of short circuit should guide the protection design?

RQ2: *How can the protection functionalities of existing solid-state circuit breaker technologies be enhanced for maritime applications?* Just as in the previous case, Fig. 1.6 summarizes the procedure and its outcome, and the following sub-questions are considered.

- Which circuit breaker topologies are most convenient for state-of-the-art primary shipboard DC systems?
- What protection functionalities can enhance selectivity in shipboard DC systems?
- How can additional protection functionalities be integrated into existing circuit breaker products?
- How can a solid-state circuit breaker be designed to incorporate additional features for better protection performance?

RQ3: *How can the protection capabilities of power converters in a shipboard DC grid be enhanced using power electronics-based protection technology?* The summarized procedure is depicted in Fig. 1.7, and the following sub-questions are part of the research.

- What protection mechanisms should power converters have to withstand short circuits?

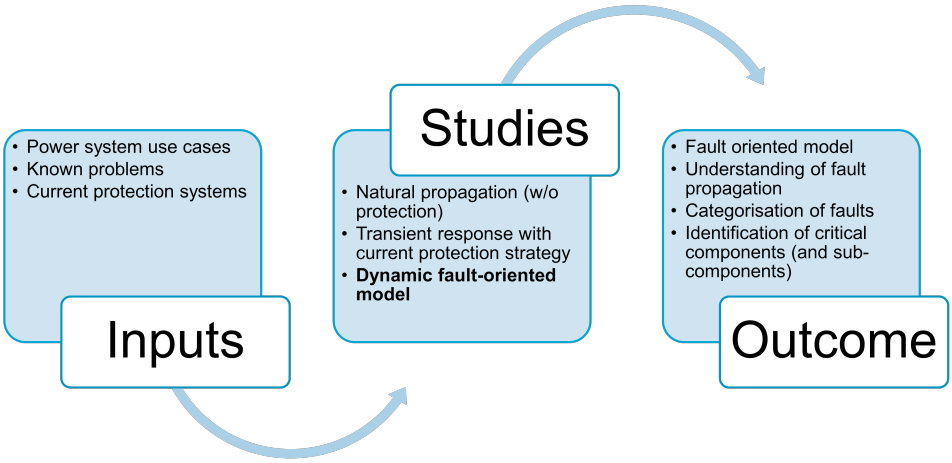

Figure 1.5: Overview of requirements, studies and outcome for RQ1: *What are the characteristics of short circuits in shipboard DC systems?*

- How can protection functionalities be integrated into power converter topologies?
- How can efficency be enhanced in a power converter with solid-state protection?
- How can DC protection be integrated into a DC-DC power converter?

1.3. Contributions

The execution of the proposed research objectives has led to a set of concrete contributions, each mapped to the chapters of this book. This section summarizes the main contributions of this work to improve state-of-the-art shipboard DC protection.

1. **Chapter 2:** Establishes a strong technical foundation to enhance shipboard DC systems, highlighting how converter placement affects system weight, exposing limitations in marine-approved DC protection, and promoting Power Electronics Building Blocks for greater modularity and scalability. Published in [11].
2. **Chapter 3:** Proposes a severity-based fault categorization for shipboard DC systems, supported by transient short circuit analysis and highlighting the critical impact of cabling inductance on fault severity. Published in [12].
3. **Chapter 4:** Demonstrates that solid-state circuit breakers can do much more than mimic AC breakers. Minor enhancements to the controller and gate driver enable advanced protection features, such as integrated current limiting and

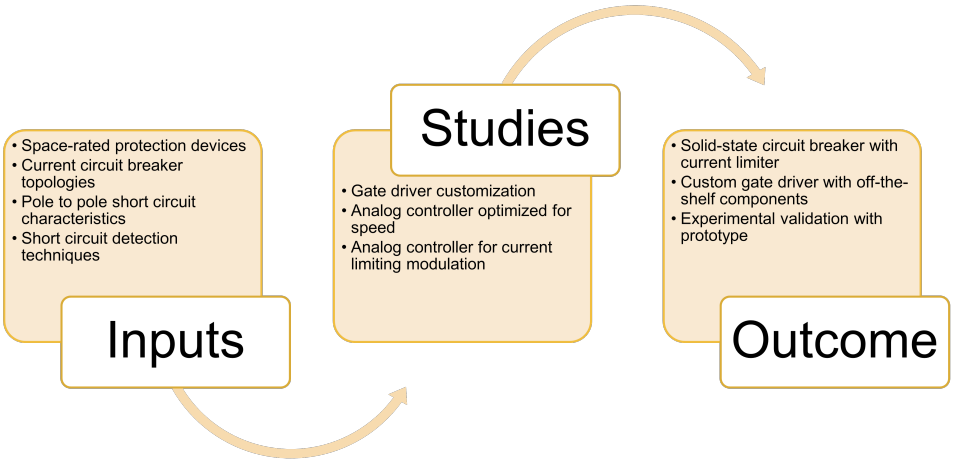

Figure 1.6: Overview of requirements, studies and outcome for RQ2: *How to enhance the protection functionalities of existing solid-state circuit breaker technologies in maritime applications?*

improved selectivity, offering an innovative approach to handling DC short circuits. Submitted for publication in [13].

4. **Chapter 5:** Extends the concept of power electronics-based protection by integrating it into the converter topology via an electronic capacitor, reducing the power processed by the protection system by over 80% compared to conventional designs with series-connected solid-state circuit breakers. Submitted for publication in [14].

1.4. Outline

The contributions presented in the previous section are the result of a structured research journey which unfolds in the chapters of this thesis. To help the reader navigate through the proposed ideas, this section outlines the content and purpose of each chapter, illustrating how they collectively address the challenges identified in this introduction.

The thesis is organized into six chapters, as summarized in Fig. 1.8. Each chapter is designed as a standalone and offers the necessary context and background to support its findings. Therefore, there might be some overlap in the background section among the different chapters.

- Chapter 1 (cyan) is this introduction, summarizing the context, research opportunities, questions, and main contributions of the work.
- Chapter 2 (green) delivers a critical overview of shipboard DC systems, with a focus on challenges in primary distribution, protection technologies, and

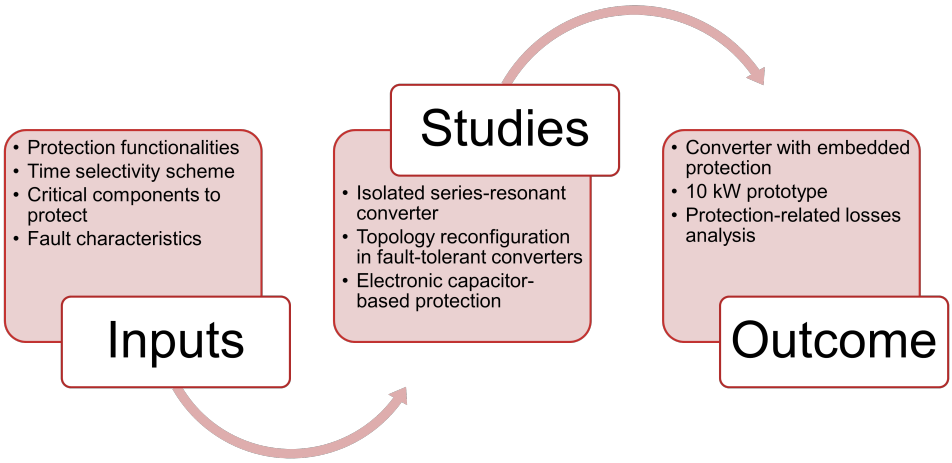

Figure 1.7: Overview of requirements, studies and outcome for RQ3: *How to enhance the protection capabilities of power converters in a shipboard DC grid, derived from the power electronics-based protection technology?*

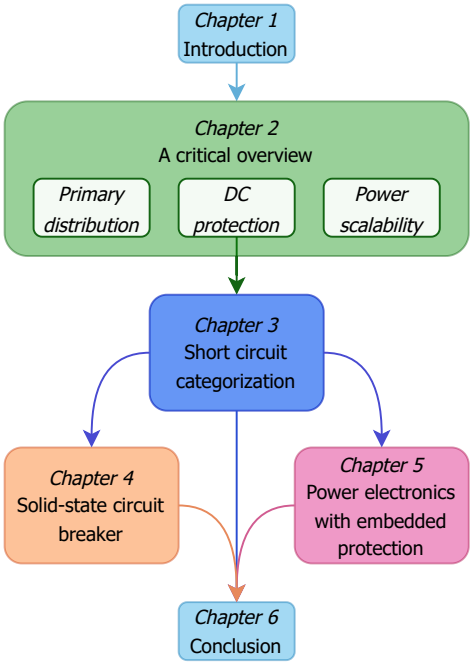

Figure 1.8: Outline of the book: definition of the chapters and their connections.

system scalability. It also highlights the motivation for transitioning toward

Power Electronics Building Blocks.

- Chapter 3 (blue) analyzes the transient behavior of pole-to-pole short circuits in a referential shipboard DC system. It introduces a fault severity categorization and examines how existing protection components influence fault dynamics.
- Chapter 4 (orange) presents the design and validation of an advanced solid-state circuit breaker featuring a current-limiting function. The chapter demonstrates how a dedicated controller and modified gate driver enable significant gains in protection performance and selectivity. This performance is demonstrated in a solid-state circuit breaker prototype that uses off-the-shelf components only.
- Chapter 5 (fuchsia) briefly describes the fundamentals of the electronic capacitor that, combined with the solid-state circuit breaker controller, comprises the protection module. The protection operation is validated in a prototype of a fault-tolerant bidirectional series resonant converter.
- Finally, Chapter 6 (cyan) includes the conclusion of this research, which addresses identified societal and technical problems and answers the research questions.

2

Shipboard DC systems, a Critical Overview: Challenges in Primary Distribution, Power Electronics-based Protection, and Power Scalability

This chapter gives an overview of challenges in primary distribution, protection and power scalability for shipboard DC systems. Given that DC technology is in development, several aspects of shipboard systems have not yet been sufficiently devised to ensure the protection and efficiency demanded. Several issues in DC systems arise from the lack of complete relevant standardization from different regulation bodies. Unipolar and bipolar bus architectures have application-specific advantages that are discussed and compared. The placement of power electronics in DC systems creates opportunities for switchboard design, and this chapter compares the centralized and distributed approaches. Likewise, protection architectures for shipboard DC systems have challenges. Breaker-based protection utilize slow fuses, mechanical circuit breakers, and solid-state circuit breakers.

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2

In addition, power electronics-based protection embeds the protective circuit in the power converters, but its development lags. This chapter compares the state of the art technologies, reviewing their main features. Finally, the power requirement of various applications and the low production rate of vessels force the designers to utilize commercial off-the-shelf converters to scale up power. The misuse of such converters, the modular topologies and power electronics building blocks are exposed highlighting challenges and opportunities towards the mass adoption of DC systems onboard maritime vessels.

Photos by Jelle de Gier, William Warby, Juan Manuel Núñez Méndez and Michael Steinman on Unsplash

In the vibrant understory of Colombian rainforests, frogs appear in a dazzling mosaic of colors and patterns, a testament to the rainforest's unparalleled diversity. The Amazon harbors the largest frog biodiversity in the world, and though these tiny creatures are small, they play a vital role in controlling insects and signaling the health of the ecosystem, each species a vivid thread in the complex tapestry of life.

2.1. Background

Climate change is propelling humanity to reshape the shipping industry towards more sustainable operations and fewer emissions. Maritime transportation is responsible for 3.1% of total CO_2 emissions [6, 15], and the estimations show a rising of 12-18% of total CO_2 emissions by 2050 if no effective countermeasures are enforced [7], thus projecting a pessimistic outlook for the future. As a reaction, the European Commission is implementing a CO_2 emissions reduction policy of at least 40% by 2030 for the sector, boosting the energy transition actions in the continent [3]. This energy transition is fundamental to achieving the carbon reduction objectives in an industry heavily dependent on fossil fuels and low-efficiency engines, as low as 42% at nominal load and 20% at low load regime [16]. Hence, the research and development efforts are focused on three main areas.

1. Internal combustion engine (ICE) modifications for enhanced efficiency and fuel flexibility [6].
2. System hybridization and alternative power supplies, such as fuel cells and storage systems [7].
3. Integrated power systems development [9, 17].

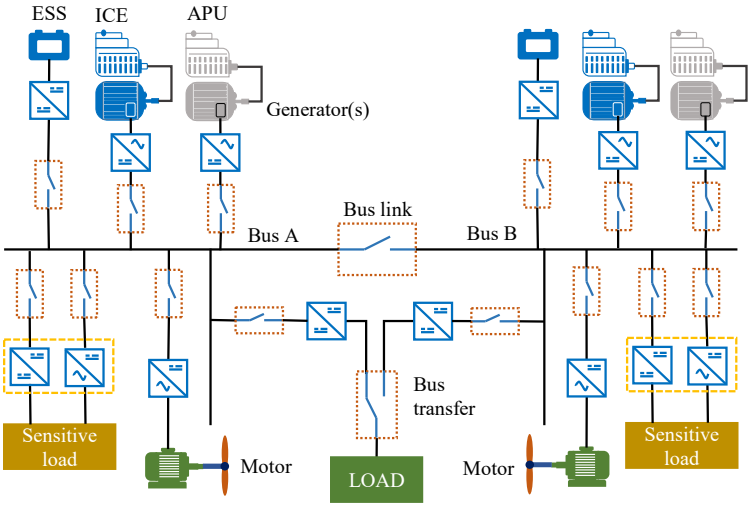
The latter is based on ship electrification to merge the power train (propulsion, power plant, power system and loads) into a single system based on electrical or hybrid propulsion [5].

The motivation to opt for electric propulsion instead of mechanical propulsion lies in several advantages as follows. In electrical propulsion, ICEs can be used frequently at rated power, reducing off-design load efficiency drops that affect mechanical drives [17]. The engines generate electricity only, allowing fuel-efficient and flexible operation with lower emissions [7]. Electrical propulsion is more efficient at low speeds and for highly variable load profiles vessels than mechanical propulsion, enabled by variable speed drives [10]. A multi-engine centralized power system has high availability and survivability. A single ICE failure has a reduced impact on the operation [18]. However, the convenience of adopting electric propulsion is normally application specific, e.g., a cargo ship could not benefit from electric propulsion as the electric motors currently do not match the cruising speed from ICEs, whereas a cruise ship get substantial benefit given that their operation focus on consumption at lower speeds [5].

Nevertheless, electrical propulsion is the most suitable option for the integrated power system. The integrated approach enables global optimization of the system for more cost-effective operation, refreshing the interest in efficient onboard power systems development in which DC distribution is considered the backbone for future vessel electrification [5].

Figure 2.1b shows a simplified representation of a generic shipboard DC integrated power system. The system has a dual DC bus configuration with a main ICE, an ESS and an auxiliary power unit (APU) attached to the loads. The illustration features electrical propulsion only. However, the concepts discussed in this chapter are also compatible with hybrid propulsion drives. Shipboard DC systems are

(a)



(b)

Figure 2.1: Referential case study for shipboard DC systems. (a) Moonrise superyacht manufactured by Feadship in 2022. Credit to Feadship [online] https://www.feadship.nl/ (b) Referential shipboard DC integrated power system with electrical propulsion, suitable for the superyacht. *Dots: DC switches*.

flexible, scalable, controllable, have increased volumetric power density, and have simpler energy storage systems (ESS) integration compared to AC systems [19–

22]. Synchronization requirements and speed restrictions from AC technology are no longer necessary, allowing optimal design and operation of ICEs and generators [5, 23, 24]. In addition, the shipboard system scalability can simplify the redundancy scheme and increase the reliability onboard, potentially enhancing survivability and reducing maintenance requirements [23]. Although these advantages are valuable for the shipping industry and the emission reduction objectives, the extent of such benefits is application-specific, and new challenges are arising from the DC technology. These are frequently related to protection, scalability, control, stability, distribution and power electronics, highlighting the importance of current development efforts.

The DC protection systems required a redesign from the AC technology, and multiple works as [25–30], show progress on the matter, frequently focusing on grounding schemes, protection devices and reconfiguration. Some shipboard DC systems scalability challenges are discussed in [28, 31–34], where the research is usually focused on power modules, modular multi-level converters (MMC) and power electronics building blocks (PEBB) to scale up power and voltage levels in different vessels. Control strategies and architectures are investigated in [25, 30, 35], proposing a similar hierarchical control approach from the AC case for the general control architecture, droop controllers on the primary level, centralized, decentralized, and distributed controllers for the secondary level, and energy management placed at the tertiary control level. Some stability issues for shipboard applications and land DC microgrids are discussed in[18, 25, 27, 35], covering voltage stability problems, pulsed and constant load limitations and stability enhancement methods. Multiple scholars are also working on distribution architectures, giving special attention to grid reconfiguration and zonal distribution [8, 19, 27, 30]. Finally, the work on power electronics for shipboard DC systems is gaining popularity, where the discussion focuses on converter topologies for generation, propulsion, loads and modular converters [8, 28, 31, 32].

Despite the extensive effort placed on the DC systems investigation, multiple research opportunities require attention to support the development. This review explores challenges regarding primary distribution, protection devices, and power scalability that are not entirely covered in previous works available in the literature and are paramount for massive technology adoption. Addressing the subsequent matters does not disregard the existence of other relevant topics, such as stability, electromagnetic interference, and quality of service, investigated by various scholars. The three key challenges are the following.

1. Shipboard DC systems lack a common framework to guarantee a suitable protection performance from the primary distribution and the protection coordination.

2. The Breaker-based protection commonly used in shipboard DC systems utilizes DC breakers based on AC breakers that have limited performance and compromised protection requirements.

3. Ship manufacturers rely on commercial off-the-shelf (COTS) converters to reach the power level requirements of the system.

First, considering that DC systems are emerging for shipboard applications, gradual evolution of rules and regulations is expected, and some scholars are discussing the standardization issues [19, 27, 36]. However, ship design includes an extensive decision-making process involving variables that can affect the protection performance and the volumetric power density. As the regulation is still evolving, the baseline for protection and coordination is missing, allowing ship designers to prioritize other variables. The effect of such decisions is uncertain given that some of the studies required to obtain the information are not defined completely. This chapter explores some of the issues inherited from the emerging condition of DC systems from the protection perspective.

1. A possible standardization delay that could facilitate undesirable behavior in the event of faults.

2. The bus architectures available and their main characteristics and protection approach.

3. The placing of power converters considering general characteristics, and a superyacht as illustrative use case comparing the centralized and distributed approaches.

Second, DC systems have two characteristics that constrain the applicability of protection measures from AC: 1) DC systems lack the natural zero-crossing of the current and the inverse impedance of AC [37]. 2) DC systems are based on power converters that utilize filtering components that remain charged [5]. As the AC circuit breakers rely on the zero-crossing to separate the contacts, they are ineffective for DC applications. Passive components can store a non-negligible amount of energy capable of quickly feeding a short circuit fault [5]. Therefore, scholars developed DC protection based on solid-state switches, mechanical and hybrid DC circuit breakers, high-speed fuses, and control actions for an integral protection system [29]. Despite some performance limitations, this protection approach is widely accepted and has allowed a relatively established market for DC circuit breakers. However, such shortcomings frequently involve time response, efficiency and size, especially for MVDC applications and more suitable solutions are needed [5, 25, 26]. To contribute in the development of shipboard DC protection systems, this chapter investigates the breaker-based and the power electronics-based protection. The study includes the protection mechanisms, their operation principle, a survey of marine certified products, and the development of SSCB considering arising challenges, and a down scaled SSCB prototype to study a breaker control strategy.

Finally, COTS converters allow building block utilization during system design, which is desirable to simplify the process and cut design costs while obtaining reliable operation and robust components. Nevertheless, the COTS converter components are unknown and often require characterization for proper controller design, energy management, and certification [38–40]. These parts are not necessarily designed for shipboard applications nor tailored for the specific vessel. Hence, the

misuse and excessive oversizing of components are frequent, compromising the volumetric power density, the overall efficiency and limiting the power scalability.

This work provides a simplified comparison among modular power converters for shipboard DC systems for various purposes within the vessel. The comparison allows a high level comparison that can partially justify the deployment of building blocks for certain applications. In addition, this chapter points out the design obstacles of PEBBs, where the thermal management can become challenging especially in a distributed switchboard.

This chapter presents an overview of the causes and consequences of each challenge and highlights the fundamental gaps to address, contributing to the shipboard DC systems development, all from a critical perspective. Section 2.2 describes the main DC primary distribution challenges. Section 2.3 presents the main DC protection technologies. Section 2.4 introduces power scalability for DC ships. Finally, Section 2.5 summarizes the conclusion of the chapter.

2.2. Primary Distribution in Shipboard DC systems

Shipboard DC distribution is an emerging technology and despite the existence of IEEE, IEC and NPR standards applicable to the industry, the rules and regulations have not reached the required maturity [8]. Furthermore, a methodology for the decision-making process during design is not yet complete because the knowledge from AC grids is not directly applicable in DC.

This section shows an overview of the standardization issues in shipboard DC systems, the DC bus architecture options and challenges, converter placing, and compares the centralized and distributes switchboard in a realistic use case. The section highlights the challenges to overcome in the widespread of DC systems onboard.

In addition, notwithstanding the research popularity of zonal architecture, their industrial adoption is delayed. A system with zonal configuration is complex and requires a complex control architecture and a high number of circuit breakers and disconnectors. Most of the current systems are demonstrators, whereas the research frequently relies on notional models [8, 18]. Furthermore, the ring architecture is occasionally used in sensitive applications, such as offshore supply vessels and drillers [25]. An additional bus-tie switch operates as redundancy in a dual-bus architecture, but some cases could feature more. Considering the tendency to retrofit vessels using radial architecture as in [41], and the aforementioned arguments, the analysis in the current section studies the radial architecture only.

2.2.1. Standardization

The IEEE std. 1709-2018 [42] is a set of recommendations that proposes a zonal distribution architecture as the best practice while ignoring the converter placement and overlooking the protection requirements. The IEC 63108 is limited to a selection of brief definitions for primary DC distribution and control systems that require

further information [43]. The IEEE std. 45 series [44, 45], the US standard for shipboard system design, does not cover DC systems. The NPR-9090 [46] focuses on residential applications, limited in the approach of protection, power levels and architecture. However, it is the completest framework for system design applicable in the European Union. Consequently, the rules and regulations for shipboard DC systems require further investigation to incorporate newer technologies.

DC protection architectures

Not all sections of a power system require the same level of protection. Critical parts of the system (e.g., propulsion system) need special protection measures, while non-fundamental load or low-power equipment require much less sensitive protection. From this, an upgrade of the NPR-9090 to onboard DC grids is a practical solution and a missing requirement for the DC system design in LVDC systems. A complete framework is required, similar to the proposed case in [47] for residential LVDC grids, where protection zones and frontiers are well-defined and have specific requirements. For shipboard MVDC systems, the situation is more complicated, IEEE Std. 1709-2018 does not include a well-defined protection structure, and the IEEE Std. 45 series barely mentions voltage classes in IEEE std. 45.1-2017 [44]. DC systems are completely disregarded by IEEE std. 45.5-2014 [45], which is intended for safety considerations in shipboard power systems.

As a result, designers and manufacturers rely on the experience from AC systems during grid design, which can originate various unidentified limitations. Some of the necessary studies for the identification of limitations are also missing, thus restricting the possibility of providing best practices from standardization bodies. Scholars are showing multiple studies to overcome the shortcomings, allowing regulators to expand the knowledge and recommendations about bus architectures and converter placing. However, studies about fault-propagation, essential in DC protection development, are scarce in the literature.

2.2.2. Bus architecture

In the current standard of AC distribution, most of the distribution utilizes three-phase systems, and only the low power loads are single phase. In contrast, DC distribution can feature unipolar or bipolar arrays, and both architectures can provide full power to the loads and propulsion, as depicted in Fig. 2.2.

The voltage levels in DC systems are more flexible than AC cases. Hence, the selection of the voltage class is essential for the performance. An increased voltage level facilitates higher power capabilities, smaller cabling cross-section and lower losses for the same power level. However, medium voltage classes require additional certifications from designers and certification entities given the increased insulation and safety concerns. Furthermore, a higher voltage gain ratio in the power converters might need modular power converters in parallel and/or series connections to match the requirements [5, 27]. In addition, utilizing low voltage levels for the same power can decrease the complexity of power converters. The

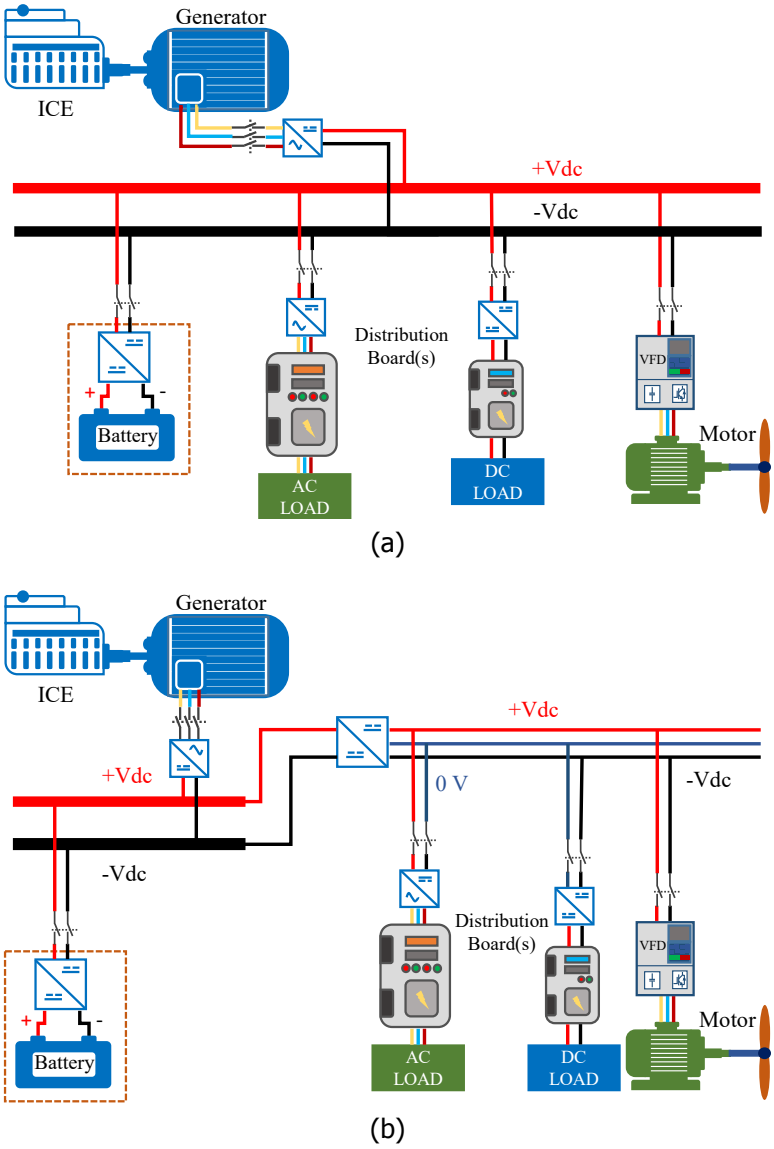


Figure 2.2: Unipolar and bipolar bus architectures for onboard DC systems. (a) Unipolar DC system, reported for various applications, such as superyachts and cable layers. (b) Bipolar DC system, recommended in the IEEE std. 1709-2018 for high survivability. *Dash: optional*.

semiconductor variety and availability improves in lower voltages, allowing the usage of more efficient modules. The usage of parallel power converters is relatively simple to achieve to cope with the higher current needs in low voltage [5, 27].

Consequently, the availability of distinct bus architectures makes more challenging the decision-making process. The unipolar and the bipolar bus architectures are the most frequently mentioned in shipboard DC grids and are affected in a different way by the previously mentioned arguments. This section discusses the benefits and challenges of both choices, including the protection approach and a simplified comparison.

Unipolar bus

The unipolar DC system uses only two conductors for distribution. The sources and loads are connected to a single level of DC using the positive (+Vdc) and negative (-Vdc) ports of the bus [8], as shown Fig. 2.2a. These systems are simple to implement and maintain, and the cabling load is balanced. However, the single voltage system reduces flexibility, and no backup power line is available in case of a fault [8, 27].

Bipolar bus

The bipolar bus architecture, also known as the three-wire DC bus system, utilizes one additional conductor as the "neutral" (0 V), as shown in Fig. 2.2b. The additional conductor creates two complementary power lines with two voltage levels in the same bus. The efficiency improves because the return wire reduces the current carried by the pole wires. Thus bipolar systems can supply higher power than unipolar systems, and the positive and negative buses can operate independently, increasing flexibility and reliability [8, 27, 30]. Furthermore, bipolar DC systems may require a voltage balance circuit to avoid stability and efficiency issues created during voltage unbalance scenarios. This circuit also requires a well-tuned control system to operate properly, which can also include a complex control strategy [8, 24, 27, 30, 48].

Protection approach

Table 2.1 summarizes the main differences between the two bus architectures discussed. This overview suggests that the protection approach shall be different in both cases. For instance, the voltage balance power converter can become a critical component to protect from a short circuit. Moreover, the available grounding scheme regulation for bipolar systems is best introduced in IEEE 1709-2018 [42]. Nevertheless, the fuse is an essential protection component [49], regardless of the bus architecture or whether the system is AC or DC, and despite their limited time response. Extensive research is required to provide an alternative solution to the fuses, protection systems for unipolar and bipolar systems and the grounding scheme for each case.

2.2.3. Power converters placing

As there is no consensus about the physical location of the power converters, the stakeholders have proposed different approaches. Depending on the application

Table 2.1: Bus architecture comparison for unipolar and bipolar DC systems.

Unipolar	**Bipolar**
• Simple to design and deploy	• Design based on balancing the load between the poles
• Based on two conductors	• Based on three conductors and a voltage balancer
• Can become vulnerable when a fault occurs	• Fault-tolerant, losing one pole does not mean losing the bus
• Preferred for most applications	• Preferred for warships considering the increased survivability
• Controlled by the converter of the main power supply	• Require an additional voltage balancer for stable and efficient operation
• Better controllability and limited reconfiguration options	• Enhanced reliability and reconfiguration options.

and the manufacturer, two general dispositions are frequently used. The converter disposition close to generators and loads and the placement embedded into the switchboard are designated distributed and centralized approaches, respectively [23, 41]. In the vessels from Wärtsilä, different placings are available [50]. The disposition and integration of frequency drives, switchboards and energy storage vary significantly according to the application.

Centralized

The centralized or multidrive approach shares qualities with a generic AC switchboard. Converter modules are placed within the same space as the protection, control and connection devices [41], as illustrated in Fig. 2.3.

The switchboard contains all the components framed by the dashed red rectangle in Fig. 2.3. The power distribution is then centralized, or pseudo-centralized, from the switchboard to the load, requiring extensive AC cabling in the vessel.

Distributed

For this case, as the name suggests, the power conversion stages are placed as near as possible to the load or the generator and away from the switchboard, as shown in Fig. 2.4.

The generated power can be fed directly to the DC bus for distribution from the rectified AC generator or the DC storage. The main load supply utilizes dedicated inverters (DC-AC converters) and DC-DC converters, and normal AC distribution requires island converters [41]. Such a configuration can significantly reduce the AC cabling for the bus circuits compared with the centralized placing.

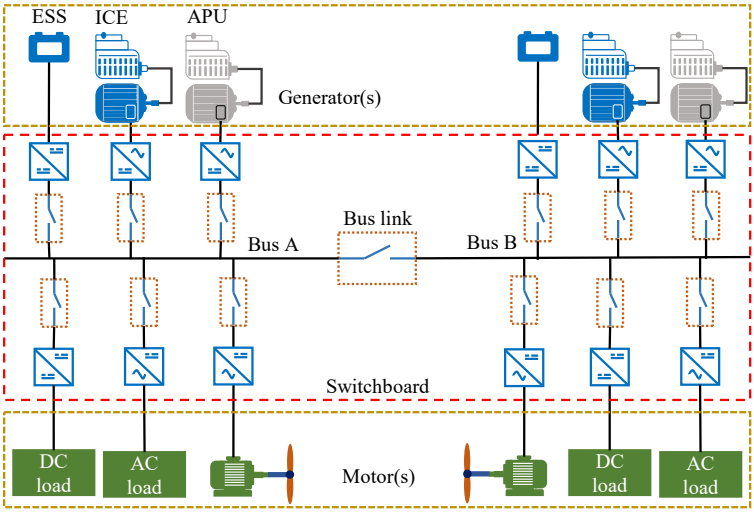


Figure 2.3: Centralized disposition of conversion stages for onboard DC systems. *Dots: DC switches, red dash: switchboard components normally placed close together, dark yellow dash: components normally placed away from the switchboard.*

Other physical dispositions

The centralized and distributed dispositions are the extreme cases where the components are contained within the same space or placed all over the ship. However, the DC systems enable mixed dispositions without matching the previous cases [8, 50], including the complete removal of the switchboard. The advantages need identification in any case and specify the disposition according to the requirements at the design level.

Table 2.2 shows a simplified comparison between the centralized and distributed placing. In the case of the switchboard-less approach, the empirical information is limited, and the implications are mostly conjectures that require further studies.

2.2.4. Switchboard approach comparison in a Superyacht

A primary switchboard cabling estimation is valuable to quantify the centralized and distributed approach differences. The system of a Superyacht (see Fig. 2.1a) allows an estimation considering a multi-megawatt calculation with relative complexity. Hence, an inference about various seagoing vessels is possible based on the current use case. The operation modes, existence of multiple generators, variable loads and electrical propulsion enable the comparison at certain extent. The DC primary switchboard features a twin system with one main diesel generator, one secondary diesel generator, one ESS, one main propulsor, and AC loads on each side *(see Figs. 2.3 and 2.4)*. An additional bow thruster is attached to one side of the switchboard, which is mainly required for maneuvering.

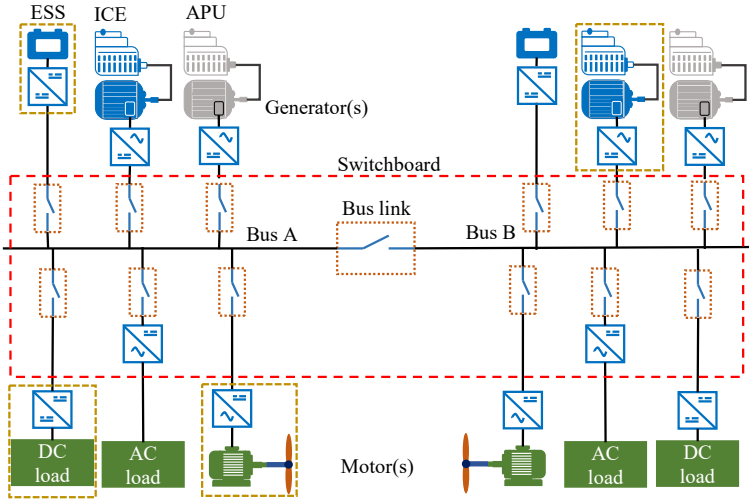


Figure 2.4: Distributed disposition of conversion stages for onboard DC systems. *Dots: DC switches, red dash: switchboard components normally placed close together, dark yellow dash: components normally placed close to their respective drives and far from the switchboard.*

Table 2.2: Switchboard approach comparison for shipboard DC systems.

Centralized	**Distributed**
• Power converters and systems are close to each other	• Power converters are close to generators and loads
• Require extensive use of AC cabling	• DC cabling is extended as close to the load as possible
• Communications and instrumentation are closely connected and centralized	• Communications and instrumentation are centralized in the switchboard and distributed in the system
• Extended VFD cables increase the losses and EMI	• Short VFD cables reduce the conduction losses and localize the EMI
• Baseline of the system volume	• A considerable volume reduction is possible

The parameters of the real system are implicit for confidentiality purposes. Some referential values provide sufficient information for the comparison. The main generators have 30% more power than the secondary diesel generators, and the thruster has 15% of the power of the main propulsors. As the switchboard is DC, the cabling of the ESS remains unchanged in the two approaches, their influence is disregarded. The voltage level of the AC components is 600 V (except for the bow thruster, which is 360 V), and the voltage level of the DC bus and the

DC components is 1000 V. The generators and the motors are 64 m away from the switchboard, and the minimum cabling cross-section is calculated using (2.1) and (2.2), as recommended in [51]. The cabling selection uses the power and control marine cables from the Prysmian Group [52], where the inner grid necessary current rating is the defining factor for selecting the number of parallel off-shelf cables.

$$A_{cs_{DC}} = \frac{LI\rho}{\Delta V} \tag{2.1}$$

$$A_{cs_{AC}} = \frac{\sqrt{3}LI\cos\varphi\rho}{\Delta V - \sqrt{3}\cdot 10^{-3}\,\frac{x}{c}LI\sin\varphi} \tag{2.2}$$

where L is the cable length, I is the nominal current rating, ρ is the cable resistivity, ΔV is the acceptable or target voltage drop, x is the cable reactance per km, and c is the number of conductors per phase. Equations (2.1) and (2.2) are frequently reported for minimum cross-section calculations despite the fact that they do not consider the thermal limits, acceptable losses, and have direct proportionality with the power line length. Additional parameters required to improve the calculations are not usually explicit in the procedures. Table 2.3 shows the summary of the cabling calculation for the Superyacht.

The column *component* considers one of the installed in the vessel. *Connection* refers to the connection type of the component or its drive. *Cables per line* account for the parallel cabling required in the installation, depending on the current rating. *Circuits* include double connections and/or parallel drives. *Cabling count* reflects the total number of cables required for the component. *Cable type* indicates the cable type selected from the marine cabling catalog [52].

Weight

The weight estimation utilizes information from Table 2.3 and the cable length for each case. In the centralized switchboard, the weight of the DC cable is neglected because the connection occurs inside the switchboard, whereas AC cables extend from the switchboard to the generators and loads. In contrast, the distributed switchboard requires extended DC cables from the switchboard to the power converters, neglecting the AC cabling.

The outcome of the weight calculation shows approximately 15.000 kg for the AC cabling in the centralized switchboard, while the DC cabling in the distributed case shows about 10.000 kg, which indicates a 35% difference. Consequently, the cabling reduction implies a volume reduction which is close to 36% for the current use case.

Losses

The calculation of the losses is a relatively straightforward process built upon the cabling selection. The cabling cross-section, the length, the resistivity and the

Table 2.3: Switchboard approach cabling comparison for a Superyacht.

Component	Connection	Cables per line	Circuits	Cabling count	Cable type
Primary generator	Three-phase	10	1	33	150 mm^2
	Unipolar DC	8	2	32	70 mm^2
Secondary generator	Three-phase	8	1	24	95 mm^2
	Unipolar DC	9	1	18	70 mm^2
Main propulsor	Three-phase	8	2	48	95 mm^2
	Unipolar DC	9	2	32	95 mm^2
Bow thruster	Three-phase	5	1	15	70 mm^2
	Unipolar DC	8	1	16	50 mm^2

number of parallel cables are the factors considered in the calculation. The carried-out estimations include two operation modes of the Superyacht. Full-speed cruising and maneuvering.

- **Full-speed cruising:** 96% of the installed power is necessary during this operation mode. All the generators operate at equal load, the main propulsors run at full-speed, and the bow thruster has minimum consumption.
- **Maneuvering:** Only the main generators operate at 45% of their capacity, while the secondary generators are off. The main propulsors run at 15%, and the bow thruster runs at 75% of their nominal speed.

Figure 2.5 summarizes the results considering the losses for the main components in the system. The losses in the cabling for the distributed switchboard are significantly lower than in the centralized case for both operation modes. The loss reduction in the cabling in cruising mode is about 32%, whereas in maneuvering rises up to 42.5%.

Nevertheless, the number of parallel cables in the system increases the current rating of the lines while reducing the losses. When considering that DC cabling losses in cruising mode are 14.2 kW lower than with AC cabling, and 1.93 kW lower in maneuvering mode, it is unclear whether such a difference could create a noticeable impact for the application and the specific use case. However, the difference is not negligible and could increase with the evolution of DC systems.

2.2.5. Key challenges

As the system design does not have a common-structured process, manufacturers and stakeholders propose their solutions to fulfill their business objectives. However, the outcome of such decisions is frequently contradictory, and some basic

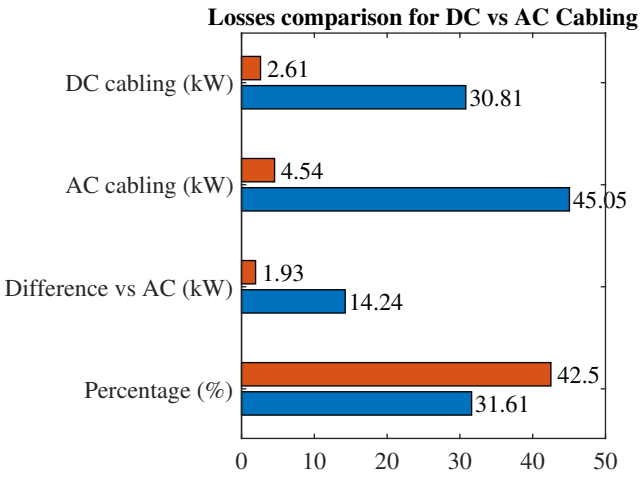


Figure 2.5: Estimated loss comparison of the primary power system for distributed (DC cabling) and centralized (AC cabling) switchboards in a DC equipped Superyacht. *Blue:* Cruising (high load), *Orange:* Maneuvering

concepts have no explicit consideration. Among the existing gaps, the absence of guidelines on control and coordination of protection to limit the impact of a fault is considered an exciting research opportunity.

Fault propagation and characterization studies in shipboard DC systems are required to characterize the behavior of possible faults onboard. These studies can be used in support of the control and protection coordination design to limit fault propagation. The result of that work should serve as input for a structured decision-making process to properly define protection and coordination requirements in shipboard DC systems considering the final application. In the future, this could also serve to expand the rules and regulations that are currently incomplete.

Considering the Superyacht under study, the system power density could increase substantially in the distributed switchboard following the cabling layout. The volume and weight savings discussed in this document are valuable for design of future DC systems and require expansion to other parts of the vessel and applications. The losses calculation in this document are a starting point to quantify the potential savings acquired by deploying a distributed switchboard.

2.3. Protection strategies in shipboard DC systems

Some challenges behind the missing DC protection guidelines hinted at in Section 2.2, rely on technical differences from AC technology because of the natural characteristics of DC [26]. These characteristics make AC protection ineffective for DC systems, forcing intensive research on DC circuit breakers and power electronics for protection systems [5]. However, these protection systems have limitations that

affect their feasibility for shipboard DC systems, such as time response, efficiency and cost-effectiveness. This section introduces some of the natural characteristics of DC systems that affect protection effectiveness. An overview of the typical faults onboard, the general protection requirements and the recommendations from the standards are also presented. The breaker-based protection for DC systems and some identified challenges are covered, including a brief survey of marine certified components. Power electronics-based protection, or breakerless protection, is introduced, showing the current limitations and challenges. The section concludes with a comparison of technologies from the perspective of shipboard DC systems.

2.3.1. Natural characteristics of DC systems

DC protection systems and design are trending topics of research. The intrinsic characteristics of DC make the protection systems more challenging than in AC [5], creating a broad selection of research opportunities to exploit. Scholars are mainly focusing on the following matters.

- **Current zero-crossing:** The lack of natural zero-crossing behavior in DC creates two challenges in protection systems. 1) Circuit breakers require a forced high amplitude counter voltage to allow the mechanical contact separation [26, 47, 53, 54]. 2) Reactive components utilized for filtering power converters and other functionalities in the system remain charged in normal circumstances [5, 26, 31].

- **High-speed - high current rising interruption:** DC systems have a relatively low impedance, which requires high-speed high-current interruptions. That is, to avoid the rapid growth of faulty current (e.g., a short circuit) that could reach the current interruption capacity of circuit breakers [26, 47, 53, 54].

- **High thermal stress and losses:** Fast solid-state circuit breakers (SSCB) protection devices produce higher conduction resistance than mechanical circuit breakers (MCB). The device has conduction losses during steady-state operation, whereas the rising currents can lead to overheating and damage of the device during transients [53].

- **Fault location:** As no information about phasor and frequency is available, detecting the fault location can be more challenging for reliable power distribution [55].

Additional challenges have been identified, such as the high-current turn-off for solid-state devices, arc extinction, grounding scheme, superconducting current limiters, cybersecurity, integration of multiple renewable energy sources or mode change. Those challenges apply to a certain extent in shipboard DC systems and are under investigation for conventional (inland) DC grids [55], which are beyond the scope of this document.

2.3.2. Faults in shipboard DC systems

Shipboard DC systems faults studies are reasonably similar to AC systems and other DC application studies. For instance, most relevant studies focus on different kinds of short circuits and their detection, whereas the standards propose related exploratory studies [26, 42, 56, 57]. As power electronics can limit the impact of open-circuit and overvoltage faults, their study is scarce in the literature for shipboard DC grids. The work in [55] categorizes the short circuits for generic DC microgrids into transient and steady-state faults. The transient considers the energy stored in capacitors, inductances and cables. The steady-state considers long-lasting faults facilitated by power supplies e.g., distributed energy resources. In shipboard DC systems, the transient response has essentially the same origin, whereas the steady-state could also come from the motors [26].

Different types of short circuit and their effects have been extensively investigated for various applications. In shipping, the short circuit capacity lies mainly on the DC filters of the drives and the impedance of the circuit [58, 59]. The time response follows the lumped RC circuit as $\tau = RC$, whereas the current variation is guided by $^{di}/_{dt}=^{V_0}/_{L}$. In general, the output capacity varies from several mF up to hundreds of mF according to the application and the number of drives, whereas the impedance mainly depends on the parasitic inductance of the system. For instance, in a multi-megawatt DC system, the capacity could reach about 300 mF, and the parasitic inductance will vary with the cabling arrangement, the bus bars and the drive connection. Scholars find the pole-to-pole and pole-to-ground short circuits the most relevant to study [26, 57, 60]. The simulation in Fig. 2.6a shows the behavior of a pole-to-pole short circuit in a 1.5 MW system, whereas the simulation in Fig. 2.6b shows the pole-to-ground case. The simulation model includes the parasitic effect of the cabling and the drives, an equivalent capacity of 50 mF and a DC bus voltage of 1000 V. In addition, the model considers a floating ground scheme commonly utilized in maritime applications [25, 42].

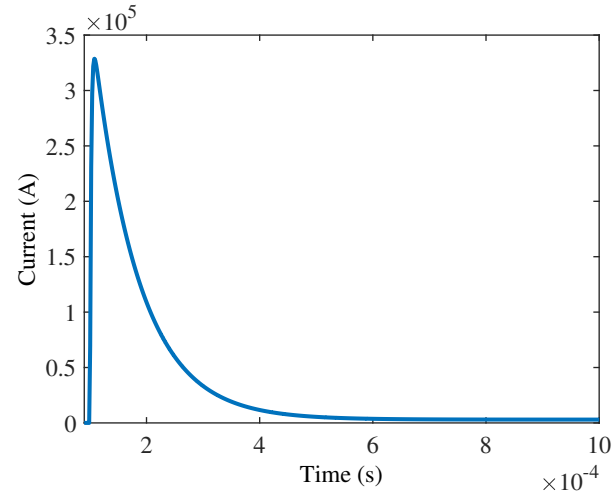
The results in Fig. 2.6a exhibit a peak current close to 330 kA in about 8 µs. Meanwhile, the pole-to-ground fault in Fig. 2.6b has a similar $^{di}/_{dt}$, but the maximum current reaches close to double the nominal current before starting to decrease. Consequently, this chapter reviews those short circuits and the protection requirements inherited from their characteristics.

Pole-to-pole short circuit

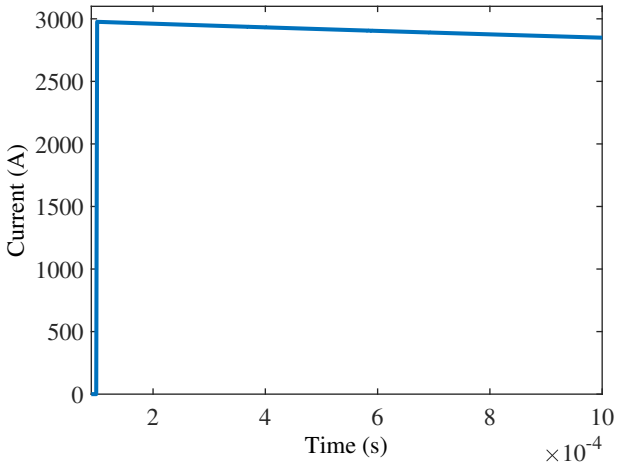
The pole-to-pole short circuit is a low impedance fault and is the most dangerous onboard [61]. During the transient event, the capacitors discharge into the fault, creating a high $^{di}/_{dt}$ condition where the current can reach tens of thousands of Amperes if not interrupted [61]. The transient and steady-state effects of the pole-to-pole fault applied to the AC generator are studied in [26, 55].

Pole-to-ground short circuit

The pole-to-ground short circuit is a high-impedance fault, and the impact is generally less severe than the pole-to-pole case [55]. Generally, the severity of the



(a)



(b)

Figure 2.6: Simulation of a short circuit in a 1.5 MW shipboard DC systems at 1000 V, considering output filters and parasitic inductances. (a) Pole-to-pole event. (b) pole-to-ground event.

short circuit depends on the grounding impedance, which varies with the grounding scheme [62]. Shipboard DC grids usually feature a floating ground, and further development on the high-impedance grounding is expected [63]. Despite the potential loss of the DC bus, the current overshoot in a pole-to-ground fault is limited or nonexistent because of the ground impedance, as shown in [55].

Protection requirements

The design of the protection system of a DC system must protect all entities interacting with it, and the service availability should not be compromised [47]. The premise of the protection system is to comply with the following directives.

- **Safety:** All systems and individuals are working/operating safely with the system.
- **Sensitivity:** The protection systems can detect different types of faults in the system.
- **Security:** The protection devices act when required only, avoiding false tripping.
- **Selectivity:** Constrained by the distribution architecture, only the faulty region/component should be isolated.
- **Speed:** Usage of high-speed protection systems to prevent blackouts and extended damage.
- **Cost-effectiveness:** Compared to the protected systems, the cost of the protection system must justify the investment.

Furthermore, the recommendations provided by some standards facilitate the overview of protective measures to consider. The IEEE Std. 1709-2018 recommends a series of studies intended to ensure the compliance of the DC system with some basic definitions of protection and survivability [42]. The standard recommends pole-to-pole, pole-to-ground, and pole-to-pole-to-ground fault studies caused by component failure, power converters and sub-systems attached to the DC bus. In addition, the document includes communication and sensor failures, cooling system malfunctions and fault management studies for post-fault restoration.

The IEEE Std. 45.1-2017 includes additional recommendations to consider despite the limitation regarding specific DC protection measures. The faults classification includes overcurrent, ground, line-to-line, internal equipment, loss of phase, and others [44]. Additional information about fault management and some protection design guidelines are also available. Nevertheless, the recommendation of DC systems is limited to a maximum short circuit current calculation.

In order to tackle the directives, two types of protection architectures for shipboard DC systems have been proposed in [5]. The *breaker-based* protective architecture, and the *power electronics-based* protective architecture also known as breakerless or unit-based protection [37, 64]. The remaining of this section investigates the protective architectures and their technology, the current panorama of DC circuit breakers and the development of SSCBs.

Shipboard protection zones

DC protection systems normally includes zones of protection for the different parts of the grid that change with the requirements [65]. One common approach is segregating in zones based on fault clearance time in a three-level protection scheme, summarized in Table 2.4.

Table 2.4: Definition of protection levels in marine DC power grids [65]

Protection	Action	Protection component	Response time
1	Fast	Solid-state bus-tie switches	up to 10s of µs
2	Medium	Solid-state circuit breakers and high-speed fuses	up to a few ms
3	Slow	Generator deexcitation, fold-back protection control, high-speed fuses, solid-state circuit breakers	up to several seconds

Such an approach is considered cost-effective for radial architectures onboard ships because of the simplicity and the lack of (complex) communication requirements. Therefore, manufacturers rely on similar schemes during protection designs [66].

The three-level protection in scheme in Table 2.4 has disadvantages in two types of fault. Bus separation failure and limited selectivity and sensitivity of the feeder protection [66]. The first challenge is addressed in the literature by enhancing the reliability, protection performance, and added features of the bus separation component. The selectivity issue requires the adjustment of the DC capacitance and high-speed fuses and circuit breakers [54, 56, 66]. In contrast, an intelligent electronic device-based differential and directional protection can identify and isolate a fault with minimum system loss. However, the system features a relatively high cost, relies on special communication systems, and requires a device with a circuit breaker in every feeder, which limits their cost-effectiveness [66].

2.3.3. Breaker-based protection

As the name suggests, breaker-based protection systems utilize several circuit breakers installed and coordinated to protect the system. Circuit breakers are the first component for short circuit and overload protection in any MVDC system. An extensive classification, description, and discussion regarding circuit breakers, including mechanical and solid-state components, is available in [53]. Another comparison is presented in [25], discussing the advantages and drawbacks of different circuit breaker technology. Future trends for SSCB are examined and discussed in [67]. The comparison presented in [54] includes DC-DC converters in the analysis and discussion to highlight the potential benefits of breaker-based and breakerless protection architectures. Finally, the work in [68] shows the design and protection

scheme and testing of SSCBs for shipboard power systems, highlighting the need for further development.

There are several circuit breaker technologies to consider. The following sections briefly introduce the fundamentals of the most relevant technologies and a brief selection of commercially available DC circuit breakers with marine approval.

1. Mechanical circuit breakers
2. Solid-state circuit breakers
3. Hybrid circuit breakers
4. Solid-state bus-tie switches
5. Marine-approved DC circuit breakers

Mechanical circuit breakers or MCBs

Circuit breakers need to build up a counter voltage at least equal, but preferably higher than the bus voltage to force the current to drop to zero ampere to interrupt the circuit [69]. For MCBs, there are two operation technologies to consider, the passive resonant circuit breaker (Fig. 2.7a) and the active resonant circuit breaker (Fig. 2.7b) [25, 53, 65].

Both active and passive circuit breakers use the same principle to operate. The use of an LC resonant branch to reach the fault current and extinguish the arc and a metal-oxide varistor (MOV) to clamp the voltage to a maximum permissible value [53]. The difference between the two circuit breakers lies in the inclusion of auxiliary switches to enhance the breaker performance [53, 54].

Solid-state circuit breakers

In SSCBs, power semiconductors controlled by gate drivers are utilized instead of mechanical switches [53, 69]. The wide variety of semiconductors enables a variety of SSCB topologies with specific advantages. Some typically employed technologies, which are used according to the current rating requirements, are the insulated gate bipolar transistors (IGBT), the reversing block IGBTs, the integrated gate-commutated thyristor (IGCT), the power metal-oxide-semiconductor field-effect transistors (MOSFET), the power junction-gate field-effect transistors (JFET) and the power diodes.

This section presents a typical categorization of SSCBs as follows: a) *unidirectional (Fig. 2.8a)*, b) *bidirectional (Fig. 2.8b)*, and c) *thyristor-based (Fig. 2.8c)*. The latter technology (thyristor) is mostly used in AC SSCBs because the commutation requires the current zero-crossing behavior to impress a high impedance into the circuit, while the other technologies depicted in Figs. 2.8a and 2.8b can impress a high impedance behavior independently of the flowing current magnitude, thus being well-suited for DC SSCBs. Extended relevant information available in [25, 32, 53, 54, 71].

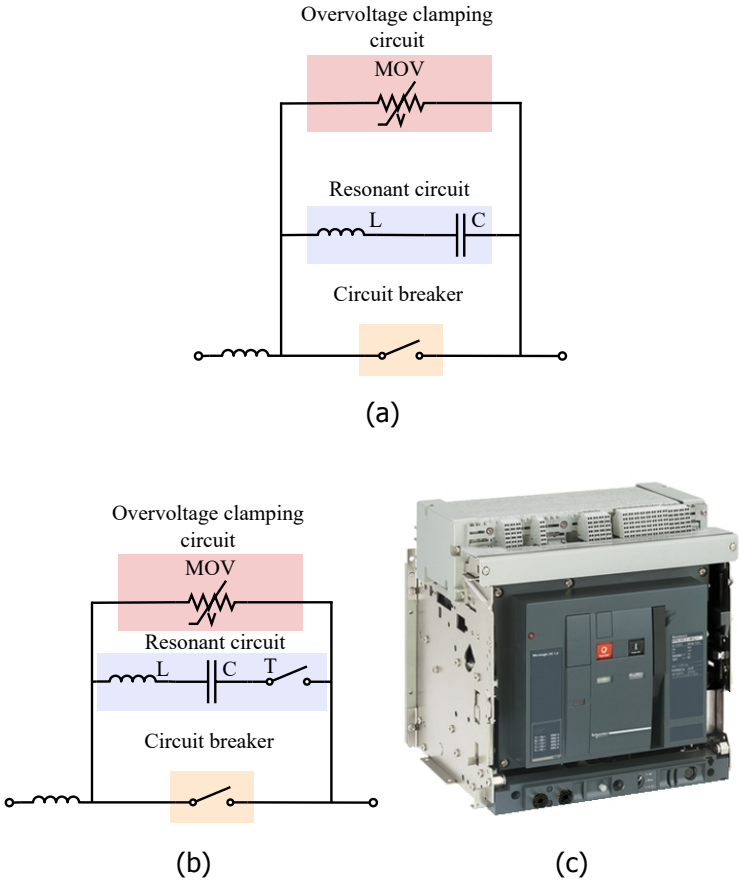


Figure 2.7: Referential schematic diagram of mechanical circuit breakers. (a) Passive configuration. (b) Active configuration. (c) Commercially available mechanical DC circuit breaker from Schneider Electric [70].

Unidirectional Unidirectional SSCBs use single or series-connected arrays of controlled switches (JFET, MOSFET). The circuit allows bidirectional current flow but unidirectional current interruption because the voltage interruption is possible in one direction only [25, 53].

Bidirectional Bidirectional SSCBs use anti-series power semiconductors e.g., IGBTs, to realize bidirectional voltage blocking. The disposition of the power semiconductors is variable and frequently placed in series arrays and/or in parallel to achieve the voltage rating and power level required. These are typically enhanced with passive components and varistors to facilitate commutation and voltage clamping [53, 54].

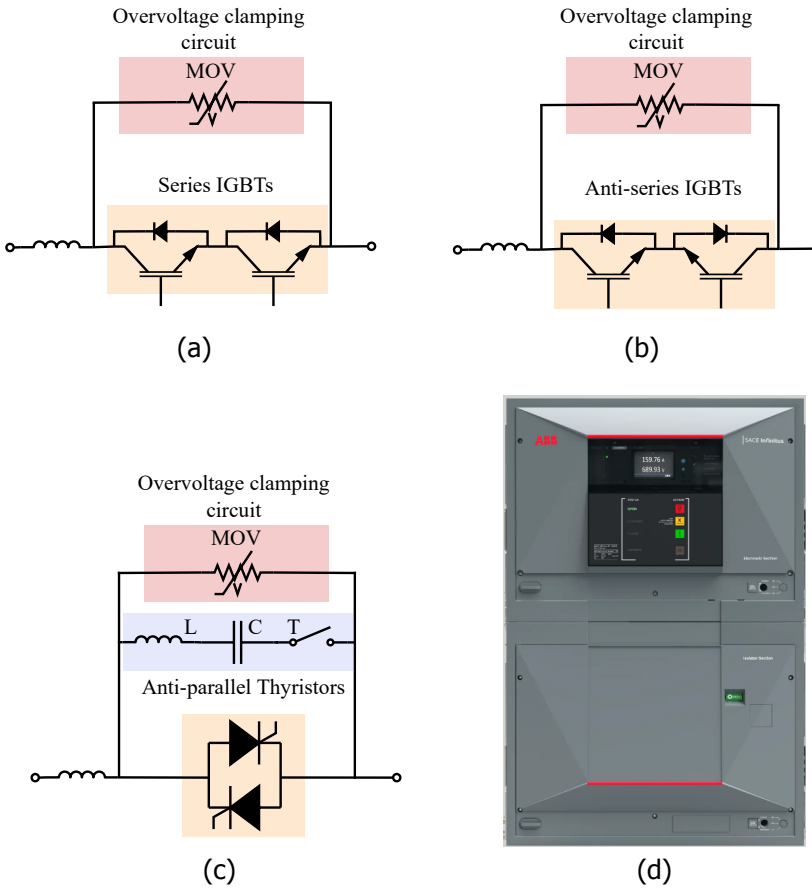


Figure 2.8: Referential schematic diagram of (some) solid-state circuit breakers. (a) Unidirectional configuration. (b) Bidirectional configuration. (c) Thyristor-based configuration. (d) Commercially available SSCB from ABB based on reverse-blocked IGCTs [72].

Thyristor-based Thyristors have high commercial readiness, have a mature manufacturing process and the highest voltage and current ratings in single-package devices [53, 73]. Nevertheless, thyristors require resonant parallel circuits to create the zero-crossing current needed for DC SSCB [53], which can also limit the protection performance of the device. IGCTs are preferred over thyristors in DC SSCBs, because of their non-zero current blocking capability. In addition, IGCTs in anti-parallel configuration do not require the resonant branches shown in Fig. 2.8c. The commercial SSCB in Fig. 2.8d is based on reverse-blocked IGCTs, which enable high-speed protection with limited losses [74].

Hybrid circuit breakers

The hybrid circuit breaker (HCB) is a combination of the SSCB and the MCB to exploit the advantages of both technologies [25, 53, 54, 75], one of many available examples is depicted in Fig. 2.9.

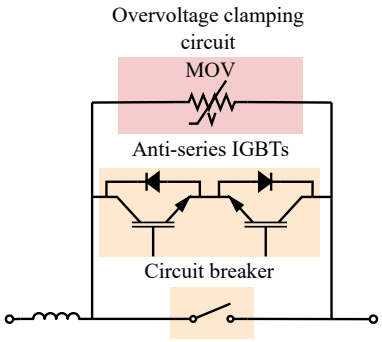


Figure 2.9: Referential schematic diagram of one (of many) hybrid circuit breaker.

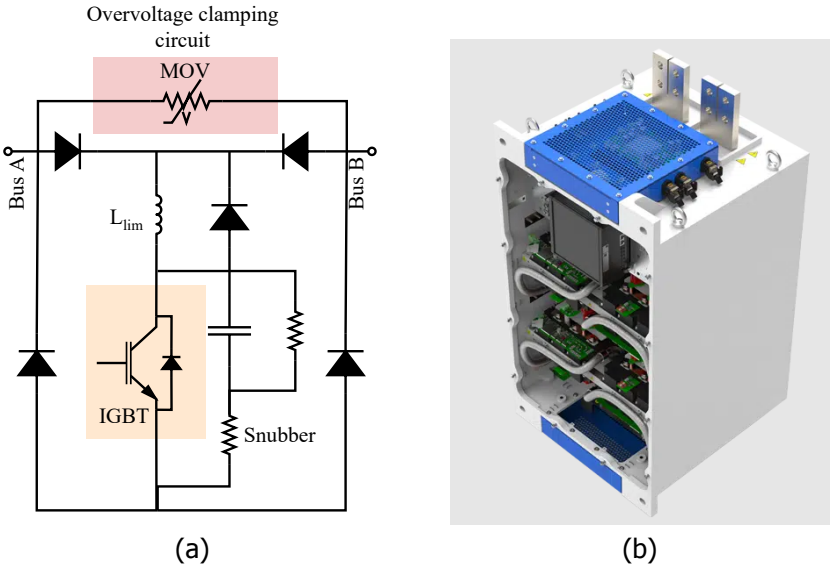
In HCBs, normal current conduction is achieved with the mechanical switch, while the high-speed protection is achieved by the power semiconductors [53]. Such configuration allows the device to break the current arc-free (possibly enhancing the mechanical switch lifetime) at high speed with low conduction losses [69, 74]. As a result, the thermal management of the semiconductor can become less complicated than the devices depicted in Fig. 2.8. The HCB topologies are also varied, allowing designers to enhance the specific characteristic of the component [53].

The works in [76, 77] show extensive dedication to improving the response time of the HCB by using wide bandgap emitter turn-off thyristors and fast mechanical switches in a 7 kV lab DC system, close to the MVDC class 6 (6 kV), triggering a 100 A fault in the DC bus with a clearance time of around 1.75 ms, which is not a fast response time for DC systems. The work in [78] shows a different HCB design using current injection to reach fast zero current with a setup of 400 V and fault current of around 90 A, cleared in about 310 µs. The described system requires adjustment to match the HVDC or MVDC levels that the author claims.

Solid-state bus-tie switch

The bus-tie switch is a special circuit breaker that shares multiple characteristics with the SSCB. These switches are specially adapted to connect two bus bars as part of the onboard DC power system [23]. The device is designed for ultra-fast and safe operation in coordination with other protection components [79]. Figure 2.10a shows one of the proposed topologies designed and tested in [65] for reference.

The solid-state but-tie switch is the first protection device to act when a fault occurs. Hence, the device should achieve a clearance time within a few micro-seconds, low conduction losses, bidirectional operation (current and voltage), and independent fault detection functionality [81].



(a) (b)

Figure 2.10: Example of a solid-state bus-tie switch (a) Referential schematic diagram of one (of many) solid-state bus-tie switch. (b) Commercially available IGBT-based solid-state bus-tie switch from KWx [80]. *disclaimer: the product from KWx does not necessarily has internal configuration of the schematic in (a).*

Different scholars are proposing using integrated procedures to enhance several characteristics, such as response time, thermal dissipation, and voltage balance for bus connections [65, 79, 81]. The complexity of the device is generally high, leading to an expected high cost that can restrict the implementation feasibility for various applications. Furthermore, the quantity of bus-tie switches in a shipboard DC system is not high, so it would be necessary to evaluate against the design requirements.

2.3.4. Development of solid-state circuit breakers

Modern SSCBs include various protection capabilities besides the breaker functionality, such as inrush current limiter and overload protection [26]. SSCB technology requires additional design considerations to ensure the proper operation of the breaker. This section reviews 1) popular control strategies, 2) thermal management, and 3) current research in SSCBs.

Breaker control

The control strategy applied to the SSCB and the solid-state bus tie switches is fundamental for the protection performance. The switch-on limiting inrush current,

the current limiter, the overload protection, and the short circuit protection are a few of the most significant functionalities embedded into a SSCB controller [82].

- **Switch-on limiting inrush current:** The functionality aims to enable a safe start of the power converters by limiting the current to slowly charge the output capacitors [83, 84]. The procedure described similarly to a rule-based controller in [82, 85] is summarized as follows. During the turn-on, the SSCB closes in a short circuit condition that limits the current charging the parallel capacitors. The capacitors charge without current overshoot, and the SSCB changes to on-mode when complete, allowing the normal load supply.

- **Current limiter:** Current saturation is a basic protective functionality for SSCBs [84]. The circuit maintains a predefined maximum current during a short circuit and avoids current oscillations when the fault is removed [82, 86]. The current saturation includes a latching timer avoids prolongation of the faulty condition beyond limits.

- **Overload protection:** The overload implies demanding more current than the maximum defined during a relatively long period, which is not necessarily triggered by a short circuit [84, 86]. The SSCB acts as current limiter throughout an overload, activating the latch timer. Once the latch timer expires, the SSCB disconnects the load and remains locked until a manual reset is activated [82].

- **Short circuit protection:** The short circuit is the worst-case scenario for a protection system [86]. The transient current overshoot is processed by the control unit, which triggers the off mode of the SSCB [83, 87]. After the transient state, the SSCB operates as a current limiter and disconnects the load, requiring a manual reset [84].

Different control strategies applicable in SSCBs enable such protection functionalities. The gate signal modulation is utilized for transient overvoltage reduction (see *gate signal modulation*), whereas the $^{di}/_{dt}$ control is suitable for current transient protection (see $^{di}/_{dt}$ *control*) [83]. Investigating these techniques is relevant to this work and are reviewed in the following sections. The latched protection action and the voltage overshoot suppression are basic complementary strategies exploited in SSCB control [88, 89].

Gate signal modulation The investigation in [88] shows the gate signal modulation for protection purposes in the three following ways.

1. Conventional two-level gate waveform Fig. 2.11a
2. Gate waveform with intermediate level during turn-off Fig. 2.11b
3. Gate waveform with slope transition during turn-off Fig. 2.11c

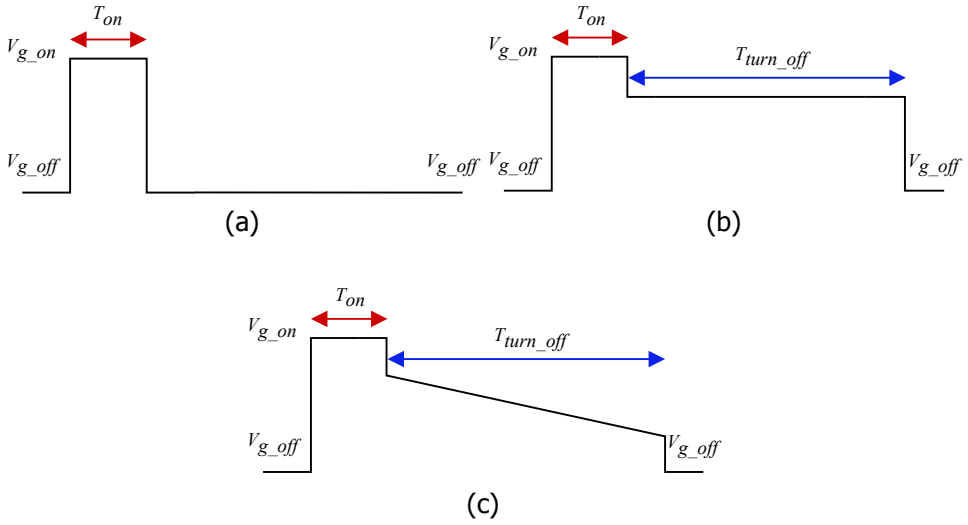


Figure 2.11: Gate signal modulation waveforms for SSCB control. (a) Conventional two-level. (b) Three-level with intermediate turn-off level. (c) Three-level with ramp turn-off transition.

The normal gate modulation in Fig. 2.11a could cause resonance considering the circuit inductance and the parasitic capacitance in the switch [88]. The overvoltage created throughout the resonance can affect the operation of nearby SSCBs, potentially reducing the performance of the protection device. For the three-level modulation in Fig. 2.11b, the resonance overvoltage could decrease by reducing the gate voltage [88]. However, such modulation does not enable zero-current switch, which can trigger a resonance behavior during part of the turn-off process. In the ramp turn-off modulation in Fig. 2.11c, the gate voltage decreases linearly, allowing a "soft" interruption of the current [88]. The resonance could attenuate its magnitude by allowing a slow reduction of the gate voltage.

Considering an adequate tuning of the PWM signal, the SSCB performance could remain within the design requirements, while the resonant behavior could attenuate significantly, especially during turn-off. Nevertheless, the utilization of resistor-capacitor-diode snubbers is common to mitigate resonance and overvoltage issues in SSCBs [90]. The snubber design requires a careful parasitic impedance estimation. However, the solution is relatively simple and does not affect the performance of the SSCB [91]. The convenience of one of those solutions is not evident for every application. A performance benchmark is then required to justify a selection and obtain a cost-effective solution.

di/dt control As discussed previously, most of the protection functionalities in SSCB are directly related to current control. Hence, current variation rate is an

expected variable to monitor during active protection. The current sensing usually requires shunt resistors, current limiting inductances, hall effect current sensors, or Rogowski coils [89, 92, 93]. In general, SSCBs demand high-speed detection sub-systems to cope with the short circuit current of DC systems [90].

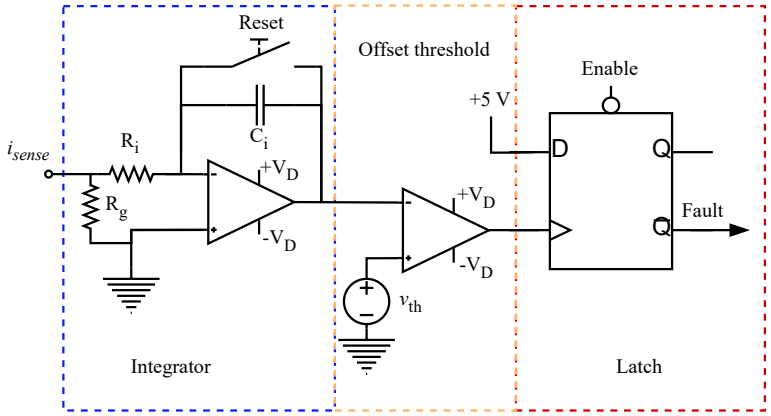
Consequently, the fault detection circuit demands a relatively short response time that outperforms most digital controllers. Hence, scholars rely on high-bandwidth comparators to implement analogue high-performance fault detection circuits [90, 92]. Different control circuits are applicable depending on the application and the installed sensor [89, 90, 92]. An example of the detection circuit designed for the desaturation functionality of SiC MOSFET drivers is depicted in Fig. 2.12a. The desaturation action normally applies to switch devices as a protection mechanism against semiconductor short circuits [94]. The diagram in Fig. 2.12a is applicable for Rogowski coil measurement, which requires an integration stage. The high-speed protection system allows fault detection and protection within 400 ns and a clearance time of around 700 ns [92].

Figure 2.12b depicts a $^{di}/_{dt}$ control circuit for a GaN SSCB with a high-speed hall-effect sensor (500 ns). The circuit includes a resistive divider with a variable resistor to adjust the threshold current. The high-speed comparators (4.5 ns) and logic gates (9 ns) allow fast fault detection and latching of the breaker [90].

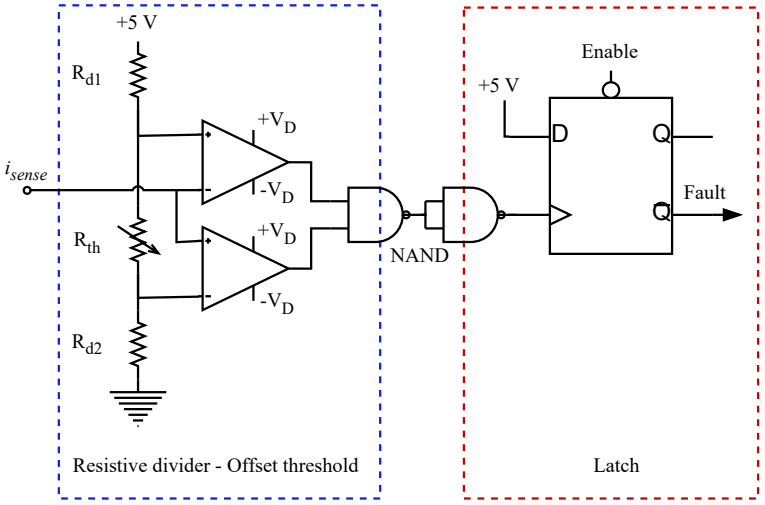
A relatively small external inductor, e.g., $L_{di/dt}$ = 500 nH, can be added to the SSCB to sense the $^{di}/_{dt}$ of the flowing current by measuring the voltage across this inductor with a high-bandwidth differential strategy. A SSCB prototype has been designed to verify this functionality with the main schematic and final circuit shown in Figure 2.13. Therein, external $^{di}/_{dt}$ inductors ($L_{di/dt}$) are used to fast detect low-impedance short-circuits, and hall-effect current sensors complements the protection as these are effective to detect short-circuits with much lower $^{di}/_{dt}$ (or high impedance short-circuits). Additionally, to protect the SSCB against over-voltages, varistors are placed across the upper- and lower-side common-source bidirectional switches, and small shunt capacitors C_f are used for improving protection selectivity. The fault detection logic is similar to that of Fig. 2.12b. More detail about this SSCB can be found in [47, 89].

Figure 2.14 shows the experimental results of the SSCB prototype in Figure 2.13, where a 350 V DC source is connected between the terminals a and n and a resistive load is connected between the terminals b and N. After a certain time, a contactor is used to apply a low impedance short-circuit between the terminals b and N. The differential voltage measurement obtains a signal proportional to the flowing current $^{di}/_{dt}$. If the $^{di}/_{dt}$ is high, then the existence of a low impedance short-circuit is detected, and the voltage across the inductor will be proportional to the rise of the fault current.

In Fig. 2.14 it is also possible to identify the detection and response time of the designed SSCB. The short-circuit occurs in A, which has a delay in the comparator detection of about 850 ns. Then, the short circuit is detected in B, where the gate command for all switches (S_{pa}, S_{pb}, S_{na}, and S_{nb}) is set to OFF, whereas the clearance of the short circuit starts with the voltage increase across the SSCB switches in C. Herein, the switch impedance is increased according to the slow drop of gate



(a)



(b)

Figure 2.12: Schematic of analogue $^{di}/_{dt}$ control circuits (a) Latched $^{di}/_{dt}$ control circuit for SiC MOSFET drive desaturation. (b) Latched $^{di}/_{dt}$ control for a wide bandgap SSCB.

voltages as shown in Fig. 2.11c. All in all, the low power prototypes available is valuable for the development of maritime certified SSCBs, and for foresee the evolution of the technology.

Nevertheless, the studies about feasible and adequate control strategies in SSCB for shipboard DC systems are not common, and further investigation is needed to achieve the performance requirements without penalizing the cost-effectiveness

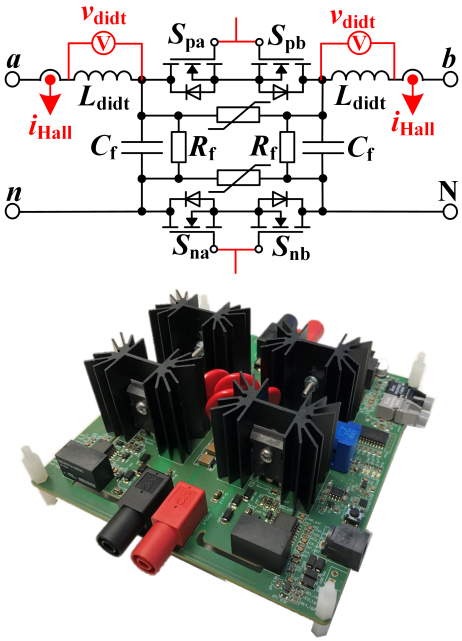


Figure 2.13: Basic schematic and prototype of a down-scaled SSCB implementing $^{di}/_{dt}$.

of the device. SSCBs offer a wide selection of functionalities for circuit protection embedded in the controller. Gate modulation strategies and damping circuits are convenient to mitigate the impact of hard breaking.

The convenience of the gate modulation or the damping circuit could require an application-specific assessment. High-speed analogue circuits are suitable for SSCB control for different applications and sensors. Given that hall-effect current sensors may have a slower response than the Rogowski coils but are less vulnerable to electromagnetic interference and noise, the characterization of specific DC systems could facilitate the selection, design and calibration of current sensors. In future developments, a selection of controllers and functionalities for shipboard DC applications is necessary to improve system safety while reducing the hardware required to comply with protection requirements.

Thermal management

The efficiency, power density, and reliability of SSCBs, HCBs and solid-state bus-tie switches are closely related to the thermal stability of the utilized semiconductors [95]. Fast heat removal is especially relevant in DC systems because the high current variations created by a fault can easily damage the semiconductor and possibly affect the equipment connected [31].

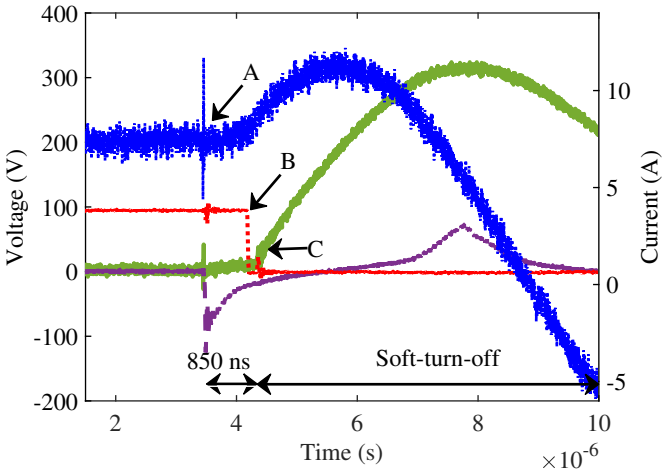


Figure 2.14: Experimental results of the solid-state circuit breaker depicted in Figure 2.13 with $^{di}/_{dt}$ protection showing the three main operation steps. A short-circuit instant, B instant of fault detection which creates a signal to turn-off all SSCB's switches, and C is the instant where the soft turn-off of the SSCB starts. *Blue:* input current measured at the terminal a, *red:* fault logic signal, *green:* voltage across the upper SSCB switches (S_{pa} and S_{pb}), *purple:* voltage across one of the $^{di}/_{dt}$ inductor.

In SSCB and HCB, steady-state and transient operation conditions have different cooling requirements [53, 96]. In the event of a fault, the rapidly rising current increases the temperature in the semiconductor. The heat transfer still requires a few additional milliseconds to dissipate the power, which means that the effectiveness of the cooling solution drops during transient events [97]. The heatsink may have a small influence on dynamic performance because of its thermal capacitance.

Figure 2.15 shows the simulation of a SSCB based on the IPB200N25N3 semiconductor, which has a maximum current of 50 A at 100 °C. To highlight the effect of various heatsinks in transient response, the SSCB is opened and closed at different intervals, allowing thermal stabilization after each event.

The ambient temperature is defined as 45 °C to consider the effect of other equipment placed in the switchboard. The thermal resistance of the heatsink in Fig. 2.15 is reduced in steps by 10% to account for various oversizing cases. Such variations have limited effect during the transient as the temperature variation is similar in all cases, with a significantly slow dynamic response. Although the steady-state junction temperature decreases when oversizing the heatsink, the transient performance is different.

In the breaking event, the junction temperature drops about 24 °C in approximately 220 ms for all cases, while the fall time of the transistor is around 12 ns. When the switch is closed, the junction temperature rises an average of 24 °C in about

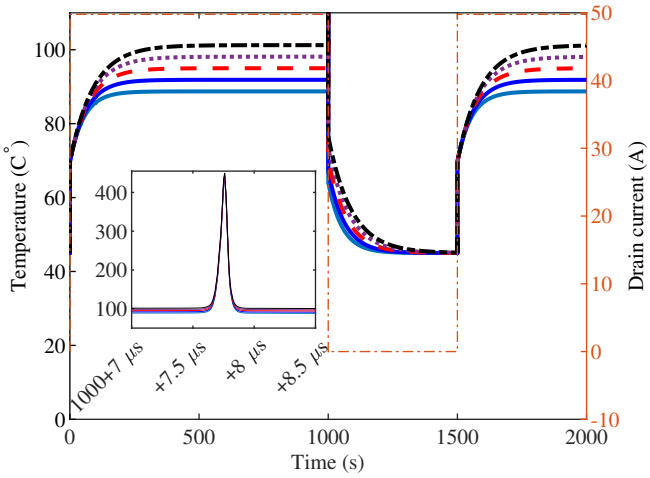


Figure 2.15: Dynamic response of the junction temperature in a MOSFET-based SSCB for various heatsink sizings at 45 °C ambient temperature. The base case considers the maximum current of 50 A at 100 °C (dash black), the current transitions from 0 A to 50 A and back (dash/dot light red), and four cases of thermal resistance. *Inset:* Detail of the junction temperature overshoot after disconnection, in microsecond scale.

50 ms regardless of the thermal resistance. After the sharp increase, the junction temperature increases by 9 °C on average for more than 30 s before the effect of the heatsink is partially visible. Such results suggest that the sizing of the heatsink has a minimal impact during transient operation and maximum effect in steady-state. Therefore, the semiconductor packaging and its maximal thermal limits will define the maximal protection current of the device (µs dynamics), whereas the size of the heatsink (ms to s dynamics) will have little impact on this matter. In subsequent breaking events, where the thermal stabilization is not achieved, the heatsink oversizing may not avoid the overheat protection triggering.

Nevertheless, the protection devices often feature oversized cooling solutions, such as high-volume heat sinks and water-cooling systems. The power density, the cost, and the reliability of the protection device can be consequently affected, which is considerably undesirable in ship applications, resulting in a mismatch with the market requirements [98].

Trending research

The investigation in [86] shows low-power SSCB for enhanced time response without considering other design variables. The work in [97] is focused on an integrated design methodology of SSCB considering clearance speed, reliability, cost and effi-

ciency. The LVDC SSCB design shown in [99] has an integral approach considering overload, short circuit detection, and load step changes as part of the SSCB design. The time response from 5 µs to 10 µs suggests a good starting point to improve the SSCB for LVDC circuits of the shipboard DC system, where the efficiency needs further enhancement.

Power efficiency is also essential to facilitate the semiconductor thermal management and, therefore, the complexity, cost, and power density of the SSCB.

For instance, hybrid semiconductor switches could facilitate the implementation of more efficient SSCBs [100]. The concept involves a combination of at least two different technologies of semiconductor functioning as a single component. The parallel Si IGBT - SiC MOSFET hybrid switch, is under study in various applications, such as residential, traction, and aircraft electrification [101–103]. Several hybrid SSCBs have been proposed and patented, exploiting the advantages of different semiconductor switches [104]. The short-circuit failure mechanisms of Si/SiC hybrid switches are studied in [105], showing the thermal runaway and the gate dielectric breakdown as the main failure modes for different short-circuit scenarios.

Considering the relative novelty of the hybrid Si/SiC switch, the background for SSCBs scarce. A comparison of Si IGBT, SiC MOSFET, and hybrid Si/SiC switches-based SSCBs was conducted in [100]. The Si/SiC hybrid SSCB prototype tested in [100] is similar to the schematic in Fig. 2.16, which is considered intrinsically fault-tolerant [106]. The research concludes that the hybrid circuit breaker is more

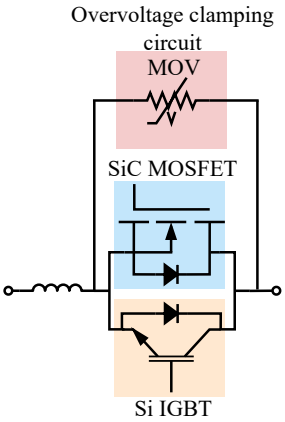


Figure 2.16: Referential schematic of a hybrid solid-state circuit breaker.

efficient and cost-effective than the SiC-based SSCB, showing higher current limit and overload capacity, lower surge voltage, better gate voltage stability, and lower cost. However, additional research and testing is required to assess the short-circuit current withstanding capabilities, the conduction losses quantification, the overall complexity increase, and the effect of the high-speed turn-off from the MOSFET in the reliability of the IGBT.

Further development on SSCB technologies is required to cope with the drawbacks compared to MCBs, such as cost, form factor and size of the complete device.

The development of marine certified SSCBs requires an integral approach to consider the previously mentioned research topics, and the intensive testing program that the device must undertake. Under such premises, it could be possible to develop a family of technologies that fulfill the technical requirements in ship applications.

2.3.5. Commercially available DC circuit breakers

There are several solution of DC circuit breakers and their availability changes with the application and the technology they use. The options for marine certified products required for DC systems is relatively limited compared to residential applications. For instance, the information regarding SSCBs is extensive for academic purposes, commercially available products are scarce when considering the certification. In contrast, certified mechanical solutions are more common, mainly because some vendors could provide an upgrade for already existing products.

Table 2.5 briefly describes some DC circuit breakers available in the market. The mechanical product is a suitable option for the application among different vendors, and have negligible power losses. The SSCB is a recently launched product by ABB and further information is required to create a complete assessment.

The loss estimation of the solid-state bus-tie switch at 1 kA comes from the nominal current losses in the datasheet. Such a calculation allows a rough comparison with other products and a detailed benchmark is necessary in the near future. At the time of writing, no marine-certified hybrid circuit breaker had been identified.

From the commercial products in Table 2.5, the following characteristics are identified and discussed.

Table 2.5: Example of commercially available DC circuit breakers with marine certification [70, 72, 80].

Type	**MCB**	**SSCB**	**Solid-state bus-tie switch**
Vendor	Schneider Electric	ABB	KWx
Reference	NW20HDC-C	SACE Infinitus	AA-10411-203
Rated voltage (V)	1000	1000	1000
Breaking current (A)	2000	2500	3000
Breaking time	30 ms	$\leq$ 25 µs	15 µs to 21 µs
Power losses (kW)	Not reported	1,3 @ 1 kA 0.67 @ 1 kA est.	6 @ 3 kA
Cooling solution	Air	Liquid	Liquid
Dimensions HxWxD mm	352x422x427	Not reported	507x207x912

1. Market choices
2. Breaking time
3. Conduction losses
4. Cooling solution
5. Volume

Market choices

The availability of MCBs is substantially broader than that of solid-state products, several major manufacturers (ABB, Schneider Electric, Siemens, Eaton) offer complete portfolios for different marine applications.

Breaking time

The breaking time of solid-state components is, on average, three orders of magnitude faster than the mechanical device. The performance of the protection system is affected by the time response of the circuit breakers, given that DC short circuit are relatively fast events. The MCB action may not be quick enough for protection against severe short circuits.

Conduction losses

Solid-state devices have relatively high conduction losses, and their characterization is essential for solid-state devices. On the contrary, mechanical components have negligible conduction losses. More efficient semiconductors are needed and expected in the future to increase the system efficiency. However, the conductors used in the mechanical devices should remain more efficient and faster mechanical solution could be developed.

Cooling solution

The device cooling is especially relevant for solid-state components. The liquid solution allows the downsizing of the heat sink for solid-state devices, whereas MCBs normally do not require additional components. Solid-state products require more complex solutions than the air-cooled heat sinks to operate adequately, potentially increasing the cost of the overall system. Nevertheless, in maritime applications, utilizing liquid cooling is well-known, which can benefit the implementation of this technology in centralized switchboards.

Volume

The volume of MCBs is substantially smaller than the solid-state counterparts, which is an advantage for installation. The solid-state units require space for additional components and other supplemental functionalities not considered for this analysis.

Despite the absence of information on the dimensions of the SSCB (from ABB), a form factor similar to the solid-state bus-tie switch could be possible.

The diversification of the SSCB solutions portfolio is necessary for the development of breaker-based protection. Such a scenario can improve the cost-effectiveness of the overall solution and possibly facilitate improvements in efficiency, cooling solutions, and volumetric power density.

2.3.6. Power electronics-based protection and fault- tolerant converters

Contrary to breaker-based protection, the power electronics-based protective architecture dispenses the circuit breakers and embeds the protection functionalities in the power converters, while employing fault-tolerant topologies, as illustrated in Fig. 2.17. The idea highlighted in this schematic is that the solid-state blocking capability is directly provided by the converter itself, e.g., by the upper and bottom switches of the active neutral point-clamped converter. Therefore, the power converters provide short circuit, overload and overvoltage protection, galvanic isolation and logically the power conversions [65]. However, the successful implementation of all SSCB functionalities is yet to be demonstrated in power electronics-based protection. Nevertheless, the technology requires only disconnectors and switches for circuit segmentation and bus transfer, which reduces the number of necessary components and system complexity. Figure 2.17 is an illustrative representation of a power electronics-based protection converter, which could replace e.g., the battery converters in Fig. 2.3 and their protection components.

The fault-tolerant topologies in Fig. 2.17 are based on reconfiguration capabilities after a component failure and redundancies [107, 108]. The converter allows several reconfiguration actions depending on the fault location and its severity. A mechanism allows the connection of the redundant "c" legs *(in blue)* to replace the malfunctioning of legs "a" or "b", maintaining the power level of the converter

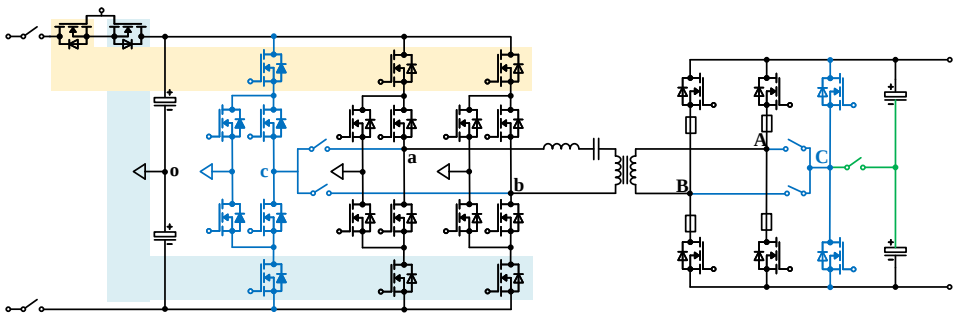


Figure 2.17: Representation of fault-tolerant power converter (Active neutral point-clamped series resonant converter) with embedded protection, part of a power electronics-based protection concept.

[109]. The three-level structure on the primary side allows several alternative current paths depending on the position of the faulty semiconductor, enabling partial power operations. The three-level topology can be considered then a single-failure tolerant architecture for the semiconductors, and do not require the incorporation of fuses within the semiconductor bridge-legs. In addition, the series semiconductors can be used as redundancy in case of a partial failure. The faulty switch is short circuited and the remaining switch provides the control [110]. Likewise, the full bridge on the secondary side can operate as a voltage doubler to maintain the operation voltage. This can be provided by the auxiliary switch drawn in green which can interconnect one of the transformer terminals to the capacitor mid-point. These reconfigurations are extensively studied in [107–109], where a survey about power converter topologies and prone-to-fail components are presented.

In addition, the protection circuit in Fig. 2.17 hints to a necessity of developing compact protection strategies, close to the converter or part of the topology to fulfil the safety requirements of maritime applications. The existence of conduction losses and the high relative cost of SSCBs can compromise the cost-effectiveness of the protection solution. Hence, the mechanical switch in Fig. 2.17 provides additional galvanic isolation of the converter with negligible losses. Nevertheless, the complete protection strategy is missing, and the technology requires development and a validations, which are not in the scope of research from this work.

The fault detection strategy and the (coordinated) control system lead the protection performance in the converter [111]. Isolated power converters with bidirectional current control are being utilized for fault isolation (using the switches to handle the fault current) [25, 26, 37]. Additional transistors can be placed as part of the power converters to increase the protection performance and reduce losses during steady-state operation [112]. Those designs result in converters with increased complexity compared to breaker-based protection [26]. However, the complete protection solution should have less complexity and more volumetric power density than the breaker-based system [5, 65].

The dual-active bridge converter (DAB) and the MMC are commonly researched topologies to use in DC-DC protection and fault-tolerant DC power grids for different applications (including onboard DC power grids) [26, 28, 113–119].

Both converters have a flexible design process, extensive development background, controllable bidirectional power flow, galvanic isolation and modular capabilities. Both the DAB and the MMC have benefits and challenges. Both converters can be downsized by adjusting the switching frequency but are susceptible to thermal management issues and control complexity [26, 28, 119].

Scholars are working on improving different characteristics in breakerless systems. For instance, the DC bus capacitor discharge is proposed in [49] to enhance the selectivity of the protection system. A capacitor filtering approach is explored in [65], for line-to-line short circuit detection in residential bipolar DC grids. Modifications of the DAB are investigated in [56] to obtain highly efficient energy conversion and bidirectional fault handling. The installation of energy storage embedded in a MMC is simulated in [120] to enhance bidirectional fault isolation. The work in [121] shows a diagnosis strategy used to improve the efficiency and reliability of the DAB.

Furthermore, the performance assessment in [122] shows a diagnosis strategy used to enhance the efficiency and reliability of the DAB, the performance assessment in [123] compares the DAB and an isolated MMC for breakerless protection with experimental validation. The generator side protection is studied in[29], assessing the time response in a simulated voltage source converter.

Currently, breakerless system protection in the use case of onboard power grids is scarce. Identification of a commercial solution has not been possible, suggesting that the development of the system is falling behind. In addition, the reported implementations include laboratory setups or demonstrators, where the proof of concept (fault isolation) occurs under power and voltage-downscaled environments. The power and voltage scaling-up process relies on parallel module implementations, which also needs a complete testing process in experimental facilities [26].

2.3.7. Analysis and comparison

Breaker-based and power electronics-based protection have several features and challenges discussed in this section. Table 2.6 includes a simplified summary of the main characteristics as an overview to facilitate the comparison. This section investigates some relevant characteristics to visualize the current status of the technologies.

Several features and challenges of the breaker-based and power electronics-based protection are discussed in [5, 37, 64, 73, 125], basing the discussion on the premise of an available zonal distribution architecture. The development of protection architectures in this context is not realistic because of the limited number of vessels featuring that architecture. The survivability and reconfiguration options depend mostly on the distribution architecture, not the protection architecture. A definition of protection features in the framework of architecture may not be applicable in current use cases. Hence, the massive adoption of the zonal distribution architecture is essential to validate the studies. Nevertheless, current works provide important contributions into the field that should not be disregarded despite the limitations.

The scope of other works, such as [26, 54, 65, 66], have a more realistic use case definition by proposing the radial architecture, partially aligned with the information shown by ABB [41] and Wärsilä [50]. The survivability and reconfiguration limitations are considerable challenges that require more engagement, and the protection system should contribute in their mitigation. An adaptation closer to a ring architecture or the double feeding of sensitive loads could partially mitigate some limitations of the radial architecture. Which can also enhance the performance of the protection system or reduce their complexity.

The diversification of the architecture options (distribution and protection) is a significant challenge in the context of protection systems. An integral approach is missing, considering both technologies without the current bias in favor of the breaker-based protective architecture. Having a common framework for distribution and protection architectures may be useful for multiple applications in the shipping industry, potentially easing the iterative process of defining protection strategies,

Table 2.6: Protection architecture comparison for breaker-based and power electronics-based systems.

Breaker-based	**Power electronics-based**
• Relieve the power converters of fault location and current limiting functionalities [5].	• Voltage transformation, galvanic isolation and current limiting are handled directly by the power converters [5, 37, 64, 73].
• Reduction of converter complexity and communications requirements compared to the breakerless architecture [64].	• Fault detection and location methods are embedded in the power converter acting as load feeders [73].
• Current limiting, fault isolation and galvanic isolation are achieved by using external SSCBs and HCB[5, 64].	• Current limiting can be used to inhibit the effect of line-line, line-ground, and line-line-ground short circuits [5, 64].
• Preferred for high survivability because of the distributed approach of the protection devices [73].	• Distributed communications among the generator, the energy storage and the switches are required for coordination and fault isolation [5].
• Different algorithms can be deployed to detect and locate faults [61, 73].	• Low impedance faults are also handled by the power converters by controlling and blocking the current flow into the system [5].
• Snubbers and filters are embedded in the device to improve the transient response of SSCB and switches [73].	• Expected to have relatively lower risk and cost than the breaker-based architectures (fewer multi-functional components) [64].
• Adequate for high peak current mitigation coming from a fast discharging DC bus capacitor [37].	• High power density compared to the breaker-based architecture, fewer components and embedded functions could enable this feature [37, 64].
• Multiple types and architectures of SSCB and HCBs are used for unidirectional and bidirectional current limitation, and fault isolation [5].	• Support for digitalization-related functionalities and prediction or aging models.
• The technology readiness level (TRL) of MVDC HCBs and SSCBs is considered low at the time of this writing [5, 25, 124].	• Conduction losses from SSCB are removed, better efficiency than breaker-based protection is therefore expected.
• Relatively established market with availability of commercial products	• Product and market on development, no commercially available options.

protection requirements and devices while designing the primary distribution system.

In protection systems, most of the research efforts are focused on fault detection, location and prediction algorithms and mechanical, hybrid and solid-state circuit breakers. Several fault detection and localization methods are compared in [25, 26, 60], such as active impedance estimation, traveling waves, neural networks, and wavelets. Noise pattern analysis is investigated in [126] to detect pole-to-ground short circuits. The directional protection algorithm in [127] uses the current direction for detection purposes. Furthermore, extensive work is done on instrumentation, algorithms and devices to improve the speed and sensitivity of detection [26, 54, 66]. The variety of techniques under investigation shows significant interest in the topic. Nevertheless, the detection algorithms usually require assumptions of ideal protection devices to enable real-time operation.

Furthermore, the circuit breakers technologies are still under development, especially for MVDC. The MCBs have a slow dynamic response, SSCBs have conduction losses, and the HCBs still have a slow dynamic response for the requirements.

The evolution of solutions using power electronics-based protection is delayed upon the arguments of expensive development and low performance with little evidence and business decisions. In the future, empirical evidence about power electronics-based protection performance is expected. A benchmark against breaker-based protection is required to conclude whether the efficiency and response time limitations are surpassed.

2.4. Power scalability in Shipboard DC systems

After considering the emerging challenges for shipboard DC systems in Sections 2.2 and 2.3, identifying implementation obstacles for real applications is of primary importance for the mass adoption of DC systems. For instance, the power levels of different ships diversify among applications, the power level for different ships varies greatly among applications, from 40 kW to 190 MW. However, most of the semiconductors utilized for power converters can withstand a fraction of that power, making power scalability essential. Usually, ship manufacturers harness COTS converters for simplicity, making compromises on performance and volumetric power density. This section explores the power requirements for the propulsion of different vessels and the misuse of COTS converters in shipboard power systems. A discussion about modular power converters and PEBB is also present for power scalability, with an overview of benefits and challenges. A design challenges analysis for modular converters placed in the PEBB framework finalizes this section.

2.4.1. Power levels in ship applications

In most applications, propulsion power is the highest load on the ship. Thus, propulsion power is a reference of the total power level, except for cruise ships and large warships, in which the hotel and other loads are higher [5]. The use of electrical propulsion (EP), hybrid propulsion (HP) and mechanical propulsion (MP) is application-specific. When considering the same application, EP ships have the

largest electric power systems, followed by HP vessels and MP ships. This review focuses on EP vessels as power converter scalability is critical for such vessels.

The information summarized in Table 2.7 includes an estimated range of propulsion power for different applications in contexts with the propulsion architecture. The information of propulsion power was extracted from [5, 41, 50, 128–130], and the references for propulsion architecture are [4, 6, 10, 131–135].

From Table 2.7 it is visible that multiple applications use EP and HP in standard operation. Sensitive applications, such as drilling vessels and cable layers, require additional thrusters to improve maneuverability, usually by using EP. Electric motors can provide full torque at low speeds and better controllability than ICE, which is desirable for those applications [4]. It is also visible in Table 2.7 that the power levels for the different applications are broad, increasing the challenges for scalability in DC systems.

2.4.2. Commercial off-the-shelf solutions

Power scalability challenges for power converters are especially relevant for shipboard DC systems. Manufacturers rely on mature and closed COTS converters mainly because they can obtain reliable performance and robust components and systems. However, these components are not necessarily designed for shipboard applications nor tailored for the specific application, possibly compromising volumetric power density and efficiency and limiting modularity and maintenance schemes. In addition, the deficit of valuable information about the equipment can affect the control design and the energy management strategies, possibly limiting the performance. For that reason, closed systems enforce additional tests for control design and certification [38–40].

A blackbox strategy is indicated in [38] to foresee the dynamic response of COTS converters for integrated power systems on ships. A similar method is investigated in [39], extended with parameter-varying transfer functions to account for severe nonlinearities in COTS converter characterization for DC microgrids. And the work in [40] shows the frequency deviation of a COTS uninterruptible power supply for ship applications for electromagnetic interference certification. The referenced investigations point out the convenience of COTS converters for easy integration and agree on the imposed challenge of additional assessments required to identify the dynamic performance of the components.

The COTS converters for shipboard DC systems mentioned by ABB, Siemens, and Danfoss are complete ecosystems provided by the manufacturers. In such products, the components are closed and protected, the interoperability is not guaranteed, the backward compatibility is explicitly limited, and the modularity is restrictive to their family of products [41, 136, 137]. The design standardization and regulation issues discussed in Section 2.2 are also contributing factors. The detailed information about closed systems from major manufacturers is difficult to obtain and the integration flexibility of their products is not always clear. Hence, the system design has constraints linked to technical limitations already surpassed in other applications (e.g., inland LVDC grids).

Table 2.7: Propulsion type and power for different vessels.

Ship type	Power train	Propulsion power (MW)
Ferries	EP, HP	0.04-40
Tugs	EP, HP	0.5-2.5
Fishing	EP, HP, MP	0.2-6
Yachts	EP, HP, MP	1-19.2
Cruise ships	EP	20-60
Drilling Vessels	EP	18-25
Cable layers	EP	13.4-22
Icebreakers	EP	4.3-18
Offshore vessels	HP	1-10
Cargo ships	HP, MP	5-100
Inland cargo	EP, HP	2-5
Tankers	HP, MP	3-50
Dredging vessels	HP, MP	4-22.5
Naval frigates	HP	36-40
Naval destroyers	HP	40-75
Capital naval vessels	EP	72-190

2.4.3. Modular power converters

As an alternative to the COTS converters, modular power converters are advantageous to reach the power level of generators, motors, and high-power loads in different vessels without losing functionalities. Shipboard DC systems require converters for rectification, propulsion, energy storage integration, load supply and bus interfaces. Several benefits and challenges are present in various modular converter topologies utilized for multiple purposes within the DC system. Table 2.8 shows a characteristics summary for the most relevant converters.

Table 2.8: Definitions of modular power converters for shipboard DC systems [5, 8, 25, 28, 32, 36].

Application	Configuration	Benefits	Challenges
Three-phase generator	MMC rectifier [24]	• Suitable for MVDC applications • Voltage scalability • High efficiency	• Unnecessarily complex • Extensive development process
Multi-phase generator	• Multi-pulse parallel rectifier [24]	• All rectifiers rated at the full DC side voltage • Current is divided by the number of rectifiers • Natural redundant configuration	• It might require series semiconductor devices to reach the voltage requirements • Series switches and snubbers require voltage balance circuits
	• Multi-pulse series rectifier [24]	• Reduce the voltage requirements for the semiconductors and the rectifiers • Flexible for voltage class selection	• The rated current flows through each of the rectifiers • It might require to balance the voltage amongst the rectifiers
Three-phase AC machines	• Neutral point clamped inverter (three-level) [8, 32]	• Reduced semiconductor stress • Enhanced power quality • Fault tolerance capabilities • Suitable for high-power propulsion • Modular and scalable	• Asymmetrical losses distribution • Uneven heat dissipation • Lacks efficiency when the input voltage is low • Extensive development process
	• MMC inverter [8, 32]		

Continue on next page ...

Application	Configuration	Benefits	Challenges
MVDC-LVDC interfaces	• Input series output parallel DAB [8]	• High power density	• Low fault current controllability
		• Scalability for high-power interfaces	• Power balance is required to suppress the circulating current
	• Input parallel output parallel DAB [5, 32]	• High power density	• Asymmetrical current distribution
		• Scalability for high-power interfaces	• Controllability limitations when having several power converters
		• Fault tolerance capabilities	
	• Neutral point clamped based DC-DC [8, 32]	• Reduced voltage stress	• Increased current stress for high-power MVDC applications
		• Enhanced power quality	• Uneven heat dissipation
		• Reduced electromagnetic interference	
	• MMC DC-DC [8, 32]	• Fault tolerance capabilities	• Reduced number of submodules can affect the performance for shipboard applications
		• Simplified maintenance requirements	• Capacitor voltage balance and circulating current among submodules is a major challenge
		• Modular and scalable	

From Table 2.8, it is clear that MMC converters have the flexibility to operate in different parts of the power system. However, the extent of the benefits is constrained by the vessel application, given that the voltage and power levels are variable within a wide range, compromising the power density, fault tolerance and the feasibility of such converters for the extensive development process. For multi-phase generators, the arrays of multi-pulse rectifiers are preferred instead of MMC rectifiers because of their simplicity and power density [24]. The array configurations can fulfill the design requirements, providing the proper power balance functionalities for the semiconductors and voltage balance for the rectifiers.

The DAB arrays can offer flexible solutions for a wide range of ship applications, providing the control strategy that allows power balance while reducing the circulating current, a wide soft-switching operation range for the semiconductors, and avoiding transformer saturation [138, 139]. Nevertheless, series input DAB configurations require controllability improvements for fault currents that affect the dynamic response of the converter. Furthermore, parallel DAB can suffer from controllability issues when using a high number of modules to scale up power, creating power unbalances and circulating currents.

Some modifications of the neutral point clamped converters are candidates for relatively low-power MVDC-LVDC interfaces and propulsion. The active version of such converters is mentioned in [8] and can be used to compensate for the asymmetrical heat dissipation, increasing the converter complexity and the control scheme.

2.4.4. Power electronics building blocks

First introduced by the office of the U.S. Office of Naval Research, the PEBB is a generic framework to include semiconductors, gate drivers, signal conditioning, communications, controllers, filters, sensors, protection, and thermal management into standard scalable blocks to achieve high-power converters [5, 32, 140, 141].

Power levels on ships can vary from less than one MW to hundreds of MW (see Table 2.7); AC bus voltage from 690 V up to 11 kV [36]; and DC bus voltage from 700 V to 6 kV [36, 46], for commercially available converters, higher levels can be achieved in the future [5]. The outcome of PEBB, in theory, is cost reduction, improved reliability, and reduction in design and operation complexity within those operation ranges. Moreover, the product development and maintenance processes can be simplified as well [32, 140–142].

Furthermore, recent works point out that the use of PEBBs presents limits on power density, especially for ship power grids due to discrete components and the power density of silicon IGBTs. Several scholars propose the integrated PEBBs based on SiC MOSFETs and integrated multi-purpose substrates as a solution [143–145]. Such technology could provide volume and weight reductions [143], and further development is necessary to assess its feasibility and TRL improvement to ease mass adoption.

The simplified architecture depicted in Fig. 2.18 includes the modules required in general for a PEBB based on the DAB converter. The generic architecture features the power switches packed in half-bridge or H-bridge disposition, the gate drivers,

the control and sensors units capable of locally controlling power and temperature, and the passive components [142].

The external power supply placed for the gate drivers is not only a consideration of redundancy and reliability but also a matter of safety. It is fundamental for the proper operation of the PEBB that the gate drivers are always powered before the power stage to avoid incidents led by controller unavailability [140, 142].

The start-up and the connection with charged power stages procedures require closed-loop control for correct operation. During start-up, the voltage builds up from zero, and an activation delay in the drivers and controllers is necessary for transient

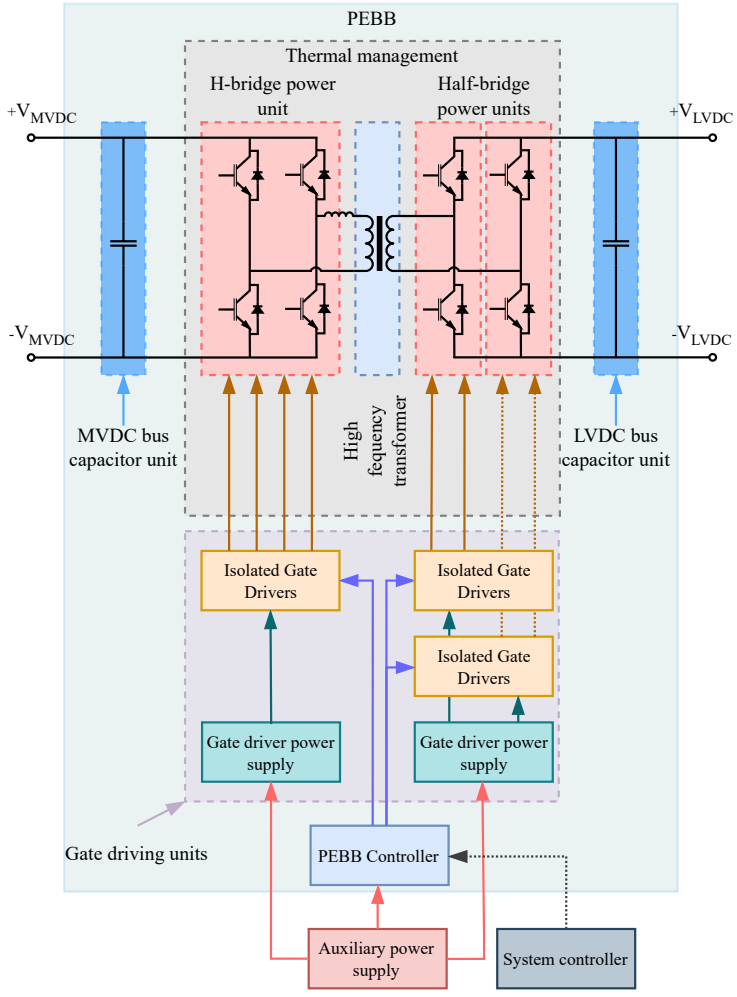


Figure 2.18: Concept architecture of PEBB for a DAB DC-DC converter.

protection [141, 142]. The charged stages connection requires voltage balance to avoid circulating current and voltage dips. Finally, the PEBB coupled to the system controller allows the integration into the power grid and the interaction with other PEBB modules, providing the proper control and communication architectures [146].

2.4.5. Design obstacles

When considering series and parallel arrays and modular power converters, any variation of the device characteristics, naming module, gate driver, circuit impedance, filter, or cooling solution can cause asymmetrical power distribution, which also increases with power [36]. The remaining of this section includes an overview of the following obstacles 1) Voltage balance and circulating current, 2) Thermal management, and 3) emerging challenges to overcome.

Voltage balance and circulating current

Parallel connected converters and modules can present circulating current when the operation point or utilized components (with their intrinsic features) are slightly different. Hence, additional circuits for balance and control compensations are required [5]. In addition, controlling multiple parallel converters can become challenging, potentially compromising their dynamic response within the system.

For series-connected converters, the current flows through all the converters avoiding circulating currents. In this case, the voltage can be different for the converters and an advanced modulation strategy, e.g., sorting algorithms in MMC, and a voltage balance, with the proper control strategy, is mandatory [24].

In MMCs, both series and parallel modules can be present. Cascaded modules create series configurations with a potential voltage unbalance. In that case, the capacitors of the modules will cause a circulating current among the modules, increasing the losses [8]. Hence, additional control strategies are required to perform compensations. The intra-arm voltage balancing control, the capacitor voltage balancing controller, the circulating current elimination control, and the circulating current injection controller are a few of the preferred strategies. The added control strategy must operate in addition to the regular controller to mitigate the unbalance and circulating currents, thus increasing the system complexity [147, 148].

In practice, no converter is equal to others, parameter variations are unavoidable, and integrated solutions for circulating current for parallel modules and voltage balance for series modules are required. In order to exploit the advantages of modular converters, those solutions should be placed at the circuit and the control level. Furthermore, PEBBs approach the modular power converter concepts from an integral perspective. Therein, it is advisable to use the component screening method to match the parasitic elements of the parallel PEBBs, i.e., to provide means to equalize the on-state characteristics of semiconductors and passive elements. However, the suppliers providing the screening services will most likely increase the cost of the components when considering off-shelf devices, but this will be relative to the purchase volume of each item.

Thermal management

Thermal management in shipboard power converters and PEBB is considered essential and challenging. For instance, the high-power requirement in a relatively power-dense converter can dissipate a considerable amount of heat despite the converter efficiency [33]. The *thermal management* zone in Fig. 2.18 aims to highlight the components inside the PEBB that dissipate more heat, where the effect of thermal management is critical.

Traditional cooling strategies employed in shipboard PEBB include heat sinks, heat pipes and liquid cooling. The work in [149] thoroughly discusses different cooling approaches. Therein, most techniques are not currently applicable for shipboard PEBBs, given the distinctive operation and environmental requirements for those systems, along with maintenance complexity and safety concerns [33].

- For the heat sinks, forced air-cooling is feasible in shipboard PEBB, and most of the heat is removed by convection [149]. The humidity and air saltiness conditions constraint the performance of such a solution.
- Direct liquid cooling utilizes flexible hoses inside the PEBB to circulate liquids, such as de-ionized water or dielectric substances, for removing heat[33].
- External liquid cooling harnesses liquid circulation to remove heat from a plate in contact with the PEBB. The same liquid selection for direct cooling is applicable [33, 150].
- Heat pipes employ a contained fluid that evaporates in the presence of heat (evaporation), producing internal pressure changes that move the vapor to the section of the duct that is in contact with a heat sink. The steam is then condensed, causing a pressure change that forces the liquid back into the evaporation section [149].

Both the heat pipes and the liquid cooling solutions can be more compact than a forced-air heat sink, especially in the case of liquid cooling [33]. However, liquid solutions are more complex to design and maintain than heat sinks or heat pipes [149]. Heat pipes, on the other hand, have the flexibility to remove heat from components located in different places, which is not the case for the simple forced-air heat sink. Nevertheless, both technologies are frequently combined to enhance cooling performance. Depending on the sizing (power and voltage), the PEBB can rely on one or another thermal solution, and the approach of a more complex solution needs to be justified.

Challenges to overcome

The framework of power electronics for shipboard DC systems is complex, where voltage and power scalability are challenges during development. For instance, the power ratings of power semiconductors are limited, and highly complex converters are expensive and difficult to maintain. Current solutions utilize COTS converters,

which can limit the system capabilities, especially regarding volumetric power density, specific power and dynamic response.

Framing the development of power converters within the PEBB concept could accelerate the acceptance of newly developed technology. However, the process is also complex and extensive, and an approach based on high TRL designs could accelerate the development while reaching the performance and power level requirements.

In addition, the switchboard approach can also affect the cooling solution available for the power converters. The liquid cooling utilized in some centralized switchboards may become unsuitable for distributed systems as the cooling circuit is centralized. The addition of liquid cooling components into the building blocks may affect their form factor and reliability. Consequently, the distributed switchboard approach requires an extensive development of the cooling solution for the PEBBs.

2.5. Outlook and Conclusion

Shipboard DC systems have remarkable properties that make them suitable replacements for the current AC systems. In doing so, many opportunities will be available to possibly contribute to meet emissions targets in the maritime sector. Enhanced volumetric power density and controllability are part of the value promise of DC systems. Additional to the flexible engine operation, modular integration of DC sources and storage, and potential reduction of conversion stages. This chapter introduces a critical overview of the missing developments in primary distribution, DC protection and power scalability. By addressing all the identified gaps, shipboard DC systems can become safer and more robust, easing the technology acceptance. The main topics addressed in this chapter are listed in the followings:

2.5.1. Primary Distribution

The selection of unipolar or bipolar bus architectures affects the protection design. For instance, the voltage balance converter becomes critical for protection in bipolar systems. The unipolar system has fewer protection zone reconfiguration options, which demands better protection performance. The definition of a distributed or centralized switchboard concerns the entire distribution system, including protection architecture. The effect of this decision-making process is not well-studied in the literature. The opinion from the industry is divergent, and further studies are necessary to improve the regulation and the design process shortly.

The use case studied in this chapter suggests that the power density of the primary system in a superyacht could increase substantially in the distributed switchboard. The results also show a reduction in the cabling losses, which varies with the operation mode of the vessel. Additional benefits of the distributed switchboard regarding electromagnetic interference and layout flexibility are possible. Such advantages require further investigation to quantify the benefit for the use case and other use cases. Despite the positive results, additional challenges for the distributed disposition require identification and solving processes. For instance, the

required cooling solution modification needs to be investigated as part of the research to adopt the distributed approach.

Fault-propagation studies and protection coordination guidelines can support a future common framework for system design. The fault-propagation characterization can help to rewrite the protection requirements to obtain a more suitable solution for the DC technology. The basis of testing and validation stages requires further investigation for DC technology, given that fundamental concepts regarding fault propagation and protection are missing. Consequently, the basics of DC system design come from AC systems, which can compromise reliability, safety or efficiency.

2.5.2. DC Protection

In breaker-based protection, MCBs have considerably low losses and slow response. Solid-state devices have a fast response but relatively high losses. Hybrid breakers are quicker than MCB and more efficient than SSCB but noticeably slow for shipboard applications. Hence, multiple research efforts focus on lossless solid-state and faster hybrid technologies, while other protection devices, less reliant on the circuit breaker performance, are frequently disregarded. The power electronics-based protection investigated in this chapter can be appropriate to overcome some of the performance limitations of the DC breaker technology. Additional benefits regarding volumetric power density and system complexity are possible, enforcing the motivation for its development.

As the power electronics-based protection technology requires further development, some technical limitations require identification. However, a protection system based on well-known, reliable power converter topologies can ease the development cycle, and a rapid transition from a prototype to a product could be possible. Despite the limited access to marine-certified solid-state protection components, this investigation provides a theoretical background valuable for DC protection systems development. The analysis covers the advantages of the considered technologies, the key challenges to overcome in their development, and their operating principle.

2.5.3. Power scalability

Matching voltage and power levels in DC systems is challenging for the maritime sector. The high power and mobility preconditions force shipyards into making fast and practical decisions, frequently resulting in misused and oversized COTS converters. Meanwhile, the acceptance of PEBBs is growing, creating a diversity of products that might reshape the future of DC technology. However, some major ship manufacturers can still prefer a solution provided by reputed converter vendors, such as ABB, Siemens and Danfoss.

It is unclear whether shipyards or COTS converters manufacturers will adopt the PEBBs for DC systems in the future. However, by utilizing a power scalability scheme based on PEBBs, it is possible to overcome some limitations of COTS converters in shipboard DC systems, especially regarding volumetric power density and system

characterization, which is nonexistent in closed product families. In addition, the development of power electronics-based protection within the framework of PEBB could enable cost-effective power scalability while maintaining protective properties. Such a product could be advantageous for multiple applications in the section, potentially increasing their value in the future.

This research highlights some of the most urgent challenges of shipboard DC PEBB development as a suitable candidate for modular shipboard DC systems. The scalable architecture of the building block requires voltage balance and circulating current countermeasures to ensure efficiency. A proper thermal management concept will ensure the efficient operation of the building block for different switchboard concepts. The form factor of the PEBB may require adjustments to comply with the requirements of ship designers. By addressing those challenges, the massive implementation of shipboard DC systems could take a step forward into becoming a reality.

3

Short Circuit categorization

The protection of DC systems in mobility applications, such as land transport, aircraft, and shipping, presents significant challenges due to the need for high power density equipment in confined spaces. This chapter focuses on DC systems on board ships, for which diverse applications require different power levels, architectures, and protection strategies. Existing protection frameworks and regulations are often inadequate or outdated for the field, leading to certification issues and insufficient fault analysis. This research proposes a use case-based categorization of short circuit currents for primary systems. A reference scenario is created using a simulation model of a 5 MW system in a superyacht to provide a short circuit inventory. The study proposes three contributions. A comprehensive fault inventory, a qualitative categorization, and relevant recommendations for power converter design. The research highlights the importance of fault categorization in understanding the impact of various short circuits on shipboard DC systems. The study emphasizes the importance of the evolution of materials and power converters in developing efficient protection technologies for ships. This work addresses some fundamental gaps in shipboard DC systems, providing a foundation for improved protection strategies and regulations, ultimately contributing to the advancement of protection of shipboard DC systems.

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3

Photo by Joshua J. Cotten on Unsplash

Arapaima or Pirarucu, the king of the Amazon River, glides through its waters with a quiet dominance, reaching lengths of up to four and a half meters. As one of the largest freshwater predators in the world, it shapes the aquatic ecosystem, its movements both commanding and essential, a living testament to the power and mystery of the river it calls home.

3.1. Background

Protection of DC systems has proven to be a challenging enterprise when considering mobility applications. Several sectors, such as land transportation, aircraft electrification, and shipping, require a relatively large amount of power in a compact volume [135, 140, 151]. For example, a Scania heavy duty full electric truck has a traction power ranging from 270 kW to 450 kW. Meanwhile, inland cargo ships, which have electric propulsion, require 2 MW to 5 MW [36, 135]. These electric systems may feature a DC microgrid, which inherently have a relatively low impedance characteristic between power sources and loads.

A primary obstacle to the widespread adoption of these systems is the lack of a clear understanding of fault behavior and a standardized framework for assessing fault severity. Energy storage systems, such as batteries and filter capacitors, can amplify the effect of a short-circuit, yet state-of-the-art DC ships lack effective fault analysis and protection technologies [5, 152]. Existing protection frameworks for other domains [46, 89] are not entirely suitable, and a comprehensive categorization of faults for onboard primary DC systems is missing.

The core contribution of this work is to address this gap by providing a use case-driven analysis and categorization of short-circuit currents in shipboard DC systems. This chapter presents a fault inventory and a severity-based categorization derived from a simulation model of a 5 MW primary DC system for a superyacht similar to Fig. 3.1. The system features a distributed architecture with converters close to loads and generators and DC distribution lines. The categorization simplifies the assessment of faults, which is critical for the design phase and for decision-making during real-life events. The key outcomes of this research are:

This work has four main takeouts that could enhance the design of safe and fault-tolerant DC systems on board.

1. A fault inventory that provides a clear understanding of pole-to-pole fault current behavior, representing a worst-case scenario.

2. A severity-based categorization of these faults to facilitate risk assessment and inform system design.

3. A foundation for enhancing DC ship regulations by generalizing the fault impact.

4. Insights that can guide the design of more robust power converters by quantifying potential threats

This research covers pole-to-pole (type-A) short circuits in shipboard DC systems, as these events potentially have the most destructive consequences [153]. Since generic DC systems are dependent on power electronics, severe overcurrent can become catastrophic for their power switches [62, 153]. Other types of faults, such as open circuit, pole-to-ground (type-B) and pole-to-pole-to-ground (type-C) short circuits, are beyond the scope of this document. The terms type-A fault, event, short circuit current, and pole-to-pole short circuit are used interchangeably throughout the text. Open circuit faults generally occur in generator feeders and

Figure 3.1: Referential case study for shipboard DC systems. Moonrise superyacht manufactured by Feadship in 2022. Credit to Feadship [online] https://www.feadship.nl/.

have a limited overcurrent due to power drives [153]. Type-B and type-C faults depend on the grounding of the system [58, 154], which makes it difficult to conduct a representative study. However, the literature suggests that type-B faults are less problematic than type-A, as primary shipboard DC systems frequently feature a floating ground [26]. Depending on the grounding scheme, type-C events can become similar to type-A, which highlights the relevance of the latter.

Energy storage devices (e.g., batteries) in large vessels are typically connected to DC bus bars through a DC-DC converter. Therefore, filter capacitors govern the fault current in pole-to-pole short circuits. The low impedance of DC systems and the capacitor energy facilitate a high current build-up with minimum time constants [5, 53]. The fault current from AC sources and freewheeling diodes could represent a relatively lower threat to the system. The diodes have conducting resistance that could dampen the fault despite their potential permanent damage [26]. Furthermore, the fault current coming from batteries is beyond the scope of this research because, since they require DC-DC converters operating in current control mode to impose the charging profiles, a current limiting feature would be naturally imposed that restricts the influence of the battery energy capacity to a bus fault. Furthermore, faults between the battery and the DC-DC converter are typically resolved within a few µs resulting in only a small dynamic influence of the DC-bus of the ship. The fault current from capacitors, batteries, and AC sources and their current characteristics are further discussed in [58].

The analysis and waveform estimation of the fault current in shipboard DC systems is challenging. Standard recommendations such as [155] describe the current from different sources, proposing independent solutions for the calculations of

rise and decay. However, they cannot accurately predict fault currents for several feeders in parallel and are focused only on AC systems. The voltage drops in a converter-controlled low voltage DC grid with fuse protection are investigated in [156]. The work shows several tests with various fuses and assesses the protection performance in a bipolar system, which is uncommon in shipping. The study also covers two-location fault testing using RL transmission lines. However, the purpose of their research diverges from maritime applications, especially in relation to primary distribution. Consequently, the potential energy of the capacitors and the characteristics of the power (300 W) and voltage (380 V) do not allow for an appropriate comparison.

The lack of a cost-effective solution for DC protection in maritime applications hinders their adoption in general. Mechanical DC circuit breakers have slow response times and minimal losses. Solid-state counterparts exhibit acceptable response times but high losses, whereas hybrid circuit breakers do not have significant differences from the other cases [53, 58, 127]. Therefore, solid-state circuit breakers in shipboard DC systems serve regularly as bus-tie switches (BTS), especially for highly demanding applications, such as offshore supply vessels and cable layers. Until now, fuses have still been preferred for the protection and galvanic isolation of faulty feeders on DC ships, despite their limitations in response time and extensive replacement period [49].

State-of-the-art protection technologies are not sufficiently developed to satisfy the high demands of the shipping industry. Consequently, the evolution of materials and power converters should lead to improved and efficient protection technologies. This chapter aims to provide insight into the characteristics of different short circuit currents, giving an integrated perspective on design, regulation, and diagnosis. Therefore, the numerical model incorporates fuse-based protection strategies to assess their performance. For this purpose, a simple method that facilitates the process and its repeatability is necessary. This research employs a six-step approach, susceptible to iteration in all steps as follows.

1. **System information collection:** Baseline definition of the primary shipboard DC system under study. The main parameters come as input from an existing vessel, so a relatively realistic scenario is taken into account. However, significant modifications are necessary to adapt the specifications to the numerical model.

2. **System modeling:** Development of a model in alignment with the purpose of the simulation considering distribution architecture, cabling, loads, and protection components. The she sampling period, the discretization method, the solver, the simulation time, the initial conditions, and the type of model per component are defined.

3. **Test case definition:** The definition of scenarios implies decisions about the operation modes that affect the initial conditions and loads. The location of the short circuits and the protection mechanisms complement the decision-making process.

4. **Simulation and results analysis:** Execution of simulations and individual confirmation of success for all relevant scenarios. Characterization and analysis of key parameters, such as peak current, specific energy, and absorbed energy, for relevant test cases.

5. **Performance analysis:** Performance comparison of state-of-the-art protection approaches based on peak current, average current-rate variation, absorbed energy, and peak power estimation for critical test cases.

6. **Fault categorization:** Fault categorization definition based on qualitative criteria. The fault severity indicates the category, which also considers detection speed, localization complexity, and potential consequences.

The structure of this document corresponds to the method listed in the following outline. Section 3.2 shows a detailed description of the simulation model (Steps 1 and 2). Section 3.3 summarizes the test cases in the study (step 3). Section 3.4 presents the fault inventory, comparing three relevant protection strategies, fault characteristics, and a sensitivity analysis of the cabling inductance (step 4). Section 3.5 focuses on the protection performance benchmark studying critical test cases and potential consequences (Step 5). Section 3.6 includes the fault categorization (step 6). Finally, Section 3.7 summarizes the main conclusions of the work and prospects for future research.

3.2. System description

This section aims to describe the different components of the model and detail the main assumptions and limitations. Fig. 3.2 illustrates the primary distribution system of a referential superyacht using a DC system. The system has a dual bus radial configuration integrated via a single BTS. There are six power supply feeders, four of which are generators, and two include energy storage. Furthermore, two load zones *(blue dots)* or load feeders integrate propulsion and hotel loads into the DC system. The green shade in Fig. 3.2 represents the switchboard and indicates that all components within are located close together. The remaining drives are located close to the generators and loads and at a certain distance from the switchboard in a distributed architecture, as discussed in [8, 36]. Weight and volume reductions and flexible component positioning are possible with distributed architectures [5]. The feasibility of distributed DC ships onboard could be improved by analyzing their protection demands.

Transient and steady-state analyses are necessary for fault current characterization in a DC circuit. The following subsections present the model segments intended for the simulation of the DC system as follows.

1. Load and supply feeders
2. Fuses
3. Bus-tie switch

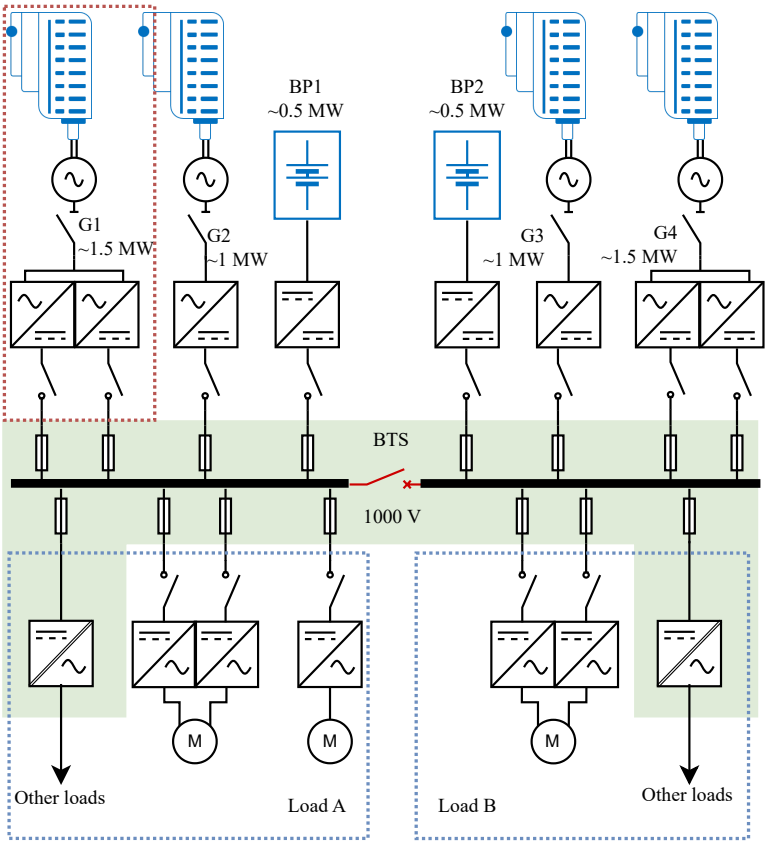

Figure 3.2: Referential case study for shipboard DC systems. Primary shipboard DC system, suitable for the superyacht. *Red dots: Components placed close together, blue dots: load zones, green shade: switchboard components placed close together*.

4. Short circuit branch
5. Summary of parameters

3.2.1. Load and supply feeders

Since the DC system (see Fig. 3.2) has six supply feeders and two load zones, two general types of circuit are used in the modeling. The power supply feeder shown in Fig. 3.3a and the load zone feeder depicted in Fig. 3.3b. The supply feeders in this work are of three types. 1) Primary generators (G1 and G4), 2) secondary generators (G2 and G3), and 3) battery packs (BP1 and BP2). The main difference among the types is the number of output filters and the cable count, which also depends on the number of circuits.

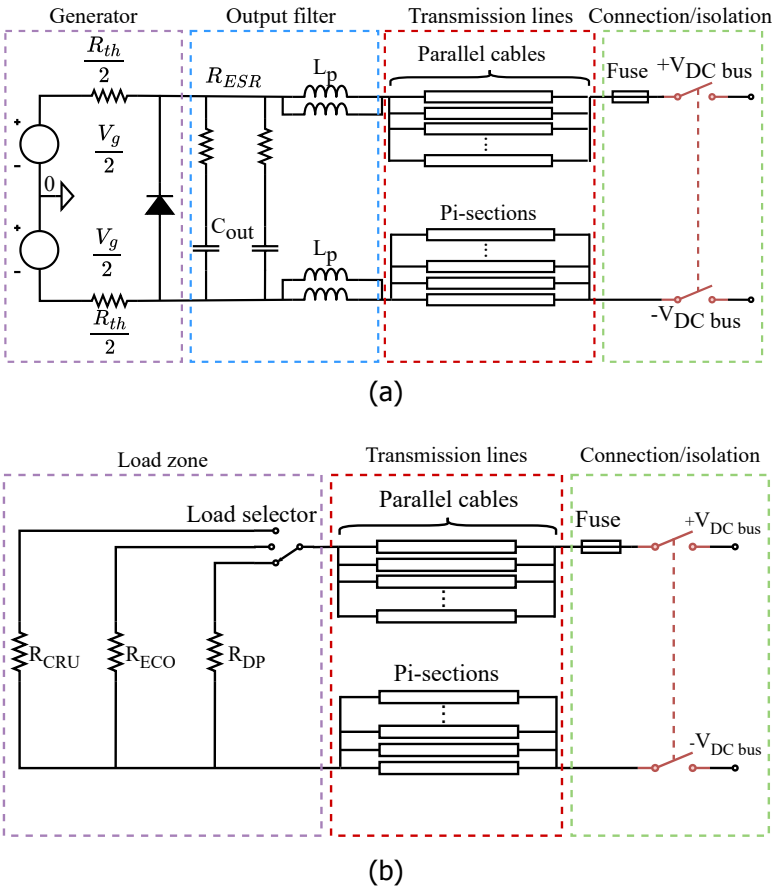

Figure 3.3: Schematic diagram of the modeled power supply feeders and load zones. (a) Feeder circuit for the main generator. (b) equivalent circuit of a load zone. *Purple dash: generator, load, blue dash: output filter, red dash: parallel transmission lines, green dash: bus coupling point, disconnector and fuse*.

For example, generators G1 and G4 utilize two converter drives as in Fig. 3.3a, generators G2 and G3 require one converter drive, and battery packs BP1 and BP2 have three output filters for a single drive. Table 3.1 summarizes the cable count per component and the number of circuits.

The following components in Fig. 3.3 describe the circuits in the model.

1. Sources
2. Output filters
3. Transmission lines

Table 3.1: Cabling arrangement per main component in the DC system based on 1 kV class DC cables according to [49].

Component	Cables per line	Circuits
Generators G1& 4	8	2
Generators G2 & 3	9	1
Battery packs BP1&BP2	9	1
Load zones A & B	9	2

4. Load

Sources

Modeled with ideal DC sources and equivalent Thevenin resistors (R_{th}) to limit the output power of the source, accounting for the steady-state initial conditions of the fault. The voltage source V_g and the equivalent resistor are divided into two, creating the middle point grounding while keeping the rest of the circuit floating.

Output filters

The original manufacturer of the drive provides data for the output filter capacitors (C_{out}), their equivalent series resistance (ESR), and the parasitic inductances (L_p), which ultimately guide the transient characteristics of the circuit. Such parameters are assumed to be constant for the operation frequency and temperature for this work. The ESR absorbs part of the potential energy, limiting the amount of energy supplied to the fault. The energy absorbed by the ESR depends on the location of the fault within the DC system, and Section 3.4 provides further discussion. In addition, parasitic inductance affects the maximum current and the $^{di}/_{dt}$ of the fault. However, the effect of these inductances is negligible compared with those of the transmission lines.

Transmission lines

The transmission line model incorporates the effects of the cabling impedance in the system model. The Pi model depicted in Fig. 3.4 corresponds to that of the simulation. Cable manufacturers provide parameters R_x, L_x, and C_x, which are mainly dependent on intrinsic characteristics and geometry [51]. For simulation, the parameters extracted come from marine-certified cable catalogs in the range of 1000 V [52].

Load

The load is modeled as a fixed resistor that represents an equivalent power consumption. The initial conditions are assumed constant since load variations in shipboard systems occur in hundreds of milliseconds, whereas short circuit overcurrents

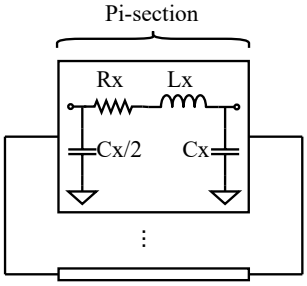

Figure 3.4: Schematic diagram of the pi transmission line segment employed in the model.

happen within several microseconds. Furthermore, the power flow is considered unidirectional and the load does not have an input filter. The effect of additional filter capacitors is discussed in different test cases in Section 3.4 and discussed further in [26], where the input filter can increase the short circuit current in a generator-motor feeder. The influence of load inductance is examined through a sensitivity analysis in Section 3.4. For this research, three operation modes define the values of the load resistors that ultimately impose the initial conditions.

- **DP mode:** The dynamic positioning (DP) mode requires the propulsion systems to maintain the vessel in a relatively static position ($\approx 17\%$ of installed power).
- **ECO mode:** Indicates a reduced speed or economic cruising that maintains optimal fuel consumption ($\approx 25\%$ of installed power).
- **CRU mode:** Refers to the maximum cruising speed for the propulsion system ($\approx 84\%$ of installed power).

3.2.2. Fuse

Fuses are essential in shipboard DC systems to provide the first layer of protection and galvanic isolation [42, 49]. However, the literature rarely reports their behavior in DC cases, and there are no standard methodologies for their modeling. Authors in [156] study voltage dips in a fuse-protected bipolar DC system caused by short circuits. The study includes tests with various fuses in the system without focusing on the behavior of the fuse itself. The work in [157] shows an RC circuit and a variable resistor to model the arcing of a fuse for a DC power supply. The fuse model in [158] uses an algorithm to calculate the RC values while removing the variable resistor. However, the variety of feeders, transmission lines, and parasitic components complicate the tuning of the RC constant in a shipboard DC system. Furthermore, the large capacitors in the output filters dominate the dynamic response of the circuit, allowing the assumption that the fuse capacitors are

negligible in the model. Consequently, the fuse model consists of a variable resistor (arcing resistor) in series with the nominal resistor and a cutoff switch, as depicted in Fig. 3.5.

The reference control structure of the fuse in Fig. 3.5 incorporates a *specific energy* threshold that represents the prearcing. *Specific energy* refers to i^2t and is hereinafter used as the specific energy of the current impulse in $\mathrm{J}\Omega^{-1}$. The fuse blows when the threshold is exceeded (in the datasheet), activating a linearly increasing variable resistor that simulates the arcing of the fuse. The fuse cutoff triggers when the minimum current $i_{\min}$ is reached. Despite the limitations of the fuse models, their behavior gives sufficient insight for complete system simulation.

3.2.3. Bus-tie switch

The BTS or bus coupler exists in various architectures and technologies, and was extensively discussed in [53, 152], providing several components that differ significantly in dynamic response, efficiency, and protection effectiveness. For the simplified model, the component response time is sufficient to provide insight into how low- and high-speed components could affect the fault. Figure 3.6 includes the simple BTS utilized in the model and the simplified control strategy.

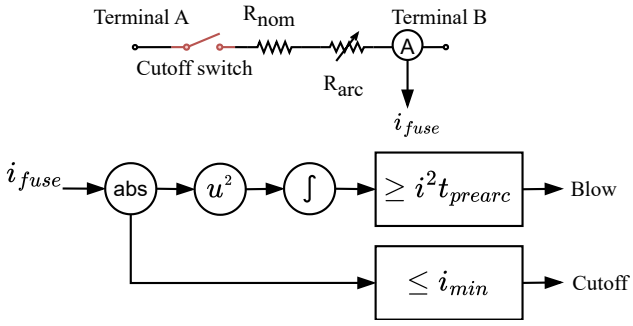

Figure 3.5: Schematic and control diagrams of the modeled fuse.

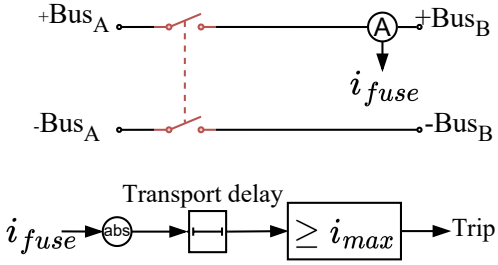

Figure 3.6: Schematic and control diagrams of the bus-tie switch.

The overcurrent threshold i_{max} and the duration of the transport delay define the switch time response that controls the ideal switches. The time response of the BTS follows the typical time response of a mechanical switch with a series fuse, which is around 8 ms [70], and the maximum opening time in a certified solid-state BTS, which is close to 21 µs [80].

3.2.4. Short circuit branch

The generation of faults in the simulation environment requires a short circuit (fault) resistor R_{SC}. The fault resistor is 100 µΩ to represent a solid short circuit. The magnitude differs in more than one order of magnitude from the ESR and load resistors and is about half of the nominal resistance of the fuse. The load resistors R_{DP}, R_{ECO}, and R_{CRU}, and the equivalent source resistors, are on the order of hundreds of milliohms, and the nominal resistance of the fuse is in the hundreds of microohms range. The diagram section in Fig. 3.7 shows how the branch is integrated into the model.

3.2.5. Summary of parameters

The simulation model tools, adjustments and parameters can significantly affect the outcome. The parameters in Table 3.2 facilitate a reasonable analysis and replication, together with the following configurations.

- The system integration utilizes Simulink, and the circuit models the PLECS blockset.
- The Simulink and PLECS configurations use the fixed-step discrete solver at a sampling rate of 10 ns.
- The discretization of the system is based on the fifth-order Runge-Kutta method, as the accuracy for high-speed events is considered better than the second-order Tustin method [159].

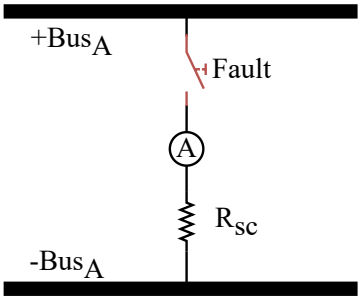

Figure 3.7: Schematic diagram of the pole-to-pole short circuit branch utilized in the model.

- The sampling time of 10 ns satisfies the Nyquist criterion and accounts for most of the aliasing effects.
- The sampling rate is more than 100 times faster than the increase time of a short circuit current of ≈170 kHz for proper transient visualization.
- Algebraic loops and divisions by zero are minimized to facilitate computation and improve accuracy.
- The Pi transmission line model accounts for the effect of RLC parameters in each cable and includes the effects of wave propagation.

3.3. Test cases

A selection of test cases with different variables is necessary to provide a comprehensive testing framework. The variables are operation mode (3), fault location (5), and protection approach (3) for 45 possible test cases. The operation modes DP, ECO and CRU, and the fuse model, were introduced earlier in Section 3.2. Fault locations 1) and the associated protection approaches 2) are introduced in the following subsections.

3.3.1. Location

The physical location of the fault can significantly affect the outcome of the event, given the relative complexity of the case of use studied. The distributed approach with DC cabling modifies the impedance of the circuit compared to the centralized switchboard. For instance, in a pole-to-pole fault close to the output filter of generator G1, the adjacent output filter dominates the time response τ of the first current overshoot (3.1).

Table 3.2: Summary of parameters utilized in the simulation model.

Component	**Value [Unit]**
C_{out}	14.4 mF
ESR	5.5 mΩ
L_p	4 nH
V_{BUS}	1000 V
R_{nom}	0.229 mΩ
R_{SC}	100 µΩ
Load line	≈60 m
Source line	≈50 m

Moreover, the remaining current flowing into the fault comes from various places with different time responses. The characteristics of the output filters together with the impedance of the DC cables could justify such variations.

$$\tau \approx \frac{L_p}{R_{ESR}+R_{SC}} \tag{3.1}$$

Therefore, the variable location tests include five places, indicated with a red flash in Fig. 3.8. Generators G1 and G2 and battery pack BP1 have different cable counts per feeder and output filters, giving several options to study.

Bus A short circuits are particular cases that can simultaneously accumulate energy from all the filters at the fault point. These cases do not have adjacent filters and are affected by the impedance of the entire circuit. Furthermore, load zone A has an extra set of cables that can modify the characteristic impedance even further, affecting the fault current to a greater extent. The faults are located on Bus A, so it is assumed that the behavior of instances on Bus B will mirror the other

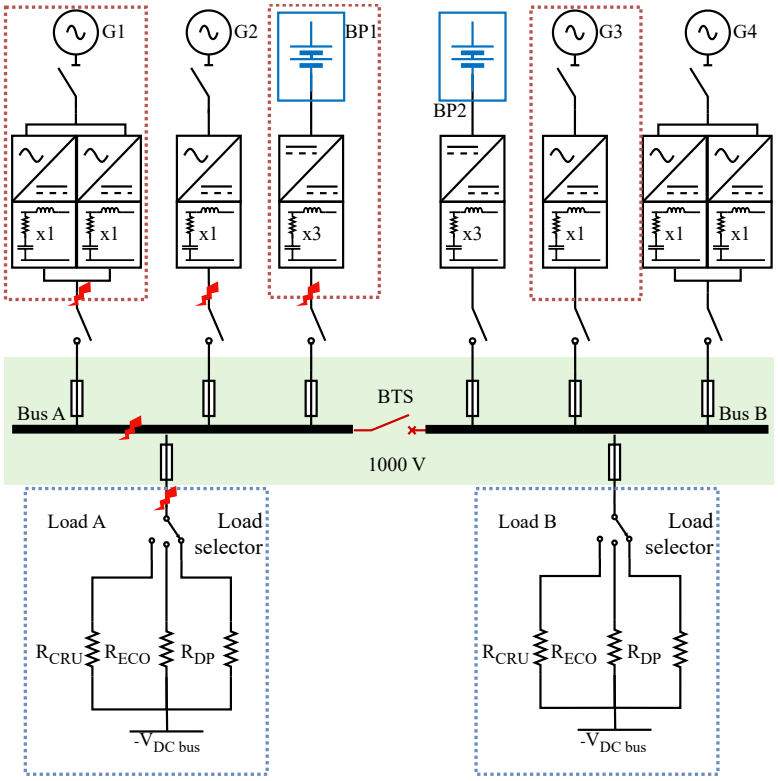

Figure 3.8: Simplified diagram of the system including the short circuit locations. *Red dots: Components placed close together, blue dots: load zones, green shade: switchboard components placed close together.*

cases.

3.3.2. Protection approach

The protection strategies are selected considering two objectives. First, analyze the natural response of the DC system in the event of a fault and provide insight into the worst-case scenario, and second, benchmark two popular protection strategies based on fundamental protection components (fuses and BTS) as specified in [45, 49]. The unrecoverable blackout is the worst case considered for the system. A blackout is considered unrecoverable if the downtime exceeds a predefined limit, which depends on the type of vessel, e.g., 60 s from blackout detection to thrust restoration in DP types.

The protection approaches are divided into three possibilities.

1. System without feeder protection and low-speed BTS (8 ms).
2. System with feeder fuses and low-speed BTS (8 ms).
3. System with feeder fuses and high-speed BTS (21 µs).

The framework of this research facilitates the creation of an inventory of short circuit currents from the simulation, which is compared, in principle, with analytical methods.

3.4. Fault current characterization

This section aims to present significant findings from the simulation model under different conditions. The benchmark of several test cases based on extracted and calculated parameters, such as peak current, dissipated energy, and specific energy, allows a comprehensive distinction among fault types and locations, which is the core of the categorization in Section 3.6.

The inventory follows a logical structure, in principle, providing a complete overview of the selected cases.

1. The potential energy stored in the capacitors and the energy dissipated by the ESR are discussed.
2. The analytical model based on circuit analysis and the potential limitations of the method are introduced.
3. Results and calculations of the test case without protection.
4. Results and calculations of the test case with feeder fuses.
5. Results and calculations of the test case with feeder fuses and high-speed BTS.

The section ends with a DC cabling sensitivity analysis, given that their length affects the fault current waveform. The cable length ranges from centralized to distributed primary systems in a single-feeder test.

3.4.1. Potential Energy

Most of the transient-state energy in a DC short circuit gets transferred from the output filter capacity. Table 3.3 summarizes the potential energy of the capacitors for the superyacht case in Fig. 3.2, including the equivalent total energy.

The energy dissipated during the short circuit reflects a fraction of the potential stored in the filtering capacitors. The ESR dissipates the remaining energy, which varies depending on the location of the fault. Therefore, the architecture and parameters of the DC system affect the proportion in which they split apart. The reason is that the ESR is approximately one and a half orders of magnitude larger than R_{SC}, and the location affects the equivalent ESR influencing the fault. The energy dissipation ratio from R_{SC} to ESR in the superyacht based on the fault location is:

- **Generators G1 & G4:** 27.5 times
- **Generators G2 & G3:** 55 times
- **Battery pack BP1 & BP2:** 18.3 times
- **Bus A & B:** 4.58 times
- **Load A & B:** 4.58 times

In short, the component storing the energy can dissipate most of it during the transient. The energy dissipation ratio facilitates the health estimation of the output filters by providing insight about the absorbed energy during the fault.

3.4.2. Analytical model

Mathematical models are essential for simulation tools and can be used to analyze fault currents in shipboard DC systems to a certain extent. For example, the power grid in Fig. 3.2 has multiple sources connected to the two buses via DC power lines. For faults adjacent to any of the output filters, it is possible to estimate the behavior of the fault current by working with simple assumptions. Figure 3.9 shows a simplified circuit of the feeder that connects generator G1. As the fault resistor is adjacent to the filter, the current through the transmission lines is initially neglected.

In the case of an event such as a type-A fault, the mathematical representation gives (3.2) and (3.3). Here i_{SC} is the fault current and v_{cap} is the capacitor voltage.

Table 3.3: Potential energy stored in capacitors per feeder

Generators G1 & G4 (kJ)	Generators G2 & G3 (kJ)	Battery packs BP1 & BP2 (kJ)	Total (kJ)
14.4	7.2	21.6	86.4

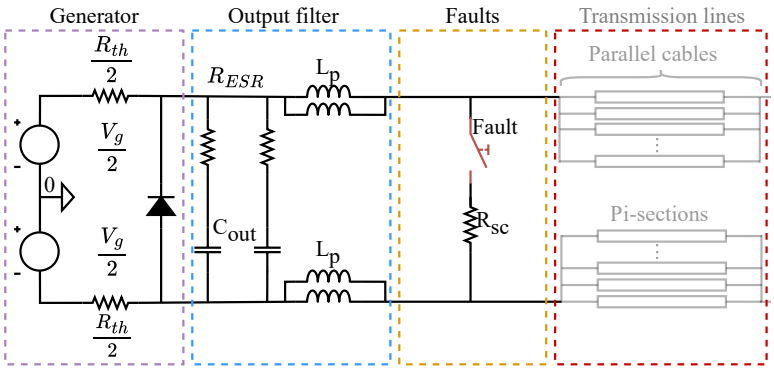

Figure 3.9: Schematic of the simplified generator G1 circuit for short circuit current analysis. *Purple dash: generator, blue dash: output filter, yellow dash: short circuit resistor, red dash: parallel transmission lines.*

$$2L_p \frac{di_{SC}}{dt} + i_{SC} R_{SC} = v_{cap} - C_{out} R_{ESR} \frac{dv_{cap}}{dt} \tag{3.2}$$

$$i_{SC} = C_{out} \frac{dv_{cap}}{dt} + \frac{V_g - V_{BUS}}{R_{th}} \tag{3.3}$$

The current response can be overdamped or underdamped depending on the parameters, which gives two families of solutions in (3.4) and (3.5), respectively, for the differential equations system. More details on solution and analysis methods are available in [26, 58, 160, 161].

$$i_{SC}(t) = \frac{e^{-\alpha t}}{2\beta} \left[\frac{V_{cap}}{L_p} \left(e^{\beta t} - e^{-\beta t} \right) + \beta I_g(0) \left(e^{\beta t} + e^{-\beta t} \right) \right] \tag{3.4}$$

$$i_{SC}(t) = e^{-\alpha t} \left[\frac{V_{cap}}{\omega_d L_p} \sin \omega_d t + I_g(0) \cos \omega_d t \right] \tag{3.5}$$

Where $I_g(0)$ is the initial condition of the generator current, which is given by the operating mode, $\alpha = \frac{R_{ESR}}{2L_p}$, $\beta = \sqrt{\left(\frac{R_{ESR}}{2L_p}\right)^2 - \frac{1}{L_p C_{out}}}$, and $\omega_d = \sqrt{\frac{1}{L_p C_{out}} - \left(\frac{R_{ESR}}{2L_p}\right)^2}$.

The fault current from the circuit in Fig. 3.9 is overdamped and Fig. 3.10 shows in blue the current response obtained by using the parameters from Table 3.2 in (3.5). The peak current is ≈343 kA with a peak time of ≈ 6 µs.

A simulation of the feeder in Fig. 3.9, attached to the load, is shown in dashed red in Fig. 3.10. This result suggests that it is possible to estimate the first current overshoot in a pole-to-pole short circuit, as long as the fault occurs close to a filter. The single feeder simulation reaches ≈ 323 kA in about 10 µs despite including parallel cables in the analysis.

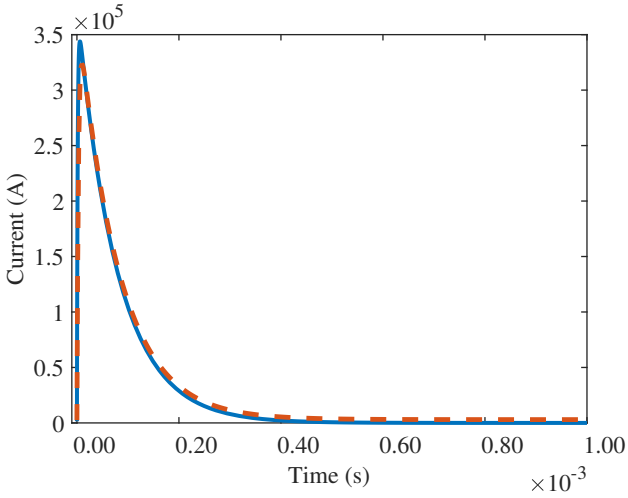

Figure 3.10: Comparison of fault currents during a pole-to-pole short circuit in a single-feeder system based on generator G1 and maximum nominal load. *Blue: analytical model, dash red: simulation model*.

However, the results of the analytical method are overly complex when studying the entire circuit. The augmented system introduces numerous state variables, and thus numerical methods are preferred. The fault current computation results are less intensive and potentially more accurate. The information aids in mitigating possible threats, conceivably enhancing design procedures and streamlining the analysis.

3.4.3. Non-protected system

This section includes the main takeaways of the numerical model that utilizes a non-protected approach under type-A faults. The related test cases show the natural response without feeder protection. The low-speed bus-tie switch is the only protection component in this configuration and its influence is limited. It is worth mentioning that this case is not practical in reality, but it gives insight into the phenomenon. The section covers the following topics: Initially, 1) the fault current at different locations for a single operation mode is shown. Later, 2) the fault current sources and their contribution to a single event are analyzed, 3) the voltage disturbances present during a short circuit are outlined, and 4) several short circuit characteristics in different operation modes are discussed.

Fault current at various locations

The event location significantly affects its waveform because the cabling modifies the impedance of each feeder. Figure 3.11 shows the natural response of several faults in the system under study, which facilitates their comparison.

The output capacitors dominate the behavior of the phenomenon. An initial overshoot is visible when the fault occurs adjacent to generator G1 or G2 and battery pack BP1. The earliest response in these signals is rather aggressive and they appear to overlap completely. The time scale of the figure allows for a comparison among the five fault locations and other figures, but creates an overlapping perception. However, their di/dt is different, shifting the current peak and the time to peak. The inset in Fig. 3.11 shows the fault in generator G2 reaching about 173 kA, 339 kA for generator G1 and 495 kA for the battery pack BP1. After the initial overshoot, the inductance and capacity of the complete system must be considered. The current exhibits subsequent amplitude decaying oscillations that supply the utmost energy to the fault. An overview of the waveform shows that the first overshoot has a limited area, implying that its energy is lower than that of the first subsequent peak despite the lower maximum.

Faults at Bus A or load zone A behave differently from the other cases. The initial overshoots are comparable to the subsequent overshoots obtained at the other points. In addition, the impedance of the feeders shifts the initial peaks, which also implies higher energy.

Furthermore, the resonance among the components in the DC system governs the oscillations in the fault currents. The current from the sources varies with different decay factors and frequencies, making the period irregular. The zero-crossing visible in Bus A (purple) is also a consequence of the oscillations and does not work in fault clearing.

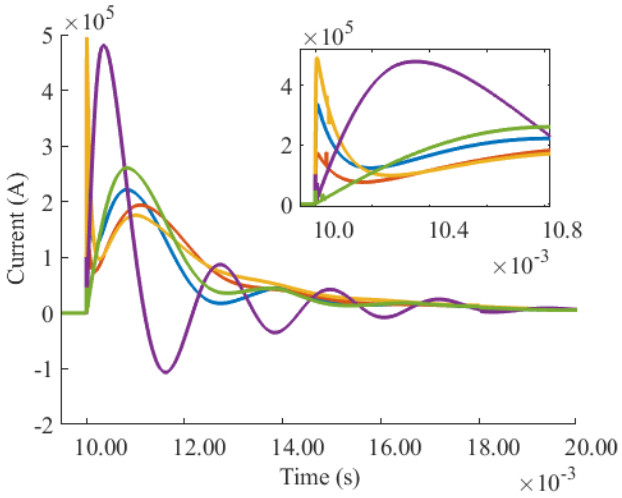

Figure 3.11: Pole-to-pole short circuit current response at various locations with the DC system operating in DP mode. *Blue: generator G1, red: generator G2, yellow: battery pack BP1, purple: bus A, green: load zone A. Inset: Detail of the initial current overshoot after the short circuit.*

Fault current sources

In practice, direct measurement of the short circuit current is not feasible. However, at least partial waveform reconstruction is possible from measurements present in real applications. For instance, adding together the output current of the converters in the DC system can be derived in any of the fault current waveforms in Fig. 3.11. This subsection intends to analyze the contribution of the different sources in a particular fault and some of the implications.

The current measured in the output filters when the short circuit occurs by generator G1 is visible in Fig. 3.12. Most of the energy stored in the adjacent capacitors is dissipated by the ESR, and the remaining energy is transferred to the fault. Notice the initial $^{di}/_{dt}$ among the signals compared to generator G1 (blue).

In Fig. 3.12, the average $^{di}/_{dt}$ in generator G1 is approximately 51.3 kA µs^{-1}, whereas the same variable at generator G4 is close to 81.4 A µs^{-1}. The current rise at the sources away from the fault have a comparable behavior, and they overlap in the simulation. This result suggests that it would be possible to detect a type-A event when it occurs adjacent to an output filter.

The fault current oscillations are challenging to anticipate in real-time usage, and the lack of consistent behavior impedes their utilization in protection. Despite the existence of zero-crossing in some signals in Fig. 3.12, these events depend on the damping factor of the grid for the specific transient, and the operation of a circuit breaker should not rely on them. For example, zero-crossing of battery packs (magenta and dash light blue) occurs approximately 2 ms after the short

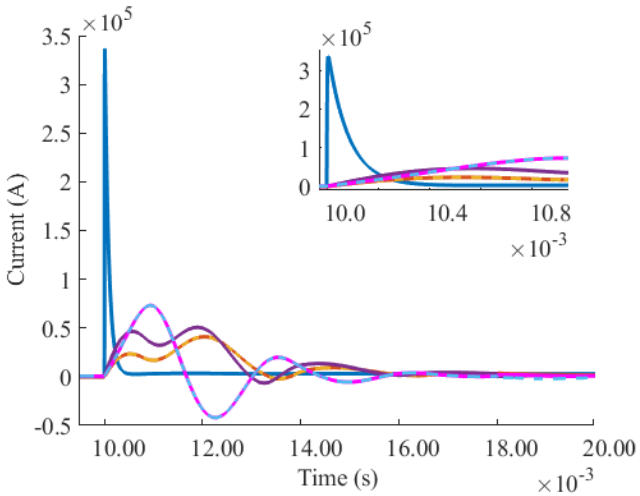

Figure 3.12: Fault current fed by different sources into a pole-to-pole short circuit at generator G1 in the DC system operating in DP mode. *Blue: generator G1, red: generator G2, dash yellow: generator G3, purple: generator G4, magenta: battery pack BP1, dash light blue: battery pack BP2. Inset: Detail of the initial current variation after the short circuit.*

circuit. Meanwhile, the current in generator G4 (purple) oscillates without a zero-crossing until after 3 ms. In contrast, the current of the adjacent filter does not have zero-crossings, which aligns with well-known DC protection obstacles.

Voltage disturbances

Significant voltage variations are logical consequences of a fault in a low-impedance DC system such as shipboard grids. This section discusses the sequence of events that depict voltage disturbances that arise from a pole-to-pole fault on generator G1.

1. Short circuit occurrence.
2. The voltage in generator G1 drops to zero as the output capacitors are discharged.
3. The subsequent current oscillations force the voltage decay at the remaining locations.
4. The voltage in all nodes stabilizes at zero volts after a few milliseconds.
5. All the potential energy in the capacitors gets dissipated.
6. The BTS trips 8 ms after the fault, creating voltage oscillations.
7. The voltage restoration starts at the healthy side of the system.

The numerical model shows the voltage oscillations caused by the abrupt load change. Such variations can cause sympathetic tripping in a shipboard DC system, potentially compromising the correct protection selectivity. The amplitude, characteristics, and mitigation of voltage variations require a detailed study, which is beyond the scope of this work.

Fault current characteristics

The characterization of the fault current requires the analysis of the peak amplitude together with the specific and dissipated energy. Including parameter and initial condition variations facilitates a more complete understanding of the phenomena. The study of test cases considers the following parameters. 1) Peak current, 2) Specific energy during the initial overcurrent and the complete fault. 3) Absorbed energy also for the first overshoot and the rest of the event, 4) Specific and absorbed energy from the filter adjacent to the fault point (when applicable) and 5) peak power.

The analysis is applicable to the entire set of tests. However, battery feeders feature the highest capacitance of the system, and only such cases are discussed. Type-A faults at Bus A are studied in Sections 3.4.4 and 3.4.5, investigating more realistic scenarios.

1. **Peak current:** The events placed adjacent to output filters (generators G1 to G4, battery packs BP1 and BP2) show consistent similarities. The total fault current exhibits a first high frequency overshoot followed by a composite of subsequent oscillations. Therefore, the peak current analysis includes the first overshoot, supplied mainly by the adjacent filter, and the first succeeding peak. The cases without adjacent filters (bus bars and load zones) behave differently. The first overshoot shows a lower frequency, whereas the second peak is significantly lower than in the other instances *(see Fig. 3.11)*.

2. **Specific energy:** The specific energy of the fault current allows the calculation of the absorbed energy for any component of the circuit path.

   The specific energy calculation uses (3.6) where t_1 coincides with the start of the fault in all cases. The end of the interval t_2 has two instances for calculation. 1) The initial discharge accounted until the local minimum via the first derivative, which is the starting point for the subsequent discharges. And 2) covers the fault current until it reaches the (approximate) steady-state.

$$\frac{\mathrm{W}}{\mathrm{R}} = \int_{t_1}^{t_2} i^2(t)\,\mathrm{d}t \tag{3.6}$$

3. **Absorbed energy:** The absorbed energy considers the specific energy transferred to the short circuit resistor. The calculation is carried out in the same intervals as in the previous case, according to (3.7).

$$\mathrm{E} = \mathrm{R_{SC}} \int_{t_1}^{t_2} i^2(t)\,\mathrm{d}t \tag{3.7}$$

4. **Energy from adjacent filters:** Replicating the analyses in 2) and 3) for the output energy from the contiguous filter allows the evaluation of their contribution in the first overshoot.

5. **Peak power:** The instantaneous peak power allows visualization of the power reached at the maximum fault current.

Table 3.4 summarizes the analysis of pole-to-pole short circuits at battery pack BP1 in the DC system for the DP, ECO and CRU operating modes. The main characteristics of the events are the following.

1. The subsequent current peak is about 35%, on average, of the initial overshoot.

2. The specific and absorbed energy of the initial discharge are close to 20% of the total.

3. The energy supplied by the adjacent filter during the initial peak is about 17% of the total and about 83% of that during the first overshoot (Fig. 3.13).

Table 3.4: Characteristics analysis of pole-to-pole fault currents with different initial conditions at the battery pack BP1

Parameter	Operation mode		
	DP	ECO	CRU
Peak current (kA)			
1^{st}	495.56	495.32	493.58
Subsequent	175.79	175.52	173.53
Specific Energy (kJ Ω^{-1})			
1^{st}	13576	13554	13474
Total	66405	66227	65023
Energy (kJ)			
1^{st}	1.36	1.35	1.35
Total	6.64	6.62	6.5
Energy from adjacent filter			
Specific (kJ Ω^{-1})	11337	11325	11245
Energy (kJ)	1.13	1.13	1.12
Peak power (MW)	24.55	24.53	24.36

4. The energy stored in the output filter is about 21.6 kJ (see Table 3.3), and from (3.7), the ESR dissipates approximately 20.78 kJ during the first overshoot.

In addition, initial conditions appear to have little influence on fault characteristics, and energy seems to decrease when the initial load is the highest (CRU mode). For instance, the peak current in DP mode is approximately 1.3% larger than in the CRU mode, absorbing the maximum energy. Furthermore, the difference in specific and absorbed energy is close to 2.1% in favor of the DP case. Therefore, the initial conditions of type-A faults adjacent to an output filter have a negligible influence on the phenomenon.

The analysis in Table 3.4 provides insight into the natural response of pole-to-pole short circuits in shipboard DC systems. This information could facilitate the development of future protection systems and the proper design of well-known technologies. However, the rest of the short circuit inventory studies more realistic scenarios based on currently approved solutions.

3.4.4. Fuse protection

After the analysis of natural response, a system configuration closer to an actual implementation is studied. The protection system of certified DC ships is mainly based on fuses for selectivity and galvanic isolation [49, 158]. This section investigates several type-A faults in a shipboard DC system similar to Fig. 3.8, where each feeder has fuses, as described in Section 3.2. The fuse selection is based on marine-certified fuses [162] and the nominal drive current plus minimum 10% as a security margin.

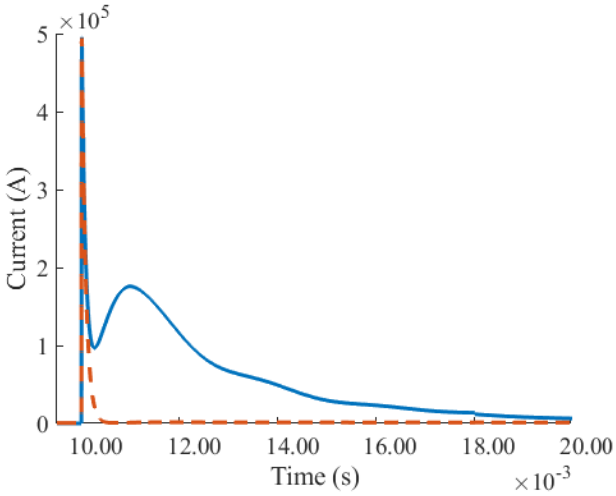

Figure 3.13: Current supplied by the filter adjacent to a pole-to-pole short circuit at the battery pack BP1 with the DC system operating in DP mode. *Blue: short circuit current at battery pack BP1, dash red: current supplied by the filter adjacent to the fault location.*

The procedure is equivalent to the non-protected case, and, therefore, the section includes, in principle, the same subsections. Nevertheless, the behavior of bus bar and load zone faults is significantly different from the other cases, requiring a dedicated analysis. Hence, the section outline is the following. 1) Fault current at different locations, 2) fault current sources, 3) voltage disturbances, 4) characteristics of short circuit current, and 5) bus bar faults.

Fault current at various locations

Figure 3.14 shows the simulations of pole-to-pole short circuits located in various sections of the DC system. From the non-protected system case, it is clear that the location of the faults can affect their waveform, which is mainly due to the nonhomogeneous characteristics of the feeders in the DC system. Including fuses does not have a significant apparent influence on the initial waveform of the fault current. At least initially, the overcurrent peak varies only slightly in magnitude compared to Fig. 3.11, attributed to the nominal resistance of the fuse.

Faults adjacent to a filter exhibit a first overshoot followed by a subsequent overshoot, which decreases significantly as the effect of the arcing resistor grows. The remaining phenomenon shows only a slow magnitude decay until it reaches the nominal current of the source. The fuse cutoff does not completely clear the fault, since the short circuit resistor is in parallel with the output filter, whereas the fuse is in series with the cable at the bus connection point.

The faults at bus bars and load zones exhibit a behavior comparable to that in

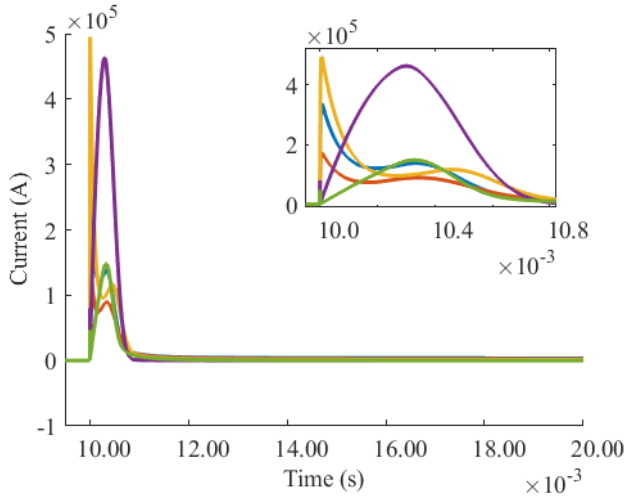

Figure 3.14: Pole-to-pole short circuit current at various locations with fuse protection, and the DC system operating in ECO mode. *Blue: generator G1, red: generator G2, yellow: battery pack BP1, purple: bus A, green: load zone A. Inset: Detail of the initial current overshoot after the short circuit.*

the non-protected case, and the effect of the fuse is visible only after the initial overcurrent. Eventually, the fuse cuts off, and the fault current drops to zero, clearing the fault from the power supplies in the system.

The output of the simulations suggests that it is possible to isolate a faulty generation feeder with the fuse and remain operating with the rest of the system. However, sympathetic tripping and accelerated fuses degradation are plausible consequences of a fault. Table 3.5 summarizes the blown and degraded fuses during short circuits in Fig. 3.14 according to the numerical model. The fuse is considered to be degraded when the current increase during the fault is significant, but not high enough to activate the prearcing for the duration of the simulation. On average, fuse prearcing starts about one millisecond after fault, which is consistent with catalog data [162]. The nomenclature identifies the fuse by its location in the system as follows.

- **Generator feeders (G1 to G4):** FG1, FG2, FG3, and FG4.
- **Battery pack feeders BP1 and BP2:** FB1 and FB2.
- **Bus bars A and B:** FBusA and FBusB.
- **Load feeders A and B:** FLA and FLB.

Table 3.5: Fuse activation and degradation derived from the faults at various locations with a low-speed BTS in Fig. 3.14.

Location	Blown	Degraded
Generator G1	FG1	FG2 and FG3
Generator G2	FG2	FG3
Battery pack BP1	FB1	FG2 and FG3
Bus A	All	N/A
Load A	FLA	ALL

Fault current sources

This section completes the fault analysis by focusing on the current from the supplies. The type-A short circuit current in generator G2 shown *(in red)* in Fig. 3.14 is equivalent to the source currents in Fig. 3.15.

In general, the fuse attenuates the current oscillations after the initial overcurrent. The time response of the fuses may not be sufficient to avoid the discharge of adjacent capacitors. Thus, the initial overshoot lacks attenuation, and the total energy in the contiguous capacitor is transferred into the fault and the ESR.

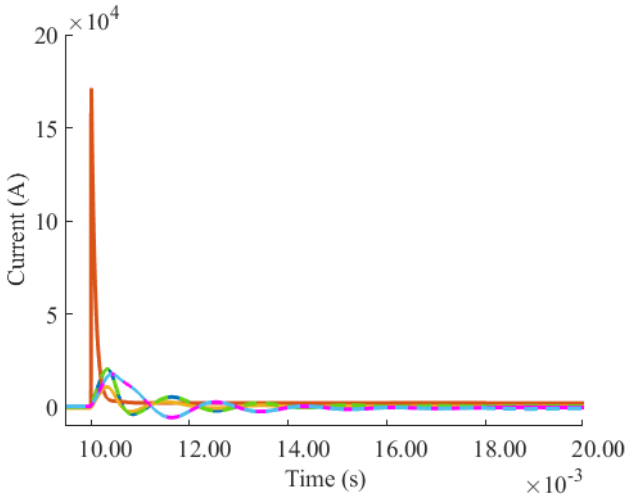

Figure 3.15: Fault current fed by different sources into a pole-to-pole short circuit at generator G2 with fuse protection, and the DC system operating in ECO mode. *Blue: generator G1, red: generator G2, yellow: generator G3, dash green: generator G4, magenta: battery pack BP1, dash light blue: battery pack BP2.*

Voltage disturbances

Pole-to-pole faults located close to an output filter can create a severe voltage drop when using feeder fuses. This section describes the voltage fluctuations caused by the feeder fuses. The voltage disturbances in the presence of a pole-to-pole short circuit at generator G2 exhibit the following sequence of events.

1. Short circuit occurrence.
2. The capacitor voltage in generator G2 drops to zero after about 0.96 µs.
3. Voltage at the bus bars initially decay as in the case without protection.
4. The feeder fuse blows, showing the protective effect after around 0.28 ms.
5. Voltage in the healthy nodes start to recover.
6. The BTS trips 8 ms after the fault, creating voltage oscillations.
7. The voltage restoration in the healthy side ends after a few milliseconds.

This result could become representative, assuming that the voltage drop protection, featured in most certified drives, triggers after the BTS (8 ms). This scenario is consistent with the recommended three-zone protection scheme for shipboard DC systems [65].

Fault current characteristics

This section examines further the parameters of the pole-to-pole faults located close to an output filter in the referential shipboard DC system. Table 3.6 summarizes the parameters, already introduced in Section 3.4.3, at battery pack BP1 for different initial conditions.

The main takeouts from the analysis are the following.

1. The subsequent current peak is about 23.8% of the initial overshoot.
2. The specific and absorbed energy of the initial discharge are close to 76% of the total.
3. The energy supplied by the adjacent filter during the initial peak is about 64% of the total and around 84% of that during the first overshoot.
4. The energy stored in the output filter is approximately 21.6 kJ, and the ESR dissipates approximately 20.72 kJ.

In general, including the feeder fuses could prevent the largest share of potential energy from being transferred to the fault. Such a scenario is only applicable if the fault occurs close to an output filter in a similar use case. The phenomenon is attributed to the sharp increase in current, which is possible when the inductance between the fault and the output filter is low. Section 3.4.6 covers the effect of the inductance in the waveform of the short circuit. As a complement, Section 3.5

Table 3.6: Characteristics analysis of pole-to-pole fault currents with different initial conditions at the battery pack BP1, considering fuse feeder protection.

Parameter	Operation mode		
	DP	ECO	CRU
Peak current (kA)			
1^{st}	487.8	491.56	489.76
Subsequent	116.71	116.62	115.94
Specific Energy (kJ Ω^{-1})			
1^{st}	13423	13497	13376
Total	17660	17728	17583
Energy (kJ)			
1^{st}	1.34	1.35	1.33
Total	1.76	1.77	1.75
Energy from adjacent filter			
Specific (kJ Ω^{-1})	11342	11330	11245
Energy (kJ)	1.13	1.13	1.12
Peak power (MW)	23.8	24.16	23.99

summarizes the comparison of protection performance for the different test cases. The analysis benchmarks the non-protected, fuse feeder protected, and fuse feeder protected with high-speed but-tie switch cases.

Fault at the bus bars

Bus bar faults require dedicated analysis and classification, and this section studies type-A events at the bus bars with a worst-case perspective. Despite having similar behavior to the bus fault, the load zone event has an additional set of DC cabling that increases the impedance. Therefore, the short circuit current is damped and isolated by the fuses, while the overcurrent-driven thermal stress in the other feeders can be reduced, possibly allowing the generation feeders to continue operating.

Hence, the bus bar fault results are important for understanding the protection mechanisms for future shipboard DC systems. The purple signal in Fig. 3.14 is the total fault current in bus A. The peak value is the second largest among the test cases in the plot. However, the rise and fall times are comparable, which implies that the transferred energy becomes significantly higher than in other instances. In addition, the event occurs approximately in parallel with all the filters, which decreases the resulting ESR and facilitates the energy transfer to the fault.

The numerical model indicates that the fault can create an unrecoverable blackout (worst-case scenario) by blowing all the fuses in the generation feeders. The energy transferred from the capacitors surpasses the fuse limits in all generation feeders. Considering that the acceptable worst-case involves losing one bus, a blackout is inherently a catastrophic fault that demands prolonged downtime for a partial recovery. The parameters in Table 3.7 describe the main characteristics of

the pole-to-pole event on Bus A with different initial conditions.

The absence of initial overshoot is not necessarily positive, as the peak current rises close to the maximum in the battery pack BP1 *(see Table 3.6)*. The total energy in the capacitors is 86.4 kJ *(see Table 3.3)*, and the amount transferred to the fault is, on average, 6.54 kJ, while the amount dissipated in the ESR is approximately 29.98 kJ. The outcome suggests that the fuses limit the transfer and dissipation of 57% of the potential energy in the output filters. However, the specific and absorbed energy are approximately 4.87 times larger than that of the battery pack BP1 case. Such a result could indicate that, despite the benefits of feeder fuses, short circuits in shipboard DC systems remain potentially dangerous and the development of proper technology is necessary.

3.4.5. High-speed bus-tie switch

Shipboard power grids utilized in sensitive applications, such as offshore platforms and cable layers, demand stricter design requirements than a superyacht [5, 49]. Therefore, it is recommended to employ solid-state bus tie switches in DC system protection to enhance the performance of the three-zone scheme [66]. The braking time of solid-state protection components (several microseconds) against their mechanical counterparts (a few milliseconds) can justify the recommendation [53]. Nevertheless, their cost, availability, and efficiency can hinder their deployment in shipboard DC systems.

The numerical model in this section includes a high-speed BTS, assuming negligible losses, to evaluate the protection performance gain of the system under several type-A faults. The response time of the BTS is 21 µs, according to the marine-certified solid-state component in [80]. The procedure is similar to previous cases, and the section covers the following topics. 1) Fault current at different locations, 2) fault current sources for one of the locations, 3) voltage disturbances for the same case, and 4) the fault characteristics of two representative test cases.

Fault current at various locations

This section shows the effect of the high-speed BTS on the total fault current at different locations within the shipboard DC system. The analyses in Sections 3.4.3

Table 3.7: Characteristics analysis of different short circuit currents at Bus A considering fuse protection.

Operation mode	Peak current (kA)	Specific Energy ($kJ\,\Omega^{-1}$)	Energy (kJ)	Peak power (MW)
DP	463.79	65591	6.56	21.51
ECO	463.52	65544	6.55	21.48
CRU	461.14	65090	6.51	21.29

and 3.4.4 conclude that faults occurring close to a filter get most of the initial overshoot energy from the capacitors, which implies that the high-speed BTS should not modify the fault current waveform of such cases during the first overcurrent.

Figure 3.16 shows the fault current at various locations in the DC system. The corresponding signals in generators G1 and G2 and the battery pack BP1 exhibit no apparent differences against the previous case (*Fig. 3.14*). On the contrary, short circuits located on Bus A and load zone A display interesting differences to consider.

The action of the BTS interrupts the current build-up in Bus A and load A by curtailing the energy transfer. Moreover, sympathetic fuse tripping, mentioned in Section 3.4.4, can become more apparent when having a high-speed BTS. Table 3.8 summarizes the activation and degradation of fuses during faults in Fig. 3.16, since the model can determine whether a fuse blows and the event instant.

The indicators in Table 3.8 depend mainly on the sizing of the fuse. For example, the fuse in generator G2 can experience sympathetic tripping when a short circuit occurs in generator G1, since the sizing corresponds to the lowest current. On the contrary, the cases condensed in Table 3.5 show the degradation of the fuse in generator G2 for the same fault location. Consequently, the action of the high-speed BTS can create oscillations sufficiently large to force the sympathetic tripping of the fuse, which could prolong the downtime of the faulty bus.

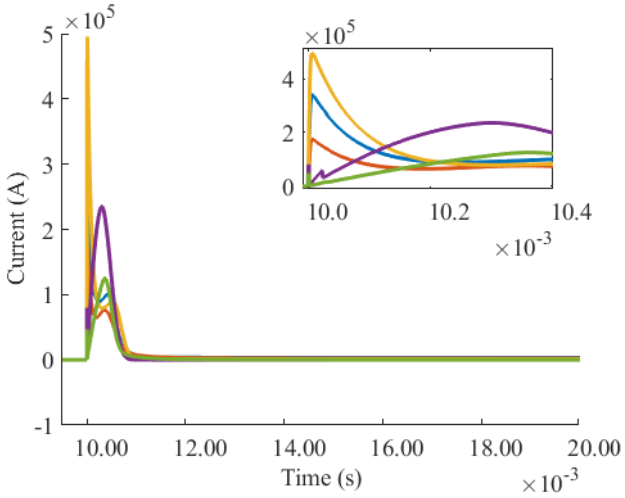

Figure 3.16: Pole-to-pole short circuit current response at various locations with fuse protection and high-speed BTS, and the DC system operating in DP mode. *Blue: generator G1, red: generator G2, yellow: battery pack BP1, purple: bus A, green: load zone A. Inset: Detail of the initial current overshoot after the short circuit, and the effect of the BTS.*

Table 3.8: Fuse activation and degradation derived from the faults at various locations with a high-speed BTS in Fig. 3.16.

Location	Blown	Degraded
Generator G1	FG1 and FG2	None
Generator G2	FG2	None
Battery pack BP1	FB1 and FG2	None
Bus A	FG1, FG2, FB1	None
Load A	FLA	FG1, FG2, FB1

Fault current sources

Given that the added value of the high-speed BTS is most noticeable during pole-to-pole short circuits at the bus bars, this section studies the fault current sources for the Bus A fault case and highlights the contribution of the component.

The fault current on the bus bars lacks the initial current overshoot since the use case does not include a DC bus capacitor (*Fig. 3.16*). Instead, the current waveform is relatively similar for all contributing sources, as shown in Fig. 3.17.

The BTS action, detailed in Fig. 3.17, explains the current drop at approximately 21 µs after the fault in Fig. 3.16. The BTS trips during the build-up, interrupting the current flow from Bus B and allowing continuous operation with one bus. In

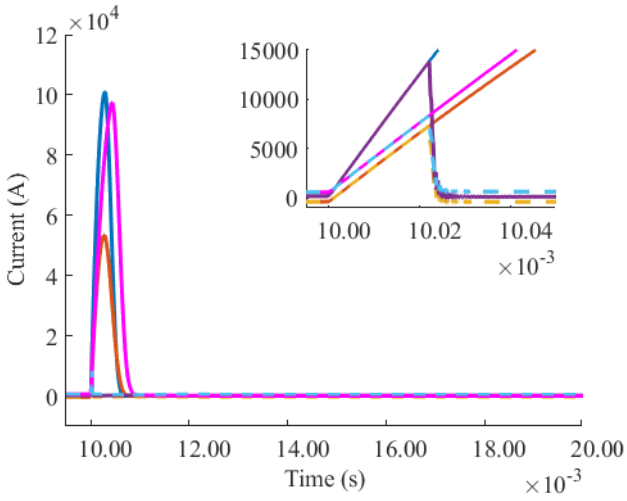

Figure 3.17: Fault current fed by different sources into a pole-to-pole short circuit at Bus A with fuse protection and high-speed BTS, and the DC system operating in DP mode. *Blue: generator G1, red: generator G2, yellow: generator G3, dash green: generator G4, magenta: battery pack BP1, dash light blue: battery pack BP2.*

this case, determining the availability of the bus after a fault could be simplified to measuring the bus and load voltages to a certain extent. In addition, the fuses on the faulty bus eventually blow, clearing the fault and protecting the sources from a long-lasting overcurrent.

Voltage disturbances

This section provides insights into the voltage disturbances when a Bus A short circuit occurs, and the system has a high-speed bus-tie switch.

Section 3.4.4 shows that buses A and B might fail simultaneously after a type-A fault on Bus A when using a low-speed BTS. By deploying the high-speed component, the system can recover the voltage from the healthy side relatively quickly.

The BTS acts in a time frame comparable with the fault time, generating voltage oscillations, after which Bus B and load zone B remain active. Thereafter, fuses on the faulty side operate, allowing the voltage recovery on the healthy bus, providing adequate time for diagnosis and reconfiguration actions. Finally, some control actions, such as load shedding and load management, can limit the effect of the contingency, allowing a better operation scenario during defect corrections.

Fault current characteristics

This section aims to quantify the fault characteristics in the presence of a high-speed bus-tie switch. The fault characteristics of the battery pack are condensed in Table 3.9, considering the parameters explained in Section 3.4.3.

Table 3.9: Characteristics analysis of pole-to-pole fault currents with different initial conditions at the battery pack BP1, considering fuse protection and a high-speed BTS.

Parameter	**Operation mode**		
	DP	**ECO**	**CRU**
Peak current (kA)			
1^{st}	487.8	491.56	489.76
Subsequent	89.74	89.66	89.06
Specific Energy (kJ Ω^{-1})			
1^{st}	13219	13294	13204
Total	15932	16003	15883
Energy (kJ)			
1^{st}	1.32	1.33	1.32
Total	1.59	1.6	1.59
Energy from adjacent filter			
Specific (kJ Ω^{-1})	11361	11350	11265
Energy (kJ)	1.14	1.13	1.13
Peak power (MW)	23.79	24.16	23.99

As anticipated, the parameters describing the fault adjacent to a filter are similar to those of the low-speed BTS case, and Section 3.5 presents a more in-depth comparison. Nevertheless, the main characteristics of short circuit currents are the following.

1. The subsequent current peak is about 18.3%, of the initial overshoot.
2. The specific and absorbed energy of the initial discharge are close to 83% of the total.
3. The adjacent filter provides 71% of the total energy and about 85.5% of it during the first overshoot.
4. The energy stored in the output filter is approximately 21.6 kJ, and the ESR dissipates about 20.76 kJ.

In addition, the fault on Bus A exhibits different characteristics that highlight the benefit of the high-speed BTS. Table 3.10 summarizes the indicators describing pole-to-pole faults at the bus bars for various initial conditions.

BTS protection significantly reduces the peak current, allowing the specific energy to drop close to the case of battery pack BP1. Consequently, the short circuit resistor absorbs about 1.68 kJ, and the ESR dissipates approximately 7.7 kJ, which comprises roughly 10.8% of the total potential energy.

The results suggest that increasing the performance of the BTS can improve the protection of the DC system in the event of a bus bar or load zone fault. However, it has a significantly limited effect on events close to output capacitors because of their disposition into the grid.

3.4.6. Inductance sensitivity

Since the cable inductance is a function of the line length, the previous characterization can become somewhat susceptible to that parameter. A sensitivity analysis of the transmission line length in a single-feeder test could facilitate the visualization of such a tendency. The simplified model includes the feeder of G1, which

Table 3.10: Characteristics analysis of pole-to-pole short circuit currents with different initial conditions at Bus A, considering fuse protection and a high-speed BTS.

Operation mode	Peak current (kA)	Specific Energy ($kJ\,\Omega^{-1}$)		Energy (kJ)		Peak power (MW)
		1^{st}	Total	1^{st}	Total	
DP	235.56		16849	1.68		5.55
ECO	235.43		16837	1.68		5.54
CRU	234.38		16729	1.67		5.49

requires a double circuit (18 cables per pole) attached to a load that demands the nominal power and is in parallel with a type-A fault branch. The iterative simulation varies the length of the transmission line from 0 m to 120 m, taking steps of 4 m, increasing the distance from the output filters to the load and the short circuit.

The procedure advances using different computation tools and transmission line models to determine whether the model is agnostic to the software. The tools used are PLECS, LTSpice, OrCAD, and PSim, showing negligible differences across the tests. However, the tools based on SPICE models are considered more accurate, given the possibility of including more behavioral details.

In addition, the sensitivity analysis considers the variations in the transmission line model to enhance simulation performance. The variations include the pi section based on the telegrapher's equation, the RL model as lumped components, and an equivalent L model.

The pi section-based model gives the only relevant result, since the error between pi sections and equivalent L models is close to 3.4% for the maximum peak and about 1.4% for the minimum. Furthermore, pi-section-based simulations and RL-based models have comparable results, in which the RL case demands a fraction of the computational burden of the pi. Nevertheless, the RL model standardized in [160] and utilized in [127] seems appropriate for complex shipboard DC systems.

The simulation in Fig. 3.18 shows the effect of the line length on the short circuit current for the single-feeder test. The peak current, the average $^{di}/_{dt}$, and the time-to-peak current change significantly. The power line could delay the current overshoot to curtail the peak utilizing a high-speed BTS depending on the architecture and design constraints.

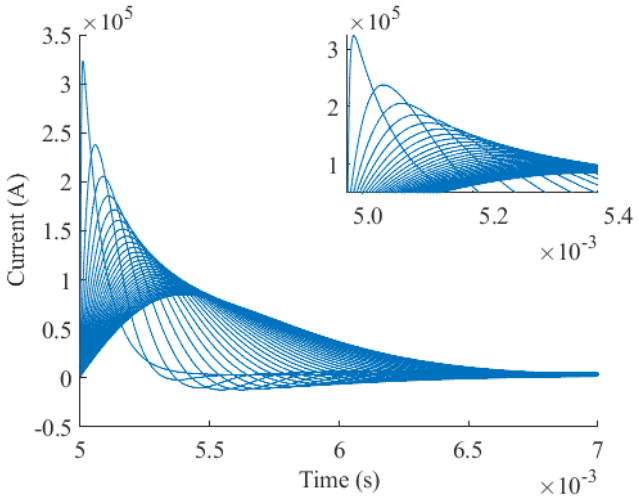

Figure 3.18: Simulation of the line length sensitivity analysis in generator G1 during a pole-to-pole short circuit using pi section models in a single-feeder model.

The influence of the resistive parameters on the limitation of the maximum current is considered negligible. Hence, the energy absorbed by the sort circuit resistor is similar to some extent for all cases. For the same type of fault, the maximum values for the extreme cases (0 m and 120 m are summarized in Table 3.11.

Table 3.11: Summary of extreme parameters in the line length sensitivity analysis in generator G1 during a pole-to-pole short circuit.

Peak current	$^{\Delta i}/_{\Delta t}$	**Cabling inductance**
334 767 A	312.73 kA µs^{-1}	0 H
85 012 A	2.09 kA µs^{-1}	2.64 µH

The sensitivity analysis indicates that it could be possible to modify the waveform of a short circuit by changing the inductance in the terminals by a few microhenrys. However, it may be necessary to assess the effect of the inductance regarding stability and impedance while achieving appropriate damping. Furthermore, the development of improved shipboard DC protection should not entirely rely on the damping effect of the inductance, given the variety and applications of power grids on board.

3.5. Performance analysis

This section aims to benchmark the performance of the protection approaches studied in Section 3.4; the shipboard DC system with feeder fuses and low- and high-speed BTSs. The severity of a short circuit in a DC system can be quantified by analyzing the peak current, the average $^{di}/_{dt}$ (3.8) and the energy absorbed. By determining the performance indicators for cases A) battery pack BP1 and B) Bus A, it is possible to assess the protection countermeasures in state-of-the-art shipboard DC systems.

$$\frac{\Delta i}{\Delta t} = \frac{I_{\max}}{t_{I_{\max}} - t_{\text{fault}}} \tag{3.8}$$

3.5.1. Battery pack BP1

The high-speed BTS has little effect on the total short circuit current for filter-adjacent faults compared to the low-speed case. In addition, fuses partially mitigate the propagation of the fault, which enables continuous operation in these cases. Table 3.12 summarizes the performance indicators for the fault in battery pack BP1.

A peak current fed by a relatively large capacity appears aggressive. The average maximum of 491 kA in a 1000 V DC system is a possible threat indication for the vessel. The average $^{di}/_{dt}$ suggests that fault mitigation could become challenging, while the (thermal) stress of several components can become unendurable. Meanwhile, the total energy dissipated in the fault decreases by approximately 9.

Table 3.12: Performance indicators summary for the Battery pack BP1 considering pole-to-pole fault currents, and low-speed and high-speed bus-tie switches.

Bus-tie switch type	Peak current	$\Delta i / \Delta t$	Total energy	Peak power
Low-speed	491.56 kA	54 136 A µs^{-1}	1.77 kJ	24.16 MW
High-speed	491.56 kA	54 136 A µs^{-1}	1.6 kJ	24.16 MW

6%, which, in principle, reduces the stress in the output capacitors. However, the dissipated energy in the filter, estimated in 20.8 kJ from Table 3.9, may remain excessive. Hence, a high-speed BTS could reduce the propagation of faults near the output capacitors, with limited stress reduction in the ESR.

Subsequently, estimating capacitor damage is fundamental to diagnose the extent of a possible defect. The temperature rise estimation in the capacitor core is a well-known damage indicator, and the temperature limits are available in most datasheets. Equation (3.9) yields the approximate core temperature in the capacitor based on power losses and thermal properties.

$$T_{\text{core}} = T_{\text{air}} + P_{\text{loss}} \mathrm{R}_{\text{th}_{\text{c-a}}} \left(1 - \mathrm{e}^{-t/\tau}\right) \tag{3.9}$$

With T_{core} and T_{air} being the temperature at the core of the capacitor and the ambient temperature, respectively, P_{loss} the power losses in the ESR, $\mathrm{R}_{\text{th}_{\text{c-a}}}$ the core to air thermal resistance, and τ the thermal time constant of the capacitor [163, 164].

The following example illustrates the temperature rise estimation in a referential output capacitor in battery pack BP1. The analysis is based on an array of 7 parallel legs of 2 series capacitors of reference 520C562T500DG2B [165] from CDM Cornell Dubilier. The equivalent capacitance obtained is 19.6 mF and the ESR is 5.6 mΩ, since the modules indicate 5.6 mF and 19.7 mΩ in the datasheet. The equivalent ESR is close to the value in Table 3.2, allowing a fair estimate. The battery pack utilizes three output capacitors, which leads to a peak power loss of approximately 1.03 MW per leg. The thermal resistance of the base capacitor is 0.84 °C W^{-1} if it has a metal heatsink and an air circulation of 5 m s^{-1} [165]. Since the losses in ESR are significant, the short circuit leads to an uncontrollable temperature rise that exceeds the damage threshold (around 105 °C) within tens of microseconds. Overheating increases the ESR, leading to a wear-out fault when the nominal value doubles [166, 167]. The calculation assumes impedance balance among capacitor modules and submodules, splitting the fault current evenly.

3.5.2. Bus A

The performance protection gain from the high-speed BTS becomes appealing when analyzing short circuits at the bus bars. Table 3.13 summarizes the calculations

based on (3.6) to (3.8) for high and low-speed BTS, and faults at Bus A. The peak current decreases at about 49.2% of the expected value with a low-speed component. The current variation rate drops to half (50.9%) of the average indicator. The specific and absorbed energy of the short circuit current are only around 25.6% of the reference value. In addition, the peak power is close to one-fourth (25.8%) of the maximum power expected with a low-speed bus-tie switch.

Table 3.13: Performance indicators summary for the Bus A considering pole-to-pole fault currents, and low-speed and high-speed bus-tie switches.

Bus-tie switch type	Peak current	$\Delta i/\Delta t$	Total energy	Peak power
Low-speed	463.79 kA	1527.4 A µs^{-1}	6.56 kJ	21.51 MW
High-speed	235.56 kA	777.26 A µs^{-1}	1.68 kJ	5.55 MW

Furthermore, the maximum power dissipated by the output capacitors on the recovered side decreases significantly. For instance, when taking the same reference capacitor as in battery pack BP1, the ESR losses at generator G4 jump from approximately 1.98 MW to 38.28 kW per leg. As of (3.9), the core temperature drops from a thermal damage of roughly 268 °C to a reasonable level of about 49 °C. On the other hand, the output filters on the faulty side are exposed to potential wear-out. Generator G2 seems especially vulnerable, since the ESR losses yield an approximate 2.2 MW peak per leg, which from (3.9) gives a core temperature close to 295 °C, damaging the component.

Therefore, the protection performance gained from the implementation of high-speed BTS is remarkable. The fault in Bus A is effectively contained into a less threatening state while restraining the possible capacitor wear-out, which is essential in the operation of the DC system. The high-speed BTS could prevent the blackout discussed in Section 3.4.4, limiting a multi-capacitor wear-out, affecting most of the primary system, into a selective wear-out, degrading only a section of the grid. Nevertheless, the inventory shows that the absence of efficacious feeder protection represents a substantial hurdle, which compels further investigation and improvement.

3.6. Fault categorization

The quantitative analysis in the fault inventory comprehensively describes the possible threats in the superyacht. The purpose of this section is to harness the results in Section 3.4 to create a generic framework suitable for multiple types of vessels. Such a framework relies upon a fault categorization using qualitative indicators, such as potential consequences, detection speed, localization complexity, and fault severity.

The fault categorization is summarized in Table 3.14, followed by 1) the categorization indicators and 2) the interpretation of severity.

3.6.1. Indicators

The categorization utilizes several indicators to provide a comprehensive overview of the faults and determine their severity. The short circuit categorization indicators are the following.

- Location.
- Potential consequences.
  - Protection with slow BTS and fuses (*SB+F*).
  - Protection with fast BTS and fuses (*FB+F*).
- Detection
- Localization

The location and potential consequences depending on the protection scheme are discussed in-depth in Section 3.4. Detection and localization participate in the categorization by jointly analyzing $^{di}/_{dt}$ differences and locations as follows.

Faults close to an output filter exhibit a high $^{di}/_{dt}$ that is relatively straightforward to separate (e.g., Fig. 3.12). Assuming that the protection systems fit within a three-zone selectivity scheme, the alert signal generated by the drive can swiftly provide the most likely location of the fault.

In contrast, faults occurring far from the drives are more complex to identify (e.g., Fig. 3.17). The fault alerts could show a similar timestamp, suggesting that the most likely fault location is the bus bars or the load zones. However, it is necessary to compare the detection alerts and combine them with detection algorithms to accurately determine the location. Consequently, detecting such faults is complex and slow. Notice that previous definitions are possible by assuming the existence of appropriate $^{di}/_{dt}$ and average current detection as in [89, 90].

3.6.2. Severity interpretation

The severity indicator in Table 3.14 provides the fault category for each scenario. The lowest severity indicator implies the most severe type of short circuit. Although the categorization seems initially counterintuitive, the arrangement allows the worst-case visualization always as number one. In addition, the proposed numeration is consistent with the task prioritization schemes existent in most industrial controllers.

The categorization begins from the bus bars as the worst-case, followed by generation feeders to finalize in the load zones. The categorization order from the highest to the lowest output capacitance is governed by the equivalent capacity that feeds the initial fault overcurrent. For example, the adjacent capacitor dominates the initial overshoot in a fault at generator G2. In the case of Bus A, the measured overcurrent is supplied simultaneously by all parallel capacitors with their respective time constant.

Table 3.14: categorization of short circuits in a double bus shipboard DC system considering low-speed and high-speed bus-tie switch based on Section 3.4.

Location	**Potential consequence**		**Detection**	**Localization**	**Severity**
	Protection SB+F	Protection FB+F			
Bus A or B	• Blackout • Multiple capacitor wear-out	• Bus failure • Selective capacitor wear-out	Slow	Complex	1
Battery Packs BP1 or BP2 *Largest filter*	• Feeder failure • Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Feeder failure • Sympathetic failure • Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out	Fast	Simple	2
Generators G1 or G4 *Smaller filter*	• Feeder failure • Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Feeder failure • Sympathetic failure • Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out	Fast	Simple	3
Generators G2 or G3	• Feeder failure	• Feeder failure	Fast	Simple	4

Continue on next page ...

Location	Potential consequence		Detection	Localization	Severity
	Protection SB+F	Protection FB+F			
Smallest filter	• Double bus instability • Long-lasting overcurrent • Selective capacitor wear-out	• Single bus instability • Long-lasting overcurrent • Selective capacitor wear-out			
Load A or B	• Load feeder failure • Double bus instability • Selective capacitor wear-out	• Load feeder failure • Single bus instability • Selective capacitor wear-out	Slow	Complex	5

3.7. Outlook and Conclusion

A fault categorization considering potential threats in shipboard DC systems has been proposed in this chapter. The general methodology can be extrapolated to several types of vessels to enhance protection and control systems in modern, sustainable vessels. A better understanding of faults was introduced, which is essential for the proper design and protection of power converters. In addition, the outcome of this work could help the evolution of the regulatory requirements of maritime power systems. To the best knowledge of the authors, the conducted studies have no precedent.

The fault characterization provides a framework for analyzing possible short circuits at different locations on board, utilizing comprehensive parameters to describe and differentiate events. Faults located in generation feeders produce similar fault waveforms, whereas events at the bus bars require different analyses. In the same way, fluctuating characteristics lead to variable consequences that escalate from a single-feeder failure to a blackout.

The added value of the work lies in combining different techniques to give essential insight about the events. The techniques used involve analytical methods, simplified numerical models, and complete simulation models covering 45 test cases.

From the analytic model it is possible to determine the approximate waveform of the initial overcurrents in the events adjacent to the filter because most of the energy comes from the capacitor. However, bus bar and load zone faults require additional complex calculations to incorporate all feeders, compromising the practical benefit of the method.

Complimentarily, the complete numerical model allows a comprehensive analysis of the fault current and the sources involved. The studies compare the effect of three system configurations during pole-to-pole short circuits in various scenarios.

1. Non-protected approach
2. Protection with feeder fuses
3. Protection with feeder fuses combined with a high-speed bus-tie switch.

Ultimately, fuses can interrupt the propagation of specific faults after the initial overshoot, blocking about 70% of the potential energy. However, the rest of the phenomena could be sufficient to cause permanent damage in some components and temporary malfunctions. The system becomes more fault-tolerant by incorporating the high-speed bus-tie switch since the healthy bus is effectively protected. Faults on the bus bars and load zones seem to be attenuated by current limitation. However, initial overshoots are not significantly affected by the performance of the BTS, which can still lead to permanent damage.

The simulation model based on realistic, state-of-the-art shipboard DC systems mainly considers a distributed switchboard. Thus, parallel cabling creates electric distances among the components that could dampen the peak current. The purpose of the simplified simulation model was to include the inductive effect of the cabling to expand the applicability of the results. Correspondingly, the sensitivity analysis shows that the inductance dominates the damping effect of the short circuit in the case study.

The scale of the DC system is an obstacle for the experimental validation of the simulation results considering the entire system. However, the detailed study of the simplified feeder shown in this document is the basis for future work that involves systematic testing of novel protection devices. A combination of low power mock-up shipboard DC systems and high power single-feeder tests could provide sufficient evidence in validating the results. The following subjects are considered relevant for future work in the development of DC protection systems.

- The BTS model requires an independent study, mainly focusing on certified topologies and assessing their limitations.
- Experimental validation is necessary to assess the dependence of ESR and other parasitic elements on temperature and frequency during a fault.
- Fuse models are widely considered oversimplified, as their behavior is challenging to model. Validation with scaled-down setups could reduce the uncertainty, but only for specific fuses and distribution architectures.
- Faults to ground require further investigation, as they depend on the grounding scheme.
- Simulations based on ideal sources may not be suitable for long-lasting fault assessments and their potential effect on drive controllers.
- The adaptation of the model to a real-time environment could help reduce uncertainty while potentially increasing accuracy.

The development of hardware protection requires significant improvement. The current situation shows that blocking of the fault current sources may be necessary to reduce the possibility of severe defects. However, solid-state circuit breakers are not considered cost-effective or efficient enough to be suitable for widespread use in maritime applications.

Advancements in protection technologies enable safe primary DC systems, crucial for the integration of alternative energy sources. Such technologies are fundamental for global emission reduction and a sustainable future.

4

High-speed Solid-State Circuit Breaker with Latching Current Limiter for Shipboard DC Systems

The advancement of DC systems, especially in transportation applications, hinges on the development of effective protection mechanisms. Robust protection systems are crucial for enabling the widespread adoption of DC technologies in important transport modes, offering both operational and economic benefits. This paper introduces a high-speed solid-state circuit breaker designed for enhancing the protection of general DC systems. The upgraded breaker integrates the functionality of a latching current limiter, designed to minimize modifications to existing technologies. A custom gate driver and controller are developed and experimentally validated to support the circuit breaker. A scaled solid-state circuit breaker prototype is tested under various operational conditions to evaluate its performance. The breaker's behavior is simulated in SPICE to guide the experimental validation on a referential DC system. The results demonstrate high performance, with a clearing time close to 200 ns, effectively reducing system stress during short circuits. The current limiter functionality prevents unnecessary tripping during temporary overcurrents, keeping the current within safe parameters. The innovative gate driver simplifies the implementation of the latching current limiter, offering a practical and scalable solution. This work represents a significant step forward in DC protection technology, promoting the adoption of DC systems

This chapter has been accepted with some modifications for publication in the IEEE Open Journal of Power Electronics **8**, (2026) [13].

in transportation applications and beyond, by addressing critical protection challenges.

4

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Hummingbird live at the edge of the possible, flying like no other bird. Fierce and unyielding despite its size, it defends its flowers with a lightning grace, a testament to speed, endurance, and will. *The hummingbird in this photo is a mysterious one.* Its colors do not match any known species, and it has never been photographed again. Some speculate it may be a hybrid or the result of a color mutation; however, nobody knows for sure, as the bird appeared and disappeared in a flash.

4.1. Background

Transportation serves as the main backbone of modern society, requiring robust and efficient systems to support its critical role [15]. These systems are indispensable for global production lines, supply chains, and leisure industries [6]. However, the transportation industry faces a significant environmental challenge as its operations contribute to substantial carbon emissions [3], which exacerbate climate change and threaten sustainable living. Reducing the carbon footprint in transportation is imperative to minimize their environmental impact while preserving their vital role in the global economy [7, 168].

Ongoing efforts to decarbonize transportation focus on alternative fuels, improved efficiency, and broader electrification [7, 18, 151]. Examples include ammonia combustion, sustainable aviation fuel, and the use of fuel cells and batteries across various modes of transport. Electrification, particularly with DC systems, supports these goals by simplifying the integration of clean energy sources, improving efficiency, and significantly reducing emissions [27, 30, 169].

The widespread adoption of DC technologies in electric and more-electric transportation is based on the confidence of the stakeholders, which requires clear assurances of efficiency, reliability, and safety. Robust protection systems are critical to ensure the safety of involved personnel and the reliable operation of vehicles, ships and aircraft [25, 49, 103]. However, most existing protection systems rely on breaker-based designs, and current DC breaker technologies are not yet fully prepared to meet the demands of DC protection in multiple applications [58, 65]. Addressing these challenges is critical to unlocking the full potential of transport electrification.

Current circuit breaker technologies for DC systems face a trade-off as solid-state types are effective but inefficient, whereas their mechanical and hybrid counterparts are efficient but less effective [5, 97]. This concern is amplified by the severe risk posed by short circuits, which most existing DC circuit breakers struggle to contain effectively [26, 127]. For instance, certified DC circuit breakers capable of handling short circuits and robust fault clearance selectivity are both scarce and expensive [11]. Table 4.1 summarizes the main parameters considered to assess commercially available DC circuit breakers, which is adapted from [11].

To unlock the potential of DC systems, it is essential to address the limitations of existing DC circuit breakers, focusing on improving their efficiency, effectiveness, and safety. Solid-state circuit breakers (SSCB), which employ semiconductors to achieve the breaking action, present a promising alternative, especially if their functionality is expanded beyond simply replacing AC circuit breakers. For example, a conventional SSCB can provide additional protection features such as Latching Current Limiter (LCL), designed to limit and hold current flow at safe levels during fault conditions, a technique already used in sensitive applications like aerospace [170, 171]. By preventing excessive current flow, the LCL enhances operational safety and protects downstream components [172].

LCLs mainly employ gate signal modulation to operate the power FET in its linear region, which ultimately limits the current by increasing the equivalent channel resistance R_{DSON} [173]. Available, certified-products, such as the AstrolKWx model

Table 4.1: Example of commercially available DC circuit breakers with marine certification, *adapted from [11], with references to prior studies [70, 72, 80].*

Type	**Mechanical circuit breaker**	**SSCB**	**Solid-state bus-tie switch**
Vendor	Schneider Electric	ABB	AstrolKWx
Reference	NW20HDC-C	SACE Infinitus	AA-10411-203
Rated voltage	1000 V	1000 V	1000 V
Breaking current	2000 A	2500 A	3000 A
Breaking time	30 ms	$\leq$ 25 µs	15 µs to 21 µs
Power losses	Not reported	1.3 kW@1 kA	6 kW@3 kA 0.67 kW@1 kA est.
Cooling solution	Air	Liquid	Liquid

in Table 4.1 and the Vacon NXP DC drive in [137], are primarily based on IGBTs, given the relatively high current ratings expected in heavy duty applications [5]. However, IGBTs are bipolar devices whose gate-turn-off characteristics are nonlinear, making them less effective when using the device's linear region to provide the LCL functionality [174]. Therefore, implementing the LCL into a conventional SSCB implies a paradigm shift towards FETs, where SiC MOSFETs or JFETs could become suitable replacements.

The key contribution of this chapter is a practical implementation of a LCL for DC systems that moves beyond conventional time-based selectivity [65]. This is achieved through a design based on the integration of two key elements: a custom three-level gate driver [175] and a high-speed analog controller. The three-level gate driver enables stable operation of SiC MOSFETs in their linear region, while the dedicated analog controller provides high-speed operation for breaking and current limiting. The resulting design offers a less complex and more practical implementation compared to sophisticated LCL circuits (e.g., those used in space-rated applications), demonstrating a viable path to achieving current-based selectivity to prevent fault propagation and enhance the reliability of DC power systems.

A scaled-down prototype of a bidirectional SSCB with adapted LCL was tested. Experimental validation confirms that the device can effectively break the current during pole-to-pole short circuits while avoiding unnecessary interruptions during transient overloads. This work provides design guidelines for upgrading a conventional SSCB to include the LCL and demonstrates their potential as advanced protection devices for next-generation DC systems. The results strengthen the case for SSCBs not just as AC breaker replacements but as key enablers of more selective, compact, and reliable DC protection architectures.

The FET-based SSCB with the proposed custom gate driver and controller exhibits a breaking time approximately two orders of magnitude lower than the commercial models in Table 4.1. It performs breaking actions within 200 ns which can significantly decrease semiconductor stress by limiting the initial fault current, thus im-

proving operational safety. This work serves as proof-of-concept for the upgraded SSCB, and future work should tailor the design to a specific application.

To showcase the contributions, the document is organized as follows: Section 4.2 describes the considered DC system, the reference SSCB, and the design of the dampening components. Section 4.3 presents the custom three-level gate driver designed to enable LCL functionality. Section 4.3.1 details the control design that enables high speed breaking and effective current limiting, supported by simulation results for both protection modes. Section 4.3.2 shows a high-level summary of the SSCB design to facilitate visualization. The experimental validation of the designed SSCB showcasing its protection capabilities is presented in Section 4.4. Finally, Section 4.5 summarizes the findings and draws the conclusions.

4.2. SSCB Considerations

This section provides an overview of the simplified DC system circuit employed to test and design the SSCB with LCL. In addition, some basic design parameters and features of SSCB design, including fault-dampening components are discussed.

4.2.1. Single-feeder system

To simplify implementation and analysis, a generic, simple DC system is proposed. This single-feeder system, illustrated in Fig. 4.1, retains the essential elements of more sophisticated DC systems while reducing complexity. The circuit includes a power supply modeled as an equivalent DC source with an anti-parallel diode. The latter emulates the diodes of a generator or grid connection with a rectifier, or the output port of an isolated DC-DC converter. A large DC-link capacitor with low equivalent series resistance (ESR) serves as the output filter. Transmission lines, mimicking cabling or bus bars, connect the generator to a DC bus equivalent, which includes the load. For protection design, testing focuses on the bus connection point, where typical faults such as overloads and pole-to-pole short circuits are more likely to occur.

4.2.2. Topology

Figure 4.2 presents the schematic of the SSCB employed as baseline design, which is part of the single-feeder testing circuit for validation. This SSCB topology allows for bidirectional power flow and protection, while utilizing SiC MOSFETs facilitates power scalability [53]. This configuration is also convenient for unipolar DC systems, with floating or high impedance grounding, which can reduce the severity of pole-to-ground faults [25]. The SSCB should feature protection of the negative pole in applications that employ different grounding schemes and bipolar DC systems. Conceptually, these circuit breakers are not significantly different and can be sold separately when purchased off-the-shelf.

The development of DC protection requires a structured framework that covers aspects such as protection device design, transient current analysis during faults,

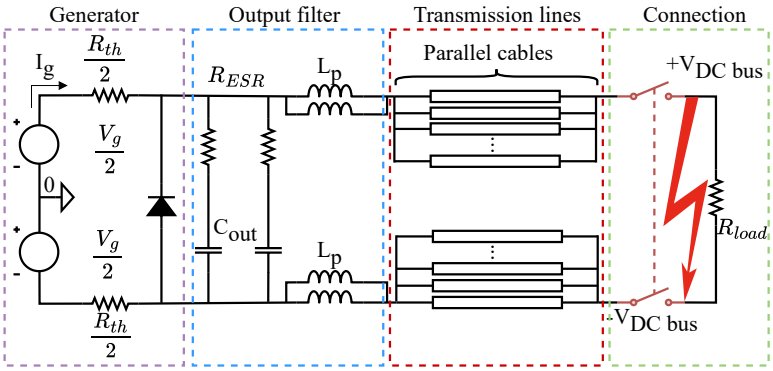


Figure 4.1: Simplified schematic of the DC system utilized in the study.

and accurate modeling of SSCB components. Several guidelines, such as [71, 97, 99, 155], are available in the literature. These procedures guide the design of application-specific SSCBs and include semiconductor selection, voltage clamping circuit or varistor, limiting inductance, component isolation, conventional gate driver and fault detection strategies.

When considering the upgraded design from Fig. 4.2, the key features of the SSCB are:

- **Decreased semiconductor stress:** High-speed detection prevents excessive current rising.
- **Time selectivity:** Current limiting keeps the current within safe values for relatively long periods.
- **Voltage oscillation attenuation:** The soft turn-off reduces possible voltage oscillations, avoiding sympathetic tripping.
- **No-load switch (NL_{SW}):** Provides circuit isolation.
- **RC damper (R_d C_d):** Enhances transient fault current behavior for better selectivity.
- **Dampening inductance (L_d):** Limits the current rate variation of a fault.
- **Fault detection** $v\,{}^{di}/_{dt}$**:** Monitors L_p voltage for fast short circuit detection.
- **Hall-effect current sensor (i_{HALL}):** Senses the current through the SSCB for the LCL functionality and serves as a secondary short circuit detector.
- **Power SiC semiconductor (SiC MOSFET)**: Manage bidirectional current flow, blocking and current limiting.
- **Metal-oxide varistor (MOV):** Provides overvoltage clamping across the semiconductors as a last resort.

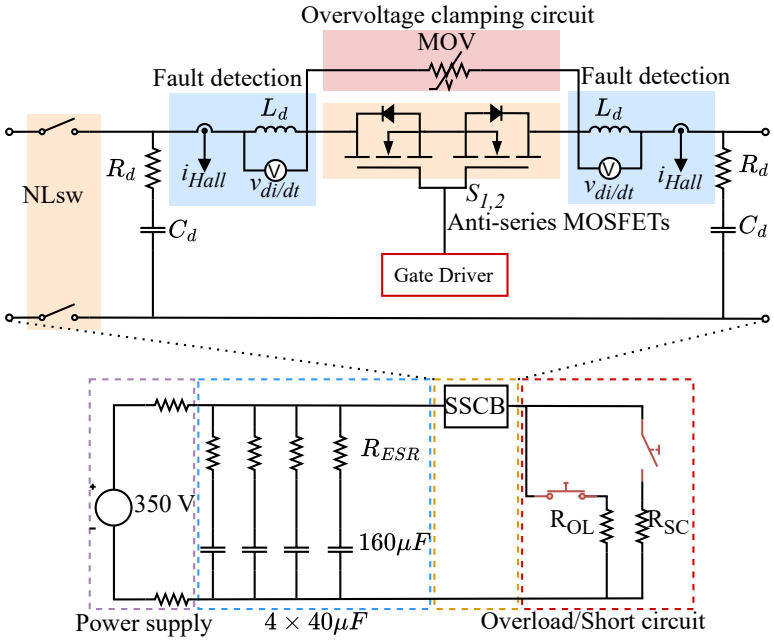


Figure 4.2: High-speed solid-state circuit breaker for DC systems. *Upper side:* Exploded view of the schematic with main components and zones. *Lower side:* Schematic of the tested DC system with floating ground with the SSCB.

- **Gate driver:** Customized to integrate LCL and high-speed breaking functionalities.

These elements collectively ensure robust and efficient operation of the SSCB, particularly under fault conditions requiring high-speed response.

The test circuit shown in Fig. 4.2 represents the single-feeder model of the primary DC system, including the power supply, capacitor bank, and fault branches. This configuration serves as a bridge between simulation and practical implementation.

Once the SSCB topology is known, the design of additional protection functionalities begins with an analysis of the fault conditions that require interruption and their associated behavior. Practical simplifications and assumptions guide the selection of passive components and power semiconductors in general. A detailed examination of DC short circuit currents, based on standards such as IEC 61660-1 for DC auxiliary systems [160] and IEC 62305-1 for lightning protection [176], leads to the development of fault response models. These models, described by (4.1) and (4.2), account for overdamped and underdamped current responses, respectively, forming the basis for the design and operation of the SSCB.

$$i_{SC}(t) = \frac{e^{-\alpha t}}{2\beta}\left[\frac{V_{nom}}{2L_p}\left(e^{\beta t} - e^{-\beta t}\right) + \beta I_g(0)\left(e^{\beta t} + e^{-\beta t}\right)\right] \tag{4.1}$$

$$i_{SC}(t) = e^{-\alpha t}\left[\frac{V_{nom}}{\omega_d L_p}\sin\omega_d t + I_g(0)\cos\omega_d t\right] \tag{4.2}$$

where $I_g(0)$ is the initial condition of the generator current, V_g is the generator voltage, which coincided with the rated SSCB voltage V_{nom}, L_p is the parasitic inductance of the output filter, and α, β and ω_d are (4.3) to (4.5) respectively.

$$\alpha = \frac{R_{ESR}}{4L_p} \tag{4.3}$$

$$\beta = \sqrt{\left(\frac{R_{ESR}}{4L_p}\right)^2 - \frac{1}{L_p C_{out}}} \tag{4.4}$$

$$\omega_d = \sqrt{\frac{1}{L_p C_{out}} - \left(\frac{R_{ESR}}{4L_p}\right)^2} \tag{4.5}$$

4.2.3. RCL damper design

The protection design focuses on reshaping the current waveform, particularly its rising characteristics. The RCL damper, shown in Fig. 4.2 as R_d, C_d and L_d acts as the first protection layer. During a fault, the initial pulse resembles a right triangle and can be approximated using a sawtooth model. This simplification allows the inductor to be designed based on (4.6), as described in [89].

$$2L_d = \frac{\sqrt{3}V_{nom}t_{max}}{I_{max}(t_{max})} \tag{4.6}$$

Equation (4.6) is valid when L_p, the inductance of the bus bar and the inductance of the transmission line are negligible. Otherwise, the equivalent inductance should be added, resulting in a lower L_d. The maximum current $I_{max}(t_{max})$ is a design objective, and should align with the maximum pulsed current rating of the semiconductor.

Given that L_d is commonly used in SSCB design as di/dt limiter, care must be taken during its selection. L_d should guarantee that the normal dynamic performance of the system is not compromised and that the maximum design voltage of the SSCB (V_{max}) is respected as (4.7).

$$2L_{d,max} \leq \frac{v_{max}t_{max}}{I_{max}(t_{max})} \tag{4.7}$$

A well-designed detection circuit and signal conditioning can help to reduce the peak current, minimizing semiconductor stress and decreasing power dissipation.

This approach enhances the overall lifetime of the device. The RC damper calculation complements the inductor selection and is derived from (4.8) and (4.9), based on the guidelines presented in [89, 97].

$$C_d >> \frac{t_{max}^2}{4\pi^2 2L_d} \tag{4.8}$$

$$2\sqrt{\frac{2L_d}{C_d}} < R_d < \frac{V_{L,max}}{I_{nom}} \tag{4.9}$$

Where C_d and R_d are the dampening capacitor and resistance, respectively, I_{nom} is the nominal design current, $V_{L,max}$ is the maximum acceptable voltage across L_d for short circuit detection, approximated as (4.10).

$$V_{L,max} \approx \frac{2I_{nom}2L_d}{t_{max}} \tag{4.10}$$

During SSCB commissioning, $V_{L,max}$ must be recalibrated to ensure proper operation under the specific system conditions.

4.3. Three-level gate driver design

After designing the SSCB parameters, focus shifts to the integrated three-level gate driver and its operation. Incorporating the LCL in the SSCB is particularly worthwhile in isolating faulted circuits while maintaining the functionality of the remaining system. This is valuable in satellites, where isolating a failed subsystem ensures the undisturbed operation of other payloads [177, 178]. A quick response to a fault reduces energy losses due to prolonged overcurrent or thermal damage, improving overall system efficiency and reliability [172, 177].

The work in [178] shows a LCL with a complex structure, segregating the controller, telemetries, and logic as building blocks in a photolithography-based construction. Moreover, the limited response time (milliseconds) and the overall burden of producing custom chips make this approach unfeasible. Although [173] shows a simpler design, the complications related to the analog design and the magnetic isolation remain substantial, while the response time falls within hundreds of microseconds. The design in [177] uses a conventional LCL with limited details about the control and internal electronics. The application is for a low voltage subsystem, in which the time response is close to 2 ms. Off-the-shelf, space-rated devices, like those described in [173, 179], require advanced control and measurement circuits that are not typically required for less demanding applications.

This research exploits existing gate drivers to achieve a simple and robust SSCB with integrated LCL. Research highlights the critical role of precise gate driver tuning in achieving safe and effective breaking action [90, 93, 180]. This is considered for the conceptual architecture of the integrated three-level gate driver, shown in Fig. 4.3, utilized for this work.

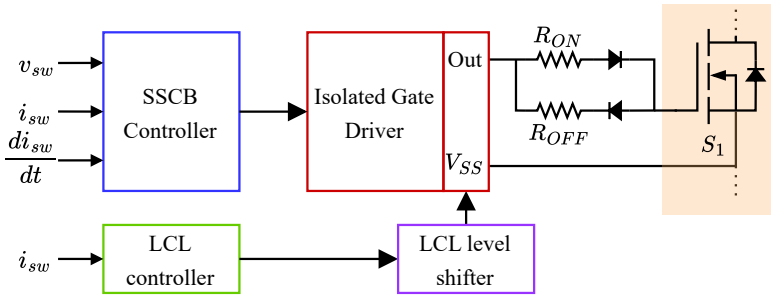


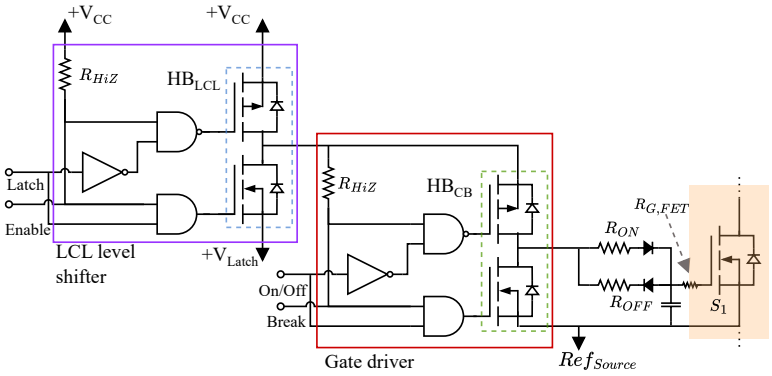
Figure 4.3: Functional blocks architecture of the integrated gate driver implemented for breaking and current limiting in the SSCB. *Adapted from [180].*

The SSCB controller integrates closely with the gate driver logic, monitoring the drain-source voltage of the power switch (v_{DS}), the drain current (i_{D}), and its rate of change $\mathrm{d}i_{\mathrm{D}}/\mathrm{d}t$. Short circuit protection is primarily governed by $\mathrm{d}i/\mathrm{d}t$ sensing, while average current serves as a supplementary parameter. The gate driver design can incorporate a commercially available component with an *enable* pin, paired with an isolation stage and a soft turn-off network. The proposed gate driver topology, denoted as a three-level, employs two identical off-the-shelf gate drivers in cascaded disposition as depicted in Fig. 4.4a.

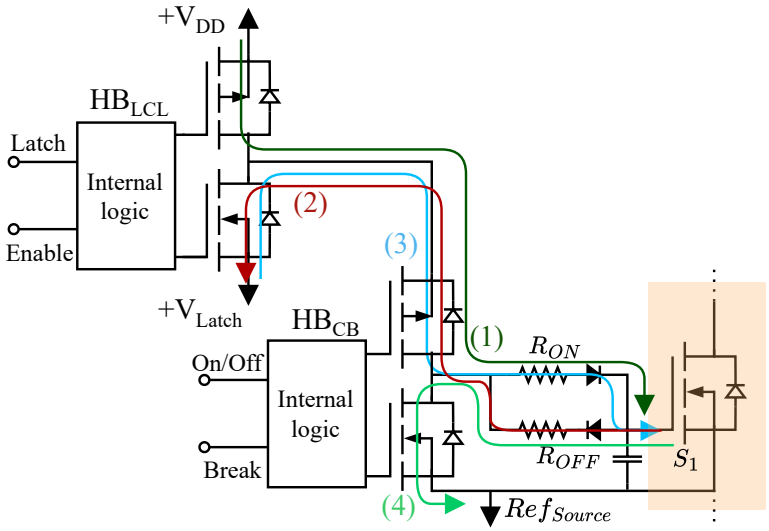
The LCL half-bridge ($\mathrm{HB_{LCL}}$) acts as the power supply for the circuit breaker half-bridge ($\mathrm{HB_{CB}}$) that ultimately drives the power switch S_1. $\mathrm{HB_{LCL}}$ is the LCL level shifter, fed by $+V_{\mathrm{DD}}$ on the positive port, supplying normal gate voltage to S_1. The low-side voltage in $\mathrm{HB_{LCL}}$ defines the LCL voltage $+V\mathrm{LCL}$. The current paths in the gate driver for the different operation modes are illustrated in Fig. 4.4b, where *path (1)* is active during normal turn-on and when the LCL turns-off, and *path (4)* for normal turn-off and breaking. *Paths (2)* and *(3)* are necessary for the LCL functionality. *Path (2)* becomes active when the LCL command signal is set on, then v_{GS} decreases from $+V_{\mathrm{DD}}$ to $+V_{\mathrm{LCL}}$, partially discharging the parasitic capacitor in the switch. Complementarily, *path (3)* allows the $+V_{\mathrm{LCL}}$ voltage to be maintained until the LCL signal is off. The *enable (and break)* pin adds an additional safety layer by forcing the gate driver into a high impedance, when the logic signal is off. Details about the controller are explained later in this section.

The proposed configuration facilitates precise tuning of the SSCB's dynamic behavior during turn-on and off, and current limiting. Gate resistors R_{ON} and R_{OFF} are used to adjust the dynamic response of the gate driver. The sink-source capability of the gate driver depends on the gate loop resistance, determined by its output stage, diodes, and gate resistors, as formulated in (4.11) to (4.13). This setup ensures the SSCB operates reliably under varying conditions.

$$I_{\mathrm{ON}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{GDF}}}{\chi \mathrm{R_{OH}} + \mathrm{R_{ON}} + \mathrm{R_{G_{FET}}}} \tag{4.11}$$



(a)



(b)

Figure 4.4: Proposed three-level gate driver topology with soft turn-off network for a SSCB with integrated LCL. (a) Implementation of the gate driver including internal logic circuitry. (b) Simplified schematic with current flow indications. *Path (1) is active when the SSCB is on, path (2) applies when the LCL starts, path (3) is used when holding the LCL gate voltage, and path (4) when the SSCB is breaking or turned off.*

$$I_{\mathrm{OFF}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{GDF}}}{\mathrm{R_{OL}} + \mathrm{R_{OFF}} + \mathrm{R_{G_{FET}}}} \tag{4.12}$$

$$I_{\mathrm{LCL}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{GDF}}}{\mathrm{R_{OH}} + \mathrm{R_{OL}} + \mathrm{R_{OFF}} + \mathrm{R_{G_{FET}}}} \tag{4.13}$$

Where V_{GDF} represents the forward voltage of the gate diodes, $\mathrm{R_{OH}}$ is the pull-up resistance in source mode, $\mathrm{R_{OL}}$ is the pull-down resistance in sink mode, $\mathrm{R_{G_{FET}}}$ denotes the gate resistance of the power switch, and χ is equal to 1 when the SSCB operates normally, and equal to 2 when the LCL is active. Both $\mathrm{R_{OH}}$ and $\mathrm{R_{OL}}$ are part of the gate driver, and are embedded in the transistors in $\mathrm{HB_{LCL}}$ and $\mathrm{HB_{CB}}$ for the high and low levels respectively.

The LCL controller in Fig. 4.3 modulates the gate signal during LCL operation. It monitors i_{D} and dynamically adjusts the gate signal voltage by controlling the auxiliary power supply. Since the power supply is a commercial component, a voltage adjustment circuit, referred to as the *LCL level shifter*, is incorporated into the design. Ultimately, this architecture is realized with the three-level gate driver, and the level shifter corresponds to $\mathrm{HB_{LCL}}$. This circuit, directed by the LCL controller, drives the power MOSFET (S_1) into its linear region, increasing the equivalent device impedance $\mathrm{R_{DSON}}$ and introducing controlled power losses to effectively limit the current flow for a short period. Since the gate turn-on and off characteristics of IGBTs present nonlinearities [174], carefully operating in the linear region becomes challenging, which makes them less suitable for this research. Consequently, SiC MOSFETs are preferred for the SSCB design.

4.3.1. Protection Control design

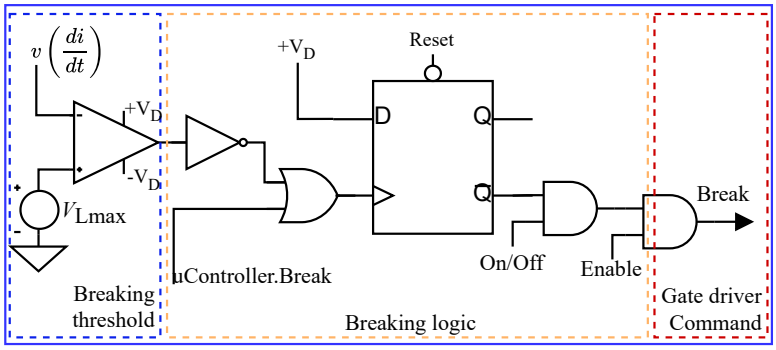
Integrating a SSCB with an LCL requires the design of a suitable controller for the gate driver. This section presents the controller that governs the breaking and the current limiting functionalities in the three-level gate driver. The simulation of both protection cases is also discussed in this section.

The primary function of the control circuit is to precisely manage the parasitic gate-source capacitance of the power MOSFETs. According to (4.14), the adjustable parameter is V_{GS}, which the gate driver modulates by charging and discharging this capacitance to achieve the desired control. This careful management of V_{GS} ensures accurate and reliable operation of the integrated protection system.

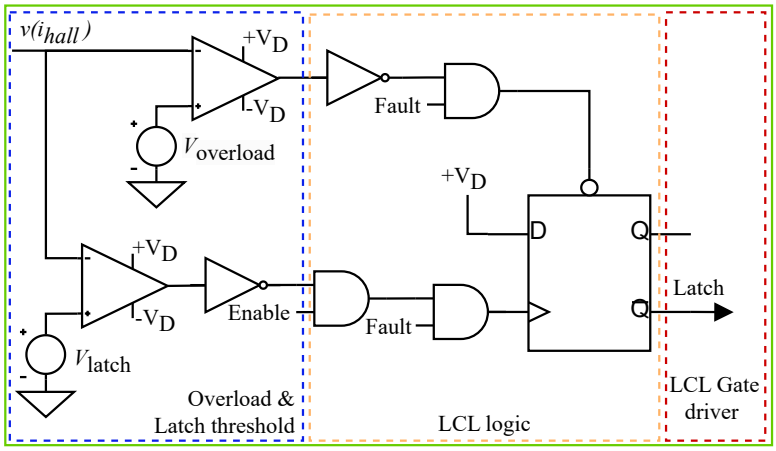
$$\mathrm{C_{gs}} = \frac{\mathrm{Q_{gs}}}{V_{\mathrm{GS}}} \tag{4.14}$$

The gate driver must support two distinct control modes: high-speed breaking for short circuit protection and current limiting for LCL operation. Both control modes require inverted logic signals, meaning that the on-state (logic high) indicates that breaking and/or LCL functionalities are off.

High-speed breaking The breaking logic sequence, illustrated in Fig. 4.5a, monitors the voltage across $\mathrm{L_d}$ and compares it to a reference value $V_{\mathrm{L,max}}$. This reference is established during the design phase based on load characteristics, ensuring the SSCB trips under appropriate fault conditions. As this functionality is



(a)



(b)

Figure 4.5: Schematic of analogue control circuits. (a) Breaking latched $^{di}/_{dt}$ control circuit. (b) Latching current limiter control circuit. *Note that "Latch" and "Break" signals are normally ON.*

time-sensitive, it requires critical components such as high-bandwidth comparators and logic gates to have minimal propagation delays (in the order of tens of nanoseconds).

The high-speed breaking controller's operation was tested in simulation, with the main results presented in Fig. 4.6. In Figure 4.6a the gate driver voltage transitions from 10 V to 0 V. The fault current, depicted in Fig. 4.6b, reaches approximately 92 A with a rise time of about 250 ns and a clearance time near 950 ns. These results suggests low stress on the semiconductor, with the surge current remaining well within its maximum current pulse rating.

Figure 4.6c shows the voltage across the SSCB. Initially a high-speed surge is observed, stabilizing momentarily, as the driven signal reacts. The gate driver's

effect becomes evident when the voltage across the SSCB increases as expected. The simulation results indicate reduced reliance on the MOV for voltage clamping, which may enhance system reliability. However, detailed studies on MOV and its long-term performance longevity are beyond the scope of this research. These findings demonstrate the controller's effective performance and its potential for real-world application.

Current limiting The primary design consideration for the LCL is its response time, as it must suppress current surges rapidly without disrupting system dynamics. In marine applications, components adhere to standards such as IEC 62040-3:2021, which specify an overload factor of 1.2 for a duration of 100 s [181]. Furthermore, the LCL controller adopts a hiccup modulation strategy, a well-established method for protecting power converters during overload conditions by temporarily inhibiting PWM signals [182].

To achieve proper operation, the LCL design incorporates two set-point com-

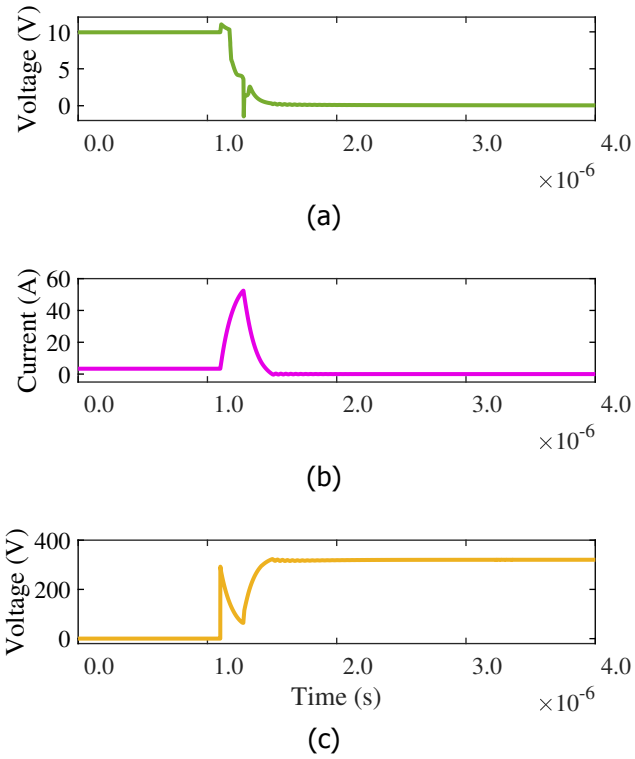


Figure 4.6: Simulation of the SSCB to validate the performance of the high-speed short circuit controller. (a) Gate-source voltage of the power switch. (b) Current through the SSCB. (c) Voltage across the SSCB.

parators with similar propagation delay, as shown in Fig. 4.5b. Timing of the LCL controller is key for efficient current limiting. High-speed components are necessary to obtain a fast LCL that avoids transient overcurrents, excessive losses and load disturbances. The overload state (V_{overload}) is detected using a high-speed comparator and a high-bandwidth hall-effect current sensor, with the current measurement signal $i(t)$ conditioned as $i(t) = \text{SF}v_{(i_{\text{hall}})}$, where SF represents the scale factor for signal conditioning. The overcurrent state (V_{LCL}) triggers the LCL mechanism, providing the falling edge for the D-latch. The LCL resets when the current returns within nominal limits, as described by (4.15a) to (4.15c). Specifically, the LCL is triggered when $i(t)$ surpasses $1.2I_{\text{nom}}$. Once the current decreases below the nominal region, the LCL resets, ensuring seamless operation and effective suppression of transient overcurrents.

$$i(t)\begin{cases}\text{Nominal}, & i(t) < I_{\text{nom}} \quad (4.15a)\\ \text{Overload}, & 1.2I_{\text{nom}} > i(t) > I_{\text{nom}} \quad (4.15b)\\ \text{LCL}, & i(t) \geq 1.2I_{\text{nom}} \quad (4.15c)\end{cases}$$

The gate driver requires an adjustable power supply that becomes active during limiting phase of the LCL operation. During this phase, the source primarily acts as a sink for the gate charge (Q_{gs}) by pulling down v_{GS} to a predefined value V_{LCL}, as described in (4.16).

$$+V_{\text{CC}} > +V_{\text{LCL}} > V_{\text{th}} \quad (4.16)$$

This adjustment reduces v_{GS} from its normal $+V_{\text{CC}}$ to a level above the threshold voltage (V_{th}), enabling current limitation. Since this type of modulation counteracts the excess current in the protected system with heat dissipation in the SSCB, limiting the LCL time in accordance with the semiconductor parameters is essential. The practical implementation of the LCL requires the analysis of the dissipated energy (E_d) in (4.17), which gives the virtual junction temperature rise (ΔT_{vj}) in (4.18).

$$E_{\text{d}} = V_{\text{DS}} I_{\text{D}} t_{\text{LCL}} \quad (4.17)$$

$$\Delta T_{\text{vj}} = E_{\text{d}} Z_{\text{th(j-c)}} \quad (4.18)$$

Where t_{LCL} is on-time of the LCL, measured from the drop until the recovery of v_{GS}, and $Z_{\text{th(j-c)}}$ is the junction-case thermal impedance of the semiconductor. The LCL controller must guarantee that T_{vj} does not exceed 80% of the reported maximum, as advised by manufacturers. However, a more conservative value should be used whenever possible. A practical estimation is possible by assuming that the current waveform due to the LCL is triangular, and that the temperature rise is equal during every LCL cycle (constant duration). The number of LCL cycles for a given ΔT_{vj} is calculated using (4.19).

$$\text{Cycles}_{\text{LCL}} = \frac{2\Delta T_{\text{vj}}}{I_{\text{D}} V_{\text{DS}} t_{\text{LCL}} Z_{\text{th(j-c)}}} \quad (4.19)$$

Since the duration of each cycle is known, the number of cycles gives a rough estimation of t_{LCL} as an absolute maximum when using nominal parameters. A safety margin of at least 10% is recommended. Calculating the total t_{LCL} is relatively straightforward by using the microcontroller break signal in Fig. 4.5a. The controller can implement (4.20) to determine t_{LCL} and compare it with the maximum LCL time $t_{LCL,max}$.

$$t_{\mathrm{LCL,max}} \leq \int t_{\mathrm{LCL}}(t)\ \mathrm{d}t \tag{4.20}$$

Where $t_{\mathrm{LCL}}(t)$ is a boolean signal according to (4.21b) and (4.21a).

$$t_{\mathrm{LCL}}(t) \begin{cases} 0, & \text{LCL off} \quad (4.21a) \\ 1, & \text{LCL on} \quad (4.21b) \end{cases}$$

The LCL control circuit was simulated with the SSCB, and the key results are presented in Fig. 4.7.

The simulation uses a reduced source voltage of 50 V and an overcurrent setpoint of 3.3 A to align with experimental results (Section 4.4). During LCL, v_{GS} drops to

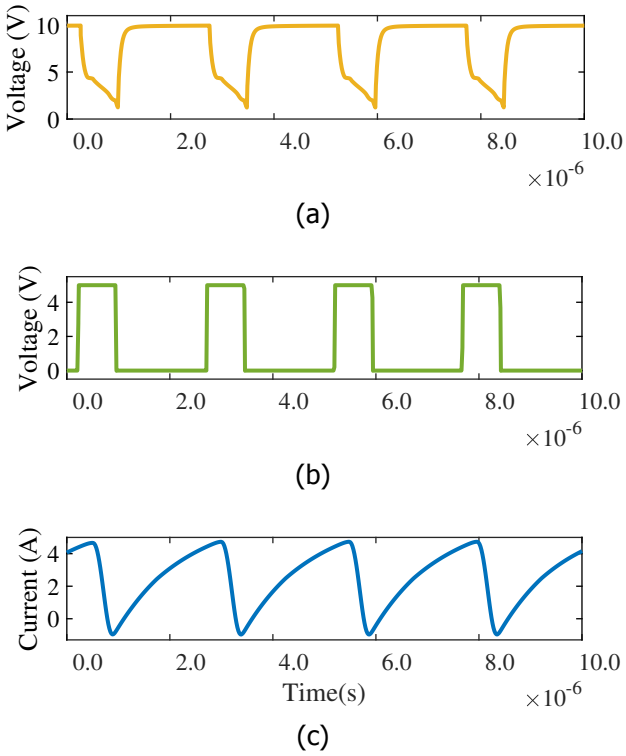


Figure 4.7: Simulation of the SSCB in overcurrent to validate the operation of the LCL. (a) Gate-source voltage of the power switch. (b) LCL logical command. (c) Current through the SSCB.

V_{LCL}, reducing Q_{gs}, approximately following (4.12). Once the current returns to nominal levels, the LCL deactivates, and v_{GS} returns to its normal operating value of 10 V.

The gate driver behavior during current limiting is depicted in Fig. 4.7a, with corresponding command signals in Fig. 4.7b. These signals synchronize with the gate voltage v_{GS} and the SSCB current, which oscillates as the LCL activates and deactivates (Fig. 4.7c).

The current rises approximately 3.5 A, exceeding the LCL threshold, at which point the LCL forces it back, recovering once it returns to the nominal levels.

In scenarios where the overcurrent persists, the LCL triggers the SSCB to trip, preventing semiconductor overheating. Notably, current zero-crossings are observed in Fig. 4.7c, caused by circuit inductance and the reduced DC voltage of 50 V during the simulation. This phenomenon, also observed in the experimental setup, can be mitigated by operating at the nominal SSCB design voltage of 350 V, which would reduce output voltage drops and improve LCL performance. Further validation of these findings, including tests at nominal voltage, is beyond the scope of this research.

4.3.2. Design summary

Designing DC protection is an ever-evolving process that does not have a generalized procedure. The standard design of SSCB tends to follow diverse sets of requirements, since a converging regulation is missing and unlikely to materialize. Furthermore, LCLs are used mainly in aerospace, and there is no broadly established framework for standardizing their design across other industries. Design guidelines from aerospace regulators, such as the European Cooperation for Space Standardization (ECSS) [171], offer valuable insights. This section summarizes the design of the upgrades proposed for the SSCB with LCL. The design assumes a generic SSCB following specific regulations and objectives, used as a platform for the implementation of the enhancement functionalities.

Figure 4.8 exhibit the simplified procedure, extracted from Sections 4.2, 4.3 and 4.3.1, utilized as the design structure for this investigation. These guidelines can be adapted to suit several DC applications, enabling the transfer of key principles while addressing their unique challenges. The process begins with understanding the application, assumed as received information about the use case, regulations, testing requirements, and overload and derating factors. System parameters such as voltage, current, connected passive components, and grounding schemes must be clarified during the analysis, resulting in the definition of nominal and maximum values. In addition, short circuit current studies can be performed to guide the overall design and provide a reference of the effect of the designed SSCB.

The selection of the power switch mainly takes into consideration parameters such as voltage class, nominal current, maximum drain current, short circuit withstand time, on-state resistance, power dissipation, gate voltage threshold, turn-off delay, gate charge, thermal impedance, virtual junction temperature, and the safe

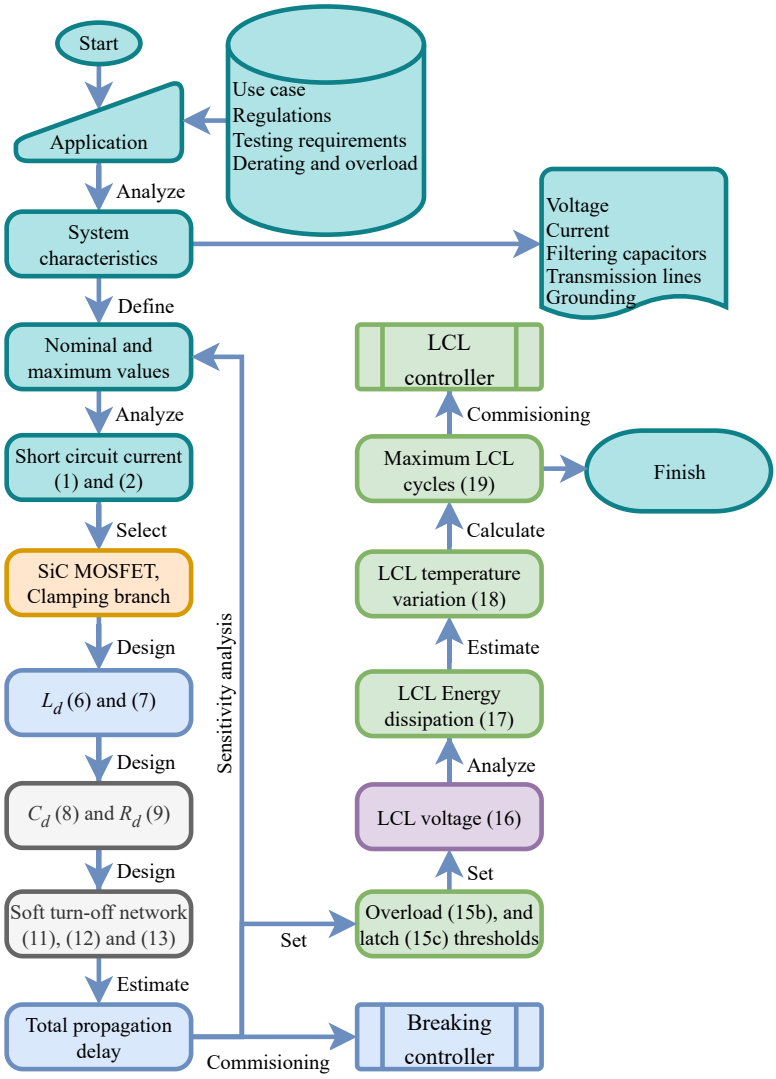


Figure 4.8: Simplified design process of a generic SSCB with LCL. *Numbers in blocks:* Reference to equations in the document.

operating region. It is handy to employ switch selection guidelines as in [97, 183], focusing on the tripping characteristics of the circuit breaker and how it matches the safe operation region of the switch. Additional parameters used during standard power electronics design should also be considered.

The voltage-clamping branch is essential in a generic SSCB design. Opting for a MOV or an RCD snubber is an application-specific choice. The guidelines in [74] discuss the selection requirements for the MOV. [99] illustrate the trade-offs of using

the RCD snubber in a bidirectional SSCB. The final choice and selection depends on the application and the expected short circuit characteristics. Ultimately, the designer should consider reliability constrains, since the voltage clamping branch can be exposed to significant stress.

The remainder of the procedure follows an iterative design, based on previously discussed parameters, in the form of a sensitivity analysis to achieve adequate performance. Some reference values should be commissioned, calibrated, or set during the process flow given that the controller governs the operation of the power stage. The outcome of the design process for this research is summarized in Table 4.2.

4.4. Experimental validation

After completing simulations and determining hardware recommendations, an experimental setup was established to validate the results. This setup replicates the generic DC system, including power supplies, capacitor banks, loads, protection devices, and a short circuit forcing branch (Fig. 4.2). Both transient and steady-state responses were analyzed to refine the simulation model and validate key functionalities. The high-speed breaking and LCL functionalities were tested using an SSCB prototype with an integrated gate driver. The results were compared against commercial-off-the-shelf solutions to highlight improvements. Such a comparison is valid to some extent, given that the employed power SiC MOSFETs

Table 4.2: SSCB design parameters from the proposed design guidelines.

Parameter	**Value**
Overload factor	1.2
Dampening inductance L_d	0.47 µH
Dampening capacitor C_d	300 nF
Dampening resistance R_d	4.3 Ω
On resistance R_{ON}	4.64 Ω
Off resistance R_{OFF}	9.28 Ω
Breaking delay*	38 ns
Clearing time*	≈200 ns
LCL threshold	3.2 A
LCL maximum temperature rise	25 K
Energy per LCL cycle E_d	6.6 µJ
Temperature rise per LCL cycle	2.18×10^{-6} °C
Maximum LCL cycles	22957000
Maximum LCL time $t_{\mathrm{LCL,max}}$	22.7 s
Maximum LCL time @350 V, 10 A	7.57 s
Actual LCL time	20 µs
LCL delay*	250 ns

* Measured value

are expected to behave similarly with higher current ratings. In contrast, some DC systems on ships or heavy duty vehicles may require parallelization of power semiconductors to reach the required ratings, and further testings is necessary. However, it is noteworthy that certified LCLs outside spacecraft applications are scarce or unavailable, highlighting the added value of this work.

The key parameters of the test circuit are summarized in Table 4.3. Figure 4.9a shows the implemented SSCB, which is primarily commanded via optical fiber to enhance safety and communication speed. High-speed breaking and LCL controllers were developed using discrete components, leveraging their superior timing characteristics compared to digital controllers. The experimental setup, illustrated in Fig. 4.9b, includes a power supply, a low-impedance film capacitor pack for short circuit testing, and an SSCB connected to an overload branch (*not visible in the figure*). The prototype, shown again in Fig. 4.10, consists of three boards. The gate drive board (blue), the LCL controller and safety board (red), and the SSCB power board (green). The main components and instruments used are listed in Table 4.4.

Care must be taken when selecting the commercial gate driver, since a high impedance output option, and a relatively low undervoltage lockout are necessary. The former prevents the MOSFET from false-gating when the SSCB has tripped, and the latter allows for a broad range of V_{LCL} without shutting down the gate driver during LCL. Although it was not necessary for this research, implementing a negative bias turn-off for the power switch can enhance false-gating immunity. This becomes unavoidable when relatively high-magnitude electromagnetic interference is present.

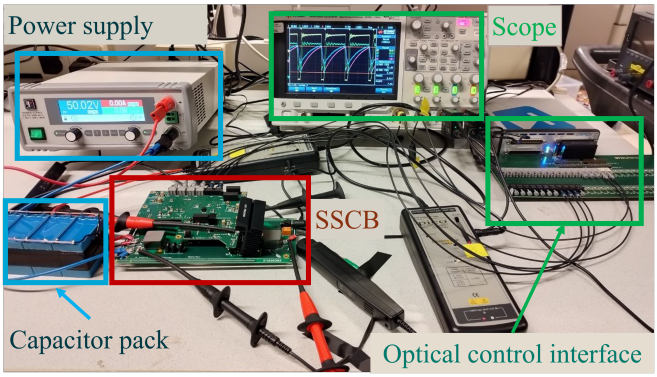
Due to practical limitations and simplification efforts during testing, the external power supply generated a gate voltage lower than the device manufacturer's recommended value. However, a significant performance variation for both short circuit and LCL is not expected and the results are conclusive.

Table 4.3: System and circuit breaker parameters.

Parameter	**Value**	**Subsystem**
Nominal voltage V_{nom}	350 V	Generator
Filter capacitance C_{out}	160 µF	Output filter
Capacitor ESR	1.325 mΩ	Output filter
Parasitic inductance* L_p	250 nH	Output filter
Nominal current I_{nom}	10 A	Generator, SSCB
On-resistance (FET) R_{DSON}	≈ 39 mΩ	SSCB
Drain-source reverse voltage	≈ 3.8 V	SSCB
Peak source current	9 A	Gate driver
Peak sink current	9 A	Gate driver
Line inductance	8.32 µH	Load
Load resistance	8.9 Ω	Load

* Estimated value

(a)



(b)

Figure 4.9: Implementation of the single-feeder setup and the SSCB for testing. (a) Experimental high-speed SSCB concept design. (b) Testing setup with main components.

4.4.1. Breaking mode

The high-speed breaking functionality was validated using the circuit in Fig. 4.2. Two scenarios were tested: the performance case, with the high-speed controller, and the reference case, where the propagation delay of the controller is comparable to commercially off-the-shelf SSCBs. The breaking mode performance experiment was conducted by directly shorting the output port of the SSCB with the negative port of the capacitor pack. The result, shown in Fig. 4.11, presents v_{GS}, at the top, reacting to the short circuit after approximately 98 ns of propagation delay from the fault instant. The detection delay allows the breaker current I_{SSCB} to increase (*from zero*), reaching a peak value of about 20.9 A with a rise-time of approximately 102 ns. The total fault time is close to 356 ns, which is approximately 254 ns after

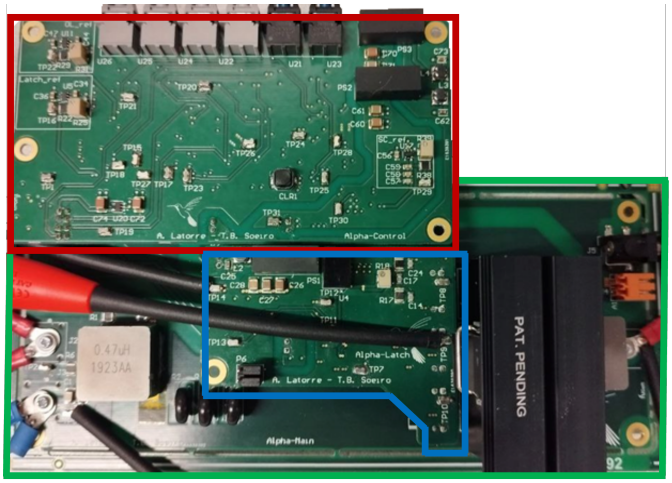


Figure 4.10: Implementation of the solid-state circuit breaker with latching current limiter using the three-level gate driver. *Green:* Power board, *red:* control board, *blue:* three-level gate driver board.

Table 4.4: Main components employed to implement the SSCB.

Component	Reference
Gate driver	
Commercial gate Driver	IXYS IXDD609SI
Schottky diode	Nexperia PMEG2010EPK
Power stage	
SiC MOSFET	Infineon IMW120R040M1H
MOV	Panasonic ERZV10D431
Capacitor	EPCOS B32776G4406K000
Sensors and control	
Hall-effect sensor	Allegro ACS37032LLZATR
High-speed rail-to-rail comparator	TI TLV3601
High-speed OR gate	TI SN74LVC1G32-EP
High-speed AND gate	TI SN74LVC1G11-Q1
High-speed Inverter gate	TI SN74LVC3GU04
High-speed D-Latch	TI SN74AHCT74DR
Measurement	
Current probe	Micsig CP1003B
Differential probe	Micsig DP700
Differential probe for LCL	Pico TA043
Scope	Keysight DSOX3024A

the breaking time.

The experimental results in Fig. 4.11 surpassed the simulation predictions, showing similar response times but with peak current magnitudes reduced to approximately 60% of the simulated values. These discrepancies arise from testing circuit characteristics, where the inductance was estimated and reduced.

Furthermore, Fig. 4.12 highlights the benefit of the proposed SSCB; its low propagation delay allows the breaker to interrupt the fault before the current rises excessively, thereby reducing stress on the semiconductor devices. For comparison, commercial SSCB products from AstrolKWx [80] and ABB [72, 98] exhibit significantly longer propagation delays. This is illustrated by a failed current blocking experiment, in which a delay of about 3 µs, comparable to those commercial products, caused destructive overcurrent in the semiconductor. In contrast, the proposed high-speed SSCB, with its narrow operation window and fast control action, achieves timely interruption without the need for large device oversizing.

In contrast, the failed experiment shows large fluctuations with delayed breaking action from electronics. The MOSFET is likely overheating when the command occurs since it takes only a few microseconds to destroy it.

4.4.2. Hiccup mode

To validate the LCL functionality, the circuit shown in Fig. 4.2 was used, with the corresponding experimental setup depicted in Fig. 4.9b. The DC voltage was set to 50 V, and the LCL threshold was established at 3.3 A, consistent with the simulation parameters. From (4.19), the maximum LCL time for the conditions of the experiment is around 1.3 s, estimated for a junction temperature rise of 25 K. In nominal

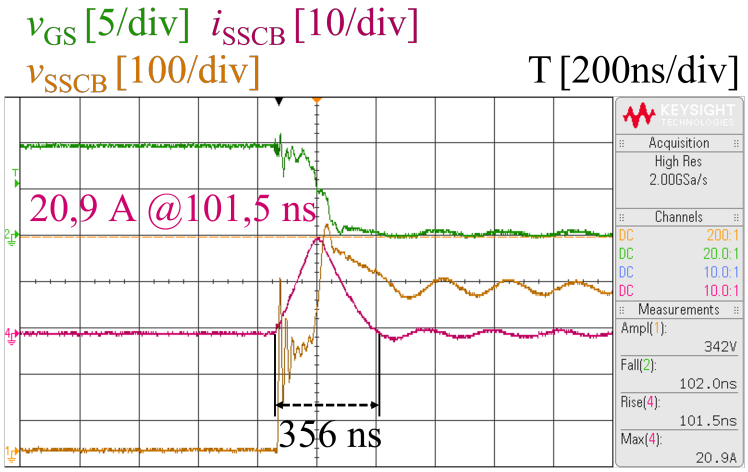


Figure 4.11: Scope snapshot of short circuit test for the proposed high-speed SSCB. *Green-top:* v_{GS}, *magenta: middle:* i_{SSCB}, *yellow-bottom:* v_{SSCB}.

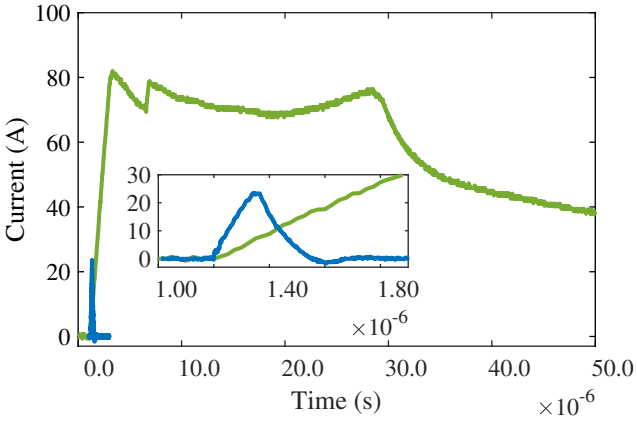


Figure 4.12: Short circuit current through the SSCB comparison for two cases of propagation delay. *Green-top:* 3 µs delay, *Blue-bottom:* 80 ns. *Inset:* Detail of the low propagation delay test, achieved with the designed gate driver.

design conditions (350 V, 10 A), it would decrease to around 150 ms for the same junction temperature rise.

The experimental results, presented in Fig. 4.13, demonstrate the v_{GS} response of the gate driver to command signals, with a measured propagation delay of approximately 150 ns. This alignment between experimental and simulation parameters confirms the successful validation of the LCL functionality.

When the LCL threshold is reached, the SSCB reduces v_{GS} to V_{LCL}, increasing R_{DSON} and forcing the current to decrease. Once the current returns to nominal levels, the latch is released, restoring v_{GS} to its normal value. The command delay causes the current to drop further than necessary, creating oscillations in i_{SSCB} due to circuit inductance.

The results validate the LCL functionality with minimal modifications to a conventional SSCB. Despite the reduced test voltage of 50 V, the current remained within safe limits and no false tripping occurred. This was verified with the v_{GS} measurement and the command signal, as they do not drop to zero at any point. The employed independent detection mechanisms ensured that $\mathrm{d}i/\mathrm{d}t$ fluctuations did not exceed the breaking threshold, while the hall-effect sensor effectively managed the LCL control. This demonstrates that the LCL design proposed in this work achieves adequate current limitation without compromising system integrity, and expanding selectivity.

4.4.3. Future work

The technology developed in this work is versatile and applicable beyond transportion due to its relatively simple design. Although the design is for a general DC

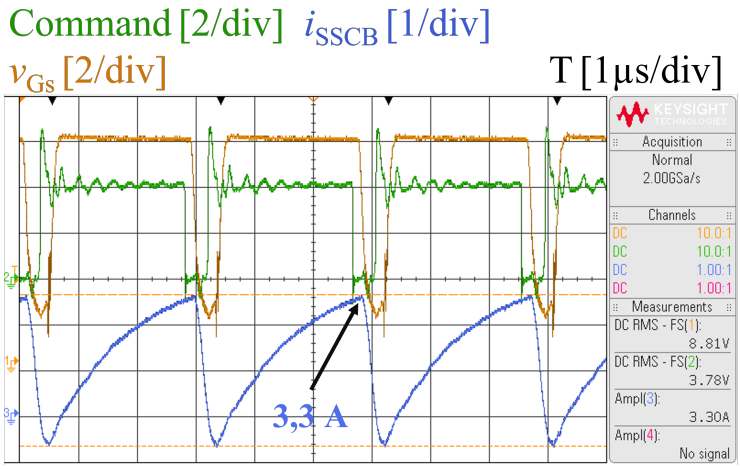


Figure 4.13: Scope snapshot of the SSCB operating as LCL with the proposed gate driver. *Yellow-top:* v_{GS}, *green-middle:* LCL command signal, *blue-bottom:* i_{SSCB}.

system in transportation, various applications, such as datacenters and residential buildings, have compatible protection requirements and could benefit from the proposed solution.

The SSCB with LCL in this research requires further studies to confirm its suitability for high-power DC applications. To further enhance this research, the following areas are proposed for future investigation.

- **Loss estimation:** Accurate calculation of semiconductor losses during LCL is required to minimize wear and estimate component lifespan. The design requires further study of component selection, thermal management, and current balancing. Additionally, the SSCB's efficiency must be characterized by measuring power losses under nominal conditions.
- **FPGA Implementation:** Deploying protection controllers on FPGAs could streamline hardware design, reduce costs, enable field updating, and increase flexibility without PCB modifications. Comparative benchmarking against the analog controller used in this work is essential to quantify tripping delay, false tripping, PCB relative complexity and possibly electromagnetic interference immunity.
- **Scalability testing:** The scalability of the SSCB prototype, designed for parallel MOSFET configurations, should be assessed. Testing the LCL under higher average currents is necessary to validate the suitability of the proposed SSCB with LCL for high power DC systems. In such case, self-sufficient modules comprised of a three-level gate driver and MOSFET are necessary. Furthermore, including a buck converter on the gate driver would increase

the flexibility of the third voltage level, which could facilitate the balancing of power losses among MOSFETs during LCL operation.

4.5. Outlook and conclusion

The development of advanced protection technologies is vital for the widespread adoption of future mobile DC systems, which are critical for sustaining modern transportion. DC protection is an enabling technology, yet current limitations hinder the adoption of DC power systems, particularly in high-power transportation systems.

This work demonstrates that existing, robust SSCB technology can be significantly improved with modifications to its control mechanisms that are relatively simple to implement. The proposed three-level gate driver architecture enables the integration of high-speed SSCBs and LCLs using a shared front-end, enhancing selectivity and reducing system complexity. The proposed SSCB demonstrated a clearing time close to 200 ns, with a peak current of 20.9 A. The LCL functionality based on the three-level gate driver was also demonstrated, limiting the current to 3.3 A for 20 µs. Experiments suggest that the proposed SSCB can reduce unnecessary tripping while containing severe short circuits, which is necessary for several applications. A comprehensive guideline to upgrade and implement a LCL in a SSCB highlights the relevance of this research for the development of DC systems in general.

This approach is particularly relevant given the high cost and perceived value of DC protection technologies currently on the market. By incorporating additional functionalities, such as LCLs, into existing platforms, the value and feasibility of these solutions grows. LCL technology, adapted from aerospace, can be customized for less demanding applications to avoid unnecessary disconnection of critical loads during key operations.

By enabling advanced protection functionalities without the stringent requirements of aerospace systems, these innovations can promote the adoption of DC systems in diverse applications. This would unlock significant potential for cleaner energy technologies based on DC systems, contributing to a more sustainable future.

5

Electronic Capacitor-based Protection for Converter-Interfaced DC systems

This chapter presents a proof-of-concept of a DC-DC converter with embedded fault protection. The proposed DC protection module, based on the concept of an electronic capacitor, is experimentally validated on a 10 kW LLC converter prototype. Results show that solid-state circuit breaker technology can provide effective converter protection with only modest design complexity. By placing the protection module in series with the DC-link capacitor, the processed power is significantly reduced, leading to a proportional reduction in semiconductor conduction losses compared to conventional protection schemes where the solid-state circuit breaker is in series with the converter. The protection module is compact, relatively simple, and remains compatible with fuses for improved selectivity. These findings highlight a practical and efficient protection approach that can accelerate the adoption of DC power systems, with particular relevance for converter-interfaced DC microgrids supporting the energy transition.

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Photo by Mauricio Latorre, Mutiscua, Colombia

The spectacled bear moves quietly through the cloud forests, a solitary presence yet deeply tied to the rhythms of its land. By feeding on fruits, leaves, and bromeliads, it leaves behind both traces of its passage and the seeds of renewal, sustaining a world larger than itself.

5.1. Background

Protecting DC power systems remains a major obstacle to their widespread adoption [5]. The absence of natural current zero crossings, combining with low impedance and large DC-link capacitors, make fault interruption particularly challenging [54, 58]. Consequently, pole-to-pole short circuits can severely damage components and cause partial or total system failures. Protection strategies are application-specific and depend on the regulatory context. For example, some DC ships use high-speed fuses and mechanical DC circuit breakers (MCB) [25, 158], whereas others combine solid-state circuit breakers (SSCBs) and MCBs [81, 97]. High voltage DC transmission systems often employ hybrid circuit breakers (HCBs) [5]. Aerospace applications may use solid-state current limiters [173], and some studies investigate breakerless protection, based mainly on power converters control and the optimal design of their output capacitors [29, 59].

Ultimately, these solutions involve trade-offs in protection effectiveness, efficiency, power density, and response time, forcing system designers into complex design processes.

This chapter proposes a converter-integrated protection approach that embeds a protection module in the topology of a bidirectional LLC converter (see Fig. 5.1). Contrary to common breakerless protection definitions, this work uses the oper-

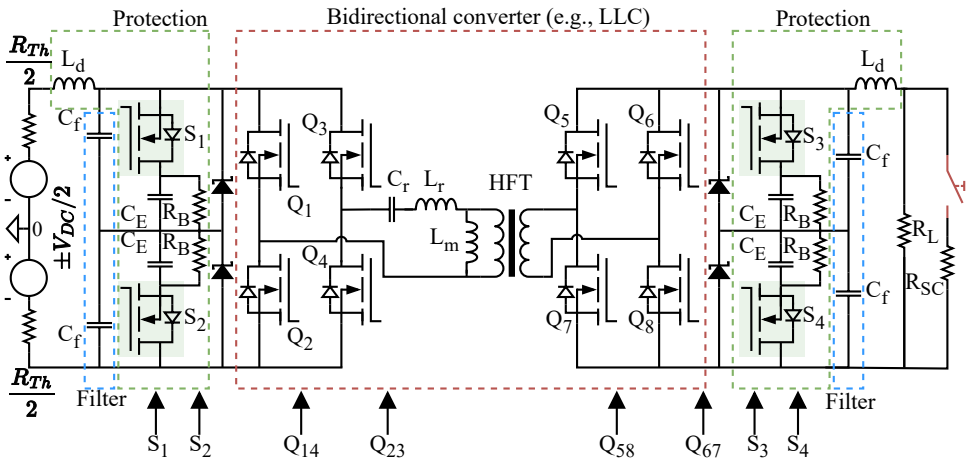


Figure 5.1: Schematic of the bidirectional DC-DC converter with the electronic capacitor-based protection module and the testing circuit. The LLC converter works as an example to illustrate the concept in this research. *Green shade:* Power switches for the protection module. R_{TH}: Thevenin equivalent resistor of the power supply, L_d: current dampening inductor, C_E: electronic capacitor, R_B: energy bleeding resistor, C_f: output filter capacitor, $Q_{1,2,3,4}$: transistors of the primary side, $Q_{5,6,7,8}$: transistors of the secondary side, R_L: Load resistance, R_{SC}: short circuit resistance.

ating principles of well-known unidirectional SSCBs. The main contribution of this chapter is the experimental validation of a compact, self-protecting power converter that inherits the advantages of modern SSCBs. The integrated protection module offers significant efficiency gains over conventional SSCB arrays and is adaptable to different converter topologies.

The core concept involves placing a power MOSFET in anti-series with the DC-link capacitor, connecting its source terminal to the positive node. This configuration allows permanent current flow through the switch through the anti-parallel diode and controlled conduction through the transistor, similar to the unidirectional SSCB behavior. In some applications, similar arrangements are referred to as *electronic* or *active capacitors*, generally used to enhance efficiency or bandwidth in power converters [184, 185]. However, their application for DC protection is limited in the literature.

Among the existing studies using *electronic capacitors* for DC protection, [186] proposes an anti-series IGBT with the DC-link capacitor to protect the DC side of various voltage-source converter (VSC) topologies. While the concept is insightful, there are limited details on timing and control and it does not include hardware implementation. Moreover, the simulated use case involves a large inductance that shapes the short-circuit dynamics, limiting its applicability to compact DC systems.

Similarly, the authors in [187] employ normally-ON SiC JFETs to realize a current-limiting function in the DC-link capacitor of a VSC. Their results show the potential of electronic capacitors as protection devices, with significant current attenuation in experiments. The JFET-based current limiter from [187] is further discussed in [188] for maritime applications, highlighting its potential for parallelization. However, key implementation aspects such as control design, timing coordination, and device lifetime remain unaddressed. Other approaches focus on using capacitor-based SSCBs to disconnect bus capacitors during faults [186]. While this effectively reduces capacitor discharge currents, the breaker processes a large fraction of the converter power, which increases conduction losses.

Unlike earlier works on electronic capacitors and breakerless protection, this study provides a fully integrated implementation that combines SSCB-inspired operation with converter-embedded protection. By inserting SiC MOSFETs in anti-series with the DC-link capacitor and integrating SSCB logic (detection, latching, and PWM interlock), the proposed module achieves:

1. Fast fault clearing (<300 ns breaking time)
2. Significantly reduced processed power (≈22% of SSCB losses)
3. Compatibility with fuse-based selectivity
4. Experimental validation on a 10 kW LLC prototype.

This combination of speed, efficiency, and experimental proof makes it the first practical converter-integrated protection solution for DC systems.

The authors of [189] propose a shoot-through protection device using an IGBT in series with a relay, placed between the two DC-link capacitors to protect a back-to-back JFET-based converter. Their scheme uses conventional desaturation circuit

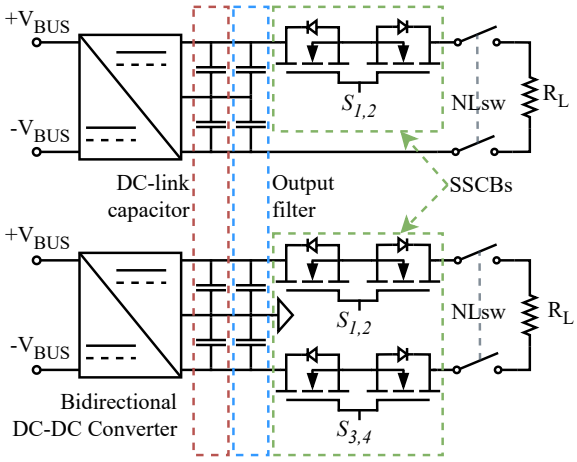


Figure 5.2: Simplified schematic of a generic bidirectional DC-DC converter protected with conventional bidirectional SSCBs, intended to be replaced by the proposed protection module. *Up:* unipolar system with floating ground. *Down:* bipolar system with midpoint ground.

to deactivate the IGBT upon fault detection. Once deactivated, a parallel charging resistor becomes the only path for fault current, allowing the converter to be protected while providing time to fold back. Experimental results report a clearance time of 1.2 µs, which may be adequate for the intended application. However, the work does not provide details on the control implementation, and a shoot-through can be less severe than a pole-to-pole short circuit, where precise timing is essential.

The previous literature review suggests a lack of research on a complete protection strategy based on the electronic capacitor. This chapter proposes a SiC MOSFET-based protection module that implements the electronic capacitor concept within a bidirectional DC-DC converter. While the electronic capacitor protection module can be adapted to various DC-DC or AC-DC converter topologies, its operation is demonstrated using a bidirectional LLC converter as shown in Fig. 5.1.

Furthermore, this research introduces a detection and protection control system, termed the *Surge dampening logical system* (SDLS), completing the protection architecture. The SDLS includes the gate driver and the necessary energy bleed branch to ensure safe operation. The proposed solution is validated through both simulation and experiments on a 10 kW bidirectional LLC converter. The protection module fits in the normal converter design procedure, where the output filter capacitors facilitate compatibility with fuses (see Fig. 5.1). Additionally, the electronic capacitor is compatible with both two-level and three-level LLC converter configurations.

The proposed protection module dissipates only about 22% of the power handled by a typical SSCB in unipolar systems with floating ground, as the one shown in Fig. 5.2. In bipolar DC systems with a midpoint ground (also shown in Fig. 5.2), this

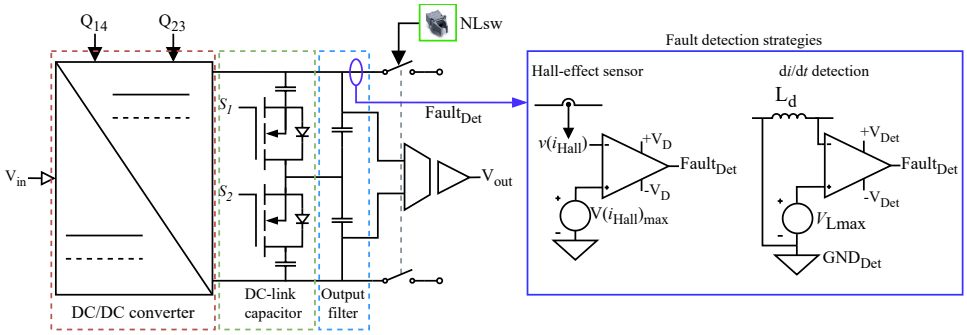


Figure 5.3: Simplified schematic of the electronic capacitor protection system as part of a generic power converter using several fault detection methods. *Dash-red:* generic DC/DC converter, *dash-green:* DC-link capacitor realized by an electronic capacitor, *dash-blue:* conventional output filter capacitor, *solid-dark blue*: fault detection sub-circuits.

processed power could be reduced further. For simplicity, this research focuses on the unipolar case, where the protection module allows for significant savings with a compact design for sensitive DC systems. In addition, the short-circuit breaking time is approximately 300 ns, comparable to high-speed SSCBs [90, 190].

The remainder of this chapter is organized as follows. Section 5.2 briefly introduces the conceptual solution with its complete architecture. Section 5.3 presents the simulations and experimental results and compares power losses. Finally, Section 5.4 presents the conclusions.

5.2. Protection module

This section introduces the proposed protection module, including its power switches, the essential auxiliary systems for its proper operation, the SDLS, and its compatibility with DC fuses. Figure 5.3 illustrates the concept of the electronic capacitor used as a protection element within a notional power converter. The schematic includes a generic converter, DC-link capacitors, output filter capacitors, a no-load switch (NLsw), and two detection methods compatible with the protection module.

1. **DC-DC converter:** a generic converter featuring an input voltage and four controllable power switches Q_1, Q_2, Q_3 and Q_4, grouped in pairs (Q_{14} and Q_{23}) to facilitate visualization.
2. **DC-Link capacitor:** the protection module including the electronic capacitor with two series power MOSFETs S_1 and S_2 placed in series with the DC-link capacitor.
3. **Output filter:** designed as part of the power converter to reduce voltage ripple.

4. **Fault detection strategies:** two fault detection strategies equipped with comparator detection flags.

As shown in Fig. 5.3, the output filter capacitors remain in the converter, allowing continuous dynamic operation with the protection module disabled or temporarily inactive. In addition, the compatibility with fuse selectivity, later explained in this section, depends on the energy stored in such capacitors.

5.2.1. Power switches

The power switches in the protection module must operate safely within their safe operating area during tripping, as in a conventional SSCB. A straightforward method to estimate initial ratings consists of analyzing the RMS current through the DC-link capacitor. For example, the secondary of the LLC converter in Fig. 5.1 has a full-bridge formed by Q_{58} and Q_{67} that delivers the current I_{SR} from the synchronous rectifier. Assuming that C_f is absent, the current through C_E (I_{CE}) is (5.1) and the corresponding RMS is (5.2).

$$I_{\mathrm{CE}} = I_{\mathrm{SR}} - I_{\mathrm{RL}}. \tag{5.1}$$

$$I_{\mathrm{CE,RMS}} = \sqrt{\frac{1}{T}\int_0^T \left(I_{\mathrm{SR}} - I_{\mathrm{RL}}\right)^2 \,\mathrm{d}t} \tag{5.2}$$

Here, I_{RL} represents the load current, showing that the RMS current through C_E decreases inversely with the I_{RL}, thus, the worst-case occurs at light load. For the LLC converter, I_{SR} is (5.3), applying first harmonic approximation gives $I_{\mathrm{SR,avg}} = {}^{2}/_{\pi} I_{\mathrm{peak}}$, under ideal operating conditions the average of $I_{\mathrm{CE}}(t)$ is zero, yielding (5.4).

$$I_{\mathrm{SR}}(t) = I_{\mathrm{peak}} \sin\left(2\pi f_{sw} t\right) \tag{5.3}$$

$$I_{\mathrm{CE,RMS}} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{\mathrm{RL}}\right)^2 - I_{\mathrm{RL}}^2} \tag{5.4}$$

Initially, (5.2) could be used to estimate the current through the switches S_3 and S_4, giving a starting point to select the appropriate power devices. The transistor selection guidelines available in [97, 183] offer useful criteria applicable to several converter topologies. When the power MOSFETs employed in the converter meet the required tripping characteristics, the design process is further simplified, as only one type of switch is required. Furthermore, the two-switch configuration shown in Fig. 5.3 supports compatibility with three-level topologies, enhancing the flexibility and scalability of the solution.

5.2.2. SDLS

This section presents the logical control system that governs the proper operation of the protection module. The system comprises a fault detection mechanism, a controller managing both the converter and the protection devices, a gate driver,

and an energy bleed branch to effectively protect against short circuits. Figure 5.4 illustrates the main functional blocks of the SDLS applied to a generic variable-frequency PWM DC-DC converter.

Detection

Short-circuit detection can be implemented using one or more methods, and the protection module should be compatible with most of them. Common techniques include shunt resistor, Hall-effect sensor, or measuring the voltage across a dampening inductor to capture $^{di}/_{dt}$. These signals can be conditioned to generate a fault flag using a rail-to-rail comparator. This concept is illustrated in Fig. 5.3 showing that some detection methods require signal isolation stages and floating reference points. Hall-effect sensors provide natural galvanic isolation and could be conditioned directly. In contrast, $^{di}/_{dt}$ measurements require a floating reference and an isolation stage, such as a digital isolator, to maintain low latency.

Control

The control architecture includes two parts. 1) The PWM for the converter and 2) the protection module.

- The converter controller implements a well-known foldback or a controlled shutdown mechanism interlinked with the protection module. The example in Fig. 5.4 features a changeover switch commanded by the protection control to force the PWM to the lowest available frequency. After a brief delay, the protection controller fully disables the PWM signals.
- The protection controller is based on conventional SSCB latched logic, allowing a simple design with low propagation delay and providing a signal interlock upon tripping of the protection module.

Gate driver

The protection module requires an isolated gate driver with dedicated source pins and allows simultaneous activation of the high- and low-side transistors. A component featuring desaturation protection, low propagation delay and high-impedance gate protection is preferred.

Energy bleed

A bleeding branch parallel to the DC-link capacitor is necessary to fully discharge it after protection activation. A resistor branch R_B can be used to reduce complexity, but this incurs continuous power losses (see Fig. 5.4). Alternatively, an active bleeding branch using a power transistor eliminates steady-state losses but requires additional components for operation [191, 192].

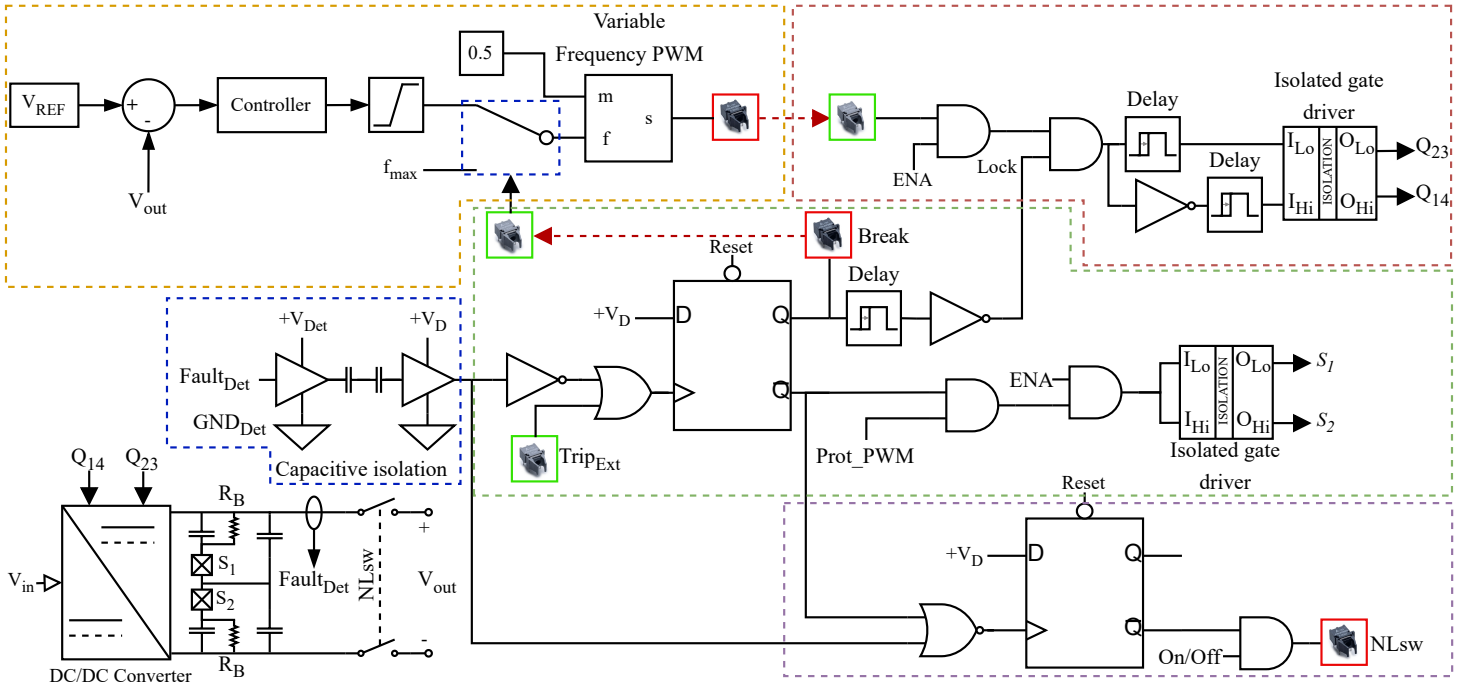


Figure 5.4: Blocks diagram of the surge-dampening logical system designed for the electronic capacitor protection for a generic DC/DC converter. *Dash-yellow:* conventional closed-loop control with variable frequency PWM and minimum frequency changeover switch, *dash-red:* hardware implementation of PWM signals for the converter including isolation stages and lock-down/enable signals, *dash-green:* hardware implementation of breaking logic including isolation stages for the protection switches S_1 and S_2, *dash-purple:* hardware implementation of the No-Load switch control signal, *dash-blue:* capacitive isolation stage for the fault detection signal.

5.2.3. Fuse compatibility

To enhance selectivity, the energy stored in the output filter capacitors can be utilized to blow downstream fuses when required. The pre-arcing specific energy of a fuse is obtained by (5.5), and it is essential for fuse calculation and selection.

$$\frac{\mathrm{W}}{\mathrm{R}} = \int_{t_1}^{t_2} i^2(t)\,\mathrm{d}t \tag{5.5}$$

In general, fuses are designed after the drive, but conceptually the filter capacitor should follow (5.6).

$$E_{\mathrm{cap}} > E_{\mathrm{fuse}} + E_{\mathrm{ESR}} \tag{5.6}$$

Here, E_{cap} is the energy stored in the capacitor, E_{fuse} is the maximum energy absorbed by the fuse according to its specific energy, and E_{ESR} is the energy absorbed by the series equivalent resistor in the capacitor itself.

5

5.3. Validation

Two validation stages are conducted to demonstrate the operation of the protection module: the simulation; and the experimental implementation. This section covers both the simulation and experimental testing of an LLC converter equipped with the electronic capacitor and the SDLS. Additionally, a power loss analysis compares the proposed solution with a conventional SSCB in series with the same LLC converter (see Fig. 5.2).

5.3.1. Simulation

A PLECS model of the circuit in Fig. 5.1 was developed to evaluate the protection module in Fig. 5.3, incorporating the SDLS shown in Fig. 5.4. Circuit parameters are listed in Table 5.1. The LLC converter design procedure is detailed in [193], and the detection inductance calculation in [89].

Table 5.1: LLC converter prototype parameters.

Parameter	Value	Subsystem
Nominal voltage V_{nom}	600 V	Power supply
Nominal current I_{nom}	16.6 A	Power supply
Nominal power	10 kW	Bidirectional LLC
Input capacitance $C_{E,in}$	20 µF	Input protection module
Input capacitor ESR	6.5 mΩ	Input protection module
Input detection inductor $L_{d,in}$	220 nH	Input protection module
Resonant frequency f_r	32 kHz	Bidirectional LLC
Resonant capacitor C_r	114.05 nF	Bidirectional LLC

Continue on next page ...

Parameter	Value	Subsystem
Resonant inductor L_r	213.5 µH	Bidirectional LLC
Magnetizing inductor L_m	2.3 mH	Bidirectional LLC
SiC FET Output Capacitance C_{oss}	66 pF	Bidirectional LLC
Output Filter Capacitance C_f	5 µF	Bidirectional LLC
Output capacitance $C_{E,out}$	40 µF	Output protection module
Output capacitor ESR	5.2 mΩ	Output protection module
Output detection inductor $L_{d,out}$	220 nH	Output protection module
Load resistance R_L	33.3 Ω	Load

Figures 5.5 and 5.6 show the converter operating in steady-state, following a voltage setpoint on the secondary side. At time t_{SC}, the short-circuit interrupter is triggered, creating a pole-to-pole short-circuit because R_{SC} (see Fig. 5.1) is in the milliohm range. After the fault occurs, the detection system sends a latched protection command following a delay t_D. At breaking time t_B, switches S_3 and S_4 are turned off, as the fault is on the secondary side. The short circuit current then decreases to zero by t_C, at which point the fault is cleared and the NLsw is opened. Note that the energy stored in the resonant tank of the LLC converter can still flow through the output capacitor through the anti-parallel diode of the protection module and also to the output terminals.

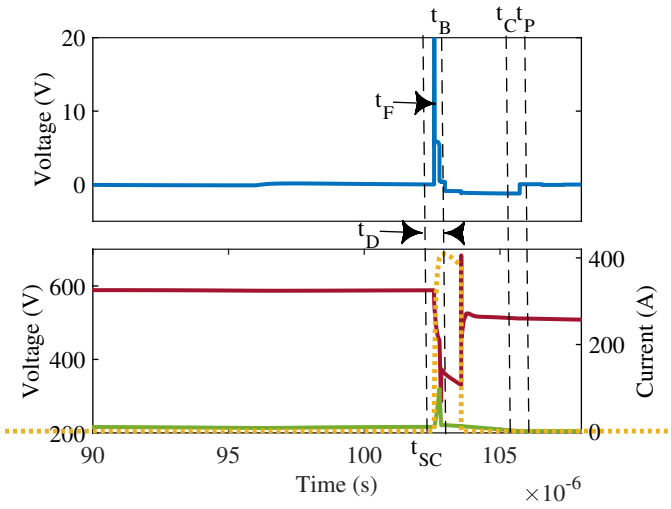


Figure 5.5: Simulation of the LLC converter equipped with the electronic capacitor as a protection module under a pole-to-pole short circuit. $L_d di/dt$ detection signal (blue), converter output voltage (dark red) and current (green), short circuit current (dotted yellow).

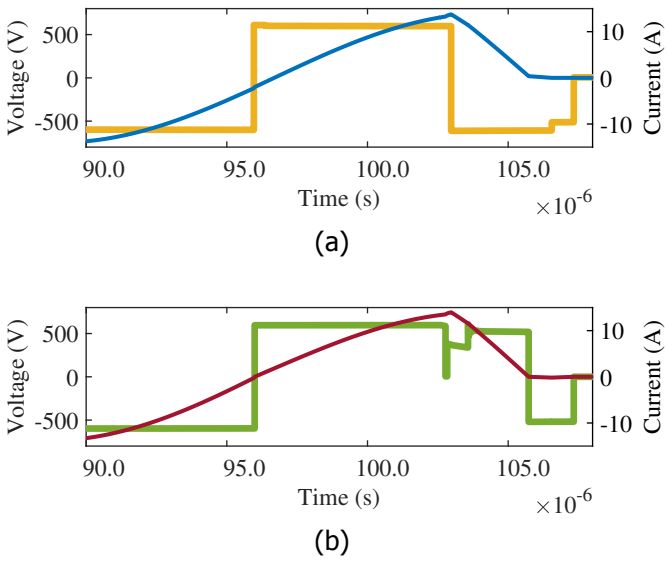


Figure 5.6: Simulation of the LLC converter equipped with the electronic capacitor as a protection module under a pole-to-pole short circuit. (a) Voltage (yellow) and current (blue) in the primary. (b) Voltage (green) and current (dark red) in the secondary.

In the SDLS protection sequence, the fault is detected at t_F, prompting the changeover switch to set the PWM generator to its maximum frequency. After an additional delay t_P, all PWM signals are disabled, locking the converter in fault mode. The short circuit current in Fig. 5.5 (in yellow) is interrupted is interrupted in the short circuit branch after after 1 µs to protect the semiconductors used to create the short during experimental testing. The current contribution of the protection module (in green) is relatively small compared to that of the output filter (in yellow). The peak current from the protection module reaches approximately 97.5 A, while the output filter current is about 408.8 A. Without the protection module, the peak current from the converter would be near 402 A for about 2.7 µs, which could cause severe damage or total converter failure.

Applying (5.5) to the short-circuit current yields the pre-arcing specific energy of approximately $0.15\,A^2\,s^{-1}$, which can be compared with a reference fuse, such as Mersen A050URD1.2T13I, used in semiconductor protection, which indicates $0.13\,A^2\,s^{-1}$ [194]. This suggests that the proposed system could be compatible with a selection of low current fuses, chosen for selectivity purposes.

Because the protection concept allows sudden discharge of the output filter capacitor, component wear must be considered. Film capacitors are preferred over electrolytic types due to their higher short-circuit tolerance [195]. Fuse ratings should be chosen in relation to capacitor size to ensure effective protection and reduce stress. Monitoring ESR allows estimation of capacitor health after several

short circuit events.

5.3.2. Experimental setup

The proof-of-concept of the electronic capacitor-based protection module is validated using a 10 kW bidirectional LLC converter prototype, as depicted in Fig. 5.1. The prototype is shown in Fig. 5.7, where the main components correspond to: *Green:* protection module. *Blue:* output filter capacitor. *Red:* bidirectional LLC converter. The converter is controlled via an RT-Box with optical fiber connections, ensuring operation during testing without compromising performance. Table 5.2 lists the main components and test equipment. The load is constant using power resistors, while the short circuit is implemented with paralleled SiC MOSFETs.

The test conditions replicate the simulation scenario. A pole-to-pole short circuit is applied to the secondary side during steady-state operation under a 5.5 kW load. Figure 5.8 shows the short circuit current in yellow, the converter current in green, the secondary output voltage in magenta, and the $L_d {}^{di}/_{dt}$ in blue.

Table 5.2: Components and equipment to validate the LLC with the protection module.

Component	Reference
Power stage	
SiC MOSFET	Wolfspeed C3M0065090D
Capacitor	EPCOS B32776G4406K000
Power supply	ITECH IT6018C-1500-30
Short cirtcuit stage	
SiC MOSFET	Wolfspeed C2M0080120D
Capacitor	EPCOS B32774D8505K000
Sensors and control	
Hall-effect sensor	AKM CZ375DCB-HA
High-speed AND gate	TI SN74LVC1G11-Q1
Measurement	
Current probe	Micsig CP1003B,CWT UM/03/R
Differential probe	Micsig DP700
Scope	Keysight DSOX3024A

Similar to simulation results, the measured short-circuit current peaks at 414.3 A, while the converter current reaches 40.7 A, confirming correct operation of the electronic capacitor. Using (5.5), the calculated specific energy is sufficient to trigger the reference Mersen A050URD1.2T13I fuse. The fault clearance time is approximately 2 µs, while the breaking time is closer to 200 ns when using ${}^{di}/_{dt}$ detection. Despite the relatively long clearance time compared to the breaking time, the contribution of the converter to the fault is limited, as the current ripple, after the first overshoot, remains below 20 A, showing potential to fit within existing selectivity schemes in DC systems.

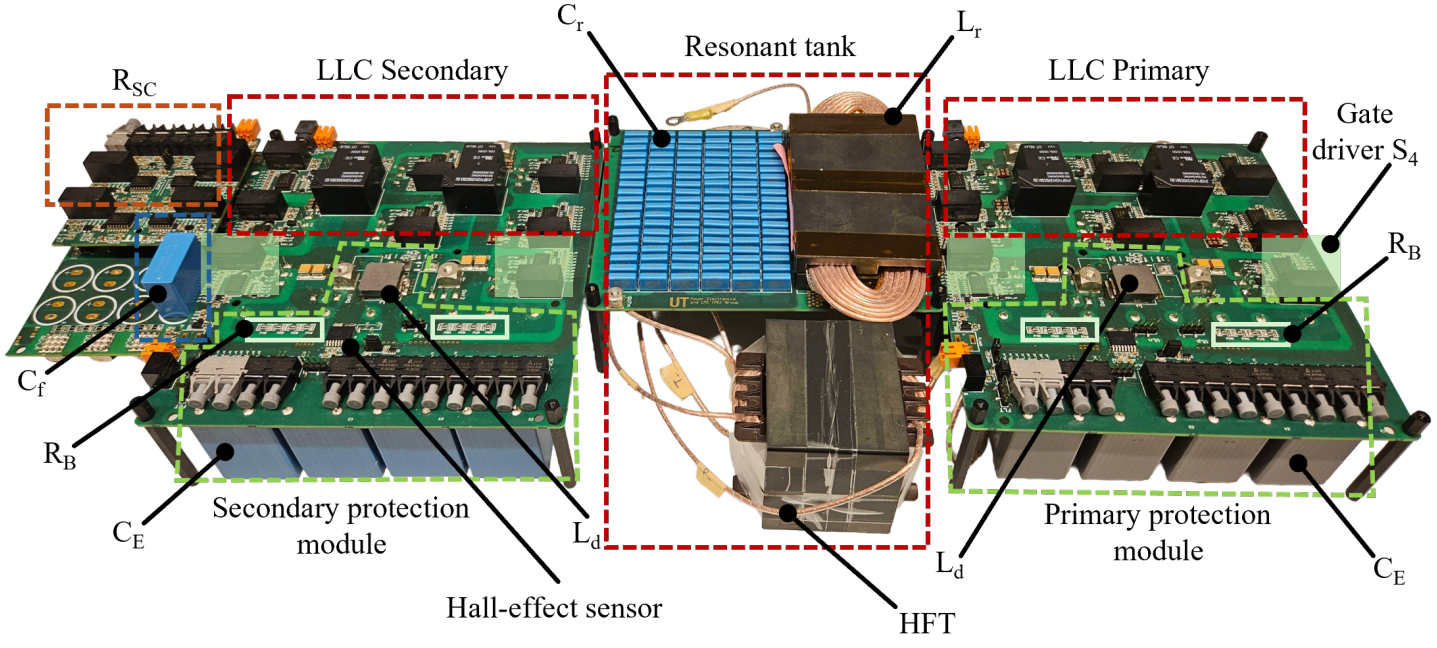
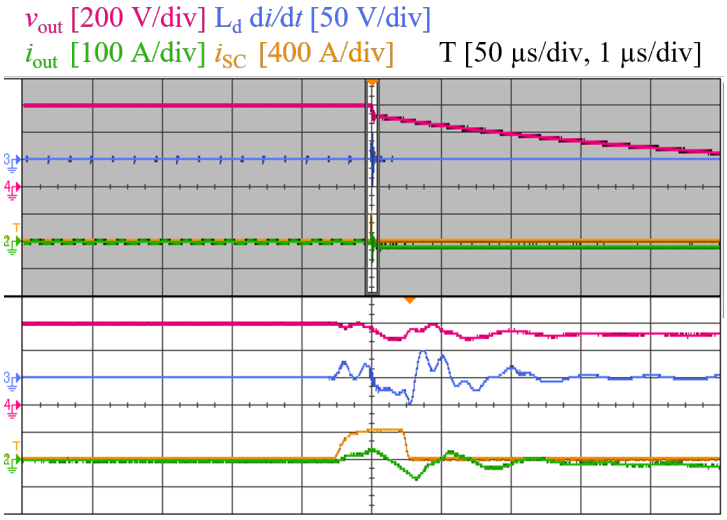
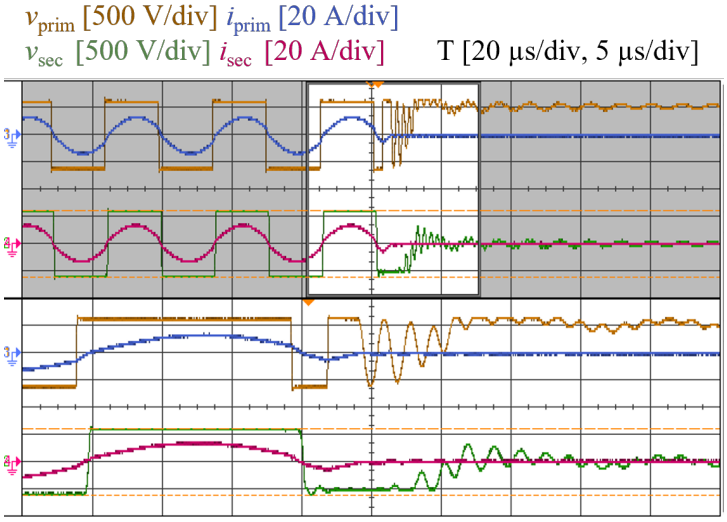


Figure 5.7: 10 kW prototype of a bidirectional LLC converter equipped with the protection module. *Green shade:* Gate driver of the power switches for the protection module. L_d: current dampening and detection inductor, C_E: electronic capacitor, R_B: energy bleeding resistor, C_f: output filter capacitor R_{SC}: short circuit branch.



(a)



(b)

Figure 5.8: Experimental results of the LLC converter equipped with the electronic capacitor as a protection module. (a) Short circuit test highlighting the effect of the protective action and the contribution of the protection module to the short circuit current. (b) Measurement of the primary and secondary voltages and currents of the LLC converter during a pole-to-pole short circuit.

Figure 5.8b presents the LLC converter behavior during the short circuit event. The converter is soft-switching at resonance frequency when the short-circuit is introduced. Proper PWM deactivation is observed as the primary and secondary voltages in yellow and green, respectively, stop switching upon enable signal deactivation. Primary and secondary currents, in blue and magenta, respectively, decay rapidly due to the low stored energy in the resonant tank. This observation provides context for the overall fault-clearing process and its influence on the converter operation.

The slightly longer fault-clearing time observed in experiments compared to simulation is mainly due to propagation delays in the detection and gate-driving circuits, as well as parasitic elements in the prototype. These aspects can be reduced in optimized hardware, suggesting that the practical clearing time could approach the simulated value.

Although the short circuit is not completely interrupted initially, the self-protected converter brings the fault current to zero and latches itself from the rest of the system without overshoot. This performance is enabled by additional protection features, including PWM inhibition (enable) and desaturation in the gate driver.

The proof-of-concept experiments confirm the correct operation of the protection module and SDLS, demonstrating a compact and fuse-compatible protection strategy. Future work will address efficiency trade-offs, protection module reliability under repeated short-circuit events, compatibility with higher current fuses, and selectivity adjustments for integration into larger DC systems.

Although the validation has been carried out on an LLC converter, the protection concept is generic and can be extended to other DC-DC or AC-DC converter topologies with minor adaptations, which will be explored in future work.

5.3.3. Power losses

Since the protection module shows effective protection performance, it is important to quantify the conduction losses generated during steady-state operation at nominal power. Such losses are compared with those of the reference system in Fig. 5.2, where a bidirectional SSCB is placed in series with the positive pole of the converter. This comparison leverages the simulation model discussed previously by implementing the thermal model of the switches provided by the manufacturer. In this section, two simulation types are necessary: 1) analyzing the losses due to the electronic capacitor; and 2) studying the power dissipated by the SSCB. To provide a more comprehensive analysis, an additional set of simulations is included to account for the LLC using the electronic capacitor as the only output filter (removing C_f). The model simulates the LLC converter at nominal load, constant ambient temperature of 25 °C, and stabilized junction temperature of the power switches under study. The simulations use the same SiC MOSFET, Wolfspeed C3M0065090D for both cases, and the parameters obtained for power dissipation are summarized in Table 5.3.

From the comparison, it is noticeable that the conduction losses using electronic capacitor protection are, on average, 85.3% lower than those of the SSCB for the

Table 5.3: Conduction losses comparison between conventional SSCB and electronic capacitor protection.

Parameter	Electronic capacitor	SSCB
LLC with C_f		
Junction temperature	29.8 °C	49.28 °C
Conduction losses	4.98 W	33.9 W
LLC without C_f		
Junction temperature	31.2 °C	49.8 °C
Conduction losses	7.62 W	33.88 W

case with the output capacitor C_f. In contrast, the converter without C_f dissipates about 22.49% of the conduction losses of the SSCB. The arrangement of the protection module results in approximately 4.98 W and 7.62 W of losses including and excluding C_f respectively, whereas the SSCB shows around 33.88 W, as it processes the full power transferred to the load.

Although further measurements are necessary to validate the efficiency gain when electronic capacitor protection is used, the simulation model provides a good approximation of the real case. This potential efficiency gain could motivate the further development of embedded power electronics-based protection solutions in multiple DC grid applications.

5.4. Conclusion

This chapter presented a DC-DC converter with integrated protection based on the electronic capacitor concept combined with solid-state circuit breaker technology. In this configuration, the protection module is connected in series with the DC-link capacitor rather than the converter output. This arrangement reduces the current handled by the protection module compared to a conventional SSCB connected in series with the converter. The proof-of-concept aims to simplify DC protection by enabling converters to withstand severe pole-to-pole short circuits without external devices. The approach was validated through simulation and experimental testing on a bidirectional LLC converter equipped with the proposed protection module. While further investigation is needed, the results indicate that the concept can support wider adoption of DC power systems.

While only a limited number of short-circuit events were tested in this prototype, repeated-event robustness and device lifetime under thermal cycling are important considerations. These aspects will be part of future reliability studies.

By inserting power MOSFETs in series with the DC-link capacitor, the module effectively attenuates fault current surges. Integrating solid-state circuit breaker functions, such as control and fault detection, enhances protection capability, while maintaining compatibility with existing fuse-based selectivity strategies in microgrids.

The design can be extended to other converter topologies, including three-level architectures, with minimal modification. Retaining the output filter capacitor ensures sufficient stored energy to operate properly rated fuses with a limited efficiency penalty. The protection functionalities are comparable to those of stand-alone solid-state circuit breakers, yet generate only a fraction of the conduction losses.

In addition to demonstrating fast interruption times (approx. 200 ns breaking time) and fuse coordination potential, the proposed solution highlights a pathway to compact, efficient, and converter-integrated protection. This approach reduces system-level complexity, supports modularity, and could enable new standards for DC microgrids and high-reliability applications such as maritime, aerospace, and data-center power systems.

Future work will extend the study to larger fault currents, integration with higher-rating fuses, and comprehensive efficiency measurements, while also exploring long-term reliability under repeated faults. A broader investigation of interoperability with existing DC protection frameworks is also required.

Overall, the proposed module offers a compact, adaptable, and fuse-compatible protection solution that provides significant gains in protection capability with only modest changes to the converter design.

6

Conclusion

Photo by Vivek Kumar on Unsplash

Humpback whales hunt not as solitary giants but as a community, circling their prey in spirals of bubbles that no single whale could create alone. In this shared effort, each whale finds its place in the whole, and together they secure the food that sustains them all.

The widespread adoption of shipboard DC systems is a work in progress. As DC technologies mature and are deployed across more vessels and vessel types, new challenges inevitably emerge. To the best knowledge of the author of this thesis, there is no way around the paradigm: *"more unit types = more problems."* Therefore, research and development play a key role in anticipating these issues and identifying practical solutions.

This work emerged as an opportunity to develop the knowledge about shipboard DC systems and propose a solution to some of the urgent challenges. However, transport electrification has a diversity of topics requiring attention among which protection technology appeared too essential to overlook. This means that other applications face similar obstacles when implementing DC systems, and adapting technology from those fields could not suffice.

Therefore, the work supporting this thesis was shaped by understanding the particularities of shipboard DC systems and why and how short circuits can be hazardous. However, the research conducted resulted in two nonconventional protection solutions, agnostic to the application and valuable in different fields, inspired by two in-depth studies on primary shipboard DC systems and their protection schemes.

The research presented in this thesis could be analyzed as one of the opening chapters in the revolution of DC protection. This means that most of the development remains as future work, as promising technologies require full-scale demonstrators. This thesis also aims to suggest a positive prospect for future DC systems in transport electrification in general, and multiple alternative research paths are to be discovered.

This conclusion chapter reflects on how the research objective have been met by answering the research questions in Chapter 1 and provides recommendations for future research based on actual findings. Moreover, Chapter 2 serves as the platform that motivates the entire work, as it not only frames the theoretical and conceptual foundations but informs and justifies the research questions introduced in Chapter 1.

6.1. Objective

To *enhance protection effectiveness of shipboard DC systems by improving the capabilities of circuit breakers and DC-DC converters:*

This general objective has been fulfilled by completing several chapters. Effectively, four concepts are enhancements of shipboard DC protection effectiveness, explored in Chapters 3 to 5.

1. Short circuit characterization in DC systems (Chapter 3).
2. High-speed solid-state circuit breakers (Chapter 4).
3. Solid-state circuit breakers with latching current limiting (Chapter 4).
4. DC-DC converters with electronic capacitor protection (Chapter 5).

The understanding of potential short circuits in shipboard DC systems is essential for properly designing protection devices, such as SSCBs, LCLs and Electronic Capacitors. Analyzing the system architecture, fault location, and existing protection technologies allows for an informed design that accounts for potential threats and their consequences for the system and the protection devices.

The protection effectiveness of solid-state circuit breakers has been improved by developing a high-speed prototype that can detect short circuits with low propagation delay and quickly clear the fault. Furthermore, the gate driver of the circuit breaker was modified to enable current-limiting capability, so that the circuit breaker only trips when it is really necessary, improving power availability in the system. In addition, the enhanced solid-state circuit breaker was designed based on short circuit propagation studies for the primary DC system of a superyacht, tailoring the design to its specific needs.

In addition, a protection module for DC-DC converters based on the electronic capacitor concept has been proposed to enhance the self-protection capabilities of power converters. The concepts of electronic capacitors and solid-state circuit breaker merge to create a protection module capable of protecting the power converter from aggressive short circuits while maintaining compatibility with fuses, which remains fundamental in mainstream DC protection on ships. The module is compatible with multiple power converter topologies and was demonstrated in a bidirectional LLC prototype, and it is expected to increase the volumetric power density of shipboard DC systems.

6.1.1. Research questions

Logically, completing the main objective of this thesis involves answering research questions. The answer of each question is presented in this section.

RQ1: *What are the characteristics of short circuits in shipboard DC systems?* Chapter 3 shows that the primary DC system of a superyacht can behave similarly an impulse current generator, as used in lightning protection. Depending on the protection strategy, mostly still based on fuses, a distributed double bus primary DC system can suffer from feeder, bus, or even total system failures following a fault.

Pole-to-pole short circuits are identified as the most aggressive fault type in the study and can be categorized by their potential severity, which is related to their physical location. Short circuits occurring near the output filter of a converter can generate large current overshoots, reaching hundreds of kiloamperes, posing significant thermal stress on capacitors. In contrast, short circuits at the bus bars show lower current peaks, dampened by cable inductance, but result in a rapid discharge of energy from all DC-link capacitors, stressing other system components significantly.

RQ2: *How can the protection functionalities of existing solid-state circuit breaker technologies be enhanced for maritime applications?*
Chapter 4 has been dedicated to demonstrate the unexploited potential of existing

solid-state circuit breakers in shipboard DC system protection and how they can be enhanced with limited added complexity. The use of bidirectional solid-state circuit breakers on the positive pole, complemented by a no-load switch, is convenient for modern DC ships, since most state-of-the-art primary DC ships operate with floating grounding. This configuration supports both bidirectional power flow and protection, placing two semiconductors in anti-series.

When implemented with SiC MOSFETs, the solid-state circuit breaker can be enhanced by modifying the gate driver to deliberately operate the devices in their linear region. This controlled dissipation of energy can limit transient overcurrents, avoiding unnecessary tripping. By integrating a high-speed controller with a custom three-level gate driver, a latching current limiter, commonly used in space applications, can be embedded within a conventional solid-state circuit breaker. This combined approach confirms that solid-state circuit breakers can provide advanced, multi-functional protection beyond simply replacing traditional AC breakers. The resulting solid-state circuit breaker offers better fault selectivity than conventional designs by reducing the isolation of feeders affected by transient overloads. This feature can be attractive for sensitive applications, potentially reducing the complexity of protection schemes on future DC systems.

RQ3: *How can the protection capabilities of power converters in a shipboard DC grid be enhanced using power electronics-based protection technology?*
Chapter 5 redefines power electronics-based protection by presenting a self-protective DC-DC converter with embedded protection features. This converter can protect itself and parts of the system against short circuits, integrating protection directly into the converter.

A protection module demonstrated in an LLC converter prototype incorporates solid-state circuit breaker functions within an electronic capacitor. By placing power MOSFETs in the DC-link capacitor path, it achieves unidirectional protection and bidirectional power flow, with some added losses in the capacitor pack. However, short circuit detection and latched control of solid-state circuit breakers prevent significant thermal stress in the DC-link capacitor when a short circuit occurs.

This integrated protection-converter approach is especially attractive for applications with strict volumetric power density constraints. It offers higher efficiency than traditional converters paired with external circuit breakers, as the protection module only handles a fraction of the output power across the complete range of operation. For maritime systems, this could enable more compact, less complex designs with faster time-to-market if proven feasible.

6.2. Recommendations

The following recommendations can be used for future research.

- The short circuit categorization in Chapter 3 should be studied with different primary system architectures to validate its applicability as system complexity increases.

- The solid-state circuit breaker with latching current limiter in Chapter 4 requires further development to increase its nominal current capacity to better match real-world applications.
- Additional studies are needed to analyze the aging process of SiC MOSFETs due to the increased losses during the latching current limiter operation described in Chapter 4.
- The aging analysis of power semiconductors in the electronic capacitor, presented in Chapter 5, requires extensive testing to demonstrate reliability.
- The protection module in Chapter 5 was designed to be compatible with three-level converters; such validation is necessary.
- Further simulations and testing of the prototypes in Chapters 4 and 5 are required to evaluate their performance within larger protection schemes.
- Replacing the analog controllers in the prototypes of Chapters 4 and 5 with FPGAs could simplify hardware implementation, but protection performance parameters must be thoroughly assessed.
- The concept proposed in Chapter 5 could be integrated into the power electronics building block framework discussed in Chapter 2, enabling power scalability with embedded protection.

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Nomenclature

ΔT_{vj}	Virtual junction temperature rise
$Z_{\mathrm{th(j-c)}}$	Junction-case thermal impedance
E_{d}	Dissipated energy
I_{D}	Drain current
i_{hall}	Hall-effect sensor current
I_{max}	Maximum design short circuit current
I_{nom}	Nominal design current
I_{OFF}	Gate driver sink current
I_{ON}	Gate driver source current
i_{SC}	Short circuit current
t_{LCL}	Latching current limiter time
t_{max}	Maximum design clearance time
$V\mathrm{g}$	Generator voltage
V_{DS}	Drain-source voltage
V_{GDF}	Forward voltage of gate driver diodes
v_{GS}	Gate-source voltage
$V_{\mathrm{L,max}}$	Maximum inductance detection voltage
V_{latch}	Latching current limiter reference voltage
V_{max}	Maximum design voltage
V_{nom}	Nominal design voltage
V_{overload}	Overload reference voltage
V_{th}	Threshold voltage
APU	Auxiliary power unit
BTS	Bus-tie switch
C_{d}	Dampening capacitor
C_{gs}	Gate-source parasitic capacitance
C_{out}	Output capacitor
COTS	Commercial off-the-shelf
CRU	Full-speed cruising
DAB	Dual-active bridge converter
DP	Dynamic positioning
ECO	Economic cruising
ECSS	European Cooperation for Space Standardization
EMI	Electromagnetic interference
EP	Electrical propulsion
ESR	Equivalent series resistor
ESR	Equivalent series resistor
ESS	Energy storage system
FET	Field-effect transistor
HB_{CB}	Half-bridge circuit breaker
HB_{LCL}	Half-bridge latching current limiter
HCB	Hybrid circuit breaker

HP	Hybrid propulsion
ICE	Internal combustion engine
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
JFET	Junction-gate field-effect transistor
L_d	Dampening inductor
L_p	Parasitic inductance
LCL	Latching current limiter
LVDC	Low voltage direct current
MCB	Mechanical circuit breaker
MMC	Modular multi-level converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOV	Metal-oxide varistor
MOV	Metal-oxide varistor
MP	Mechanical propulsion
MVDC	Medium voltage direct current
NL_{SW}	No-load switch
Q_{gs}	Gate-source charge
R_{DSON}	Equivalent channel on-resistance
R_d	Dampening resistance
$R_{G_{FET}}$	Gate resistance of a power switch
R_{HiZ}	High impedance resistance
R_{OFF}	Gate driver turn off resistance
R_{OH}	Gate driver pull-up resistance in source mode
R_{OL}	Gate driver pull-down resistance in sink mode
R_{ON}	Gate driver turn on resistance
R_{SC}	Short circuit resistor
R_{th}	Thevenin resistor
SDLS	Surge dampening logical system
SiC	Silicon carbide
SSCB	Solid-state circuit breaker
TRL	Technology readiness level
VSC	Voltage-source converter

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J.A. Latorre Correa
Delft, December 2025

Curriculum Vitæ

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List of Publications

7. A. Latorre, A. K. Iyer, T. B. Soeiro, R. Geertsma and H. Polinder. 'Electronic Capacitor-Based Protection for Converter-Interfaced DC Microgrids (under review)'. In: *IEEE Trans. Ind. Electron.* (2026)

6. A. Latorre, T. B. Soeiro, A. K. Iyer, R. Geertsma and H. Polinder. 'High-speed Solid-State Circuit Breaker with Latching Current Limiter for DC Systems (accepted)'. In: *IEEE Open Journal of Power Electronics* (Aug. 2026), pp. 1–14. doi: 10.1109/OJPEL.2025.3625092

5. A. Latorre, T. B. Soeiro, X. Fan, R. Geertsma, M. Popov and H. Polinder. 'Pole-to-Pole Short-Circuit Categorization for Protection Strategies in Primary Shipboard DC Systems'. In: *Open journal of the Industrial Electronics Society* 5 (June 2024), pp. 596–615. doi: 10.1109/OJIES.2024.3417939

4. A. Latorre, T. B. Soeiro, R. Geertsma, A. Coraddu and H. Polinder. 'Shipboard DC systems, a Critical Overview: Challenges in Primary Distribution, Power Electronics-based Protection, and Power Scalability'. In: *Open journal of the Industrial Electronics Society* 4 (July 2023), pp. 259–286. doi: 10.1109/OJIES.2023.3294999

3. A. Latorre, T. B. Soeiro, R. Geertsma and H. Polinder. 'Three-level Gate Driver for Latching Current Limiter in DC Microgrid Protection'. In: *2025 IEEE 7th International Conference on DC Microgrids (ICDCM)*. IEEE, June 2025, pp. 1–5. doi: 10.1109/ICDCM63994.2025.11144676

2. A. Latorre, T. B. Soeiro, R. Geertsma and H. Polinder. 'Gate Driver Design for Solid-State Circuit Breaker with Integrated Latch Current Limiter in Shipboard DC Systems'. In: *2024 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*. IEEE, Nov. 2024, pp. 1–6. doi: 10.1109/ESARS-ITEC60450.2024.10819826

1. T. Kopka, A. Latorre, A. Coraddu and H. Polinder. 'Energy-Based Voltage Stabilization in DC Shipboard Power Systems with Dual Loop Control'. In: *IEEE Access* 13 (July 2025), pp. 117105–117118. doi: 10.1109/ACCESS.2025.3586382