Signal Up-conversion for Integrated Radar Systems

By

Lai Jiang

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Supervisors: Dr. Ing. L.C.N. de Vreede, TU Delft

Prof. Dr. John R. Long, TU Delft

Dr. Cicero S. Vaucher, NXP

Abstract

Frequency up-conversion is an integral part of the (sub)mm wave integrated radar system that is currently developed at the TUDelft in the context of the MEMPIS program. The proposed up-converter IC allows the necessary signal modulation for the radar to be generated at a relative low frequency, afterwards up-conversion to W-band takes place. In our case, the FMCW (frequency modulated continuous wave) principle is used for the actual radar operation. This up-conversion, based on analogue signal multiplication, reduces the source signal bandwidth requirement by the amount of its multiplication factor.

The purpose of this work is to explore the possibility of implementing a wideband high-order frequency up-converter which suits the needs of our radar system, including high conversion gain, spur suppression, improved noise performance, as well as limited DC power consumption.

In our system, the up-converter converts an input signal from X and Ku-band (around 10GHz) to W-band (around 94GHz). The up-converted signal is used to drive both the transmitter antenna and the receiver mixer LO port. The whole circuit includes a multiply by 8 chain and necessary gain blocks on W-band.

Study of the frequency multiplication process has resulted in a carefully planned frequency allocation, as well as, power leveling for each sub-circuit. A wideband frequency doubler capable of high conversion gain and low unwanted spur generation is designed. In the multiply by 8 chain, optimum operation of the frequency doubler together with on chip filtering are performed to guarantee the spectrum purity of the output signal over wide bandwidth. Two W-band medium power amplifiers are optimized for flat gain frequency response. The multiply by 8 chain provides an output signal from 80GHz to 112GHz, with an in-band conversion gain ranging from 13.2 dB to 16.6dB. The suppression of unwanted spurs is better than 40dB. The antenna driver amplifier delivers more than 3dBm output power with about 3dB in-band gain variation. The LO driver amplifier delivers more than 150mV peak voltage swing at mixer LO port with less than 2dB in-band gain variation.

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Chapter 1 Introduction

Over the past few decades, we have experienced an explosive development of the IC industry. Both functionality and performance of solid state circuit are advancing constantly. As a result, more and more applications have been made possible. The advance of integrated circuit has been the driving force to the development in many other realms. Huge amounts of information are handled, distributed, stored or exchanged around the globe every second. The communication capacity is enhanced so much, that wireless video application or other high quality instant services can be supported. The accuracy of sensor systems is improved to catch the exact details of nature. Looking back to the prophecy by G. Moore in 1965 [1], almost all expectations have been reality now. The stemming applications in turn put forward new demands on IC performance and push it toward further development. One of such examples concerns the applications at very high frequencies, including high capacity wireless communication and compact radar system.

This thesis presents the design of a frequency up-conversion chain that features wideband operation from Ku band to W band. It is part of the Memphis project A8 which focuses on (sub)mm-Wave Radar System Design. Applications of this radar system include bad-weather vision system, logistic inspection and medical usages. Both FMCW (frequency modulated continuous wave) principle and integrated phased array are employed to endow the radar system more capability and better flexibility. This design is carried out with IBM 8hp BiCMOS process.

1.1 Background Information

1.1.1 Radar Technology

Radar is an electromagnetic system for the detection and location of reflection objects [2]. By comparing the reflected signal with the transmitted signal, information concerning the object can be obtained, such as its presence, distance to radar and even moving speed and direction. Often, single antenna is used for both transmitting and receiving in a time division way. Pulsed waveform is adopted to focus energy in time domain and to determine the target distance. The pulse duration determines maximum unambiguous range between two objects. To steer the beam direction, mechanical means is required to point the antenna to different directions. Fig 1.1 shows the basic principle of radar.

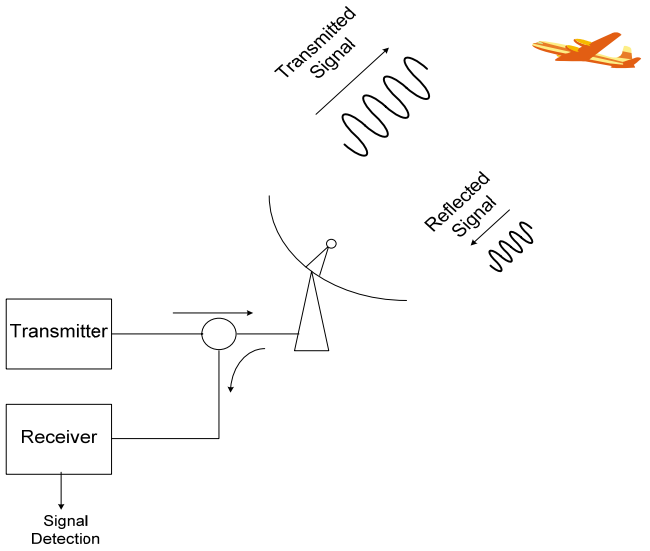

Fig 1.1 Basic principle of radar

1.1.2 Phased Array System

Phased array systems can imitate the beam of a directional antenna in a way that the beam can be controlled electrically [3]. This property takes the place of mechanical orientation of antenna reflector, which makes the radar system much more compact. Besides, the distributed nature of signal handling elements improves the robustness of the system against the failure of a single element. Distribution also means that the requirement on each active device in terms of power handling and noise is relieved. Coherent signal detection can be applied taking advantage of the difference between signal and interference or noise, resulting in better sensitivity and directivity.

The advancement of MMIC technology makes it possible to integrate more and more essential parts of the phased array system into the same package or chip. Various designs have already been put forward during the past decade [4], [5], [6]. These integration efforts further reduce the cost and size while improving the reliability and providing the system with new possibility of on-chip signal processing.

1.1.3 FMCW Radar Techniques

FMCW radar is a technique for obtaining range information of the target by frequency modulating a continuous wave signal [7]. Unlike time division radar operation, CW radar receives while transmitting. The advantage stems from several related aspects. The frequency modulation schemes are widely available from solid-state transmitters. The range detection hence the frequency measurement can be performed with quickly advancing digital processors and algorithms. Besides, the highly deterministic waveform allows better prediction of the return hence improves the detection of target. Low probability of intercept waveform also makes intercepting or jamming the FMCW radar signal more difficult. Theoretical analysis shows that the range resolution of FMCW radar is determined by the chirp bandwidth and chirp linearity [8].

1.1.4 Radar around 94GHz

The phased array antenna's size and shape depend on the frequency or wavelength of the radio waves being sent or received and the number of antenna elements. To reduce the dimension of each antenna element, the frequency of the signal it transmits or receives should be increased. For our integrated beam forming demonstration system, the small antenna size means signal frequency on the order of 100 GHz. The planned final version of the system even requires signals to be as high as 300 GHz. The maturity of suitable technology that provides passive and active devices, operating at such high frequencies, allows large scale integration of these beam forming systems.

Another reason for the interest in millimeter wave radar is due to a minimum (window) in the atmospheric attenuation in the vicinity of 94GHz. Although the attenuation is actually higher compared to the attenuation of water vapor absorption line around 22.2GHz [9], the bandwidth of that window points the potential of wide band operation of millimeter wave radar.

1.1.5 Advances in SiGe Technology

Although there are considerable research activity going on to explore the possibility of using CMOS transistors for millimeter wave applications. They are fundamentally not devised for these applications. Some III-V compound based technology such as InP or GaAs shows much better performance due to their far higher mobility, higher saturation velocity, as well as, their direct-gap band structure [10]. However, their higher cost prohibits large scale production. The advent of Silicon-Germanium (SiGe) Base Transistor bridges the gap between cost and performance. Through band gap engineering to the base region, the transistor performances in terms of current gain, base-transit time, emitter-base junction charging time are improved. These improvements lead to significant increase of transistor transit frequency which makes SiGe transistor competitive to III-V compound transistors for high frequency applications.

The advance of commercially available SiGe technology has already pushed transistor transit frequency up to more than 200GHz [11], which opens up the possibility for application even in mm-wave range. Other than the advance of active transistors, improvement of the on chip passive structures extends the functionality of these high frequency circuits. The IBM 8hp BiCMOS process features 0.13um SiGe bipolar transistor, 0.12um FET transistor, 7 backend metal layers, high precision MIM capacitor, varactor [12]. The thick top metal layer makes it possible to build various passive structures such as transmission line and high Q inductor that are essential for higher frequency circuits.

1.2 Design Challenges and Objectives

In our (sub)mm-wave radar system, the beam forming ability of phased array and the advantages of FMCW operation are combined to achieve three-dimensional positioning capability(See Fig 1.2 for illustration). This combination also means more design challenges than a system adopting either one of the techniques.

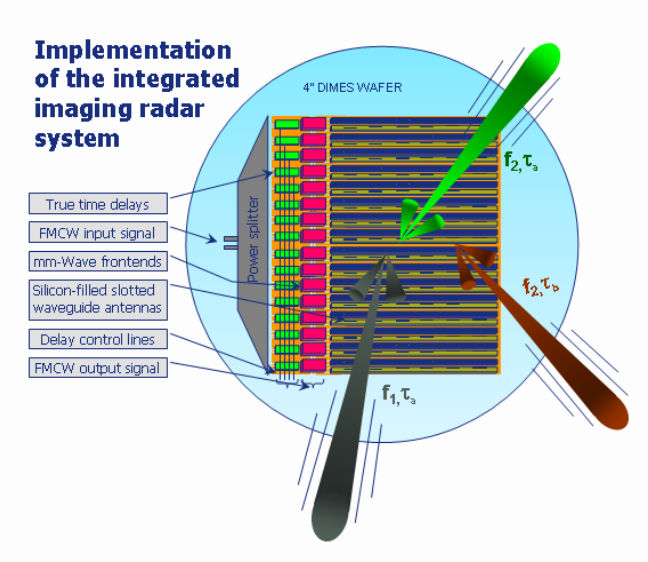

Fig 1.2 Illustration of our FMCW phased array radar system [13]

The phased array system implemented within MEMPHIS requires a large signal bandwidth for stirring the beam to give wide observation angle. However, it is very difficult to generate wideband high quality linear FMCW signal at higher frequency. To enhance the chance of success, the frequency chirp signal will be first generated at lower frequency and then up-converted to W band to drive the antennas. The up-conversion process is the central task of this subproject.

The circuit for signal up-conversion is subjected to various performance requirements. It should cover the necessary bands between the input signal band and the output signal band around 100GHz. Both active and passive circuit performance is expected to change tremendously across this frequency range. Different circuit topologies suitable to operate in different frequency range will be investigated. The wide bandwidth means many frequency components of considerable strength coexist in the circuit. They should not affect the normal operation of the circuit. Efforts must be made to guarantee stability with the presence of these frequency components. Since the same signal will be used for transmission as well as the LO signal of the receiver mixer, noise performance of the circuit should be addressed. The wideband requirement appears to be a multiplication factor to the other requirements mentioned above. Besides, since each row of antenna elements have their own signal up-conversion circuit, there will be dozens of up-conversion circuit within the whole system. Hence, the DC power consumption should be controlled to a reasonable value. These design challenges will be addressed in detail in the following chapters.

1.3 Organization

Chapter 2 reviews the theory and design examples of various frequency multipliers. Key design considerations are summarized and adopted to the design of a wideband frequency doubler. Performances of the doubler under different drive conditions are analyzed and hold as a reference for the design of a high order multiplier chain in the next chapter.

Chapter 3 begins with a study about the harmonic generation mechanism within a multiplier chain. Then circuit blocks are defined based on functional division of the whole signal up-conversion chain. Design methodology of a Multiply by 8 Chain is presented. Design considerations for each building block are also discussed. Performance of the multiplier chain is presented with simulation results.

Chapter 4 discusses the circuit blocks that operate in W band, mainly the driver amplifiers for the transmitter antenna and for the mixer LO port. Their design strategies are explored and verified through simulation.

Chapter 5 summarizes the whole design and mentions the future work related to this topic on different levels.

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Chapter 2 Frequency Multiplier

The core circuit for frequency up-conversion is frequency multiplier. It translates a lower frequency input signal to output signal at higher frequency. This type of circuit is widely used for generating signal at higher frequencies. This chapter will start with a review of the theory and examples of various types of frequency multipliers. A balanced frequency doubler will be proposed and its design considerations and performance will be discussed. This doubler will be used in our frequency up-conversion chain. Its interaction with other related circuit blocks will be discussed in chapter 3.

2.1 Theory and Realization

Frequency multiplication is a means to generate a signal at an integer multiple of source frequency. This is very often realized by generating higher harmonics from the input signal. Numerous designs have been put forward based on this idea at frequencies ranging from Sub GHz to THz, including both passive and active circuits. In this section, we shall take a look at the theory and examples of some most widely used frequency multipliers.

2.1.1 Passive Frequency Multiplier

Generating harmonics is the trait of nonlinear circuit. In many applications, this is considered a downside and should be avoided. However, if used constructively, the nonlinearity can be advantageous for frequency generation. Many passive circuits, including varactors, step-recovery diodes (SRDs), and Schottky-barrier diodes, show nonlinear transfer function due to various reasons, which makes them good candidates to make frequency multipliers.

According to the discussion in [1], reactive multipliers, including varactors and SRDs, depend on the diode's nonlinear capacitance. Being reactive components, their advantage lies in introducing very little noise of their own, only from the parasitic series resistance and the losses. When low phase noise is desired, this proves to be most valuable. On the other hand, a tuning circuit is often used to match these devices to the source impedance and to improve efficiency, which makes their performance optimized for narrow bands. By comparison, varactors are oftenly used for lower-order multiplication, and SRDs are more suited for higher order multiplication mainly due to their stronger nonlinearity. The short pulse generated by them contains stronger higher order harmonics.

2.1.1.1 Reactive Frequency Multiplier

The operation of a varactor multiplier can be analyzed with the model shown in Fig (2.1), the varactor is driven from a single-tone current source.

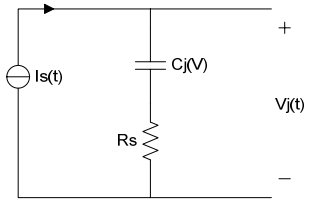

Fig 2.1 Simply model for varactor multiplier

With open circuit assumption on harmonic frequencies, no frequency component other than the fundamental current exists in the junction The charge stored across the varactor thus varies with the sinusoidal current and it will be of the same frequency. From the Q/V relation of an ideal uniformly doped junction, V can be expressed as a function of Q:

$$V = \phi\left(\frac{Q_\phi^{\,2} - Q^2}{Q_\phi^{\,2}}\right) \tag{2.1}$$

In which, $Q_\phi = 2C_{j0}\phi$ is a constant. ϕ is the diffusion potential and C_{j0} is the zero-bias junction capacitance. Equation 2.1 shows that the sinusoidal varying junction charge will cause the junction voltage to vary as a sinusoidal of double frequency. Thus frequency doubling is accomplished with the ideal nonlinear Q/V(I/V) relation. However, the square transfer limits the harmonic to the second order if only fundamental current runs through the junction. In order to achieve higher-order multiplication, current of some intermediate frequency should be allowed to flow through the junction. So, the mixing product of the fundamental and intermediate frequency components will be at harmonics higher than the second. Conceptually, this is done by an ideal block called “idler”, which provides short circuit connection only to the designated frequencies.

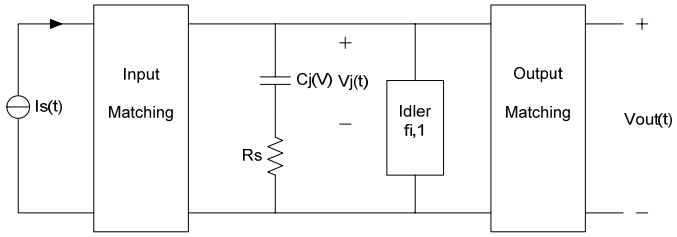

Fig 2.2 varactor multiplier with idler and matching

For instance, in Fig 2.2 an idler short-circuits the varactor on 2nd harmonic frequency (2fo). With all other conditions unchanged, 2fo current circulates in the loop made up of the varactor and the idler. Now, both fo and 2fo current exist in the junction, through the square Q/V relation, now also a 3fo voltage is generated through 2nd order mixing. By providing idlers at other intermediate frequencies, any high order harmonics can be generated in principle. But the efficiency drops quickly as the order increases. Anyway, by maximizing the intermediate frequency current, idler does help to improve conversion efficiency.

The operation of SRD depends on the strong nonlinear C/V characteristic. It is capable of generating a very steep voltage pulse during each excitation cycle. Then harmonics can be selected through filtering. Narrow pulses contain stronger higher-order harmonic components, so SRD is more suitable for higher-order multiplication. An idler can help the SRD to get higher-output power. Port impedances on certain frequencies are defined as the ratio of the voltage and current components on that frequency. Matching at the harmonic frequencies makes this type of multiplier narrowband.

2.1.1.2 Resistive Frequency Multiplier

As alternative to the above mentioned varactor multipliers, resistive diode multipliers show quite the opposite features, lower conversion efficiency but more predictable behavior and capable for wideband operation.

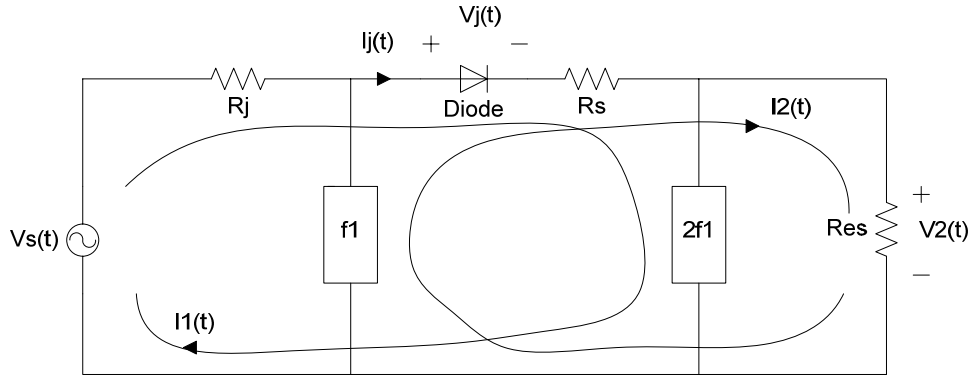

Fig 2.3 circuit of a resistive diode frequency doubler

Shown in Fig 2.3, the Schottky-Barrier diode is represented by an ideal diode and its series resistance, the junction capacitance is assumed to be negligible at this point. The two black boxes with note f_1 and $2f_1$ have ideal band stop characteristic, each only shows infinite impedance to the fundamental and second harmonic frequency respectively, and provides short circuit to all other frequencies. Rj represents the source impedance which is matched to the input impedance of the diode on fundamental frequency, this impedance is defined as the ratio of fundamental junction voltage $V_1(t)$ to fundamental junction current $I_1(t)$.

First assume that the load impedance R_{ld} is small enough that the voltage drop on it can be neglected. When appropriate bias and input power are selected, the diode can be turned effectively on and off during each excitation cycle. The junction current $I_j(t)$ is a train of pulses that can be approximated by half cosine waves. This waveform contains all the harmonic components of the input frequency. Now the two band stop filters come into the picture, they force the fundamental and second harmonic current to flow along the route shown in Fig 2.3. Only these two currents cause a voltage drop on the junction and resistors, remember that for all the other frequencies, the diode current is short circuited by these filters

thus all the other harmonic currents circulates within the loop made up of the diode and two filters and do not contribute to voltage.

In [1], through the calculation of fundamental input power and output power on second harmonic, it is found out that even with zero series resistance, the maximum available conversion gain is very low, only -8.8dB. With most of the input power lost in the diode junction, the resistive diode multiplier is by nature not so efficient.

The study of resistive diode multiplier shows that the output power is determined by the shape of output voltage and current waveform. Proper current pulse shape and a large Imax give the highest possible output power. This is achieved by proper choice of dc bias and input power. Harmonics in the junction current are selected by terminal conditions, which can be realized in many ways resulting in different operation bandwidth. Although the output power is lower, resistive multiplier has the potential of wideband operation.

2.1.2 Active Frequency Multiplier

2.1.2.1 Modeling Harmonic Generation

Large amount of work has been done on the topic of active frequency multiplier over many decades. Both experimental results and analytical models have been published. In literature, FET are picked for analysis mainly due to the extensive use (MESFET,HEMT etc.) in high frequency multipliers. Nevertheless, we shall see that the general analysis can be extended to bipolar device without losing validity.

To understand how devices operate for frequency multiplying purpose, it is instructive to study models that describe the nonlinear transfer. Ciardha, Lidholm and Lyons [2] made a pretty comprehensive summarization of the modeling at their time, and improved those by developed a more unified description. Here we shall follow their generalization first.

There are several sources of nonlinearity in a FET, including C_{gs} nonlinearity, I_{ds} clipping and the nonlinear $V_{gs} - I_{ds}$ transfer characteristic. Although they all contribute to harmonic generation in I_{ds} , some are not strong enough to give high conversion efficiency. Gopinath et al. [3] found that I_{ds} clipping is the primary contributor to second harmonic generation. They also concluded that a gate bias near pinch-off or near forward conduction is the optimum bias points for frequency doubling operation. In both cases clipping of the I_{ds} current waveform leads to significant harmonic generation.

In the book of Maas [1], forward conduction is avoided and a piecewise linear transconductance model is adopted mainly to describe I_{ds} clipping near pinch off. Although this model is idealized, it embodies the principal source of harmonic generation and helps to derive a first-order estimate of the optimum drive/biasing combination.

When the device is biased near pinch off, then the ac input brings the instantaneous gate voltage above pinch-off only during a faction of the full ac cycle. This mode of operation is similar to that of a Class-B or Class-C amplifier operation. Hence the induced drain current appears as a train of discrete pulses, which can be modeled as a rectified cosine wave. Klymyshyn et al. adopted the same model in their harmonic generation analysis [4]. Here we follow their expression of relating the conduction angle to the harmonic signal content.

The conduction angle of current pulses can be varied with the dc gate bias and input power. Suppose $V_{gg} < V_{th}$, which is the usual situation, the FET is turned-off during most of the excitation cycle, then the conduction angle is low. Let 2θ denote the conduction angle (in degrees).

Let t_0 denotes the current pulse duration, T is the period of excitation, t_o / T is the duty cycle.

According to the pulse shape assumption, the Fourier-series representation of current pulse contains only cosine components,

$$I_d(t) = I_0 + I_1 \cos(w_p t) + I_2 \cos(2w_p t) + \cdots + I_n \cos(nw_p t) + \cdots \qquad (2.2)$$

where w_p is the angular frequency of the excitation signal.

When $n \geq 1$, the coefficients are

$$I_n = I_{\max} \frac{4\theta}{\pi^2} \left| \frac{\cos n\theta}{1-(2n\theta/\pi)^2} \right| \qquad (2.3)$$

and

$$I_{dc} = I_0 = I_{\max} \frac{2\theta}{\pi^2} \qquad (2.4)$$

In order for the multiplier to achieve maximum output power and efficiency, I_n on the desired harmonic should be maximized. Gate bias and input power can be adjusted to set θ to the value which maximizes I_n.

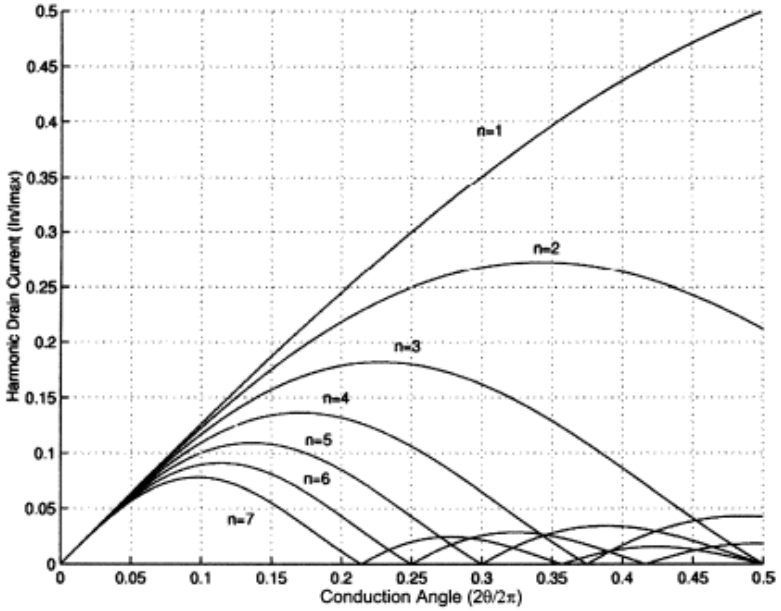

Fig 2.4 Ideal drain harmonic current vs. FET drain conduction angle[4]

Plotting the harmonic components as a function of θ as in Fig 2.4, we can observe how duty cycle affects the harmonic components. It is obvious that the peak value of higher harmonic is less than for the lower harmonics. The peak value of higher harmonic appears at lower conduction angle. For example, the 2nd harmonic has a peak near $\frac{t_0}{T} = 0.35$, while the peak of 4th harmonic is near $\frac{t_0}{T} = 0.16$. So, to maximize certain harmonic component means to maximize the peak current value $I_{\max}$ as well as to choose the optimum conduction angle to maximize the ratio $I_n / I_{\max}$.

Looking at figure 2.4, we observe that the conduction angel related to the dip of 4th harmonic content is close to the one related to the peak of the 2nd harmonic. It is thus possible to suppress a certain harmonic by proper biasing. However if the input power has to be adjusted or the circuit should handle a large range of input power, this condition can not be met all the time.

With the same piecewise linear gm assumption as Maas, Ciardha et al. [2] modified the model. Instead of half-wave rectified sinusoids, the current waveform is assumed to be a clipped sinusoid, proportional to the part of gate voltage that exceeds the threshold voltage. These models give close results up to conduction angle of 180 degrees, which is suitable to describe the current pulse generated in a Class-C like operation mode.

One could come to some practical problems when trying to increase the higher harmonic with

this operation mode. If we take 3rd harmonic as an example, its peak value is $0.185I_{\max}$, which is occurs at $\frac{t_0}{T} = 0.21$. It is not a good choice to lower the conduction angle by reducing $I_{\max}$, since that also reduces the overall output power. The gate voltage swing should be increased together with a decrease of gate bias to reduce the conduction angle. Since the phase of drain voltage is opposite to that of the gate assuming any delay in the device can be ignored, the maximum reverse gate-drain voltage could exceed the break down limit under large drive. Meanwhile the high input power required, means low gain and that is against the goal to improve the overall efficiency of the multiplier.

Other bias schemes have been investigated to increase the efficiency of certain harmonics. Fudem and Niehenke proposed in [5] a different bias scheme that is suitable for 3rd harmonic generation. They did not bias the FET device near pinch off. Instead, they choose the bias point half way between pinch off and forward conduction. With this Class-A DC bias, when driven hard, the drain current clips near both the positive and negative peak of input sinusoidal and approximates square wave. In this way, both current clipping mechanisms are utilized for harmonic generation. The Fourier coefficients of an ideal square wave are

$$I_n = \frac{2I_{peak}(-1)^n}{n\pi}, \text{ when n is odd} \tag{2.4}$$

$$I_n = 0, \text{ when n is even} \tag{2.5}$$

The peak value of I_3 from an ideal square wave is higher than that from a half cosine pulse wave. It seems that this operation mode is better suited for odd-order harmonic generation.

Based on the two operation modes above, Ciardha et al. [2] made a more generalized model which takes into account of both single side and double side clipping. A contour analysis was conducted to find out the optimum bias and conduction angle for doubler and tripler operation. It is confirmed that the optimum point found with the half cosine wave model was valid for doubler optimization and that the square wave model was valid for tripler optimization.

As an extension of their theory, Ciardha et al. [2] checked the square wave with duty cycle of 1/6. It gives the same amount of 3rd harmonic component, but there will be even order harmonics and a considerable DC current in the output mainly due to Class-C operation. In fact, this low conduction angle poses a high risk of breakdown that it is less likely to be realized with actual FET device. However, the difference in 2nd harmonic content shows an important aspect of frequency multiplication----unwanted harmonic suppression.

The study of mathematical model for single transistor harmonic generation reveals the relation between the relative harmonic strength and conduction angle, which serves as the bridge to link the circuit performance to bias and excitation condition.

2.1.2.2 Harmonic Termination

Next to setting the right DC bias and the optimum input power, harmonic terminations at both input and output have a strong impact on both the desired and the undesired harmonic output. Many design strategies are developed to find the right combinations of the harmonic termination that gives the best performance.

There is more consent about the source impedance at the fundamental frequency and the load impedance on the desired output. At the input, conjugate matching maximizes the power delivered to the input. So, $Z_{src,f_0} = Z_{src,f_0}^{*}$ improves the conversion efficiency. However this power dependant input impedance is usually different from the small signal value. At the output, maximum output power is obtained according to loadline theory. Optimum load impedance at desired frequency Z_{ld,xf_0}, guarantees the use of full voltage and current range available at the device output. That means to fit the saturation limit with the full current swing. Thus, the output power is maximized.

Many researches have been conducted toward the influence of the source and load impedance on other harmonic frequencies to conversion gain, harmonic suppression, stability etc. of the multiplier.

In [1], Maas's conclusion is quite representative for the more traditional view. At the input, although short circuit on some other harmonic frequencies may not maximize the desired output, it is preferred for stability concern. For instance, as for a doubler, second harmonic at the input many increase the desired output if the phase relation is favorable to the secondary mixing effect. At the output, to avoid generating power on unwanted harmonics, as well as for stability, short circuit terminations are also desirable. He mentions that instability in active frequency multipliers usually results from a reactive drain termination at frequencies where the drain should be short-circuited.

Thomas and Branner [6] verified this widely adopted approach through checking different combination of harmonic termination quantitatively. In several publications [7] [8] [9], Johnson and Branner studied the effect of source and load impedance as well as the DC bias shift of the multiplier device. Although not expressed explicitly, simulation results point out that their adjustment changes the output harmonics, wanted or unwanted, through affecting the current wave form. The essence of maximizing the wanted harmonic and minimizing the unwanted harmonic is to shape the current waveform to the optimum form.

Campos-Roca et al. [10] investigated the secondary influences of the harmonic terminations: the 2nd harmonic source impedance at the input, the fundamental, 2nd and 3rd harmonic load impedance for doubler and tripler. Multiharmonic load-pull is

performed. Circuit simulator optimization function is utilized to find the best combination of these impedances. The harmonic terminations other than the fundamental at the input and the desired one at the output are kept reactive to avoid unnecessary power losses. The phases from their reflection coefficients are swept to find the optimum point. Then actual matching network are designed according to these findings. Also, sensitivity toward component and frequency variation is considered. From the load-pull contours, the absolute best performance as well as the sensitivity toward the harmonic termination is shown. Although producing a good result, this procedure is device specific, and it deals with single-stage multiplier design. The major goal is still to maximize the output power at desired frequency.

2.1.2.3 Unwanted Harmonic Suppression and Filtering

For many applications, on top of a relatively large output on the intended harmonic frequency, it is desirable to suppress the other harmonics and the fundamental frequency. If we first look at the output, some form of filtering can serve this goal. For example, a high-low impedance filter is connected close to the drain to filter out the fundamental and odd order harmonics, then output matching converts the load impedance to the right value for higher efficiency.

For frequency doubler, the fundamental and the third harmonic components should be short circuited. A quarter-wavelength open stub can short circuit these components without affecting the 2^{nd} harmonic output. However with transmission lines, e.g. a microstrip line, short and open circuit condition is only valid within a narrow band. Although being a simple scheme, this leads to a narrow bandwidth inevitably. Frequency tripler is a bit more tricky, there is no such simple elegant way of short circuiting both fundamental and the 2^{nd} harmonic component without affecting the 3^{rd} harmonic, probably some bandpass filter has to be used. Similar problem also exists in higher-order multiplication.

In [4], Klymyshyn and Ma demonstrated the design and optimization procedure of a 4^{th} order multiplier. They used a coupled line bandpass filter to suppress the unwanted harmonics, especially strong lower order components, like the fundamental, 2^{nd} and the 3^{rd}. Between the filter and the drain terminal, matching network converts the 50 ohms to the optimum fundamental impedance. The drain bias choke and output matching branch form approximately reactive impedance on odd-order harmonics and optimum impedance on the 4^{th} harmonic. At the design frequency, the nearby harmonics are at least 30 db lower than the 4^{th} one. Since the filter has a passband of about only 3GHz around 28GHz and the input and output matching network also limits the bandwidth, the multiplier shows a -3db bandwidth of 500MHz. Nevertheless, it shows a good design approach for narrowband single stage high order multiplier.

2.1.2.4 Balanced Circuit for Harmonic Generation

The operation bandwidth of a frequency multiplier is defined mainly according to the output signal at the desired bandwidth and the suppression at unwanted harmonic or spur frequencies. The above mentioned theories mainly focus on a single operation frequency. It is rather difficult to extend these approaches to wideband design because of the narrowband harmonic

termination implemented with passive network. Filtering should instead be realized in other forms that are not so sensitive to frequency variation. Before we deal with balanced multipliers which adopt this idea, let's first have a look at some basic ways of microwave components interconnection [1].

A single device has limitations that may be troublesome in certain applications. Sometimes by connecting multiple devices with either passive power combining components or in a direct fashion, the circuit can give better performance in terms of output power or eliminating troublesome harmonic or intermodulation components. Here we will study some balanced circuit through direct connection that are related to frequency multiplication.

Fig 2.5 shows the voltage and current relations in a nonlinear model with three different voltage and current polarity. The + sign on the device block shows the reference polarity of the device, to which the voltage and current directions are referred. Fig 2.5(a) shows a nonlinear device with V/I relationship described with

$$I = f(V) = aV + bV^2 + cV^3 + dV^4 + \cdots \tag{2.6}$$

If the polarity in Fig 2.5(a) is hold as a reference, then Fig2.5(b) illustrates the connection by reversing the port voltage but retaining the port current direction.

$$I = f(-V) = -aV + bV^2 - cV^3 + dV^4 + \cdots \tag{2.7}$$

And Fig2.5(c) illustrates the connection by reversing both the port voltage and the current directions.

$$I = -f(-V) = aV - bV^2 + cV^3 - dV^4 + \cdots \tag{2.8}$$

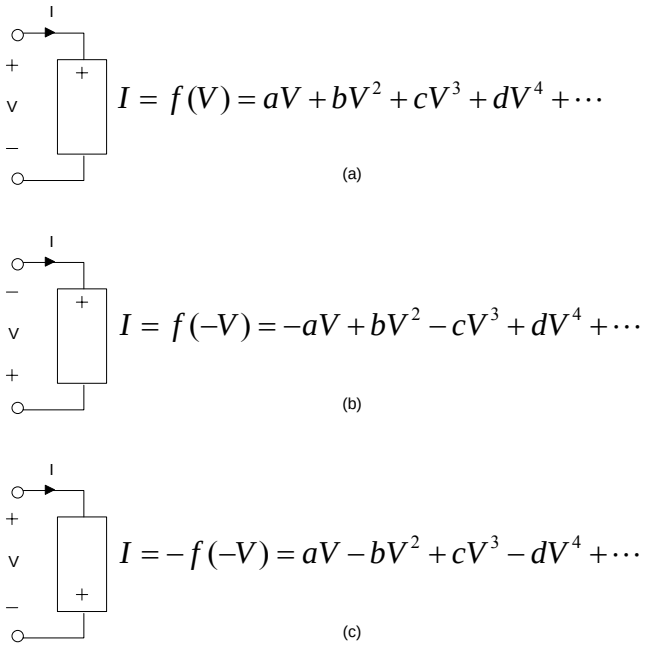

Fig 2.5 V/I relation in a nonlinear model with different voltage current polarities

As we can see that in Fig 2.5(b) and (c), either odd order and even order components in the current have changed sign with respect to the reference. This property can be utilized to separate and select even and odd order harmonic components through directly connecting two devices together. The theory is demonstrated here with two terminal nonlinear devices, but it can be extended to 3 terminal devices like FET or BJT.

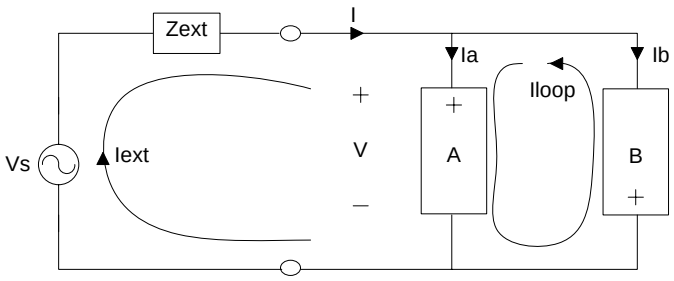

Fig 2.6 Anti-parallel connection of two nonlinear 2 terminal devices

Fig 2.6 shows the anti-parallel connection. Current in device A, I_A is found by

$$I_A = f(V) = aV + bV^2 + cV^3 + dV^4 + \cdots \tag{2.9}$$

Accordingly, current in device B, I_B is found by

$$I_B = -f(-V) = aV - bV^2 + cV^3 - dV^4 + \cdots \tag{2.10}$$

Their sum is the external current, I_{ext}, which circles in the excitation source and the external impedance. This current defines the terminal voltage of the anti-parallel connected devices.

$$I_{ext} = I_A + I_B = f(V) - f(-V) = 2aV + 2cV^3 + \cdots \tag{2.11}$$

Only odd-order components exist in I_{ext} and they are doubled in strength. It seems as like the external circuit does not see any even-order nonlinearity in the devices. By looking at the difference in I_A, I_B and I_{ext}, one can find that the even-order components form an internal circulating current, I_{loop}. There is no odd-order component in this internal current.

$$I_{loop} = I_{A,even} = -I_{B,even} = bV^2 + dV^4 + \cdots \tag{1.12}$$

Since the even-order components do not flow in the external loop which consist out of the source and the external impedance, they do not contribute to the terminal voltage of the anti-parallel connected devices. In another word, the two devices effectively short circuit each other on all the odd order frequency components.

Another important point is that, since even-degree nonlinearity generates even-order mixing products, under the circumstance of multiple excitations, anti-parallel connected nonlinear

devices generate no even–order mixing products from the frequency in their terminal voltages. This is in fact the property that helps to suppress unwanted harmonics and spurs in frequency multipliers for wideband operation. For example, anti-parallel diodes can realize a frequency tripler with low 2nd and 4th harmonic output.

A dual example to the anti-parallel connection is the anti-series connection as is shown in Fig 2.7.

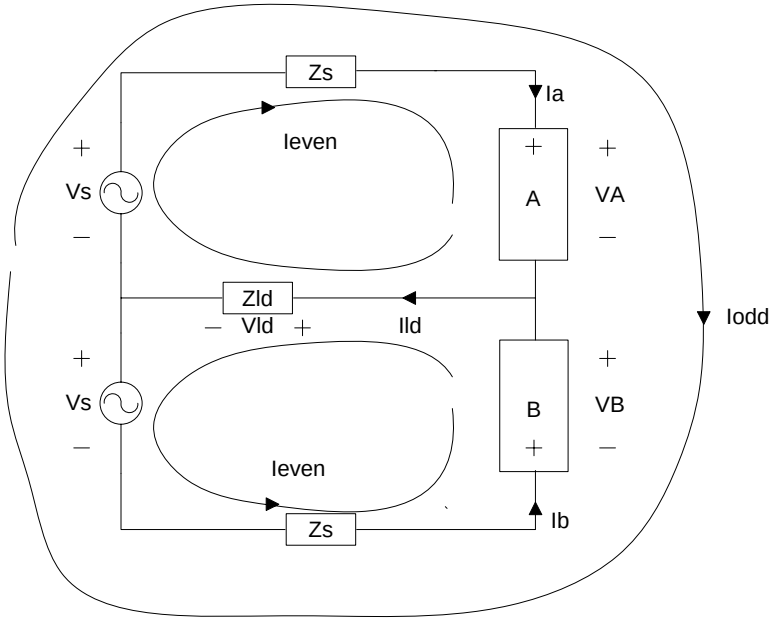

Fig 2.7 Anti-series connection of two nonlinear 2 terminal device

Due to circuit symmetry, we have $V_A = V_B = V$ .Also $I_{ld} = I_A + I_B$, in which I_A and I_B are the reference direction of the current in device A and B. From equation (2.6) and (2.7), we have the following current expression:

$$I_A = f(V) = aV + bV^2 + cV^3 + dV^4 + \cdots \tag{2.13}$$

$$I_B = f(-V) = -aV + bV^2 - cV^3 + dV^4 - \cdots \tag{2.14}$$

$$\text{So,}\quad I_{ld} = I_A + I_B = 2I_{even} = 2bV^2 + 2dV^4 + \cdots \tag{2.15}$$

The even order current component I_{even} circulates in the upper and lower loop including the load impedance Z_{ld}. I_{even} from two loops combine at the nod where device A and B are connected directly and form the load current. There are no odd-order components existing in I_{ld}, since they circulate in the overall big loop without Z_{ld}. As a result, I_{odd} does not contribute to the load voltage V_{ld} and the upper half loop consisting Vs, Zs and device A short circuits the lower half consisting Vs, Zs and device B on all odd order term frequencies, and vice versa. Under the circumstance of multiple excitation, anti-series connected nonlinear

devices generate no odd–order mixing products in their center-tap terminal voltages. In this regard, anti-series connected diodes have also good potential to make a wideband frequency doubler.

In the above analyses, several assumptions are vital. Identical nonlinear elements, source impedance together with perfectly balanced excitation guarantee the ideal harmonic selection property of these circuits. In reality, finite unbalance of input signal and mismatch between the nonlinear devices would degrade the ideal harmonic cancellation. Anyway, the above mentioned connections reduce the unwanted mixing product seen by the load compared to a single device. This relaxes the requirement on other filtering function considerably. The frequency independence feature of this cancellation scheme makes it very appealing for wideband operation.

As an example, Fig 2.8 shows the idea of an anti-series frequency multiplier. The devices are driven out of phase from a balun, and the drain terminations are connected together at point C. It acts like a virtual ground at fundamental and all odd-order harmonics since the two devices short circuit each other at those frequencies. The even-order harmonics combine at point C. Through output matching, the desired even-order harmonic is selected.

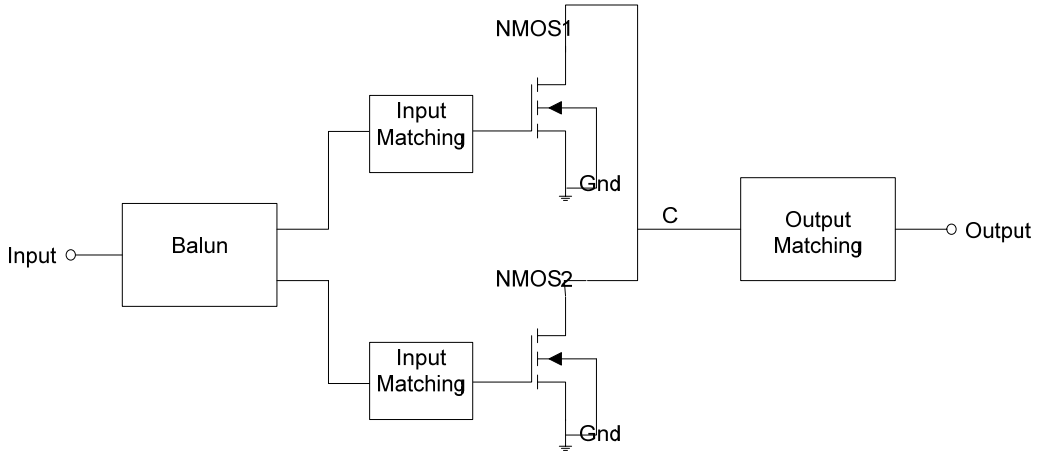

Fig 2.8 anti-series balanced frequency multiplier

2.1.3 Other Frequency Multiplier

The above mentioned multipliers depend mostly on device nonlinearity from a single transistor. We shall look at some other multiplier design examples, for a broader view on the use of nonlinearity in frequency multiplication, especially frequency doubling.

Fig 2.9 helps us to illustrate an instinctive view toward frequency doubling. The parabola represents the transfer function between the input and output signal. When this transfer function can be described with $y = kx^2$, then an ideal sinusoidal input signal can be converted to a sinusoidal output signal on double frequency, while no other harmonic tones will be

produced.

Various circuits are proposed or utilized to shape such a transfer function. In [11], Kimura et al. used two identical unbalanced emitter-coupled pair with emitter area ratio K to shape the large signal transfer function. By choosing different K value, they can approximate the parabolic transfer function within the various input ranges. It is a good idea for a low-frequency doubler, however this topology shows some inherent drawbacks that prohibit it to be used at higher frequency. The difference on device size makes the capacitive parasitic on two output signal paths differ a lot, which limits the balance of two output signals. The large device area ratio means an inevitable increase on input capacitance which is not preferred for high frequency operation.

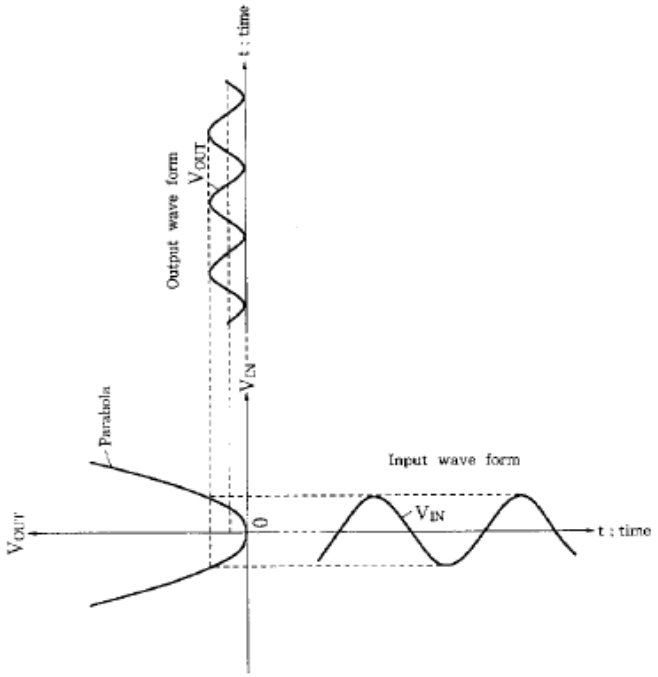

Fig 2.9 Graphical illustration of frequency doubler operation [11]

Translinear circuit [12] can be used to synthesize certain mathematical relation between the input and output. A deesign based on this idea has been proposed in the 70's [13]. Once again the idea is elegant at low frequencies. However, the translinear principle relies on the assumption of low base current and low parasitics to derive the ideal input output relation. The presence of these parasitic terms gives rise to distortion in the output signal. At higher frequency, parasitics of both transistors and einterconnection or current sources seriously reduce the validity of these assumptions. The spurs generated due to the imperfections are not tolerable to our application. Hence this idea does not suit our system either.

A subharmonically-injected quadrature LO generator is proposed by Ma et al. [14]. The ring oscillator tracks the injected signal and produces 3rd harmonic quadrature signal. However the phase unbalance between I/Q outputs varies with the locking frequency. Since our system does not require quadrature signals at this point, the complexity for generating the quadrature outputs does not seems to be worthwhile. Besides, whether this topology can work over a large bandwidth still needs to be investigated.

Mixers are used to obtain the sum or difference frequency from two input tones. It is natural to use the mixer as frequency doubler by feeding the RF and LO port with signal on the same frequency. Hackl et al. demonstrated a narrow band frequency doubler based on mixers [15]. The advantage is that double balanced mixer has both differential input and output ports, so a balun is not needed between two mixers. The problem is that the mixer operation generates many unwanted spurs other than the sum frequency tone. It is difficult to suppress these spurs over a wide bandwidth.
In [16], Xuan et al. built their frequency doubler based on full-wave rectifier. The idea is similar to the one shown in Fig 2.9. But instead of a parabola transfer function, the rectifier provides a transfer function that looks like a bended line. The nonlinearity to produce double frequency component is available, only much more harmonic components will also be generated. Their measurements shows a flat conversion gain and better than 50dB fundamental suppression over 20% of relative bandwidth. Further extension of this idea accords with the idea of balanced frequency doubler presented in the last section. Its sheer simplicity means better chance to be used at millimeter wave frequencies.

2.1.4 Multiplier Chain

The analysis in section 2.1.2 shows that active transistors may not make good frequency multipliers with higher multiplication factor due to low conversion gain and output power. However, there are also needs to build higher-order multiplier for some applications. Maas [1] recommended use low order, most likely doublers or triplers, in cascade to construct a higher order multiplier chain. Buffer amplifiers may be necessary to provide enough gain, as well as isolation. Some design examples of higher order multiplier chain are presented here.

Wang et al. used doublers and buffer amplifiers with HEMT technology to build a 23.5 to 94 GHz quadrupler more than 10 years ago [17]. It gives a conversion loss of about 6dB near the design frequency. Measurement results show that gain compression is achieved in a wide input power range. The work demonstrated the possibility to make high order multiplier chain into W band

Karnfelt et al. built their X8 multiplier for 60GHz transceiver by cascading a quadrupler and a doubler with buffer amplifiers [18]. Gain compression is emphasized in the design. Results show a flat output power over 10dB input power change. Nearby harmonic suppression is also considered.

Kallfass et al. built their sixtupler by connecting a tripler with a doubler [19]. Filtering effect from higher order interstage matching network is utilized to select the desired harmonic and reject spurs on other frequencies. Balanced structure broadens the relative bandwidth in W band to 28.6%. All in band spurs are found to stay below -25 dBc with respect to the desired sixth harmonic.

2.2 Frequency Doubler Design

2.2.1 Circuit Topology

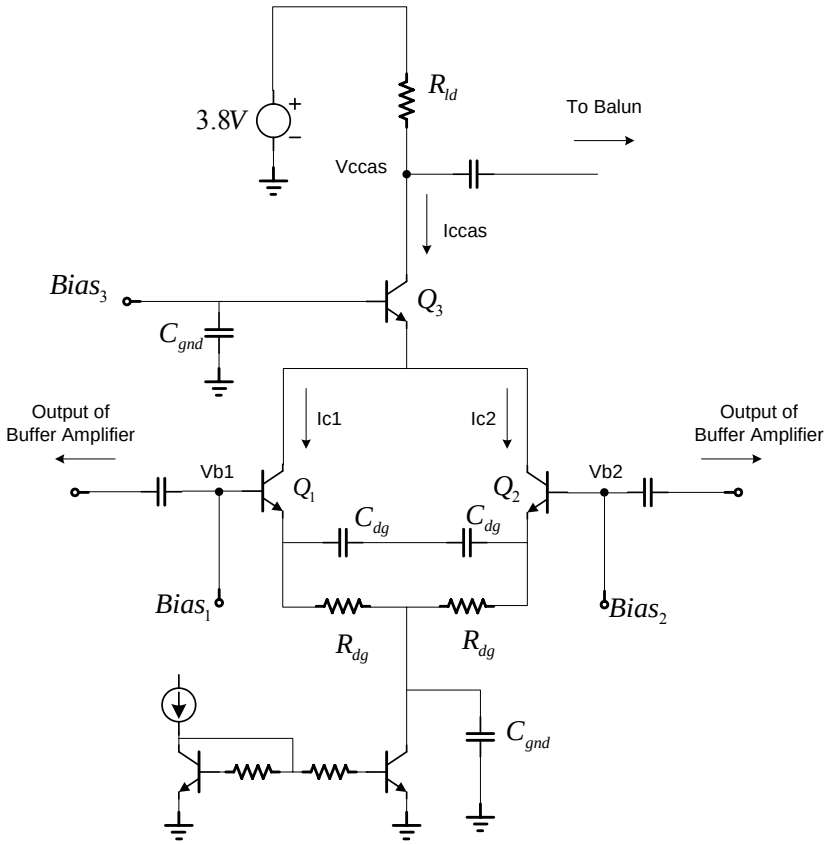

Fig 2.10 Circuit topology of the balanced doubler

Fig 2.10 shows the frequency doubler topology. It is composed of an anti-series differential pair, a cascode transistor and a tail current source and proper decoupling. The voltage bias circuit is omitted. The anti-series differential pair is the core of this block. The bias current has a strong impact over the harmonics produced. The bias point is chosen according to the criteria discussed in the previous chapter. Simulation verifies that 2nd harmonic could be enhanced when the differential pair is operating like a Class-C power amplifier. Considering the available input power from the buffer amplifier, it is found that the optimum collector DC bias current is about 40% of the peak ft current. At this bias point, the conduction angel is suitable for a large 2nd harmonic output and relatively low 4th harmonic. Simulations with different scale of transistor at different frequency lead to this conclusion.

Tail Current Bias

Since the bias point is not much higher than the turn-on point of the BJT transistor, the transient collector current, as well as the conduction angle of the transistors is quite sensitive to the variation on the DC Base-Emitter bias. So, voltage bias through the base of the differential pair may not be accurate enough. Instead, the differential pair could be biased

with a tail current. In this way, as long as the current source is made accurate, it is not too difficult to duplicate the current accurately with a current mirror. The circuit is also made insensitive to the gate bias variation of the differential pair since the emitters are now connected to the collector of the tail current transistor through degeneration components and is effectively floating DC wise.

The high impedance looking into the collector of the tail current source, although lowered somewhat at higher frequency by parasitic capacitance, reduces the common-mode current flowing in the differential pair. This is indeed the mechanism to provide common mode rejection in a normal differential pair. However, the even harmonic output currents of this frequency doubler are in common mode. To maximize the 2nd harmonic output current, this high impedance must be decreased at the operation frequency. A simple idea is to provide a short circuit to ground by large capacitor. Since the on chip ground is far from an ideal ground plane, proper decoupling must be done at that point to guarantee conversion gain, as well as to avoid oscillation. There were also ideas of implementing a harmonic termination with a certain length of transmission line to suppress the unwanted harmonics at the same time. But due to parasitic from the tail transistor, these harmonic terminations are not so effective over a wide bandwidth. In view of this, a wideband short circuit to ground with LC resonator is chosen here, the inductor needed is small enough to be implemented with a short interconnecting.

RC Degeneration

Between the tail current source and the differential pair is the RC degeneration which compensates the frequency related gain drop. The intuitive explanation is that the degeneration resistor R_{dg} reduces the effective transconductance of the pair at lower frequency while the degeneration capacitor C_{dg} introduces a zero to that transconductance, which makes it increase up to the frequency where the effect of degeneration is negligible. The output current hence shows a relatively flat curve to frequency sweep. The typical frequency response is illustrated in Fig 2.11.

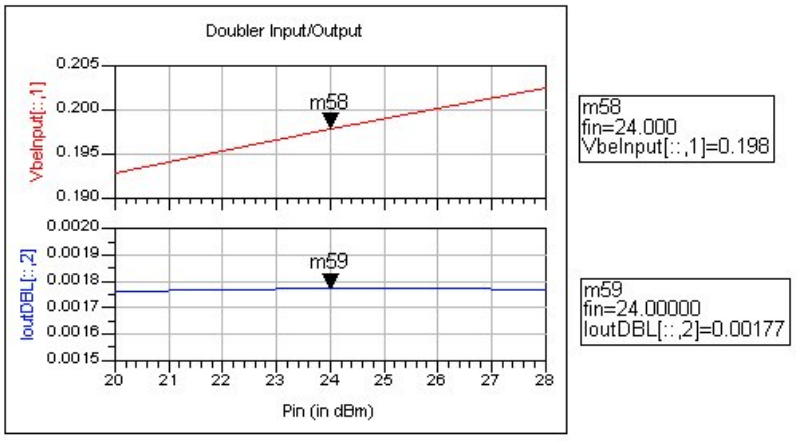

Fig 2.11 Typical input voltage and output current vs. frequency sweep

A large R_{dg} kills more gain at lower frequency so that it pushes the peak of output current to higher frequency. But too large R_{dg} also soften the input voltage swing on the base-emitter junction of the input transistors, especially the negative peak becomes less negative, so the transistors are not effectively turned off during part of the cycle. As a result, the conduction angle increases and the desired 2nd harmonic usually decrease under the bias and input power of choice mentioned before. As shown in Fig 2.11, R_{dg} and C_{dg} are chosen to result a flat response within the band of interest. In the actual multiplier chain, in order to compensate the gain drop from other stages, mainly from the active balun, in some stages the combination of R_{dg} and C_{dg} is even chosen to given an increasing output current vs. frequency. But on top of increasing the conduction angle, over degeneration at lower frequency may even deform the current pulse and generate much more unwanted harmonics in the output. So, a trade off must be made between the amount of peaking from the doubler and its output spectrum purity. Depending on the position of the doubler in the whole chain, different performance is emphasized. For instance, the harmonics from the 1st doubler have a strong impact on the strength of closeby spurs in later stages. So the first stage is optimized more towards low 4th order harmonic. On the other hand, because the active balun following the 2nd doubler shows more drop over a wider bandwidth, the 2nd doubler is optimized to provide more gain peaking.

Cascode

The cascode transistor provides a low impedance load to the differential pair and senses their output current. The reduced voltage swing at the collector of the differential pair means several advantages. First, the differential pair is less likely to enter saturation region. Second, Miller effect of the differential pair is mitigated. Third, the load only sees the capacitive parasitic from the cascade device as opposed to that of two transistors otherwise, which benefits frequency response. And finally, possibility of instability due to feedback of harmonic signal from the output is minimized.

2.2.2 Drive Conditions

2.2.2.1 Gain Compression

Fig 2.12 shows the typical input fundamental voltage and output 2nd harmonic current component during an input signal power sweep. It is shown that the output current first increases, then shows a peak and drops finally. The plot reveals an important condition of frequency multiplier operation: the choice of input power.

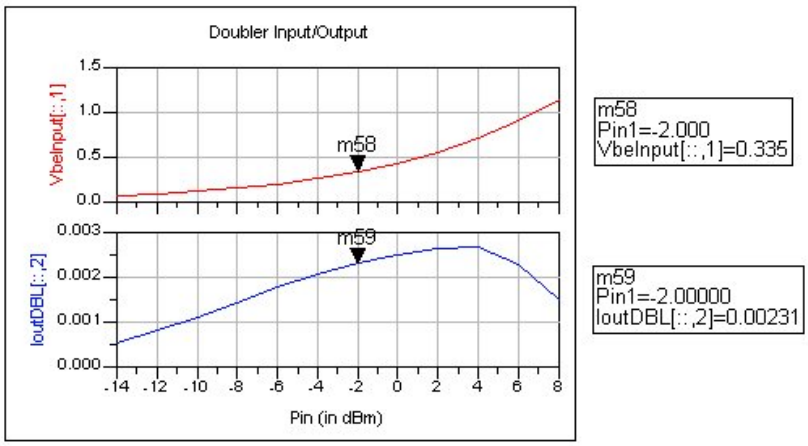

Fig 2.12 Typical input voltage and output 2nd harmonic current vs. input power sweep

Frequency multiplying can be explained as multiplying two input signals. As a result, the output power has a nonlinear relation to the input power. For an Nth order multiplier working in small signal regime, 1dB input power change induces N dB output power change. The doubler should operate under certain condition to reduce the sensitivity of output power on input power. This is generally called gain compression. The mathematical derivation is deferred to related sections in Chapter 3. Here we try to explain this phenomenon by looking at the current waveforms.

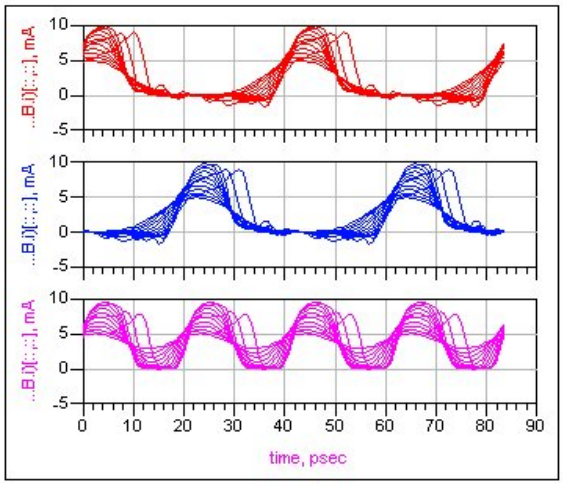

Fig 2.13 Typical current wave form of a balanced doubler during a power sweep

Fig 2.13 shows the typical current wave form of a balanced doubler during a power sweep. The top two are the collector current waveforms from the differential pair. The lower one is the collector current from the cascode device. When the input power increases, the conduction angle of the two input transistors decreases, so that the combined pulse train at the output increases its amplitude. Because of the soft turn-on characteristic of the transistor, the bottom side of this pulse train is quite curvy at first, which contains less higher-order harmonics. As the input power keeps increasing, the conduction angle decreases to a point where the soft turn-on could no longer shape a round bottom to the combined pulse train, and the transition

near turn-on point becomes more abrupt. Under this condition, the second harmonic in the waveform increases slower and finally drops, when the collector current pulse deforms from approximately half cosine wave. Before this deformation happens, there is an input power range where the output current increases slower than the increment of the input power, which shows the effect of gain compression. Gain compression proves to be the desired operation region for a frequency multiplier, for both a stable gain and for reducing the output AM noise through limiting effect.

2.2.2.2 Optimum Drive Point

Fig 2.14 shows the output harmonic of a doubler during a frequency sweep and an input power sweep. During the frequency sweep, the 2nd harmonic output current of the doubler varies little on log scale(dBm). Since the output waveform is maintained almost the same across the frequency range, the unwanted harmonics also remain quite constant. This doubler is excited with a single-tone fully differential source, so that in the output the odd-order harmonics are cancelled ideally, which appear to be below -300 dBm, only higher even-order harmonics exist as unwanted terms. During the power sweep shown in Fig 2.14 (b)**,** in the input power range of 10dBm from -6dBm to +4dBm, the 2nd harmonic output current increases by about 3.6dB. This illustrates the gain compression region. Looking at the 4th harmonic, there is an apparent dip around -4 dBm. This is the optimum driving point to minimize the 4th harmonic. It lies in the gain compression region while not requiring an excessively large input power, which makes driving the doubler near this point quite feasible.

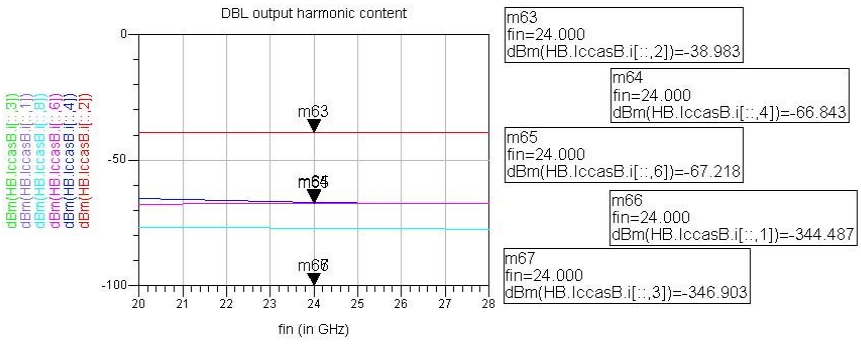

Fig 2.14 (a) Doubler output current harmonic contents during a frequency sweep, Pin=-6dBm

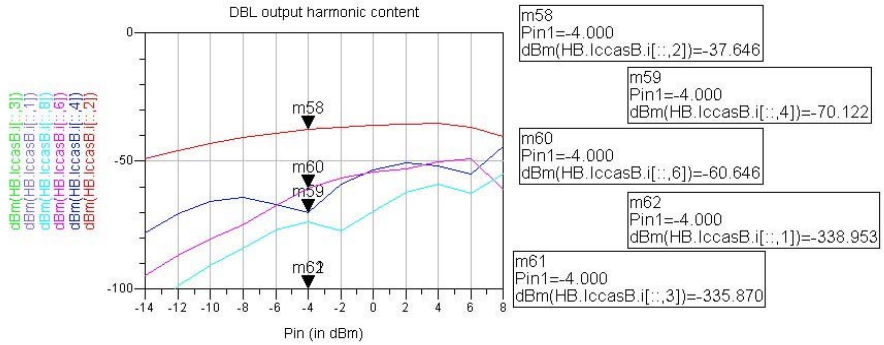

Fig 2.14 (b) Doubler output current harmonic contents during a power sweep, fin=24GHz

2.2.2.3 Ideal Source vs. Drive Amplifier

Notice that in the above simulations, the input signal is taken from a power source that can provide arbitrary high input power. E.g. when input power is +6dBm, the fundamental voltage swing on input BE junction is about 0.9V. In reality, the buffer preceding the doubler may not be able to provide such large voltage swing partly due to headroom limitation. So the input voltage would already compress much earlier before reaching the peak output point determined by the doubler itself. From Fig 2.12 we observe that the doubler begins to enter the gain compression region with an input voltage swing of about 300mV.

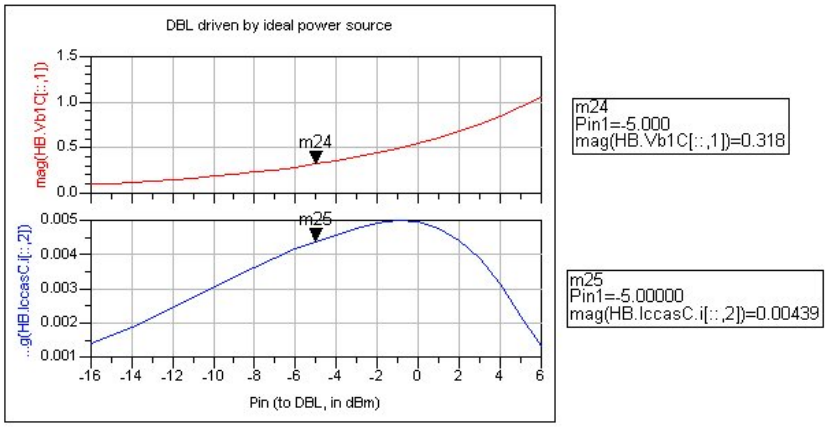

Fig 2.15 (a) Doubler input and ouput during a power sweep with an ideal power source

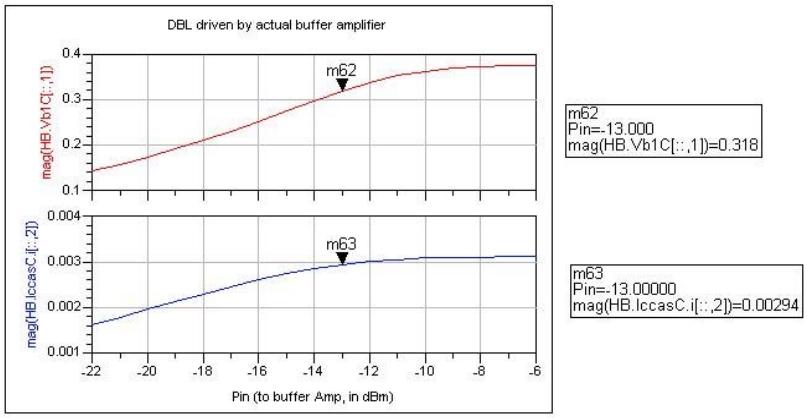

Fig 2.15 (b) Doubler input and output during a power sweep with an actual buffer amplifier

Fig 2.15 (a) and (b) shows the input voltage and output current variation of a doubler driven by a power source and a buffer amplifier respectively during power sweep. The impedance of the ideal source is chosen close to the value of the output impedance of the buffer amplifier. The horizontal axes bear the overall input power for the two cases. With the presence of a buffer amplifier in the case of Fig 2.15(b), the two cases can not be compared for the input power value. The input fundamental voltage term serves as the standard for a fair comparison.

We choose 318mV as a comparison point. The output current from the source driven doubler is 4.39mA while the current from the amplifier driven doubler is 2.94mA. Although the actual amplifier reduces the output current, it still gives gain compression. Actually, the output 2nd harmonic current stays constant for a large range of input power. The reduced output power can be recovered by scaling up the doubler.

The harmonic contents of the output current in the two cases are compared in Fig 2.16 (a) and (b). Except for more than 3dB of difference in the 2nd harmonic, difference exists among all the other harmonics. The buffer driven doubler does not necessarily produce higher unwanted harmonics at all the related frequencies, such as the 6th and 8th harmonic. But it generates 4db higher 4th harmonic, so the ratio between the 2nd harmonic output and the 4th harmonic reduces from about 22dB to 15dB, which means the influence of high-order nonlinearity is magnified.

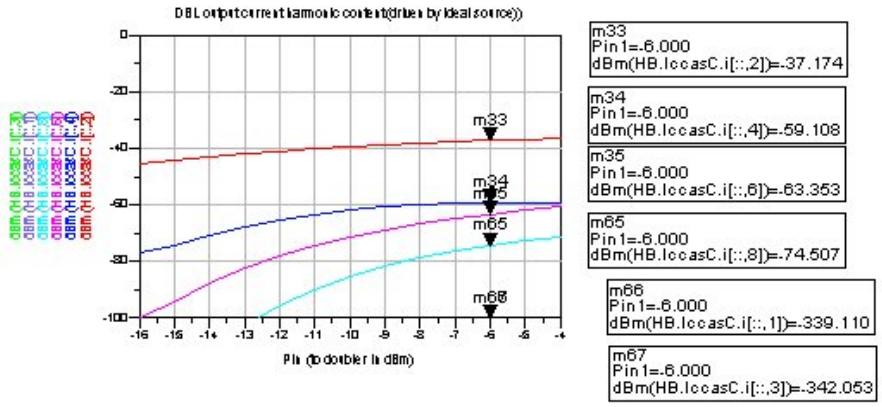

Fig 2.16 (a) harmonics in doubler output current during a power sweep with ideal source

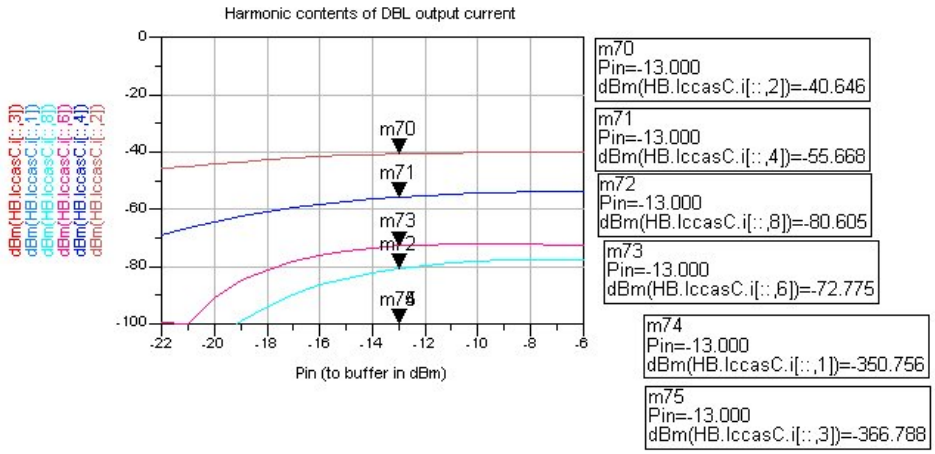

Fig 2.16 (b) harmonics in doubler output current during a power sweep with buffer

2.2.2.4 Balanced and Unbalanced Drive

The influence of buffer amplifier to the doubler operation makes one wonder how exactly input signal causes these differences in the output current. The starting point of the investigation is simulation with an idealized single tone power source. Actually two identical power sources are connected in series. On the two terminals, we have signal of equal amplitude and 180 degree phase difference. Since this drive signal is fully differential, we say doubler is under DM(differential) drive. The input voltage and output current spectrums are shown in Fig 2.17. As expected, the combined output current looks like a fullwave rectified sinusoidal. All the odd order harmonics and the fundamental are negligibly low (more than 300dB lower). The higher even order harmonics are at least about 25dB lower than the 2nd harmonic output.

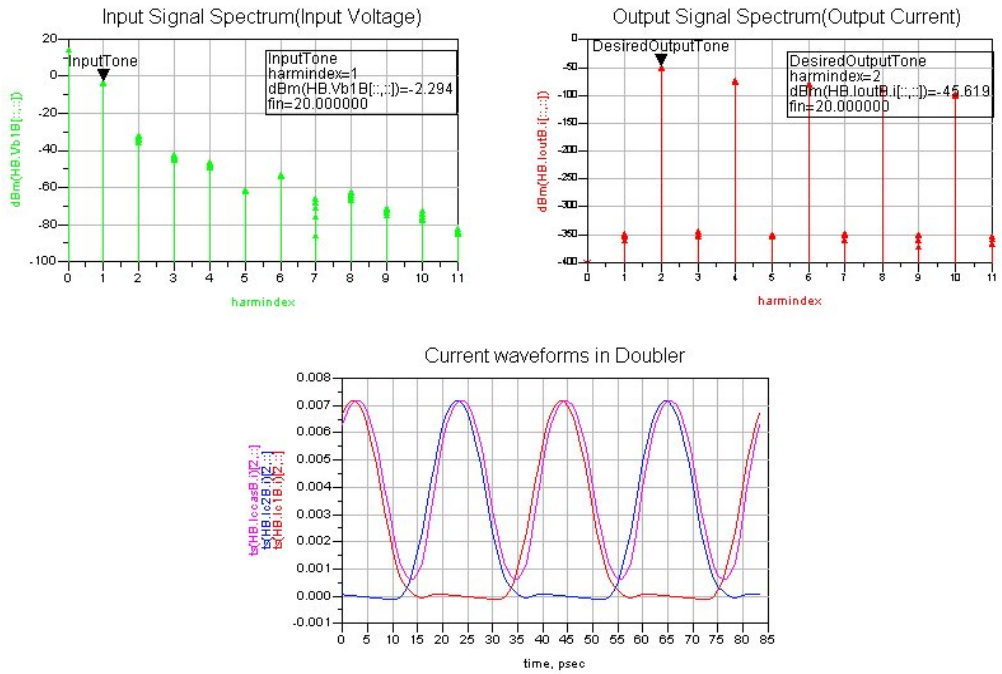

Fig 2.17 Doubler input voltage and output current under balanced drive

Fig 2.18 shows the situation where the two input of a doubler is intentional driven by signals of 0.3dB amplitude difference and 177 degrees phase difference. These figures may seem quite close to a balanced signal, but the output spectrum of the doubler will be changed a lot. Odd order harmonics will not be cancelled ideally in the output current. As will be explained in the next chapter, they can cause big trouble to the spectrum purity of a multiplier chain.

Similar problem also arises when multi-tone excites the input of a doubler. In a multiplier chain, these unwanted tones could come from harmonic components from the output of the preceding doubler. Further analysis about unbalanced drive and multi-tone excitation of a doubler can be found in Appendix B.

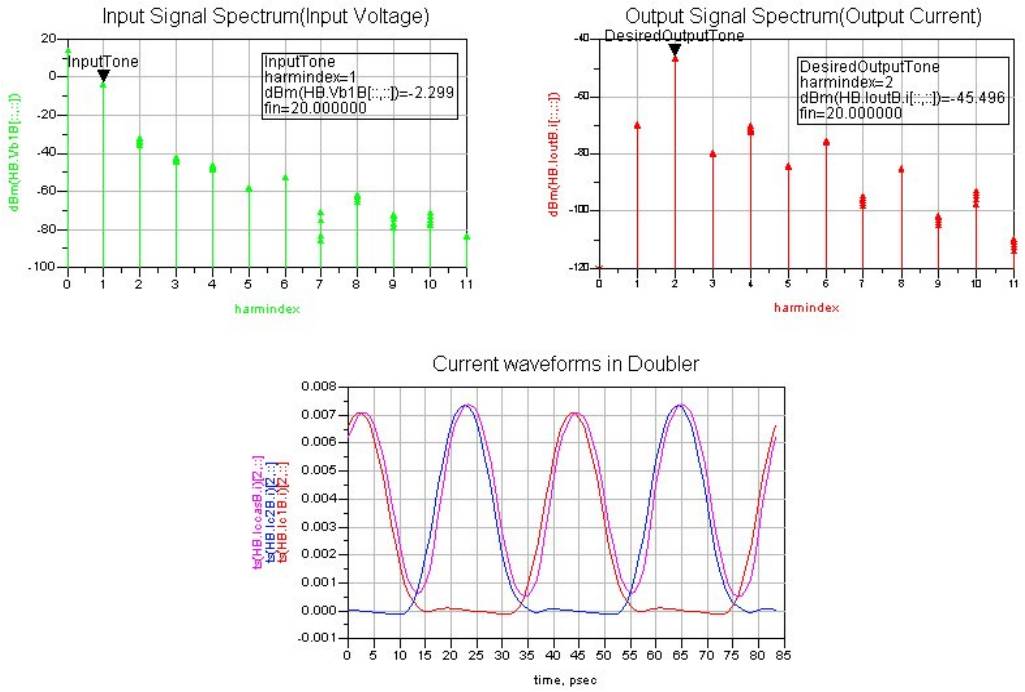

Fig 2.18 Doubler input voltage and output current under slightly unbalanced drive(0.3dB amplitude unbalance and 3 degree of phase unbalance)

2.2.3 Conclusion

From the above analysis, we can generalize a set of rules concerning the balanced frequency doubler and its buffer amplifier.

In order to operate the doubler in gain compression, its buffer amplifier should provide large enough output voltage swing. The nonlinearity, represented by the harmonic tones generated by the buffer amplifier should be kept as low as possible. Strong nonlinearities cause by current clipping or saturation should be avoided. The balance of input signals to the doubler determines how well odd order harmonics can be cancelled as intended by anti-series connection of two transistors. As a result, the common-mode rejection from the buffer should be emphasized. Considering that the actual circuit may operate over an input power range, it would not be realistic to keep the conduction angle, which is directly related to the input power, always at the same point. So, no excess effort is made to operate the doubler at the exact the input power level where the 4^{th} harmonic in the output current is minimized. However, just by applying large enough input power, the conduction angle is already not too far away from the optimum point in terms of 4^{th} harmonic suppression.

2.3 Summary

In the first part of this chapter, the theory and examples of various frequency multipliers are reviewed. Some key points are noted, such as the relation between input power, signal wave form and harmonic content. The second part presents the design considerations of a balanced frequency doubler that will be used in the multiplier chain. Its performance with respect to different driving condition is discussed in detail.

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Chapter 3 Multiply by 8 Chain

3.1 System Level Considerations

In our phased array system [1] implementation, each slotted antenna, which comprises a row of radiation elements, has its own time/phase delay control and frequency up-conversion block. The up-conversion chain converts the low-frequency chirp signal (FMCW signal) up to W band (around 94GHz). At the output side, this up-converted signal is then fed to the transmitter antenna, as well as, the LO port of down conversion mixer. Fig 3.1 gives the block diagram of the phased array system. Only one antenna is shown.

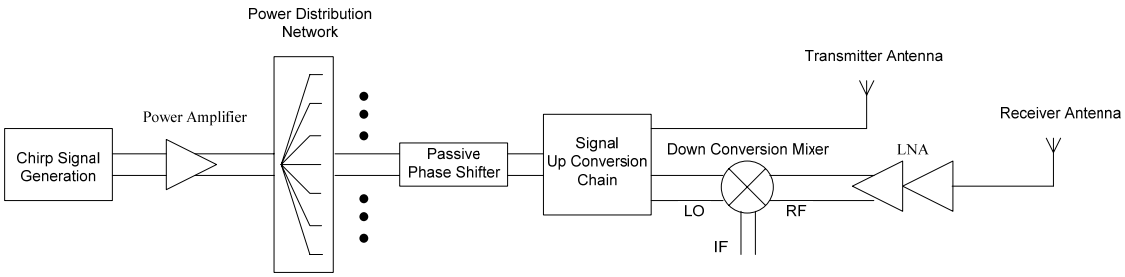


Fig 3.1 Block diagram of the phase array system

3.1.1 Bandwidth Requirement

In terms of driving a phased array with frequency scanning antennas, the RF operating bandwidth is mainly determined by the bandwidth requirement for steering the beam directionn. Simulation of the intended frequency scanning antennas shows that frequency sweep from 88GHz to 104GHz can result in +/-30 degree beam angular sweep range from a single antenna [2].

According to the FMCW principle, wider chirp bandwidth allows higher range resolution [3]. This requirement alone wouldn't be a trouble for base band DDS signal generation. In practice chirp bandwidth is set by the low frequency chirp generator. Probably it would still be difficult to generate the FMCW signal with DDS directly at the input frequency of our frequency multiplier chain. Some additional frequency up-conversion is required at lower frequency. It is quite popular to use a PLL for this purpose. However, as a close loop system, PLL shows a certain bandwidth of following its input signal quickly. Demand of fast frequency chirp sweeping can cause the PLL not able to follow its input frequency, thus introducing distortion to the frequency sweep.

Comparing the above bandwidth requirements，the bandwidth of the frequency up-converter is mainly set by the requirements of the frequency scanning antenna.

The frequency up-converter mainly affects the output signal in three ways. First, the frequency dependant gain of the up-conversion chain limits the practical bandwidth. Second, unwanted spurs generated during the up-conversion process affects spectrum purity. Nearby spurs would give rise to unwanted antenna beams pointing at directions other than the main lob. For narrow band frequency multiplication systems, harmonic termination around each multiplier stage can be used to suppress these unwanted spurs. It is generally more difficult to guarantee low unwanted spurs over wide bandwidth. So, also unwanted spurs can limit the useful bandwidth of the system. In this design, we try to reduce all nearby spurs to more than 40dB lower than the desired output signal. The nearby spurs are defined as those spurs that may appear in the bandwidth of the antenna. Third, noise sources within the up-converter contribute to the excessive phase noise to the output signal. As will be explained later in this chapter, LO phase noise can cause series problem in a continuous wave radar system.

By designing an up-conversion chain producing a flat intended output harmonic over the band, as well as, less unwanted spurs within the bandwidth of the antenna, we grant the radar system with a better opportunity to use a wider bandwidth, resulting in a better range and angle resolution. We set our band of interest from 80GHz to 112GHz, resulting in a center frequency of 96GHz with a relative bandwidth of 33.3%. Previous simulation of the frequency scanning antenna shows about +/- 75 degrees of corresponding beam stir range.

3.1.2 Power Requirement

The power required by the transmitter antenna is higher than the power required by the LO port of the mixer. We will discuss the power delivered to the antenna first. According to the fundamental radar theory [4], the maximum range over which a radar can detect an object is related to its transmit power (3.1).

$$R_{\max} = \left(\frac{P_t G A_e \sigma}{(4\pi)^2 S_{\min}} \right)^{1/4} \tag{3.1}$$

The quadratic root relation between Rmax, the maximum detection range, and Pt, the transmitter power means the detection range reduces quickly with reduced transmitter power. Since our application is mainly short range. The required transmit power is relatively low. The phased array concept offers for the transmitter the advantage of combining the signals from each antenna element and focusing the power to a certain direction, the effect is reflected in higher antenna gain. For the receiver in a phased array the reflected signals are combined constructively to improve the received SNR which improves the detection. [5].

Even with advanced silicon-based MMIC technology, it is difficult to provide high gain or high power at millimeter wave frequencies. The power handling / speed trade-off of active device poses the major limitation. Based on the system application and initial simulations we aim for a transmit power of 5dBm per each roll of transmit antenna.

The power delivered to the mixer LO port should be high enough to switch the switching quad of the mixer effectively. In previous mixer simulation [6], the peak-voltage swing at one end of the differential LO port is chosen to be 150mV. The LO driver, also part of this circuit, should generate at least this voltage swing across the band of interest. The real power delivered to one-end of the differential LO port is calculated to be about -2dBm at 96GHz.

At the input of the up-conversion chain, the available input power is determined by the preceding circuit blocks. For the demonstration system at around 94GHz, about 40 slotted antennas are planned to put in parallel. Each of them has its own phase shifter and frequency up-conversion block, but their input power comes from a single frequency chirp source. The generated chirp signal is divided into 40 channels by a passive power distribution network. 1/40 power means -16dB gain in the signal path. The estimated insertion loss from the passive phase shifter is about 4dB. Another 10dB loss is budgeted for dissipation from the power distribution network and other potential circuit blocks before the up-conversion chain. In total -30dB gain is budgeted from the input of the power distribution network to the input of the signal up-conversion block. A power amplifier amplifies the output signal from the chirp generator to drive the power distribution network. Above 10dBm of output power is expected from that power amplifier. From these assumptions, we set the nominal input power of the signal up-conversion chain to be -20dBm.

Besides, in order to take into account possible loss along signal path or other variations, the up-conversion chain should be able to operate over an input power range and still deliver comparable performance. This is partly achieved by operating each multiplier into gain compression.

3.1.3 Multiplication Factor

Frequency multiplication is also a bandwidth expansion. The bandwidth of signal referred to the input of the up-conversion chain equals to the required bandwidth at the output divided by the multiplication factor. Higher multiplication factor brings down the input signal frequency band and reduces its bandwidth. These are favorable conditions for the DDS chirp generator. But for the frequency multiplier itself, higher-order multiplication makes it more difficult to achieve the wide bandwidth intended. Besides, the power consumption for frequency up-conversion is comparatively high. Although when the output frequency range is decided, increased multiplication factor means additional stage at lower frequency, the added power consumption is still a factor to consider.

Considering the requirement on the chirp generator and that on the up-conversion chain, multiplication factor close to 10 is initially decided. Later the multiplication factor is set to be 8 mainly because of the requirement on the nearby harmonic suppression. Since the frequency doubler discussed in detail in chapter 2 shows the potential of wideband operation, as well as, harmonic suppression, we intend to construct the up-conversion chain with several of these frequency doublers in cascade. Considering the bandwidth requirement, 3 of such doublers are put in cascade to build an up-conversion chain with multiplication factor of 8.The resulting input signal band is from 10GHz to 14GHz. Fig 3.2 shows the frequency planning of

up conversion chain.

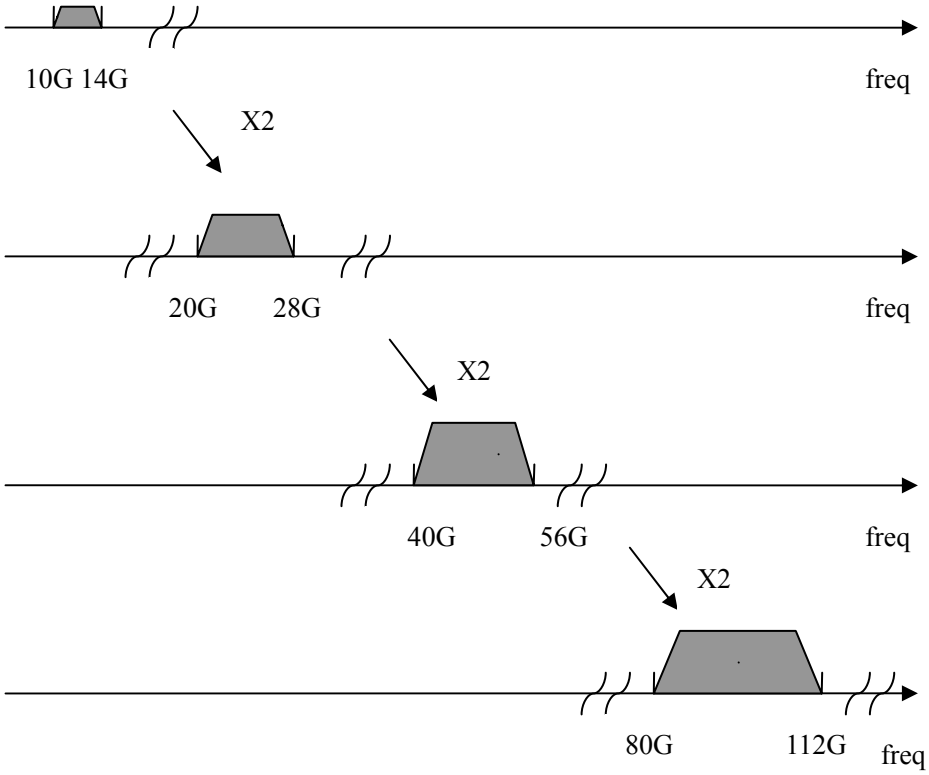


Fig 3.2 frequency planning of the multiplier chain

3.1.4 Terminal Requirement

The input of the up-conversion chain loads the passive phase shifter, which needs good termination impedance. Here we assume 50 Ohm termination impedance at the input. Since the phase shifter we use is differential, the input signal to the up-conversion chain is also a differential signal. Two output signals are expected at the output, one to feed the transmitter antenna, the other drives the LO port of the down conversion mixer. The respective terminal requirements are set by these loads. The transmitter antenna requires a single-end drive signal while the LO port of the double balanced mixer requires a differential signal. The above mentioned performance requirements of the multiplier chain are summarized in Table 3.1.

Table 3.1 Some Requirements on the Up-conversion Chain

Performance Term	Requirement
Input signal power	About -20dBm
Input signal band	10GHz to 14GHz
Input port and its port impedance	Differential, matched to 100 Ohm
Multiplication factor	8
Output signal band	80GHz to 112GHz
Output signal power to transmitter antenna	About 5dBm
Output port to transmitter antenna	Single-ended, matched to 50 Ohm
Output signal power to mixer LO	High enough ~ -2 dBm
Output port to mixer LO	Differential, no matching needed
Output signal unwanted spur suppression	Better than 40dB

3.1.5 Functional Division

The whole circuit can be divided into two parts based on their function. As is shown in Fig 3.3, the first part is denoted “multiply by 8 chain”, which mainly converts the signal upconversion from around 12GHz (in X and Ku band) to around 96GHz (in W band). The second part gives enough amplification to this up-converted signal and produce the two drive signals for the transmitter antenna and the LO port. It is denoted as “W band gain blocks”. Whether the connection between these two parts is single-ended or differential is to be decided during the actual circuit design. The single line connection drawn in the plot is only an indication for now. This chapter mainly discusses the design consideration and simulation results of the multiply by 8 chain. The second part will be discussed in the next chapter.

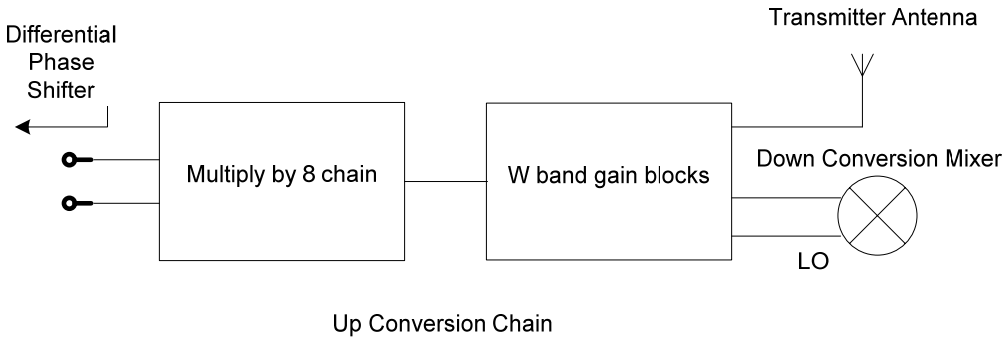


Fig 3.3 Functional division of the signal up-conversion chain

3.2 Multiply by 8 Chain

The choice for a multiply by 8 chain is mainly based on the potential of good performance from the frequency doubler studied in chapter 2. Three doublers bases on this topology will be connected in cascade with buffers and other necessary circuit blocks in between to build the multiply by 8 chain. Before we present the final implementation of the multiply by 8 chain with doublers, buffers, baluns and filters, we need first to expose the problems involved and explain our solutions. Frequency planning will be discussed afterwards.

3.2.1 Circuit Between Two Doublers

Our first trial was to connect two doublers together. Since the doubler has differential input and single-end output, there should be a circuit block to convert the single-end output signal from a doubler stage to a differential input for the next stage. Besides, the doubler should be driven hard enough into gain compression to reduce the output power sensitivity to its input power. Although one doubler stage can be scaled up to deliver higher output power, its output is not high enhough to give sufficient voltage swing to the input of the next doubler over a large bandwidth. The capacitive input impedance of the next doubler adds considerable frequency dependant loading to the preceding doubler. Hence, a buffer should be inserted between two doublers to provide enough drive power for the second stage, as well as, proper impedance transformation to lower the loading of the first stage. As first step an ideal balun

preceded by an ideal amplifier is inserted between two doublers. Both these blocks show no frequency dependency. The gain of the amplifier is adjusted to drive the 2nd doubler into gain compression. Block diagram of this circuit is plotted in Fig 3.4.

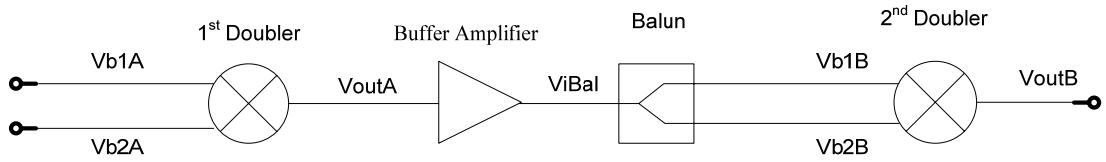


Fig 3.4 Block diagram of two doublers connected with ideal buffer and balun

The topology of the frequency doubler and the notations of signal voltage and current are plotted in Fig 3.5 again for ease of reference. The input voltage waveform and the collector current waveforms from the transistors in two doublers are plotted in Fig 3.6.

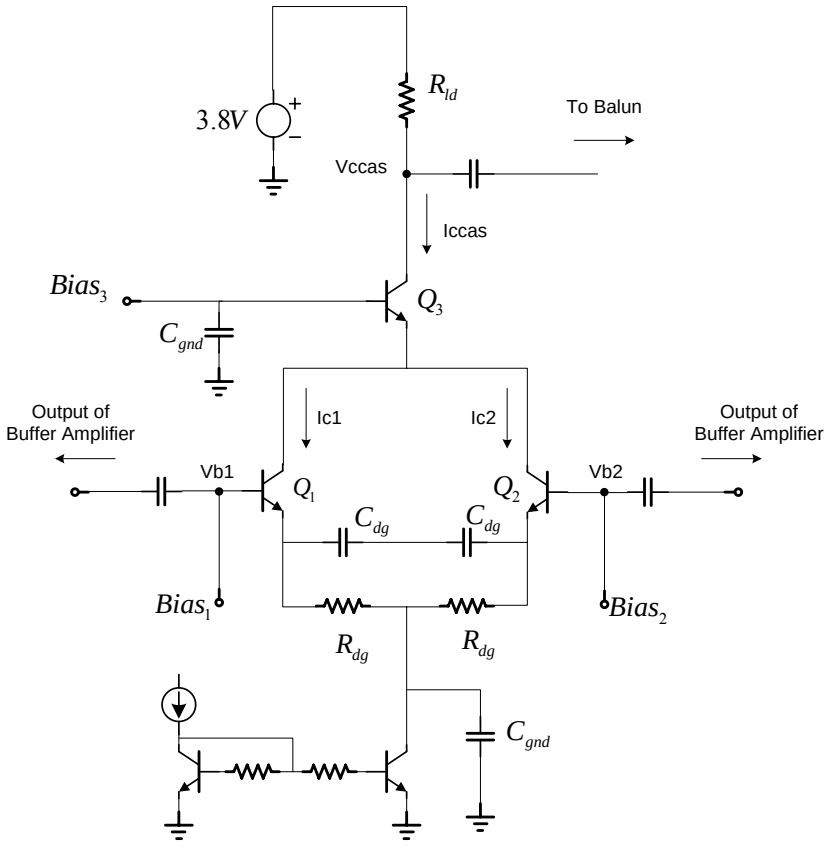


Fig 3.5 Circuit topology of the balanced doubler

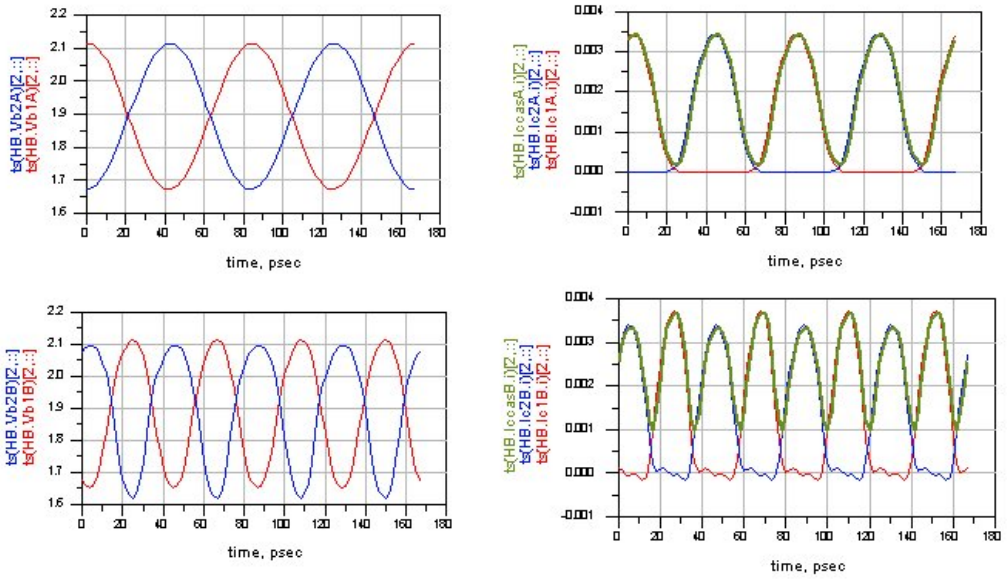


Fig 3.6 Waveform of input voltages and the collector currents from the transistors in two doublers, test circuit topology is shown in Fig 3.4

The problem is presented in Fig 3.6 quite clearly. The output voltage waveform of the 2nd doubler shows strong distortion. This is because the input voltage to the 2nd doubler is not differential single tone signal but the distorted output of the first doubler. As was discussed in Chapter 2, any amplitude and/or phase unbalance, or harmonic contents present in the two input signals of the doubler affects the ideal operation of this doubler. Unwanted spur contents will then be generated in the output current of this second doubler. When plotted as time domain waveform, this distortion shows up accordingly. Fig 3.7 illustrates this finding with signal spectrum at the input and output of the 2nd doubler. Comparison between two input signal nodes reveals that distorted and unbalanced drive introduces considerable distortion to the output signal.

One point worth mentioning is that the input to the first doubler is taken from a pure single-tone fully differential signal source. Consequently, the first doubler operates ideal and all the odd order harmonics are cancelled in its output current. Consequently, we do not observe any odd-order harmonics in subsequent stages.

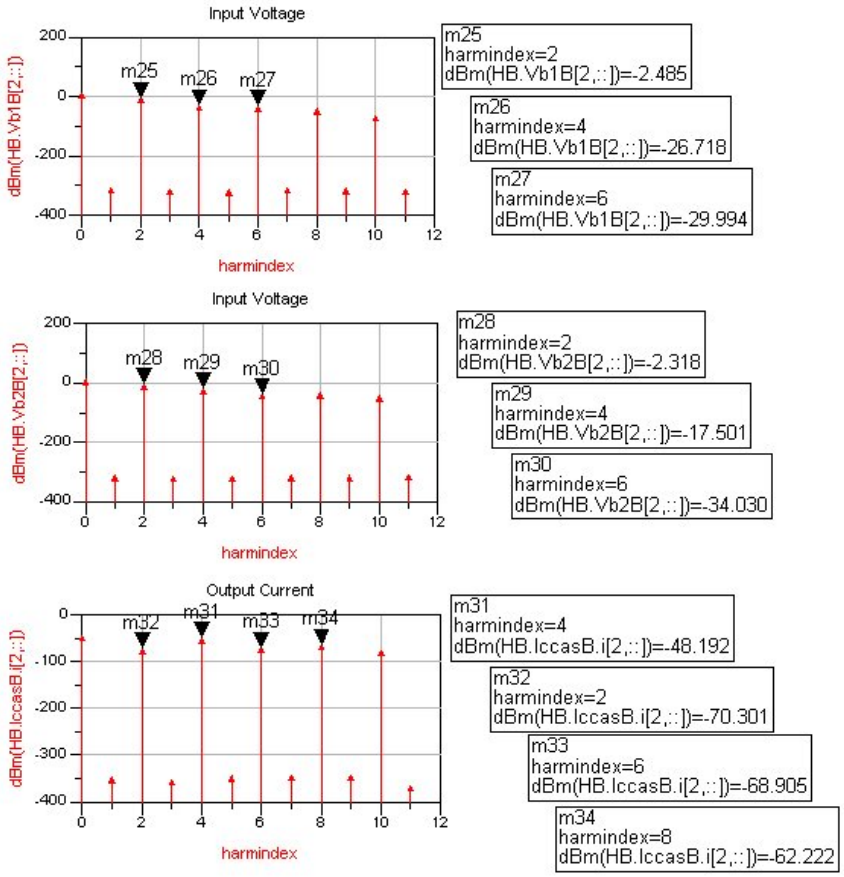


Fig 3.7 Harmonic contents of input voltages and the output current in the 2nd doubler, test circuit topology is shown in Fig 3.4

To correct the unbalance in the drive signal of the second doubler and to suppress the unwanted harmonics in its input, a band pass filter is inserted between the buffer amplifier and the balun as shown in Fig 3.8. The stop band of the filter is set to give at least 25dB attenuation to nearest even order unwanted harmonic.

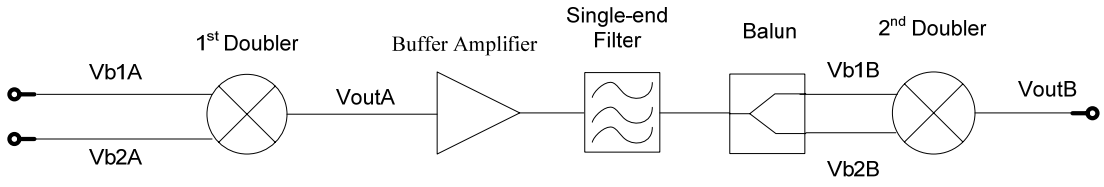


Fig 3.8 Block diagram of two doublers connected with ideal buffer, bandpass filter and a balun

The resulting voltage and current wave forms are plotted in Fig 3.9. This time, the input voltage signals to the 2nd doubler is much more symmetrical. At least we wouldn't observe apparent difference in their wave forms, also the output current of the 2nd doubler looks also much more like a sine wave.

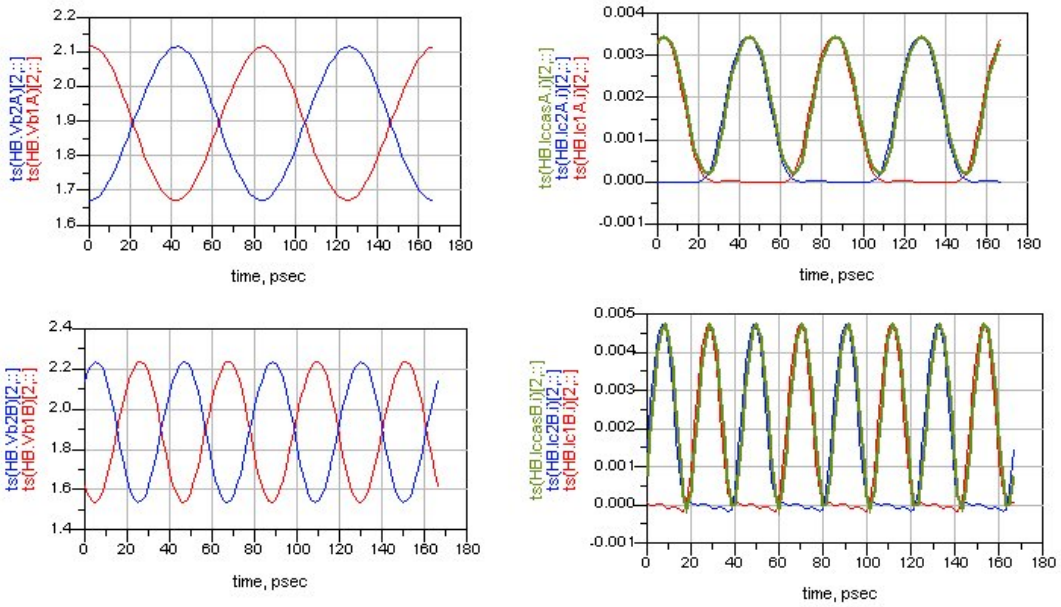


Fig 3.9 Waveform of input voltages and the collector currents from the transistors in the two doublers when interstage filtering is implemented, the test circuit topology is shown in Fig 3.8

The spectral components give a more quantitative view. The input voltage and output current spectrum contents of the 2nd doubler are plotted in Fig 3.10. Note that now much less difference between the input signals exist at desired frequency (harmonic index 2). Component at nearby unwanted harmonics (harmonic index 4) are also much closer to each other. This indicate that the input voltage waveforms of the 2nd doubler are now more balanced than those shown in Fig 3.6. Comparing the harmonic contents of the output currents in Fig 3.7 and Fig 3.10, we see that the nearby even order unwanted harmonics in the output current of the 2nd doubler (harmonic index 2 and 6) are about 20dB lower due to the use of the band pass filter.

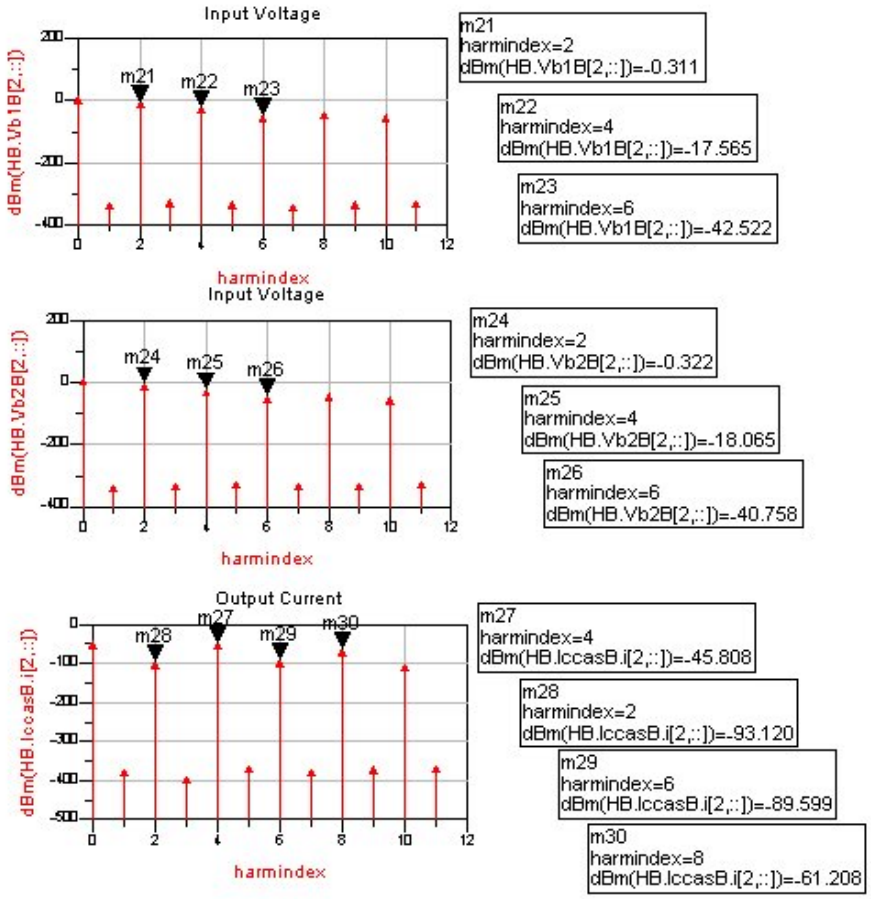


Fig 3.10 Harmonic contents of input voltages and the output current in the 2nd doubler when inter-stage filtering is implemented, the test circuit topology is shown in Fig 3.6

The above comparison shows that filtering between the two doublers cleans up the spectrum and keeps the doubler performance close to ideal. In the aimed implementation of the multiplier chain, the balun is connected directly after a doubler followed by a differential filter and buffer amplifier. The block diagram is shown in Fig 3.11. The circuit blocks between the 1st and 2nd doublers as well as those between the 2nd and 3rd doublers make use of this topology. Since the input signal to the up-conversion chain is differential, there is no need for a balun at the input. Depending on the spectrum purity of the overall input signal, it may be necessary to put a band pass filter before the first doubler. But considering the large size of such a passive component at lower frequencies, on chip implementation is not desired.

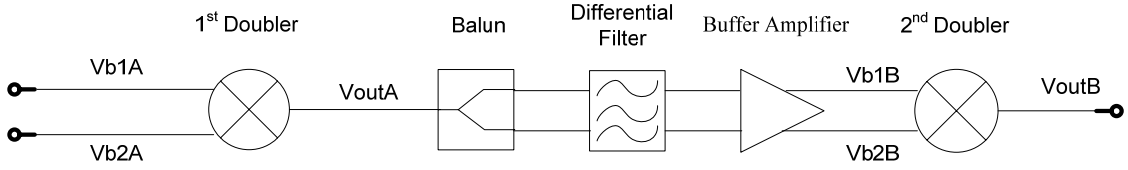


Fig 3.11 Block diagram of two doublers connected with a balun, differential band pass filter and differential buffer

3.2.2 Sub Stage Division

As already mentioned in Chapter 2, the performance of a doubler is closely related to the buffer amplifier that precedes it. The balun loads the single-end output port of the doubler, so it should be designed together with the doubler. Fig 3.12 shows the block diagram of the multiply by 8 chain, consisting of 3 doublers as well buffers, baluns, and filters. The operation frequency band of respective circuit blocks are labeled on the plot. Each doubler operates across two frequency bands.

Separated by two bandpass filters, this multiplier chain can be subdivided into three active circuit stages which are named Stage A,B and C. Each stage up-converts its input signal frequency by a factor of two. Stage A and B consists of a doubler, its buffer amplifer and the balun. Stage C connects to the circuit blocks operating on W band and does not include an active balun. This division is mainly for the easy of characterization. Since the external ports of these stages interface well defined passive structures like phase shifter or filters, it is easier to define the driving and loading conditions to them.

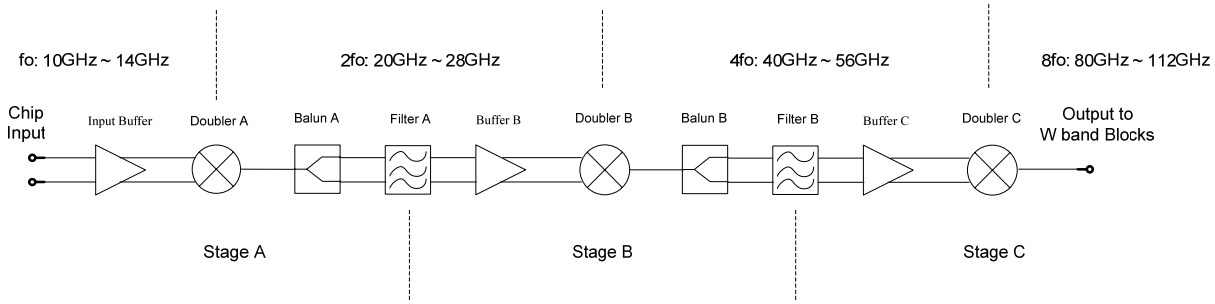


Fig 3.12 block diagram of the multiply by 8 chain

3.2.3 Unwanted Spur Generation

In the previous sections, we have seen the effect of frequency domain filtering between two doublers. There, we set the pass band and stop band specifications of the band pass filter without explanation. In this section, we will look into how unwanted spurs are generated in this multiplier chain, from which we can derive the specification of the filters.

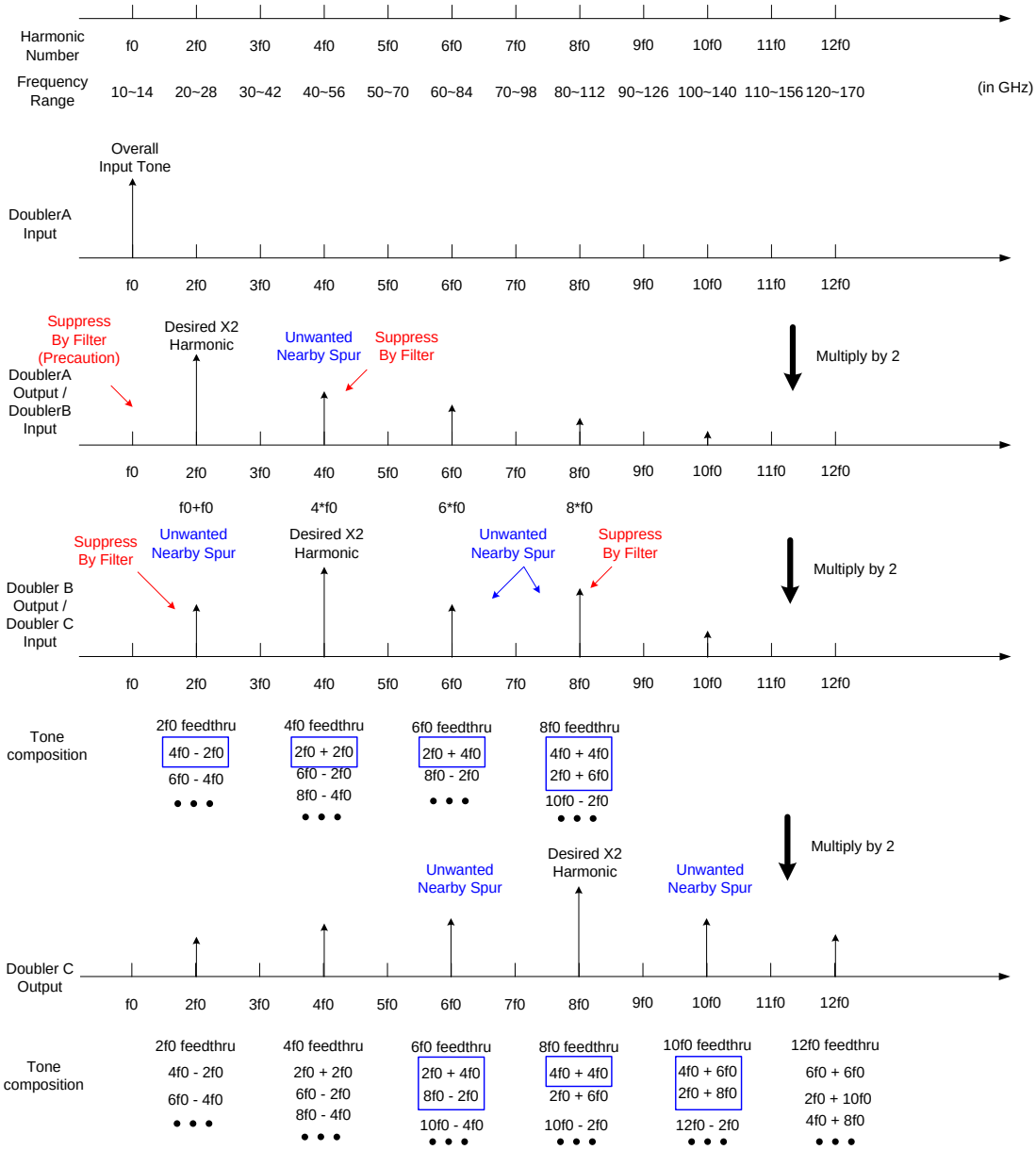


Fig 3.13 Tone generation through the multiply by 8 chain

Fig 3.13 shows how the desired harmonics and unwanted spurs are generated through the multiply by 8 chain. The topmost axis shows the harmonic numbers as well as the frequency band they may appear in. The input signal is labeled as f0, which occupies frequency range from 10GHz to 14GHz. The axis below shows the signal spectrum at the input and output of each frequency doubler in the multiply by 8 chain. It is assumed that the buffers between the doublers are linear, and they do not generate any spurs by their own. It is also assumed that the nonlinearity introduced by the input loop of a frequency doubler is low enough, so that the spectrum at the input of a doubler is the same as the spectrum at the output of the preceding doubler. At the overall input, we assume a pure single-tone sinusoidal excitation at f0 and no other harmonic components, as is shown in the 2nd axis from the top. The first doubler is assumed to operate ideally so that all the odd order harmonic contents are cancelled and only Even order harmonics are generated, as is shown in the 3rd axis from the top. The 2nd and 3rd

doubler does not share this assumption because considerable unwanted tones appear at their input.

Since frequency multiplication expands the signal bandwidth, there are more overlaps of band between nearby tones with higher harmonic numbers. For example, 8f0 occupies the band from 80GHz to 112GHz. Bands of 6f0, 7f0, 9f0 and 10f0 all have partial overlap with that frequency range. This means that if spurs on these harmonics are generated, part of them will also appear in the pass band of the antenna transfer function and can cause higher side lobes in the radiation pattern. Spurs outside this range experiences more suppression and are normally of less concern. The goal here is too minimize these nearby inband unwanted spurs.

Remember from the discussion about doubler performance in Chapter 2, that it shows only even order nonlinearity to a purely differential single-tone input. When excited with common mode signal, there will be fundamental tone feed through, together with all odd order harmonics generated at the output. In reality, the output of a frequency doubler would contain both even and odd order mixing products due to not ideal input signal.

In order to suppress odd order nonlinearity, the actual input signal to a doubler will be kept as balanced as possible. Hence the strength of common mode input signal is normally much lower than the differential mode input signal. Simulations show that the presence of low strength common mode signal does not affect the differential response of the doubler significantly. On the other hand, the large differential mode input signal alters the operating point of the doubler. Consequently, the common mode response will be affected by the differential input, there is correlation between common mode transfer and differential mode input signal. Nevertheless, since the strength of output signal components due to common mode input is much weaker, those components can be modeled as additive perturbation without losing validity in our circuit scenario.

The transfer function toward differential mode input and common mode input can be described with two power series. Note that both transfer functions embody the influence of large differential mode input signal implicitly by incorporating signal dependant nonlinearity coefficients $a_1(x_{dm})$, $a_2(x_{dm})$, $a_3(x_{dm})$,….and $b_1(x_{dm})$, $b_2(x_{dm})$, $b_3(x_{dm})$,….

$$y_{dm,input} = a_2 x_{dm}{}^2 + a_4 x_{dm}{}^4 + \cdots \tag{3.2}$$

$$y_{cm,input} = b_1 x_{cm} + b_2 x_{cm}{}^2 + b_3 x_{cm}{}^3 + b_4 x_{cm}{}^4 + \cdots \tag{3.3}$$

The overall transfer function can now be described by their sum,

$$y_{tot} = y_{dm,input} + y_{cm,input} \tag{3.4}$$

Simulation shows that the level of nonlinearity, hence the coefficients in the transfer function have the following trait. Coefficients representing the same order nonlinearity for both common mode and differential mode transfer functions have similar order of magnitude. For

example, the magnitudes of a2 and b2 are close. The values of those coefficients depend on the actual waveform of output current, which is related to the conduction angle of the transistors. With the practical conduction angle that can be achieved with reasonable input power and bias, higher-order nonlinearity coefficients are much lower than lower order ones. We take a2 and a4 as an example. Under single-tone excitation, this means that 2^{nd} harmonic generated will be much higher than the 4^{th} harmonic. Under multi-tone excitation, this means that mixing products generated through 2^{nd} order nonlinearity are much more dominant than those generated by the 4^{th} order nonlinearity. Although multiple tones appear at the input of the 2^{nd} and the 3^{rd} doubler, the model based on the above assumptions and simplifications catches the most dominant nonlinearity, the 2^{nd} order one.

Return to the spur generation mechanism shown in Fig 3.12. The output tones of a doubler are the mixing products of all its input tones. The frequencies at which the output tones may appear are the linear combinations of the input tone frequencies. We ignore the mixing product of all higher order nonlinearity and focus on those generated from 2^{nd} order nonlinearity. Looking at the bottom two axis representing the output tones from the 2^{nd} and the 3^{rd} doubler, the composition of both desired harmonic and unwanted tones are listed below. Considering the strength of the input tones, several stronger output tones are listed. The ones showing the highest magnitude are emphasized with a blue square box. For instance, in the 2^{nd} doubler (Doubler B), the desired output tone on 4f0 is generated mainly from the mixing of two tones on 2f0. So, it is listed as 2f0 + 2f0. The nearby unwanted tones locate on 2f0 and 6f0. Their major composions are 4f0-2f0 and 4f0+2f0 respectively.

Because of the bandwidth expansion effect, it is more difficult to suppress these nearby tones if possible at all, in later stages in the multiplier chain. Not to mention band overlapping that makes static filtering useless, when band spacing is narrower, filters with narrower transition band and/or higher stop band suppression should be used. This leads to higher order and more complicated filter structures which are difficult for on chip implementation at higher frequencies. Therefore the implementation difficulty of integrated filters has been taken into consideration for choosing which harmonic(s) to suppress.

The bottom axis shows the output tones of the 3^{rd} doubler, nearby spurs that may appear in band are on 6f0 and 10f0. Looking at the frequency composition, the tones on 2f0,6f0 and 8f0 at the output of the 2^{nd} doubler are the sources to these spurs. Normally speaking, after the 2^{nd} doubler is optimized by choosing the right input power and bias, the spur on 8f0 will be about 25~30dB lower than the desired harmonic on 4f0. The spurs on 2f0 and 6f0 depend on both differential and common mode transfer. As long as the unwanted input tones to the 2^{nd} doubler are not much too strong, spurs on 2f0 and 6f0 are lower than that on 8f0. 2f0 and 8f0 are at appropriate distance to the desired harmonic at 4f0 to allow filtering with reasonable complexity. But the spur on 6f0 is too close to 4f0. So, the filter at the output of the second doubler is meant to suppress the spurs lower than and including 2f0 as well as higher than and including 8f0.

The spur on 6f0 at the output of the 2^{nd} doubler remains a problem. This is partly solved with

another filter at the output of the 1st doubler. Looking at the 2nd axis from the bottom which represents the output of the 2nd doubler, we find that the unwanted spurs on 2f0, 6f0 and 8f0 stems mainly from unwanted spur on 4f0 at the output of the 1st doubler. The distance between 2f0 and 4f0 allows a relatively smooth filtering. So, at higher frequencies, the filter after the first doubler suppresses harmonics higher than and including 4f0.

In the next section we shall observe that nearby odd order harmonics generated by the 1st doubler, on f0 and 3f0, could be a serious problem to the final spectrum purity in W band. It is prudent to also design the first filter such that it also gives some suppression to signal in those frequency ranges. 3f0 is too close to the desired signal 2f0, it will not be significantly suppressed by the limited order filter. However on the lower frequency side, f0 resides at an appropriate distance. It can be suppressed by the filter.

Mixing products rising from different order of nonlinearity may enhance or partly cancel each other due to different phase relations. There are clever designs that utilize this constructively and suppress some harmonic components to a large extent. However most of those ideas involve accurate control of harmonic terminations, including some out of band ones. It is even more difficult to implement those ideas for wideband circuit. Considering the complexity and potential large chip area needed, no effort is made in this direction for this multiplier design. The major means to suppress spurs are through bias/power optimization and filtering.

To sum up, we decide to use filters to suppress the spurs on f0 and 4f0 at the output of Doubler A and the spurs on 2f0 and 8f0 at the output of Doubler B. Two bandpass filters will be included in the multiplier chain. Detailed filter specifications will be discussed in the section about filter implementation.

3.2.4 Spurs on Odd Harmonic Frequency

In the above analysis, the 1st doubler is assumed to work ideally, so that no odd order harmonics will appear in the subsequent stages. This is based on the basic mathematical principle that linear combinations of even numbers can only be even number, while the linear combinations of odd numbers can be odd or even.

Actually, spurs at the input of the first doubler or unbalanced input signal generates odd order harmonics at the output of the 1st doubler. These odd order tones will generate nearby unwanted tones that are not shown in the analysis above. Fig 3.14 shows the typical actual spectrum along the multiplier chain where the first doubler generates odd order harmonics.

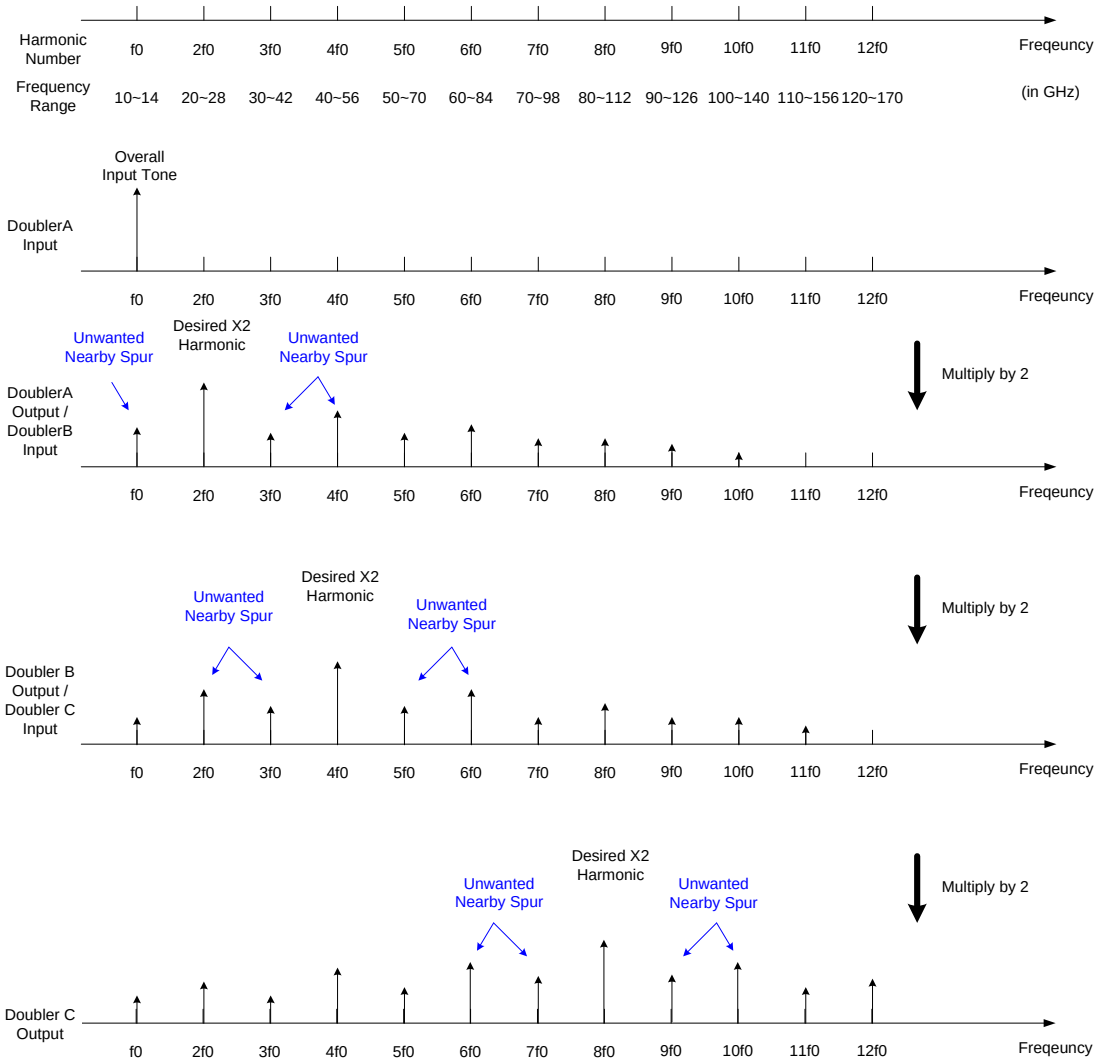


Fig 3.14 Odd order tone generation through the multiply by 8 chain

We shall see that with the presence of odd order nonlinearity, new unwanted nearby spurs appear at the output of each doubler. Their can be stronger or weaker compared to the nearby even order spurs. Since they are even closer to the desired harmonic, it is more difficult to suppress them with filtering. More overlap simply means that they appear in the transition band or the pass band of the filter and experience less suppression. So, it only takes relatively low level of harmonic or unbalance at the input of the 1st doubler to cause considerable amount of nearby odd order harmonics at the output of the multiply by 8 chain.

Because spurs generated in later stages depend on the spurs generated in the preceding stage, it is vital to keep the 1st doubler close to ideal operation and generate as low odd order harmonics as possible. This poses stricter requirement concerning linearity and common mode rejection of the input buffer preceding the 1st doubler.

3.2.5 Gain Compression

When the input signal to the frequency doubler is relatively low, the operation of the doubler can be modeled with a linear multiplier. Fig 3.15 shows the model.

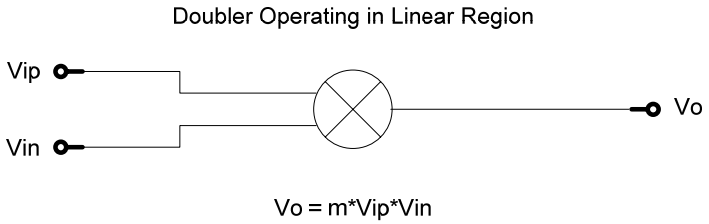


Fig 3.15 Doubler "linear" operation model

The input signal Vip and Vin are a pair of anti-phase sinusoidal. $Vip = V_i \sin\theta$, $Vin = -V_i \sin\theta$. V_i is the amplitude of input signal. If the doubler operates "linearly", we say the output signal of the doubler is linearly related to the multiplication of two input signal. We have $Vout = m*Vip*Vin = m*V_i \sin\theta * -V_i \sin\theta = mV_i^2(\frac{\cos 2\theta - 1}{2})$. The output signal on double frequency is $Vout = \frac{mV_i^2}{2}\cos 2\theta = V_o \cos 2\theta$.

The signal power is proportional to the square of signal amplitude. We have $Pin \propto V_i^2$ and $Pout \propto V_o^2 = \left(\frac{mV_i^2}{2}\right)^2 = \frac{m^2}{4}V_i^4$. Suppose input signal is increased from V_i to $k*V_i$, the input power increment in dB is $\Delta Pin\_dB = 10\log(k^2)$. The corresponding increase in output is $\Delta Pout\_dB = 10\log(k^4) = 2*\Delta Pin\_dB$. This means that for 1 dB input power variation, output power will change by 2 dB.

This conclusion can be extended to higher order "linear" multiplication. When an Nth order multiplier works "linearly", 1 dB input power change leads to N dB output power change. For an 8th order multiplier, this means the output power will change by 8dB for each dB of input power change, which is actually not a desired property for two reasons. First, this makes it difficult for the succeeding stage to handle a large signal range. The output power is so sensitive to input power that it is difficult to adjust the output power to a desired level. Second, for a wideband multiplier chain, this means difficulty of getting a flat gain. Any gain variation in each multiplier stage will be amplified along the multiplier chain.

Fig 3.16 shows the typical input-output power relation of a frequency multiplier. Depending on the multiplication factor N, the slope to of output power in linear region is N. When input signal increases beyond the linear gain region, due to compression of the output harmonic

signal, the output power increases slower than at lower input power level. The multiplier enters gain compression region when output power varies much slower than input power. At certain point, the output power may level off or even decrease due to deform of the output waveform.

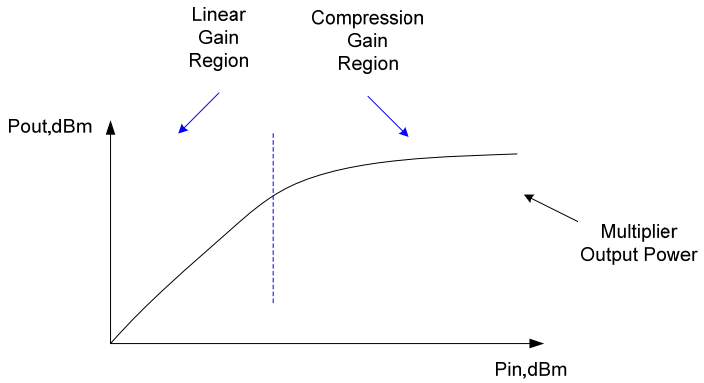


Fig 3.16 Typical multiplier output power response vs. input power sweep

To avoid the unfavorable linear region, the input power to a multiplier should be high enough to drive it into gain compression. This is especially important when designing a multiplier chain, because each multiplier stage depends on the output power from the preceding stage. Operating in the linear region makes the output power level very unpredictable.

One point worth mentioning is that the driver circuit of a multiplier can compress by itself. If we look at the output of the multiplier, similar compression effect will be observed. But actually, the multiplier is not operating in its gain compression region. So when the input signal to the buffer reduces, the output power of the multiplier would drop quickly. It is thus necessary to guarantee the linear operation of multiplier driver.

3.2.6 Noise Consideration

3.2.6.1 Impact of LO Noise Side Band

The receiver mixer will take the difference frequency of LO and reflected RF signal to produce the IF frequency signal which contains the target range information. Noise coming along with the LO signal plays an important role in this down conversion procedure.

Fig 3.17 shows the RF, LO and IF spectrum of a superheterodyne receiver. A much stronger adjacent interferer is present at the RF port together with the desired received signal. If the LO is an ideal single tone, then after the down conversion, two IF tones will be produced with the same frequency spacing as the RF tones. However, in reality the LO signal is accompanied by its noise sideband. As a result, the down converted IF signals also have their noise skirts. Since the Interferer could be much stronger than the desired signal, the IF sideband related to the interferer may overwhelm the desired IF signal. This problem is caused by reciprocal mixing of RF signal with unwanted tones, in this case, the noise side band of the LO signal. [7]

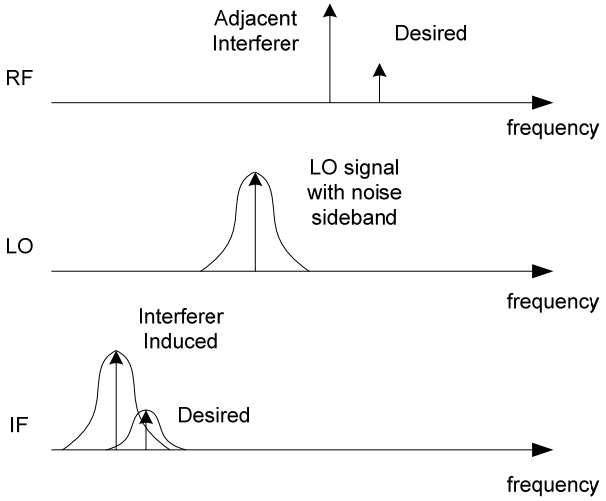


Fig 3.17 Effect of LO noise sideband on superheterodyne down-conversion

In the context of a continuous wave radar system, similar problem exists. Since in a continuous wave system, same LO is used for both transmitted signal and the mixer LO, the effect of noise sideband will corrupt the RF spectrum itself. Fig 3.18 shows the transmitted and received signal with or without LO noise. Clutter sideband would obscure the target return or at least reduce the SNR of received signal. [8]. Then after down- conversion, the IF signal will no doubt be further obscured.

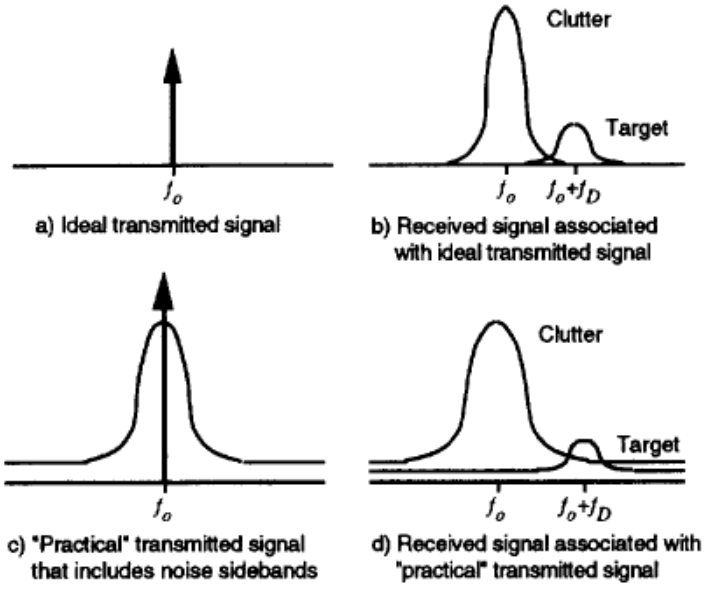


Fig 3.18 Effect of LO noise sideband on CW radar received signal [8]

CW radar must transmit while it is receiving, which poses a big problem if not handled carefully. The leakage of transmitted signal into the receive path could seriously degrade its performance. This is a significant problem even with a dual antenna configuration. Since normally the transmitted signal is much stronger than the reflected signal, such a leakage may blur the RF spectrum at the receiver input when LO noise sideband exists. Fig 3.19 shows several possible leakage paths in a single chip dual antenna CW system.

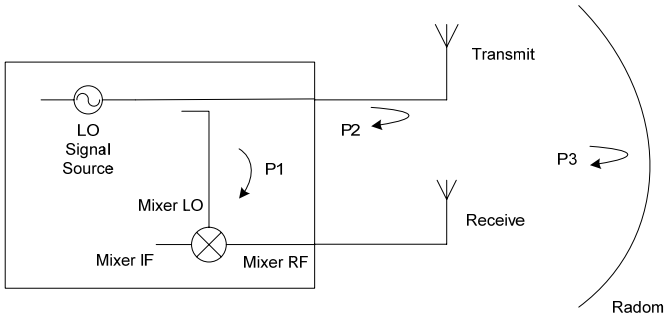


Fig 3.19 Possible leakage paths in a single-chip dual antenna CW radar configuration

P1 denotes the leakage within the chip to mixer RF port. Several possibilities exist in that category, including the leakage from mixer LO port to mixer RF port, as well as the leakage through coupling between transmit and receive paths. P2 denote the leakage due to antenna mismatch. Reflection from the transmitter antenna back to the chip may again leak to the receive path through various routes. P3 denotes the reflection from the radom in front of the antenna. Ideally, it should be transparent to the radar, but in reality, leakage from that path could be on the same order as P2 [3]. Although dual antenna configuration avoids the leakage through the circulator used in single antenna configuration, other leakage paths can still degrade the received signal SNR. Fig 3.20 shows the spectrum of LO, RF and down-converted IF signal spectrum in a CW radar system. Notice that the noise side band at IF due to LO leakage overshadows the desired down-converted signal.

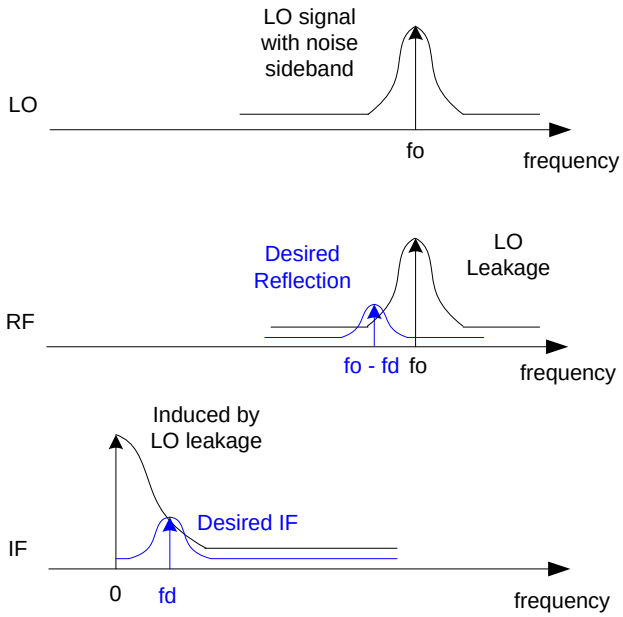


Fig 3.20 Effect of LO to RF leakage in a CW radar system

3.2.6.2 Phase Noise in Multiplier

The problematic noise sideband in the above plot contains both AM component and PM component. Due to the amplitude limiting effect by gain compression of the multiplier chain, the AM noise side band is suppressed to lower level [9]. It is thus important to reduce the phase noise of the transmitter.

Frequency multiplier also multiplies the phase deviation of the input signal. Even with an ideal multiplier without any noise from itself, the output phase noise spectrum will suffer the inevitable degradation of 20*logN dB, where N is the multiplication factor. [10]. More in depth theoretical analysis can be found in [11]

On top of that, noise sources from the multiplier also contribute to the total phase noise. This part of phase noise is called “excessive phase noise”. Some work decades ago [12],[13],[14] tried to characterize their contribution through experiment. Suggestions to reduce the phase noise are proposed, such as applying RF degeneration.

In order not to let the up-conversion chain be the bottle-neck of phase noise performance of the transmitter, the excessive phase noise from the multipliers should be minimized. The noise performance of the up-conversion chain is under trade off with other design goals, such as frequency response and spectrum purity. Some measures are taken to lower the noise added by the circuit blocks. The phase noise performance is characterized after the design. Limitation due to excessive phase noise is found from simulation results.

3.3 Sub Circuit Modules

3.3.1 Considerations on Each Block

When multiple circuit blocks are put together, their interaction determines whether the overall circuit can work concordantly and deliver good performance. Some of the considerations on the above mentioned circuit blocks in the multiply by 8 chain are discussed in this section Details about the doubler have been discussed in Chapter 2. The topology and performance of the rest circuit blocks will be discussed in the following sections.

Doubler:

On top of high conversion efficiency and low spurs in the output, the doubler should maintain an appropriate input and output power level so that its buffer can deliver enough drive power to it over the frequency band and the balun can operate linearly to guarantee its performance.

Filter:

The filter should have a flat passband response and a sharp transition band to give enough suppression to the unwanted tones. Actual passive components introduce losses through metal or substrate loss, so higher passband insertion loss is expected. We would like to keep them as low as

possible and to preserve the transfer function shape of the bandpass filters.

Balun:
The major function of balun is to convert the single-end output signal from the doubler to a differential version. It should keep the amplitude and phase unbalance of two output signals as small as possible over the entire band. It is better that its frequency response does not drop quickly so that it can be used in a wideband system. It should provide wideband termination impedance to the filter. It should work linearly, since saturation of the transistors not only introduces unwanted spurs but also degrades the balance of output signals.

Buffer Amplifier:
The buffer amplifier should drive the doubler hard enough into gain compression for a more constant output power level regardless of the input power. As discussed in Chapter 2, there is a trade off between frequency response and output spectrum purity of the doubler just by adjusting its degeneration. An active balun typically introduces a roll off frequency response rather than any peaking for a better balance performance. Additional matching would take more chip area and introduce higher loss. These limitations make the buffer amplifier the only logic choice for compensating the overall frequency response. It should not generate spurs since it drives the doubler directly. Any spur from its output will affect the doubler operation. If it introduces too much nonlinearity, then the effort of introducing a filter to reduce the unwanted spurs is just useless. The input of the buffer amplifier should provide wideband termination impedance to the preceding filter. Besides, common mode rejection of the differential buffer amplifier helps to correct the residual unbalance from balun output, which is also important for doubler operation.

3.3.2 Filter

As discussed in the previous section, two band pass filters are required in the signal up-conversion path. These filters are used to suppress the harmonics and the spurs generated during frequency multiplying. The nearby odd order spurs are meant to be suppressed by perfect balanced operation of the doubler. Filtering mainly targets nearby even order spurs. By suppressing these terms, the succeeding doubler is guaranteed to be driven by input signal with a cleaner spectrum.

Derivation of Filter Specification
The respective frequency bands in which each harmonic term may appear is listed again in Table 3.2.

Table 3.2 Frequency range of each harmonic component

Harmonic component	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$	$6f_0$	$7f_0$	$8f_0$	$9f_0$	$10f_0$	$11f_0$	$12f_0$
Frequency range(GHz)	10 ~14	20 ~28	30 ~42	40 ~56	50 ~70	60 ~84	70 ~98	80 ~112	90 ~126	100 ~140	110 ~154	120 ~168

We denote the instant frequency of the input tone to be f0. When swept over frequency for FMCW operation, it takes the band from 10~14GHz. The passband and stopband frequencies can be determined according to the requirement for spur suppression as mentioned before. It is restated here. The first filter should suppress tones on f0 and 4f0 and pass tone on 2f0. The second filter should suppress tones on 2f0 and 8f0 and pass tone on 4f0.

Exactly how much dB of attenuation is required in the stop band is not determined from system level simulation because the spur generation is related to the specific circuit blocks like the doubler. Instead, filters and the active circuit blocks are developed in parallel. Specification of the filter, especially stop band attenuation, is studied with simulation of the whole multiplier chain. Part of the specifications of the two filters is listed in table 3.3.

Table 3.3 Part of specifications of two filters used in our design

	1st filter	2nd filter
Maximum pass band ripple (attenuation)	As little as possible	As little as possible
Pass band	20GHz to 28GHz	40GHz to 56GHz
Stop band attenuation	To be determined	To be determined
Stop band	Lower than 14GHz and higher than 40GHz	Lower than 28GHz and higher than 80GHz

Component Limitations

The physical limitation of the components is considered when determining the type and order of the filter. Generally speaking, sharper transition requires higher order filter, and components of more extreme values. Large inductors are difficult to realize with on chip passive structure at higher frequency. On the other hand, limitation on minimal structure dimension forbids the use of excessively small capacitance. The IBM design kit offers a wide choice of passive components. The minimum nominal capacitance value of a MIM capacitor is about 90fF. The minimum nominal inductance value of an rfline is about 50pH, but the related line is very wide. Lines with more common widths show effective inductance about 80pH in W band. If components of lower value have to be used, customized layout of these components should be made. Then these structures are to be simulated with 2D or 3D EM simulator to get more accurate parameters. Even so, there will be difference between the simulation results from the EM simulators and that from library data, not to mention spreading of the manufactured components. To avoid these uncertainties, the filter prototypes are chosen and modified to use as less custom components as possible.

Filter Comparison

Butterworth (Maximum flat), Chebyshev (Equal ripple) as well as Elliptical filter can all provide the frequency response required with reasonable order (3rd order). The variation of pass band insertion loss and the transition band sharpness is a pair of contradicting goals. Butterworth filter shows no ripple in the pass band, but it requires higher order to have a sharp transition comparable to Chebyshev or Elliptical filters. A Chebyshev filter shows

constant amplitude ripples in the pass band and monotonous attenuation behavior in the transition band and stop band. 3rd order

Elliptical filter provide comparable pass band ripple as Chebyshev filters, and their transition is even sharper. Its stop band suppression is not monotonous as frequency deviates from the band center. There is a dip in its frequency response where maximum suppression is observed. This is not necessarily a negative point for our system since we are more concerned about nearby harmonics. But the Elliptical filter requires more LC resonance branches to give the additional pole and zero required. Frequency response curves of three filter prototypes, one of each type mentioned above, are given in Fig 3.21. The specifications are listed in Table 3.4:

Table 3.4 Specifications of three filter prototypes

Filter Specifications	
Maximum pass band ripple	0.1dB
Pass band bandwidth	20GHz ~ 28GHz
Stop band attenuation	More than 25dB
Stop band edges	Lower than 14GHz and higher than 40GHz
Reference impedance	50 Ohms

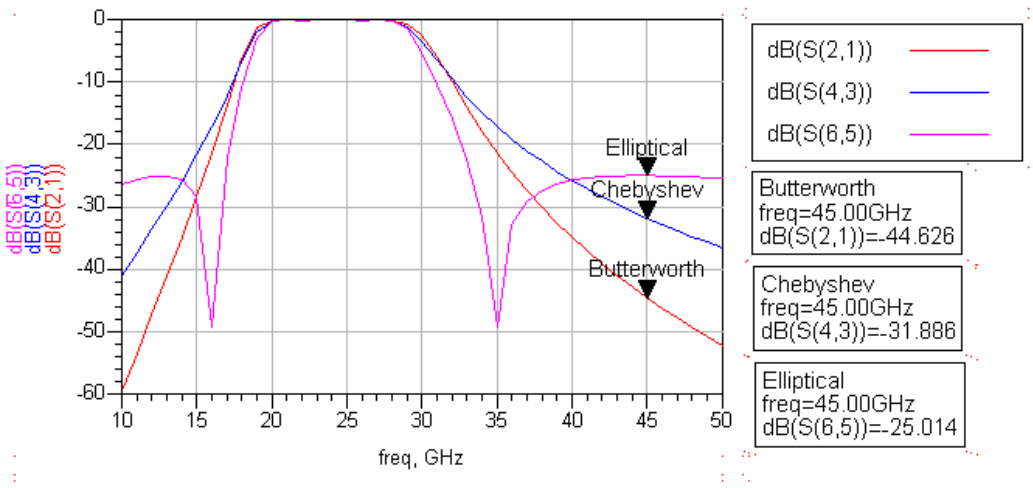


Fig 3.21 Frequency response comparison of three filter prototypes using a order of 3 for the Chebyshev and Elliptical filter and an order of 5 for the Butherworth filter.

The pass band characteristics are kept similar for fair comparison. To achieve the 0.1dB of passband variation, Butterworth filter requires 5th order, while Type I Chebyshev and Elliptical filters requires 3rd order. But the Elliptical filter has one more resonance branch. Higher order also causes the Butterworth filter to show sharper transition than the Chebyshev one. The component counts and the minimum and maximum component values required to construct these filters are summarized in Table 3.5

Table 3.5 Components used in the above filters

	Butterworth	Chebyshev	Elliptical
Inductor counts	5	3	4
Capacitor counts	5	3	4
Minimum inductance value	82pH	110pH	126pH
Maximum inductance value	1.1nH	1.14nH	947pH
Minimum capacitance value	41fF	40fF	48fF
Maximum capacitance value	547fF	410fF	360fF

Looking at the numbers, probably the most problematic component is the small capacitance. This small capacitance is normally found in the series path as part of a LC series resonator. Other components also show some difference, but they are all within the range available from the IBM library. There are several implementations for each type of filter, for example, with the first element in parallel or in series with the port. Different implementations do not affect the component values a lot, but the topology is changed. For instance, some may have more large value inductors than others. When differential filter is constructed, topology affects the value of the components in the shunt path. Considering performance, complexity and component values, Type I Chebyshev filter is chosen as the prototype.

Reference Impedance

In the above comparison, the reference impedance of the filters is kept to be 50 Ohms. The filter component values are related to this reference impedance. Choosing other reference impedance values may result in better realizable component values.

Matching network can be used to transform impedance between two ports. They can be used to transform the port impedance of active circuit to required reference impedance of the filter. But putting several matching network in cascade inevitably limits the bandwidth. To avoid this, we use buffer amplifier to provide the wideband termination impedance for the filter with minimum matching in between. Other constrains like the gain and output power of the buffer amplifier limits the actual range of termination impedance. The range that can be realized by the wideband buffer we designed spans from roughly 30 Ohms to more than 50 Ohms. Within this range, the component values of the filter do change, but not so much. As the first try we still choose 50 Ohms to be the reference impedance of filters.

Constructing Differential Filter

The filter is connected between the balun and buffer amplifier in a differential form. The way of constructing a differential filter from a single-end prototype is by connecting ground points of two single-end prototypes together and keeping them floating (no ground). Then input output signals are applied across the differential input and output ports. The components in the shunt path can be combined according to series and parallel impedance relation. This may or may not lead to more favorable component values, depending on the component type and topology. The procedure is illustrated in Fig 3.22. A third order Chebyshev band pass filter is used as an example.

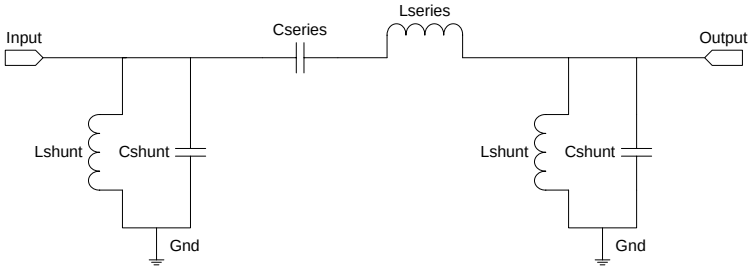


Fig 3.22(a)

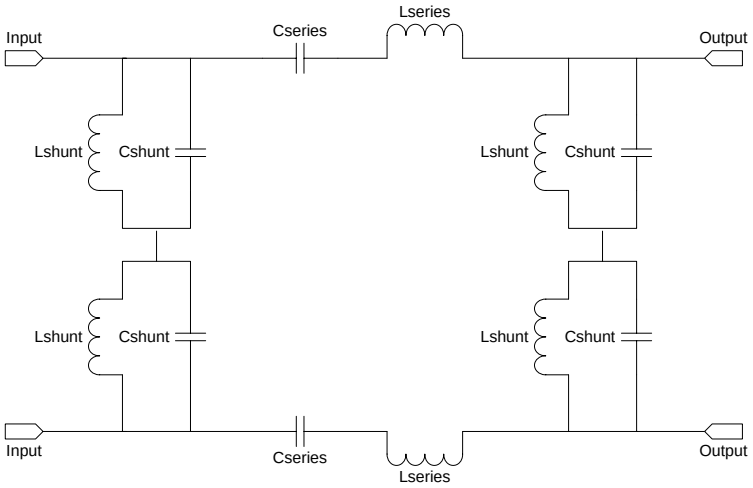


Fig 3.22(b)

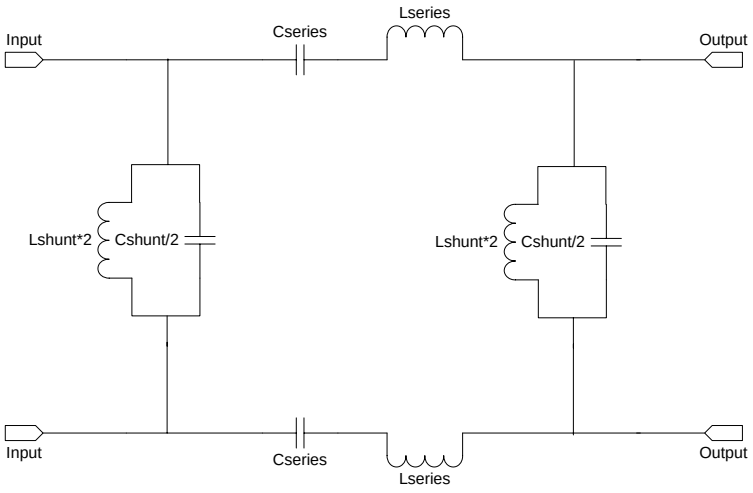


Fig 3.22(c)

Fig 3.22 Procedure to construct a differential filter from single-end prototype, (a) the prototype, (b) combining two single-end filter, (c) merging shunt path components

The series paths are not affected in this procedure. So the small capacitor and large inductor in that branch remains unchanged. But capacitance value in shunt path is effectively halved and inductance value there is doubled. In fact, when implementing the filter with real

components, to keep the filter balanced, the shunt capacitor is still realized by connecting two MIM capacitors in series. In this way, the unequal parasitics on the top and bottom plates of MIM capacitor will not unbalance the filter.

Termination Impedance Sensitivity

The transfer function of the filter depends on its components as well as the termination impedance. The nominal port impedance of the filter is chosen to be 50 Ohms. As the termination impedance deviates from the nominal value, the frequency response also deforms. Fig 3.23 shows the frequency response of a Chebyshev band pass filter. The termination impedance is swept to examine the sensitivity. Plot shows that higher termination impedance causes larger passband ripple as well as sharper transition. Lower impedance reduces the bandwidth and makes the transition less sharp. By comparison, the impact of higher termination impedance is less problematic. So, buffer amplifiers should avoid providing lower than nominal termination impedance.

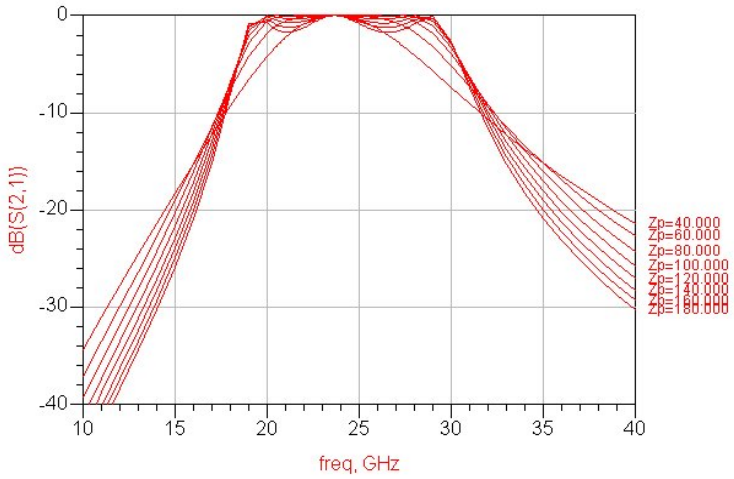


Fig 3.23 Sensitivity of filter transfer function to port impedance variation

Filter Implementation

The component values of the first filter are been labeled on Fig 3.24. It's based on a 3rd order Chebyshev band pass filter. The component that's most difficult to realize is the series capacitor. It is only 39.6fF, much smaller than the minimal capacitance available from the design kit.

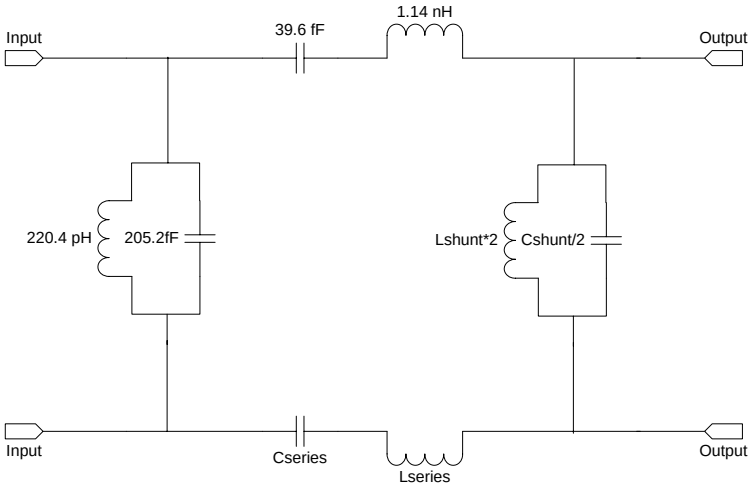


Fig 3.24 Ideal component values for the first differential band pass filter

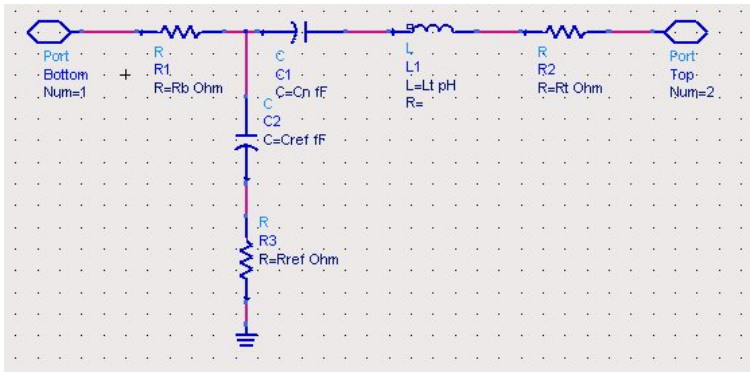


Fig 3.25 Model for MIM capacitor

In order to generate this small capacitance, we can either make a custom capacitor or construct it with the existing components. One way is to connect two capacitors in series to get a low capacitance value. The MIM capacitor available is unsymmetrical, and its model is shown in Fig 3.25. For the series connection, the two bottom plates should be connected together to minimize the effect of parasitic. Model fitting of the minimal size MIM capacitor gives the following numbers. The nominal capacitance, Cn is 91.2fF; the top contact inductance, Lt, is 5pH; the contact resistance, Rb and Rt is 1 Ohm respectively, the capacitance to substrate, Cref, is about 1.5fF. When the bottom plates of two such capacitors are connected together, the effective capacitance is halved to about 46fF. This value is close to the required 39.6fF capacitance. So it is possible to make a series LC resonator that behaves similar to that of the ideal one in the filter prototype. The frequency response of the filter can be better preserved.

Layout Floor Plan

Fig 3.26 shows the rough layout floor plan for the differential filter. The symmetrical inductor (Symind) has only one turn so that two outputs can be brought very close, and the traces connecting the shunt capacitor and inductor is kept very short. The parasitic from those traces can thus be minimized. The MIM capacitor is a 3D structure with port connections on top and bottom layers, the traces leading to shunt capacitance can be further shortened if the 3D

structure is fully utilized. In this way, the parallel resonator can better approximate the ideal one. Like the series capacitance, the parallel capacitance also consists of two series connected MIM capacitors for symmetry. To avoid mutual coupling between the two shunt inductors, they should be separated by some distance.

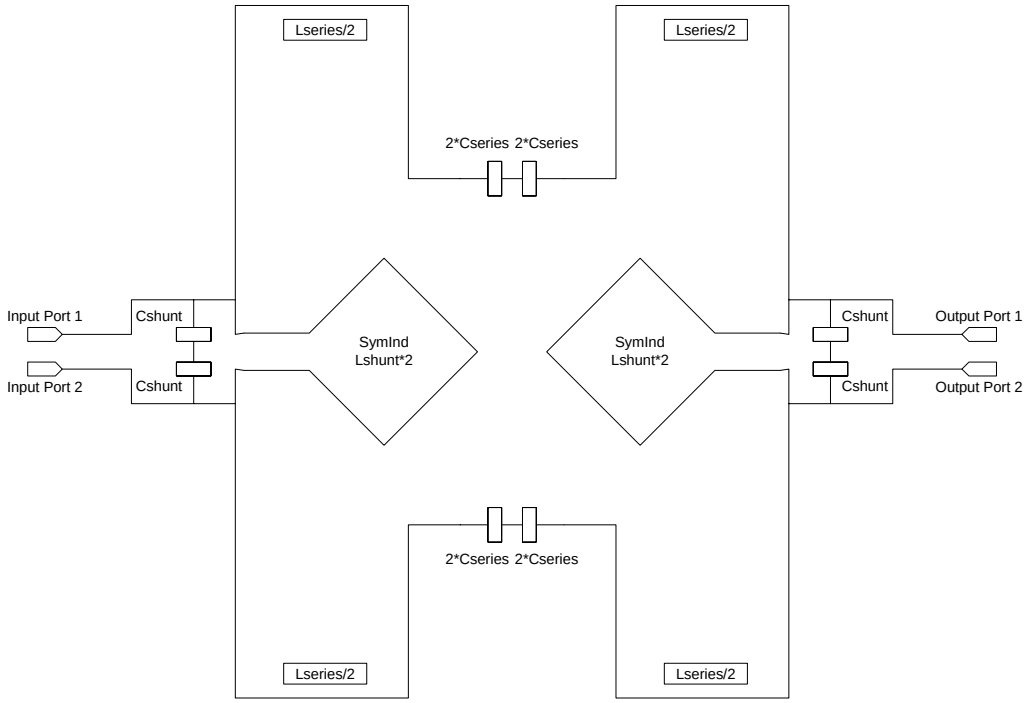


Fig 3.26 Rough layout for the bandpass filter

To make the series path symmetrical around the vertical center axis as shown in Fig 3.26, the inductor L_{series} is broken into two equal pieces and connected to both side of the series capacitor. Since Lt is very small, it can be absorbed easily. And C_{ref} can be neglected for the same reason. The series resistance models the losses; they are accountable for more insertion loss than filter with ideal components. The series inductor can be realized with rfline, which is narrow and flexible. It can be bended to make the whole layout compact. About 500um long on each side actually leaves freedom for layout, especially when big spiral inductors are used for the shunt inductor. Overall, this structure avoids long parasitic interconnections, and crossovers. The overall dimension is estimated to be about 300um*300um.

The shunt inductor is about 220pH. When implemented with an Rfline, the actual space it takes would not be much smaller than that of a symmetrical inductor. So, a one turn symmetrical inductor is chosen to implement the shunt inductor for better accuracy.

Fig 3.27 shows the frequency response comparison between an ideal filter and the filter designed with the above mentioned network. Since the actual layout has not been made, schematic simulation is performed for comparison. Except for the mutual coupling between the two symmetrical spiral inductors, other parasitic effect should be negligible. Within the pass band, the actual filter shows about 2.8dB to 3.7dB insertion loss. The transition band and stop band characteristic is almost identical to that of the ideal filter.

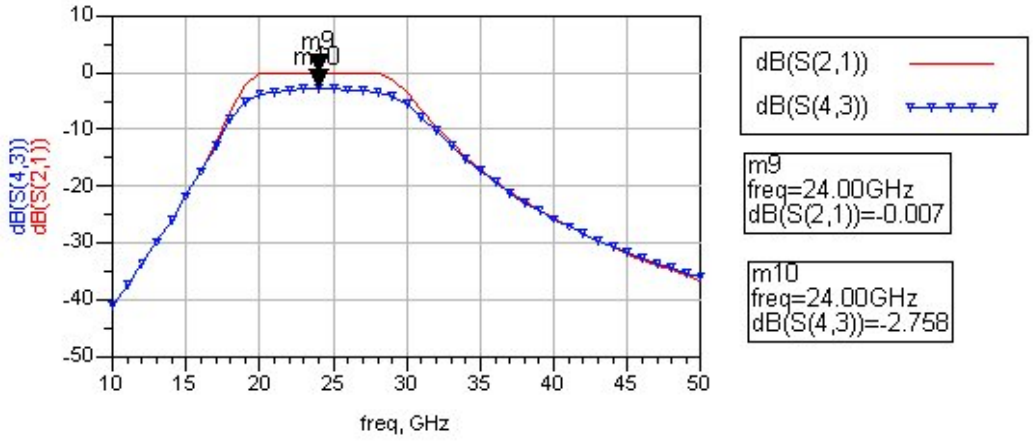


Fig 3.27 Frequency response comparison of the 1st filter

2nd Filter

We also meant to construct the 2nd filter with the same topology. Operating at higher frequency, the 2nd filter demands some even smaller component values. Fig 3.28 shows the ideal component values of the 2nd differential filter. The minimum capacitor value is reduced to 19.8fF. It is half the value of the smallest capacitance in the 1st filter. The first try is to construct this small capacitance with four capacitors in series. But the additional parasitics makes it difficult to approximate the ideal filter transfer by adjusting component values. Fig 3.29 shows the frequency response of the filter with 4 capacitors in series. Custom layout should be made for this small capacitance, attention should be focused on minimizing parasitic especially the parasitic inductance.

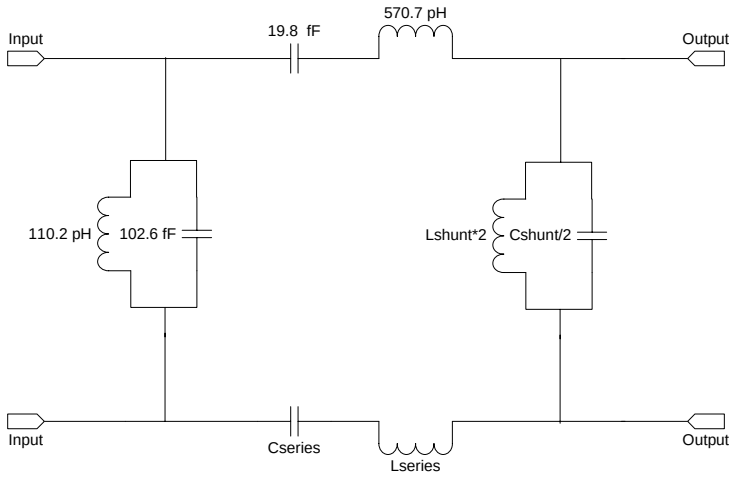


Fig 3.28 Ideal component values for the 2nd differential band pass filter

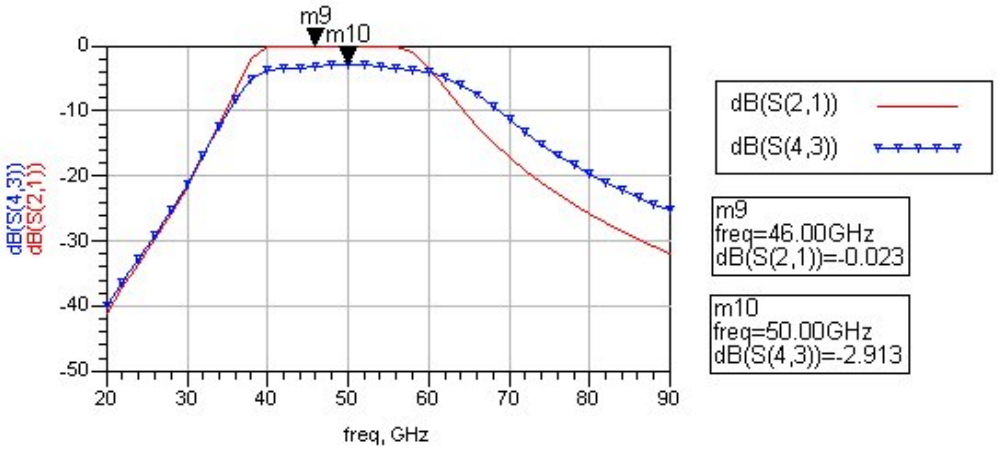


Fig 3.29 Frequency response comparison of the 2nd filter

3.3.3 Balun

The fact that the doubler has differential input and a single-end output means it is necessary to include a circuit block capable of converting a single-end signal back to its differential form. Many circuit structures, both passive and active ones are able to achieve this goal. They are called Baluns, which stands for Balance-to-Unbalance conversion.

In this multiplier chain, the balun should be inserted between two doubler stages. Differential signal path shows better tolerance to many troubles than single-end one, such as parasitic and noise from supply and ground paths. To avoid processing the signal in a single-end fashion, single-end path should be kept as short as possible. It is thus logical to connect the balun directly to the single-end output of a doubler.

The balun that we build is application specific. The context of a multiplier chain poses some requirement on it. First, its frequency response should not be a limiting factor to the overall bandwidth of the system. If it is not possible to keep the frequency response exactly flat, at least it should be relatively flat or in a shape easier for other circuit blocks to compensate the overall response. Second, the balun should not introduce too much nonlinearity. Although for spectrum purity considerations the most important doubler is the first one, latter stages can strongly affect the output spectrum if their nonlinearity is not controlled. In chapter 2, we have observed that a doubler stage is quite sensitive to unwanted tones in its input signal. Strong nonlinearity from buffer stages between two doublers may cause the spurs to increase by large amount in doubler output and result in serious degradation in spectrum purity. Third, the balun drives a differential filter of termination impedance about 50 Ohm. It should provide this wideband termination impedance.

For a long time people have used passive baluns at microwave frequencies to generate differential signals. Transformers and 180 degree hyrids can be used for this purpose. Advance of on-chip passive structures makes it possible to incorporate these structures in a MMIC. Passive baluns show good linearity, good balance around the band center. Some of

them can offer even a quite wide operation bandwidth. Their shortcomings include losses and large area consumption even when implemented at higher frequencies.

Improvements of active devices, mainly the increase of transistor ft, enable active circuits to operate at higher frequencies. In literatures, many active baluns are built for different frequencies. They complement passive baluns in several ways. They use transistors to provide conversion gain. Their gain is frequency dependent because of capacitive parasitic. They have a nonlinear transfer that distorts the input signal. They consume DC power but take much less chip area than their passive counterpart.

One of the very popular topologies is based on the bisymmetric Class-AB input stage of the Micromixer proposed by Gilbert [15]. A common-base transistor is combined with a current mirror to provide the two anti-phase outputs. Because of the low input impedance from these stages, it shows a relative good linearity. The topology is often used in a double balanced mixer with single-end RF input [16]. In [17], Hiraoka et al. combined a common gate stage and a common source stage to build a broad-band frequency doubler with single-ended input. The idea of antiphase signal paths is the same as that is used in a balun. Also differential pairs have long been used as balun. Raay et al. used a balun for their doubler work [18]. Several types of improvements have been made to the differential pair Balun. An RC parallel resonator at the emitter node has been added to block leakage current at resonant frequency [19], [20]. Ma et al. proposed a compensation RLC resonator from the collector of the common emitter transistor to the base of the common base connected transistor [21]. Kumar et al. proposed an RC feed forward waveform shaping network in their multiplier work [22]. In [23], Viallon et al. derived their unbalance evaluation criterion based on CMRR (common mode rejection ratio). They further derived the optimum impedance to improve CMRR for differential CE(common emitter) ,CB(common base) and CC(common collector) stages in the microwave frequency range(K Band). In [24], Tiiliharju et al. utilized CMRR of multiply stages to improve the balance. Statistical simulation result shows confirms the improved performance.

Appearing in many forms as they do, these circuits share a central idea to keep the amplitude and phase unbalance, as small as, possible over the operation bandwidth. The presence of parasitics limits the bandwidth for balance as well as transfer function. Linearity and balance are affected by power handling capability of the transistor.

Actually, both passive and active baluns have been evaluated through design phase. Some merits of passive baluns, like linearity and bandwidth, make them attractive for this application. However, considering the large chip area required, we have to turn to active balun instead. Since the multiply by 8 chain is modular, it is possible to replace several part and compare their effect on the whole circuit. In fact, several versions of conversion chain consisting of different baluns have been constructed and compared. The simulation results will be presented later in the chapter in the section about whole chain performance. Here we simply state without proof that using active balun incurs tolerable amount of degradation in output spectrum purity.

Two active baluns working around 24GHz and 48GHz will be used in the multiply by 8 chain. Their design considerations and performance will be discussed in the following section. A third balun will be used around 96GHz in W band blocks. Because of the high frequency, active balun no longer gives satisfactory performance. The performance of passive baluns, especially ratrace hybrid, will be discussed in the next chapter.

Choice of Active Balun

We have investigated several balun topologies to pick the most suited one for our circuit. The candidates are the input stage of the Micromixer [15], and two others based on common emitter differential pair. One of them has a capacitor resistor feed forward path, hence called RC Feed Forward Balun. The other has an inverting path that is split into two braches, hence called Invert Path Split Balun. Among the three candidates, the RC feed forward Balun is most promising. Its performance will be discussed in detail next. Detailed simulation result of input stage of Micromixer and Invert Path Split Baluns can be found in Appendix C. For conciseness, we only put some findings here about those two.

The problem with the input stage of Micromixer is that the phase shift along two signal paths differs a lot due to different transistor numbers. Phase relation of the two output currents differs from the ideal 180 degree by as much as 40 degrees around 48GHz. Such a large phase difference is too much for a Balun to be useful. The Inverting Path Split Balun shows comparable performance as the RC feed forward Balun in terms of amplitude and phase unbalance, as well as, frequency response. However, in order to make the output voltage signal balanced, the bias conditions of the transistors in two signal paths are made different. The output balance is achieved by a delicate combination of unbalance in both the effective input signals and the transconductances in two signal paths. This means more uncertainty when device mismatch is considered.

Differential Pair as a Balun

Common emitter differential pair gives differential output under differential excitation. Thanks to common mode rejection of this stage, it can produce output signals that contain a large differential part and a relatively small common mode part even when input signal is a single-ended one. The amplitude and phase difference of the output currents from a differential pair with single-end input signal is shown in Fig 3.30. Over 1dB of amplitude difference and less than 4 degrees of phase difference over a wide input frequency range shows the potential of further improvement for better balun performance.

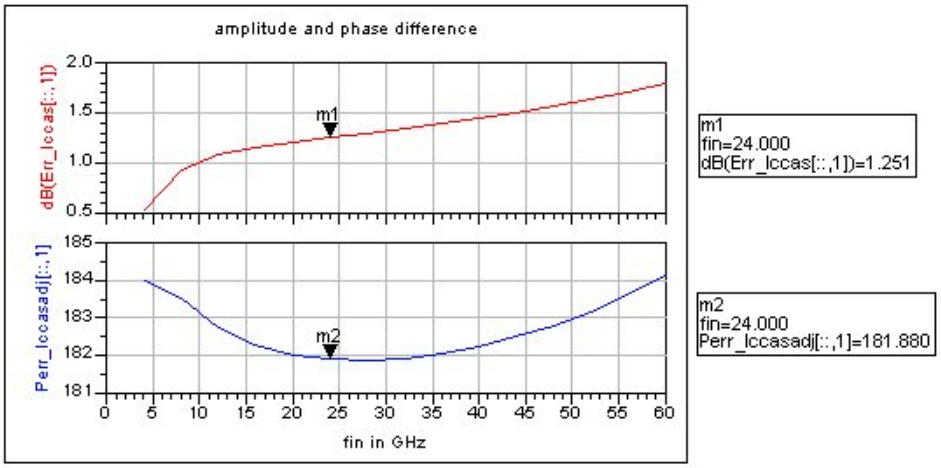


Fig 3.30 Unbalance between two output currents in a differential pair with single-end input

An observation made on the differential pair under single-end excitation is that the effective input voltages on the two transistors are different. This can be explained with the help of the following simplified model. Fig 3.31 shows a simplified small signal model for a differential pair with single-end excitation. T-model is used for the transistors, in which $Ze = \frac{Z\pi}{1+\beta}$. R_{bb}, C_{μ}, Rout and C_{out} are ignored for simplicity.

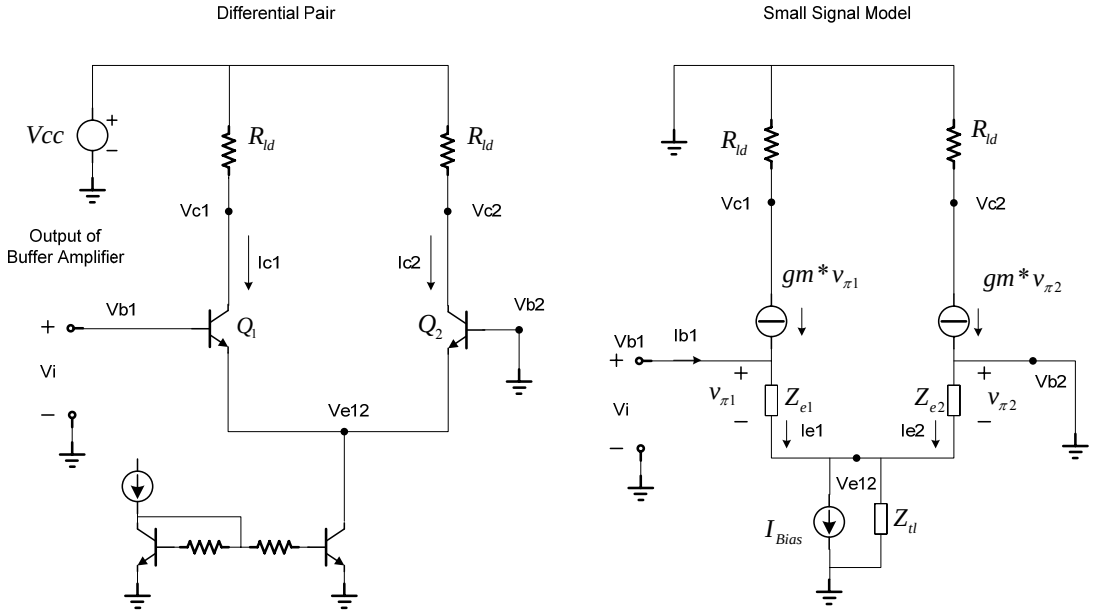


Fig 3.31 Small signal model of a differential pair with single-end excitation

The output impedance of the tail current source, Z_{tl}, diverts away part of signal current from the emitter of Q1. If the DC bias current of the two transistors are the same, then $Z_{e1}=Z_{e2}$.

From $v_\pi = Z_\pi * I_b = \frac{Z_\pi}{(1+\beta)} * I_b(1+\beta) = Z_e * I_e$, we have the following equation along the input loop from Vb1 to AC ground at Vb2, $\frac{v_{\pi 1}}{v_{\pi 2}} = -\frac{I_{e1} * Z_{e1}}{I_{e1} * Z_{e2} \,||\, Z_{tl}} = -\frac{Z_e + Z_{tl}}{Z_e}$ (3.5).

The above analysis shows that the major cause of different v_{be} on two transistors is the finite output impedance from the tail current source. Even though at lower frequency this impedance can be increased by degeneration or with another cascode transistor for the tail current source, at higher frequency, parasitic capacitance at that node will reduce the output impedance and reduce the effective voltage on the common base connected transistor,Q2. Besides, different effect of C_μ when referred to the base-emitter loop of the two input transistors also introduces unbalance. In the above analysis, the ground is assumed to be ideal. In really, parasitic along ground path alters the voltage division relation and has a strong impact on the balance of two signal paths. So, it is crucial to implement good local AC ground at those nominal signal ground nods, especially at the base of the common base connected transistor.

RC Feed Forward Balun

The fact that $|I_{e1}| \succ |I_{e2}|$ points to a most instinctive solution to divert part of the input signal from Q1 to Q2, so that when balance is reached, $|v_{\pi 1}| = |v_{\pi 2}|$. Adding another signal path from V_{b1} to V_{e12} can make this happen. Actually, this idea was already presented by Kumar et al. [22] in their multiplier work.

A resistor inserted between V_{b1} and V_{e12} can compensate different input signal on the two transistors. There should be a capacitor in this additional path as a DC block. The impedance related to the feed forward path affects both the amplitude and the phase difference at the output. Simulation shows that small capacitance used in the feed forward path worsens the phase unbalance. It is possible to correct the phase unbalance with another inductor in series. But it normally takes several hundred pH of inductance to correct a few degrees of phase unbalance at the frequency of interest. Considering the difficulty of layout and additional area needed, we did not use inductor here. An RC series branch is used as the feed forward path. The capacitor value is chosen just large enough not to degrade the phase unbalance performance. Cascode transistors are added to minimize Miller effect and to make the output impedance of the two branches closer. The circuit topology is shown in Fig 3.32.Emitter followers used to interface the band pass filter is also included here.

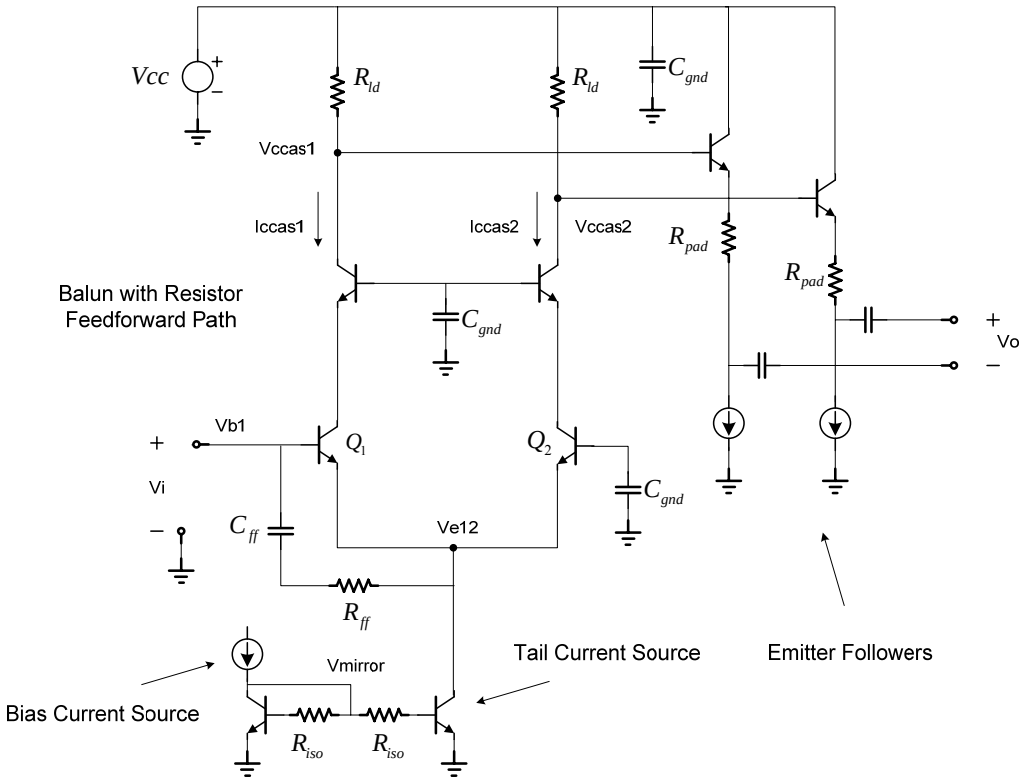


Fig 3.32 Topology of the RC feed forward Balun

The feed forward path connects the emitter point of the differential pair to the input. This connection increases the input capacitance. When connected to a doubler, this means more capacitive loading to the doubler which is not desirable for the overall frequency response. The typical frequency response is shown in Fig 3.33. Efforts have been made to use degeneration or feedback to compensate for the frequency response. But these changes modify the impedance along two signal paths and are often against the balance performance of the Balun. So, the roll off in frequency response is accepted. It has to be compensated in other circuit blocks, which is achieved mainly through peaking in the buffer amplifier.

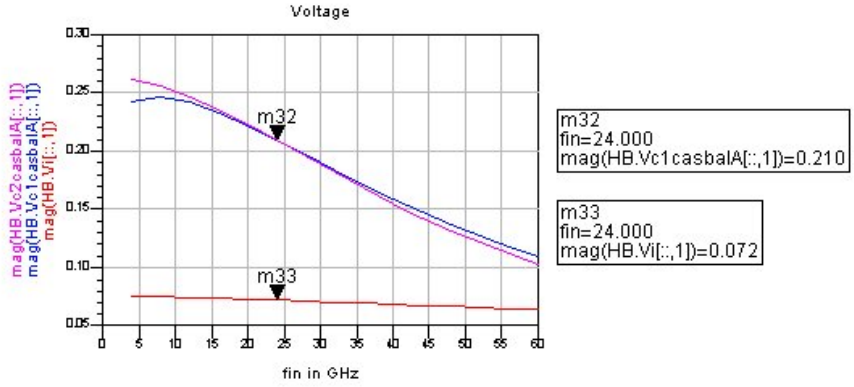


Fig 3.33 Typical input and output voltage relation of an RC feed forward Balun

One point worth mentioning is the high value(over 2K Ohm) resistor inserted at the base of the tail current mirror to isolate the impedance of DC bias path from RF signal path in the Balun. Such isolation is necessary for obtaining a predictable balanced performance.

Rff Sensitivity

Fig 3.34 shows the amplitude and phase balance between two outputs. In case of this example, the Balun is optimized for operation from 20GHz to 28GHz. The amplitude unbalance within that band is within +/-0.2dB, the phase unbalance is less than 2 degrees. The balance relies on the absolute value of R_{ff} as well as matching of all the devices between two branches. It is necessary to check the sensitivity of output balance to the variation of R_{ff}. Fig 3.35 shows the simulation results with 15 percent variation on R_{ff} value. The degradation is within a reasonable range. According to the data sheet of the IBM bicmos process, the NS resistor of several geometries rarely deviates from the design value for 8 percent across all temperature and process corners. So it is safe to say that the structure is robust against resistance spread.

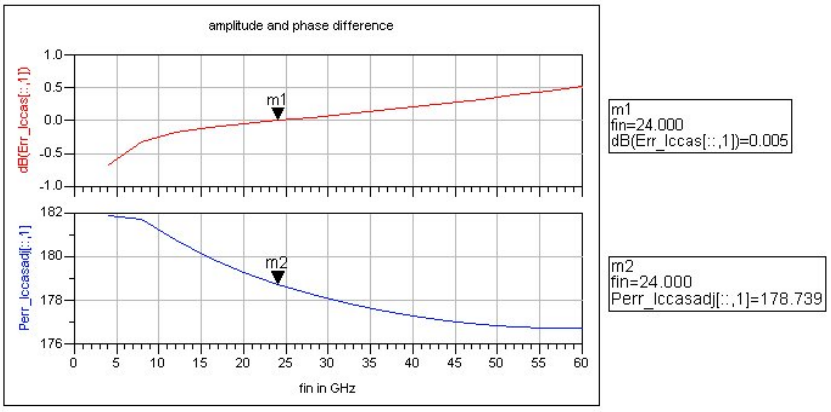


Fig 3.34 Unbalance between two output currents in a RC feed forward Balun with single-end input

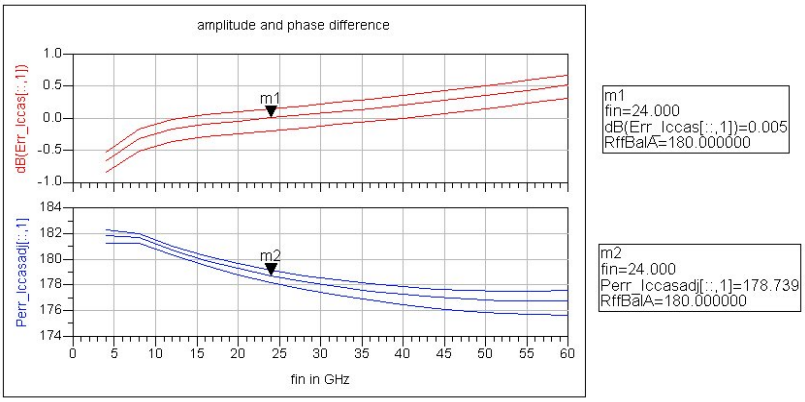


Fig 3.35 Variation of output unbalance from RC feed forward Balun with 15% of variation on R_{ff} value

Power Handling Ability

Under normal operation, the input power to the balun is kept low enough to avoid transistor saturation or hard clipping. When connected with the doubler together, this is achieved by choosing the right device size for the doubler so that its output power will not cause strong nonlinearity in the Balun. Although smaller transistor size for doubler means lower conversion gain, considering the spectrum purity requirement, this is an inevitable trade off.

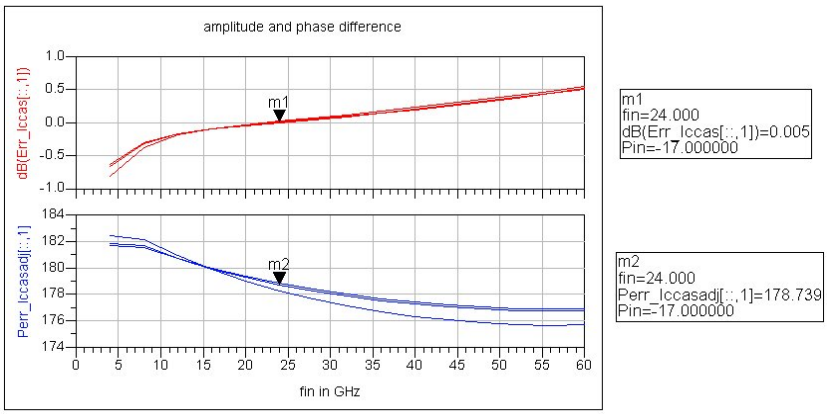


Fig 3.36 Variation of output unbalance from RC feed forward Balun with +-6dB of variation on input power

Fig 3.36 shows the simulation results by varying the nominal input power by +/- 6dB. Margin has been left with higher bias current to guarantee balance as well as linearity of this stage. Since the doubler preceding the balun operates normally in gain saturation, its output remains within a range of 3 or 4 dB due to input variation of more than 10 dB. In this sense the balun can keep its performance when used in the multiplier chain.

On the balun side, RC feed forward path diverts away part of input signal, lowers the input voltage swing thus improves its power handling capability. Other Baluns may be able to handle higher input power without causing strong nonlinearity, their gain is also lowered. So, for an overall good conversion gain from the input of the doubler to the output of the Balun without causing strong nonlinearity problems, our choice is reasonable.

Emitter Follower as Filter Driver

As mentioned before in order to suppress the unwanted spurs, a bandpass filter should be inserted between the Balun and the buffer amplifier of the next doubler. Since the Balun directly loads the doubler, the bandpass filter will be in a differential form. There should be a stage providing the interface to the filter. It should have wideband 50 Ohms output impedance. It should produce enough current to feed the filter, and the frequency response should not show quick roll off. It should not introduce too much nonlinearity since the intention of having a filter is to improve spectrum purity. It is better if this stage can also provide a higher impedance to lower the loading on the Balun. To sum up, the ideal interface should be a voltage buffer with wideband 50 Ohms output impedance.

Simulation shows that emitter follower can meet the needs mentioned above. It approximates a voltage buffer in the sense that the high input impedance allows a lower input power to mobilize large current swing at the output so that the output voltage follows the input voltage. Even though its performance degrades as the frequency rises, it is still quite effective to work as an impedance transformer to reduce the loading of the preceding stage by the input impedance of the following stage. Detailed analysis of the emitter follower in both low and high frequency regions can be found in [25].

The current density of the transistor is roughly limited by fT, so scaling determines the current output capability. Scaling up the emitter follower increases the bias current and also the amount of current that can be stirred by input voltage. Larger transistor size also means lower input impedance and higher loading to the preceding stage. More capacitive part is presented to the Balun.

Scaling up also lowers the output impedance of the emitter follower. The output impedance of an emitter follower is affected by the impedance connected at its base terminal, in this case, the output impedance of the Balun as well as the pull up resistor. Considering normal value of those impedances, the emitter follower needs to be scaled down to a pretty small size to give a real part of output impedance that is close to 50 Ohms. However the small size introduces a problem, bias current is so low that the collector and emitter AC currents are easily clipped and that the emitter follower can not provide enough AC current to the filter.

This contradiction is solved by adding a padding resistor of about 10 to 20 Ohm in series at the emitter side. By adjusting the value and emitter length of the emitter follower transistor, the output impedance and unclipped large AC current swing are satisfied at the same time. The draw back of resistive padding is additional noise and higher input power required from the preceding stage, still these are overweighed by its merits.

The output impedance of the emitter follower contains an inductive part. It is compensated by a capacitor in series with the emitter. Value of the capacitor is adjusted to set the series resonance frequency to the center frequency of our band of interest. This capacitor also serves as a DC block. The output impedance has a real part that is close to 50 Ohms, and the imaginary part that varies slowly around zero across our bandwidth. A typical output impedance frequency response is shown in Fig 3.37. Fig 3.38 shows the typical input and output voltage signal wave form. The DC bias has been subtracted for a clearer comparison.

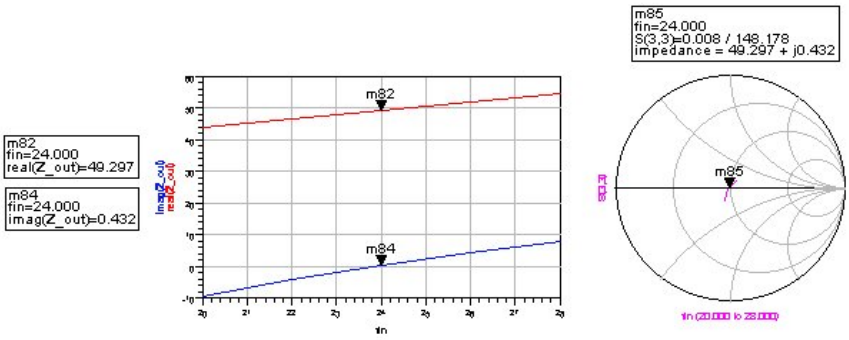


Fig 3.37 Output impedance and output reflection coefficient of an emitter follower

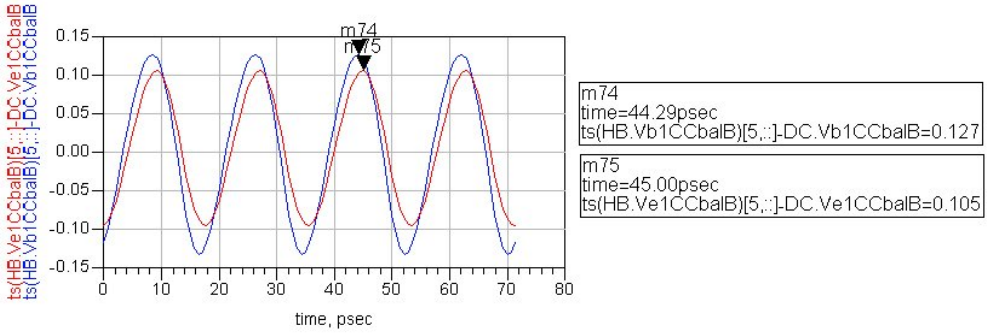


Fig 3.38 Voltage waveform on base and emitter terminals of an emitter follower

The emitter follower is DC coupled to the output node of the Balun. It can be biased with a current source to provide emitter DC current. The simplest realization of this current source is a large value resistor. Depending on the current required, a resistor of several hundred to over a kilo Ohm is required. It can also be implemented as an active current source. Although the output impedance would be lower than the resistor bias, and the transistor introduces more capacitive parasitic to the signal path, bias with current mirror makes the design more robust against resistance variation. The influence from the parasitic can be taken into account during the design procedure, so that it won't be a limiting factor.

The same resistor padding idea is also applied to the common base stage used to load the filter. Thus on both sides of the filter, wideband port impedance is provided to allow the filter deliver better performance. Emitter follower is also used to drive the doubler, which will be discussed in the section about buffer amplifiers.

3.3.4 Buffer Amplifiers

The buffer amplifier senses the signal from the filter and then amplifies it to drive the doubler. Here are the requirements on the amplifier:

Firstly, it should provide large output voltage swing to operate the next doubler in gain compression for a more constant output power level. Secondly, it shoulders the responsibility to compensate the overall frequency response. The frequency response roll off caused by the Balun should be corrected with peaking from this stage. Thirdly, it should operate linearly since it drives the doubler directly. Since the filter can normally suppress the far away harmonics to a rather low level, this buffer amplifier dominates how much unwanted tones will be delivered to the next doubler. Tolerable linearity should be maintained over a range of input power, although because of gain saturation of the preceding doubler, the input power to the buffer should not exceed the nominal value too much. Fourthly, it should provide wideband termination impedance to the preceding filter. And finally, common mode rejection of the differential buffer amplifier helps to correct the remaining unbalance in the output of the balun. It is also important for the doubler operation.

Since the buffer preceding the first doubler has other constraints, it will be discussed in the next section. Here we shall look at the buffer for the 2nd and the 3rd doublers first. The same topology has been used for these two stages. The following simulations about the buffer amplifier and its related stages are all base on Buffer B, referring to Fig 3.12. The signal voltage at the input of Buffer B, the input of Doubler B, the input of the Balun B and the input of Filter B are plotted in Fig 3.39. It is shown that with the help of the buffer amplifier, the signal at the input of Filter B, labeled as ViFltB, is relatively flat over a wide bandwidth.

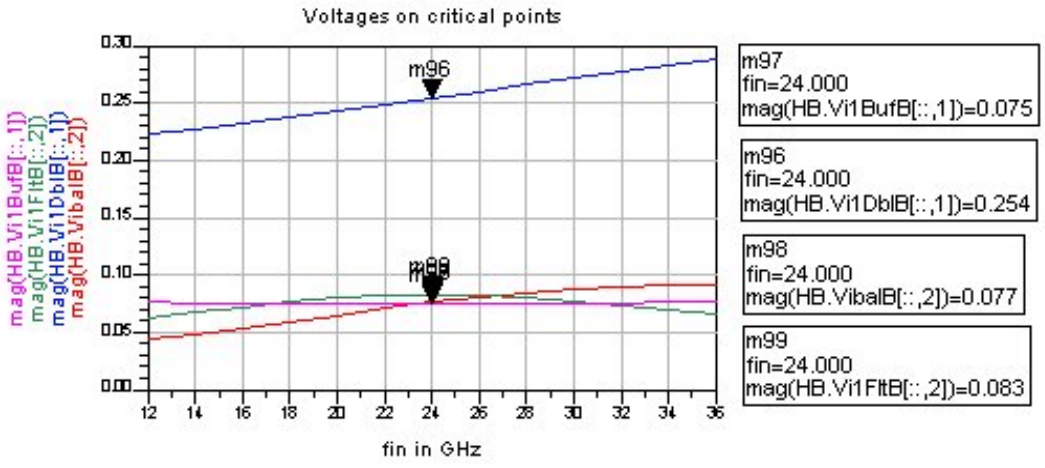


Fig 3.39 Voltages at several points along the chain made up of Buffer B, Doubler B and Balun B

About Cherry-Hooper Amplifier

Considering the wideband requirement of these amplifiers, we turn to some amplifier topologies that have been proven suitable for wideband operation. One of them is the long existed Cherry-Hoopper amplifier [26]. In [27], Rein et al. gave a qualitative analysis. The application of their amplifier is for optical communication, so the bandwidth of the broadband amplifier should extend from DC to tens of GHz. At higher frequencies, gain drops due to the effect of the capacitive components at both the input and output of a gain stage. If large impedance mismatch between neighboring stages is maintained, the transfer function of different stages remains approximately constant up to comparatively high frequency. Consequently, the cutoff frequency of the low-pass like transfer function of the amplifier is pushed upwards. The original Cherry Hoopper amplifier achieves the impedance mismatch by connecting common emitter stage, resistive shunt feedback transimpedance amplifier and emitter follower in cascade as shown in Fig 3.40(a). Impedance mismatch is obtained at each interface. The common emitter stage and the transimpedance stage are combined together, which forms the Cherry-Hoopper amplifier, shown in Fig 3.40(b). It can usually extend the cutoff frequency up to about 1/4 of the common emitter transit frequency of the transistor used.

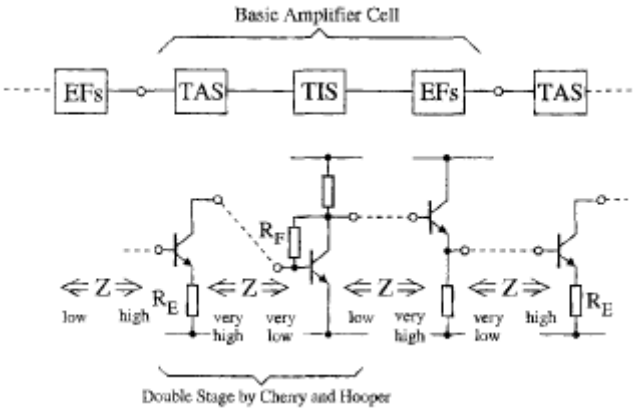


Fig 3.40(a) Principle of strong impedance mismatch in wideband amplifiers [27]

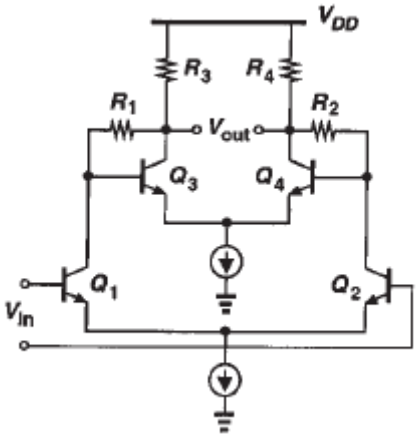


Fig 3.40(b) Topology of the original Cherry-Hooper Amplifier [28]

Over the time, improvements have been made to the original Cherry-Hoopper amplifier. Emitter follower was inserted in the feedback path in the feedback stage [29], [30] to separate two antiphase output currents that lower the actual output signal. Still, the central idea of large impedance mismatch is preserved.

Some modifications have to be made on this wideband amplifier to let it satisfy the requirement of our system. The Cherry-Hooper amplifier combines the common emitter stage with a resistive feedback amplifier. Since for optical communication, the bandwidth should extend to DC, these two stages should be DC coupled, which means that the RF performance is correlated to the DC bias through the choice of resistors. Low breakdown voltage of the BJT transistor poses constraint on choosing the component values. When an emitter follower is inserted in the feedback loop, this DC-RF correlation is even more problematic. However, for our application, signal within several discrete frequency bands should be processed. There is no need to extend the lower end of the transfer function to DC. So, AC coupling through capacitor can be used in both feedback path and between stages.

Other than that, the large impedance mismatch within the Cherry-Hooper amplifier is based on small signal analysis. When the circuit operates with large signals, the loop gain of the feedback stage drops and the large impedance mismatch, as well as, the related bandwidth extension effect diminishes. In fact this topology is better suited to be used for the beginning stages of the preamplifier for optical receiver module where the signal level is relatively low [28]. In our application, the buffer amplifier should provide close to 300mV peak voltage swing at its output to drive the doubler into gain compression. Besides, the buffer should operate linearly so as not to generate a lot of spurs to rattle the operation of the succeeding circuit block. In this sense, Cherry-Hooper amplifier could not be borrowed just as it is.

The topology of the buffer amplifier for Doubler B and C is shown in Fig 3.41. It is made up of a common base input stage, a dual loop feedback amplifier and an emitter follower output stage.

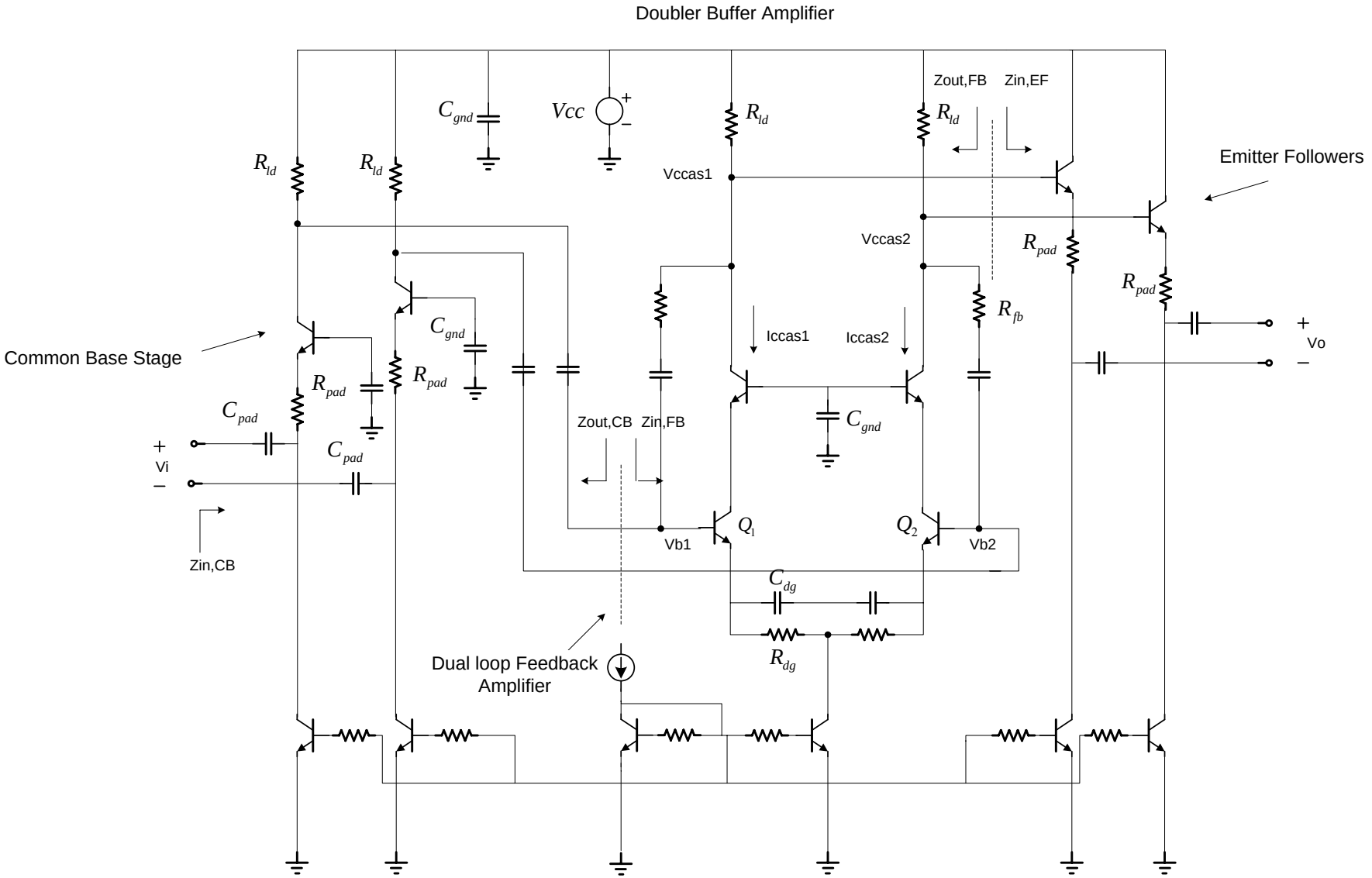


Fig 3.41 Topology of the buffer amplifier for the doubler

Design Considerations

Since at the input of our amplifier, wideband low impedance about 50 Ohm is required, a common base stage is used there. The output impedance of a common base stage can be made much higher than the input impedance of the feedback stage. But due to gain and linearity trade off, the pull up resistor at the collector limits the real part of its output impedance.

For the same reason as the emitter follower driving the filter, padding resistors are used to resolve the contradiction between input impedance and current swing. Input impedance frequency response is shown in Fig 3.42.

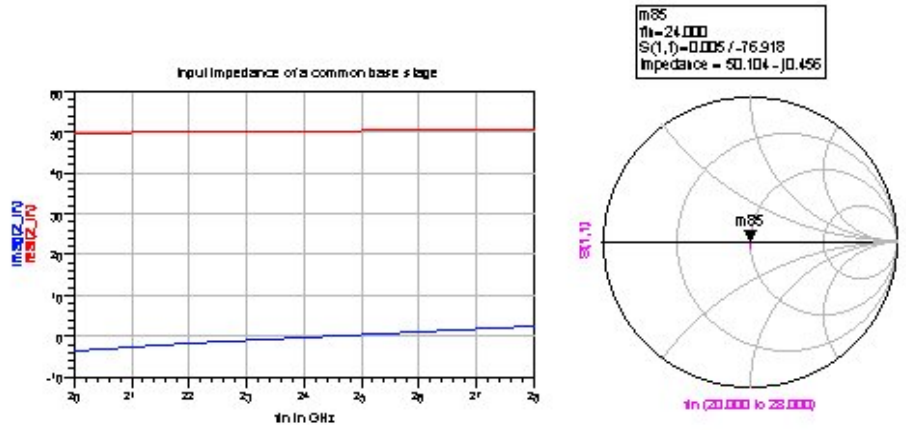


Fig 3.42 Input impedance of the common base stage

For the differential pair, cascode transistors are included to reduce Millor effect, as well as, to increase the output resistance. To lower the input impedance of the middle stage, shunt resistive feedback with AC coupling is used. However, this alone is not sufficient to provide a peaking response with enough gain. The RC degeneration is added to enhance the peaking effect. Its contribution is explain below. At lower frequencies, resistor Rdg dominates and the degeneration lowers the effective transconductance of the differential pair. As the frequency rises, the impedance of capacitor Cdg drops which reduces the degeneration effect and the effective transconductance starts to increase. This effect corresponds to a zero in the open loop transfer function. As the frequency increases more, the degeneration effect becomes negligible and the effective transconductance reaches a limit that is determined by the transistor transconductance. This process corresponds to a pole in the transfer function. The effective transconductance increases between the zero and the pole at higher frequency. This range allows peaking in the overall transfer function.

In the shunt feedback loop, an emitter follower can be inserted to reduce the loading on the collector nod of the cascode. However, simulation show that with feedback resistor value of several hundred Ohm, the recovered gain by adding an emitter follower is relatively low compared to the extra DC current. So, we do not choose to use emitter follower in the feedback loop.

The doubler after this buffer stage expects an input signal that rises with frequency to compensate the frequency response. The input impedance of the doubler can be roughly modeled with a series RC combination. It adds a considerable amount of capacitive loading to the differential amplifier when connected directly to the output. In order to lower the capacitive loading, as well as, to provide enough drive power to the doubler, an emitter follower is inserted as a voltage buffer. The emitter follower effectively converts a larger load capacitance to a smaller capacitance at its input impedance. to maintain impedance mismatch at its input in order to enhance a wideband operation. Fig 3.43 shows the input impedance of the emitter follower under similar input power. The capacitive part of that impedance is relatively high, even though its magnitude drops with frequency, it is still much higher than the output impedance of the dual loop amplifier, which is about 100 Ohms, across the band of interest. The capacitive loading to the amplifier has been reduced from 16fF to about 6fF with the help of emitter follower in this case. Due to the capacitive loading by the input of the doubler, the real part of the input impedance in Fig 3.43 drops quickly, at higher frequency it even enters negative region. This could lead to oscillation. However, the pull-up resistor of the dual loop amplifier serves to damp any oscillation at that point.

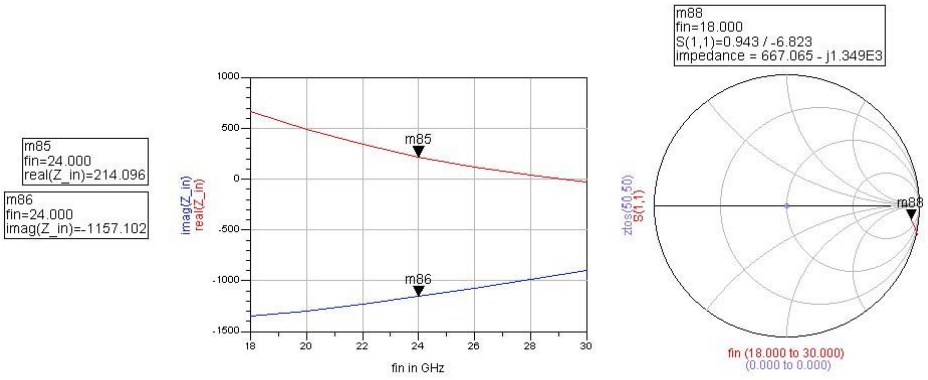


Fig 3.43 Input impedance of the emitter follower used to drive the doubler

Component Sensitivity

The degeneration RC combination is made differential to keep the circuit balanced. The bottom plates of the two MIM capacitors are connected together and floating. Parasitic capacitance to ground at that node has little influence on the performance. Fig 3.44 shows the effect of +/-15% variation of the feedback elements on the input voltage to the doubler, ViFltB, and the input voltage to the next filter, Vi1DblB. The shunt feedback resistor R_{fb}, the degeneration resistor R_{dg} and capacitors C_{dg} are varied respectively to find out frequency response sensitivity to them.

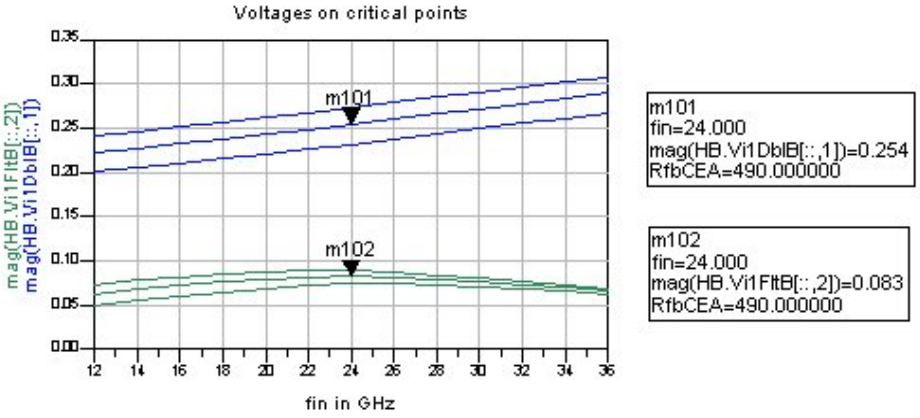


Fig 3.44 (a) Sensitivity of input signal voltage of the next doubler and filter to 15% variation of shunt feedback resistor

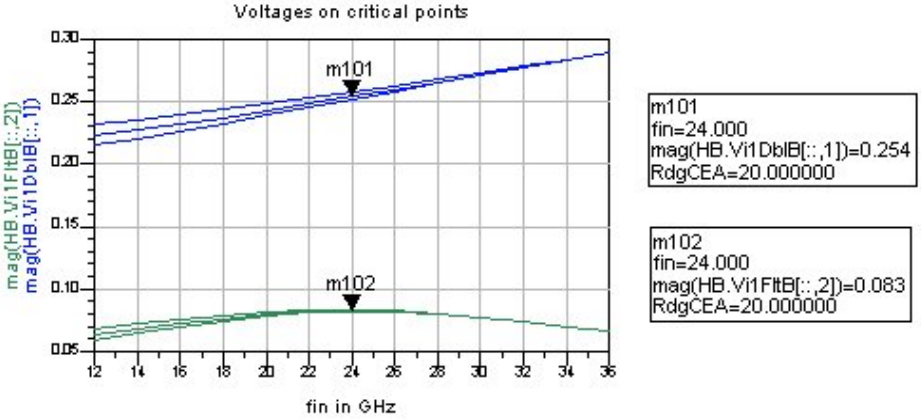


Fig 3.44 (b) Sensitivity of input signal voltage of the next doubler and filter to 15% variation of degeneration resistor

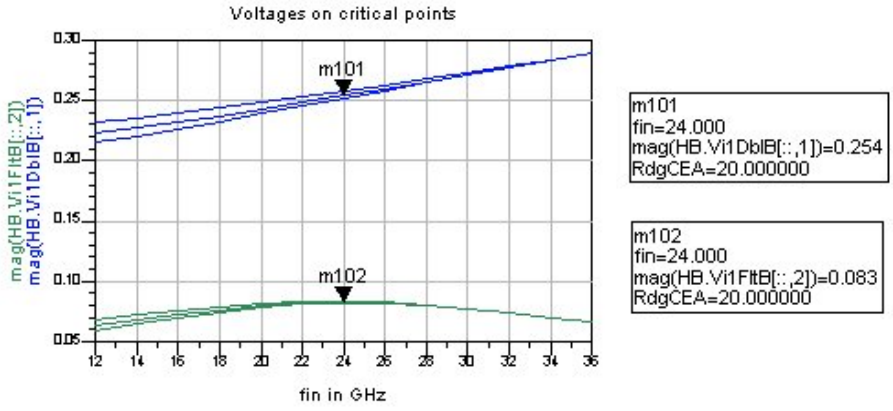


Fig 3.44 (c) Sensitivity of input signal voltage of the next doubler and filter to 15% variation of degeneration capacitor

Gain Linearity Consideration

The linearity requirement on this amplifier stage should be emphasized. With proper scaling, the emitter follower does not have to be the limiting factor. The common base stage shows better linearity than a common emitter stage for the same device size and bias current under the same input power. Because the common base stage as input buffer provides some gain, higher signal power reaches the differential pair based dual loop amplifier. We can observe that the dual loop amplifier dominates linearity.

In light of this, a trade off has to be made between the gain from the common base stage and the gain, as well as, the linearity from the dual loop amplifier. More gain stages is not so desirable here since they tend to limit the bandwidth and consume a lot more power. Our target is mainly focused on reaching a balanced point where single-stage feedback amplifier can satisfy the need for both gain peaking and necessary output power.

Voltage headroom limits the pull-up resistor value hence the voltage swing that the dual loop amplifier can generate without introducing more nonlinearity. Fig 3.45 shows the harmonic contents in the output voltage of the buffer when loaded with a linear load impedance representing the input loop of the next doubler. The input power is swept in a range of +/-3dB around the nominal value. The unwanted harmonics rises by a fair amount with increased input power mainly due to the nonlinear ic-vbe characteristic of its input differential pair transistors [31].

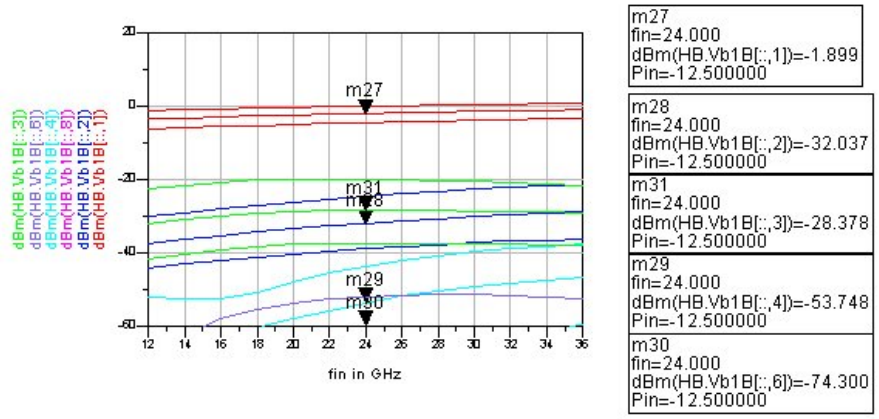


Fig 3.45 harmonic contents in the output voltage of the buffer with +-3dB power sweep

Intercept Point (eg. IIP3, OIP2) is calculated with extrapolation from small signal simulation. It is commonly used figure of merit to characterize the small signal nonlinearity of an amplifier or mixer stage. However, under large-signal operation, the actual harmonic contents do not follow the extrapolation line. As a result, IIP3 or OIP3 does not reflect the large signal nonlinearity accurately. So, instead of plotting IP3 as an indication of linearity, we plot the actual harmonic content at certain points in the circuit to evaluate the linearity performance.

Stability Check

In a negative feedback amplifier, excessive phase shift reduces the stablity margin which can lead to oscillation. As already observed from simulation about Baluns, the transistors show more excess phase shift between its input and output at higher frequencies. Other potential unstable sources include the parasitic in the current return path and negative impedance in the signal path due to frequency dependant gain. It is vital to guarantee that the circuit is stable at all frequencies, from MHz to over 100 GHz.

Transient simulation with step input is performed to check the stability performance. Since supply and ground path parasitic can affect the stability a lot. They should be included in the transient simulation. Attention should be paid especially to the single-end signal path, including doubler and balun. Before the layout is done, we first use passive components to build a network that represents these parasitic effects. In our circuit, the various stages operate at different frequencies. Considering the coupling between these stages, stability should be checked for each block, as well as, when several blocks are connected together. It must be noted that any attempt to study the stability prior to the final layout and parasitic extraction will be only an approximation.

3.3.5 Input Buffer

The input buffer has stricter constraints compared to the later stages. It should introduce low noise from its own. It should operate very linear to avoid harmonic generation. It should provide a perfect differential drive signal to the 1st doubler. Sufficient gain is necessary to drive the 1st doubler into gain compression. It should provide the necessary gain peaking to compensate the frequency response of the doubler and balun in Stage A. Wideband input impedance is required by the off chip phase shifter.

According to Friis's formula, the noise factor of a receiver is given by:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots \tag{3.6}$$

Although Friis's formula describes the noise relation in an impedance matched system which is not the case with our multiply by 8 chain. It does reveal that, when referred to the overall input, noise introduced by a certain stage is suppressed by the total gain before that stage. Regarding the multiply by 8 chain, although not too much gain is implemented to suppress the noise from latter stages so that their noise contribution can still be considerable, noise sources in Stage A is still among the top few contributors of the total additive noise. So, it is necessary to reduce the noise contribution from the input buffer.

As is discussed in section 3.2.6, in a continuous wave radar system, LO phase noise affects the receiver SNR through leakage to the receiver RF port. Since the signal up-conversion chain is part of the LO signal generator, its negative influence in terms of noise should be

minimized. Strong nonlinearity such as Ic clipping in the frequency doubler generates nonlinear transfer function for noise sources so that noise at other frequencies may also show their influence around the output signal tone. One of the most troublesome influences is the up-converted 1/f noise from very low frequency. When optimizing for noise performance, we have compared the effect of different input buffer topology on multiplier chain output signal phase noise. Based on that, the input buffer topology is chosen.

The requirement on linearity and balance comes from the fact that when improperly driven the first Doubler determines the generation of nearby odd order spurs. The mechanism is already discussed in the system level consideration part. Simulation result about the spectrum purity can be found in section 3.4.

Topology of the Input Buffer Amplifier

During the design phase several multi-stage input buffer amplifiers were build and compared in terms of input matching, noise, as well as frequency response. Here we only picked two of them to illustrate how the choice about input buffer is made. Referring to Fig 3.46, amplifier A has two stages. The first stage is a feedback amplifier with wideband input match, the second stage is an open loop amplifier. Amplifier B is a three stage amplifier. The input stage is a common base stage for wideband matching, the middle stage is a feedback amplifier and the output stage is an open loop one. The output buffer interfaces the Doubler A.

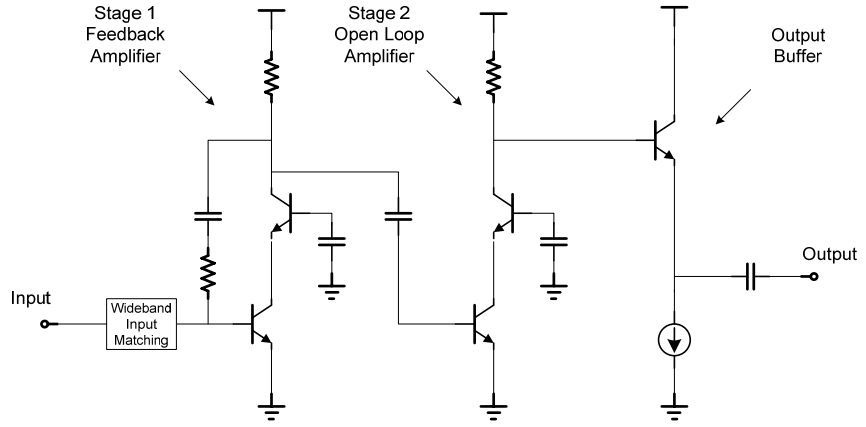


Fig 3.46(a) Topology of amplifier A

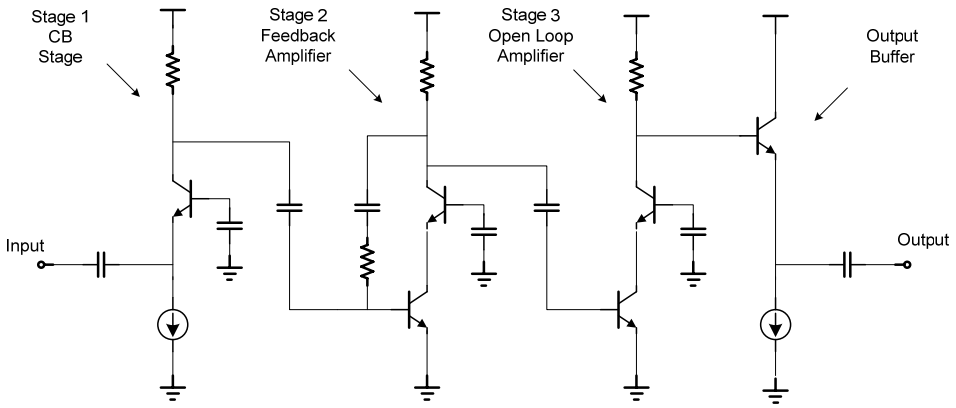


Fig 3.46(b) Topology of amplifier B

Since the output signal delivered to the first doubler is kept the same, overall gain of the buffer amplifiers is also the same. The input impedance of the doubler is a complex number. We choose its real part as the load resistance for noise figure simulation. Although this situation is different from a matched system, it serve the comparison purpose between two amplifiers.

Simulations have been done over the bandwidth, but we choose the center frequency, 12GHz, to illustrate the difference. Differential versions of these amplifiers are connected to the same multiplier chain to check their effect on the phase noise. Again we choose the center frequency for comparison, which is 96GHz at the overall output. Phase noise at several offset frequencies is compared. The results are listed in Table 3.6.

Table 3.6 Comparison of two input buffer amplifiers in terms of noise

Amplifier	Noise Figure@12GHz (single-side band, dB)	Phase Noise at multiplier chain output@96GHz(in dBc)			
		100 Hz	1K Hz	10K Hz	100K Hz
2 stage	4.7	-112	-121	-123	-123
3 stage	9.4	-111	-117.5	-118.2	-118.3

At larger offset from the carrier frequency, like 10 KHz or 100 KHz where the noise floor in phase noise dominates. There, the difference in input buffer noise figure is reflected onto the difference of phase noise. At small offsets, like 100 Hz, 1/f noise through frequency conversion dominates phase noise.

The later stages in the multiplier chain are mainly optimized for frequency response and spur suppression but not noise. To reduce excessive noise added by this multiplier chain, the input buffer should add not too much noise to the signal. So, the common base stage, which is used in later stages to provide wideband impedance match is not used at the input because of its difficulty to provide simultaneous noise and impedance match.

A one stage amplifier is used to provide around 20dB of gain before Doubler A. A passive network is utilized at the input for wideband impedance matching. The amplifier is based on differential cascode structure. It includes input matching network, shunt feedback, resonant load as well as emitter follower to drive the 1st doubler. The topology of the input buffer is plotted in Fig 3.47. Only half of the differential amplifier is shown.

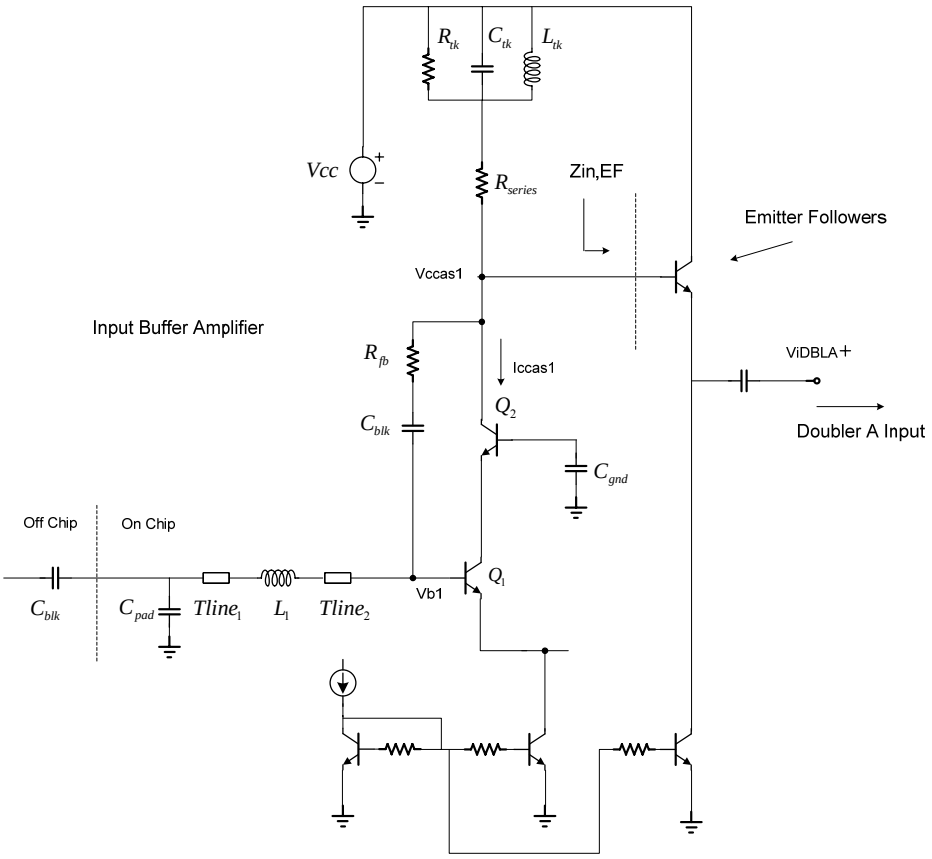


Fig 3.47 Half circuit of input buffer amplifier

Limitation on bias current due to resistive load limits the bias of transistors. Around 12GHz, the input impedance of the differential pair has a large capacitive part so that the input reflection coefficient is close to the edge of the smith chart. Although this input impedance still lies in a low Q region (with Q factor about 2.5 on smith chart), it requires several nH of inductance to build the wideband input matching network. The on chip inductor providing about 2nH has a self resonant frequency at about 20GHz, which is not high enough for our operation. So, in order to achieve wideband matching with a simple matching network and low inductance values, shunt feedback was added to modify the input impedance. The S11 trajectory from 10GHz to 14GHz with and without the shunt feedback branch is shown in Fig 3.48.

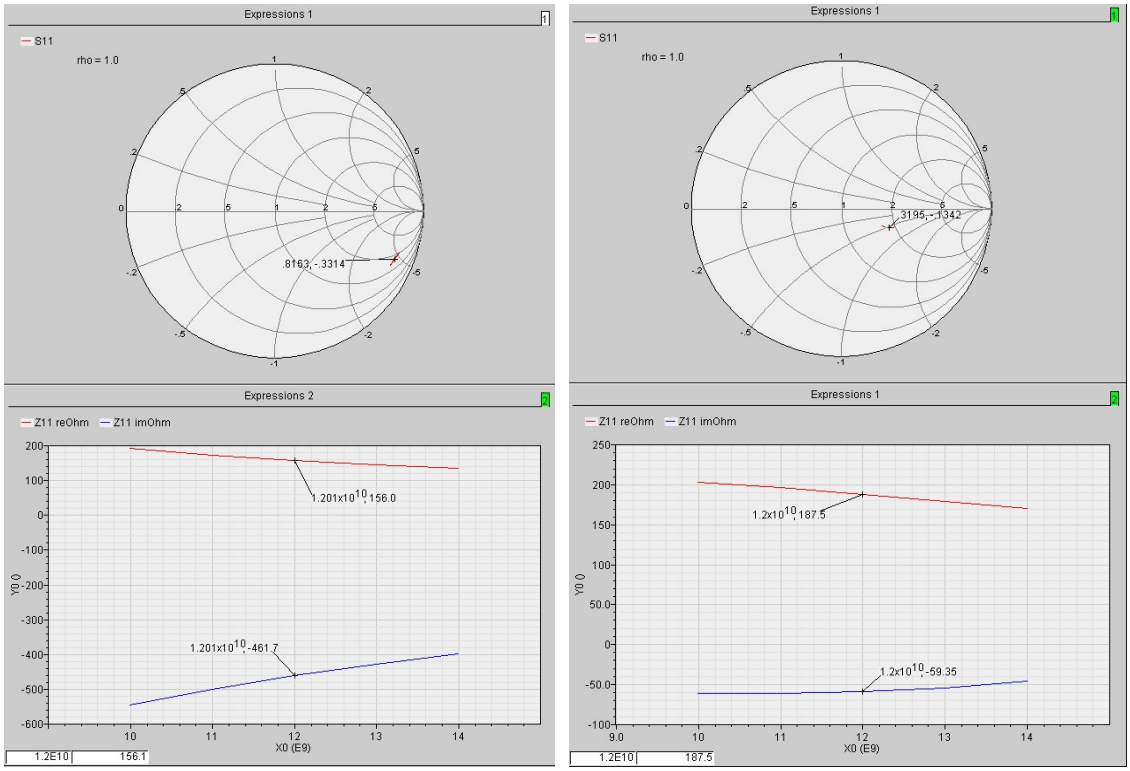


Fig 3.48 Input impedance of differential pair with and without the feedback resistor

The feedback resistance is chosen relatively large, 1K Ohm, for two reasons. First, modify the input impedance to a convenient value for wideband matching; and second, lower the noise introduced by this resistor. Phase noise simulation shows that the 1K Ohm feedback resistor ranks it outside the top 30 noise contributor to the output phase noise of the multiplier chain. Reduction of the feedback resistance value increases its noise contribution.

The impedance values in Fig 3.48 show that the resistive part of input impedance does not change much, on the other hand, the capacitive part reduced a lot. At 12GHz, it reduced from –j*462 to –j*59. This reduction can be explained with small signal model analysis of the feedback amplifier. For simplicity, a simple model of CE stage is used for the amplifier. The effect of C_u is greatly reduced due to the cascode, so it is omitted. The model for calculation is shown in Fig 3.49.

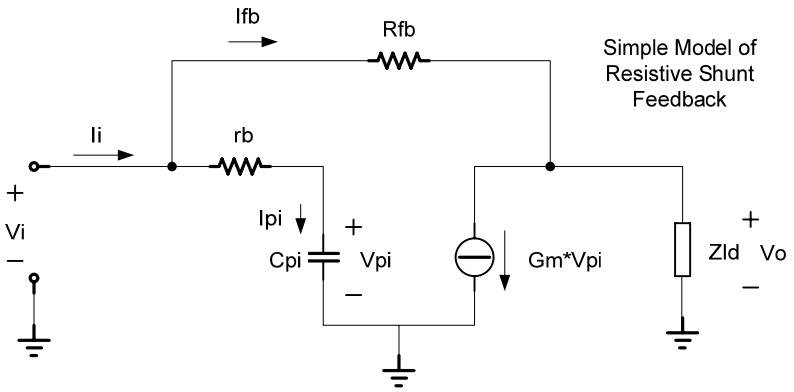


Fig 3.49 Simple model for resistive shunt feedback input impedance analysis

We apply a voltage source Vi at the input. Without the feedback resistor R_{fb}, we have

$$I_i = I_\pi = \frac{j\omega c_\pi}{1 + j\omega r_b c_\pi} V_i = \left(\frac{\omega^2 r_b c_\pi^{\,2}}{1 + (\omega r_b c_\pi)^2} + j * \frac{\omega c_\pi}{1 + (\omega r_b c_\pi)^2}\right) V_i \tag{3.7}$$

The equivalent capacitance for the capacitive part of input impedance is $C_{eq} = \frac{c_\pi}{1 + (\omega r_b c_\pi)^2}$.

When the feedback resistor is included, the input current $I_i = I_\pi + I_{fb}$, in which

$$I_{fb} = \left(\frac{1}{Z_{ld} + R_{fb}} - \frac{g_m Z_{ld}}{(Z_{ld} + R_{fb}) * [1 + (\omega r_b c_\pi)^2]} + \frac{g_m Z_{ld}}{Z_{ld} + R_{fb}} * \frac{j\omega r_b c_\pi}{1 + (\omega r_b c_\pi)^2} \right) V_i \tag{3.8}$$

In this case, the equivalent capacitance for the capacitive part of input impedance is

$$C_{eq} = \frac{c_\pi}{1 + (\omega r_b c_\pi)^2} * \left(1 + \frac{g_m r_b}{1 + \frac{R_{fb}}{Z_{ld}}} \right) \tag{3.9}$$

We can see that additional current flowing through the feedback resistance causes the equivalent input capacitance to increase by a factor of $1 + \frac{g_m r_b}{1 + \frac{R_{fb}}{Z_{ld}}}$.

Although this model is over simplified, it shows the effect of increasing the input capacitance. Note that in the above expression, load impedance at the collector Z_{ld} is treated as a resistance. If it contains reactive components, the expression for equivalent capacitance will change. As for the input buffer, although a resonant tank is used at the collector, the resistive part dominates the load impedance. So, the above analysis still reflects the influence of R_{fb} to certain extent.

With the help of this resistive feedback, much lower value of inductance is needed to implement the wideband input matching. About 800pH of inductance and 500um of transmission line are used. The input matching network also takes into account the input RF pad capacitance. Since the ESD diodes introduce too much capacitance to be absorbed by the matching network, MIM capacitance can not be used here as a DC block. The DC block can be either off chip or using a custom layout with metal layers. Fig 3.50 shows the input reflection coefficient after input matching.

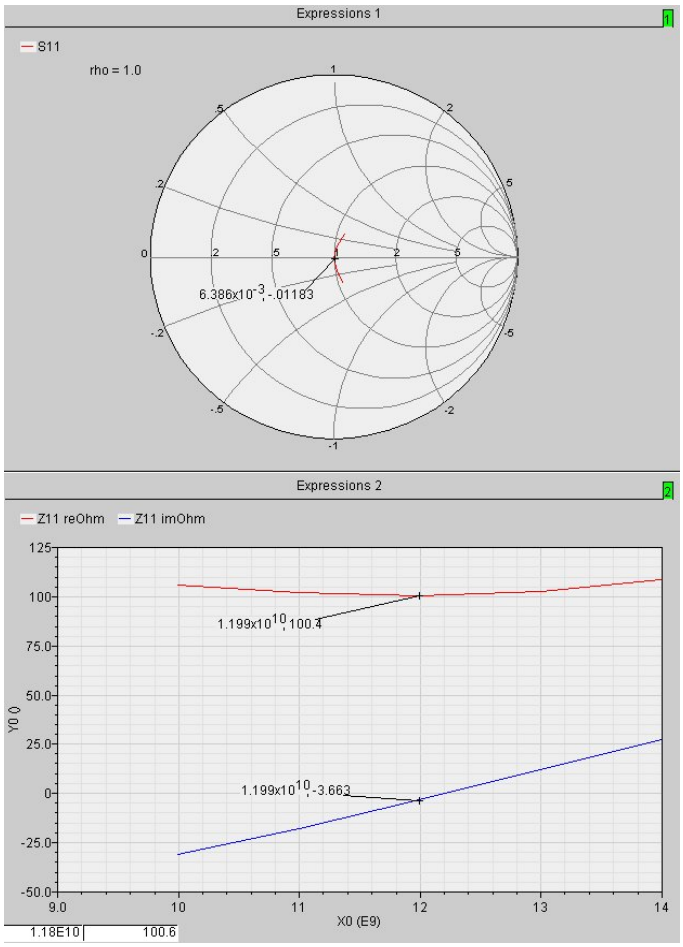


Fig 3.50 Input impedance of input buffer from 10GHz to 14GHz after input matching

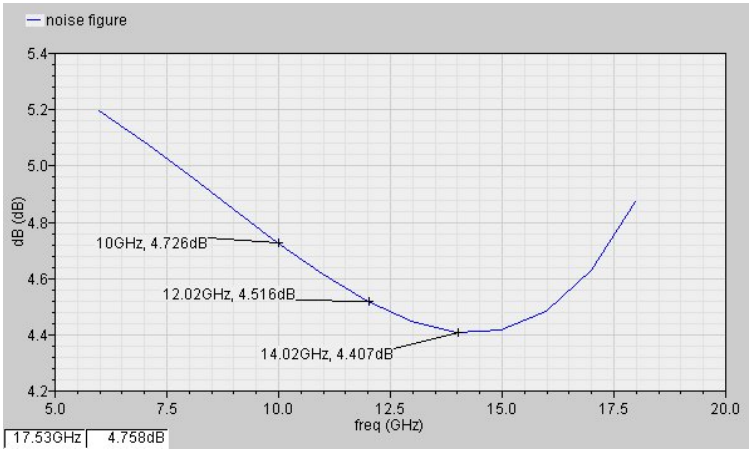


Fig 3.51 Noise figure of input buffer

The input matching network is designed for impedance matching. In terms of noise, it is not the best choice. Simulation of the differential input buffer alone shows inband noise figure varies from 4.7dB to 4.4dB, referring to Fig 3.51. The base contact resistance contributes a large portion of additive noise. Unless the transistors are scaled up a lot, this resistance still dominates noise contribution, which should be improved next.

RLC Resonant Load Frequency Compensation

The bias current is mainly limited by the voltage headroom and the resistive load at the collector of cascode transistor. In fact, this topology is inspired from the wideband LNA work by Ismail and Abidi [32]. They have utilized degeneration and input matching network to build a band pass filter like structure for wideband input matching. Inductive peaking at the output is used to compensate for a flat frequency response. In our input buffer, wideband input matching is achieved by moving the starting point of input impedance closer to 50 Ohm. To have the required gain response, some sort of passive peaking is necessary at the output. However, at this frequency, an inductor alone is not sufficient to provide the peaking we need. So, we choose to use an RLC parallel resonant tank to do this job. The value of tank inductor and capacitor determines the resonant frequency while the tank resistor and the series resistor tune the Q factor hence the slope of frequency response near resonance. The resonant frequency is put beyond our input frequency band, at about 17GHz. As a result, the gain of the input buffer keeps increasing within 10 to 14 GHz. An emitter follower is used for transforming the input impedance of the succeeding doubler to a higher value to lower the loading on the resonant tank.

Actually, the tank inductor on two branches of the differential pair is implemented with a symmetrical inductor, as shown in Fig 3.52. Due to differential excitation, the effective impedance through the current return path is doubled [33]. This improves the parallel resonator such that even with on-chip passive components it shows a frequency response, which approximates that of ideal components. The symmetrical inductor makes it possible to realize the passive signal peaking. Fig 3.53 shows the comparison of input impedance frequency response of the differential RLC resonant tank with ideal and actual components. The influence of the interconnection parasitic has been taken into account, layout of the symmetrical inductor is devised to minimize the interconnection in series with the tank capacitor and resistor. These interconnections are modeled with inductors. Since the topology is fully differential, parasitics in the ground path does not affect the performance.

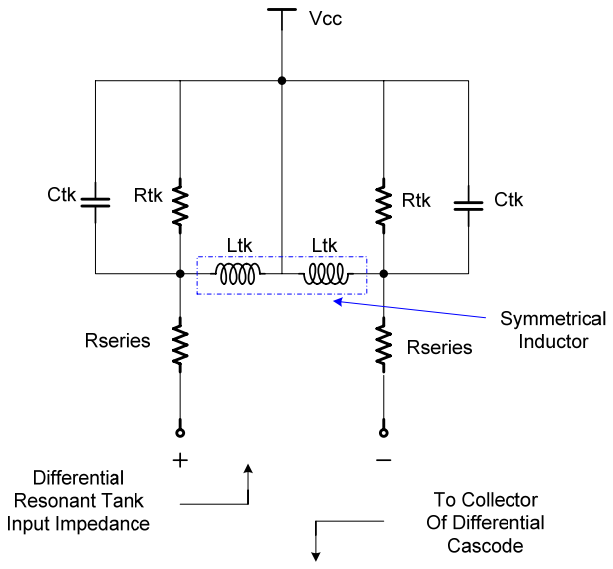


Fig 3.52 Structure of the differential RLC parallel resonant tank

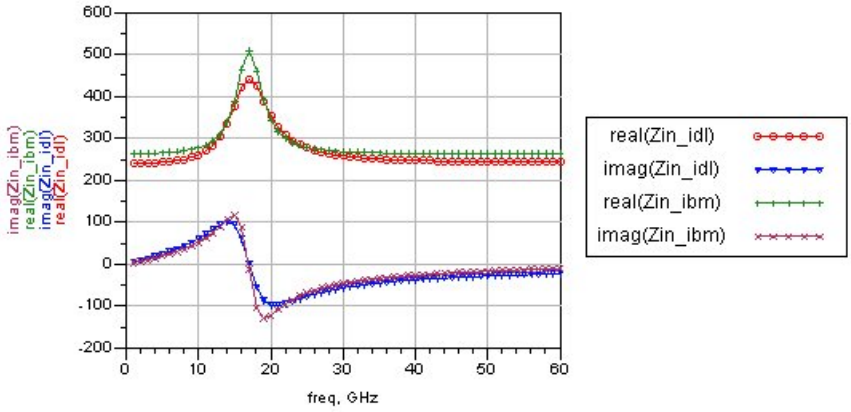


Fig 3.53 Comparison of input impedance of the differential RLC resonant tank with ideal and actual on-chip components

One pleasant side-effect of using symmetrical inductor is that it differentiates between common mode an differential mode excitation due to self coupling. The effective inductances to common mode and differential mode are different. As a result, for the common mode signal, the resonant frequency is at a different frequency, probably higher in this case, than that to the differential signal. This effect should improve CMRR, although due to the relative low coupling coefficient of the on-chip component, the improvement is limited.

Input referred 1dB compression point of the input buffer is shown in Fig 3.54. Differential input power is checked here. The an RC series branch representing the input impedance of Doubler A at 12GHz is used as load impedance. Simulation shows that 12GHz gives the worst case compression point for input buffer. Since the actual input impedance of the frequency doubler changes with frequency, the output power calculated here is not accurate. Input referred 1dB compression point is about -15dBm, the nominal input power is -17dBm.

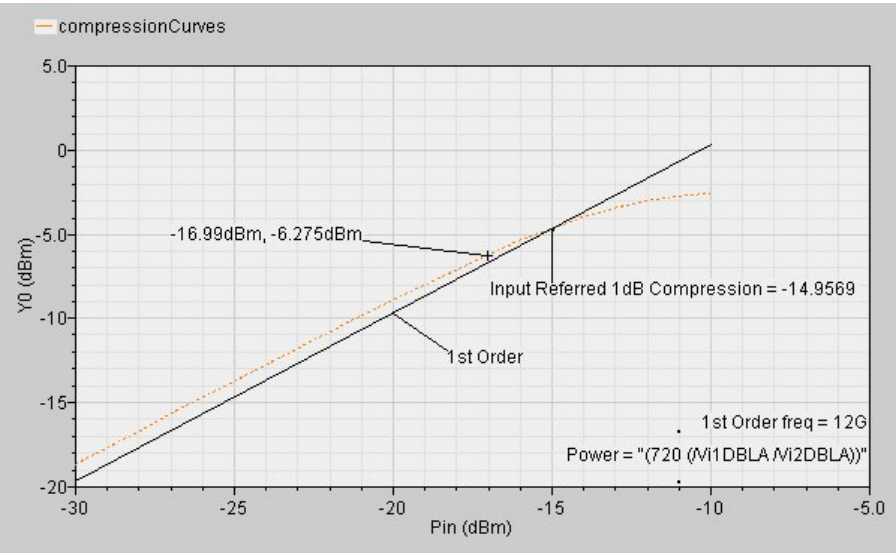


Fig 3.54 1dB input referred compression point of input buffer loaded with RC load

3.4 Circuit Performance

In the forgoing sections, we have discussed the design considerations of the Multiply by 8 Chain. In this section, we check the performance of each subcircuit part, Stage A, B and C as well as the overall performance of the multiply by 8 chain. Passive network representing the supply and ground parasitic and decoupling branches are included. Short segments of transmission line are added in certain signal path to account for loss from interconnection. Filter A is implemented with actual passive components. Filter B is made up with actual components except for the small value series capacitor. Both filters approximate the ideal filter frequency response with passband insertion loss varying from about 2.5dB to 3.5dB.

3.4.1 Performance of Each Stage

3.4.1.1 Stage A

Simulation results about Stage A are shown here. Fig 3.55 shows the signal voltage at several points in the Stage A. It is shown that peaking from Buffer A compensates the frequency response roll off mainly from Balun A. The input signal to Filter A is kept roughly flat from 10GHz to 14GHz.

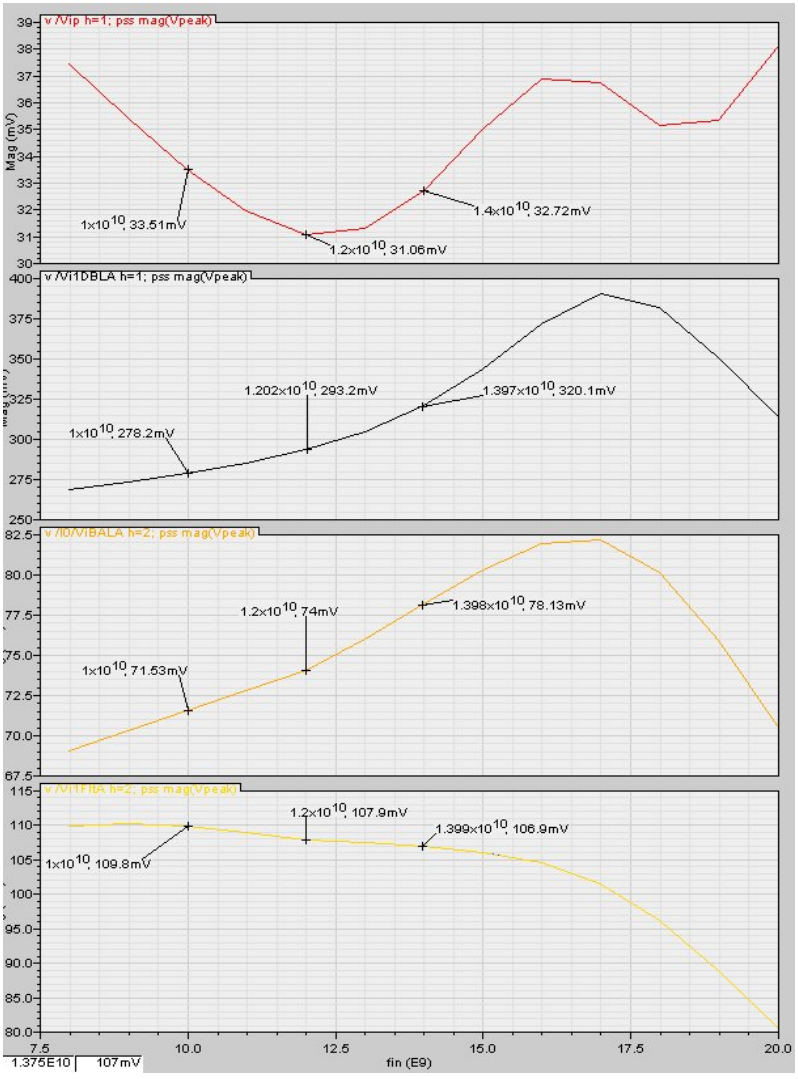


Fig 3.55 Signal voltage at several points in Stage A

Fig 3.56 shows the amplitude and phase unbalance of signal that is delivered to the input of Filter A. Result shows that the active balun reduces the unbalance of two output signal to a low extent.

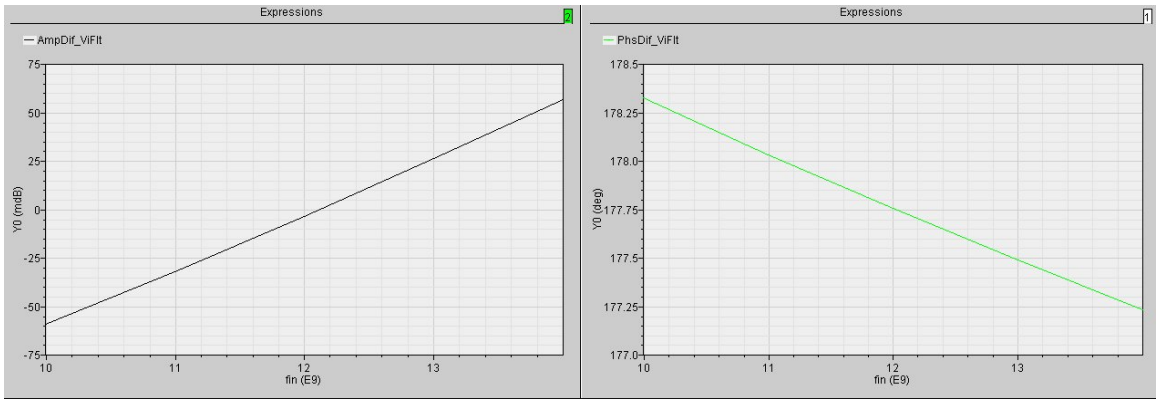


Fig 3.56 Amplitude and phase unbalance of signal at the input of Filter A

3.4.1.2 Stage B

Simulation results about Stage B are shown below. Fig 3.57 shows the signal voltage at several points in the Stage B. It is shown that peaking from Buffer B compensates the frequency response roll off mainly from Balun B.

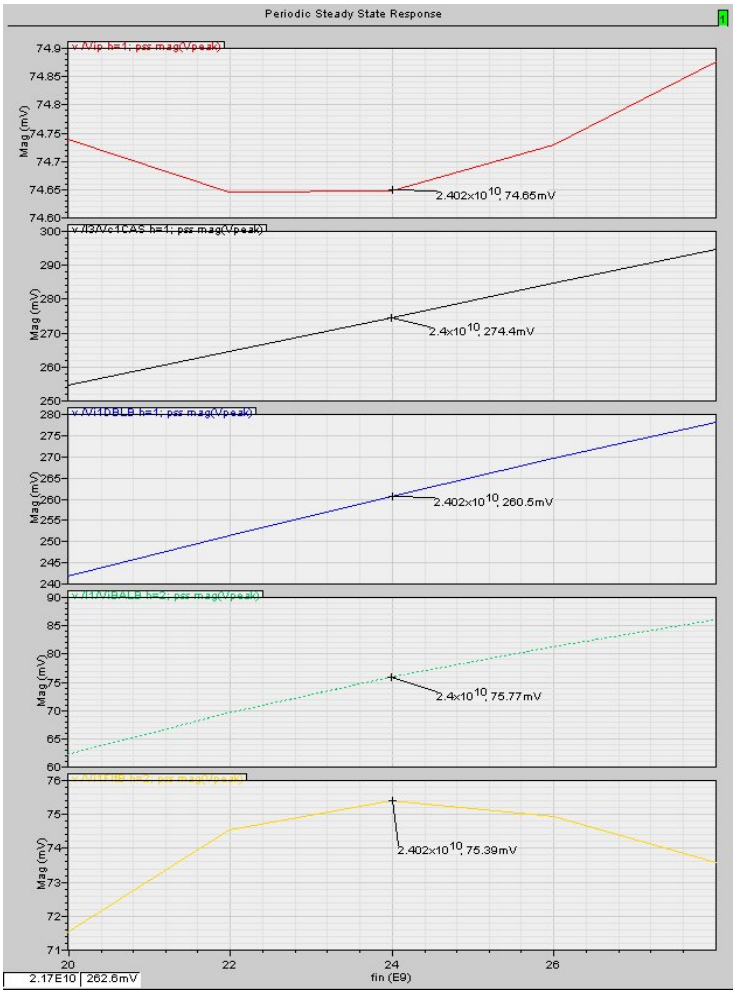


Fig 3.57 Signal voltage at several points in Stage B

Fig 3.58 shows the amplitude and phase unbalance of signal that is delivered to the input of Filter B. Result shows that although the balance performance is not as good as at lower frequency, the unbalance within the band from 40GHz to 56GHz is still reasonably low.

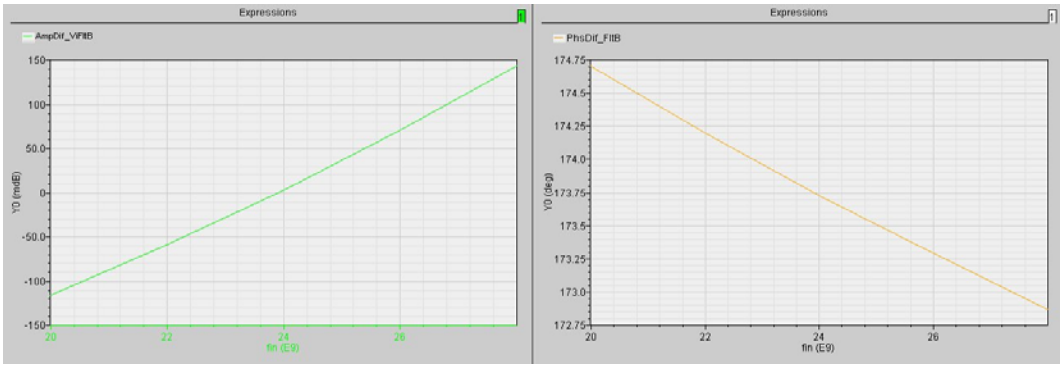


Fig 3.58 Amplitude and phase unbalance of signal at the input of Filter B

3.4.1.3 Stage C

Stage C consists of Buffer C and Doubler C. The output of Doubler C is impedance matched to 50 Ohm with passive elements. Fig 3.59 shows the signal voltage at several points in Stage C. Doubler C is optimized for high output power.

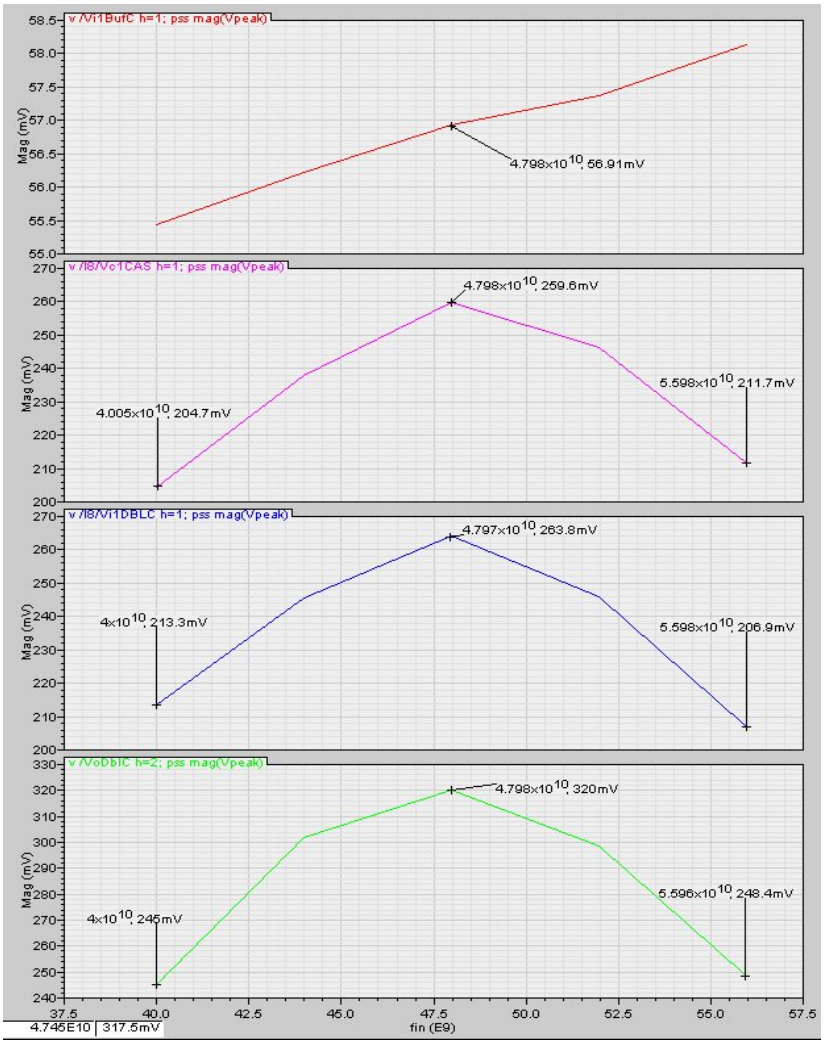


Fig 3.59 Signal voltage at several points in Stage C

Due to higher output impedance from the cascode transistor, output matching network causes 2dB inband gain variation to output signal. It is also shown that peaking from Buffer C as well as the output matching shapes the overall frequency response of this stage.

3.4.2 Performance of Multiplier by 8 Chain

The Multiply by 8 Chain draws 76mA from a 3.8V supply. The DC power consumption is 289mW. Simulation results with the multiply by 8 chain are shown below. All the DC bias points are connected through a passive network that models the supply lines. We will see the influence of interstage coupling through supply lines.

3.4.2.1 Frequency Sweep and Power Sweep

The input signal is set intentionally with 0.3dB of amplitude unbalance and 5 degree of phase unbalance.

Fig 3.60 shows the amount of real power that is delivered into and out of each doubler stage during an input frequency sweep. 5 input frequency points are chosen for simulation (10GHz, 11GHz, 12GHz, 13GHz, 14GHz). Tones on harmonic frequency from f0 up to 10f0 are shown. The input power is calculated at single-end, there should be 3dB increment for total differential input power.

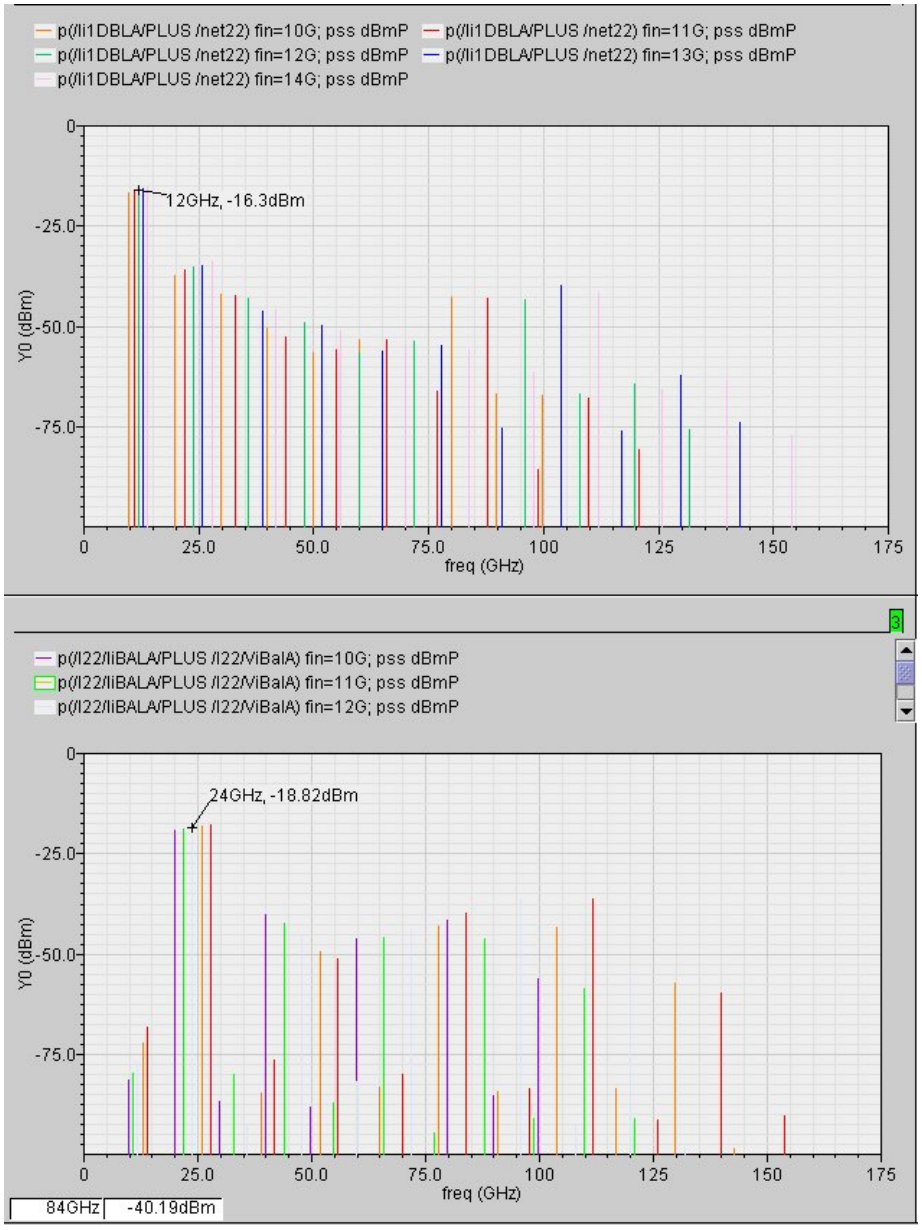


Fig 3.60(a) Power delivered in and out of Doubler A

Fig 3.60 (a) shows that considerable unwanted higher spurs exist at the input and output of Doubler A. Significant spur on 8f0 (near 100GHz) is coupled back from the supply path. Doubler A shows more than 5dB conversion loss, which is intended since the succeeding Balun determines this low output power from the Doubler.

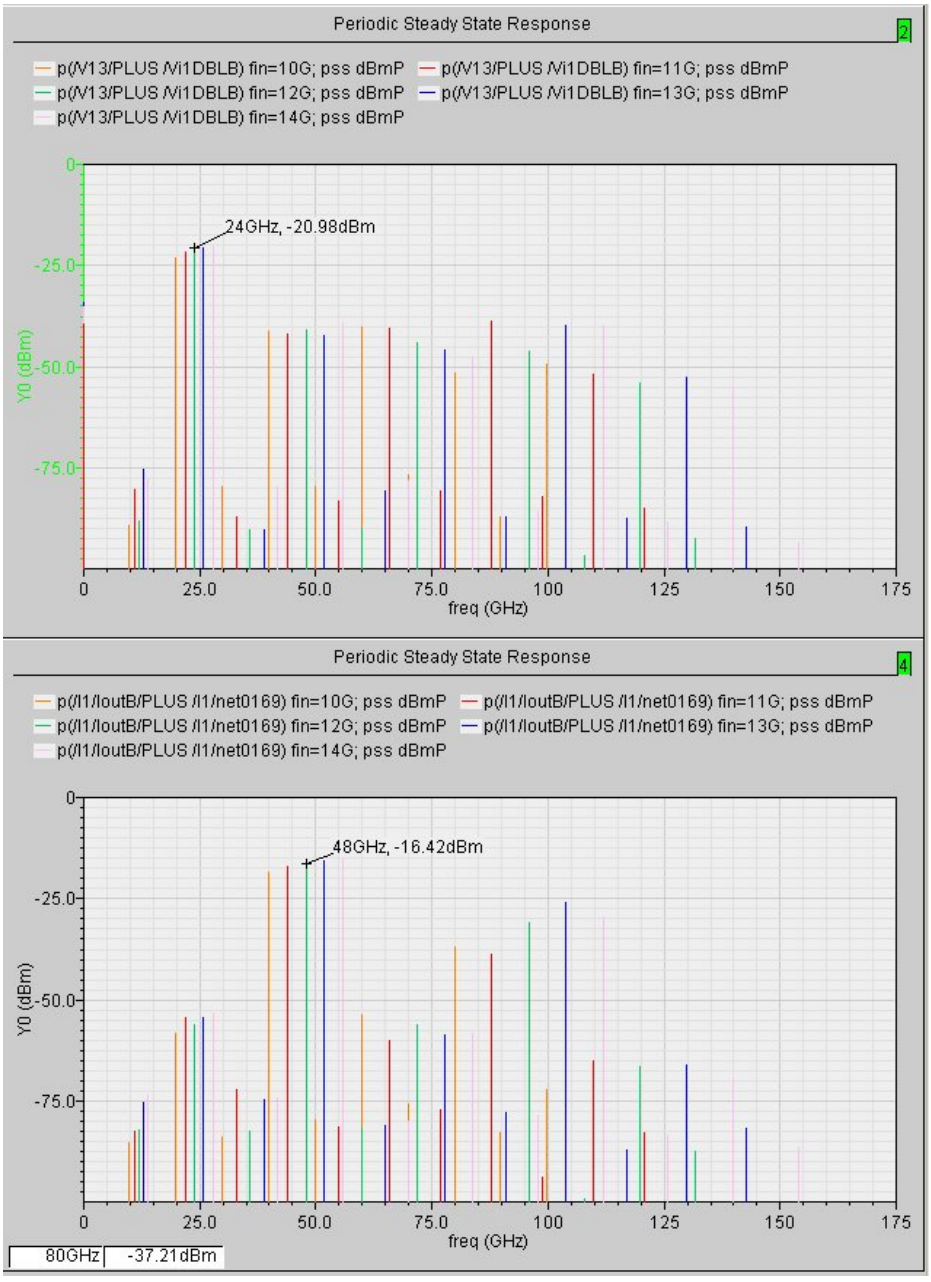


Fig 3.60(b) Power delivered in and out of Doubler B

Fig 3.60 (b) shows that considerable unwanted spurs exist at the input and output of Doubler B. The spurs on 8f0 (near 100GHz) are stronger than expected mainly due to feedback. Doubler B shows about 1.5dB conversion gain. It is not optimized for high output power, but optimized for adequate gain peaking.

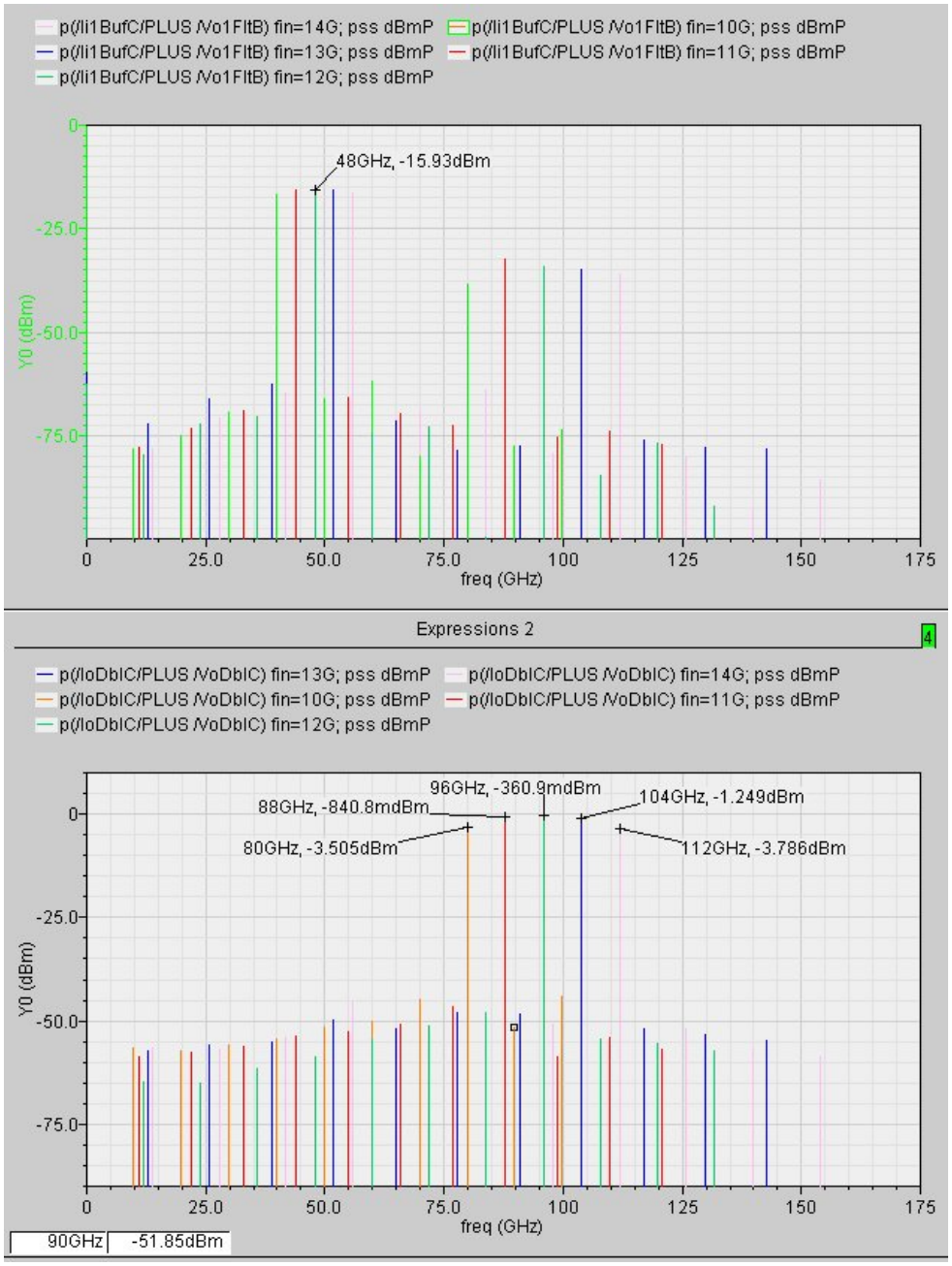


Fig 3.60(c) Power delivered in and out of Doubler C

Fig 3.60 (c) shows that considerable spurs on 8f0 exist at the input of Doubler C. At the output, most of the nearby spurs are at least lower than -45dBm. The output signal power varies from -3.8dBm to -0.4dBm. Conversion gain of Doubler C varies roughly from 12dB to 15dB. Doubler C is optimized for high output power as well as flat frequency response.

Fig 3.61 shows the harmonic contents in signal voltage at the output of three doublers during a frequency sweep. The x-axis shows the input frequency range. Tones on harmonic frequency from f0 up to 10f0 are shown in the plot. Due to feedback from supply line, high 8f0 component appears at the output of Doubler A and B, which is not predicted when these stages are simulated separately. At the output of Doubler C, spurs on 6f0, 7f0, 9f0 and 10f0 may appear in the output band from 80GHz to 112GHz for some input frequency range. Section 3.2.3 has an illustration of the spurs that may appear at the output.

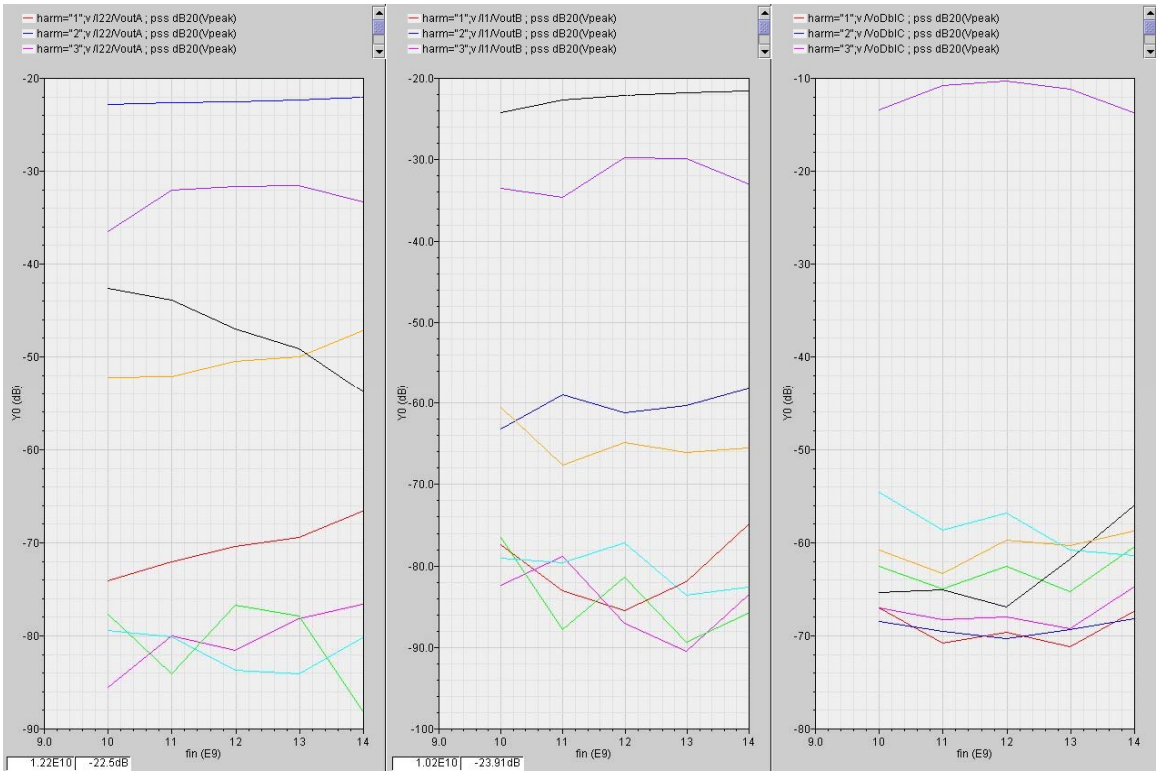


Fig 3.61 Harmonic contents at the output of 3 doublers

The output spectrum of Doubler C within +/- 6dB input power variation is plotted in Fig 3.62.

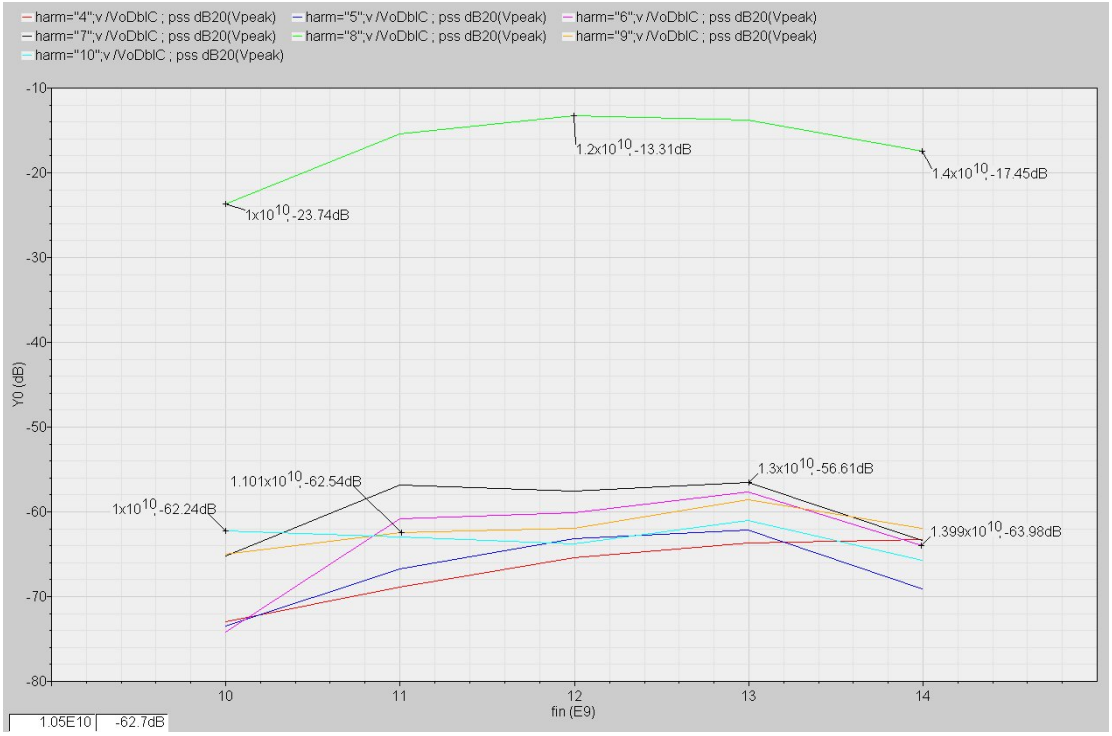


Fig 3.62(a) Spectrum components at the output of Doubler C with -6dB input power(-26dBm)

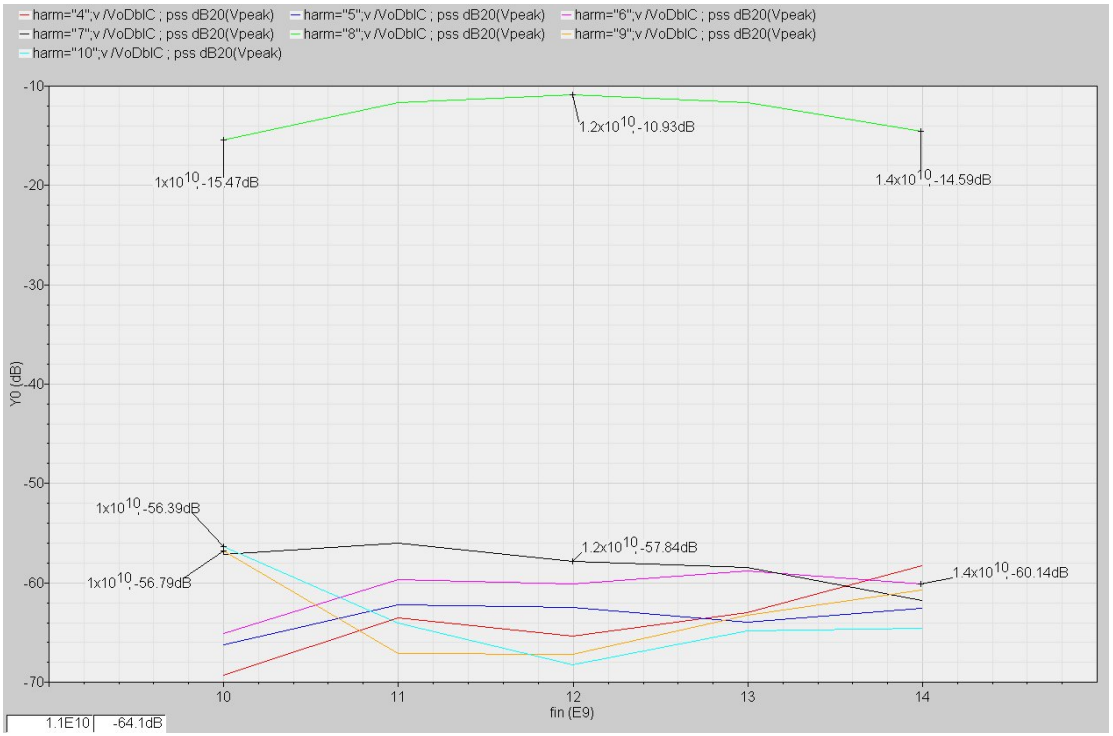


Fig 3.62(b) Spectrum components at the output of Doubler C with -3dB input power(-23dBm)

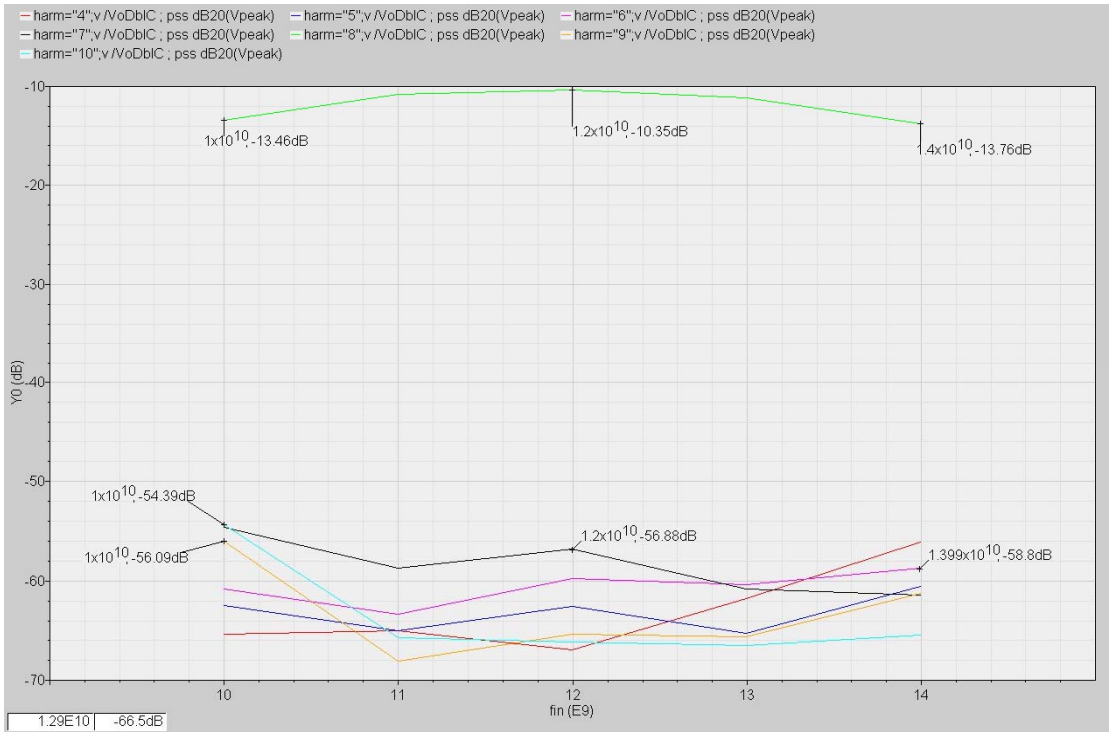


Fig 3.62(c) Spectrum components at the output of Doubler C with nominal input power (-20dBm)

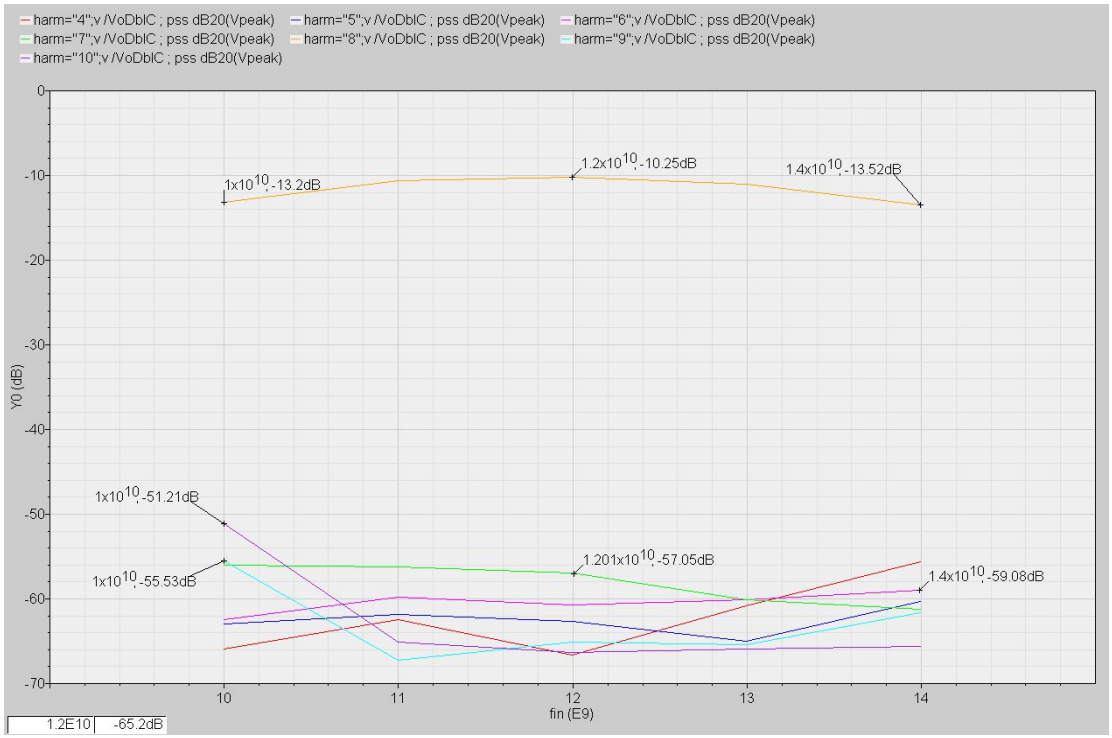


Fig 3.62(d) Spectrum components at the output of Doubler C with +3dB input power(-17dBm)

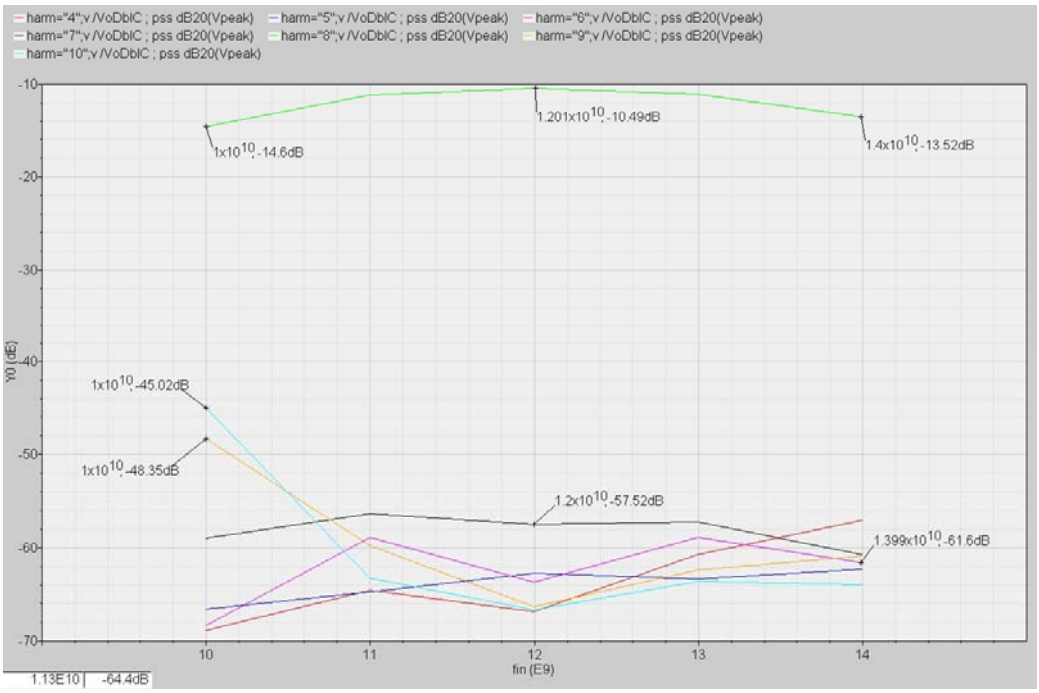


Fig 3.62(e) Spectrum components at the output of Doubler C with +6dB input power(-14dBm)

Markers show that desired output signal at 8f0 has roughly 3 dB inband variation. In the buttom part, markers show the absolute worst case of spurs on 6f0, 7f0, 9f0 and 10f0, which is the strongest spur that may appear in the output signal band. Better than 40 dB nearby spur suppression is achieved across the whole band in this case. We also observe that due to unbalanced input signal, the odd order nearby harmonics (7f0 and 9f0) are on the same order or even stronger than the even order nearby harmonics (6f0 and 10f0). Coupling through supply line also cause the degradation of spectrum purity.

Unwanted in band spurs on 9f0 and 10f0, rise higher near the lower edge of the signal band. The spurs on 6f0 and 7f0 rise higher near the upper edge of the signal band. This is due to the fact that the frequency components which generate these tones fall partly in the pass band of the filters used in the multiplier chain.

It can be observed that when the input power level is increased above nominal value, spurs on 9f0 and 10f0 rises more significantly compared to other harmonics. This is because the input buffer generates stronger harmonics with higher input power. Under the excitation of multiple harmonic tones, the first Doubler generates stronger odd order harmonics. These tones mix with other even order harmonic tones so that stronger nearby odd order harmonics appear.

Fig 3.63 shows the spectrum components at the output of Doubler C during input power sweep. 0.3dB amplitude unbalance and 5 degree phase unbalance are assumed at the input. Three output frequencies at the band center and edges (80GHz, 96GHz and 112GHz) are chosen for comparison. The plotted components include those from the f0 (10GHz, 12GHz and 14GHz) to 10f0(100GHz, 110GHz and 112GHz).

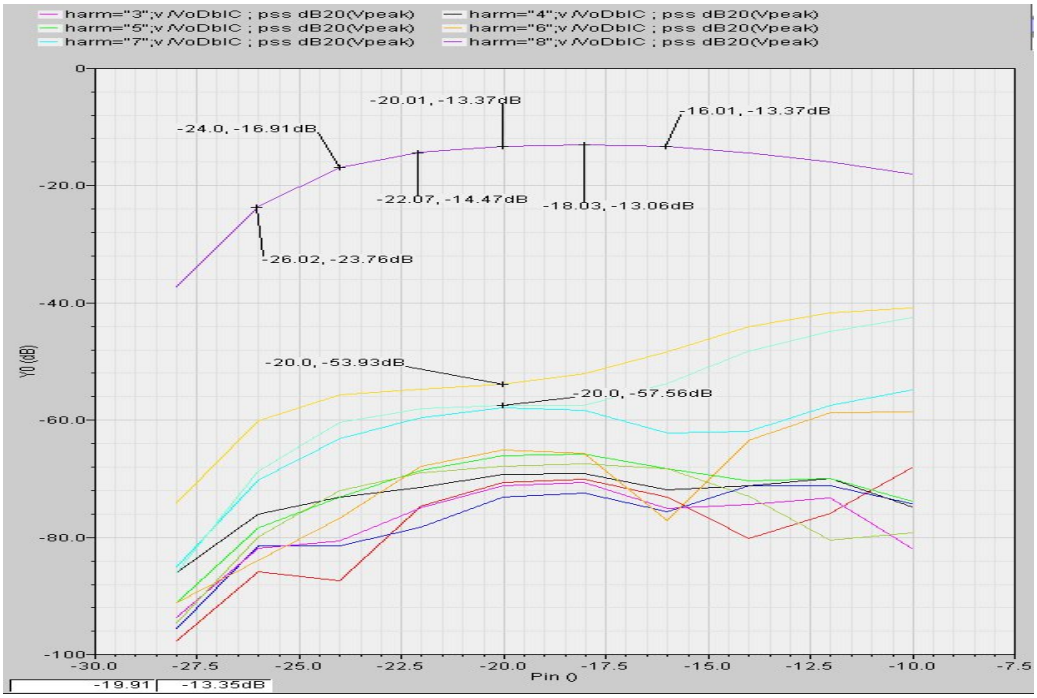


Fig 3.63(a) Spectrum components at the output of Doubler C at 80GHz

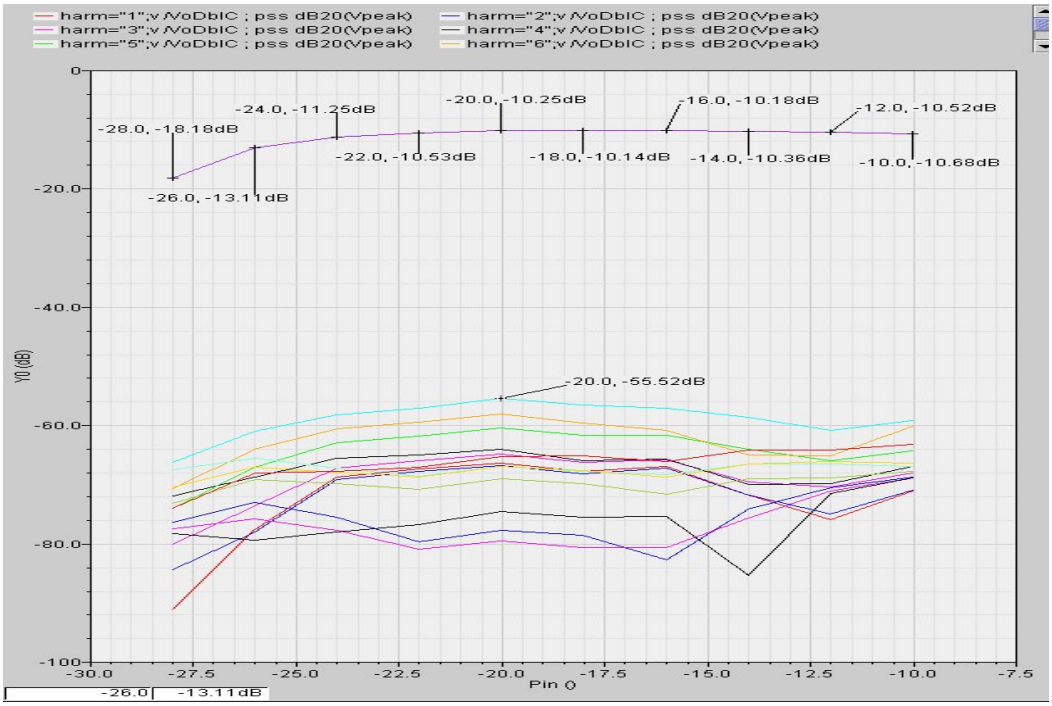


Fig 3.63(b) Spectrum components at the output of Doubler C at 96GHz

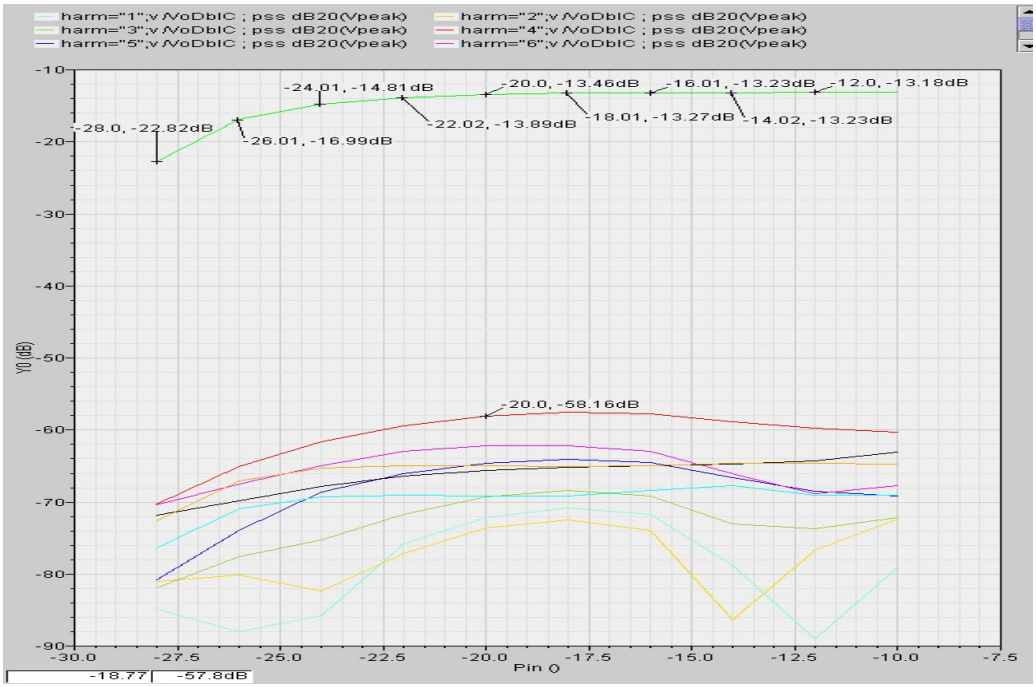


Fig 3.63(c) Spectrum components at the output of Doubler C at 112GHz

Looking at the output spectrums at these three frequencies, we can see that gain compression is achieved at all three frequencies. However, the output at the band center varies for the least amount over power sweep. Comparing the output spectrum at two band edges, the one at the lower edge varies more than at higher edge. This is because the signal at lower band edge along the multiplier chain is suppressed to render a flat overall frequency response. It is not a surprise that when input power is lowered, the multipliers operate out of the gain compression region more quickly at this frequency. It is confirmed that unwanted in band spurs, such as the one on 9f0 and 10f0, rise higher near the lower edge of the signal band. Likewise, spurs on 6f0 and 7f0 rise higher near the upper edge of the signal band.

For completeness, Fig 3.64 shows the output signal voltage and current value on 8f0. These numbers are used to determine the input signal condition of the succeeding circuit blocks working in W band.

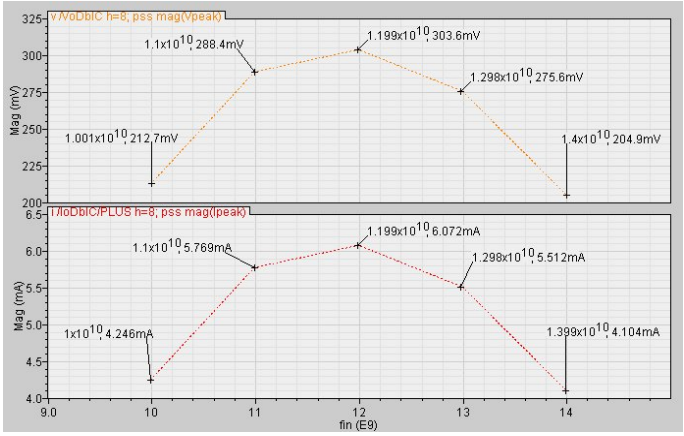


Fig 3.64 Output voltage and current from the multiply by 8 chain

3.4.2.2 Transient Simulation

Transient simulation shows the signal waveform at the output nod of three doublers. Single tone input simulation at 12GHz is shown in Fig 3.65(a). Fig 3.65 (b) zooms in to narrower time interval. It shows that the waveform of output voltage at the first two doublers contain substantial amount of higher harmonics, mainly the 8^{th} harmonic.

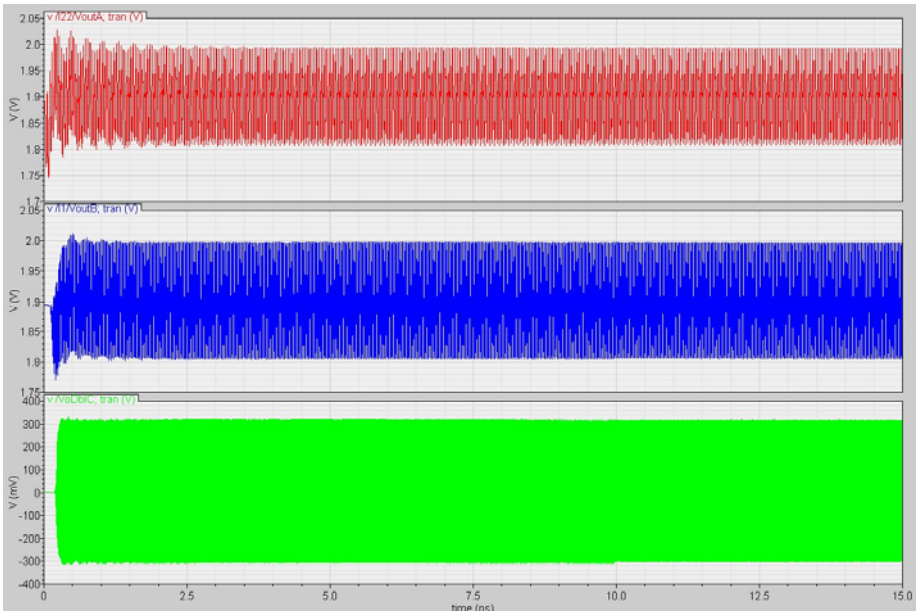


Fig 3.65(a) Output voltage waveform at the output nod of three doublers

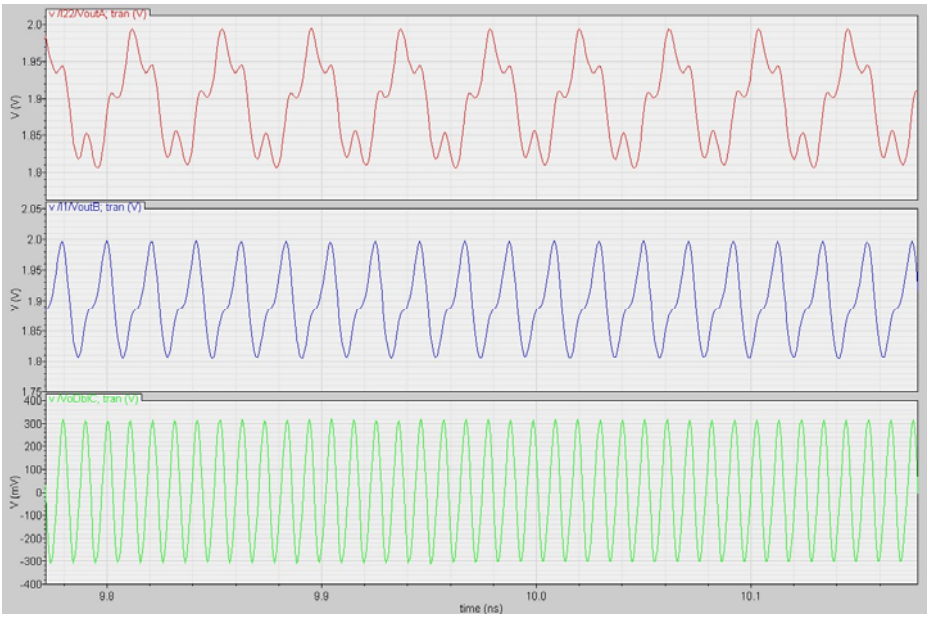


Fig 3.65(b) Output voltage waveform at the output nod of three doublers(zoom in)

Step input signal is applied to check stability of the multiplier chain. Fig 3.66 shows that oscillation at the output of Doubler B damps slowly. The frequency of oscillation is below 5GHz, which can be caused by not perfect supply decouple. This should be given full attention in the latter design steps.

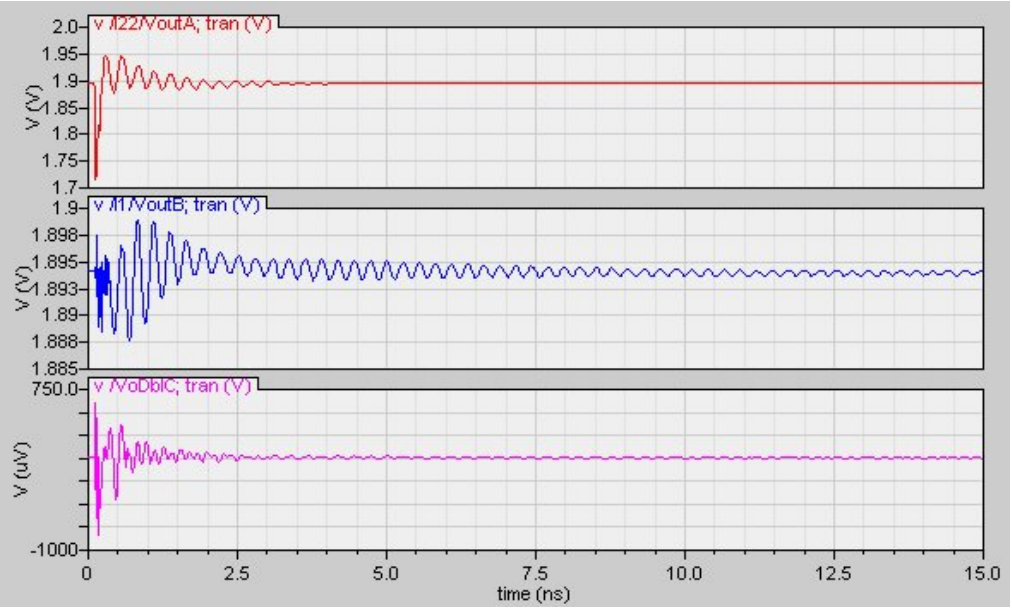


Fig 3.66 Step response at the output nod of three doublers

3.4.2.3 Noise Simulation

Noise simulation of the multiply by 8 chain is performed with ADS, some of the passive components used are ideal. Difference is expected between the results here and the actual noise performance of the up-conversion chain. It illustrates how excessive phase noise affects the output phase noise spectrum.

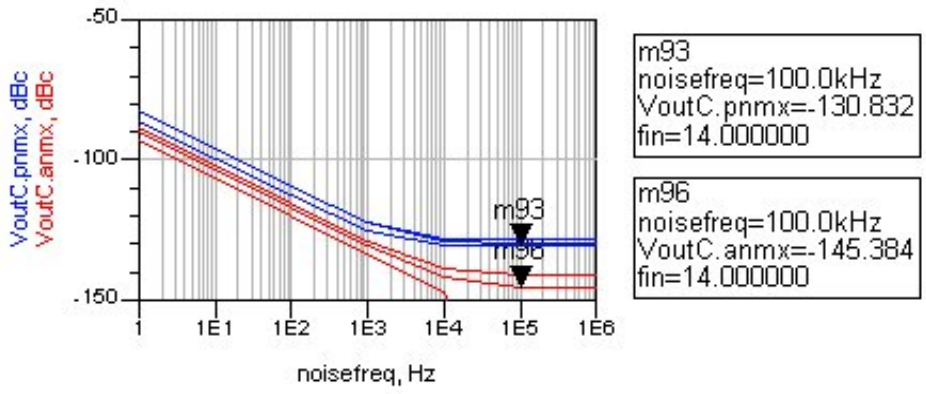


Fig 3.67 Output PM and AM noise of the Multiply by 8 Chain

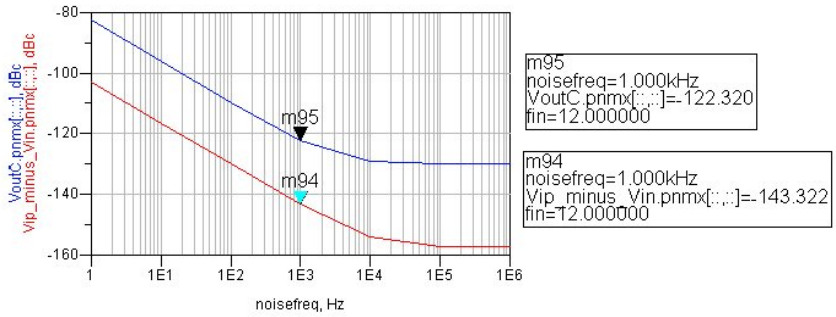
Fig 3.67 shows the output PM and AM noise of the Multiply by 8 Chain. The input carrier frequency is chosen at 10GHz, 12GHz and 14GHz. The corresponding output carrier frequency is at 80GHz, 96GHz and 112GHz. Three curves in each color represent the noise side bands around those carrier frequencies. In this case, all the noise comes from the noise sources within the multiply by 8 chain.

Results show that AM noise is relatively lower than PM noise. However the difference is not so large to claim that phase noise dominates the output noise sideband. Probably that is because the gain compression effect in multipliers is not as strong to clamp the signal magnitude as the amplitude limiting mechanisms normally found in oscillators. Still, the AM noise floor is about 15dB lower than the PM noise floor.

In the following simulations, we focus on the phase noise sideband. Input carrier frequency is chosen at 12GHz. Different phase noise sideband is specified for the input signal source at 12GHz. The source phase noise strength at different offset frequencies used for simulation are listed in Table 3.7

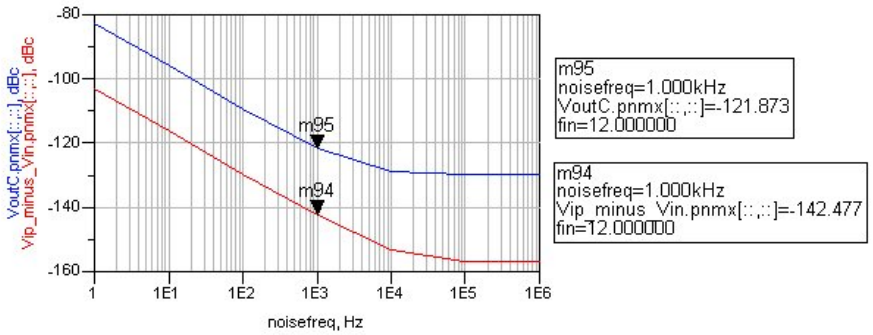
Table 3.7 Signal source phase noise configuration for several simulations

Configuration Number	Offset Frequency (Hz)/Phase Noise(dBc)					
	10	100	1K	10K	100K	1M
1	0	0	0	0	0	0
2	-130	-140	-150	-160	-170	-170
3	-100	-110	-120	-130	-140	-140
4	-90	-100	-110	-120	-130	-130



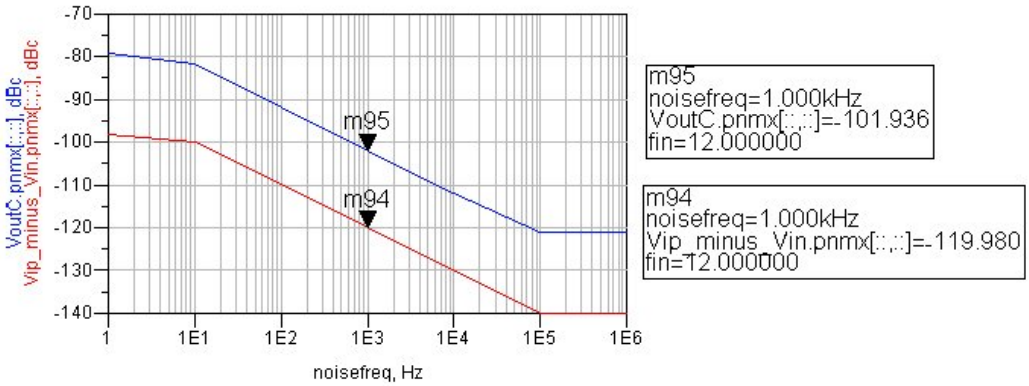
noisefreq	VoutC.pnmx fin=12.000	Vip_minus_Vin.pnmx fin=12.000	...ip_minus_Vin.pnmx fin=12.000
1.000 Hz	-82.68 dBc	-103.0 dBc	20.320
10.00 Hz	-96.18 dBc	-116.5 dBc	20.321
100.0 Hz	-109.6 dBc	-130.0 dBc	20.354
1.000 kHz	-122.3 dBc	-143.3 dBc	21.003
10.00 kHz	-129.0 dBc	-154.1 dBc	25.152
100.0 kHz	-129.7 dBc	-157.0 dBc	27.315
1.000 MHz	-129.8 dBc	-157.2 dBc	27.458

Fig 3.68(a) Input referred and Output referred phase noise of the Multiply by 8 Chain with signal source phase noise configuration number 1(signal source does not contain any phase noise sideband)



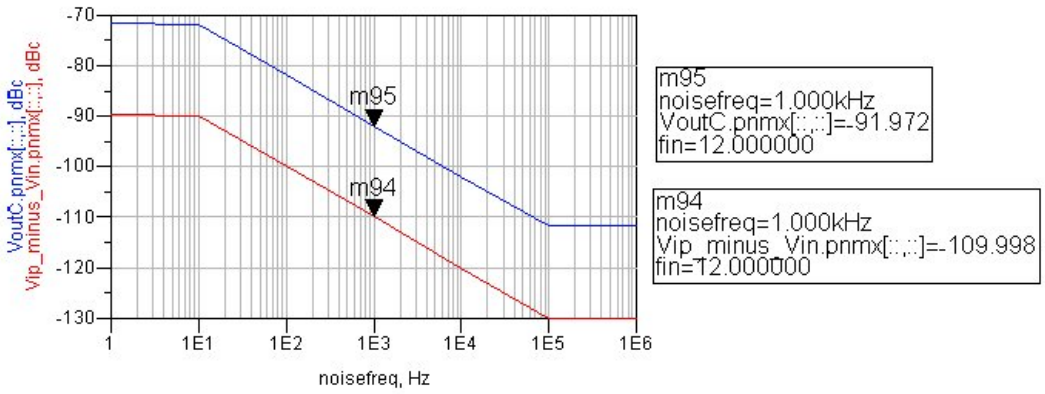
noisefreq	VoutC.pnmx fin=12.000	Vip_minus_Vin.pnmx fin=12.000	...mx - Vip_minus_Vin.pnmx fin=12.000
1.000 Hz	-82.68 dBc	-103.0 dBc	20.316
10.00 Hz	-96.07 dBc	-116.3 dBc	20.244
100.0 Hz	-109.4 dBc	-129.6 dBc	20.187
1.000 kHz	-121.9 dBc	-142.5 dBc	20.604
10.00 kHz	-128.7 dBc	-153.1 dBc	24.368
100.0 kHz	-129.7 dBc	-156.8 dBc	27.127
1.000 MHz	-129.7 dBc	-157.0 dBc	27.261

Fig 3.68(b) Input referred and Output referred phase noise of the Multiply by 8 Chain with signal source phase noise configuration number 2



noisefreq	VoutC.pnmx fin=12.000	Vip_minus_Vin.pnmx fin=12.000	...ip_minus_Vin.pnmx fin=12.000
1.000 Hz	-79.30 dBc	-98.24 dBc	18.931
10.00 Hz	-81.82 dBc	-99.90 dBc	18.089
100.0 Hz	-91.90 dBc	-110.0 dBc	18.053
1.000 kHz	-101.9 dBc	-120.0 dBc	18.044
10.00 kHz	-111.9 dBc	-130.0 dBc	18.102
100.0 kHz	-121.2 dBc	-139.9 dBc	18.696
1.000 MHz	-121.2 dBc	-139.9 dBc	18.694

Fig 3.68(c) Input referred and Output referred phase noise of the Multiply by 8 Chain with signal source phase noise configuration number 3



noisefreq	VoutC.pnmx	Vip_minus_Vin.pnmx	...ip_minus_Vin.pnmx
	fin=12.000	fin=12.000	fin=12.000
1.000 Hz	-71.62 dBc	-89.79 dBc	18.165
10.00 Hz	-71.96 dBc	-89.99 dBc	18.030
100.0 Hz	-81.97 dBc	-100.0 dBc	18.026
1.000 kHz	-91.97 dBc	-110.0 dBc	18.026
10.00 kHz	-102.0 dBc	-120.0 dBc	18.040
100.0 kHz	-111.8 dBc	-130.0 dBc	18.183
1.000 MHz	-111.8 dBc	-130.0 dBc	18.183

Fig 3.68(d) Input referred and Output referred phase noise of the Multiply by 8 Chain with signal source phase noise configuration number 4

In Figure 3.68, phase noise referred to the single-end output nod as well as to the differential input nods are plotted for each signal source phase noise configuration. The phase noise referred to the input port contains both the influence of the noise from the signal source and that from the Multiply by 8 Chain. By subtracting the phase noise components referred to the input from that referred to the output, we get the phase noise degradation in the multiplier chain. Ideally, 8 times multiplication results in 18.02dB of degradation. The output phase noise is determined by the relative strength of these two noise origins, noise injected from the source and noise generated within the multiplier chain. If the phase noise from the source is below a certain value, then the output phase noise will be dominated by the noise sources in the multiplier chain. Any further reduction of the phase noise from signal source would not be visible at the output. The simulation finds out the boundary of input phase noise spectrum where the signal source still dominates the output phase noise.

Fig 3.68(a) shows the result where no phase noise sideband is injected into the multiplier. So, the output phase noise spectrum is caused by thermal noise from the signal source as well as noise sources in the multiplier chain. The phase noise floor at 100K offset is -129.7dBc.

In Fig 3.68(b), the source phase noise contribution is still relatively weaker compared to excessive phase noise. No apparent difference is observed as compared to results in Fig 3.68(a). In Fig 3.68(c), the source phase noise starts to dominate the output phase noise spectrum. We can see that the degradation is close to the ideal limit at various offsets. In Fig 3.68(d), as the source phase noise is further increased the degradation approaches more to the

ideal 18.02dB limit.

From the above simulations, the source phase noise configuration number 3 is found to be the boundary where signal source phase noise dominates the output phase noise from the Multiply by 8 Chain. The slope of the injected phase noise sideband only serves the goal of simulation. It does not represent any actual input signal characteristic.

3.4.2.4 Multiply by 8 Chain Performance Summary

Table 3.8 summarizes the performance of the Multiply by 8 Chain.

Table 3.8 Performance of the Multiply by 8 Chain

Multiplication factor	8
Input signal band	10GHz ~ 14GHz
Output signal band	80GHz ~ 112GHz
Nominal input signal power from 100 Ohm differential source	About -17dBm differential
In-band output power to 50 Ohm single-end load	-3.8dBm ~ -0.4dBm
Conversion gain	13.2dB ~ 16.6dB
Unwanted spur suppression With 0.3dB input amplitude unbalance 5 degrees input phase unbalance	Better than 40dB
Power Consumption (with ideal biasing)	289mW

3.5 Summary

In this chapter, system level requirements on the signal up conversion chain are analyzed. The whole circuit is divided into two functional parts, the Multiply by 8 Chain and the W Band Blocks. Performance and circuit implementation of the Multiply by 8 Chain is discussed. Schematic simulation validates the design considerations.

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Chapter 4 W Band Blocks

In chapter 3, we have discussed the first part of our signal up-conversion chain, the multiply by 8 chain. When the signal is up-converted from low frequency to W band, it requires further amplification to provide enough drive power for the transmitter antenna and mixer LO port. This job is accomplished by the second part of the up-conversion chain, what we call W Band Blocks. This chapter focuses on the design considerations and performance of these circuit blocks.

4.1 Module Division

The output signal from the multiply by 8 chain is single-ended. To provide the single-end drive signal to the transmitter antenna and the differential mixer LO signal, W Band Blocks should offer functions like power division, single-end to differential conversion and the necessary signal amplification. Considering the bandwidth requirement, 80GHz to 112GHz, we have put forward a topology made up of several commonly used microwave structures and amplifiers. The block diagram is shown in Fig 4.1. Necessary matching networks are omitted. The W Band Blocks consists of a power divider, a passive balun and two medium power amplifiers.

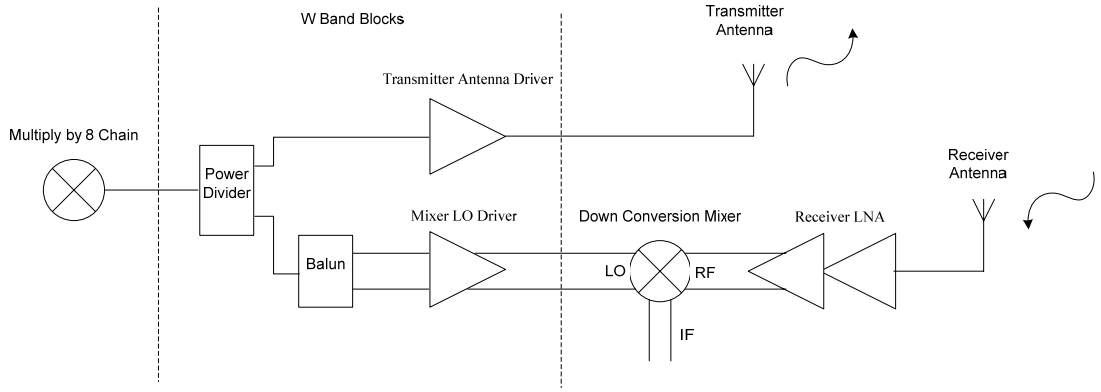

Fig 4.1 Circuit blocks working in W Band

4.2 Passive Structures

4.2.1 Power Divider

Power dividers split the input power to the output ports in even or uneven fashion. Four port networks like directional couplers and hybrids can work as power divider also. Some 3 port networks that can realize power division are often used for their simplicity. There is resistive divider, which losses half of the input power in dissipation. There is lossless T junction. But it suffers from the problem of not being matched at all ports and not having isolation between two output ports [1].

The most promising passive power divider is the Wilkinson power divider. It is lossless when

output ports are matched. There is isolation between two output ports. The basic topology of Wilkinson power divider is shown in Fig 4.2. It can be constructed with transmission lines and a resistor, which makes it ideal for on chip implementation at high frequencies.

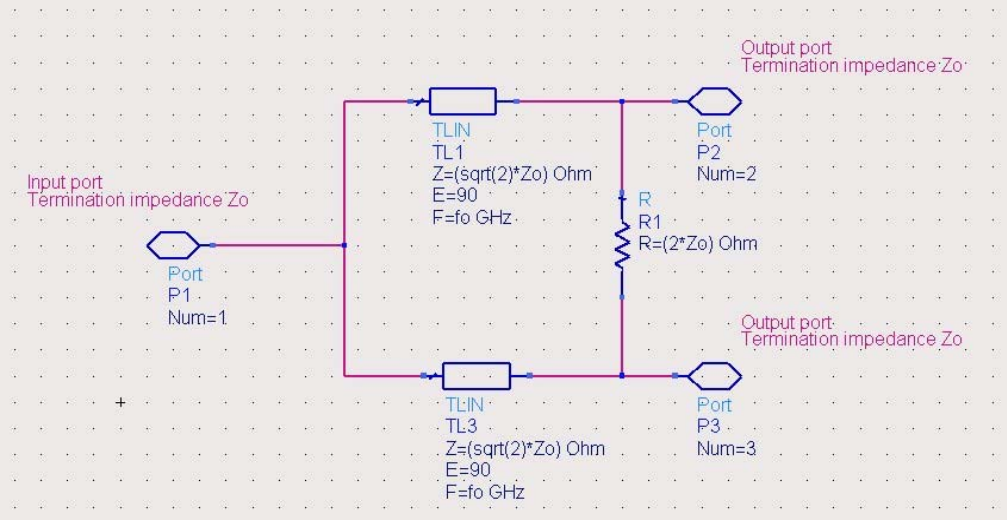

Fig 4.2 Topology of Wilkinson power divider

The IBM library provided a scalable model of the Wilkinson power divider. Simulations show that the on chip implementation approximates the performance of one with ideal components quite closely. Forward transfer from input to two output ports as well as isolation between two output ports is shown in Fig 4.3.

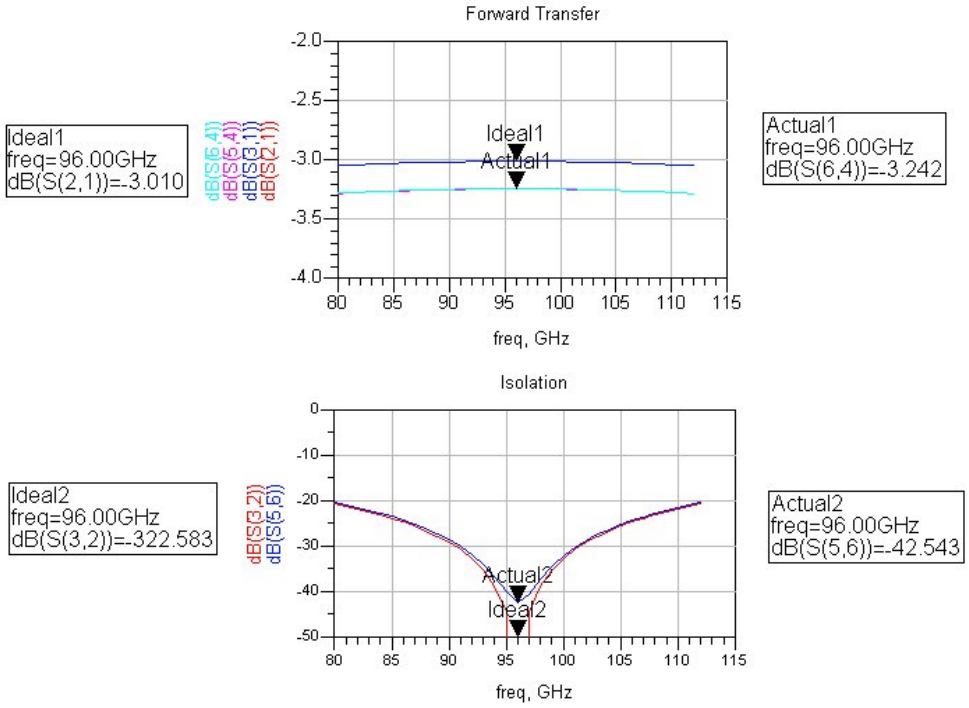

Fig 4.3 Performance comparison of two Wilkinson power dividers, one with ideal components, the other with the actual on chip passive components

The forward transfer function is actually very flat, showing only about 0.05dB variation within our band of interest. Across the whole band, better than 20dB isolation is achieved between two output ports. This is to our advantage since we do not want the Transmitter signal path and the LO signal path to affect each other. Simulations show that the performance is also not so sensitive to termination impedance variation.

4.2.2 Passive Balun

A Balun is needed to provide the differential LO signal to the double balanced receiver mixer. From the study of active Balun at lower frequency we can conclude that with the available transistor, it is difficult to build an active wideband Balun with good performance at this frequency. So a passive Balun is selected to work in W band.

A 180 degree hybrid junction can split the input signal into two antiphase outputs, which makes it a good candidate for Balun operation. There are several realizations of hybrid junctions, like ring hybrid or ratrace hybrid, tapered coupled line hybrid and magic-T [1]. Among these structures, the ratrace hybrid stands out for the possibility of on chip implementation and well characterized performance.

First, we shall follow a discussion about 180 degree hybrid operation [1]. It is a four-port network. Depending on which port the input is applied to, its outputs can be 180 degree out of phase or in phase. With reference to the 180 degree hybrid symbol in Fig 4.4, port 1 and 2 are called sum and difference ports. A signal applied to port 1 will be split evenly into two in-phase components at port 3 and 4, and port 2 is isolated. When a signal is applied to port 2, it will be equally spilt into two anti-phase components at port 3 and 4, port 1 is isolated. This is the operation mode that can be used as a Balun. In addition, the 180 degree hybrid can also be used as a combiner, when two signals are applied to port 3 and 4, their sum will be formed at port 1, while their difference will be formed at port 2.

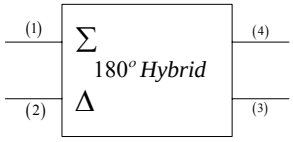

Fig. 4.4 Symbol for 180 degree hybrid

A passive Balun does not provide gain. Composed with ideal components, a 180 degree hybrid splits the input signal power evenly between two output ports at the center frequency. When the metal and substrate loss of on chip components is taken into account, some loss should be budgeted. Simulation with the on chip ratrace from IBM process shows about 1dB additional loss.

The bandwidth for Balun operation is mainly defined by the amplitude and phase unbalance between two output branches. The performance of a passive Balun shows strong frequency dependency. Output balance is ideal at the center design frequency, but as frequency deviates from the center, difference between two output ports grows. Fig .4.6 shows frequency

response of two 180 degree hybrids. One is the standard ratrace hybrid, shown in Fig 4.5(a), the other is its bandwidth improved version [2] shown in Fig 4.5(b). The input and output ports are labeled on plot. They are in accordance with the S parameter simulation result in Fig 4.6. Comparing the two set of results, we find that the ratrace with additional phase flip renders better balance over a much larger bandwidth. In it the 3/4 wavelength transmission line is replaced with a 1/4 wavelength coupled line, which improves the performance tremendously and makes the structure more compact. We shall see from further simulation results that the standard ratrace does not cause too much performance degradation to our system.

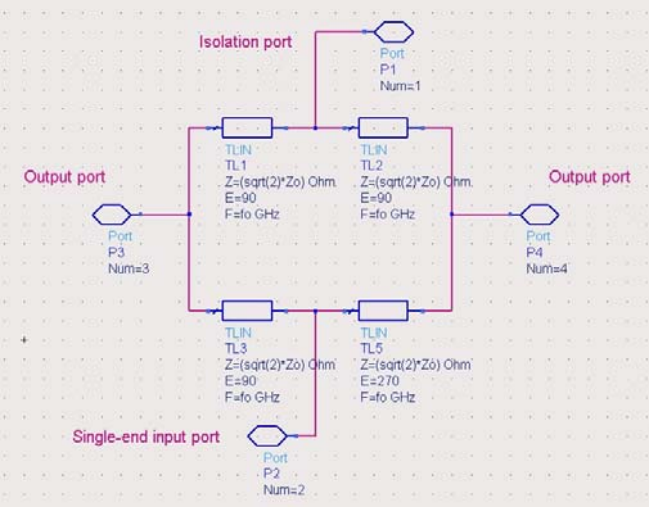

Fig. 4.5 (a) Topology of standard ratrace hybrid made of transmission lines

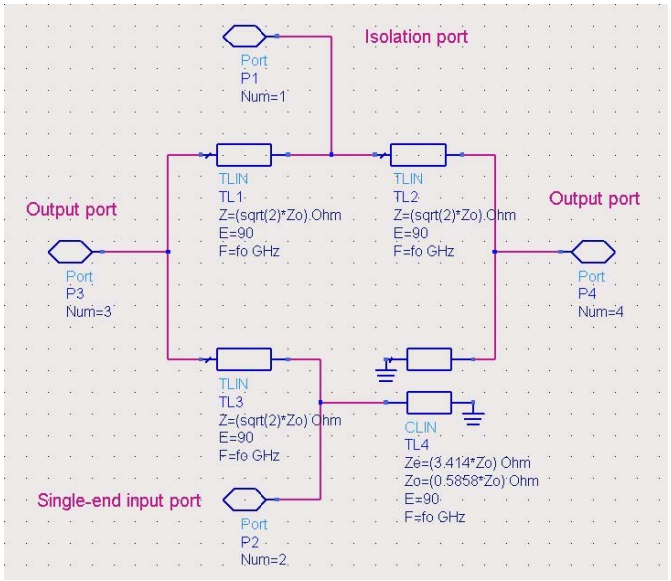

Fig. 4.5 (b) Topology of the ratrace hybrid with additional 180 degree phase flip using

coupled lines

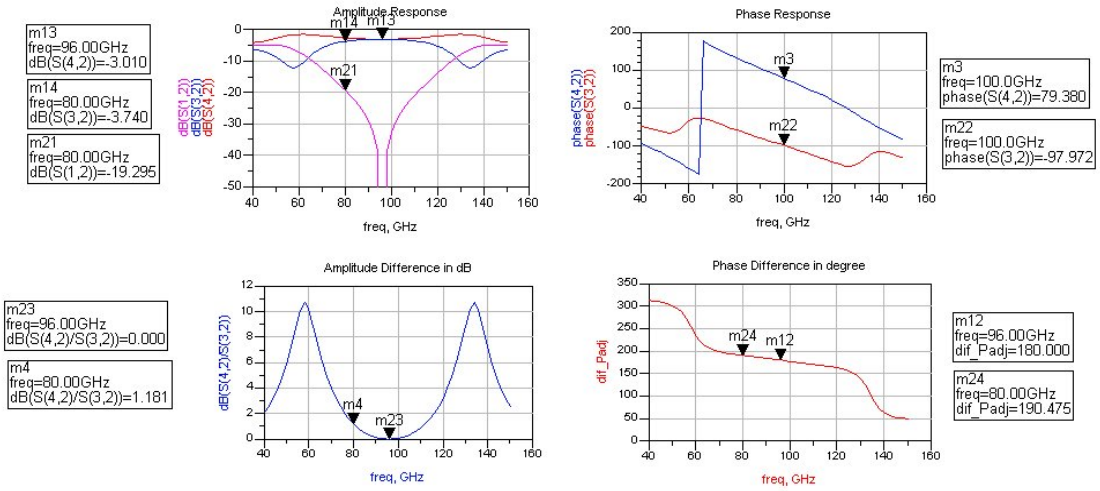

Fig. 4.6 (a) Frequency response of standard ratrace hybrid used as a Balun

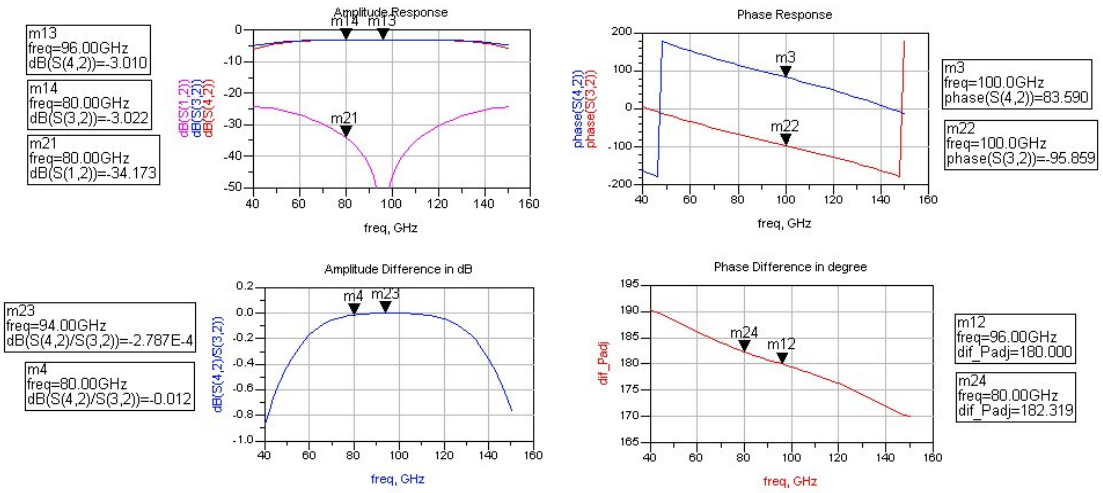

Fig. 4.6 (b) Frequency response of the ratrace hybrid with additional 180 degree phase flip used as a Balun

In the simulation shown in Fig 4.6, the center frequency of the Baluns is set to 96GHz, which is the center frequency of the output signal bandwidth of the multiplier chain. The targeted frequency band spans from 80GHz to 112GHz, which is about 33% around the 96GHz center frequency. In Fig 4.6(a), the amplitude unbalance by the standard ratrace at the band edge is about 1.2dB and the phase difference is about 10 degrees. The insertion loss of one branch at that point is 3.74dB.

Although a passive Balun shows higher insertion loss at band edge than at the center, the frequency response is still symmetrical about the center frequency. As long as the terminal impedances are close to the ideal value, these ratraces allow pretty wideband operation. The requirement on source and load impedance means that the stages before and after the ratrace

should provide a wideband port impedance with little variation versus frequency to guarantee the best performance for the ratrace. Terminal impedances are swept to find out how sensitive the performance is against these variations. It appears that the forward-transfer from single-end input to differential outputs, S(3,2) and S(4,2), are less sensitive to impedance variation than the isolation from input to isolation port, S(1,2). S(3,2) and S(4,2) drop slower when terminal impedance are higher than nominal value.

The most notable advantage of a passive balun is probably its linearity. It is the innate trait of many passive structures. No mixing product from the input tones will be added to the output. The frequency components in the input signal fed to the balun experiences only frequency dependent delay and attenuation. The frequency dependant transfer function is not a problem since for our continuous wave system, the instantaneous bandwidth is rather low compared to pulsed radar systems.

On the other hand, the drawback of these passive Baluns is also apparent, that is the large dimension of its actual implementation. The standard ratrace requires 3 pieces of 1/4 wavelength and 1 piece of 3/4 wavelength transmission line. These lines have quite a length even up to about 100GHz. To give an example, the transmission line provided by the IBM 8hp process for a 1/4 wavelength at 96GHz is about 370um long. Even with the 1/4 wavelength coupled line in place for the bandwidth improved version, unless a clever layout is devised, the ratrace still takes a large chip area. Luckily the IBM library offers a very compact scalable layout for the standard ratrace, the whole structure can be fitted into an area of about 200um*300um. Since the propagation coefficient beta is almost proportional to frequency, the length of transmission line required increases with the reciprocal of frequency. At lower frequency, the formidable length simply makes on chip implementation not so attractive.

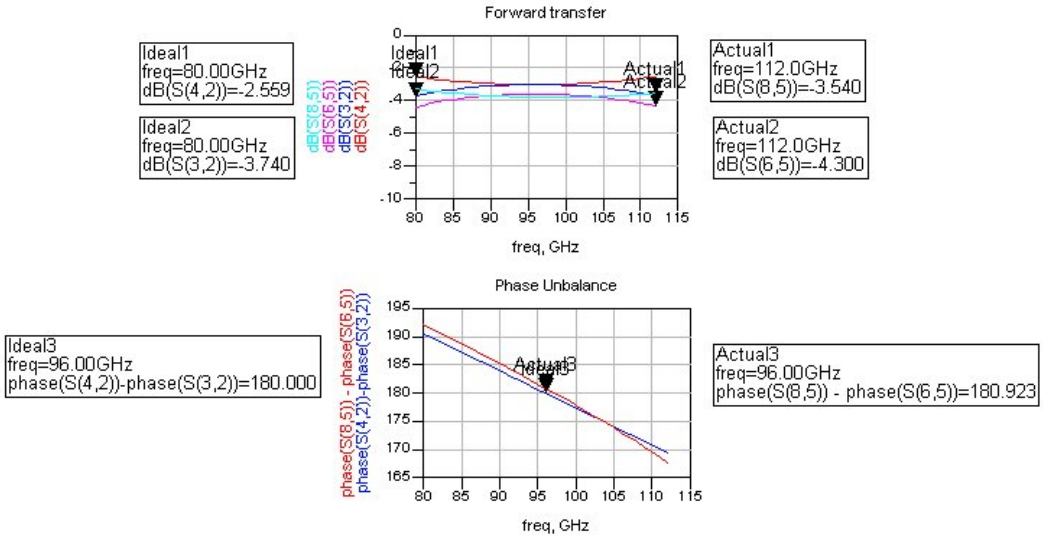

Fig 4.7 Performance comparison of two ratrace hybrids, one with ideal components, the other with actual on chip passive components

Fig 4.7 shows the performance comparison of an ideal ratrace hybrid and the one from the IBM library. For both of the two, there is about 0.8dB amplitude unbalance and about 10 degree phase unbalance at the band edges. The actual ratrace show about 1dB more insertion loss than the ideal one. For our application, this ratrace offers sufficient performance over the bandwidth. It is true that the ratrace with additional phase shift offers even better balance over a wider bandwidth. But the quarter wavelength coupled line makes the implementation more difficult. To enhance our chance of success, we use a conventional ratrace from the IBM library.

4.2.3 Connecting the Power Divider with Ratrace

The ratrace hybrid and the Wilkinson power divider require wideband ohmic terminations at their ports. It is useful to investigate how they perform with non-ideal termination impedances, since their driving and loading condition will be determined by their preceding and succeeding circuit blocks, which surely will be frequency dependant.

At the interface of the power divider and ratrace, another buffer amplifier is probably not a good choice, because at around 100GHz, it is more difficult to obtain a flat gain response from active circuit. Apart from bandwidth limitations, passive components introduce considerable losses in W band. Higher input power for the hybrid means higher losses in the passive networks, so it is better to introduce gain after these circuit blocks.

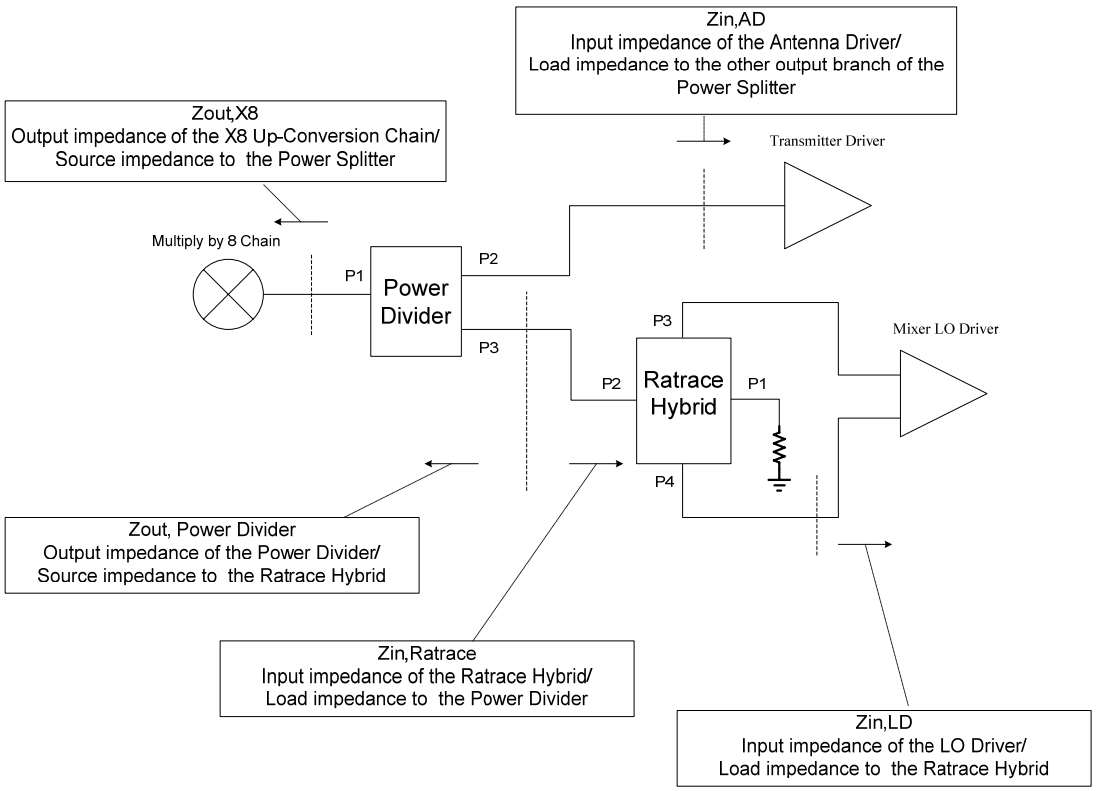

Fig 4.8 Driving and loading relation in the W Band Block

Not using the buffer, we have explored the feasibility of connecting the Wilkinson power divider and the ratrace hybrid directly and let them provide the termination impedance to each other. The circuit configuration is redrawn in Fig 4.8. The labeled port numbers correspond to the port notation used in the following S-parameter simulations. The necessary matching networks are omitted in Fig 4.8. They are considered part of the active circuit blocks.

Simulation is done with a Wilkinson power divider and a ratrace hybrid, all built from ideal passive components. The reference termination impedance is chosen 50 Ohm. Fig 4.9 shows the output reflection coefficient (S33) from 80GHz to 112GHz looking into one branch of the Wilkinson power divider. The source impedance at P1(Zout,X8), and the load impedance at P2(Zin,AD), is varied from 30 Ohm to 70 Ohm in two simulations respectively. The output impedance of the power divider remains pretty close to 50 Ohm when the source impedance changes a lot. When the termination impedance at the other output branch changes, this output impedance remains very close to 50Ohm. If the termination impedance at those two ports, namely the output impedance from the 3rd doubler (Zout,X8) and the input impedance of the antenna driver (Zin, AD) can be maintained close to 50 Ohms over the entire band, the output impedance of the power divider(Zout, Power Divider) will be within a tolerable range.

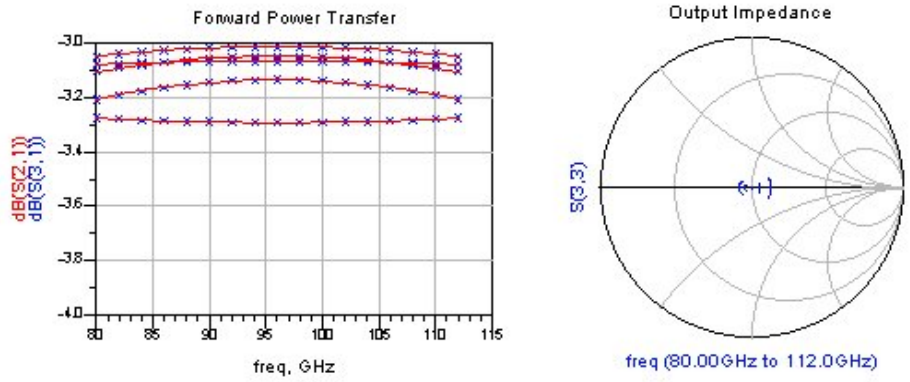

Fig 4.9(a) Forward transfer and Zout,Power Divider variation when Zout,X8 changes from 30Ohm to 70Ohm

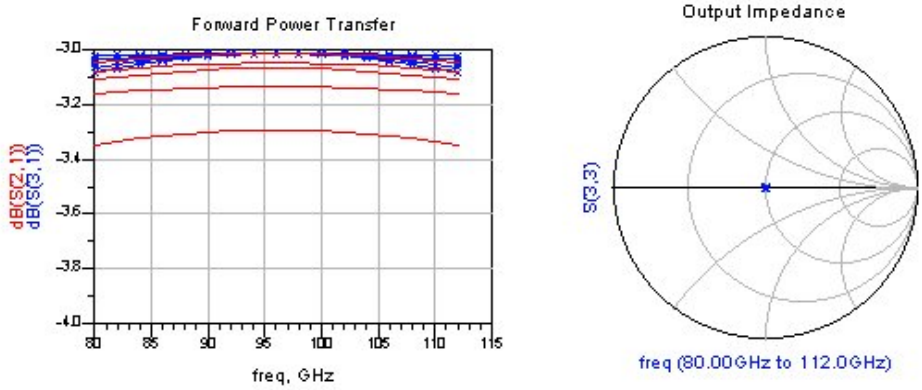

Fig 4.9(b) Forward transfer and Zout,Power Divider variation when Zin,AD changes from 30Ohm to 70Ohm

Similar simulation has been performed with the ratrace hybrid. Since the LO driver is a differential amplifier, its input impedances at two input terminals are equal when input signal is relatively small. We vary these impedances together from 30 Ohm to 70Ohm. Resulting variation of the forward transfer to two output ports and the input impedance variation are plotted in Fig 4.10. It seems that these performance quantities are sensitive to the termination condition, especially at the band edge. So, it is important to keep the input impedance of the LO driver closer to the reference value over the entire band.

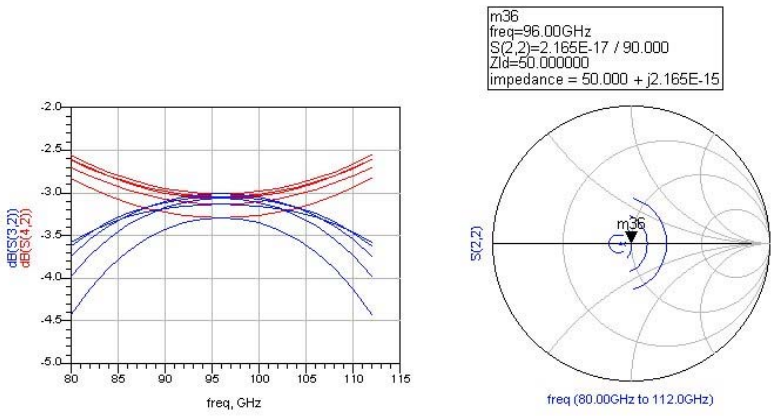

Fig 4.10 Forward transfer and Zout,Ratrace Hybrid variation when Zin,AD changes from 30Ohm to 70Ohm

4.2.4 Signal Power Level Planning

Considering the output power from the multiply by 8 chain and the input power required by the transmitter antenna and the mixer LO port, we have estimated the power level within the W Band Blocks. Although signal power varies within the bandwidth of 32GHz, the power relation here helps to substantiate the design goals. Fig 4.11 shows the power level at each point. The passive loss from the ratrace hybrid has been taken into account. Roughly about 10dB gain is targeted for the transmitter antenna driver. About 5dB gain is targeted for the LO driver.

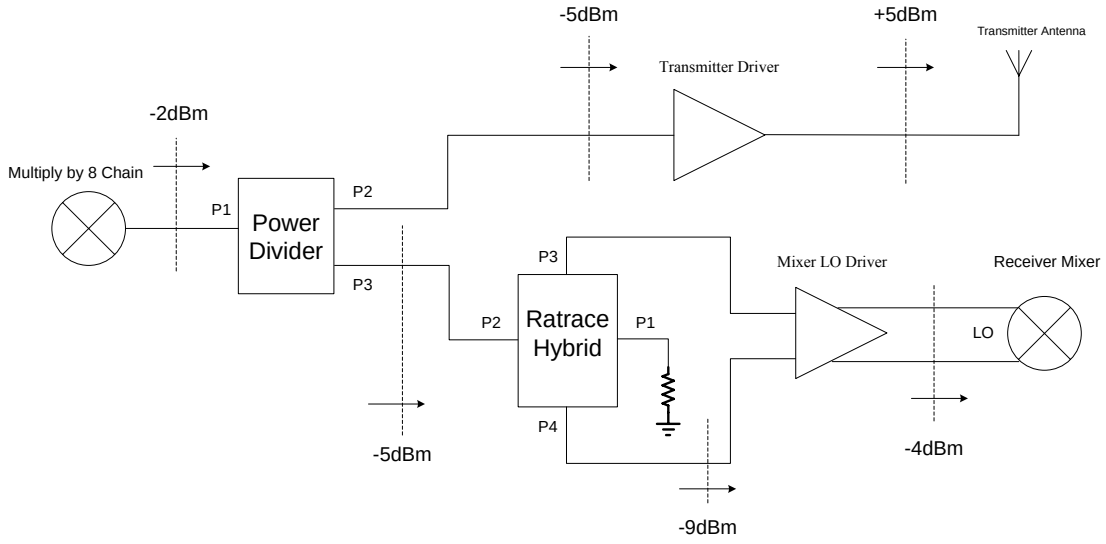

Fig 4.11 Signal power planning in the W Band Blocks

4.3 General Considerations about Driver Amplifier

4.3.1 Amplifier Operation Mode

In W band, the extreme operation condition poses some confinements to the choice of amplifier operation mode.

First, the power amplification ability of the transistor is bias dependant. Conventional higher efficiency PAs, such as Class-B and Class-C, enhances efficiency by reducing the DC bias point. However, even if the SiGe transistor is biased with higher current density, its current gain is only around 2 at 100GHz. There is just not so much room to reduce the current density.

Second, Class-B or Class-C PAs usually require higher input power to drive the transistor around turn on point. So that the conduction angle is reduced and efficiency is improved. However the output power from the multiply by 8 chain is limited. Considering the wide bandwidth that it should operate in and the loss in power divider and ratrace hybrid, we could not expect high drive power available to the driver amplifiers.

For these reasons, we build both the transmission antenna driver and mixer LO driver as Class-A linear amplifiers.

4.3.2 Bias Point

After deciding on the amplifier operation mode, the bias point can be chosen to enhance the power amplification Although the f_t is widely used as a figure of merit to judge the high frequency performance of a transistor, it is checked under idealized condition (driven by current source and AC-grounded collector output node). From the large signal operation point of view, f_{max} serves as a better indication since it takes into account the effect of r_b and $c_{u.}$. f_{max} is the frequency where the magnitude of transistor power gain is unity. It is theoretically the highest frequency that a transistor can oscillate. One of its simulation expressions is the extrapolation of the maximum unilateral power gain. But it tends to be an overestimation. A more objective method is to shift up in frequency up to the point where the device has become unconditionally stable [3]. After which f_{max} can be found by the extrapolation of G_{Amax}, the maximum stable gain, with the following expression:

$$f_{\max} = f_{measurement} * \sqrt{G_{A\max}} \tag{4.1}$$

This method is a good approximation for simulation, as well as, for measurement. Nevertheless, it is still not so accurate because at higher frequency G_{Amax} does not necessarily follow a -20dB/dec roll off. So it is better to simulate G_{Amax} at higher frequency and find the frequency where it becomes unity(0dB). Fig 4.12 shows the curve of ft and f_{max} vs. bias current Ic sweep. The transistor used for simulations has emitter length of 6um. The two

curves have similar shape and their peaks occur also at similar bias points. The current density for the power amplifier is chosen to be about 1mA/um, resulting in an f_{max} of about 240GHz.

The size of the device is chosen according to output power requirement. It will be addressed in next sections describing the specific stages.

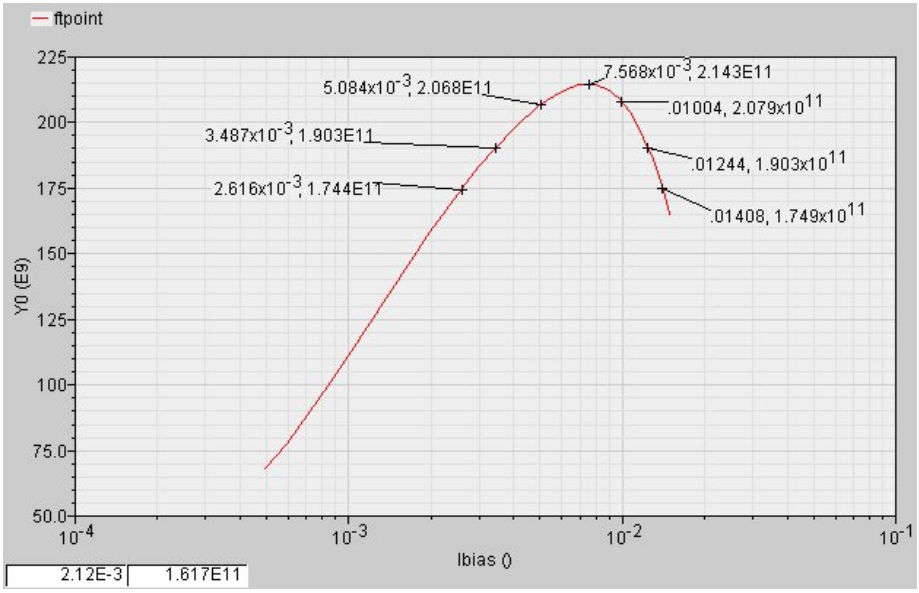

Fig 4.12(a) ft vs. collector bias current, Le is 6um

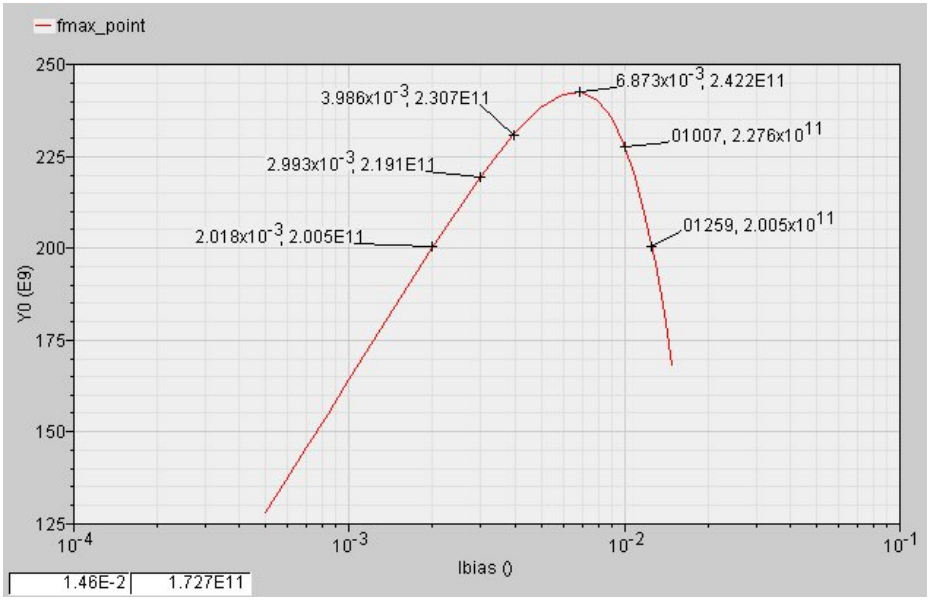

Fig 4.12(b) fmax vs. collector bias current, Le is 6um

4.3.3 Small Signal Characterization

In order to choose the amplifier topology, we need to see first how a single stage transistor behaves. A common emitter stage and a cascode stage are compared. Fig 4.13(a) and (b) show the maximum transducer power gain, the input, output reflection coefficients and the output

equivalent impedance of these two stages respectively. The emitter length of all transistors is 5um*4. Small signal S parameter simulation is conducted, although it does not reflect the large signal performance, the result shows the difference between these two stages. The output impedance is modeled with a simple RC parallel combination. This model is sufficient for our comparison purpose.

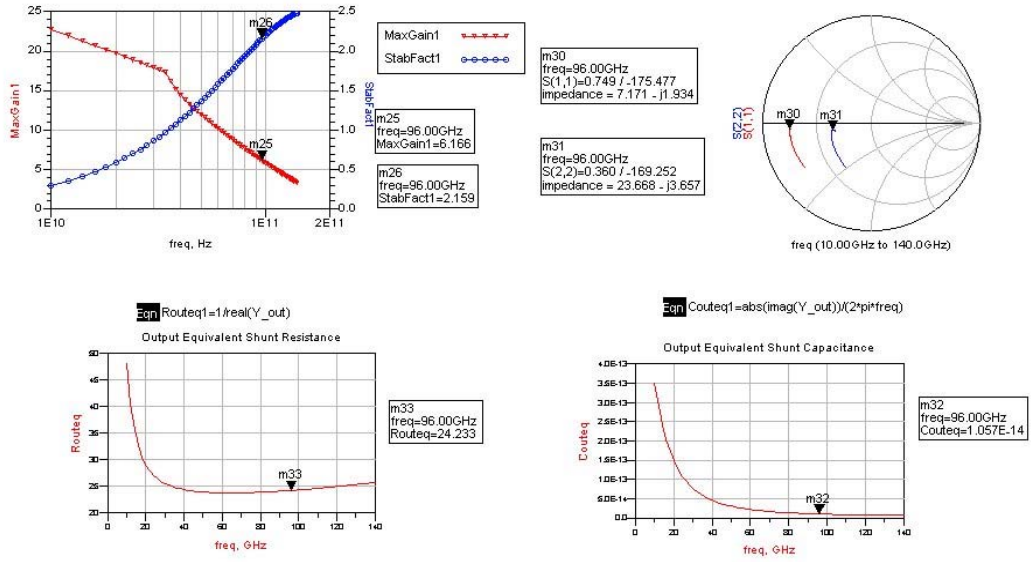

Fig 4.13 (a) Maximum power gain, stability factor, input, output reflection coefficient, equivalent output resistance and capacitance of a common emitter stage

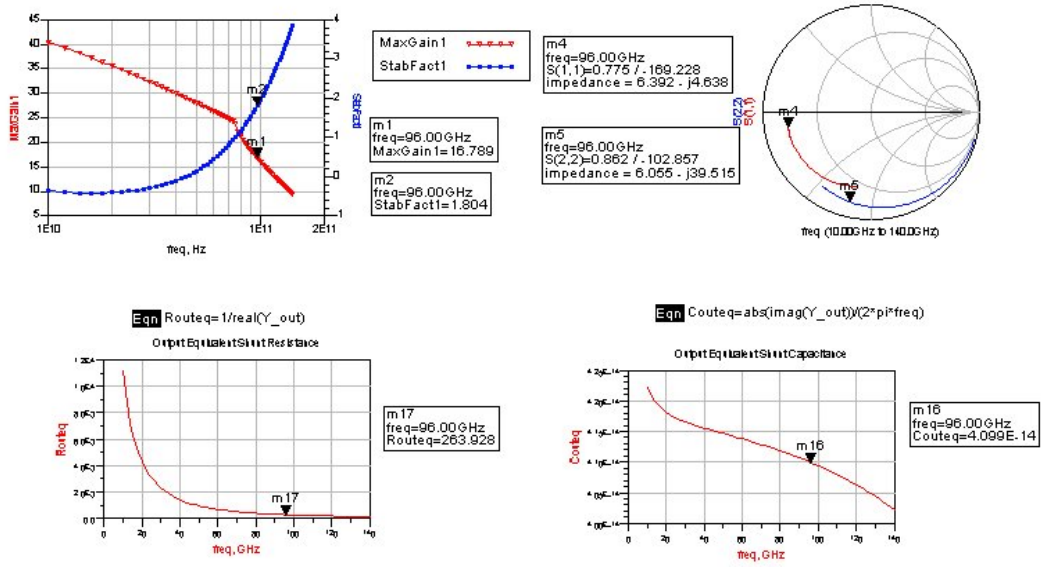

Fig 4.13 (b) Maximum power gain, stability factor, input, output reflection coefficient, equivalent output resistance and capacitance of a cascode stage

The maximum transducer power gain of the cascode stage at 96GHz is 16.8dB, about 10dB higher than that of the CE stage, being only 6.2dB at 96GHz. The stability factors of these two stages are all above unity in the band of interest. The higher gain by the cascode can be

attributed to its higher output resistance part. The output resistance of the cascode stage is about 260 Ohms, more than 10 times higher than that of the CE stage. So when the reactive part of the output impedance is resonated out, higher output power is expected. Looking at the output reactance, the cascode stage has the output capacitance of about 41fF, 4 times higher than that of a CE stage. It is found that the decoupling circuit at the base of the cascode transistor has a strong impact on this capacitance. The feedback of base-collector capacitance increases the output capacitance.

The combination of high output resistance and high output capacitance put the output reflection coefficient of the cascode stage near the rim of smith chart. It lies in the high-Q region. This means that when its output is matched to the load, the cascode stage can deliver higher power, but the bandwidth is inevitably narrower.

In an L-matching network, the quality factor, which relates to the bandwidth is fixed by the resistance ratio of the source and the load. Even when a multi-section matching network is designed to break away from this fixed relation, the overall bandwidth is still affected. Besides, being in the high-Q region makes it more difficult to implement the matching network with passive components. The resistive parasitic from inductors, capacitors and transmission lines limits the achievable quality factor, so matching networks made up by these components cannot reach to the very edge of the smith chart.

In order to lower the difference of transmitted signal power over the band, the bandwidth of the transmission antenna driver should be widened. High output power at a single-frequency point is not our focus, instead, a flat gain response over the entire band is better welcomed. Bandwidth and gain trade-off is the focus of this amplifier.

At millimeter wave frequencies, it is difficult to make a wideband AC ground, which is required for the base terminal of the cascode device. Resistive parasitics lowers its gain due to undesired feedback. Inductive parasitics in the base lead may yield oscillation. This problem is much less serious with a differential amplifier than a single-end one [9], since a large portion of base current moves back and forth between the two bases of cascode devices, providing a virtual ground.

4.3.4 Large Signal Capability

The largest output signal that a stage can handle is limited by the current and voltage swing at the output side. For a linear common emitter PA, the transient current can have a peak swing up to the maximum DC bias current of that stage. Voltage at the collector is limited on two ends. Knee voltage sets the lower boundary of the collector voltage. The higher end of collector voltage swing is normally confined by break down voltage.

In our design, the transistor property limits this maximum point. The RF transistor in use is the High ft NPN transistor. The open base collector to emitter breakdown voltage, BVceo, is only 1.77V nominal. According to [4], the avalanche break down is affected by the DC impedance connected at the base of a transistor. Lower external impedance allows the excess

holes that cross the base-collector junction into the base to be shunted before causing the base-emitter junction to increase its forward bias, which leads to avalanche multiplication. In this way the actual voltage of avalanche breakdown is increased. The breakdown voltage with certain base resistance is denoted BVcer. [5] shows that BVcer can be increase over 3 V when the base external resistance is as low as 100 Ohms.

In this design, we have checked how much can the break down condition be improved with a simple current mirror biasing as shown in Fig 4.14.

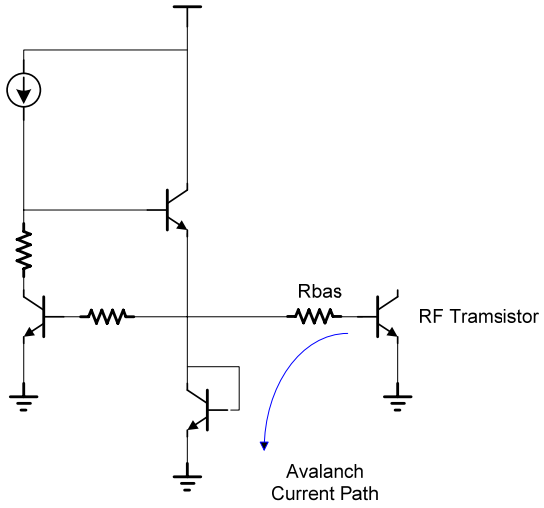

Fig 4.14 current mirror bias circuit for power amplifier stage

A diode connected tail current source is added to the current mirror, which provides the low impedance path to ground. The impedance associated with this path is roughly $\frac{1}{g_m} + R_{bas}$.

g_m is the transconductance of the diode connected transistor. With normal DC current, gm can be large enough to let Rbas dominate. The exponential V-I relation of the diode improves the reverse current handling capability of the bias circuit.

In the simulation, reference current of the mirror is swept to cover the collector current range that the RF transistor might experience with RF excitation. Then Rbas is altered to examine its influence on the breakdown performance.

Fig 4.15 shows that when Rbas=300 Ohms, the breakdown voltage with 2mA nominal collector current is about 2.4V. If the minimum allowed Vce is 0.7 V(slightly higher than knee voltage), then this condition allows a peak-to-peak collector voltage swing of more than 1.6V, which is more than enough for this stage to deliver 5dBm output power to a 50 Ohms load.

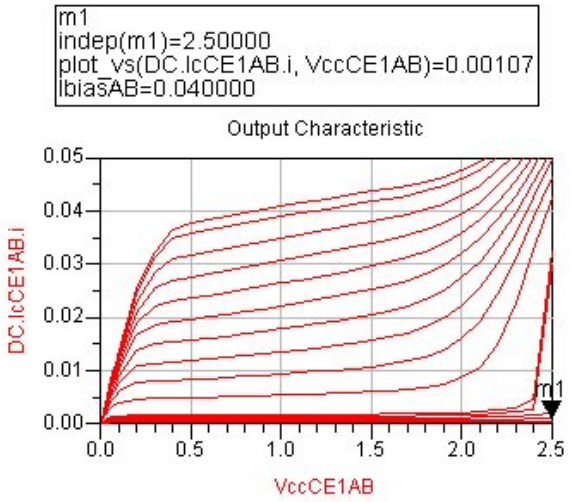

Fig 4.15 output characteristic when Rbas = 300 Ohms

If there is need to further increase the collector breakdown voltage, more complicated bias schemes should be designed to take account for the reverse base current [6], Veenstra etc. utilized feedback in the bias circuit and increased the breakdown voltage tremendously. In [7], Pfeiffer etc. adopted another feedback bias circuit, first proposed in [8] by Jarvinen etc., into their millimeter wave power amplifier design using a similar technology as ours. It allows the collector-emitter voltage to swing +/-1.5V around a 2.5V dc-bias voltage.

4.4 Transmission Antenna Driver

4.4.1 Performance Requirements

The requirements on the transmission antenna driver are as follows. About 5dBm output power is to be delivered to the antenna. Gain variation should be kept low from 80GHz to 112GHz. Input impedance should be matched to the ideal termination impedance of the power divider. Output impedance should be matched to the characteristic impedance of the antenna to minimize multiple reflections at that interface and avoid power loss through mismatch. Beside, the gain of the transmitter driver should be able to vary over a range to allow beam shaping with the parallel transmitter antennas in the orthogonal direction of the antenna. So, preferably it should be a VGA (variable gain amplifier).

According to the power planning, the input power to the transmitter driver is about -5dBm. In order to get an output of 5dBm, the amplifier gain should be close to 10dB. The input signal to this amplifier is large enough to cause compression, so the small signal gain is less relevant to the actual operation. Working far beyond the compression point reduces the gain, working below the compression point, means that we are not utilizing the full capability of the device.

So, the 1dB output compression point of this amplifier should be kept close to the nominal output power. These considerations are summarized in Table 4.1

Table 4.1 Performance requirements of the transmitter driver

Bandwidth	80GHz ~ 112GHz
Power gain	About +10dB
Output 1dB compression point	About 5dBm
Input impedance	Close to 50Ohm
Output impedance	Close to 50Ohm

4.4.2 Choice of Each Stage

A single-ended transmitter antenna requires a single-end output signal from its driving circuit. But a differential amplifier is more robust in terms of parasitic tolerance especially at higher frequencies. It is true that we can make a differential amplifier and take the output signal from only one branch to feed the antenna. However, a differential amplifier requires a differential input signal. This means a balun should be used, which further increases system complexity. Power consumption is another consideration. The transmitter driver consumes the highest DC current of the whole signal path, about more than 30mA. Making it differential adds a fair amount of DC power consumption. For these reasons, we will build a single-end amplifier for the antenna driver amplifier even though more attention should be given to parasitic and decoupling.

Based on simulation with a single stage, a two stage amplifier is the most reasonable choice for the antenna driver.

Output Stage

The output stage will be conjugate matched to the transmission antenna, which has a characteristic impedance of 50 Ohm, for low antenna reflection. So, the output impedance of the output stage directly affects the overall bandwidth. If we consider the simulation results shown in Fig 4.13, it is fair to say that CE stage has a better chance of achieving wideband matching with simple network.

In Fig 4.16, loadpull simulation shows the output power contour of a CE stage and a cascode stage respectively. The current densities and device sizes are kept the same. The inputs are matched to 50 Ohms source with simple network. The simulation frequency is set to 96GHz. In this case, CE stage gives 3dB less gain. The limit of voltage and current swing changes the maximum power relation of CE and cascode stage. Even though CE stage gives lower power gain than a cascode stage, we choose it for the 2^{nd} stage because of bandwidth consideration. The collector bias is then set according to the breakdown voltage and voltage swing.

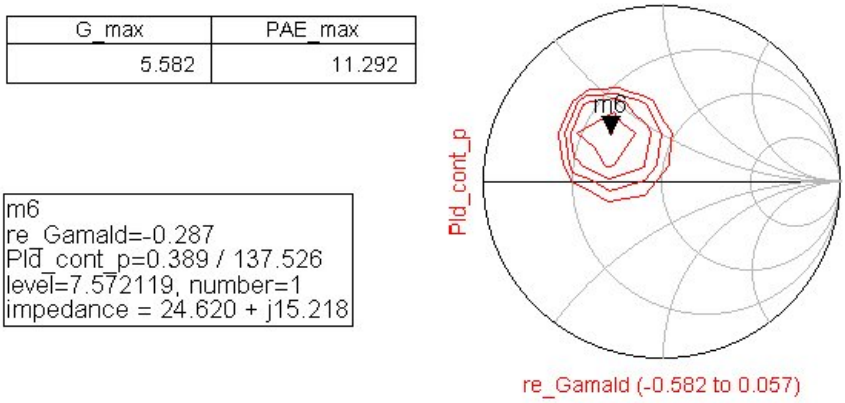

Fig 4.16 (a) Maximum power gain, Maximum PAE, output power contour of a CE stage obtained from loadpull simulation

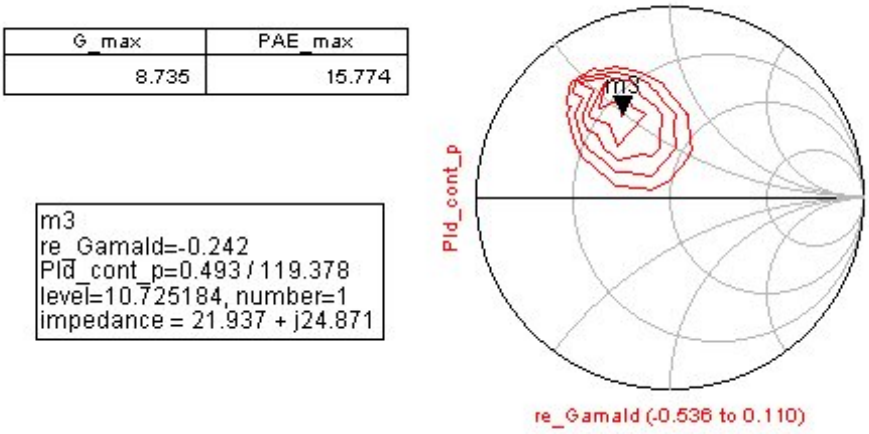

Fig 4.16 (b) Maximum power gain, Maximum PAE, output power contour of a cascode stage obtained from loadpull simulation

Input Stage

Due to its high output conductance, CE stage offers a lower gain compared to the cascode. The CE stage is used for the output stage as a compromise between bandwidth and breakdown voltage. To achieve higher gain with two stages, gain from input stage should be increased. For these reasons, a cascode stage is chosen for the input stage. Considering the voltage gain from the output stage, reduced voltage swing at the collector of the input cascode relaxes the requirement on breakdown performance.

The interstage matching network is less confined by wideband impedance matching requirement since it will provide necessary peaking effect. The large impedance difference between the output of the cascode stage and the input of the CE stage affects the overall bandwidth less.

Device Size

The actual size of the transistor is not chosen at once. This is mainly because the expectation on gain, bandwidth as well as the input power available to the antenna driver. The bandwidth requirement almost precludes the choice of a third stage. With only two stages, wide band large signal gain of more than 15dB is difficult. 10dB gain is a more practical goal.

Simulation shows that the in-band output power of the power divider ranges from about -6dBm to -4.5dBm. The sizes of the transistors are chosen and then modified to operate the amplifier close to 1dB compression point while delivering more than 10dB of gain. The emitter length of the output stage is set to be 20um, and that of the input stage is set to be 12um. The current density is kept about 1mA/um.

4.4.3 Matching Procedure

The common procedure of designing Class A power amplifier starts at the output and walks back toward the input. If narrow-band gain is the target, optimum load impedance for high output power from each stage is determined with load pull simulation. Then matching networks converts the input impedance of a stage to the optimum load impedance of its preceding stage. In this way, the overall power gain is maximized at a single frequency.

The input impedance of this amplifier directly loads the power divider. It should be maintained close to the reference termination impedance for the power splitter, which is about 50 Ohm. The output impedance connects to the transmitter antenna. In order to lower reflection at the amplifier antenna interface, the output impedance should be conjugate matched to the port impedance of the antenna, and that is also 50 Ohm for our system.

The wideband matching requirement at the input and output limits the freedom of designing these two matching networks. They are mainly optimized for low port reflection throughout the whole band. If the amplifier consists of two stages, this only leaves the interstage matching network with the freedom to shape the overall frequency response. Besides, the amplifier stages are AC coupled. So, all the matching networks should incorporate DC blocking and biasing functionality.

For the interstage matching, some trade off is expected between the maximum gain and the gain flatness. Whether impedance match(conjugate match) or power match(based on loadline) is utilized depends on their effectiveness to shape the desired frequency response. The idea is shown in Fig 4.17. In it, the respective frequency responses as well as the overall response are shown.

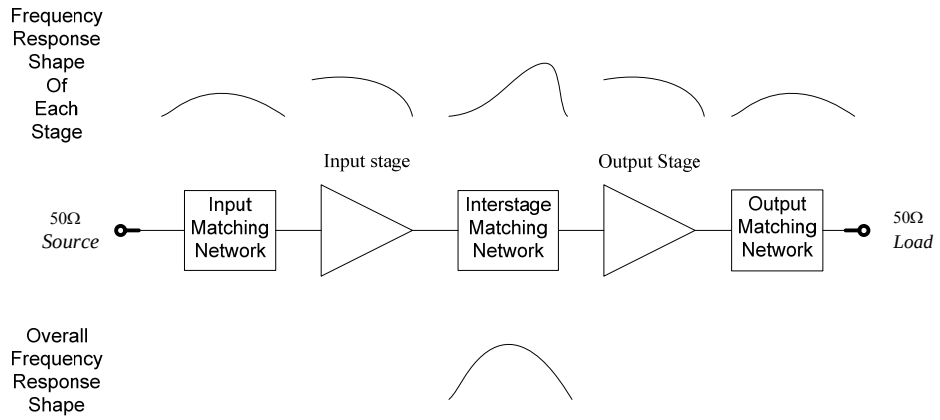

Fig 4.17 The frequency response of each stage and matching network of the two stage antenna driver amplifier

This might be better explained when the gain stages are replaced by simple transistor models. Here we assume CE stages for both input and output stages, which is sufficient to illustrate the idea of matching. Looking at Fig 4.18, only the most dominant components at high frequency are shown.

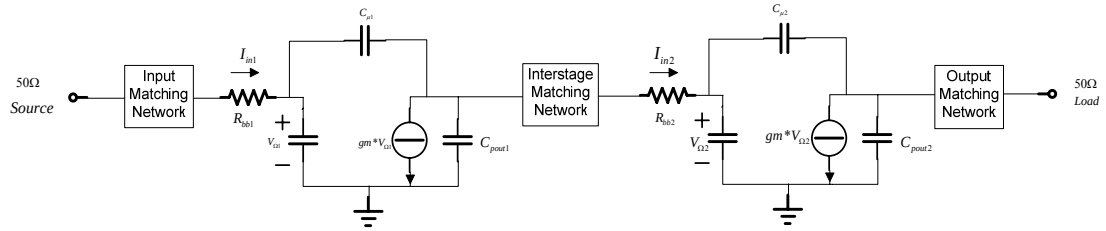

Fig 4.18 Model of the two stage antenna driver amplifier

Suppose the input of the first stage is conjugate matched to 50 Ohm source over a wide bandwidth, the current flowing into the base of input stage reaches maximum within this bandwidth according to maximum power transfer theory. However, since BE junction voltage V_π, which is effectively established on a capacitor, controls the output current I_c, V_π and I_c will show -20dB/dec drop over frequency since $V_\pi = I_\pi * \frac{1}{j\omega C_\pi}$. Output conjugate matching can not compensate for this roll off. So, the interstage matching should introduce the required peaking that compensates the roll off from both stages.

Various Matching Schemes for Peaking

At first, much effort was spent on various possibilities of interstage matching schemes. The structure of matching network determines the trajectory of its input impedance on smith chart as well as its frequency response. Depending on both the frequency at which the matching is achieved and the specific impedance trajectory of the matching network on smith chart, the frequency response of the matching network can be shaped according to our need. Through careful tuning, it is possible to shape such a frequency response that it peaks at high end of the

band and compensates the roll off nicely and renders little ripple. If this is indeed feasible, then even more stages can be cascaded without sacrificing the bandwidth a lot. But unfortunately, this idea is hampered by some practical concerns.

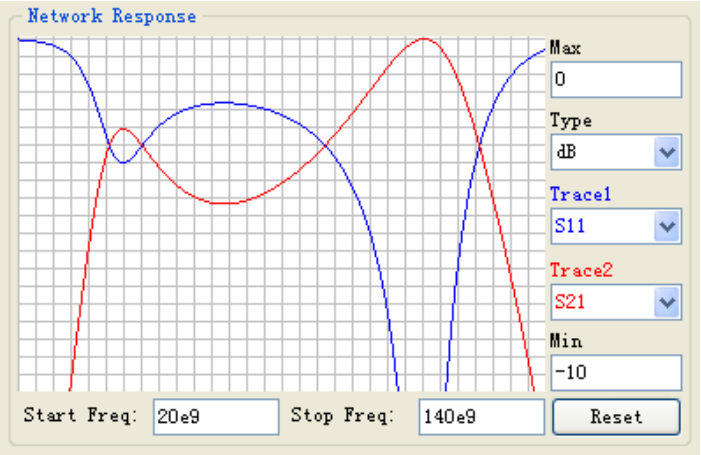

Fig 4.19 The frequency response of a typical interstage matching oriented for gain peaking

The interstage matching network plus the capacitance at its ends make up a network that resembles the form of a band pass filter. The frequency response that shapes the overall response most flatly often looks like the one depicted in Fig 4.19. Conjugate matching is done at 112GHz. The segment of transfer curve between the two peaks is the in band response we need, which is shown as a concave curve. But at the same time, there is a second peak at lower frequency, probably around 40GHz. Since the transistor has much higher gain at lower frequency, signal around that frequency peaks quite significantly, in some cases even stronger than signal in W band. This may be a problem since the drastic gain variation due to resonance could lead to oscillation. The resulting high voltage swing outside the band of interest may exceed the breakdown limit. Besides, this interstage matching scheme usually results in much higher bandwidth than required. As a result, unwanted spurs from the up-conversion chain experiences more gain, which is not intended. Fig 4.20 illustrates the above findings. The voltage component at fundamental frequency at the collectors of two stages and the output nod are depicted. Although practical decoupling network can suppress this low frequency peak to some extent, it still remains an uncertainly.

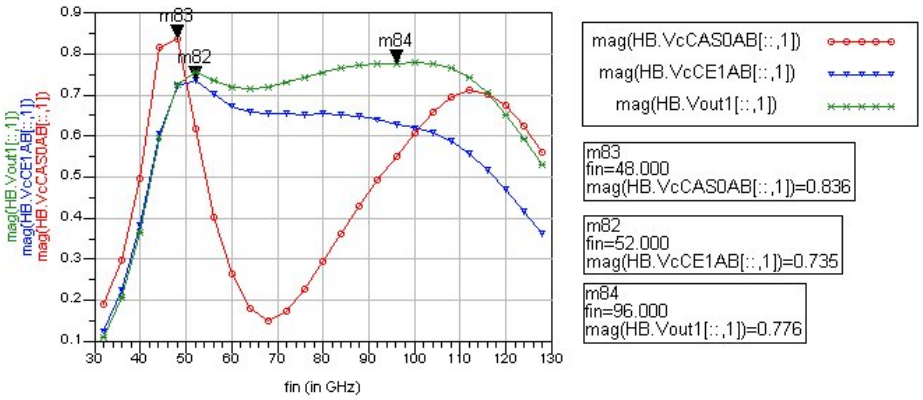

Fig 4.20 The voltage at different points with a typical interstage matching oriented for gain peaking

Other conjugate matching schemes result in curvier in-band response but do not have the problem of a second peak at lower frequency, such as the one shown in Fig 4.21n, which is shown as a convex curve.

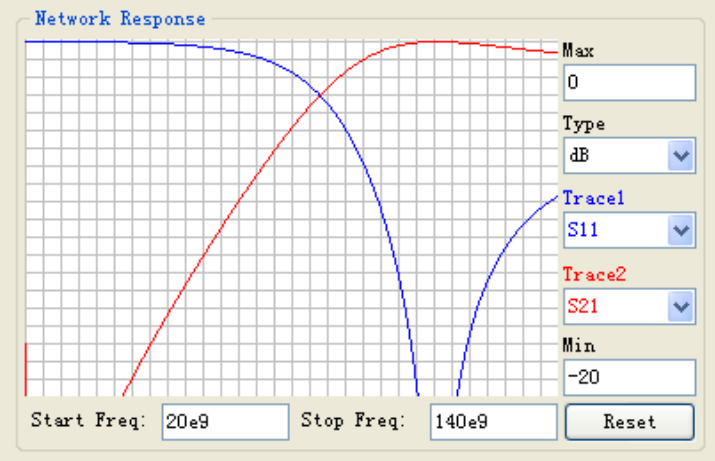

Fig 4.21 The frequency response of a typical interstage matching not introducing a low frequency peak

Power Matching or Impedance Matching

The potential problems related to the interstage matching scheme that orients toward a flat overall response makes it less attractive to be adopted. Other impedance matching networks could not give a flat overall response either. This leads us to evaluate whether power matching based on loadline theory can be used here to both render a higher gain and a relatively flat overall response. Loadpull simulation is conducted to the input cascode stage with wideband input matching. Table 4.1 shows the optimum load impedance Zld,opt, the maximum gain Gmax and the output impedance Zout across the frequency band.

Table 4.1 Zld,opt, Gmax, Zout of the input stage across the frequency band.

Freq (GHz)	Zld,opt(Ohms)	Gmax(dB)	Zout(Ohms)
80	23.7+j*50	11.7	3.8-j*71.4
88	23.5+j*50.1	11.2	5.1-j*63.6
96	23.4+j*50.1	10.4	6.4-j*57.3
104	23.3+j*50.4	9.5	7.5-j*52
112	23.4+j*50or19.1+j*41	8.3	8.5-j*47.7
120	19.1+j*41	7.3	9.5-j*43.9

Referring to Table 4.1, load impedance for power matching is different from the load impedance for conjugate matching. Greater difference exists between the real parts than between the imaginary parts. Zld,opt remains pretty constant from 80GHz to 112GHz.

Fig 4.22 shows the different load impedance positions for these two situations. Actually these two points are not so far part. A same topology matching network only with different component values can used for matching to both these points. Results show that the power match case renders about 2dB higher peak output power, and the in-band variation is about 1dB higher than the conjugate matching one.

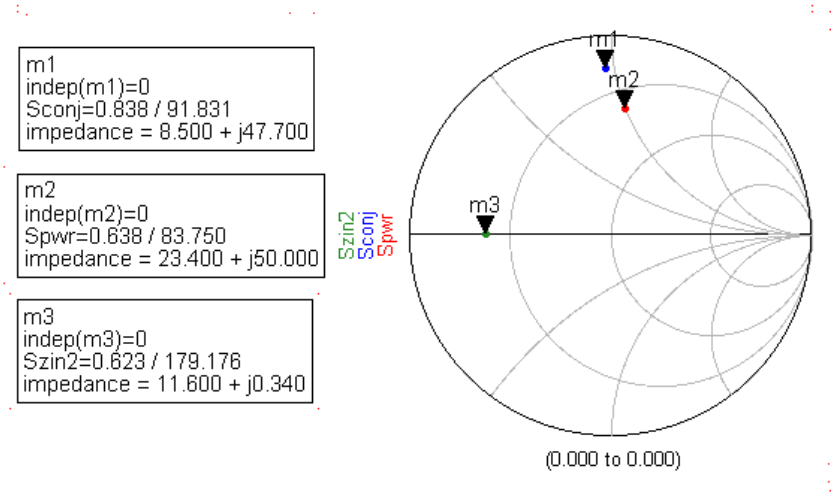

Fig 4.22 Difference of load impedance between conjugate matching and power matching

It can be seen on Fig 4.22 that the load impedance point for conjugate matching is closer to the edge of the smith chart. The bias functionality as well as the impedance trajectory determines the network topology. Since the end points of two matching schemes are near each other, they share the same topology. The difference is the component value. Smaller component value is required to reach the conjugate matching point. Although the on-chip passive components can be used to match to that point, it is still a less favorable choice. The reason is that it is difficult to realize AC ground at high frequencies. The parasitic impedance from the ground path can easily affect the matching network. By comparison, power match is more robust against those effects. So, considering the effectiveness of shaping frequency response, the stability issue, as well as the robustness of the matching network, we design the interstage matching network based on power match.

4.4.4 Circuit Topology and Component Value

Referring to the data shown in Table 4.1, interstage matching networks have been designed at different center frequencies to examine their effect on the overall response. It is found that matching at high end of band, 112GHz, results in a better shaped overall response. Topology of the whole antenna driver amplifier is plotted in Fig 4.23. Component values are summarized in Table 4.2.

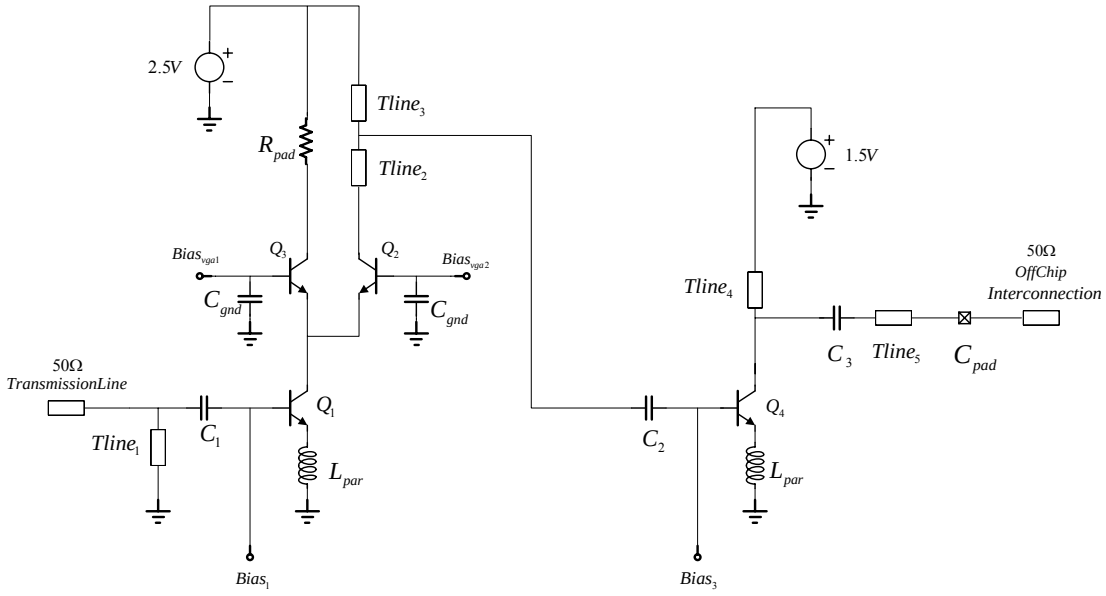

Fig 4.23 Topology of antenna driver amplifier

Table 4.2 Component value of antenna driver amplifier

Transistors			
Number	Emitter Length(um)	Multiplicity	Icollector(mA)
Q1	6	2	12.8
Q2	6	2	12.8(maximum/nomial)
Q3	6	2	0.01(minimum/nominal)
Q4	5	4	21.4

Transmission Lines						
Number	Width(um)	Length(um)	Shield Spaceing(um)	Beta(1/meter)/ Evalfreq(GHz)	Electrical Length(deg)	Characteristic Impedance(Ohms)
Tline1	4	138	10.9	4155.8/96	32.9	60
Tline2	8	128	10.6	4838.6/112	35.5	50
Tline3	8	47	10.6	4838.6/112	13	50
Tline4	8	149	10.5	3981.2/92	34	50
Tline5	8	120	10.5	3981.2/92	27.4	50

Capacitors			
Number	Length(um)	Width(um)	Effective Capacitance(fF)
C1	8	11.1	92
C2	8.7	11.1	100
C3	8.7	11.1	100
Cpad	80	80	26.5

Supply and Bias Voltages	
Name	Value/Range
Supply for input stage	2.5V
Supply for output stage	1.5V
Bias for signal path cascode	2V
Bias for shunt path cascode	1.8V(nominal)~2.2V

Reliability issues have been considered when choosing the component dimensions. The transmission line width is chosen according to DC current electrical migration limits at 100 degrees. RMS current limits are normally much less strict than the DC limit. To avoid coupling between nearby transmission lines, top level shielding is used.

Small value of inductors (10pH) is inserted to the emittor to represent vias and local ground inductive parasitic. They are included in all the related simulations. Since we desire flip chip connection to the antenna, an octagon RF bondpad is added to the output port. It can be modeled as a capacitor to ground of constant value. In the simulation here, C3 is a MIM capacitor. MIM capacitor connected directly to the output demands ESD protection, but the capacitance related to the ESD diodes are too large to be absorbed by the matching network. So a custom capacitor consisting two metal layers should be made for the final design.

Decoupling of the supply is implemented with capacitors. Since the amplifier is single-ended, their value and the inductance value related to the supply path have strong impact on the actual performance of the matching networks and the amplifier. The matching network may need to be adjusted to incorporate the effect of these components. In most of the simulation here, decoupling is not included. Fig 3.32 in the next section shows the influence of a decoupling network. The component values in Table 4.2 are thus the “ideal” value. Any modification due to parasitic effect from supply decoupling should start from these values. The influence of the parasitic is also evaluated, and they will be taken into account in the final design.

4.4.5 Simulation Results

Simulation results with the ideal passive components and actual ones are compared in Fig 4.24 and Fig 4.25. As shown in Fig 4.24, harmonic balance simulation is performed to check the voltage at the input and output port as well as the collector nods of two stages. Real power delivered to each stage is calculated. The difference in the real power delivered to each stage can be attributed to insertion loss due to actual components. Data shows that the additional insertion loss of the interstage matching is about 1.5dB while that of the output matching is about 0.6dB. With actual components, the peak power delivered to the 50 Ohm load exceeds 7dBm at band center and the output power at band edge is about 4dBm.

LSSP simulation is performed to check the port reflection coefficients, S11 and S22, forward gain, S21, as well as reverse isolation S12. Referring to Fig 4.25, the input and output matching are optimized for low reflection within the bandwidth from 80GHz to 112GHz. Actual components reduces the overall gain by about 2dB across the band. Peak power gain with actual components exceeds 12dB, and the gain at band edges is about 3dB lower than at

the band center(96GHz). Reverse isolation is better than -40dB.

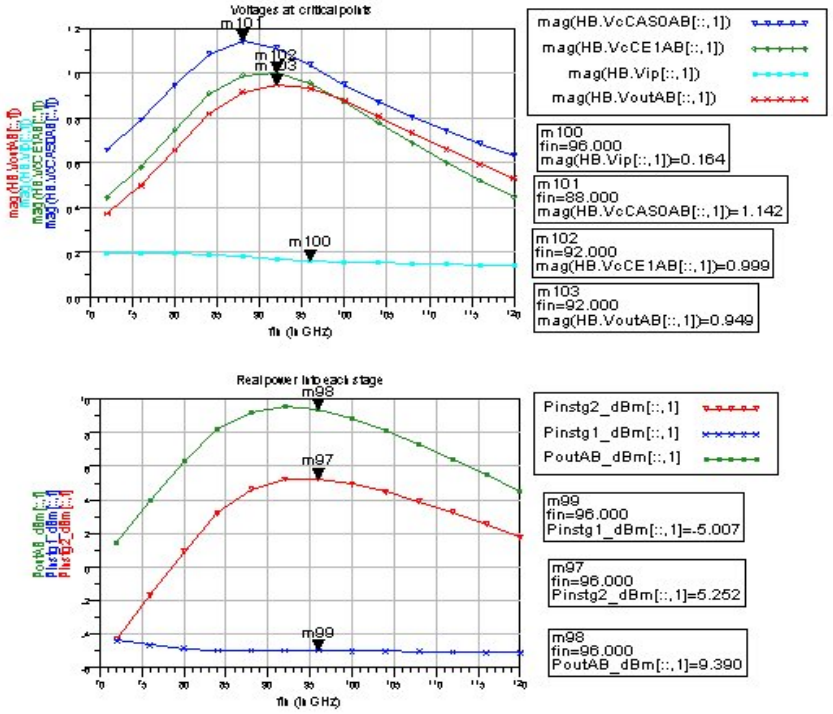

Fig 4.24(a) Voltage at critical points and power delivered to each stage in the antenna buffer, with ideal passive components

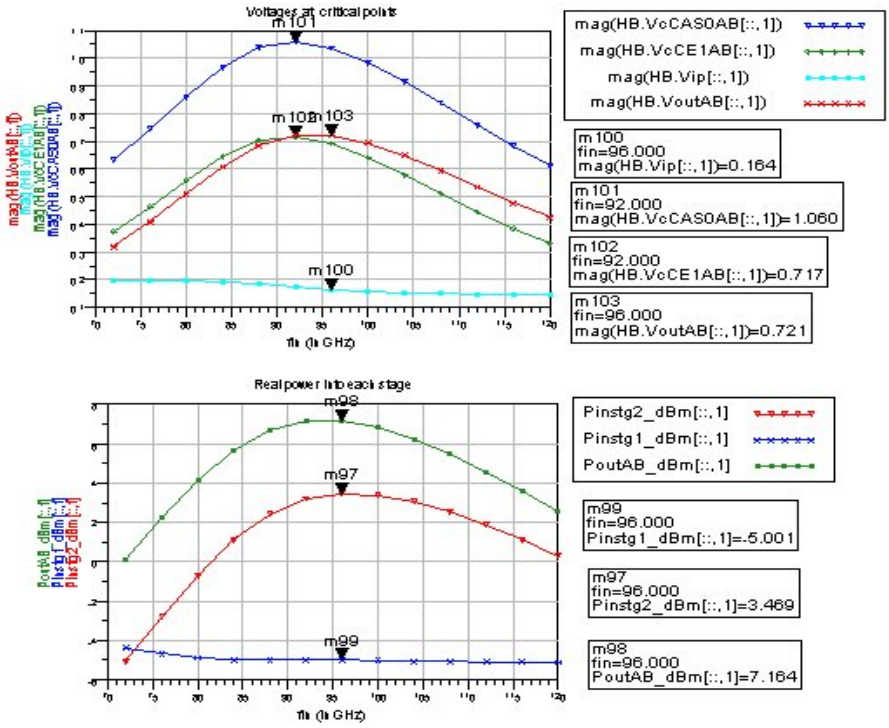

Fig 4.24(b) Voltage at critical points and power delivered to each stage in the antenna buffer, with actual passive components

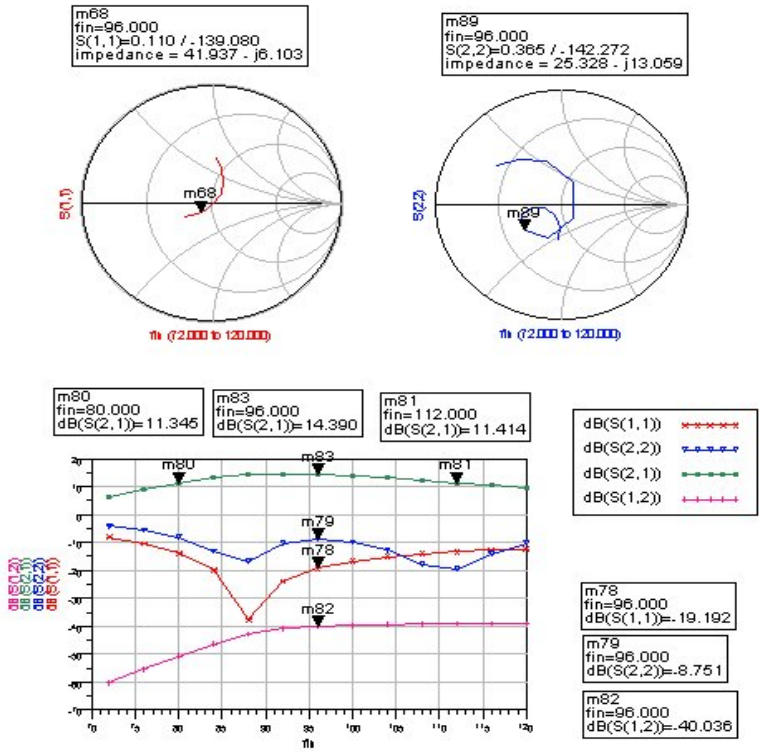

Fig 4.25(a) Large signal S parameter simulation results of the antenna buffer with ideal passive components

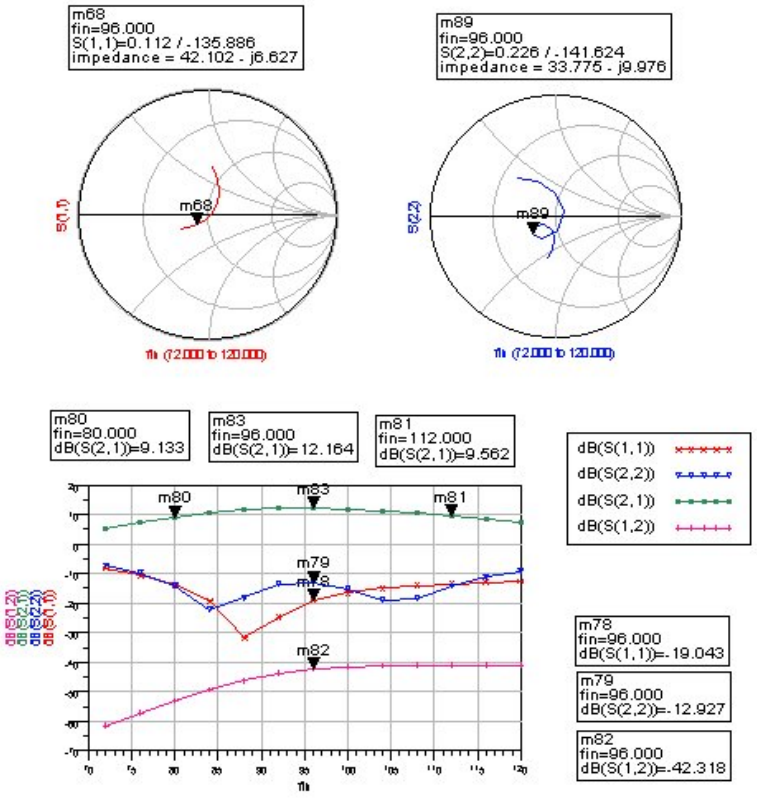

Fig 4.25(b) Large signal S parameter simulation results of the antenna buffer with actual passive components

Further simulations are based on actual passive components from the design kit. The loadline of 3 transistors composing the antenna driver is shown in Fig 4.26. The input power is the nominal value of -5dBm. The cascode transistor in the input stage is under the highest collector to emitter voltage swing. Non-conjugate match results in a more round-shaped loadline. The DC collector to emitter voltage left for the cascode device is 1.4V, which leaves 1.1V for the lower transistor to guarantee current gain at high frequency. We observe saturation of the cascode transistor when CE voltage swings down to 0.6V. To correct this, supply voltage has to be increased.

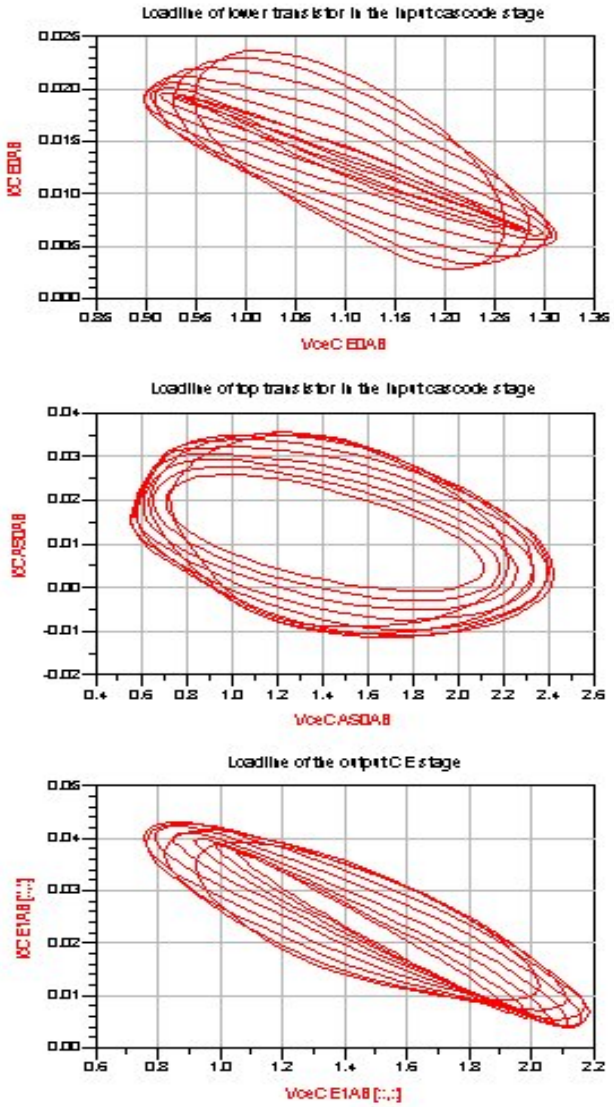

Fig 4.26 Loadline of 3 transistors in the antenna buffer, input power used for simulation is -5dBm

The amplifier response over power sweep is shown in Fig 4.27 and 4.28. Fig 4.27 shows the in band frequency response of the antenna buffer with +/-3dB input power variation. The difference in output power is less than the variation of the input power, which indicates compression. This is verified with 1dB compression point simulation at 96GHz. Fig 4.28

shows that the input referred compression point is at -9dBm. It is mainly limited by the input stage. Input stage should be scaled up to push the compression point higher. However, larger input stage poses stricter requirement on its decoupling and bias of the cascode transistor.

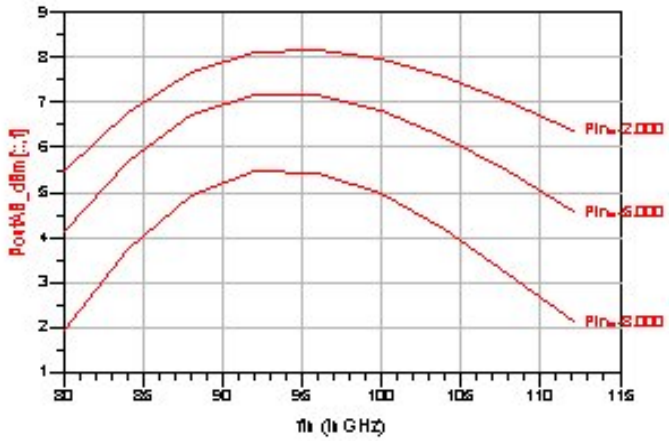

Fig 4.27 In band frequency response of the antenna buffer with +/-3dB input power variation.

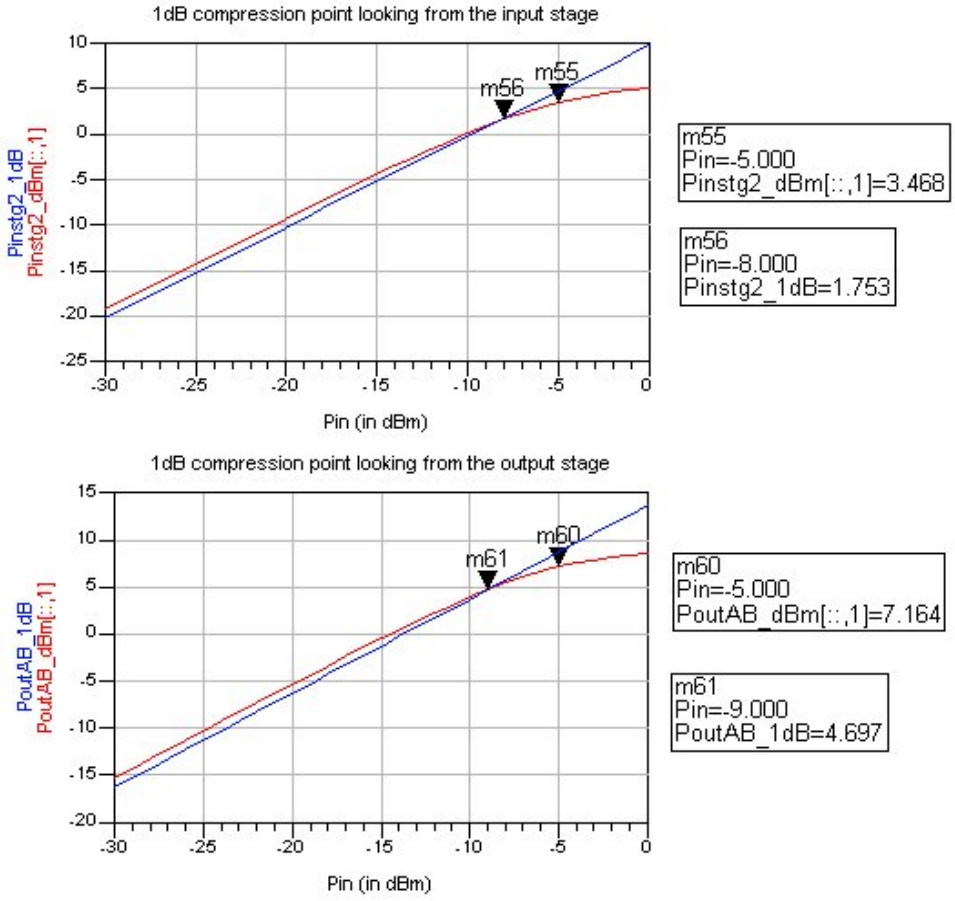

Fig 4.28 1dB compression point seen at the output of the input stage and output stage

The influence of local ground inductance is shown in Fig 4.29. Inductance from via and interconnects at the emitter of a CE stage degenerates the stage. It modifies the input impedance and changes the gain. At high frequency, even several pH of inductance makes a difference. So, we have budgeted 10pH of inductance at the emitter of each stage to represent the local inductive parasitic. Simulation results show that even when considered in the design, 10pH variation of ground inductance causes the peak power to change more than 1dB. The frequency response shape of the output power does not change a lot with this amount of parasitic.

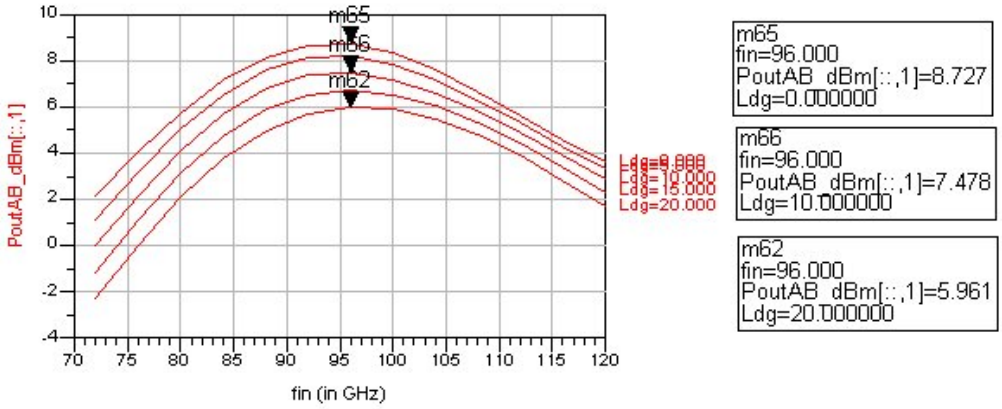

Fig 4.29 Influence of local ground path inductance

Amplifier gain can be adjusted with the base bias of the shunt transistor, the result is shown in Fig 4.30. By tuning the base bias of the shunt cascode transistor Q3, it operates from completely turned off to turned on. By diverting away the RF signal from the signal path cascode transistor. It provides variable gain control function to this amplifier. As is depicted in Fig 4.30, within the bias voltage tuning range from 1.8V to 2.22V, the overall output power shows variation of more than 20dB. Further increase of that voltage reduces the DC current of the signal path cascode device to the point that the matching is affected. As a result, the shape of overall frequency response does not preserve any more. The useful tuning range of that base bias voltage is hence from 1.8V to about 2.2V. The corresponding peak output power varies from 7.2dBm to -11.1dBm.

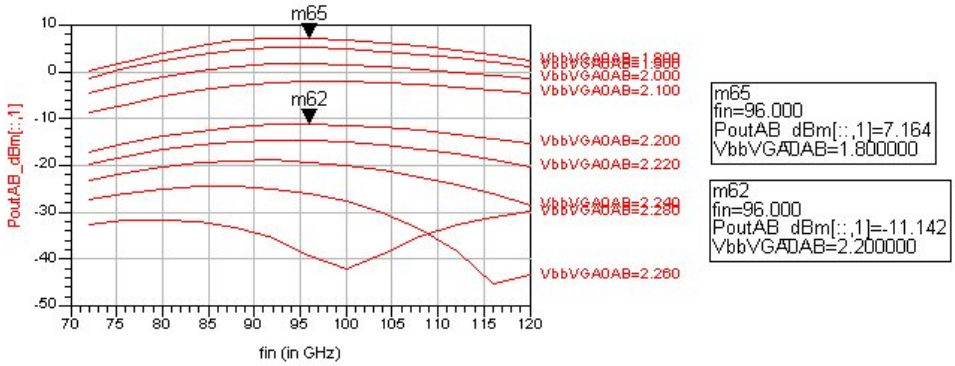

Fig 4.30 Tuning range of the output signal power

A passive network modeling the supply path and decoupling, shown in Fig 4.31, is included to check its influence on amplifier performance. If the test chip is meant for on wafer probing, this network can be simplified. But the key point is to model the large inductance introduced through the bias path.

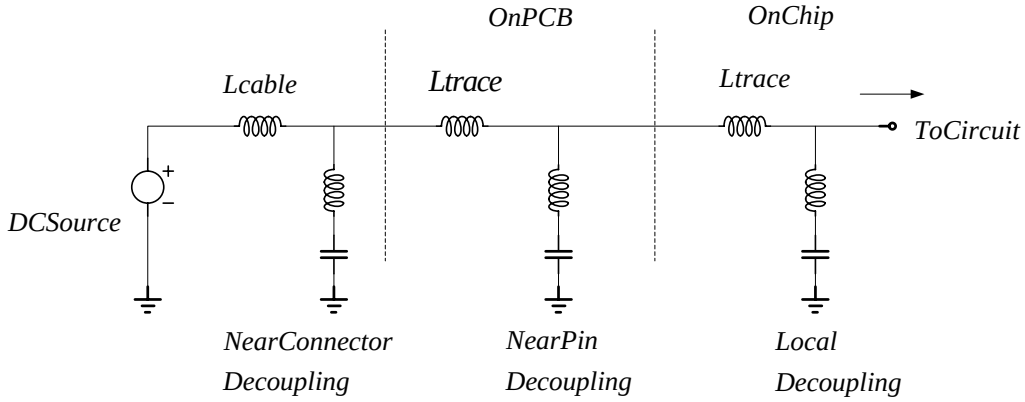

Fig 4.31 Model of supply path

Fig 4.32 shows the frequency response with and without the decoupling network. We can observe that the performance of the matching networks and the whole amplifier is indeed affected. This issue should be solved by designing the decoupling network carefully.

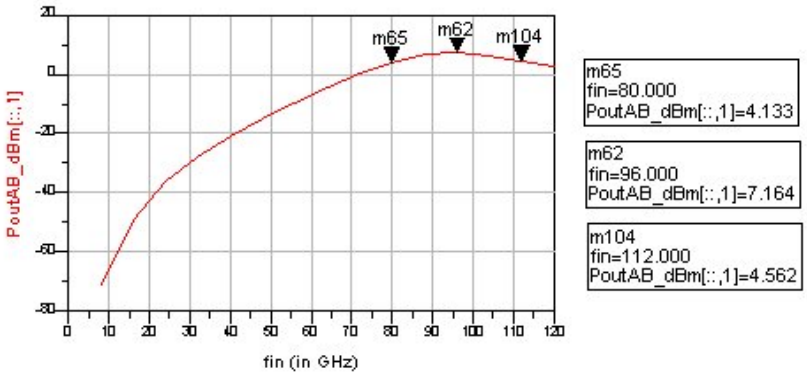

Fig 4.32(a) Frequency response with ideal AC ground at supply

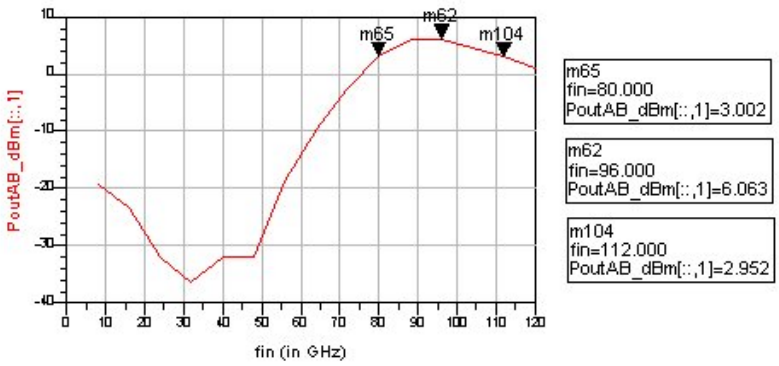

Fig 4.32(b) Frequency response with supply decoupling

Transient simulations with both sinusoidal and step input are conducted with the decoupling network to check stability. For this two stage amplifier, we do not choose stability factors base on small signal simulation as a proof of stability. Transient simulation provides a more realistic check. Since parasitic components have a strong impact on stability performance of the amplifier, stability check should always include supply and decoupling components.

Fig 4.33 shows the step response wave form at several points. Oscillation at the collector of the cascode transistor damps within several ns. It's frequency is about 5GHz. It is found that this oscillation stems from the on chip decoupling network. Further improvement should be made both to guarantee the RF performance of the amplifier and to avoid any oscillation at all frequencies.

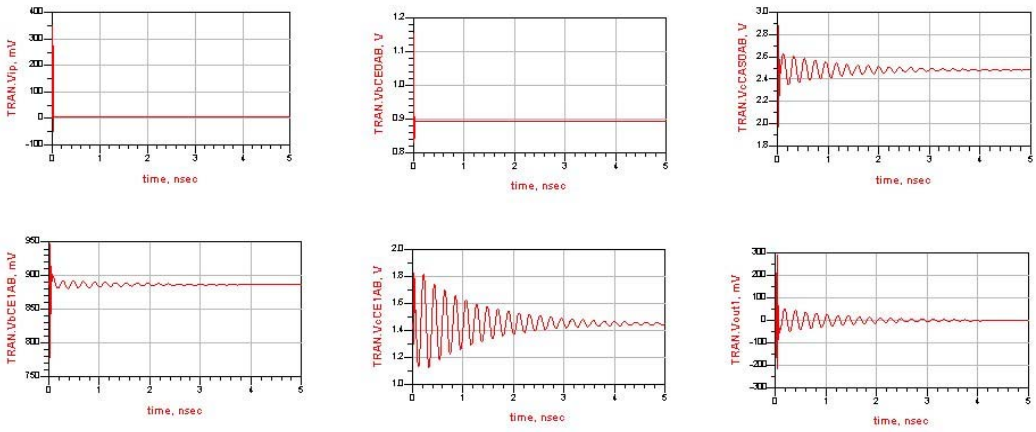

Fig 4.33 Transient simulation with decoupling network

The 2 stage amplifier draws 34mA in total from two supply voltages, 2.5V and 1.5V. Suppose the two biases are derived from a single 2.5V supply, the total DC power consumed is 85mW.

Some performances of the antenna driver amplifier with ideal supply are summarized in Table 4.3.

Table 4.3 Performance of the antenna driver amplifier with ideal supply

Operation band	80GHz ~ 112GHz
Nominal input power	-5dBm
In-band power gain variation	8dB ~ 11.3dB
Input referred 1dB Compression point @ 96GHz	-9dBm
Input reflection coefficient	<-15dBm
Output reflection coefficient	<-12dBm
DC current consumption	34mA

4.5 LO Driver

The LO driver is a differential amplifier. It provides the wideband LO drive signal to the double balanced down conversion mixer. It is preceded by a ratrace hybrid for generating differential input signal.

4.5.1 Performance Requirements

Simulation of the multiply by 8 chain shows that the power delivered to 50 Ohm load by the ratrace varies from -10.7dBm to -8.2dBm in the band. We choose -9dBm as the nominal input signal delivered to the LO buffer.

The output power required by the Mixer LO port is determined by simulation. A double balanced Gilbert Mixer designed previously [10] is used for simulation. It is found that the input impedance of LO port is affected by the source and load impedance at the RF port and the IF port of the mixer. Since the circuit at the IF path is not been finalized yet, the input impedance at the LO port may also change due to further adjustment of the circuit. To build the wideband LO driver, an accurate LO port impedance is important for designing matching network. As a result, this version of LO driver is not the finalized one. Through its design, we have investigated different matching schemes and found better suited one, we have also examined the amount of gain from the transistors, the loss in the matching network. Further adjustment will be made on the basis of this design.

To determine the LO port impedance, large-signal S parameter simulation was performed. 50 Ohm source impedance is connected at each RF port of the mixer. At the IF port, source follower with level shifting function buffers 50 Ohm load impedance. The LO input impedance is simulated over a large frequency range, Fig 4.34 shows the results. It seems that the input impedance of the LO port can be roughly modeled with a series RC branch over a large bandwidth. Simulation show that altering the input power to the LO port does not affect its input impedance a lot. So, we choose this RC branch as a approximating model of the input impedance. Output matching of the LO buffer is first designed with this model, then the LO driver is connected to the mixer and the output matching is adjusted to improve the performance.

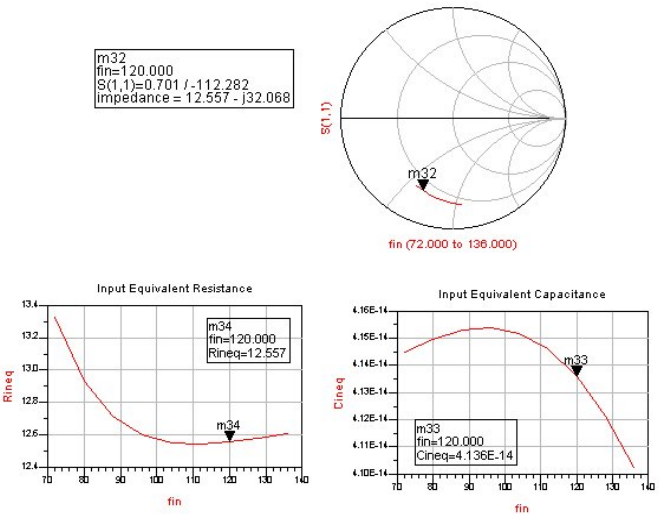

Fig 4.34 Input reflection and equivalent RC component value of the mixer LO port, LSSP simulation is performed with 50Ohms source impedance and -5dBm source power

According to Mao's design [10], a power source with 50 Ohms source impedance was used as LO driver. The nominal power under matching is -5dBm. The fundamental voltage and current signal at the LO port at 96GHz was used as the quantity for comparison. Fig 4.35 shows the waveform and the fundamental content of the voltage and current at the LO port, as well as the collector current in one of the switching quad transistors from 80GHz to 112GHz. With this ideal signal source, the collector current swing of the switching quad transistors roll off with frequency. The current that flows into the LO ports remains relatively constant in this case.

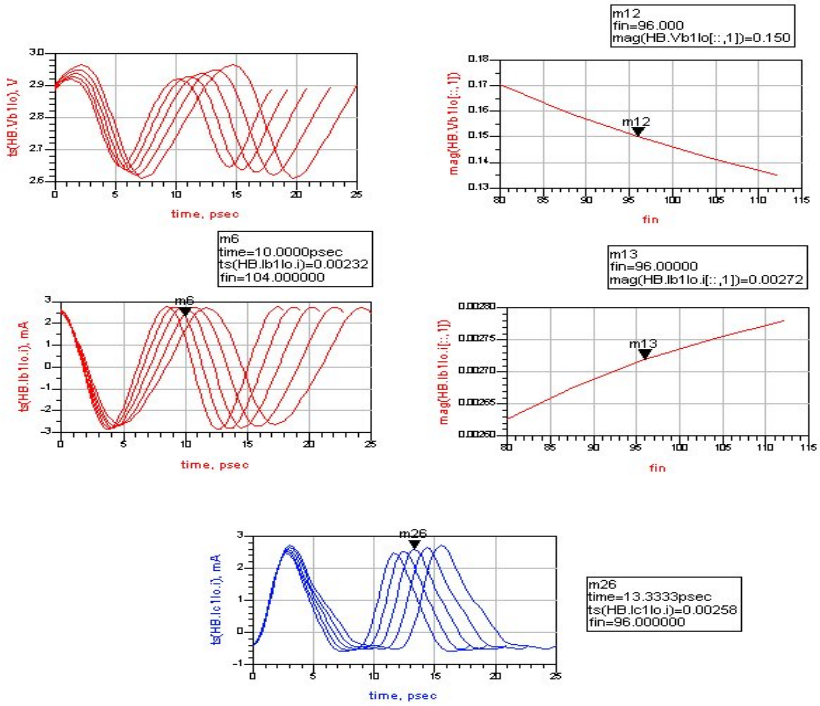

Fig 4.35 Waveform and the fundamental content of the voltage and current at the LO port and the collector current in one of the switching quad transistors

4.5.2 Design Considerations

If the switching quad collector current swing is to be kept constant for flat mixer conversion gain frequency response, the current delivered to the LO ports should increase verses frequency. The LO driver should then produce a peaking output frequency response, and the peak should be at least at the high end of the band. The input impedance of the LO driver directly loads the ratrace hybrid. As already shown, the transfer function, as well as, the input port impedance of the ratrace is sensitive to its load impedance. So, the input of the LO driver should maintain wideband impedance match to ports of the ratrace. All gain peaking is achieved at the output of the LO driver. The planned matching scheme is plotted in Fig 4.36.

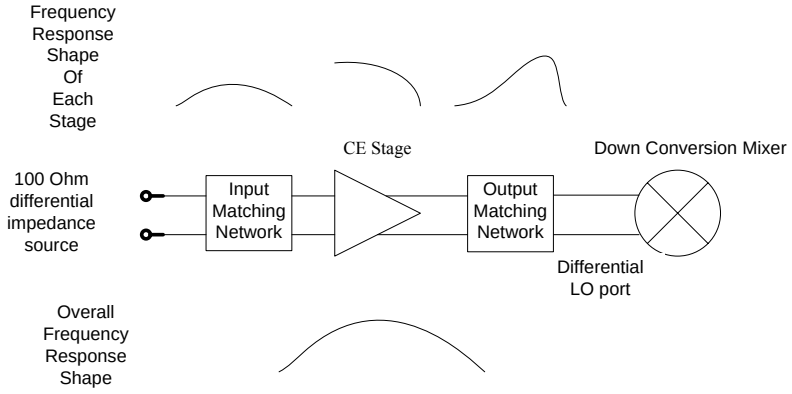

Fig 4.36 Frequency response of each stage and matching network of the mixer LO driver amplifier

Considering the requirements by the mixer, we determined that the LO driver should provide higher than 150mV LO voltage swing throughout the whole band. The gain response should be kept as flat as possible to avoid much higher mixer conversion gain to signal at the band center.

From the design of the antenna buffer, we have seen that roughly 3 to 4dB of power gain can be expected from a CE stage with wideband output matching in our band of interest. Since the input power to the LO buffer is about -9dBm and the required output power is about -5dBm. Probably one CE stage can achieve the required gain here. The simulated peak output power from the 20um output stage of the antenna buffer above is 7dBm, referring to Fig 3.24. It is 12dB, or 4 times, higher than the required -5dBm input power required by the mixer LO port. If we scale the transistor just by this power relation, then emitter length for the LO driver should be 20/4=5um. But, in this simple derivation we assumed conjugate match at output. Furthermore, output matching at high end of the band causes mismatch at lower frequencies and results in lower gain. The matching network also introduces some losses. Considering these losses, we first choose an 8u emitter length transistor for the LO driver.

Exactly at which frequency to design the peak passive gain through matching involves the trade off between gain flatness and peak gain. Matching at a lower frequency does not provide enough peaking at the high end of the band. Matching at too high frequency results in too

much suppression, especially to the signal at lower end. Several attempts where made to find a balance point of the matching frequency. Meanwhile, the topology of the output matching network, which affects the Q factor of it, also plays an important role in determining the overall frequency response. AC coupling and biasing through the matching network is also taken into consideration. For the CE stage, load pull simulation is performed. It verifies that the load impedance for conjugate matching is close to the impedance for optimum power matching based on loadline theory in a Class A amplifier. We utilize conjugate impedance matching here.

4.5.3 Circuit Topology and Component Value

We come to the matching network as shown in Fig 4.37. The input matching provides lower than 15dB input reflection throughout the band. The conjugate output matching is achieved at 120GHz, which is already outside our band of interest. Fig 4.37 shows only half of the differential pair. 2.5V supply voltage suits the differential pair with a tail current source. Considering the reduced signal swing requirement, break down voltage wouldn't be a problem to the LO buffer. Simple base biasing should be sufficient at this point. But further improvement against temperature and process variation is necessary. 5pH of parasitic is budgeted at the emitter to model local interconnect. The component values are summarized in Table 4.4.

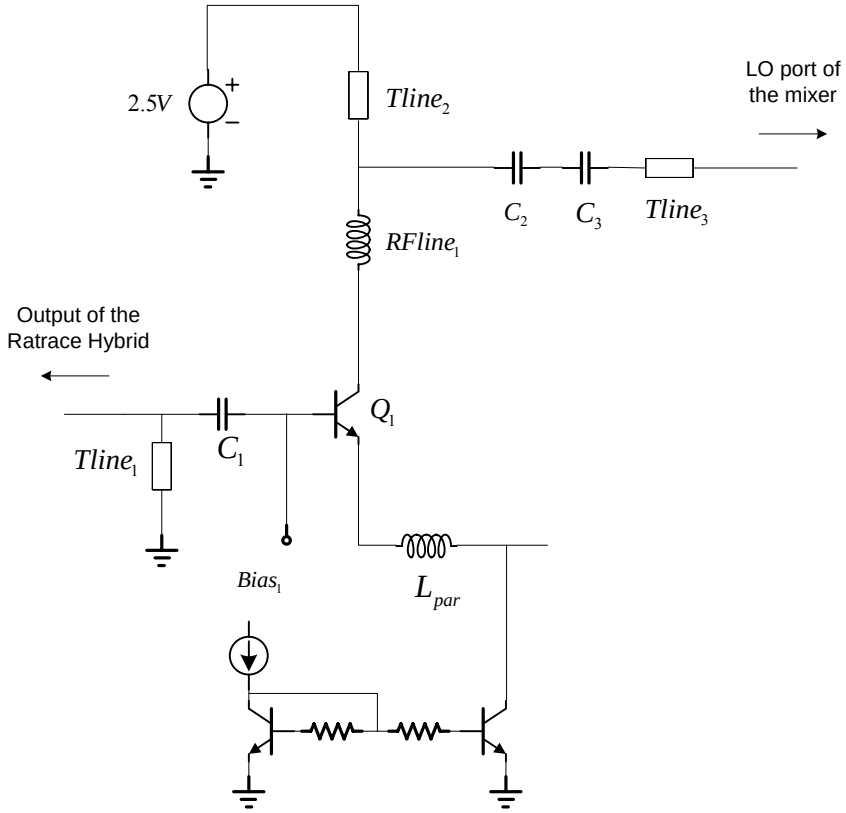

Fig 4.37 Circuit topology of the LO driver (only half of the differential circuit is shown)

Table 4.4 Component value of LO driver amplifier

Transistors			
Num	Emitter length(um)	Multiplicity	Icollector(mA)
Q1	4	2	7.9

Transmission Lines						
Number	Width(um)	Length(um)	Shield spacing(um)	Beta(1/meter)/ Evalfreq(GHz)	electrical length(deg)	Characteristic Impedance(Ohms)
Tline1	5	125	13.3	3804.6/88	27.2	60
Tline2	5	111	7.04	5208.8/120	33.1	50
Tline3	5	69	7.04	5208.8/120	20.6	50

Rfline			
Number	Width(um)	Length(um)	Effective inductance(pH)/Evalfreq(GHz)
RFline1	5	115	83/120

Capacitors			
Num	Length(um)	Width(um)	Effective Capacitance(fF)
C1	8	11.1	92
C2	12.1	12.1	150.5
C3	12.1	12.1	150.5

Supply and Bias Voltages	
Name	Value/Range
Supply voltage	2.5V
Bias at the base of the differential pair	2V

The operation frequency of this amplifier far exceeds the self resonant frequency of on chip spiral inductor. Due to its large footprint and capacitive coupling between metal lines, spiral inductor is not suitable to realize low inductance values at very high frequency with a decent Q factor.

The on chip transmission line available in the library takes the forms of a microstrip line or a coplanar waveguide-like structure depending on whether top metal ground is utilized. Both of these two types have a ground plane at lower metal layer. However, the capacitive coupling between signal line and ground line reduces the effective inductance from a segment of transmission line.

Rfline provided by the library is dedicated to synthesize small value of inductance with high Q factor at very high frequency. It consists of signal line on top metal layer and a cross hatch of deep trench. Since the low resistance substrate is blocked, the Q factor of a sub 100pH

inductor implemented with rfline exceeds 40 in W Band. After comparing these structures, we choose rfline to implement inductor for our matching network.

4.5.4 Simulation Results

Simulation is performed with both ideal and actual passive elements. The following results are simulated with the down conversion mixer as the load. Some of actual components are adjusted to improve the performance a bit. Fig 4.38 shows the fundamental signal voltage at several points, the input power to the LO buffer and the real power delivered to the LO port of the mixer. Comparison shows that the input matching network with actual components introduces about 0.5dB more insertion loss, and the output matching alone introduces about 1.8dB more. Peak LO voltage component drops from 245mV to 186mV. The LO voltage at the band edge is just about 150mV with the actual passive components. The loss from the passive components is quite significant compared to the gain at this frequency range. Loadline confirms the decrease of both current and voltage swing, shown in Fig 4.39. The collector current waveforms of these two cases are plotted in Fig 3.40.

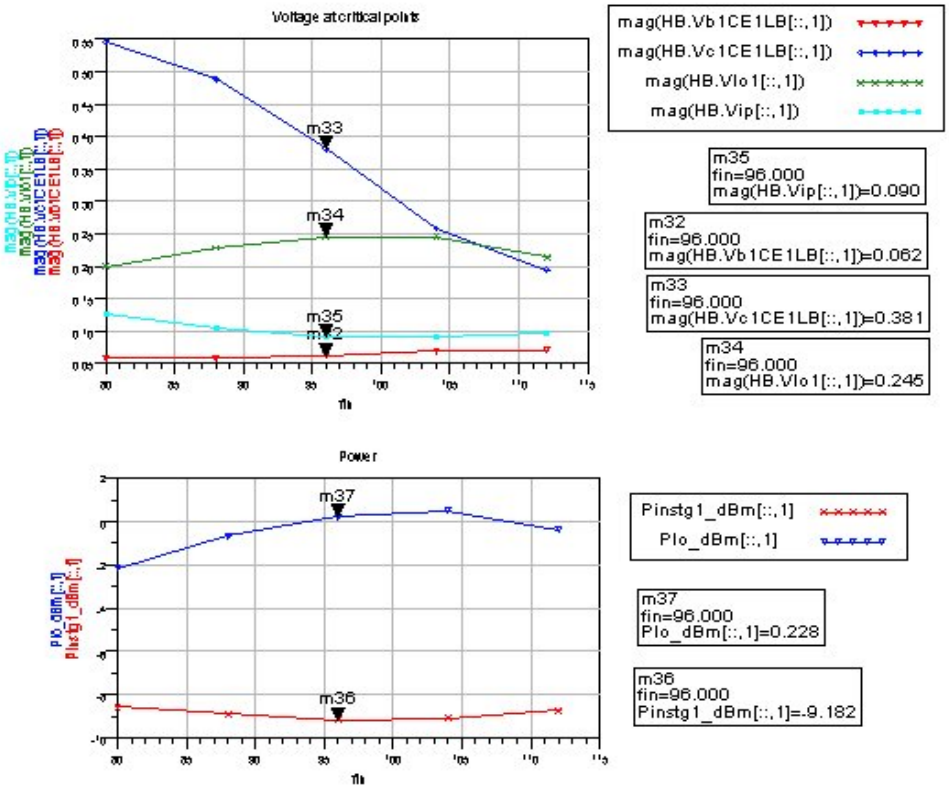

Fig 4.38(a) Voltage at critical points and input, output power of the LO driver, with ideal passive components

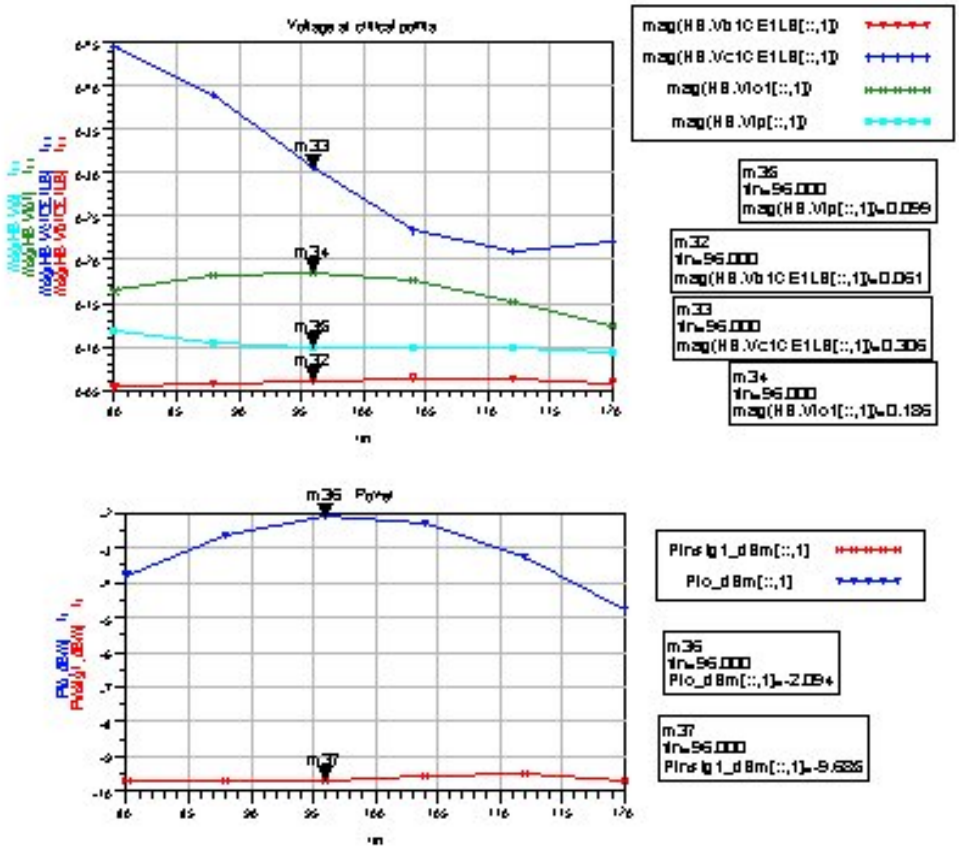

Fig 4.38(b) Voltage at critical points and input, output power of the LO driver, with actual passive components

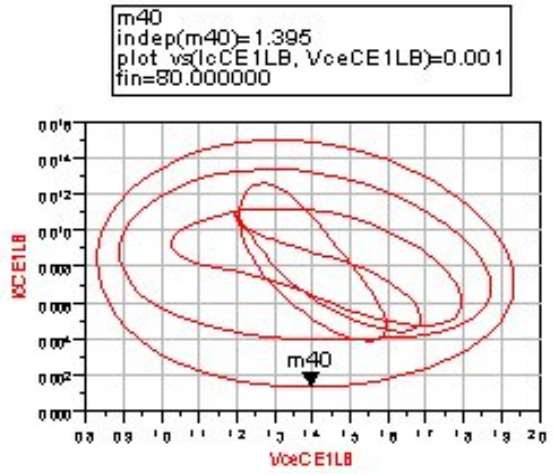

Fig 4.39(a) Load line with ideal passive components

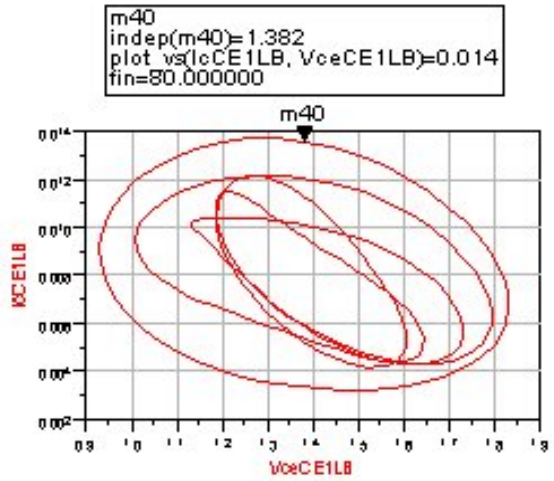

Fig 4.39(b) Load line with actual passive components

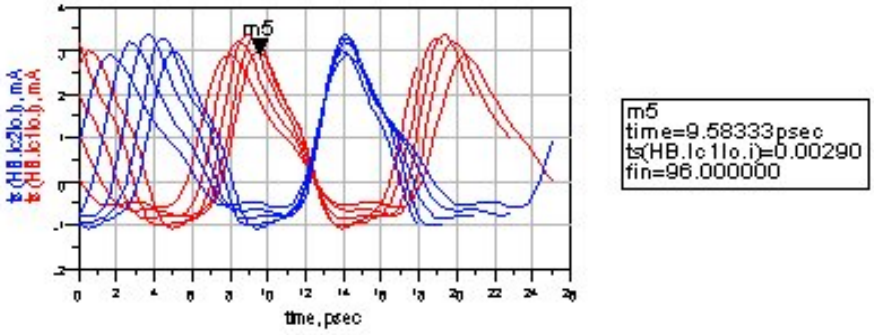

Fig 4.40(a) Mixer switching quad collector currents, with ideal passive components

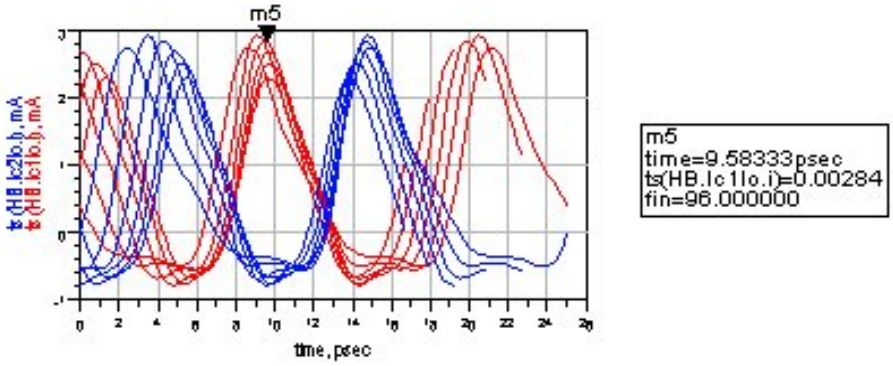

Fig 4.40(b) Mixer switching quad collector currents, with actual passive components

Input impedance of the LO driver is shown in Fig 4.41. Since the input matching network is kept as simple as possible to minimize the loss. Wideband matching is not optimized due to component value limits. Other matching network could result in better input matching to 50 Ohm source, but increased passive element counts would cause more loss. Depending on the sensitivity of the ratrace performance, a compromise should be made here.

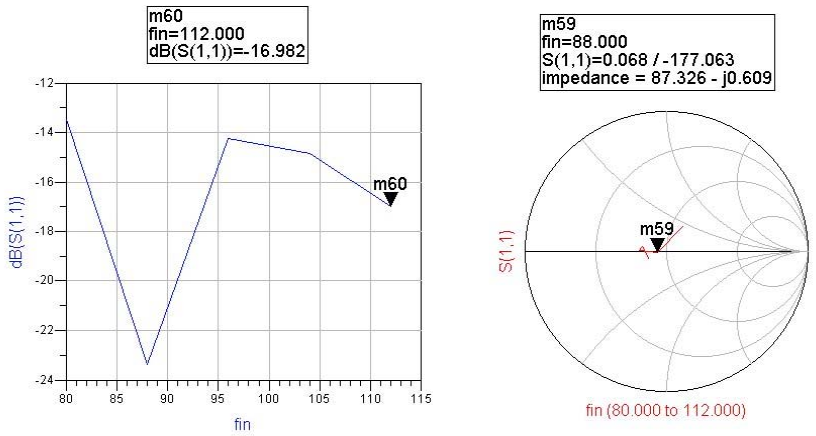

Fig 4.41(a) Input reflection with ideal passive components

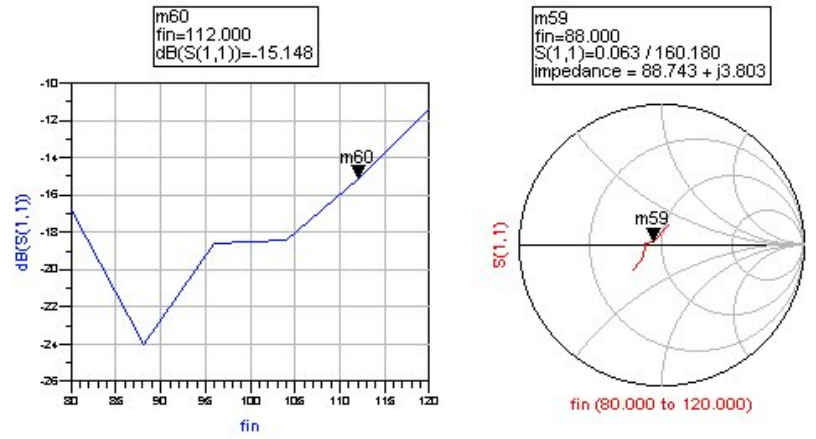

Fig 4.41(b) Input reflection with actual passive components

As shown in Fig 4.42(a), power sweep of +-3dB is performed. It seems that the circuit is not compressing within this input power range.

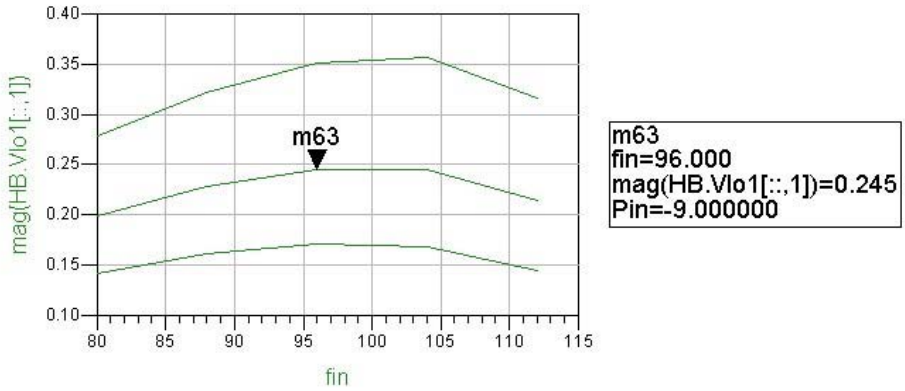

Fig 4.42(a) Input reflection with ideal passive components

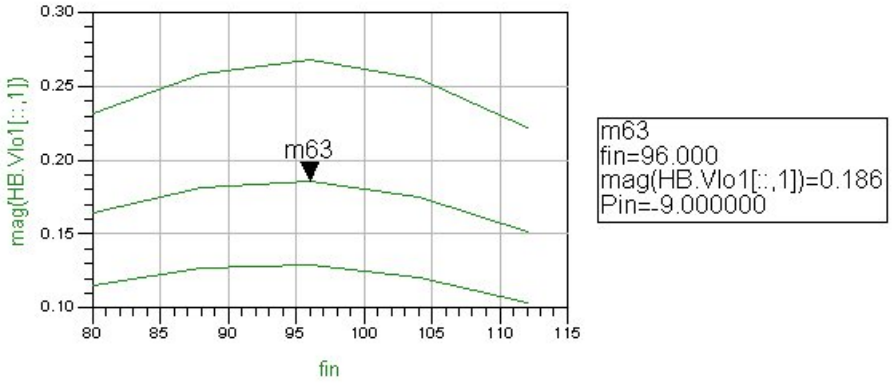

Fig 4.42(b) Input reflection with actual passive components

Simulation for the 1dB compression point at 96GHz confirms the above results. Shown in Fig 4.43, the output 1dB compression point of the amplifier with the actual components lies at about 1dBm.

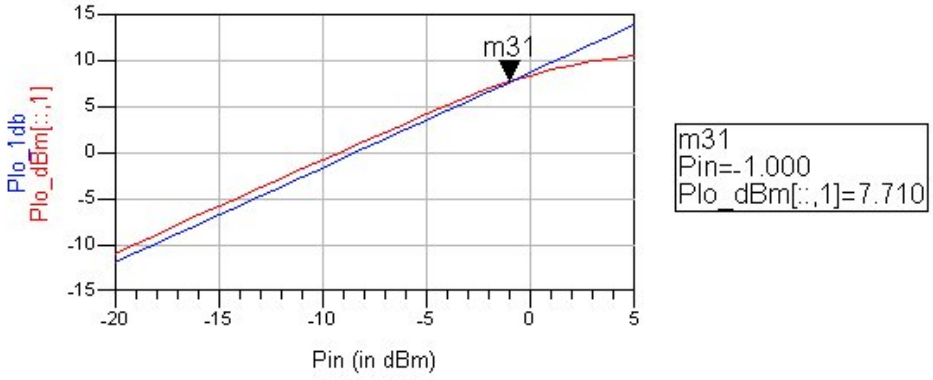

Fig 4.43(a) output 1dB compression point with ideal passive components @96GHz

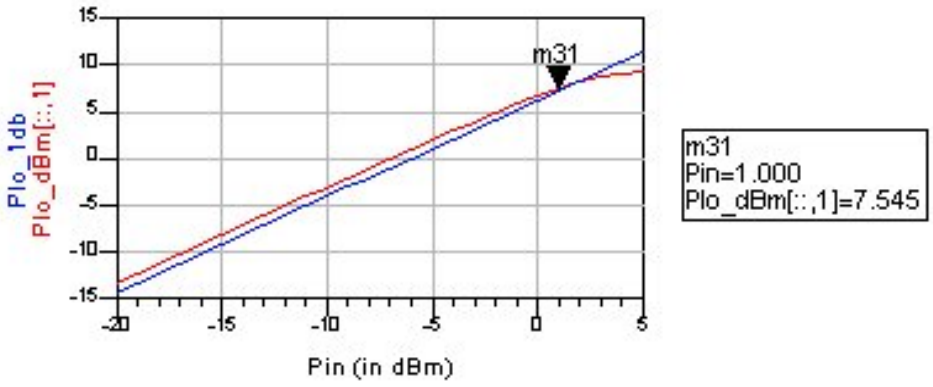

Fig 4.43(b) output 1dB compression point with actual passive components @96GHz

Since the LO driver is a differential amplifier, it can be made quite robust to the supply and ground path parasitic. If the supply and ground connection nods of the two branches are connected together, the AC current drawn from those nods will circulate in two branches. The parasitic at those nods would appear in common mode signal path only. As a result, the circuit performance almost does not change with the presence of those parasitic.

The LO driver amplifier draws 16mA in total from 2.5V supply. The DC power consumed is 40mW. Some performances of the LO driver amplifier are summarized in Table 4.5

Table 4.5 Performance of the LO driver amplifier

Operation band	80GHz ~ 112GHz
Nominal input power(single-end)	-9dBm
In-band power gain variation	5.2dB ~ 7dB
In-band LO signal voltage variation	151mV ~ 186mV
Input referred 1dB Compression point @ 96GHz	1dBm
Input reflection coefficient	<-15dBm
DC current consumption	16mA

4.6 Combined Simulation Results

After all the above mentioned circuit blocks operating in W band have been designed separately, they are connect together to examine whether they can work in harmony and to check the overall performance. Fig 4.44 shows the voltage at different points in both the antenna driver and the LO driver with ideal or actual power divider and ratrace. Fig 4.45 shows real power that flows in or out of each block, with ideal or actual power divider and ratrace. Some labels need a bit clarification:

PinPD means input power to the Power Divider.
PinAB means input power to the Antenna Buffer(Driver).
PoutAB means output power from the Antenna Buffer(Driver).
PinRR means input power to the Ratrace.
PinLB means input power to the LO Buffer(Driver).
PinLO means input power to the mixer LO port.

Since the actual power divider approximates the ideal one pretty close, the power level in the antenna driver remains close in these two situations. The ratrace on the other hand introduces more loss and is more sensitive to the termination impedance, hence the power delivered to the LO buffer reduces by about 0.8dB. The overall gain response is preserved. This verifies that terminating the Wilkinson power divider and the ratrace hybrid is indeed feasible. The inband output power variation of the antenna driver is about 3dB. And that of the LO driver is about 2dB.

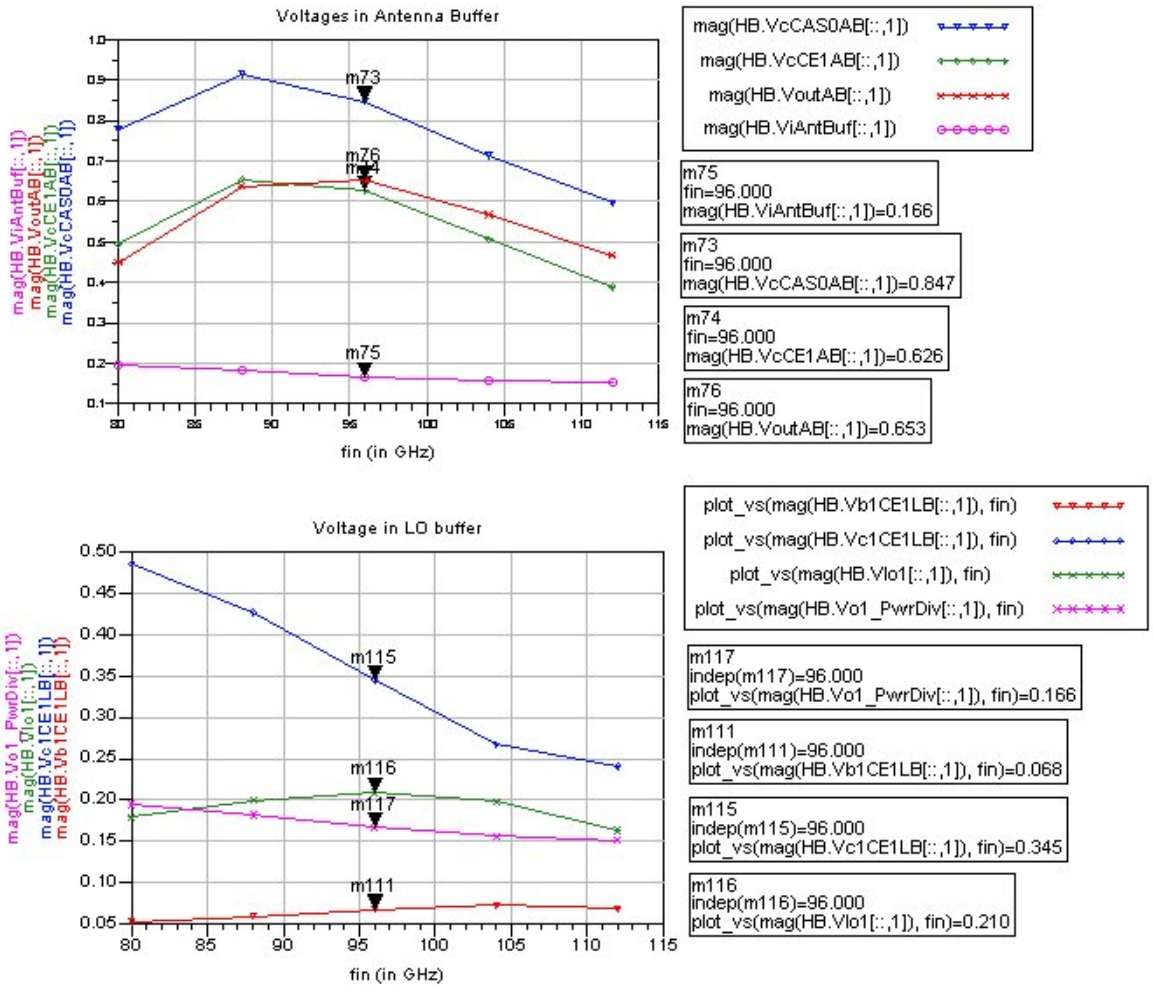

Fig 4.44(a) Voltage components at several points in circuit working in W band, with ideal Wilkinson power divider and ratrace hybrid

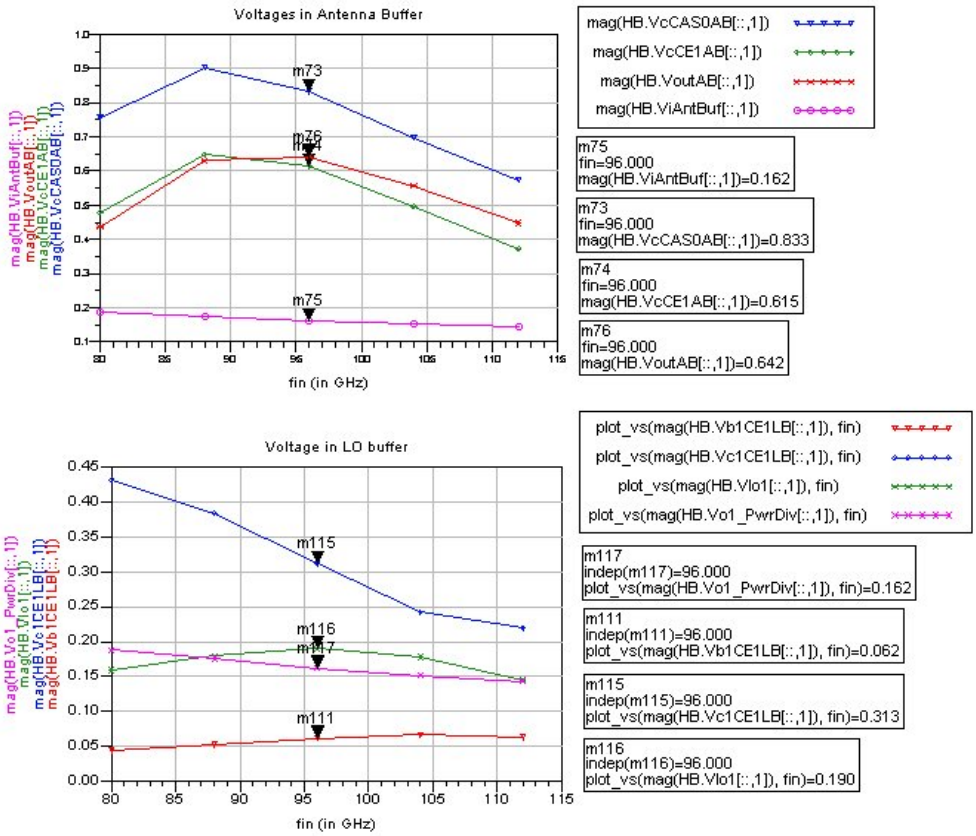

Fig 4.44(b) Voltage components at several points in circuit working in W band, with actual Wilkinson power divider and ratrace hybrid

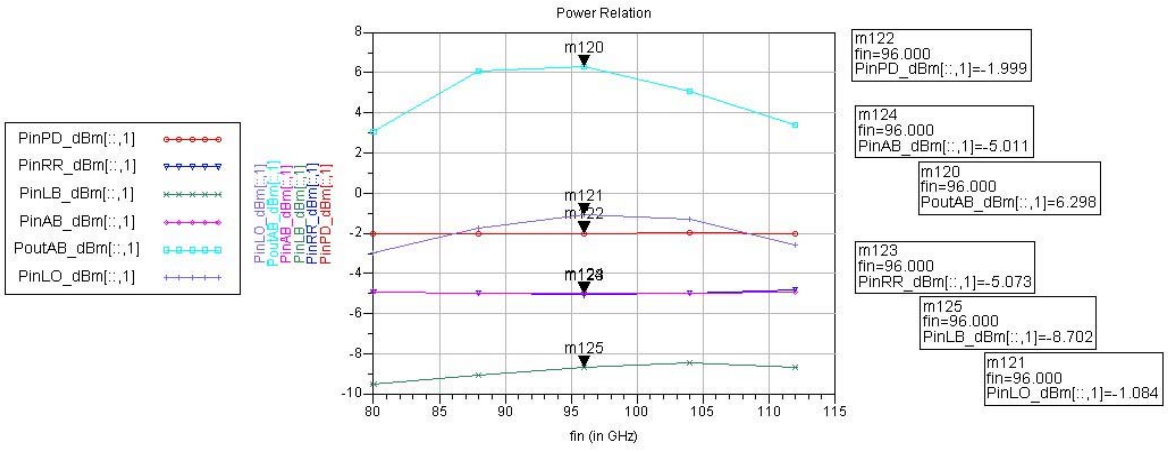

Fig 4.45(a) Power delivered to several points in circuit working in W band, with ideal Wilkinson power divider and ratrace hybrid

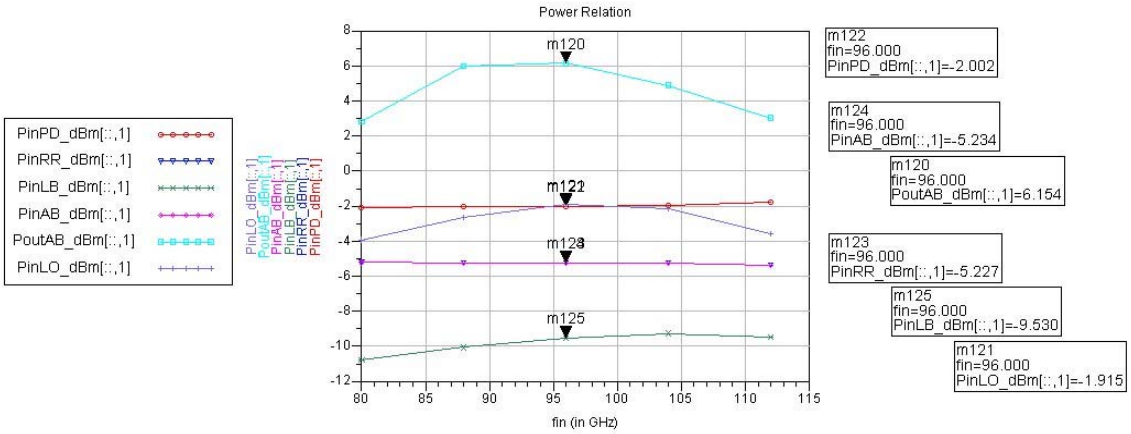

Fig 4.45(b) Power delivered to several points in circuit working in W band, with actual Wilkinson power divider and ratrace hybrid

Transient simulation is also carried out. A single tone sinusoidal excitation is applied at the input at 112GHz. Fig 4.46 shows the resulting wave forms at the output of the antenna driver and the mixer

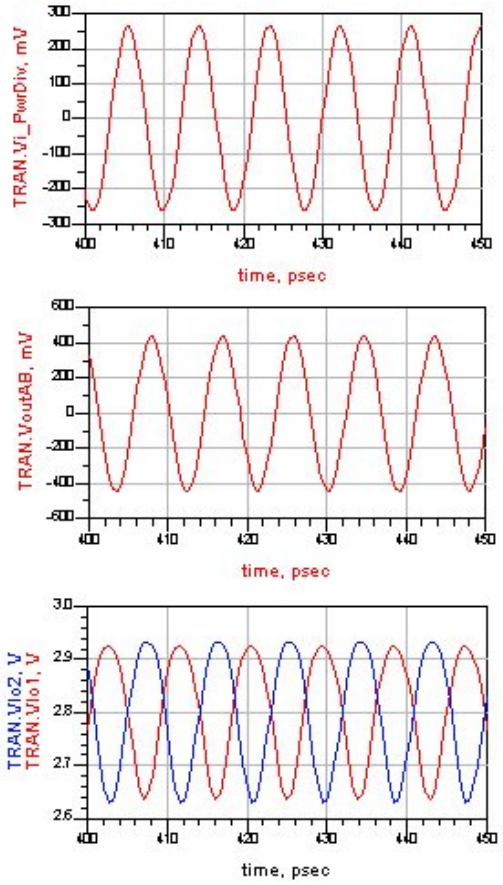

Fig 4.46 Wave forms at the input of the power divider, the antenna input and the mixer LO port at 112GHz frequency.

The whole W band blocks are designed with ADS environment. By the time of writing this thesis, they have not yet been transferred to the Cadence environment. Simulation over the entire circuit including both the Multiply by 8 Chain and the W Band Blocks has not been done. However, from the separate simulation results of these two parts. It seems that when connected together, the whole circuit will show at least 6dB in band gain variation. There is still room of improvement in terms of gain flatness.

4.7 Summary

In this chapter, the design considerations of the gain blocks operating on W band are discussed. The effect of non-ideal termination on Wilkinson power divider and ratrace hybrid is studied. Two driver amplifiers, one for driving the transmission antenna, the other for driving the LO port of the mixer, are designed. The performance of circuit blocks on W band is characterized.

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[7] U.R. Pfeiffer, A. Valdes-Garcia, "Millimeter-wave design considerations for power amplifiers in an SiGe process technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, Jan. 2006, pp.57 – 64.

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Chapter 5 Conclusion and Recommendation

5.1 Conclusion

Frequency up-conversion is an integral part of our integrated (sub)mm-wave radar project. It provides the wideband drive signal in W-band, needed for optimum operation of the phased array antenna system. This wideband signal capability offers maximum angular and distance resolution for the FMCW radar system that is currently developed within the MEMPHIS project A8. In this thesis, the key elements for signal up-conversion are investigated. A Multiply by 8 Chain and related driver amplifiers for transmission antenna, as well as, mixer LO are designed. Table 5.1 summarizes the performance of the Multiply by 8 Chain.

Table 5.1 Performance of the Multiply by 8 Chain

Multiplication factor	8
Input signal band	10GHz ~ 14GHz
Output signal band	80GHz ~ 112GHz
Nominal input signal power From a 100 Ohm differential source	About -17dBm differential
In-band output power to 50 Ohm single-end load	-3.8dBm ~ -0.4dBm
Conversion gain	13.2dB ~ 16.6dB
Unwanted spur suppression With 0.3dB input amplitude unbalance 5 degrees input phase unbalance	Better than 40dB
Power Consumption (with ideal biasing)	289mW

The antenna driver amplifier delivers 3dBm to 6dBm output power within the bandwidth from 80GHz to 112GHz. The LO driver amplifier delivers larger than 150mV peak output voltage swing and less than 2 dB gain variation within the same bandwidth. For other results please refer to related sections in chapter 4.

The major contributions of this work are:
1. A wideband frequency doubler topology giving high conversion gain is proposed.
2. Principle of signal generation on desired and undesired harmonic frequencies within a multiplier chain is investigated. Architecture of wideband multiplier chain focusing on low in-band spur is proposed. A Multiply by 8 Chain consisting 3 doublers based on this architecture is designed.
3. Large signal capability of the SiGe transistors in W-band is investigated. Wideband driver amplifiers for driving the antenna and mixer LO port are designed.

5.2 Recommendation for Future Work

This work demonstrates the feasibility of a high order millimeter wave multiplier chain. In spite of the good progress made in this study, there is still room for improvement in several aspects; such as bandwidth and noise performance. The strong correlation, however, between these performance parameters complicated the optimization process, but also provide an interesting challenge to further narrow down the optimum solution. In order to verify the design considerations involved, layout, fabrication and measurement of the proposed IC should be performed. While the multiple use of this circuit block in our phased array system calls for careful reliability and yield analysis.

In this design, filtering and optimum operation of the frequency multipliers are emphasized to improve the output spectrum purity. Although preliminary results show better nearby harmonic suppression than most published results, further improvements are still possible. As mentioned in Chapter 2, harmonic termination can be utilized to both improve conversion gain and suppress unwanted tones.

Due to the low DC-RF efficiency of active devices at higher frequencies, the power consumption of this multiplier chain is considerable. It is worthwhile to investigate ways of frequency up-conversion with lower power consumption. As is shown in Chapter 4, the output power capability of transistors at millimeter wave frequency range is limited by their low current gain, parasitics and low breakdown. Power combining can be used to increase the maximum output power of these devices, despite their inevitable high power consumption. Not only the limitations of the active devices, but also substrate loss affect the power gain and efficiency of the amplifying stages. RF-MEMS technology may help improve the situation. Micromachining to the substrate could lead to significant improvement of quality factor of on chip passive components, which is important to reduce the signal loss.

To further reduce the antenna size and improve the scale of integration, the FMCW signal should be up-converted to even higher frequencies. To reach the 300GHz frequency range, probably another frequency tripler stage should be added. As is shown in the design, the available SiGe transistor does not provide good performance at frequencies above 100GHz. Before new technology is available, this last multiplier stage can be implemented with passive devices. The use of Schottky barrier diodes for frequency multiplication above 100GHz has already been demonstrated with an enhanced version of the IBM BiCMOS8HP process [1]. The improvement in passive devices opens the door for on-chip millimeter wave applications beyond W-band.

Reference

[1] U.R. Pfeiffer, C. Mishra et al., “Schottky Barrier Diode Circuits in Silicon for Future Millimeter-Wave and Terahertz Applications”, *IEEE Transactions on Microwave Theory and Techniques,* vol. 56, no. 2, Feb. 2008 pp. 364 – 371.

Appendix A: Waveform Analysis of the Frequency Doubler

It is worth investigating the reason for the difference between the doublers driven by an ideal source and driven by a buffer amplifier as mentioned in section 2.2.2.3.

Fig A.1 plots the output current wave forms. It is clear that the output current of the buffer driven doubler shows higher negative peak and lower positive peak than the other one. This agrees with the somewhat lower 2nd harmonic output current. The higher negative peak can be attributed to higher conduction angle, while the lower positive peak could be caused by lower positive base-emitter drive.

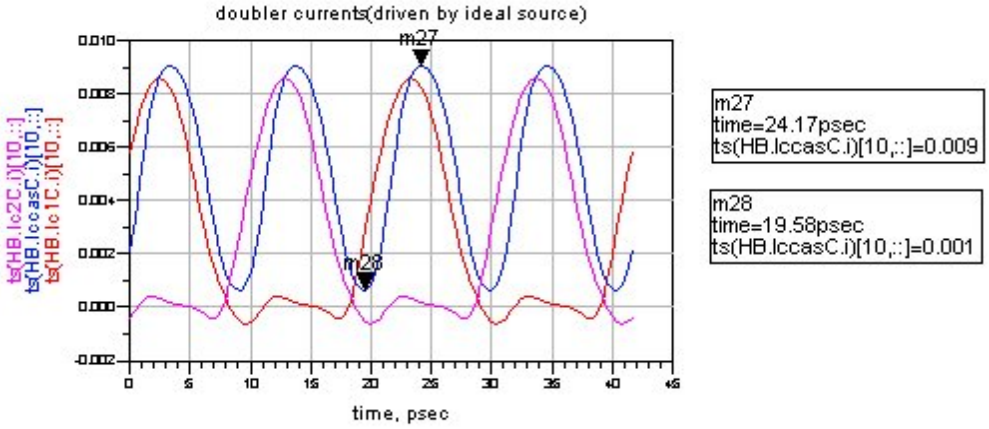

Fig A.1 (a) doubler currents during a power sweep with an ideal power source

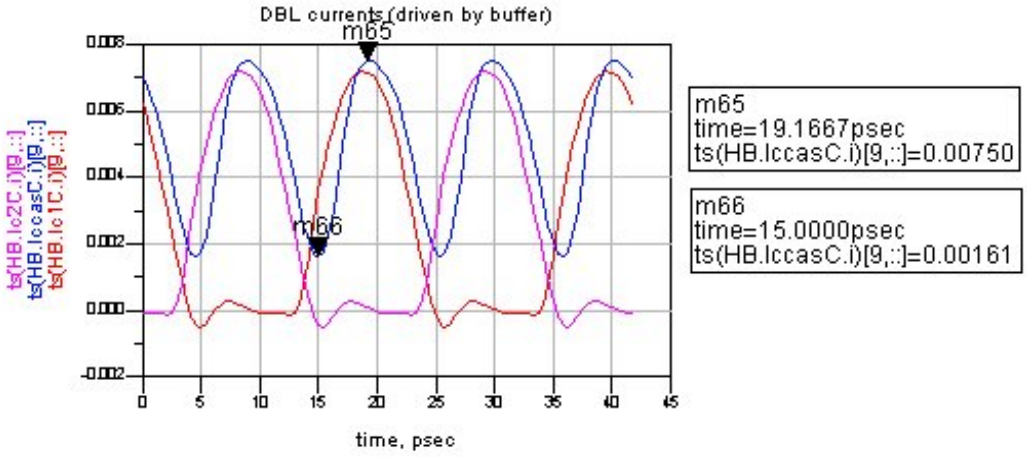

Fig A.1 (b) doubler currents during a power sweep with a buffer amplifier

The voltage waveforms at the input of the doublers are compared. In Fig A.2 (a) and (b), the upper plots show the waveform of base voltage of the input transistor of the doubler, V_b, the lower plots show the waveform of base-emitter voltage of that transistor, V_{be}. The input power of the ideal source is limited to -4dBm, which gives the largest voltage swing to be about 0.4V, close to the maximum swing the buffer can offer. We can observe obvious difference on the base voltage waveform. The ideal source has a single-tone excitation, so even with the presence of the nonlinear input loop of the doubler, V_b still approximates a sine wave. We may see that all these waveforms cross the same mid point close to the DC bias of 2V. As of the doubler driven by the buffer, it seems that V_b waveform changes much more as input power increases. It seems that for the buffer driven doubler the positive peak becomes sharper while the negative peak becomes blunter, which indicates the presence of considerable higher harmonic content. The difference in the V_b waveform should be the reason to the difference in output current.

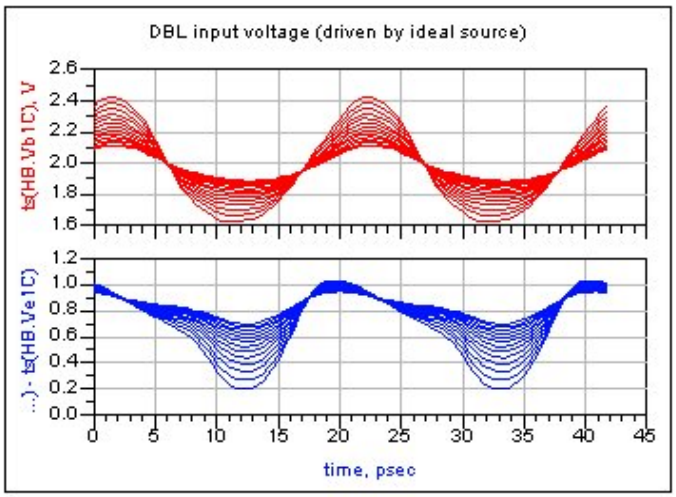

Fig A.2 (a) doubler input voltage during a power sweep with ideal source

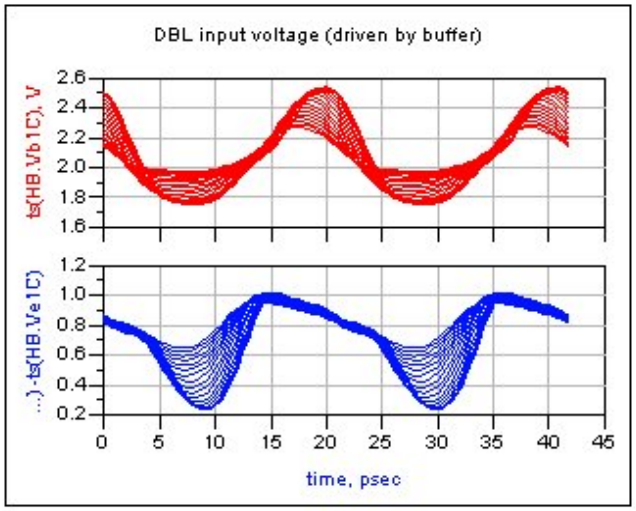

Fig A.2 (b) doubler input voltage during a power sweep with buffer amplifier

Further examining the harmonic components of V_b confirms the difference in V_b waveform. As shown in Fig A.3(a) and (b), there are stronger harmonic contents in V_b of the buffer driven doubler. If we look at the fundamental and 2nd harmonic difference, we see the one driven by the buffer shows about 5dB higher 2nd harmonic term. The difference comes from the buffer amplifier. The large signal drive of the doubler, the strong nonlinear input capacitance of the differential pair in doubler, as well as the source impedance together give rise to pretty high amount of harmonics even when the doubler is driven by a signal tone source. When a buffer is inserted in between, it also generates harmonics due to its own nonlinearity. Although the buffer is designed to avoid strong nonlinearity such as clipping, it still generates harmonics from weak nonlinear sources. Still, as a trade off with other aspects such as frequency response, the linearity of the buffer in some stages are compromised a bit.

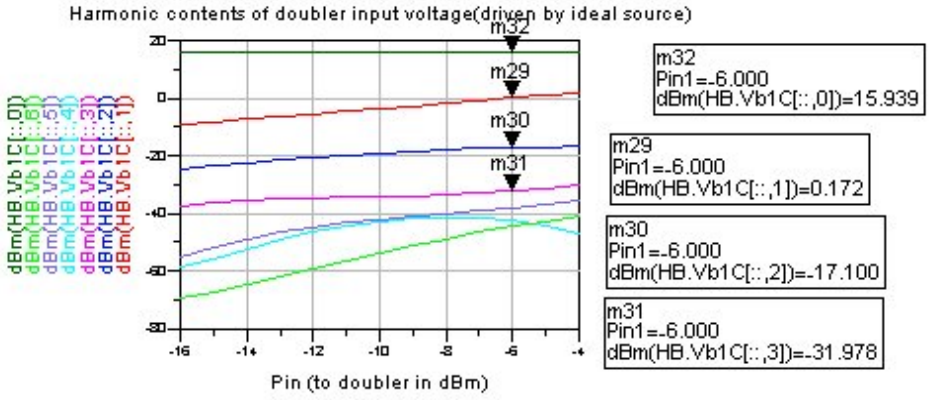

Fig A.3 (a) Harmonics in doubler input voltage during a power sweep with ideal source

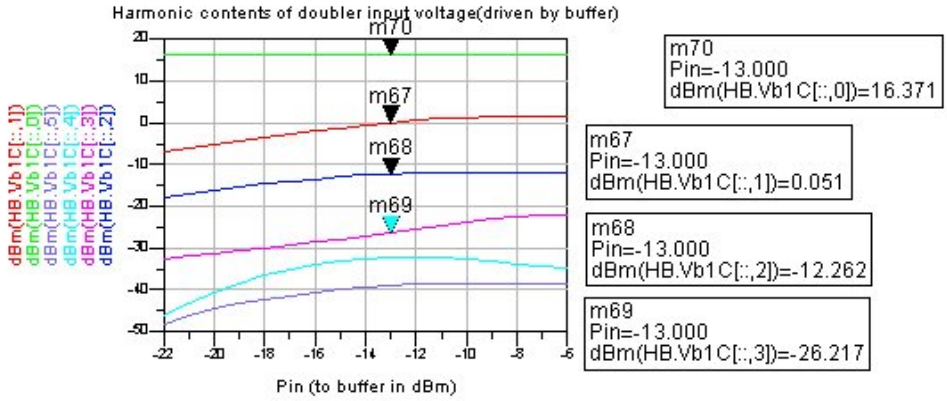

Fig A.3 (b) Harmonics in doubler input voltage during a power sweep with buffer amplifier

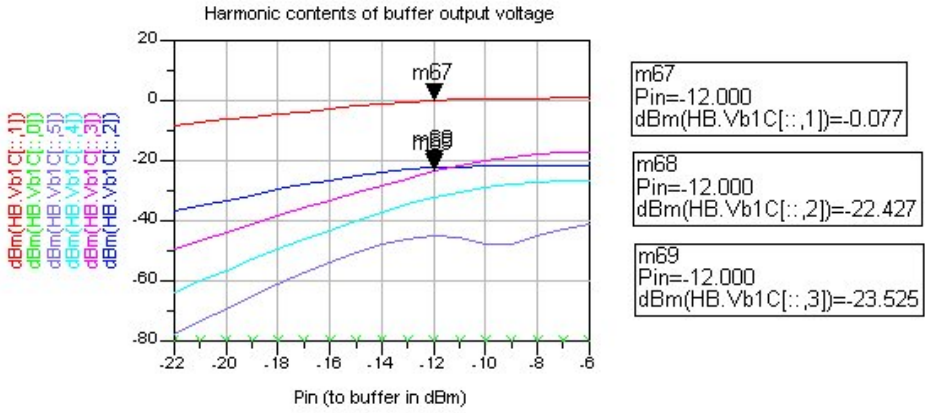

Fig A.4 Harmonic in buffer output voltage during a power sweep with RC load

Fig A.4 shows the output voltage harmonic contents of the buffer used above. It is loaded by impedance representing the input impedance of the doubler. The 2nd and 3rd order harmonics are more than 20 dB lower. The finding here is that about 10% of higher harmonics (at 2fo and/or 3fo) fed to the doubler would affect the output harmonics quite significantly. The 2nd harmonic output current dropped over 3 dB while the ratio of 4th harmonic to 2nd harmonic output increased over 5dB. It is safe to say that the doubler is sensitive to the harmonics from the source. In fact, in this sense, single-tone excitation becomes multi-tone excitation, so that mixing products from all the input tones will appear in the output.

Appendix B: Unbalanced Drive Condition of the Frequency Doubler

Differential Mode and Common Mode Drive

Referring to section 2.2.2.4, balanced drive of a frequency doubler means the drive signal to its two inputs are a pair of fully differential signal tone signal. For ease of comparison, we again plot the waveform and spectrum of a doubler under balanced drive, here we also name it differential mode drive.

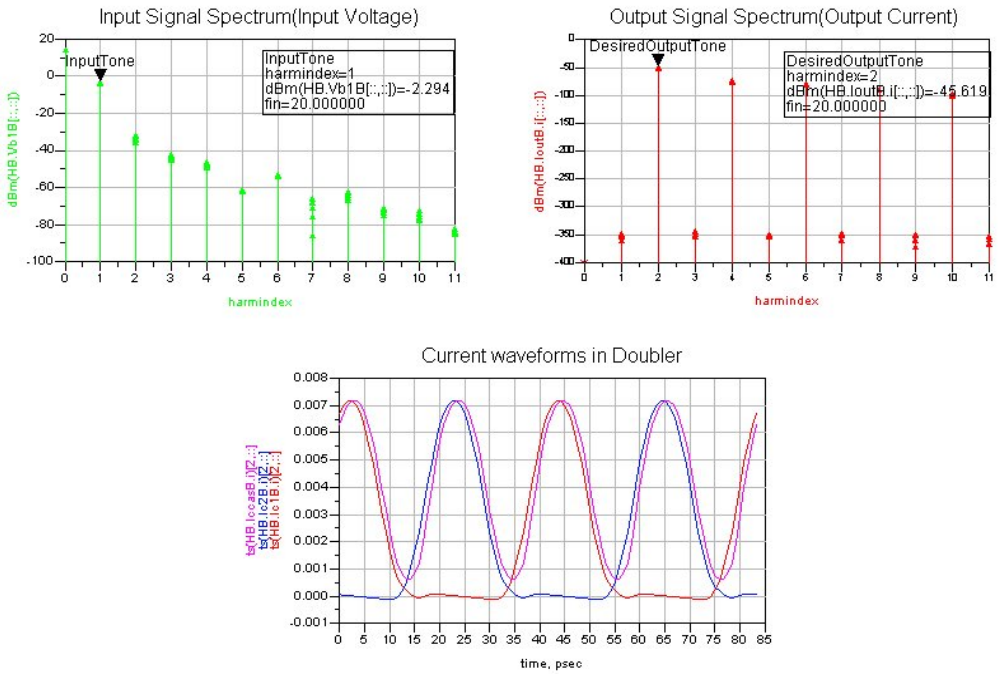

Fig B.1 Doubler input voltage and output current under differential mode drive, also called balanced drive

Fig B.2 shows the situation where the phase of one of the power sources is reversed, amplitude and source impedance are kept unchanged. In this case, the signals on both inputs of the doubler are identical, so the doubler is under CM (common mode)drive. The collector current from the two input transistors are now combined in phase and form a narrow current pulse train. This waveform contains rich harmonic components, both even and odd order ones. In fact, looking at the numbers denoting the harmonic strength, the even harmonics generated by CM drive show comparable value to those generated from DM drive. The odd order harmonics are no weaker than the nearby even order harmonics. In other words, the doubler shows similar strength of even order nonlinearity and much stronger odd order nonlinearity under CM drive than DM drive.

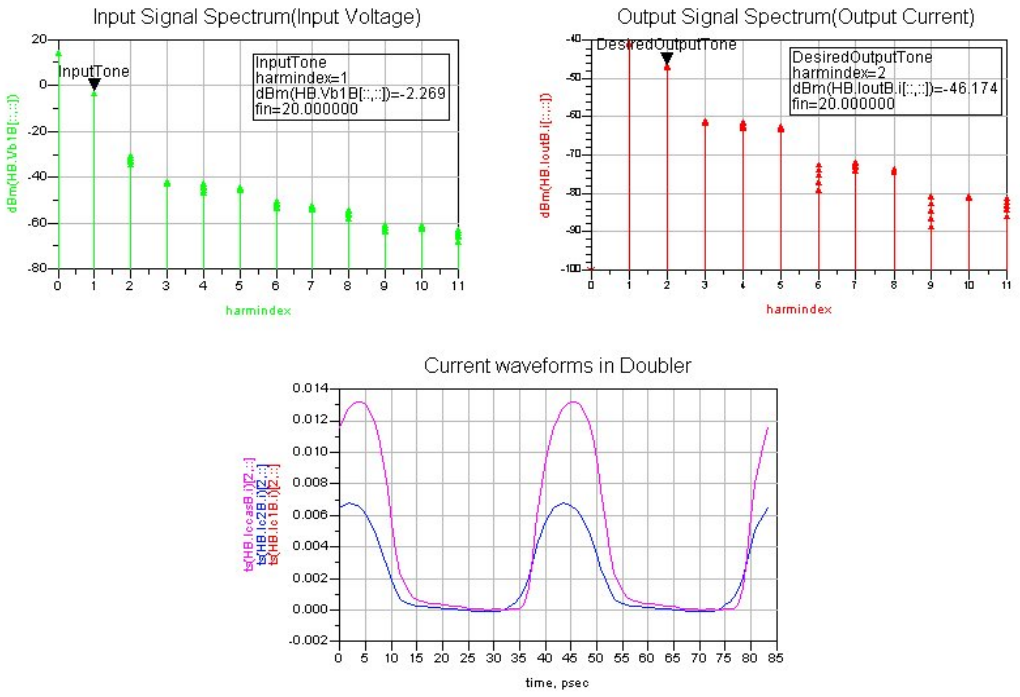

Fig B.2 Doubler input voltage and output current under common mode drive

In reality, despite the effort in layout and circuit design, mismatch always causes some unbalance between a pair of nominally differential input signals. Two different signals can be decomposed to even-order and odd-order components as described in the following equations

$$V_{cm} = \frac{1}{2}(V_1 + V_2)$$

$$V_{dm} = \frac{1}{2}(V_1 - V_2)$$

$$V_1 = V_{cm} + V_{dm}$$

$$V_2 = V_{cm} - V_{dm}$$

where V_1 and V_2 are the two nominally differential signals, V_{cm} denotes common mode signal, V_{dm} denotes differential mode signal.

For fully differential signals, as the case of balanced drive, V_1 and V_2 have equal amplitude and opposite phase, so their sum, V_{cm}, equals to a DC value at any moment. If the two signals show any unbalance, V_{cm} then has a time varying part. So on top of a large differential mode input, the circuit is also excited with a common mode input. As we shall see from the next simulations, even though this common mode part may be much weaker in terms of power, it affects the operation of a doubler a lot.

Amplitude and Phase Difference

A sinusoidal can be fully described with its amplitude, phase and frequency. The unbalance between nominal differential signals can also be described by these parameters. We can control these variables and examine their respective influence on doubler operation one by one. Fig B.3 shows the case where the drive signals have 1dB amplitude difference. Current waveforms show that the peak value of two collector currents are different, which makes peak value of the output current change in each cycle. This alternation gives rise to odd order harmonics in the output wave form. The reason is that one of the input transistors is driven by larger signal than the other. The transistors can no longer short circuit each other on odd order harmonics so that some odd order term leaks to the out.

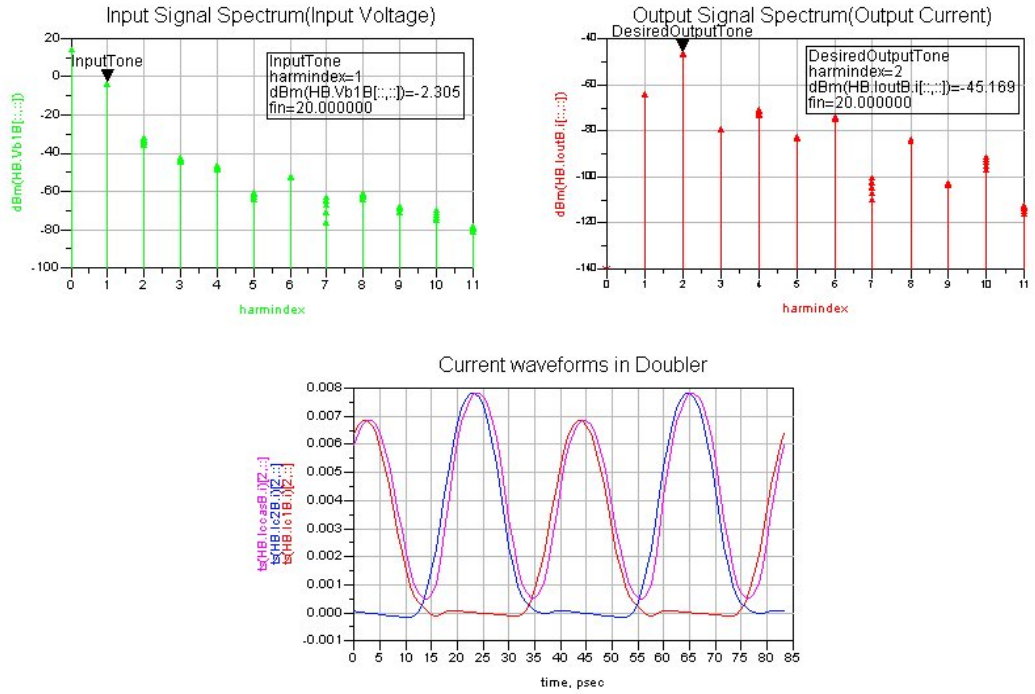

Fig B.3 Doubler input voltage and output current with unbalanced drive of 1dB amplitude difference

Fig B.4 shows the case where the drive signals have 10 degrees of additional phase difference from the nominal 180 degree relation. The bottom of the output current waveform varies in each excitation cycle. The effect in the frequency domain is similar to the above situation with amplitude unbalance. When the two drive signals have equal amplitude and opposite polarity or 180 degree phase difference, the current amplitudes at the cross points of the two current pulses are the same because of symmetry. When phase difference other than 180 degree exists between the two pulse trains, the cross point moves and the associated negative peak of the output current varies from one peak to another.

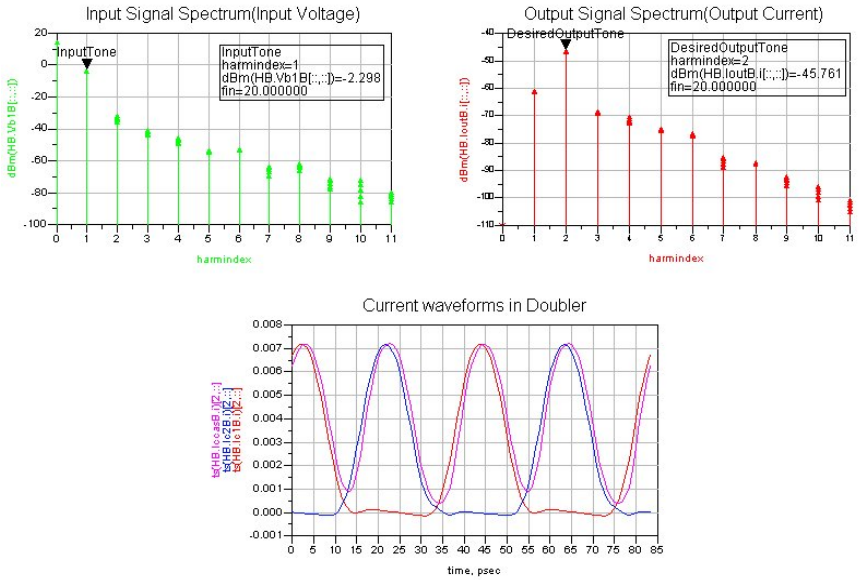

Fig B.4 Doubler input voltage and output current with unbalanced drive of 10 degree phase difference

The above two experiments show the importance of keeping the drive signal to a doubler stage balanced for reducing odd order nonlinearity.

Harmonic at the Input

In the third experiment, the original drive signal is kept balanced. In addition, a second balanced signal at double frequency whose power is 40dB lower than the 1st one is applied. In this two-tone excitation situation, the alternation of wave form is more subtle, but considerable nearby odd order harmonics appear in the output, mainly 1st and the 3rd harmonic. Comparing the base voltage of this case to the one with ideal balanced drive as shown in Fig B.5, the 2nd tone has changed the input voltage harmonic contents by only a few dB. The finding is that it only takes a little bit harmonic term in the input to rattle the ideal odd order harmonic cancellation in the output current.

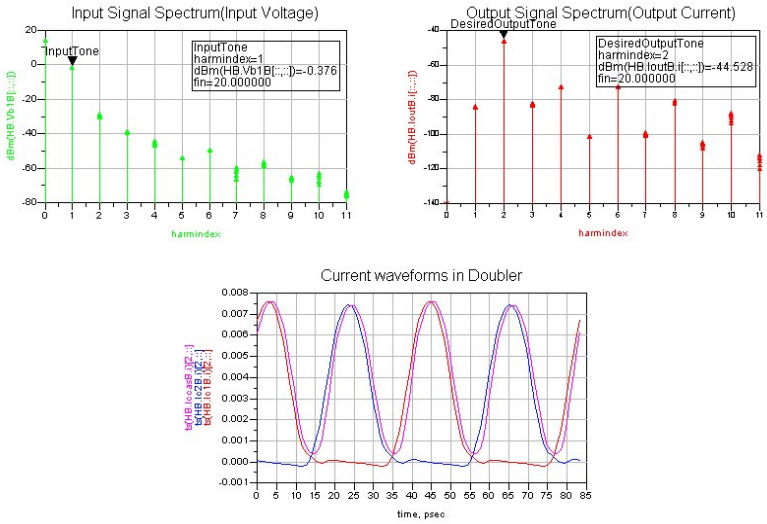

Fig B.5 Doubler input voltage and output current with 2 tone excitation

Appendix C: Simulation Results of Two Active Baluns

1. Input Stage of Micromixer

The first balun structure is based on part of the so called “micromixer” topology by Gilbert. It is widely used for single balanced mixer since its invention. Fig C.1 shows the topology with bias circuit.

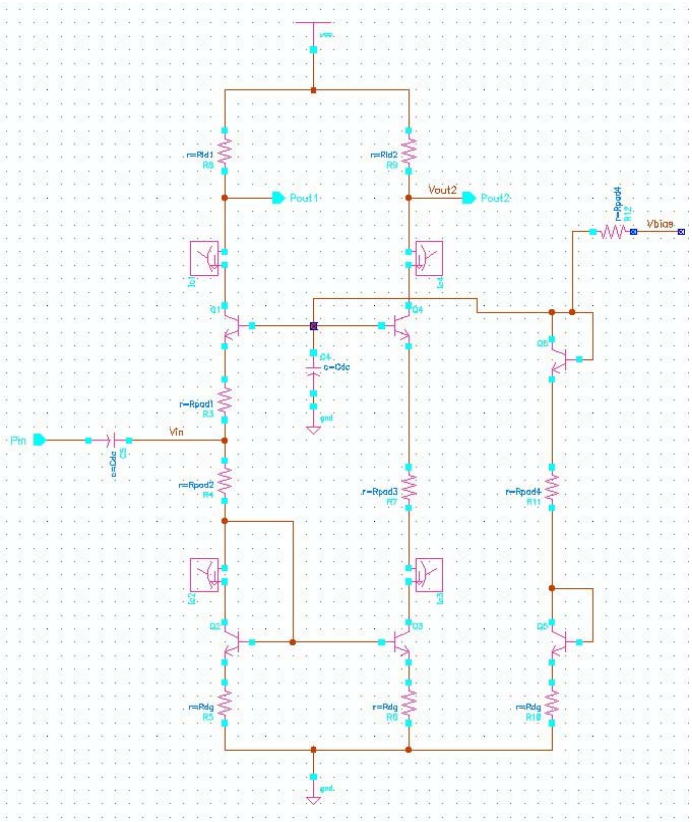

Fig C.1 Topolgy of a balun based on micromixer

The inverting signal path consists of a current mirror with transistors Q2, Q3 and Q4, while the noninverting path is made up of a common base stage. The two pad resistances at the input modify the input impedance. Their value affects how the input power is divided into two signal paths, which can be used to compensate for the amplitude unbalance between the two outputs. One of the most notable merit of this topology is its improved linearity over a wide input power range due to the combination of a common base stage and a current mirror. The lowered input impedance makes this topology ideal for current sensing. But in terms of voltage, signal gain is lowered, although the reduced input swing helps to improve linearity. Padding resistance further reduces voltage gain, so this topology does require higher input power for the same amount of output than some other structures. To avoid breakdown due to high collector emitter voltage with low break down device, another cascode is added on top of the mirror branch. However this proves to be a problem. Fig C.2 shows the phase relation of the collector currents of each transistor in RF path. The additional phase lag along the inverting path, consisting transistors Q2, Q3 and Q4, can be observed. The common emitter Q3 and the cascode Q4 each add 20 and 11 degrees to the phase shift. This problem can not

be corrected through tuning pad resistance. Different numbers of transistors in the two signal paths worsen the problem of phase shift. The phase relation also show an approximately linear relation with frequency, which leads us to attribute the problem to capacitive parasitic within the transistors. The amplitude and phase difference between the two output currents are shown in Fig C.3. We can see that although amplitude unbalance is corrected with padding, the phase difference is still pretty large. It reaches about 45 degrees around 50 GHz. Fig C.4 show the input and output voltages during a freuqncy sweep. Clear role off in the output voltage vs. frequency sweep is displayed.

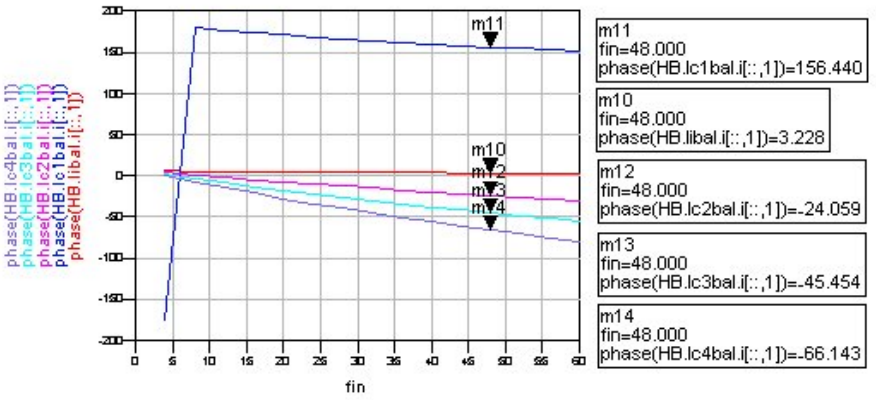

Fig C.2 Phase relation of current in a micromixer balun vs. frequency sweep

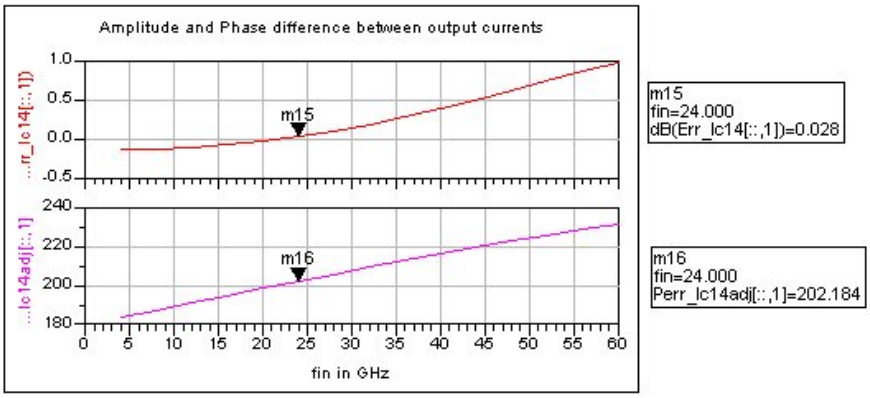

Fig C.3 unbalance between two output currents in a micromixer balun vs. frequency sweep

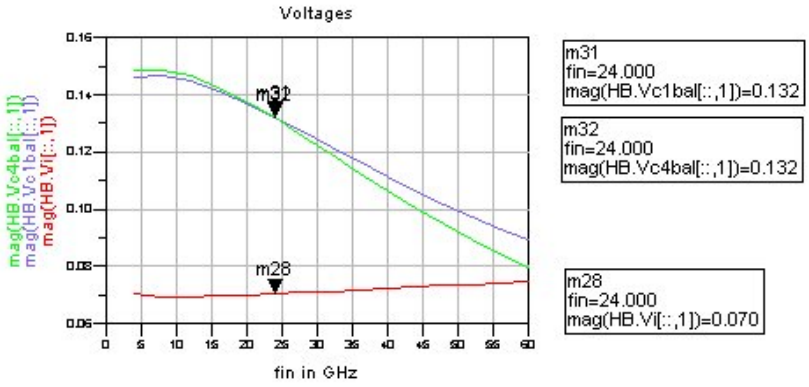

Fig C.4 Voltages in a micromixer balun vs. frequency sweep

2. Balun with inverting path split

Another variant of a differential pair is depicted in Fig C.5. The inverting path of the differential pair is been split into two branches, the one with transistor Q0 generates the inverting output signal; the one with Q6 does not contribute to the output signal. The idea is that the split path with Q6 diverts away part of the DC current through the inverting path. So the bias current through the non-inverting path including transistor Q1 is higher than that of the inverting path. But this alone is not sufficient to balance the two output signals, the base of Q6 is also connected to the base of Q0 to divert away part of the input signal. The amplitude balance is optimized by adjusting the size of Q6 and Q0 with respect to Q1.

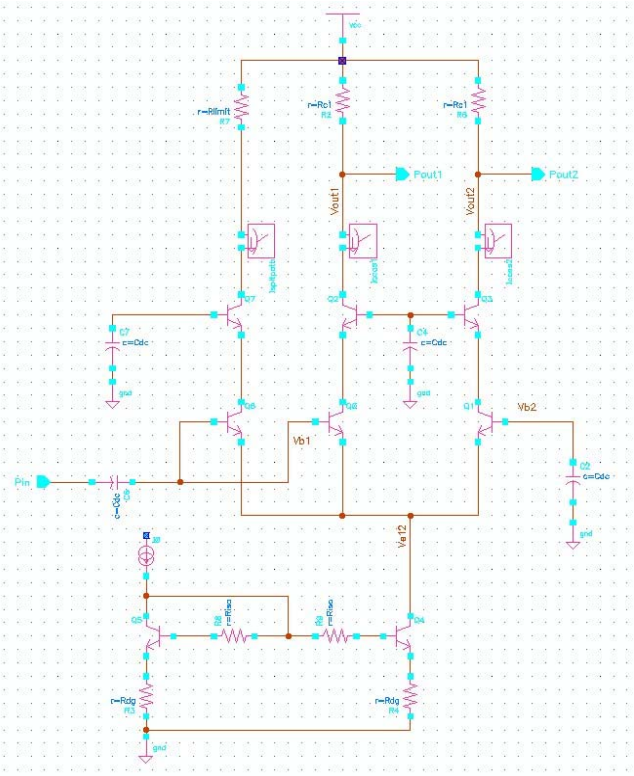

Fig C.5 Topology of balun with inverting path split

After optimization, the total emitter length of Q6 and Q0 exceeds that of Q1, resulting in increased input capacitance. Besides, the transistors have to be scaled up a little to keep linearity. With the constraint of same input power, this structure results in a bit more drop in voltage gain frequency response. Typical input output voltage relation is shown in Fig C.6.

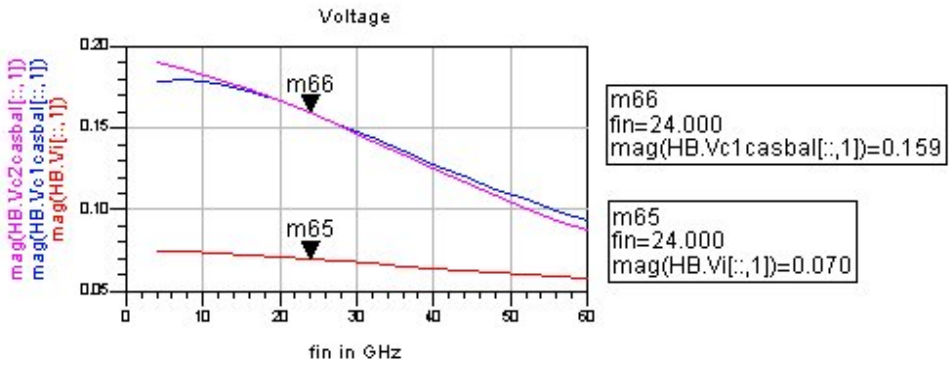

Fig C.6 Typical input and output voltage relation of an inverting path split balun vs. frequency sweep

This balun does not depend on any absolute value of resistor to improve balance. But it relies on the size of transistors. It is the mismatch between these nearby transistors that may break the balance. Data sheet states that Vbe mismatch of NPN with the size of 0.12u*0.75u*1 is about 35mV with peak ft bias current. DC voltage sources in series with the emitters are inserted in the schematic to get some idea about the influence of nearby transistor mismatch. Fig C.7 shows the result of a simulation in which the voltage source representing mismatch is in series with the emitter of Q6.

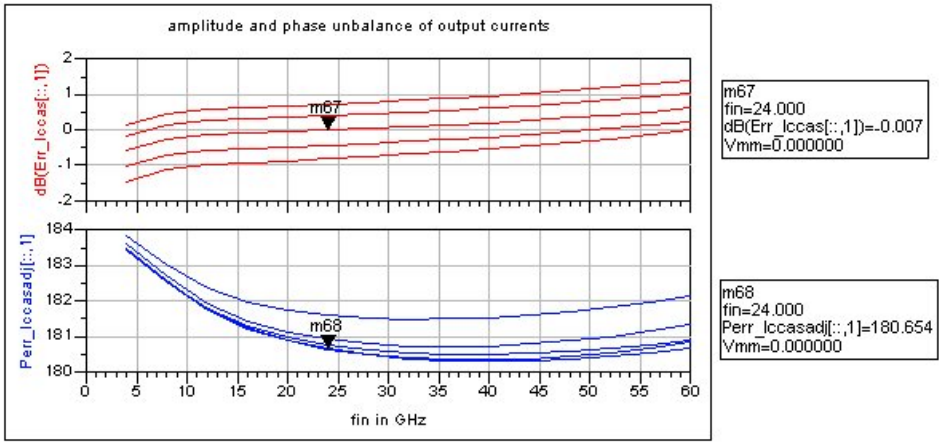

Fig C.7 variation of output unbalance from inverting path split balun with +-50mV of Vbe mismatch in one branch

In Fig C.8, Input power sweep shows comparable tolerance as the balun with RC feed forward compensation. However, compared with the other one, the balances obtained by this inverting path split balun is more subtle. The two transistors connected as a differential pair are in different sizes, they are biased with different currents, their transconductances are different and the signal voltages on their base emitter junctions are different. However, the specific combination of sizes makes the output signal about balanced. So many unequal quantities involved make the balance especially delicate. Besides, different output impedances cause addition unbalance when the balun is loaded with the next stage. For these reasons, the balun with an RC feed forward path is chosen to be used in the multiplier chain.

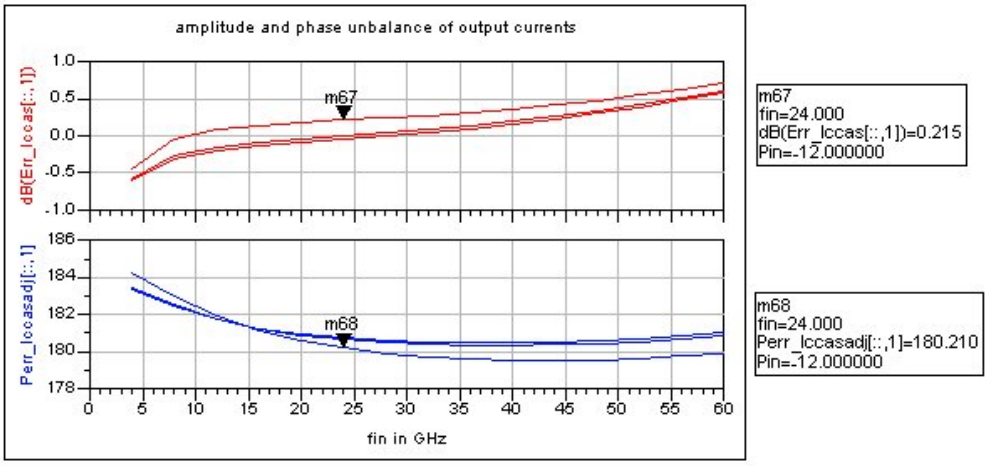

Fig C.8 variation of output unbalance from inverting path split balun with +-dB input power variation

Frequency response of the above two Baluns show clear roll off with frequency. To avoid using bulky matching network in many places, this role off is compensated by peaking in other circuit blocks