A 0.01 mm^{2}10MHz RC Frequency Reference with a 1-Point On-Chip-Trimmed Inaccuracy of ±0.28% from -45°C to 125°C in 0.18µm CMOS

An, Xiaomeng; Pan, Sining; Jiang, Hui; Makinwa, Kofi A.A.

DOI
10.1109/ISSCC42615.2023.10067530

Publication date
2023

Document Version
Final published version

Published in
2023 IEEE International Solid-State Circuits Conference, ISSCC 2023

3.4 A 0.01mm² 10MHz RC Frequency Reference with a 1-Point On-Chip-Trimmed Inaccuracy of ±0.28% from -45°C to 125°C in 0.18µm CMOS

Xiaomeng An*[1,2], Sining Pan*[1,3], Hui Jiang[2], Kofi A. A. Makinwa[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Silicon Integrated, Eindhoven, The Netherlands, [3]Tsinghua University, Beijing, China
*Equally-Credited Authors (ECAs)

CMOS frequency references based on RC oscillators are usually preferred over bulky crystals in IoT applications [1-5]. However, due to the process spread and finite temperature coefficient (TC) of most on-chip resistors, RC oscillators require trimming and temperature compensation to achieve decent accuracy. Enabled by high-resolution trimming techniques such as ΔΣ [1,2] or pulse-density [3] modulation, recent designs can obtain good accuracy (<0.1%) at the expense of large chip area. However, existing compact (<0.02mm²) designs suffer from frequency errors in the order of 1% or more [4,5]. Moreover, their temperature compensation schemes usually require the use of resistors with complementary TCs, which are not available in all CMOS technologies.

This paper describes a compact RC frequency reference with on-chip circuits with which both its TC and absolute frequency f_0 can be trimmed. Fabricated in a standard 0.18µm technology, the 0.01mm² 10MHz reference achieves a ±0.28% inaccuracy from –45°C to 125°C after 1-point trim, which represents the state-of-the-art for designs with a similar area. Moreover, the proposed temperature compensation scheme does not require resistors with complementary TCs, which significantly extends its application scope.

Figure 3.4.1 (top-left) shows the block diagram of the proposed RC-based frequency reference, which is based on a frequency-locked-loop (FLL) [3]. Driven by the output frequency F_{OUT} of a voltage-controlled oscillator (VCO), an RC network outputs a frequency-dependent voltage (V_C), which is compared with a reference voltage (V_R) derived from a resistive divider, integrated and then used to drive the VCO. Due to the large DC loop gain, the steady-state difference between V_R and V_C will be near zero, resulting in an output frequency that only depends on the properties of the RC network and the resistive divider.

On-chip resistors typically have large TCs, up to 1000ppm/°C, while that of on-chip MIM caps (~30ppm/°C) is relatively negligible. As a result, the TC compensation of RC oscillators is often achieved by combining resistors with complementary TCs to realize a so-called "zero-TC" composite resistor R_0, which ensures that V_C is temperature independent [3]. However, this requires a high-resolution resistor-trimming network, which introduces (trim-code dependent) parasitic capacitances that increase the inaccuracy of f_0. Furthermore, not all CMOS technologies have a suitable combination of resistors.

In this work, R_0 is realized as a single resistor, and TC compensation is achieved by designing the TC of the reference voltage V_R to match that of V_C. In the chosen 0.18µm CMOS technology, both R_0 and R_1 are implemented as p-poly resistors (-0.02%/°C), while R_2 is implemented by a trimmable combination of p-poly and n-poly (-0.15%/°C) resistors. As shown in Fig. 3.4.1 (bottom-left), by tuning the width of the two types of resistors so that they (nominally) have the same resistance per unit length, the length of R_2, and thus its resistance, will be trim-code independent, allowing f_0 to be trimmed in an orthogonal manner. In this work, the TC of the frequency reference can be trimmed from -40ppm/°C to 40ppm/°C in 16 steps. As shown in Fig. 3.4.1 (bottom-right), the nominal frequency f_0 is trimmed with the help of a coarse-fine capacitive DAC. This results in a trimming range of ±30%, with a worst-case trimming resolution of 0.1%, or equivalently 1fF, with a practically realizable 10fF DAC LSB.

In [3], a frequency-dependent voltage V_C is created by a resistive divider that consists of a fixed resistor and a switched-capacitor resistor. However, the periodic ripple in V_C must be limited by a relatively large stabilizing capacitor. In this work, the need for the latter is obviated by generating V_C in three phases, as shown in Fig. 3.4.2 [6]. During the reset phase, ϕ_{RST}, capacitor C_0 is pre-charged to V_{DD}, and during the subsequent discharging phase, ϕ_{DCHG} it is discharged through resistor R_0. At steady-state, the duration of this phase is equal to one period T_{VCO} of the VCO's output frequency, which can be expressed as $T_{VCO}=R_0C_0\ln(1+R_1/R_2)\approx 0.7R_0C_0$ and is, ideally, supply-independent. During the third integration phase ϕ_{INT}, a G_M-C integrator (G_M=5µS, C_{INT}=7pF) integrates the sampled difference between V_R and V_C, which is then used to drive the VCO. To facilitate the generation of the 3-phase control signals, the VCO runs at 40MHz, which is 4× higher than the targeted output frequency (10MHz). This also reduces the required RC constant (R_0=36kΩ and C_0=1pF) by 4×, and thus the chip area. To improve the FFL's energy efficiency, ϕ_{INT} is 2× longer than ϕ_{RST} or ϕ_{DCHG}. The state of the FLL is thus updated at $F_{VCO}/4$. Setting R_1=R_2=100kΩ results in an even power split between the RC and resistive-divider branches.

To suppress its 1/*f* noise and improve the oscillator's long-term stability, the G_M stage is chopped. However, the up-modulated offset will then cause ripples at the control input of the VCO (V_{CTRL}), and thus increase its output jitter. Conventionally, this problem is solved by increasing the chopping frequency or lowering the G_M/C_{INT} ratio [3]. However, the former leads to a larger residual offset and thus worse inaccuracy over PVT, while the latter results in a trade-off between capacitor area and jitter performance. In this design, the size of C_{INT} is drastically reduced by using a compact switched-capacitor notch filter to suppress the ripple [7]. The filter consists of two capacitors C_{MID} (=1.8pF) and C_{HOLD} (=2.7pF) and two switches driven by the sample (ϕ_S) and hold (ϕ_H) signals. As shown in Fig. 3.4.2 (bottom), the voltage across C_{INT} is effectively sampled once every chopping period, resulting in a ripple-free V_{CTRL} at a chopping frequency of $F_{VCO}/8$ (=1.25MHz). Compared to the two-phase filter used in [7], the use of a single-phase filter results in less ripple due to the absence of mismatched charge injection errors, at the expense of 2× more delay. However, the resulting delay is still quite small compared to that of the integrator, and so has a negligible effect on loop stability. The VCO consists of a PMOS current source that drives a 3-stage current-starved ring oscillator, while the G_M stage is a chopped telescopic amplifier with an 80dB DC gain.

The prototype RC frequency reference was fabricated in a standard 0.18µm CMOS technology, as shown in Fig. 3.4.7. To save area, all the resistors and transistors are placed below the Metal-Insulator-Metal (MIM) capacitors, resulting in a compact 100µm×100µm layout. Each frequency reference draws 56.7µA (27.5µA analog and 29.2µA digital) from a 1.5V supply. About 2/3 of the digital power is used to drive the output buffer. Over a 1.5V to 1.8V range, the frequency reference has a supply sensitivity of 2700ppm.

Seven ceramic-packaged chips (112 samples) from one wafer were trimmed and then characterized in a temperature-controlled oven. Since the intra-batch TC spread turned out to be quite small (±8ppm/°C), a fixed TC trim code (corresponding to the simulated TT corner) was used for all samples. As expected, the spread in f_0 is much larger (±1.9%) and was individually trimmed at room temperature (RT, ~25°C).

As shown in Fig. 3.4.3, the frequency reference achieves an inaccuracy of ±0.28% over the automotive temperature range from –45°C to 125°C, resulting in a residual TC of 31.5ppm/°C (box method). However, significant hysteresis (1500ppm worst-case) is observed as the samples are cycled from hot to cold, mainly due to the instability of the polysilicon resistors. Each sample was cycled twice, resulting in a cycle-to-cycle variation of less than ±200ppm, which is much smaller than the observed hysteresis.

Since polysilicon resistors are also known to suffer from drift [8], accelerated aging experiments were conducted by baking the measured samples at 150°C for one week. As shown in Fig. 3.4.4 (top), both the nominal frequency (0.5%) and its TC (10ppm/°C) suffer from drift. However, the former can be trimmed at room temperature with the help of an external reference [9], while the latter is 3× smaller than the original residual TC, and results in much less (0.17%) additional frequency error over life-time. To characterize the effect of packaging stress, seven plastic-packaged chips were also measured. Compared to the ceramic-packaged chips, they required a different TC trim code to achieve similar inaccuracy: ±0.3% from –45°C to 125°C. However, they exhibited somewhat less hysteresis (1200ppm worst-case) as they were cycled from hot to cold.

Figure 3.4.4 (bottom) shows the start-up behaviour of the frequency reference. After setting V_{CTRL} to ground, the output frequency settles within 30µs. Enabling chopping and notch filtering results in a step-wise settling transient, but does not change the settling time. The frequency reference achieves an output period jitter of 41.4ps$_{rms}$ (Fig. 3.4.5, top) and an Allan deviation of 2.3ppm for a 0.6s-stride (Fig. 3.4.5, bottom). Figure 3.4.6 summarizes the performance of the RC-based frequency reference and compares it to the state-of-the-art. Despite the use of a relatively mature 0.18µm technology, it achieves the best on-chip trimmed inaccuracy among compact (<0.02mm²) CMOS frequency references, making it a competitive timing solution for low-cost IoT applications.

References:

[1] Ç. Gürleyük et al., "A 16 MHz CMOS RC Frequency Reference with ±90 ppm Inaccuracy From -45 °C to 85 °C," *IEEE JSSC*, vol. 57, no. 8, pp. 2429-2437, Aug. 2022.
[2] W. Choi et al., "A 0.9-V 28-MHz Highly Digital CMOS Dual-RC Frequency Reference with ±200 ppm Inaccuracy from -40 °C to 85 °C," *IEEE JSSC*, vol. 57, no. 8, pp. 2418-2428, Aug. 2022.
[3] A. Khashaba et al., "A 32-MHz, 34µW Temperature-Compensated RC Oscillator Using Pulse Density Modulated Resistors," *IEEE JSSC*, vol. 57, no. 5, pp. 1470-1479, May 2022.
[4] J. Wang et al., "A 12.77-MHz 31 ppm/°C On-Chip RC Relaxation Oscillator with Digital Compensation Technique," *IEEE TCAS-I*, vol. 63, no. 11, pp. 1816-1824, Nov. 2016.
[5] J. Lee et al., "An Ultra-Low-Noise Swing-Boosted Differential Relaxation Oscillator in 0.18-µm CMOS," *IEEE JSSC*, vol. 55, no. 9, pp. 2489-2497, Sept. 2020.
[6] A. Khashaba et al., "A 0.0088mm² Resistor-Based Temperature Sensor Achieving 92fJ·K² FoM in 65nm CMOS," *ISSCC*, pp. 60-61, Feb. 2020.

2023 IEEE International Solid-State Circuits Conference (ISSCC) | 978-1-6654-9016-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/ISSCC42615.2023.10067530

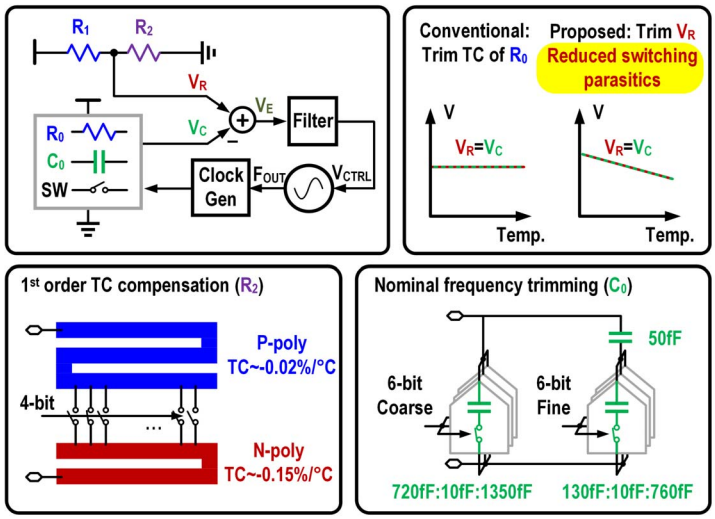

Figure 3.4.1: Block diagram and temperature compensation of an RC frequency reference (top), TC and frequency trimming (bottom).

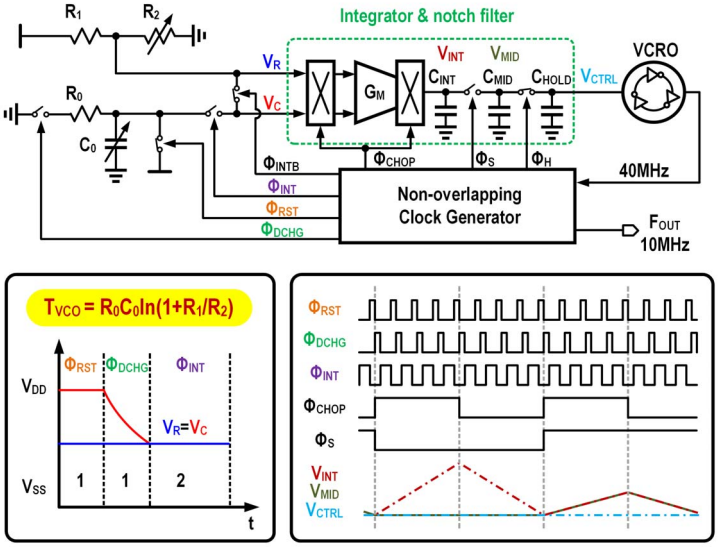

Figure 3.4.2: System block diagram (top) and timing diagram (bottom).

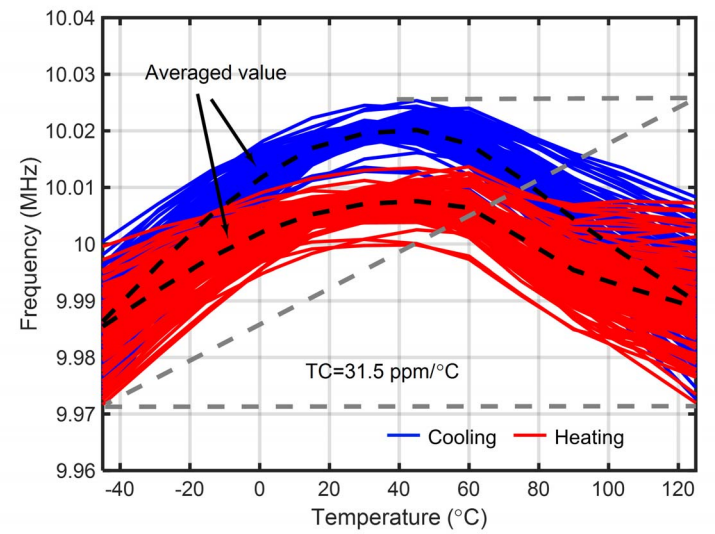

Figure 3.4.3: Temperature sensitivity and hysteresis of the frequency reference (112 samples).

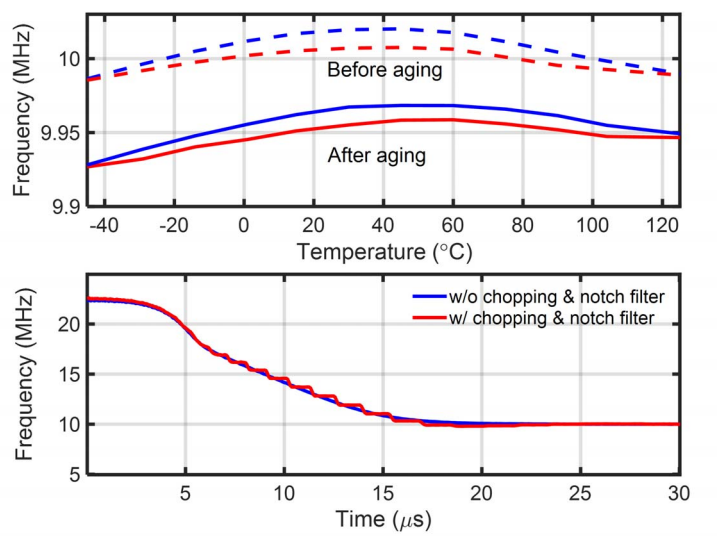

Figure 3.4.4: Averaged frequency of 112 samples before and after aging (top) and Transient response after VCTRL reset (bottom).

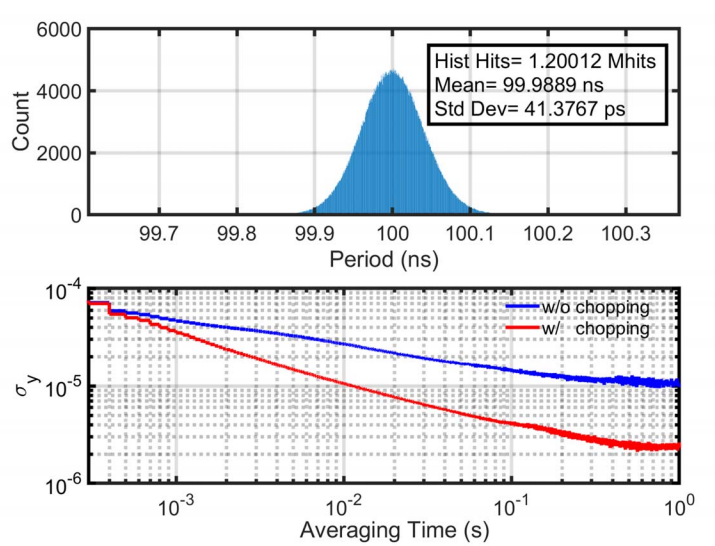

Figure 3.4.5: Measured period jitter (top) and Allan deviation (bottom).

Reference	This work	JSSC 2022 [1]	JSSC 2022 [2]	JSSC 2022 [3]	TCAS-I 2016 [4]	JSSC 2020 [5]
Technology	0.18μm	0.18μm	65nm	65nm	0.18μm	0.18μm
Area [mm²]	0.01	0.3	0.06	0.18	0.012	0.015
Frequency [Hz]	10M	16M	28M	32M	12.77M	10.5M
Power [μW]	85 [a]	220	142	34	56.2	219.8
Energy [pJ/cycle]	8.5 [a]	13.8	5	1.1	4.4	21
Temp. range [°C]	-45~125	−45~85	−40~85	−40~85	−30~120	-45~125
Max. Freq. error [ppm]	±2800	±90	±200	±400	±9000 [b]	-
Temp. coefficient [ppm/°C]	31.5 [c]	1.3 [c]	2.56 [c]	8.4	31	137
Supply range [V]	1.5~1.8	1.6~2	0.85-1.05	1.1~2.3	0.6~1.1	1.4~2.2
Supply sensitivity [ppm/V]	9000	1200	2900	80 [d]	10000	44000
Jitter [ppm]	414	638	196	713	983	104
Allan deviation [ppm]	2.3	0.32	2	2.5	-	2.8
Trimming points	1+batch (1st order)	2+batch (3rd order)	2+batch (5th order)	2	1	0
Number of samples	112	20	16	6	4	15

[a] Including driver [b] Estimated from inaccuracy plots [c] Box method [d] LDO used

Figure 3.4.6: Performance summary and comparison with previous RC frequency references.

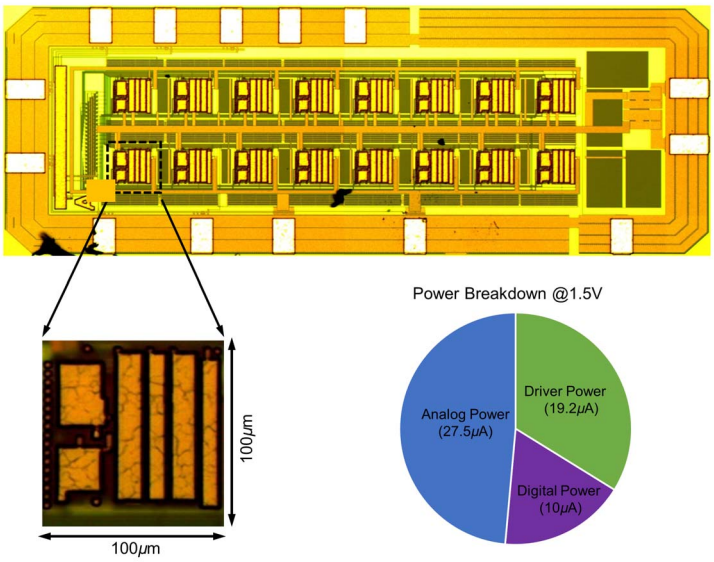

Figure 3.4.7: Die micrograph and its power breakdown.

Additional References:

[7] P. Park et al., "A Thermistor-Based Temperature Sensor for a Real-Time Clock with ± 2 ppm Frequency Stability," *IEEE JSSC*, vol. 50, no. 7, pp. 1571-1580, July 2015.

[8] A. Andrei et al., "Reliability Study of AlTi/TiW, Polysilicon and Ohmic Contacts for Piezoresistive Pressure Sensors Applications," *IEEE SENSORS*, pp. 1125-1128, May 2004.

[9] Microchip Technology Inc., "AN8002 - AVR055: Using a 32kHz XTAL for Run-Time Calibration of the Internal RC," [Online]. Available: https://ww1.microchip.com/downloads/en/Appnotes/doc8002.pdf. Accessed Sept. 2022.

978-1-6654-9016-0/23/$31.00 ©2023 IEEE