Temperature Sensor based on 4H Silicon Carbide with Measurement Range up to 400°C

TEMPERATURE SENSOR BASED ON 4H SILICON CARBIDE WITH MEASUREMENT RANGE UP TO 400°C

Proefschrift

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door

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Efforts and courage are not enough
without purpose and direction.

John Fitzgerald Kennedy

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Michaël Chengshang Yuan,
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SUMMARY

WIDE band gap semiconductor has attracted significant industrial interest over the past decade with its superior properties: such as high critical electrical field, high thermal conductivity and wide band gap. Meanwhile many industries operating in harsh environments have long had demands for sensing solutions that function at high temperature. Current commercially available silicon-based temperature sensing IC has measure range limited to 155°C . This research work aims to develop a temperature sensor based on 4H silicon carbide with pronounced higher measurement range but comparable linearity. Furthermore, this work introduces silicon carbide based bipolar junction transistor (BJT) technology in the Else Kooi Lab (EKL).

Ratio-metric measurement technique from CMOS technology is adapted to eliminate PN diode and BJT's non-linearity as a temperature sensor; and devices are implemented experimentally on epitaxial 4H-silicon carbide wafers in the EKL.

The characterization data shows that diode version sensor operates to 400 °C with a R^2 value of 0.9963, the sensitivity under 1 mA constant current source is 4.8 mV/°C . The BJT version operates to 200 °C with a R^2 of 0.9965. In the future the sensor's integration with pressure, gas, and other types of sensing solutions can provide a comprehensive sensing package. Such a package can be used to predict life time of critical components in harsh environment installations; and hence reduce the maintenance cost. Examples of application scenarios include oil&gas exploration, industrial furnaces, geothermal extraction, and so on.

SAMENVATTING

WIDE band gap halfgeleider heeft het afgelopen decennium veel industriële belangstelling getrokken met zijn superieure eigenschappen: zoals een hoog kritisch elektrisch veld, hoge thermische geleidbaarheid en brede bandgap. Ondertussen hebben veel industrieën die in ruwe omgevingen opereren, al lang behoefte aan sensoroplossingen die bij hoge temperaturen werken. De huidig, commercieel verkrijgbare temperatuursensor IC, welk op silicium gebaseerd is, heeft een meetbereik dat beperkt is tot 155 °C . Dit onderzoekswerk heeft tot doel een temperatuursensor te ontwikkelen op basis van 4H siliciumcarbide met een uitgesproken hoger meetbereik maar vergelijkbare lineariteit. Bovendien introduceert dit werk de op siliciumcarbide gebaseerd bipolaire junctietransistor (BJT) technologie in Else Kooi Laboratorium.

De ratiometrische meettechniek van CMOS-technologie is aangepast om de niet-lineariteit van PN-diodes en BJT als temperatuursensor te elimineren; en apparaten worden experimenteel geïmplementeerd op epitaxiale 4H-siliciumcarbide substraten in het EKL-laboratorium.

De karakteriseringsgegevens laten zien dat de diodeversie van het sensor tot 400 °C werkt met een R2-waarde van 0,9963. Hier is de gevoeligheid onder 1 mA constante stroombron, 4,8 mV/°C . De BJT-versie werkt tot 200 met een R2 van 0.9965. In de toekomst kan de integratie van de sensor met druk-, gas- en andere soorten detectieoplossingen een uitgebreid detectiepakket opleveren. Een dergelijk pakket kan worden gebruikt om de levensduur van kritieke componenten in installaties in ruwe omgevingen te voorspellen; en dus de onderhoudskosten verlagen. Voorbeelden van toepassingsscenario's zijn onder meer olie- en gasexploratie, industriële ovens, geothermische winning, enzovoort.

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INTRODUCTION

WIDE band gap (WBG) semiconductors are semiconductor materials that have higher energy band gaps than conventional semiconductor materials. For example, silicon carbide(SiC) as a WBG material has an band gap energy of 3.25 eV; gallium nitride(GaN) has a band gap energy of 3.4 eV. On the other hand, silicon as a conventional semiconductor material has a band gap of 1.1 eV; germanium has a band gap of 0.7 eV [1]. Generally, the electronic properties of WBG materials fall in between those of semiconductors and insulators. WBG semiconductor allows devices to function at higher temperature, higher frequencies, and higher voltages than conventional semiconductor materials. They are the critical components in military radars, lasers, and short-wavelength LEDs. They are also one of the leading candidates for next-generation semiconductor devices of general use.

Among the large group of WBG semiconductor materials, SiC is a candidate that has attracted extensive industrial interest with its outstanding electrical and physical properties[2]–[4]. The low intrinsic concentration and high band gap energy enable SiC devices to function at much higher temperature than silicon ones. Moreover, the high thermal conductivity, high break-down electrical field, and high saturation electron velocity makes them suitable for operating under extreme conditions. Over the past decade, there has been intensive research efforts into its application in harsh environments electronics and sensors[5].

The reasoning for SiC's superior material properties lies in silicon-carbide bond's high strength[6]. There exist a huge number of different crystal structure built from the same silicon-carbon grouping; they are known as polytypes when organized into diverse stacking sequences. Although over 100 polytypes exist, R&D efforts have been focused on only three polytypes: 6H, 4H and 3C. Critical properties of those SiC polytypes and other semiconductor materials are presented in table 1.1. Growth technology of 6H-SiC was advancing faster in the beginning because it was used as the substrate in producing GaN blue LEDs. However,4H-SiC demonstrated superior material properties and are preferred for other electronics devices; for example, its on-axis mobility is ten times as high as that of the 6H-SiC. Moreover,the high band gap of 3.25 eV significantly re-

duces the number of electron-hole pairs resulting from the thermal activation through the band gap; and that enable the devices made from it operational at higher than 400°C [7]. 3C-SiC is more suitable to fabricate MEMS sensor because it can grow on the silicon wafer; this property considerably reduces the manufacturing costs[8].

Table 1.1: Material Properties,source [9]

Property	Si	Diamond	3C-SiC	4H-SiC	6H-SiC
Energy Bandgap [eV]	1.12	5.5	2.3	3.0	3.2
Critical Field [MV/cm]	0.6	5	1.8	2.5	2.5
Thermal Conductivity [W/cmK]	1.5	20	3-5	3-5	3-5
Saturated Electron Velocity [10^{-7} /s]	1.0	2.8	2.5	2.0	2.0
Electron Mobility [cm^2/Vs]	1200	Very high	750	400	800
Hole Mobility [cm^2/Vs]	420	Very High	40	90	115
Young's Modulus [GPa]	190	1035	450	450	450
Chemical Stability	Fair	Fair	Excellent	Excellent	Excellent
Yield Strength [GPa]	7	53	21	21	21

1.1. MOTIVATION AND PROBLEM FORMULATION

Conventional silicon-based IC gives a limited temperature range: when the temperature becomes high, the crystal lattice expands and the atomic bonds become weakened. The energy required for an electron to jump into the conduction band hence decreases. If the density of the carrier increases tremendously, the current increases sharply. Then semiconductor material reaches the characteristics similar to conductor. Therefore, the silicon-based IC typically has a limited temperature range up to 155°C [10]. In the research work of Zhang Nuo, the diode technology based the 4H-SiC has the measurement range up to 600°C [7]. However, this technology is still in the research phase. Current commercially mature temperature sensing technologies can be mainly divided into four categories: Resistance temperature detector(RTD), thermal-electrical thermometer(Thermal Couple), silicon temperature IC, and the thermistor. Table 1.2 gives an overview of the those technologies regard to their price, response time, measurement range, measurement precision, linearity and size. One can observe that existing sensing

Table 1.2: Overview of the commercially available temperature sensing technologies, source [11]–[14]

Type	Price	Response	Range	Precision	Linearity	Size
RTD	+++	1–7Sec	-200–500°	0.1–1°	++	3.175–6.350 mm
Thermal couple	++	<1Sec	-180–2320°	0.5–5°	++	2–3m
Silicon IC	++++	<1Sec	25–155°	<0.1°	+++	several cm^2
Thermistor	+	0.05–2.5Sec	-100–300°	0.1–1.5°	+	2–3m

technologies all have their shortcomings. RTD sensor's response time is long while the thermal couple doesn't give enough precision. Silicon-based IC is precise enough but the measurement range is limited. Thermistor has the disadvantage of negative temperature coefficient. If a sensor has the same precision level as the silicon-based IC, but

meanwhile with measurement range higher than the typical device, it will be a big improvement on the current sensing technology. Temperature sensing based on SiC has the potential to achieve such a goal; the thesis project designs and tests that idea.

Specifically, the three objectives of the thesis are:

- Develop a 4H-SiC Bipolar Junction Transistor (BJT) device level model based on epitaxial structure.
- Introduce a SiC epitaxial based BJT technology to Else Kooi laboratory (EKL).
- Develop a temperature sensor based on the BJT, it should have a significantly higher measurement range than conventional silicon technology and a comparable linearity.

1.2. THESIS OUTLINE

Content of the thesis are divided into six chapters; in addition to introduction, the rest five chapters are organized as follows:

- Chapter two gives the background theory of SiC materials properties, operating mechanism of temperature sensor based on pn diode ; operating mechanism of temperature sensor based on bipolar junction transistor, and devices' circuit design.
- Chapter three documents establishment of the 4H-SiC BJT model. Different parameters' impact on the device are examined, those parameters include devices' vertical, horizontal geometries, contacts positions, and doping concentrations.
- Clean room fabrication of the devices is presented in Chapter four. Relevant concepts and tools used for fabrication are first introduced for the reader's reference. Critical fabrication steps that impact the device's performance are then discussed. The reader can find the complete flowchart in appendix B.
- Chapter five reports the device characterization. Temperature sensors based on diodes and bipolar junction transistors are both tested. And Bipolar junction transistor's I-V characters are presented. This chapter also analyzes the non-linearity of the temperature performance.
- Chapter six concludes this master thesis work and gives future research directions.

2

Background Theory

This chapter provides the background theory of temperature sensor based on PN diode and BJT. First SiC's crystal structure and material properties are briefly covered in section 2.1; after that section 2.2 discusses the PN diode's operating mechanism, and its non-idealities as a temperature sensor. Section 2.3 investigates bipolar junction transistor's operating mechanism and its temperature dependence. This section provides the theory support for performance analysis in chapter five.

2.1. INTRODUCTION TO SILICON CARBIDE

2.1.1. CRYSTAL STRUCTURE

SiC is a compound semiconductor, both silicon and carbon are group IV materials. In its crystal lattice each silicon atom is tetrahedrally connected to four carbon atoms. The distance between the silicon atom and carbon one is approximately 1.89 Å; and the distance between Si-Si and C-C atoms is 3.08 Å [15]. Figure 2.1 shows the tetrahedrally bonded silicon carbon cluster.

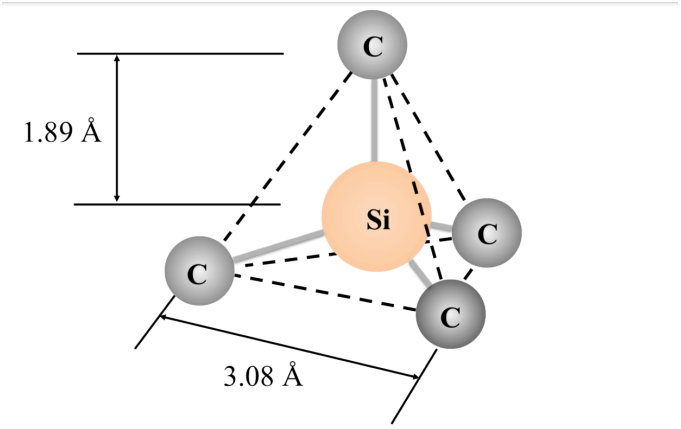


Figure 2.1: Bonded silicon carbon cluster, source[16]

There exist different SiC that have the same chemical composition but have different crystal structures. These are defined as polytypes. Over 100 different polytypes of SiC have been discovered, and the ones that have attracted most industrial research efforts are 3C-SiC, 4H-SiC and 6H-SiC.

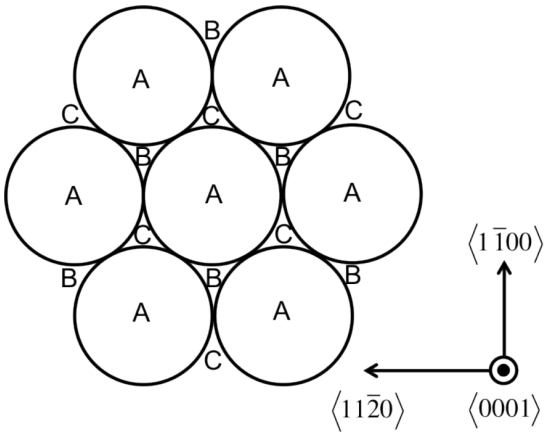


Figure 2.2: Hexagonal packing positions of silicon carbon pair,source[16]

The difference between those SiC polytypes falls in their silicon-carbon layer stacking sequence. Silicon-carbon pairs form a hexagonal pattern when they are stacked in a plane. Figure 2.2 depicts such an pattern; note that one silicon-carbon pair is represented as a sphere. The position of the first layer is indicated as A-site position; the next layer on top of the first layer can either land on the B-site position or one the C-site position. 4H-SiC's stacking sequence is ABCB; throughout the crystal lattice those four layers are repeated. Likewise, 6H-SiC's stacking sequence is ABCACB. Crystal Structures of 4H-SiC and 6H-SiC are both hexagonal. 3C-SiC is the only polytype that has a cubic crystal structure; its stacking sequence is ABC. Figure 2.3 shows the schematic structures of those three SiC polytypes.

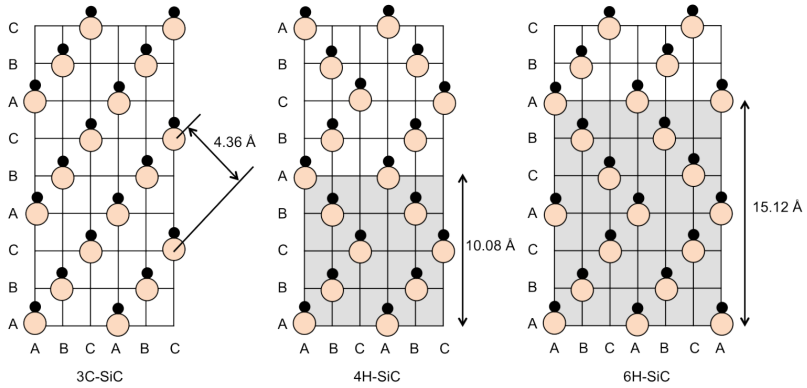


Figure 2.3: SiC-C pair's stacking sequences along the c-axis in 3C-, 4H-, and 6H-SiC, source[16]

2.1.2. MATERIAL PROPERTIES

SiC's superior electrical and physical properties make it suitable for harsh environment sensing applications. Low intrinsic carrier concentrations and wide band gap energy allows devices to operate at much higher temperature. In addition, high thermal conductivity, high saturation electron velocity, and high breakdown field permits SiC devices to function at harsh environments. It is noteworthy that SiC's mobility and critical field are anisotropic; they are dependent on the current flow and applied electric field. Table 1.1 is the overview of the common three polytypes' material properties; silicon and diamond's properties are added as a comparison. 4H-SiC is used in this research work as it has the highest band gap for temperature sensor.

2.2. PN DIODE AS A TEMPERATURE SENSOR

This section investigates PN diode's performance as a temperature sensor. Subsection 2.2.1 qualitatively discusses PN diode's operating mechanism. Subsection 2.2.2 develops PN diode ideal current voltage characteristics starting from electron concentration at a certain applied voltage. Subsection 2.2.3 gives a more accurate model of the I-V characteristics and clarifies its non-linearity as a temperature sensor.

2.2.1. QUALITATIVE OPERATION MECHANISM

When a piece of n-type and a piece of p-type semiconductor material are put together, electrons from the n-type material will diffuse into the p-type one and holes from the p-type material will diffuse into the n-type one, leaving positively charged acceptors in the n region and negatively charged donors in the p region. Charged acceptors and donors form an electrical field; such a field yields the drift current. In thermal equilibrium the drift current and diffusion current are of the same magnitude but are in opposite directions[17], hence the net current flow is zero.

Upon application of an external electrical field, such a diffusion-drift balance is disrupted. A forward bias favours the diffusion current, generating a net current from the p side to the n side and reducing the base-emitter depletion region length.

2.2.2. IDEAL DIODE CHARACTERISTICS

Subsection 2.2.1 gives a qualitative demonstration of PN diodes' operation. This subsection develops the quantitative relationship between the current and applied external voltage. The electron concentration on the p-side depletion region is given by[17]:

$$n_{p-side} = n_{p0} \cdot exp(\frac{eV}{kT}) \tag{2.1}$$

Similarly, the hole concentration on the edge of the n-side depletion region is

$$p_{n-side} = p_{n0} \cdot exp(\frac{eV}{kT}) \tag{2.2}$$

Equation 2.1 and equation 2.2 result from the Maxwell-Boltzmann approximation of the Fermi-Dirac probability function. The Fermi-Dirac probability function gives the probability of a quantum state at Energy level E occupied by an electron. It results from maxing the independent ways of arranging N electrons in a system with n energy levels. The probability function itself is

$$f_F(E) = \frac{1}{1 + exp(\frac{E-E_F}{kT})} \tag{2.3}$$

Assuming the difference between the quantum state energy E and Fermi energy is significantly higher than kT the 1 in the denominator of equation 2.3 could be eliminated, and the probability function reduces to its Maxwell-Boltzmann approximation:

$$f_F(E) = \frac{-(E_F - E)}{kT} \tag{2.4}$$

Figure 2.4 illustrates the range over which the approximation has reasonable accuracy.

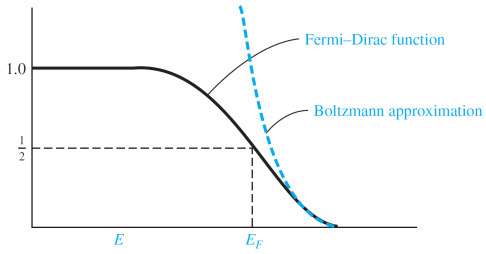


Figure 2.4: Difference between Fermi-Dirac function and Maxwell-Boltzmann approximation, source[17]

When an external electrical field V is applied to the diode, the Fermi energy position will change with V; therefore, we have the exponential dependency of minority carrier concentration on the applied voltage in equation 2.1 and equation 2.2. Away from the depletion region in the p-type material, the minority carrier concentration remains the thermal equilibrium values; hence there is a gradient at the depletion region and the area away from depletion. The gradient gives rise to diffusion current; the same mechanism happens in the n region. Total diffusion current can therefore be described by

$$I_D = \frac{qAD_n(n_{p-side} - n_{p0})}{L_n} + \frac{qAD_p(p_{n-side} - p_{n0})}{L_p} \tag{2.5}$$

A is the junction cross-section area, D_n and D_p are the diffusion coefficients of electrons and holes; L_n and L_p are their diffusion lengths. When equation 2.1 and equation 2.2 are substituted into equation 2.5, we have the classical diode characteristics:

$$I_D = I_S\left(exp(\frac{qV}{kT}) - 1\right) \tag{2.6}$$

In which saturation current I_S is

$$I_S = \frac{qAD_n n_{p0}}{L_n} + \frac{qAD_p p_{n0}}{L_p} \tag{2.7}$$

Assuming complete ionization, the electron and hole equilibrium concentration can be represented by intrinsic carrier concentration n_i, acceptor concentration N_a, and donor concentration N_d respectively.

$$n_{p0} = \frac{n_i^2}{N_a} \qquad p_{n0} = \frac{n_i^2}{N_d} \tag{2.8}$$

Substituting 2.8 into 2.7, the saturation current is simplified by

$$I_S = qAn_i^2\left(\frac{D_n}{L_n N_a} + \frac{D_p}{L_p N_d}\right) \tag{2.9}$$

When the forward voltage V is significantly larger than the thermal voltage $\frac{kT}{q}$, the -1 in equation 2.6 can be ignored. The voltage drop across the diode Vgiven an applied current I_D is then

$$V_{forward} = \frac{kT}{q} ln(\frac{I_D}{I_S}) \tag{2.10}$$

Theoretically diode's forward voltage is proportional to absolute temperature.

2.2.3. NON-IDEALITIES OF PN JUNCTION

In subsection 2.2.2, it is assumed that diffusion current is the only component of the conduction current. However, in the depletion region there is another recombination current component. Such an component is described by:

$$I_{rec} = I_{r0} \cdot exp(\frac{qV}{2kT}) \tag{2.11}$$

I_{rec} is the recombination current. The term I_{r0} is related to the intrinsic carrier concentration, minority carrier lifetime τ_0, depletion region length W, and cross-section area A

$$I_{r0} = \frac{eWn_iA}{2\tau_0} \tag{2.12}$$

The derivation of recombination current involves with Shockley-Read-Hall recombination and an assumption that the recombination rate is uniform across the depletion region. The total conduction current is the sum of equation 2.11 and equation 2.6. Since there is a 2 in the exponential term in equation 2.12, the total conduction current is given by:

$$I_D = I_S\left(exp(\frac{qV_{forward}}{nkT}) - 1\right) \tag{2.13}$$

n is the non-ideal factor in the range of 1 to 2. Under low forward bias, n approaches 2; under high bias, the diffusion dominates the recombination and n reaches 1. Equation 2.13 is a more accurate model compared to equation 2.48; in other words, the exponential behavior between current and voltage is distorted due to the recombination. If equation 2.13 is rewritten with voltage on the left:

$$V_{forward} = \frac{nKT}{q} ln(\frac{I_D + I_S}{I_S}) \tag{2.14}$$

The voltage is proportional to absolute temperature; but there is a non-ideal factor n. In bipolar junction transistor (BJT), such an recombination current is compensated by base current. In section 2.3, reader will see that I_S is also related to temperature. The diode voltage in regard to temperature is not completely linear.

2.3. BIPOLAR JUNCTION TRANSISTOR AS A TEMPERATURE SENSOR

Section 2.2 demonstrates the qualitative model of PN diode, the quantitative relationship between current and voltage, as well as its non-idealities from the ideal current voltage characteristics. At the end of that section, it is mentioned that BJT's base current compensates for the recombination current. Therefore, bipolar transistor's temperature characteristics is closer to the ideal exponential relation in equation 2.10. This section conducts a closer review on the device, and its performance as a temperature sensor. In subsection 2.3.1 the operating mechanism is presented, then non-linearity that impacts sensing performance is discussed in subsection 2.3.2; in the end voltage and currents' characteristics regard to temperature are investigated in subsection 2.3.3.

2.3.1. BJT'S OPERATING MECHANISM

A bipolar junction transistor consists of three regions: emitter, base, and collector. Depending on the whether the device is NPN or PNP, these three regions are doped with different dopants. Doping concentration in the emitter is highest among these three,

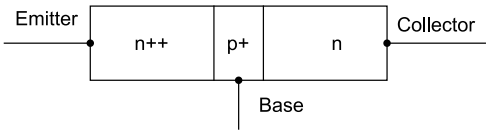


Figure 2.5: Simple sketch of a npn BJT

the base lower and collector the lowest. Typically base region has a smaller width compared with the other two. Figure 2.5 gives a simple sketch of a NPN transistor, the reason for relative doping concentrations and narrow base width will become clear as the theory develops. BJTs are normally biased in the *forward active* mode when working as a current

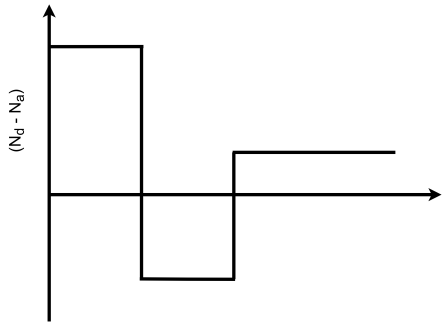


Figure 2.6: Ideal Doping of a npn BJT

amplifier: the base-emitter junction is forward biased while the base-collector junction is in reverse. During operation the forward voltage in the base-emitter pushes majority carrier electrons in the emitter into the base region, creating an excessive concentration of minority carrier; meanwhile, on the edge of the reversely-biased base-collector junction, the minority carrier electron concentration should be zero.

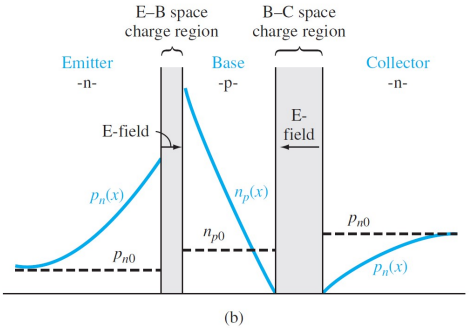


Figure 2.7: The gradient of current components, source[17]

As shown in Figure 2.7, the huge gradient of electrons makes them diffuse across the base region; then the electrical field in the space charge region of base-collector junction sweeps them into the collector. Since ideally as many electrons as possible should arrive at the emitter, the base width should be smaller than the diffusion length of the minority carrier; otherwise, the recombination with holes will dominate in the base region, resulting in an increased base current and decreased collector current.

Under the assumption that the minority carrier decreases linearly in the base region, the collector diffusion current is written as

$$i_C = eD_n A_{BE} \frac{dn(x)}{dx} = eD_n A_{BE} \left[\frac{n_B(0) - 0}{0 - x_B} \right] = \frac{-eD_n A_{BE}}{x_B} \cdot n_{B0} \cdot exp(\frac{v_{BE}}{V_t}) \tag{2.15}$$

D_n is the electron diffusion coefficient, A_{BE} is the cross-section area,n_{B0} is the thermal equilibrium concentration of electrons at the base edge and V_t is the thermal voltage. As far as multitude is concerned, equation 2.15 can be simplified as

$$i_C = I_S \cdot exp(\frac{v_{BE}}{V_t}) \tag{2.16}$$

Equation 2.16 illustrates the basic operation mode of a BJT transistor: a voltage-controlled current source in which i_C is controlled by v_{BE}.

Since the base-emitter junction is forward biased, the majority holes in the base region will be injected into the emitter region, this constitutes part of the emitter current. Similar to collector current, such a component is exponentially related to v_{BE}:

$$i_{E1} = I_{S1} \cdot exp(\frac{v_{BE}}{V_t}) \tag{2.17}$$

The second component, i_{E2} results from the electrons injected from emitter to base; hence it is i_C in essence. The Emitter current is the sum of these two components:

$$i_E = i_{E1} + i_{E2} = I_{SE} \cdot exp(\frac{v_{BE}}{V_t}) \tag{2.18}$$

As shown in equation 2.16 and equation 2.18, both i_C and i_E are functions of v_{BE}, their ratio is hence a constant.

$$\alpha = \frac{i_C}{i_E} \tag{2.19}$$

The constant is defined as the *common base amplification factor*. Since i_{E1} constitutes the base current, a higher i_{E1} also means a higher base current, it is optimal to keep α as close to one as possible. Ideally, the collector current is determined only by v_{BE} and independent of v_{CE}; the BJT works as a constant current source, as shown in Figure 2.8

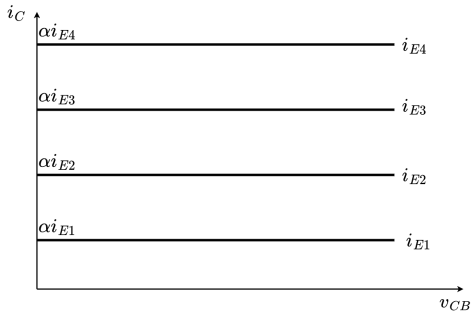


Figure 2.8: Theoretical collector current versus base collector voltage plot

In addition to i_{E1}, there is another component of base current. In the above discussion, we assumed the linear distribution of minority carrier concentration in the base, implying no recombination. However, the presence of majority carrier holes and minority carrier electrons makes recombination inevitable. Taking that into consideration, the consumed majority holes in recombination should be supplied by an influx of positive charges i_{Bb}; such an influx contributes to base current. To ensure the recombination current is as small as possible, the base width is normally designed narrow, smaller than the diffusion length of the minority carrier; this explains the relatively narrow width of base in figure 2.5.

The recombination rate of holes in the base depends on the minority carrier concentration and therefore base-emitter voltage v_{BE}. The total base current will be the sum of i_{E1} and i_{Bb}.

$$i_B = i_{Ba} + i_{Bb} = i_{E1} + i_{Bb} \tag{2.20}$$

As both components are exponentially related to v_{BE}, the base current is also proportional to $exp(\frac{v_{BE}}{V_t})$. Now the ratio of i_C and i_B will also be a constant:

$$\beta = \frac{i_C}{i_B} \tag{2.21}$$

β is defined as the *common emitter amplification factor*, it measures the amplification ability of a BJT and is usually in the order of tens to hundred in a SiC BJT device.

2.3.2. BJT'S NON-LINEARITY

DEVIATIONS IN CURRENT-VOLTAGE RELATIONSHIP

When the base-collector junction is reversely biased, carrier-generation occurs in the depletion region; this forms the first contributor of deviations in the $I_C - V_{BE}$ characteristics (The $I_C - V_{BE}$ plot is named the Gummel Plot). Another factor is the diffusion of minority carriers into the collector. When the base-collector voltage is zero, these two factors could be ignored.

But under such a condition, the minority carrier concentration at the base side of base-emitter junction is no longer zero, but equal to equilibrium carrier concentration. In the case of a PNP transistor, we take the symbol p_{B0}; The hole concentration at the emitter side of the base region is represented as $p_{n,emi}$. Although equation 2.15 applies to NPN transistors, similar collector characteristics hold for PNP devices:

$$i_C = eD_p A_{BE}\left[\frac{p_{n,emi} - p_{B0}}{0 - x_B}\right] = \frac{-eD_p A_{BE}}{x_B} \cdot p_{B0} \cdot \left(exp(\frac{v_{BE}}{V_t}) - 1\right) \tag{2.22}$$

To make it straightforward

$$I_C = I_S\left(exp(\frac{qV_{BE}}{kT}) - 1\right) \tag{2.23}$$

Equation 2.23 renders ΔV_{BE} in the optimal PTAT performance in equation 2.48 as

$$\Delta V_{BE} = \frac{kT}{q} \cdot ln(\frac{pI_{C1} + I_S}{I_{C1} + I_S}) \tag{2.24}$$

Only if I_{C1} and pI_{C1} are significantly higher than I_s is the PTAT voltage reasonably accurate. Such a requirement is particularly important at higher operating temperature as the saturation current increases significantly with temperature. (The detailed reason will be clear in the later sections)

When building the device I_C cannot be set at a random high value. As the base-emitter voltage increases, the low-level injection assumption no longer holds. In other words, the minority carrier concentration in the base due to V_{BE} reaches the same multitude as the majority carrier concentration. Figure 2.9 illustrates the effect of high-injection. Meanwhile, at the lower bias, the recombination current dominate.

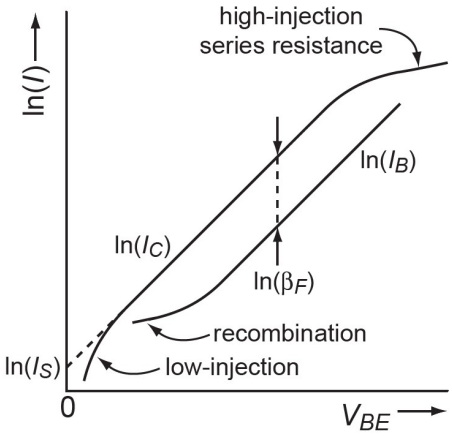


Figure 2.9: High and low injection, source[18]

To conclude, in the range where I_C is way larger than I_S but not so big as to get into the high-injection region, the current can be accurately used in PTAT application.

NON-IDEALITIES IN DIODE CONNECTION

In the CMOS technology driving the advances of integrated circuits industries over the past decades, bipolar junction transistors are usually the parasitic devices. As a result, the collectors of BJT are on the substrate and are not accessible. Such a configuration is called a diode connection, Figure 2.10 shows the diode connection of a NPN device.

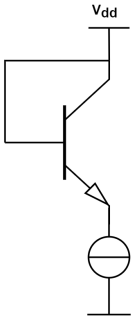


Figure 2.10: Diode connection of a BJT

By connecting base and collector, the base-collector voltage becomes zero and the resulting collector current is smaller than the applied emitter current:

$$I_C = I_E - I_B = \alpha_F \cdot I_E = \frac{\beta_F}{1+\beta_F} \cdot I_E \tag{2.25}$$

In this equation, α_F is the common base gain factor, and β_F is the ratio between I_C and

I_B. α_F denotes how much emitter current arrives at the collector region, ideally it should be unitary.

To make sure the generated voltage is proportional to temperature, as in equation 2.48, we need to make sure that α_F is current independent. In other words, the applied emitter currents ratio should yield exactly the collector currents.

α_F is determined by the base currents. It can be divided into three factors and these three factors concern the corresponding base current mechanisms.

$$\alpha_F = \gamma \cdot \alpha_T \cdot \delta \tag{2.26}$$

γ is the emitter injection efficiency. It describes the fact that there is a small diffusion electron current into the emitter from the base in a PNP transistor. The associated base current in this case is:

$$I_{B1} = \frac{qAn_{iE}^2\overline{D_n}}{L_n N_a} \cdot exp\left(\frac{qV_{BE}}{kT}\right) \tag{2.27}$$

In this equation the $\overline{D_n}$ is the average diffusion constant of the minority carrier in the emitter; Ln is the diffusion length of it. N_a is the emitter acceptor doping concentration and n_{iE} is the intrinsic carrier concentration in this region. To increase the emitter injection efficiency: there are two approaches. Either by increasing N_a to decrease the I_B, as shown in equation 2.27. Or decreasing the base-emitter width x_B, as illustrated in 2.15 so that the collector current becomes larger while the base current remains the same.

The base transport factor is defined as the ratio of minority carrier flux to the collector and the minority carrier flux entering the base from the emitter. Under the assumption that B-E junction are forward biased efficiently so that $exp\left(\frac{qV_{BE}}{kT}\right)$ is larger than 1, and the assumption that base width x_B is way smaller than the minority carrier diffusion length L_B,the base transport factor can be approximated as:

$$\alpha_T = \frac{1}{cosh(\frac{x_B}{L_B})} = \frac{1}{1+\frac{1}{2}(x_B/L_B)^2} = 1 - \frac{1}{2}(x_B/L_B)^2 \tag{2.28}$$

The third factor of the δ concerns the recombination in the base-emitter junction region, emitter-base channel, and the surface recombination. Processing defects yield surface traps and other traps and result in a current component

$$I_{B3} \propto exp(\frac{qV_{BE}}{n_E kT}) \tag{2.29}$$

n_E is the low-current forward emission coefficient. It ranges from 2 to 4 depending on the density of the current. The only factor that does not have the same relationship with V_{BE} as the collector current is δ. At high currents, the base current from recombination indicated by δ is negligible, making a high β and also the same emitter and collector current ratios. But at the low current scenario, the impact of δ becomes dominant and hence the emitter and collector ratios become twisted.

To wind up, if the BJT has a range where β_T is constant regardless of the applied current, then this current range provides optimal PTAT performance. In the substrate PNP BJT in the CMOS industry, it provides such a range. In our test of the SiC counterpart, such a range should be measured to verify the device's capacity for PTAT temperature measuring application.

2.3.3. BJT'S TEMPERATURE DEPENDENCE

In section 2.2, equation 2.7 gives the expression of the saturation current in a diode at an ideal situation. A BJT is in essence two diode connected together. However, their $I_C - V_{BE}$ characteristics are different. Consider an NPN transistor operating in forward active region. The injection of electrons into the base induces a minority carrier concentration $n_{p,em}$ at the emitter side. It is larger than the equilibrium minority carrier in the base, but still way smaller than the majority carrier concentration (the low-injection assumption). The carrier concentration is proportional to the exponential V_{BE}, its expression is given by:

$$n_{p,em} = n_{p0} \cdot exp(\frac{qV_{BE}}{kT}) \tag{2.30}$$

Such an exponential term results from The Boltzmann approximation to the Fermi-Dirac distribution function. The equilibrium minority carrier concentration is given by:

$$n_{p0} = \frac{n_i^2}{N_a} \tag{2.31}$$

n_i is the intrinsic carrier concentration, and N_a is the acceptor concentration in the base.

As we have discussed in subsection 2.3.1, if the base width is small compared with minority carrier diffusion length L_n and the base-collector junction is reversely biased. Then the minority carrier concentration at the collector side of the base region is zero. The diffusion of electrons could be simplified as a linear process, the diffusion current is:

$$I_C = \frac{qA\overline{D_n}n_{p,em}}{W_B} \tag{2.32}$$

A is the emitter area, $\overline{D_n}$ is the average diffusion constant. W_B is the width of the base region.

Combining equation 2.30, equation 2.31 and equation 2.32, we have the classical $I_C - V_{BE}$ characteristics.

$$I_C = I_S \cdot exp(\frac{qV_{BE}}{kT}) \tag{2.33}$$

The saturation current is given by:

$$I_S = \frac{qAn_i^2\overline{D_n}}{W_B N_a} \tag{2.34}$$

In the denominator $W_B N_a$ is the so-called Gummel characteristics G_B, it tells the number of impurities per unit area. When the doping is not uniform, it is the integral of doping concentration over the base width. The average electron diffusion constant appears from the Einstein relation:

$$\frac{\overline{D_n}}{\overline{\mu_n}} = \frac{kT}{q} \tag{2.35}$$

And the saturation current can thus be expressed as

$$I_S = \frac{kTAn_i^2\overline{\mu_n}}{G_B} \tag{2.36}$$

Now we have derived I_S, let us investigate how the individual terms are related to temperature. The equation could be then rewritten as:

$$I_S(T) = \frac{kTAn_i^2(T)\overline{\mu_n}(T)}{G_B(T)} \tag{2.37}$$

The intrinsic carrier concentration's dependency on temperature is given by

$$n_i^2(T) \propto T^3 exp(\frac{-qV_g(T)}{kT}) \tag{2.38}$$

$V_g(T)$ is the band-gap voltage of the material. We can assume that $V_g(T)$ is a linear function at this moment

$$V_g(T) = V_{g0} - \alpha T \tag{2.39}$$

V_{g0} is the extrapolated band gap voltage at 0 K[19]. The effective electron mobility $\mu_n$is proportional to T^{-n}, and n is a constant. Because of the bandwidth modulation effect, the Gummel number is in reality dependent on temperature. But for the sake of discussion, at this moment we assume that the Gummel number is constant at different temperatures. When putting together the temperature dependencies of all those terms, the saturation current can be written as

$$I_S(T) = CT^{\eta} exp\left(\frac{-qV_{g0}}{kT}\right) \tag{2.40}$$

$\eta = 4 - n$ and C is a constant. When putting equation 2.40 into equation 2.33, we have the I_C characteristics dependent on temperature

$$I_C(T) = CT^{\eta} \cdot exp\left(\frac{q(V_{BE}(T) - V_{g0})}{kT}\right) \tag{2.41}$$

It could be rewritten as

$$V_{BE}(T) = V_{g0}(1 - \frac{T}{T_r}) + \frac{T}{T_r}V_{BE}(T_r) - \eta\frac{kT}{q}ln(\frac{T}{T_r}) + \frac{kT}{q}ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \tag{2.42}$$

In the equation, $V_{BE}(T_r)$ is the base-emitter voltage at the reference temperature T_r

In the Spice simulation to verify this model, it is found that there is a great discrepancy between the measurement result and the model prediction. The difference is usually in the order of several microvolts. Tsividis proposed that this difference originated from the inaccurate assumption we made in equation 2.39. He gave another model of $V_g(T)$, which reduces the inaccuracy by an order of magnitude[20]. In Meijer's work, it is demonstrated that the inaccuracy is further reduced to less than 0.1 ,microvolt if η and V_{g0} in equation 2.42 are derived from the measured $V_{BE}(T)$ data[21]. Those derived values of η and V_{g0} are often found in conflict with the physics discussed above. The η is found at 4.3, but since $\eta = 4 - n$ it is not allowed to be bigger than 4. Such a discrepancy resulted from the inaccurate physical models such as the temperature dependency of V_g in equation 2.39.

Meijer also proposes another interesting aspect of presenting his model. He presents equation 2.42 as a linear approximation with a nonlinear curvature residue:

$$V_{BE}(T) = \underbrace{V_{BE0} - \lambda T}_{\text{tangent at } T=T_r} + c(T) \tag{2.43}$$

T_r is a reference temperature, it could be any random temperature at which the V_{be} is measured. $c(T)$ is the non-linearity; from the Fourier transform of equation 2.42,it is derived as:

$$c(T) = \frac{k}{q}\eta\left(T - T_r - T\ln\left(\frac{T}{T_r}\right)\right) + \frac{k}{q}\left(T\ln\left(\frac{I_C(T)}{I_C(T_r)}\right) - (T - T_r)\frac{T_r}{I_C(T_r)}\left[\frac{\partial I_C}{\partial T}\right]_{T=T_r}\right) \tag{2.44}$$

λ is the slope of the tangent line from temperature T_r.

$$\lambda = \frac{V_{BE0} - V_{BE}(T_r)}{T_r} \tag{2.45}$$

V_{BE0} is the extrapolation of the tangent line to zero temperature. To calculate it, refer to equation 2.44 and equation 2.42 we have:

$$\begin{aligned} V_{BE0} &= V_{g0} - c(0) \\ &= V_{g0} + \frac{kT_r}{q}\left(\eta - \frac{T_r}{I_C(T_r)}\left[\frac{\partial I_C}{\partial T}\right]_{T=T_r}\right) \end{aligned} \tag{2.46}$$

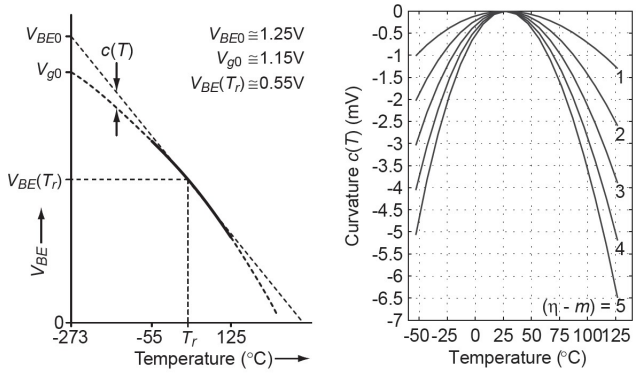


Figure 2.11: On the left is the temperature dependency of base emitter voltage (the curvature is exaggerated), on the right is the curvature at different (η- m), T_r = 300 K, source[22]

Figure 2.11 shows the V_{BE} and the curvature based on the model. In the data gathered from CMOS processing by Wang the curvature from temperature -50 °to 125 °mounts to 4 micro volt[23], which is in line with the model's prediction.

2.4. RATIOMETRIC TEMPERATURE MEASUREMENT

As discussed in section 2.2 and section 2.3, the performance of both devices as a temperature sensor is not perfect regarding their linearity. This section presents the ratiometric

measurement techniques to tackle this issue. Subsection 2.4.1 gives the theoretical concept for reducing non-linearity. Subsection 2.4.2 presents the circuit implementation in our research work.

2.4.1. PROPORTIONAL TO ABSOLUTE TEMPERATURE

All device characteristics in integrated circuits depend on temperature, the mechanisms of temperature sensors hence are largely based on the temperature dependency of devices; such as resistors[24], [25], diodes[26], MOS transistors[27], and bipolar junction transistors (BJT)[28], [29]. Most devices' characteristic on temperature, however, are non-linear and have offset. One solution is to use a reference signal and compare the measured signal to the reference[30]. In other words, the difference in base-emitter voltage ΔV_{BE} between two transistors is PTAT should these two transistors be biased at different current densities. Figure 2.12 gives an example of the proportional to absolute temperature set up with a Bipolar Junction Transistor.

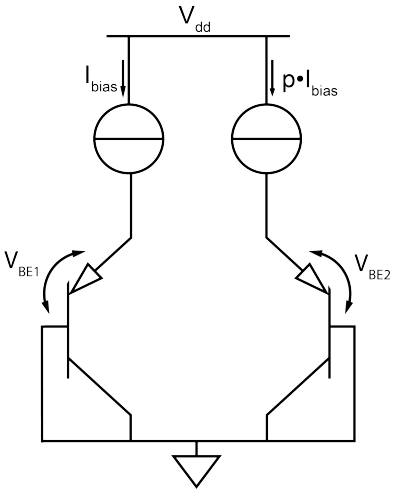


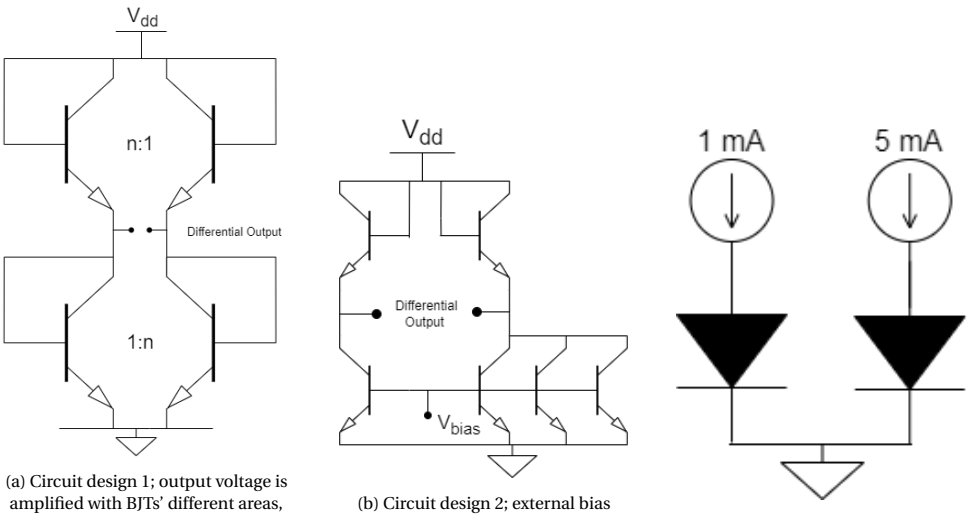
Figure 2.12: the PTAT configuration of two diodes

In the simplest model, the voltage across a diode is related to the thermal voltage $\frac{kT}{q}$ and the current through the diode, as shown in equation 2.47

$$V_D = \frac{kT}{q} ln(\frac{I_D}{I_S}) \tag{2.47}$$

As discussed in subsection 2.3.2, equation 2.40 illustrates that saturation current is exponentially dependent on temperature at different biasing conditions. Therefore, a single diode or BJT's output voltage in regard to temperature is non-linear. The ratiometric measurement method applies two current $I_D = I_1$, and $I_D = p \cdot I_1$ to a diode consecutively. The difference in the voltage drops is given by[31]

$$\Delta V = \frac{kT}{q} ln(\frac{I_1}{I_S}) - \frac{kT}{q} ln(\frac{p \cdot I_1}{I_S}) = -\frac{kT}{q} ln(p) \tag{2.48}$$



(a) Circuit design 1; output voltage is amplified with BJTs' different areas, source [32]

(b) Circuit design 2; external bias fixes the sensor's linearity

(c) Test circuit for the diode sensor

Figure 2.13: Three schematics of the temperature sensor

Theoretically, the saturation current is cancelled and the output temperature is PTAT with high linearity. Another option is to inject currents of different amplitudes into devices of same fabrication batch. In this manner the process variation is minimized. Furthermore, this measurement technique gives designer the possibility to increase the temperature sensor's output voltage amplitude with area design.

2.4.2. CIRCUIT LEVEL DESIGN

This section presents the two schematics of temperature sensor. In schematic one, the area ratio of the top two transistors is different from the that of the bottom two transistors. On the left arm, output voltage is $\frac{1}{n+1}$ of V_{dd}; on the right arm output voltage is $\frac{n}{n+1}$ of V_{dd}. The differential output voltage is then $\frac{n-1}{n+1}$ of V_{dd}. The output voltage is in the same amplitude of V_{dd} when n is large enough, therefore there is no need for additional amplifier to process the signal. In schematic two, the external bias sets the current of those two arms at exactly a ratio of 3:1; hence the linearity is expected to be better than schematic one. Schematics three tests the diode temperature sensor with external current source. Its disadvantage is the external precise current meter needed.

3

DEVICE DESIGN AND SIMULATION

This chapter documents the establishment of the device level model of the SiC BJT. Section 3.1 introduces the simulation setup; section 3.2 presents a selection of the physics models involved for reader's reference. In section 3.3 the simulation result and its analysis is given.

3.1. SIMULATION SETUP

In the semiconductor device development flow, the Technology Computer Aided Design (TCAD) aims to give an accurate prediction of devices' thermal, electrical, and physical characteristics. The whole process consists of process simulation and device simulation. Process simulation sketches the dopant profile, device geometry, and stress profiles of the device; it serves as a prerequisite for device simulation, which concerns the electrical characteristics.

In this design, Synopsys Sentaurus is chosen as the TCAD tool. In addition to the process and device simulation, the software suit also has visualization instruments to support inspection. Originally from the Standard University Processing Modelling program, it was created by combining features of existing process simulation tools in 2004. Industrial partners include Samsung Electronics, Infineon Technologies, PowerJazz, Onsemi, and so on.

3.2. PHYSIC MODELS

Appropriate physics models in TCAD Sentaurus give accurate simulation results with the fabricated device. Here the physics models concerning a Bipolar Junction transistor's performance are presented, those physical models give directions in device designs and insights.

3.2.1. BAND GAP NARROWING(BGN)

When a high concentration of doping is injected into the material, the orbitals of impurities start to overlap. As a result, the discrete energy levels of impurities start to form an energy band. Additionally, random distribution of impurities also results in potential fluctuations and hence a broadened impurity band. Ionization energy level of impurity is therefore reduced. When the impurity band overlaps with the valence or conduction band, the band-gap energy is narrowed[33], [34]. In the research work carried out by Schubert, it is pointed out that such a phenomenon is particularly pronounced when doping exceeds 10^{17} cm^{-3}[35]. In our design doping of emitter and collector ohmic layers both exceed $10^{18} cm^{-3}$; hence BGN is important in understanding the device's characteristics in the data analysis of the next chapter.

By default Synopsys models the density of states with the following equations:

$$g_c(E) = \frac{dN_c(E)}{dE} = \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{3/2}(E_g - E_c)^{1/2} \tag{3.1}$$

$$g_v(E) = \frac{1}{2\pi^2}\left(\frac{2m_h^*}{\hbar^2}\right)^{3/2}(E_v - E_g)^{1/2} \tag{3.2}$$

the band gap energy should vary as a function of the doping level. In our simulation we adopt the classical Slotboom model[19]:

SLOTBOOM MODEL

The change in the band gap energy is

$$\Delta E_g = E_{ref}\left(ln\left(\frac{N_I}{N_{ref}}\right)+\sqrt{[ln(\frac{N_I}{N_{ref}})]^2+\frac{1}{2}}\right) \tag{3.3}$$

In equation 3.3 $N_I = N_a + N_d$, and the other parameters are material properties. The fraction of band gap narrowing taken up by the conduction is also considered material-specific, in silicon, it is 0.5.

However, in Donna's research, it is suggested that the slotboom model is not accurate enough to predict the diode's forward characteristics[36]. The authors proposed that the model provided by Schubert gives better accuracy[37]:

SCHUBERT MODEL

$$\Delta E_g = \frac{-q^2\beta}{4\pi\epsilon_0\epsilon_r} \tag{3.4}$$

In this model β is the Tomas-Fermi Screening length. In the data analysis part of the next chapter, the accuracies of those two models will be verified.

3.2.2. INCOMPLETE IONIZATION

Incomplete ionization refers to the situation when the temperature within a semiconductor is so low that the donor or acceptor impurity atoms are not fully activated. The carrier concentration will hence not be the same as the dopant concentration. For nitrogen donors or aluminum acceptors in silicon carbide, the impurity energy levels are deeper than the thermal energy $k \cdot T$. Incomplete ionization should thus be taken into account in these cases.

Fermi-Dirac distribution describes the concentration of the ionized impurity atoms:

$$N_D = \frac{N_{D,0}}{1+g_D\exp\left(\frac{E_{F,n}-E_D}{kT}\right)} \tag{3.5}$$

$$N_A = \frac{N_{A,0}}{1+g_A\exp\left(\frac{E_A-E_{F,p}}{kT}\right)} \tag{3.6}$$

In Equation 3.5 and Equation 3.6 $N_{D,0}$ and $N_{A,0}$ are the substitution donor and acceptor concentrations. g_D and g_A are the degeneracy factors for impurity levels. E_D and E_A are the activation energies. In another model proposed by Matsuura [38], the general distribution function for the incomplete ionization is given as

$$N_D = \frac{N_{D,0}}{1+G_D(T)\exp\left(\frac{E_{F,n}-E_C}{kT}\right)} \tag{3.7}$$

$$N_A = \frac{N_{A,0}}{1+G_A(T)\exp\left(-\frac{E_{F,p}-E_V}{kT}\right)} \tag{3.8}$$

The $G_D(T)$ and $G_A(T)$ are the ionization factors proposed in [39] and [40] In the lower part of our measurement range incomplete ionization might contribute to some deviant behaviors of the temperature sensor.

3.2.3. RECOMBINATION MODELS

The rate at which the electrons and holes recombine plays an important role in devices' characteristics. This is especially important for Silicon carbide BJTs as abundant surface traps are present at the interface of silicon carbide and oxide [16], [41], [42].

In thermal equilibrium situation, and under the assumption of low-injection, the recombination rate is inversely proportional to the mean carrier lifetime. In a piece of infinitely large p-type material the thermal-equilibrium recombination rate is given as[17]:

$$R'_n = -\frac{\mathrm{d}\delta_n(t)}{\mathrm{d}t} = \alpha_r p_0 \delta_n(t) = \frac{\delta_n(t)}{\tau_{n0}} \tag{3.9}$$

τ_{n0} is the minority carrier lifetime and under this circumstance, it is simply related to α_r and minority carrier concentration.

During device fabrication there are always defects on the lattice and the ideal periodic potential function is no longer valid. If the concentration of the defects within the material is not great, they will create discrete energy states within the forbidden-energy band gap. Otherwise, those states need to be accounted for explaining some unexpected results.

In the following sections, the impact those states have on the device's behavior will be investigated.

SCHOCKLEY-REAL-HALL MODEL (SRH) OF RECOMBINATION

An allowed energy state within the forbidden band gap is called a trap and it acts as a recombination center. The electrons and holes will get captured by the center with equal probability. In the Schockley-Real-Hall model, the energy of the trap is assumed to be E_t. There are four basic processes[17]:

- Process 1: the capture of an electron from an conduction band by an initially empty trap.
- Process 2: the emission of an electron that is from an occupied trap back to the conduction band.
- Process 3: the capture of a hole from the valence band by a trap containing an electron (we could also consider it in another way, there is an electron emission from the trap into the valence band.
- Process 4 is the other way of process 3: the emission of a hole from a neutral trap into the valence band. (Or there is an electron from the valence band being captured by the trap)

In process 1, the rate of combination is proportional to the density of electrons in the conduction band and the density of empty trap states. The capture rates are given by:

$$R_{cn} = C_n N_t \left[1 - f_F(E_t)\right] n \tag{3.10}$$

In equation 3.10, R_{cn} is the capture rate ($\#/cm^3 - s$) and C_n is the constant proportional to the electron-capture cross section; N_t is the total concentration of trapping centers

and n is the electron concentration in the conduction band. $f_F(E_t)$ is the fermi function at the trap energy level. More specifically,

$$f_F(E_t) = \frac{1}{1+\exp\left(\frac{E_t - E_F}{kT}\right)} \tag{3.11}$$

It gives the probability that an electron is present inside the trap. $[1 - f_F(E_t)]$ is then the probability that a trap is empty.

For process 2, the rate at which the electrons emit from the traps is proportional to the density of filled traps.

$$R_{en} = E_n N_t f_F(E_t) \tag{3.12}$$

In the equation

R_{en} = emission rates $(\#/cm^3 - s)$

E_n = constant

$f_F(E_t$ = the probability that the trap is occupied.

Under thermal equilibrium, the emission of electrons from the traps should be the same as the capture of electrons from the conduction band. Therefore we have:

$$E_n N_t f_{F0}(E_t) = C_n N_t \left[1 - f_{F0}(E_t)\right] n_0 \tag{3.13}$$

f_{F0} denotes the thermal-equilibrium Fermi function. In this case, the n_0 is the electron concentration in the conduction band at thermal equilibrium. With Boltzmann approximation, we could write E_n in terms of C_n as

$$E_n = C_n n' \tag{3.14}$$

n' is equivalent to the concentration of electrons that would have existed if the quasi-Fermi energy level E_F coincided with trap energy level E_t.

$$n' = N_c \exp\left[\frac{-(E_c - E_t)}{kT}\right] \tag{3.15}$$

it is equivalent to the electron concentration if the Fermi energy level is at E_t.

Now we have discussed the situation of thermal equilibrium. Let's investigate the non-equilibrium scenarios. In this case, the excessive electrons exist; so the net rate of electrons captured from the conduction band is given by:

$$R_n = \left[C_n N_t \left(1 - f_F(E_t)\right) n\right] - \left[E_n N_t f_F(E_t)\right] \tag{3.16}$$

It is noteworthy that in non-equilibrium scenarios, n refers to the total electron concentration, including the thermal-equilibrium one and the excessive concentration. Also, the Fermi energy level in the Fermi probability function should be replaced by the quasi-Fermi energy. Given the relation of E_n and n' in equation 3.14, the net combination rate is given as:

$$R_n = C_n N_t \left[n\left(1 - f_F(E_t)\right) - n' f_F(E_t)\right] \tag{3.17}$$

And in the case of process 3 and process 4, the net rate holes captured from the valence band are given by

$$R_p = C_p N_t \left[p f_F(E_t) - p'\left(1 - f_F(E_t)\right)\right] \tag{3.18}$$

Where C_p is a constant proportional to the hole-capture cross-section, and p' is the hole concentration in valence band in non-equilibrium, including the excess hole concentration:

$$p' = N_v \exp\left[\frac{-(E_t - E_v)}{kT}\right] \tag{3.19}$$

If the trap density is not too large, the excess hole and electron concentration should equal; so do the combination rate of electrons and capture rate of holes. Put equation 3.16 and equation 3.18 in equal and solve the Fermi function, we have

$$f_F(E_t) = \frac{C_n n + C_p p'}{C_n(n + n') + C_p(p + p')} \tag{3.20}$$

In equation 3.15 and equation 3.19, it is figured out that $n'p' = n_i^2$. Substituting equation 3.20 into equation 3.17 or equation 3.18, the recombination rate of electrons and holes due to the traps at energy level E_t is:

$$R_n = R_p = \frac{C_n C_p N_t (np - n_i^2)}{C_n(n + n') + C_p(p + p')} \equiv R \tag{3.21}$$

In the case of thermal equilibrium, we have $np = n_i^2$. Then equation 3.21 is zero. It represents the recombination rate of excess electrons and holes. Now that R in equation is the recombination rate of both electrons or holes:

$$R = \frac{\delta n}{\tau} \tag{3.22}$$

Similar to equation 3.9, δn is the excess carrier concentration, and τ is the excess carrier lifetime.

SIMPLIFICATION OF SRH MODEL

The previous section gives the deduction of the Schockley-Real-Hall model; in the end, equation 3.21 gives the accurate recombination rate of electrons and holes at a certain energy level.

Nevertheless, equation 3.21 could be simplified under certain conditions. In the example of an n-type extrinsic material those two assumptions are:

- Low injection, which means the concentration of excess minority carriers is significantly lower than that of the minority carrier concentration. $n_0 \gg p_0, \quad n_0 \gg \delta p$
- The trap energy level is near mid-band gap so that n' and p' will not differ from intrinsic carrier concentration greatly. $n_0 \gg n', \quad n_0 \gg p'$

With the above-mentioned assumptions, equation 3.21 is reduced to

$$R = C_p N_t \delta p \tag{3.23}$$

Again, C_p is the constant related to the hole capture cross-section. To associate recombination rate with mean life carrier lifetime. Comparing equation 3.23 with equation 3.22:

$$R = \frac{\delta n}{\tau} = C_p N_t \delta p \equiv \frac{\delta p}{\tau_{p0}} \tag{3.24}$$

The minority hole lifetime is then

$$\tau_{p0} = \frac{1}{C_p N_t} \tag{3.25}$$

If the trap concentration increase, the probability of excess holes recombining will increase; therefore, the minority carrier lifetime decrease.

Similarly, in the case of p-type material, under the assumption of high injection and heavy doping $p_0 \gg n_0$, $p_0 \gg \delta n$, $p_0 \gg n'$, $p_0 \gg p'$, the minority carrier electron lifetime is given by:

$$\tau_{n0} = \frac{1}{C_n N_t} \tag{3.26}$$

Comparing equation 3.26 and equation 3.25, it is noteworthy that in the n-type material the minority carrier lifetime is related to the hole capture cross section while the minority carrier lifetime in the p-type material is related to the electron capture cross-section.

3.2.4. SURFACE EFFECTS

So far the development of theory depends on the assumption that semiconductor material is infinitely large. However, in real life, all the devices are fabricated on wafers and any semiconductor material should be diced. The sharp transition from solid material to a surface, for example, air, induced electrical states called surface states. The presence of those states impacts the base current density of a BJT. In this section, we address the origin of these states and investigate their recombination rate based on the SRH model discussed in subsection 3.2.3

In the SRH physics model, simple defects in the semiconductor will generate discrete energy states within the forbidden band gap. At the termination of the semiconductor, the periodic potential of the crystal lattice is disrupted. Such disruption leads to a distribution of energy states in the band gap. Figure 3.1 gives a schematic overview of the energy states.

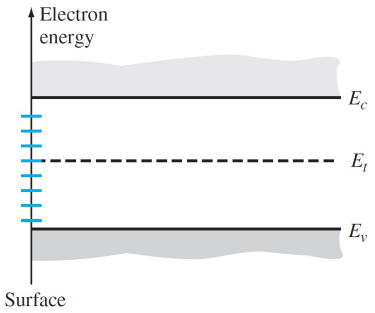


Figure 3.1: Distribution of surface state energies in the band gap, source[17]

Equation 3.26 and equation 3.25 show that excess minority carrier lifetime is inversely proportional to the density of trap states. Traps density at the surface is larger than that at the bulk. Therefore the excess minority carrier lifetime on the surface is

smaller than that in the bulk. In the case of an extrinsic n-type semiconductor, the recombination rate of the excess carrier in the bulk, according to equation 3.24 is given by:

$$R = \frac{\delta p}{\tau_{p0}} \equiv \frac{\delta p_B}{\tau_{p0}} \tag{3.27}$$

In which δp_B is the bulk concentration of excess minority holes. A similar expression for the recombination rate at the surface is given by

$$R_s = \frac{\delta p_s}{\tau_{p0s}} \tag{3.28}$$

in which δp_s is the surface excess minority carrier hole concentration and τ_{p0s} is the excess minority carrier lifetime at the surface.

If we assume that the generation rate of excessive carrier is the same throughout the semiconductor, then the recombination rate at the surface and bulk are also equal. This is because the generation rate and recombination rate are equal in equilibrium at a homogeneous semiconductor. If $\tau_{p0s} < \tau_{p0}$, then the excessive minority carrier concentration at the surface is smaller than the excessive minority carrier concentration at the bulk. In other words, $\delta_{ps} < \delta_{pB}$. There is a gradient of excessive carrier concentration from the bulk to the surface:

$$-D_p \left[\hat{n} \cdot \frac{d(\delta p)}{dx} \right] \Bigg|_{\text{surf}} = s\delta p|_{\text{surf}} \tag{3.29}$$

$\hat{n}$ is a vector perpendicular to the surface. dimensional analysis reveals that the unit of s is cm/s Hence s is claimed as surface recombination velocity. When there is no difference between the surface and bulk excess carrier concentrations, then the gradient and zero and so is the surface recombination velocity. It is an indication of the surface characteristics compared with the bulk region.

In this section physics models concerning the device's performance are covered; in the next section. Geometries in the design are also presented and discussed to investigate the potential impact on devices' characteristics.

3.3. SIMULATION RESULT

During the simulation, different parameters of the device are changed to verify impact on the device's Gummel characteristics. Those parameters are base doping, collector doping, temperature, base thickness and metallization. The writer uses those simulation as a verification to deepen his understanding of semiconductor device physics theory. Also, the simulation results provide insights into device's design.

3.3.1. GUMMEL CHARACTERISTICS

The Gummel plot depicts devices' base and collector currents versus the base emitter voltage. When different design parameters are tweaked, some unexpected phenomena happens. In this section, those phenomena are discussed with the knowledge presented in section 3.2 Figure 3.4 gives the zero device's Gummel characteristics at 300 Kelvin; further simulations reveal the conducting mechanism of the junction transistor.

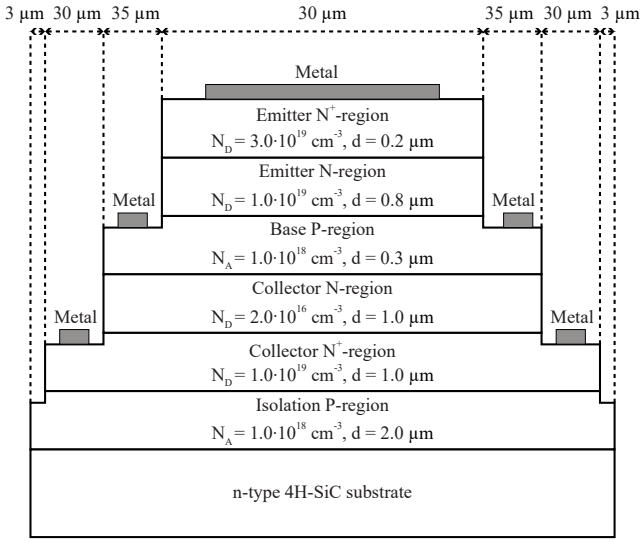


Figure 3.2: A diagram of the device

IMPACT OF BASE DOPING

As observed from figure 3.5 the base current first reduces significantly when doping increases; at extremely high doping the base current rises again. As for the collector current, it displays the same changing pattern with base doping.

As discussed in section 2.3 the collector current results from the diffusion of minority carrier concentration across the base region; if doping in the base region increases, the minority carrier concentration should decrease following the low injection assumption.

There are two components of base current: one is due to the injection of minority carrier holes in the base region under the forward bias of the base-emitter junction. Another one results from the recombination of minority electrons and holes in the base region. The recombination current is a function of both the minority carrier concentration and the carrier lifetime.

$$i_{B1} = \frac{qA_E D_p n_i^2}{N_D L_P} e^{v_{BE}/V_T} \tag{3.30}$$

The injection of holes in the emitter remains the same; but the recombination current reduces significantly.It is explained in the width of the forward biased region. The width of the forward biased region is given in equation 3.41. The width decreases with doping and hence the recombination current in the region decreases.

Meanwhile, there is this argument about the electrons from the emitter will be pushed into the base, the minority carrier increases and the recombination should increase.

However, this happens at different time. What we compared, however, is what happened at the same time instance while the doping changed. Hence it is a paradoxical

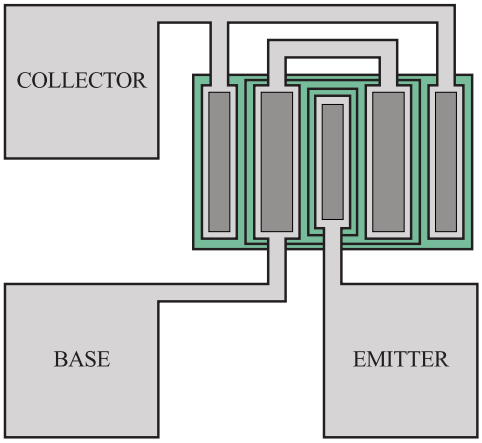


Figure 3.3: Illustration of the Mask

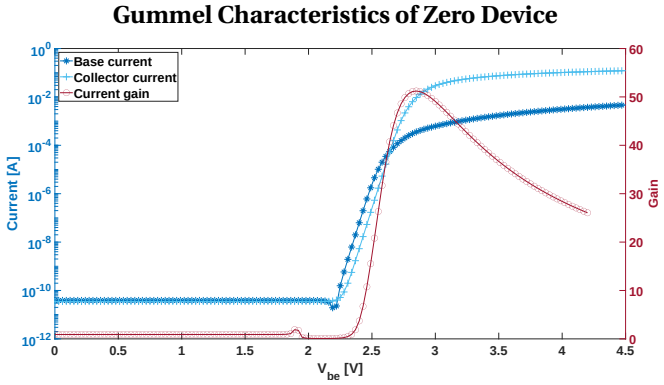


Figure 3.4: Gummel Characteristics of generation zero 300K

question. Phenomenon explained.

$$i_{B2} = \frac{qA_E W n_i}{\tau_b} e^{v_{BE}/V_T} \tag{3.31}$$

Another crossover happens when the base doping has increased significantly, in this case, the band gap narrowing discussed in section 3.2.1 has to be considered[33], [43]. When the doping and emitter increase significantly, the discrete energy levels split into an energy band. And the distance between donor atoms decreases. When the distance is so small that they interact with each other, the donor energy band widens and eventually reaches the conduction band, in this way the band gap becomes smaller.

A reduced band gap energy increases the carrier concentration. The original expression for intrinsic carrier concentration is:

$$n_i^2 = N_c N_v \cdot e^{\frac{-E_g}{kT}} \tag{3.32}$$

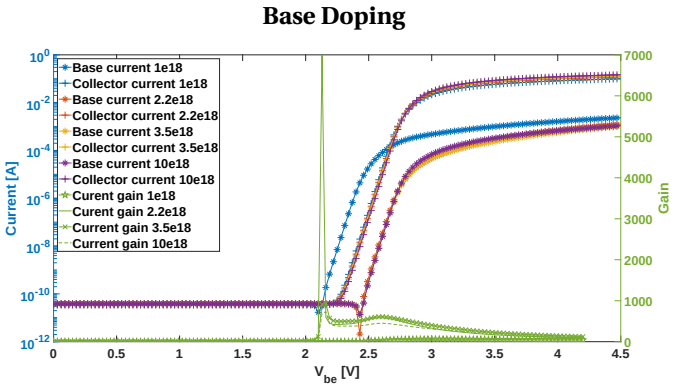


Figure 3.5: Base doping's impact on Gummel Characteristics

With the decrease of band gap ΔE_g, it becomes

$$n_{iE}^2 = N_c N_v \cdot e^{\frac{-(E_{g0}-\Delta E_g)}{kT}} = n_i^2 \cdot e^{\frac{\Delta E_g}{kT}} \tag{3.33}$$

In combination with equation 3.30 and equation 3.31, it explains the base current rising again at extreme high doping. Figure 3.6 gives an example of the impact of this effect[44].

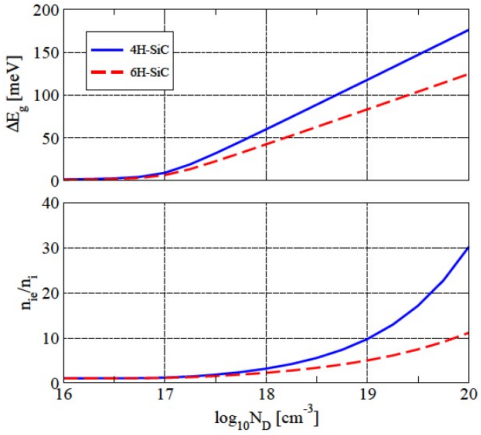


Figure 3.6: band gap narrowing in α-SiC as a function of doping, the graph on the bottom shows its effect on the intrinsic carrier concentration, source[44]

IMPACT OF COLLECTOR DOPING

In the simulation, it is discovered that the base current slightly decreases when the collector doping has increased. The behavior is explained as follows:

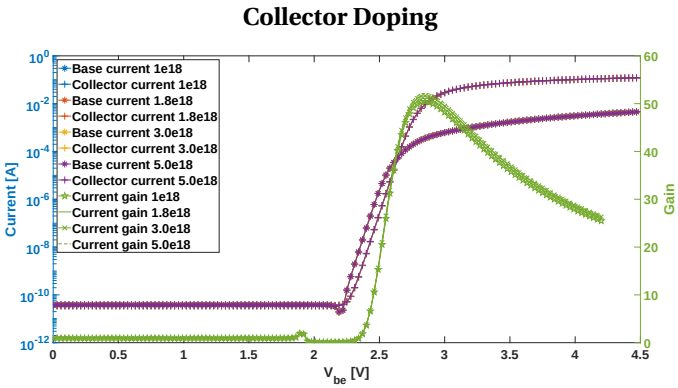


Figure 3.7: Impact of collector doping: the base current decreases slightly

The doping of the collector only impacts the base-collector junction. There are two components of base current involved with this junction: the generation current that is in the space charge region; and the ideal reverse saturation current. First, doping's impact on the generation current is analyzed. In the space charge region mobile electrons and holes don't exist, hence the electron concentration in the conduction band and hole concentration in the valence band are zero. Equation 3.21 is simplified to equation 3.34

$$R = \frac{-C_n C_p N_t n_i^2}{C_n n' + C_p p'} \tag{3.34}$$

In case the trap level lies at the intrinsic Fermi level, then n' is equal to n_i, and p' is equal to p_i. Recombination rate is further simplified as:

$$R = \frac{-n_i}{\frac{1}{N_t C_p} + \frac{1}{N_f C_n}} \tag{3.35}$$

The denominators are defined as carrier lifetimes. Hence,

$$R = \frac{-n_i}{\tau_{p0} + \tau_{n0}} \tag{3.36}$$

To simplify the equation further, a new definition is introduced as

$$\tau_0 = \frac{\tau_{p0} + \tau_{n0}}{2} \tag{3.37}$$

The recombination rate then becomes

$$R = \frac{-n_i}{2\tau_0} \equiv -G \tag{3.38}$$

A negative recombination current is a generation current; its density is the integration of the generation-rate across the reverse-biased region.

$$J_{\text{gen}} = \int_0^W eGdx \tag{3.39}$$

The result of the integration is

$$J_{\text{gen}} = \frac{en_i W}{2\tau_0} \tag{3.40}$$

In increasing the collector doping, the only changing parameter in equation 3.40 is the junction width W; the junction width of a reverse biased PN junction is:

$$W = \left\{ \frac{2\epsilon_s (V_{bi} + V_R)}{e} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2} \tag{3.41}$$

Referring to equation 3.41 and equation 3.40, the generation current will decrease upon increased base doping. Another current component, the ideal saturation current due to the diffusion of minority carriers on both sides, is given by [17]:

$$J_s = \left[\frac{eD_p p_{n0}}{L_p} + \frac{eD_n n_{p0}}{L_n} \right] \tag{3.42}$$

The n_{p0} in the collector side decreases because of the increases in carrier doping. Hence the ideal saturation current decreases significantly. When both components of the base current decrease, the sum decreases.

IMPACT OF TEMPERATURE

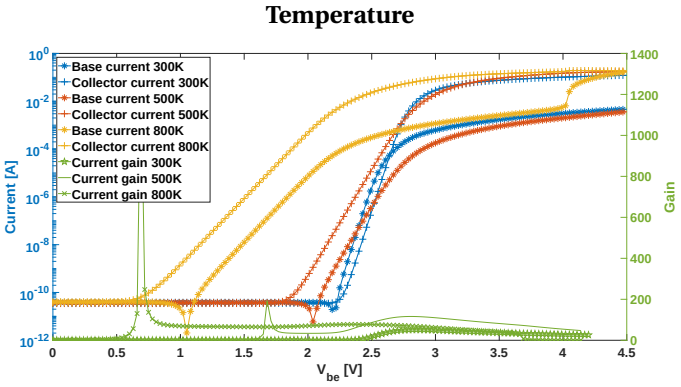


Figure 3.8: Temperature's impact on the device performance

When the temperature is applied to the simulation, there is a significant shift of conducting voltage. At higher temperature, more carriers in the valence band get activated in the conduction band and the conduction voltage hence gets smaller.

IMPACT OF BASE THICKNESS

Base thickness determines the current density of the collector current, and therefore the gain. When the thickness is low, the electrons from the emitter are pushed across the base with less recombination and hence the current grows.

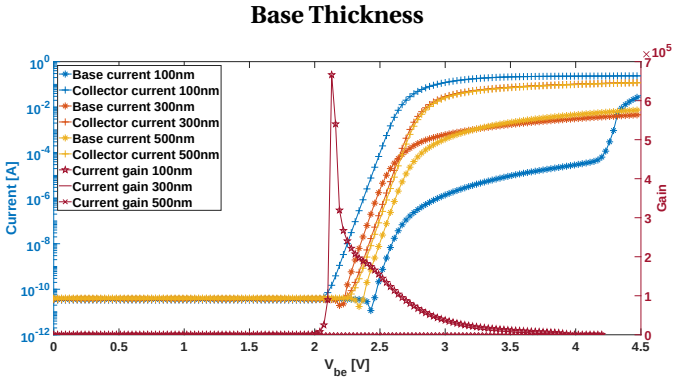


Figure 3.9: Device performance at different base thicknesses

IMPACT OF COLLECTOR THICKNESS

The thickness of the collector impacts the current density and therefore the gain. Upon increasing collector thickness, it is observed that the collector current shrinks while the base current increases.

IMPACT OF METAL POSITION

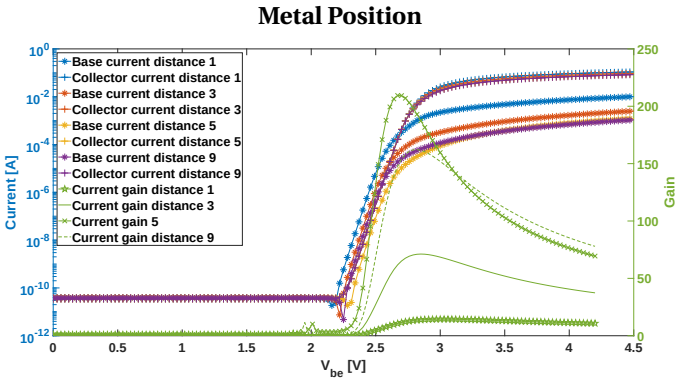


Figure 3.10: Impact of metal position

The conducting behavior changes when the metal position changes. The parameter "distance from the edge" indicates the distance between the edge of the collector Ohmic layer and the edge of the metal. When "distance from the edge" is 5, the metal lies in the middle of the collector Ohmic layer. See figure 3.11. It is discovered that when the meltallization lies in the middle of the two edges, the BJT has the highest gain of 220. In a similar research work carried out by Benedetto, it was discovered that placing the base contact very close to the emitter edge increases the base current by increasing the gradient of the electron concentration toward the base contact[45]. However, the writer attributes this experimental phenomenon to the current crowding in the collector re-

gion given that the collector Ohmic layer is thin. Electrical field distribution needs to be observed in order to verify this proposition.

Figure 3.11: Parameter"distance from the edge"

4

DEVICE FABRICATION

This chapter presents the realization of the BJT in our clean-room. During the fabrication phase there was a challenge: original vendor of epitaxial growth SiC notified that the lead time would be six months and it could not be less. The writer and his supervisors tried several vendors in Europe and they all replied that the lead time had increased to even more than 6 months. The only viable option was a vendor from china but with wafers with less high doping concentrations than what is required. This does mean that the devices will be far from ideal, will have high contact resistance, less ohmic behaviour. Moreover, the quality of the SiC is less than from the original vendor.

4.1. FABRICATION CONCEPTS

4.1.1. CHEMICAL VAPOR DEPOSITION

Chemical Vapor Deposition is an vacuum deposition method used in semiconductor industry to produce high-quality, high-performance material, it is particularly used to deposit thin films. During the deposition the substrate is exposed to one or more volatile precursors, which will decompose or react with the wafer to produce to planned product. Volatile by-products are produced during the reaction, and they get removed by gas flow in the reaction chamber. Micro-fabrication use CVD to create materials in various forms: mono-crystalline oxide, polys-crystalline oxide, amorphous one, and expitaxial one. As for carbon, there are nanotube, graphene, diamond, fibre, and nanofibre. Also, various silicon compounds are possible: silicon oxide, carbide, nitride, and oxynitride. Other materials, such as filaments, fluorocarbons,high-k dielectrics, titanium nitride, and tungsten are on the lists.

Depending on operating conditions, CVD are classified to four categories:

- Atmospheric pressue CVD (APCVD)
- Low pressure CVD (LPCVD). Undesired gas phase reactions are reduced at sub-atmospheric pressure; and the film uniformity is improved under this pressure.
- sub-atmospheric CVD.(SACVD) Different from LPCVD, ozone and tetraethly orthosilicate are used to fill high aspect ratio silicon structure with silicon oxide.
- Ultrahigh vacuum CVD.(UVCAD). CVD at very low pressure, lower than 10^{-6} Pa. It is noteworthy that in other field the division between the high and ultrahigh pressure is lower: typically 10 Pa

4.1.2. LITHOGRAPHY

Lithography is a technique that use light to pattern thin films of suitable material over a substrate. The patterned material protects the substrate under it during the succeeding implantation, etching or deposition operations.Light source of the lithography process includes ultraviolet, extreme ultraviolet, and X-rays; wavelengths of the light source determine the minimum feature size in lithography. The process can be divided into five procedures: cleaning, preparation, photo-resist application, exposure and developing. On the wafer surface there exist organic or inorganic contaminants; wet chemical treatment are applied to remove them in the cleaning procedures. There are a number of solutions available in the wet chemical treatment; for examples: methanol, acetone, or trichloroethylene, and solutions containing hydrogen peroxide.

4.1.3. REACTIVE ION ETCHING (RIE)

Reactive Ion Etching is an dry etching technique that has different characteristics than wet etching. It gives well-shaped vertical structure compared with wet etching. The whole systems sits in a cylindrical chamber. Wafer is on a plate in the bottom and gas enter the chamber through the inlets on the top. The wafer platter itself is electrically isolated from the rest of the system. Types and amount of the gas varies in different processing; sulfur hexafluoride is usually used for etching silicon. Gas pressure in the cham-

ber are maintained between a few millipascal and hundred millipascal by adjusting the gas flow rate and adjusting the exhaust valve.

Ion coupled plasma (ICP) reactive ion etching is an variant of RIE. A high frequency powered magnetic field generates the plasma. Ions of high concentration is achieved, but etching profiles are highly isotropic.

There is also the combination of ICP RIE and parallel plate RIE. ICP is applied for high density ions as to increase the etch rate; a separate bias is applied on the wafer so that the generated directional electrical fields create more un-isotropic profiles.

Deep Reactive Ion Etching (DRIE) is a special variant of RIE that creates highly un-isotropic profiles. In reactive ion etching the plasma struck the gases mixtures and change gas molecules into ions. Ions are accelerated towards the substrate and react with substrate material that will be etched; this is the chemical part of the etching process. There is also the physical part of etching: if those accelerated ions have enough kinetic energy, they directly knock atoms off the substrate. The chemical part of etching is isotropic while the physical part is directional. To achieve the unisotropic profiles, two techniques are possible

- Cryogenic Process: it cools off the wafer at -110°C and slows down the chemical process. Meanwhile the ions still bombard the substrate and create highly vertical structures. However, the disadvantage is that gases mixture tend to attach to the cold surface: electrode or substrate. Also, standard protection masks on the substrate crack under the extreme temperature

- Bosch Process: the patented production techniques prevents the isotropic chemical process with deposition of an chemical inert protection layer. For example, octafluorocyclobutane [C_4F_8] creates a chemical layer similar to Teflon. During each phase, the layer prevent further chemical reaction; meanwhile the direction ions attach the protection layer on the bottom of the trench (but not on the side). Chemical reaction hence go on only on the bottom pit. Such a phase is repeated for many times to create a highly vertical structure with small ripples on the sidewall. User can set up the cycle time to control the structure. Shorter cycle gives more vertical structure while longer cycles yield higher etch rate.

4.1.4. SCHOTTKY BARRIER

When a piece of metal and a piece of semiconductor are put together, an energy potential barrier forms at the junction region. Such an energy barrier is defined as *Schottky Barrier*. Depending on the combination of metal and semiconductor material, the barrier height is different and hence the contact may or may not have rectifying characteristics. Figure 4.1 shows the energy band diagram of n type material and a metal. Vacuum level is used as an inference; the difference between vacuum level and Fermi level of the metal is defined as metal work function Φ_m. Similarly, the difference between vacuum level and Fermi level of the semiconductor is defined as semiconductor work function Φ_s. χ is the *electron affinity*, difference between vacuum level and conduction band.

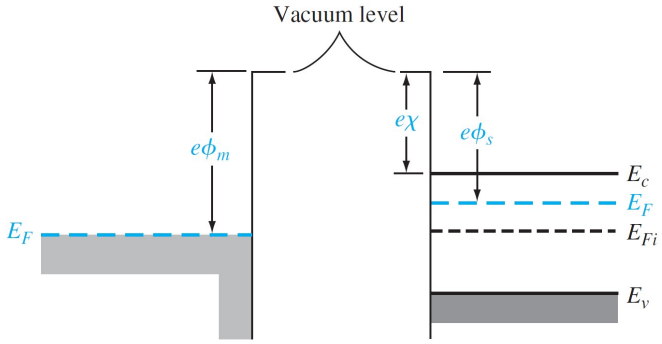


Figure 4.1: Energy band diagram of n-type semiconductor and metal; the work function of semiconductor is smaller than that of metal

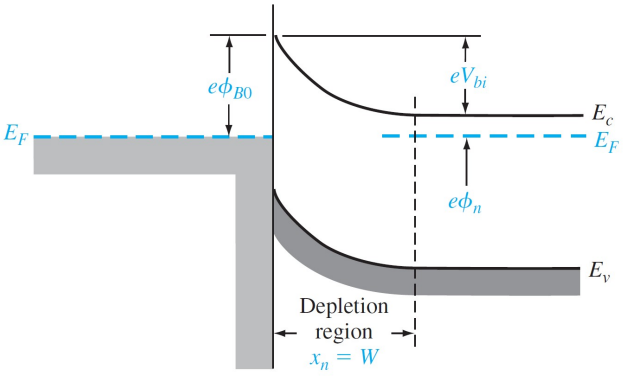


Figure 4.2: Energy band diagram of the junction at thermal equilibrium,source[17]

Upon intimate contact between the semiconductor material and metal Fermi level becomes constant throughout these two chunks. As seen in figure 4.1, electrons in the semiconductor material have a higher energy state than the ones in the metal; hence electrons will move from semiconductor to the metal, leaving positively charged donor atoms around the contact and create a space charge region. Figure 4.2 gives the energy band diagram of the junction at thermal equilibrium. Φ_{B0} is defined as *Schottky barrier*; the potential barrier for electrons in the metal to get into semiconductor.

$$\phi_{B0} = (\phi_m - \chi) \tag{4.1}$$

For an n type material, an Ohmic contact requires the following relationship:

$$\Phi_m < \Phi_s \tag{4.2}$$

when the material is n type. If the material a p type then the relationship between ϕ_m and ϕ_S should be:

$$\Phi_m > \Phi_s \tag{4.3}$$

The band gap of Silicon Carbide is expected at 3.25 eV [46]; the electron affinity is at 3.1 eV. Hence the intrinsic work function of the silicon carbide is expected at 4.83 eV. The work function of Nickle is at 5.15 eV and that of the stacked Ni/Ti/Al should be higher[47].

4.2. CRITICAL STEPS

EMITTER ETCHING

Emitter is the most critical step after zero layer. As shown in figure 3.2 Emitter layer's thickness is 1 µm,but the base thickness is only 0.3 µm. An over etching has to be performed so that metal lands on base; but meanwhile it cannot be etched so much that base layer has no contact. In the processing Rapier DRIE tool is used since its etching rate is more controllable compared with Omega Inductive Coupled Plasma Reactive Ion Etching. Only one run is performed as the wall structure of emitter does not have high aspect ratio. The cycle lasts 1075second at 0 °C . The resulting profile is measured with DekTak Profiler As show in figure 4.3,the wall structure's height is 1125 nm;an over-etch of 125nm is achieved.

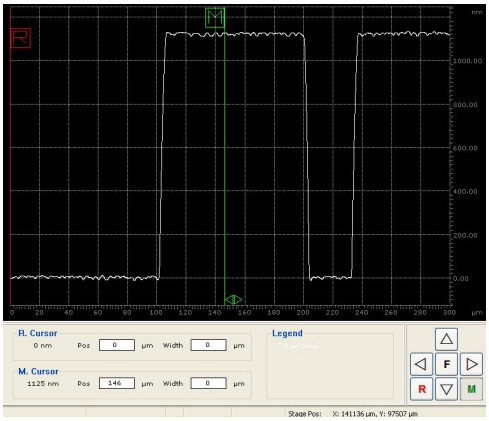


Figure 4.3: Surface profile after emitter etching

During the etching Silicon oxide is used as a mask layer covering the silicon carbide substrate. Before running the process wafer, a test wafer was used to determine the etch rate of silicon carbide and silicon oxide. Result shows that these two types of material yield similar etch rate of 1nm/s. As a cautions step: 2.5 µm PECVD silicon oxide was deposited to avoid unnecessary etching into the emitter top, which is the starting point of the processing. Oxide Deposition is performed with Novellus Concept One CVD tool at 400 °C for 35 s. Compared with thermal oxide growth in the furnace. The CVD silicon oxide has less density but meanwhile its deposition rate significantly higher. Since the etching wafer of the mask silicon oxide and silicon carbide was planned to tested, in this case the CVD silicon oxide was chosen.

METAL DEPOSITION

As discussed in subsection 4.1.4, the metal work function determines the contact's Ohmic behavior. In the literature it is stated that rapid thermal annealing (RTA) at high temperature decreases the resistance and provides better metal contact[48], [49]. Although the writer's EKL does not have the RTA capacity, it was carried out in the Kavli Nanolab. The measured I-V characteristics shows good Ohmic behavior.

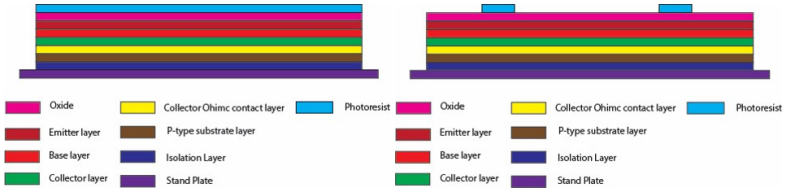
The overlay of the BJT is a stack of 300 nanometer chromium and 3 micro meter gold. Delamination of the overlay layer was discovered after overlay metal deposition in the CHA machine. This is because of the thick gold layer requires prolonged heating during gold particle generation; and such a long heating reduced the adhesion of photo resist. The deposition recipe is therefore modified to operate between 35°C and 75 °C , and instead of one-time prolonged heating the whole deposition is divided in six intervals.

SURFACE STATE IMPACTS

As discussed in subsection 3.2.3 and subsection 3.2.4, surface effects have a significant impact on the BJT's electrical characteristics. Especially in this project it plays an important role since the SiO2 passivation layer is grew on top of the epitaxial SiC wafer. The growth of SiO2 is performed with CVD technique; this brings large amount of surface states at the interface of SiC and SiO2. In the literature it is proposed that annealing in Nitrogen Dioxide (N2O) will decrease the surface state density and improve device's performance. However, the writer's clean-room does not have this capacity; and due to time limitations, the writer decided to go ahead without this step. Future work should come up with an alternative, for example in how the structures are designed, and taking this high surface effects in the device level model to improve its working without the need of this annealing step.

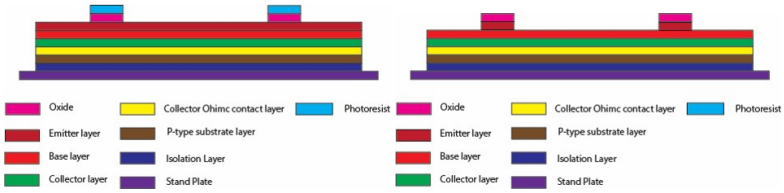
4.3. FABRICATION FLOW

As illustrated by figure 3.2, bipolar junction resistor of us has a mountain shape. High doping at different layers are not achieved in EKL but with epitaxial technology from wafer vendor. In short, the processing consists of two parts: etching and metal deposition. Etching part of the processing consists of four steps: etching of emitter, base-collector, collector-Ohmic, and mesa. Metal deposition consists of metal on the N type material, metal on the P type material, and overlay deposition. Appendix B B presents the fabrication flowchart.

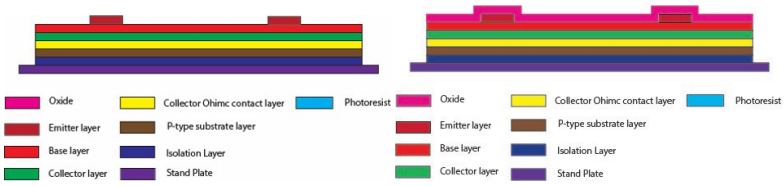


(a) Oxide and photo resist on top of wafer

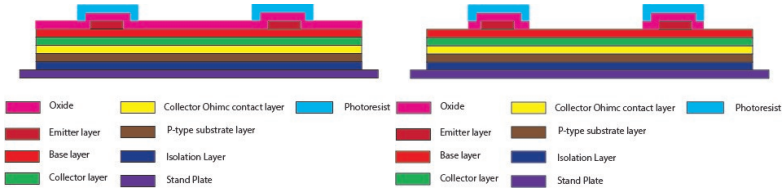
(b) After lithography



(a) Mask opening (b) Photo resist removed and DRIE



(a) Residual Oxide mask removal (b) Oxide growth for base etching



(a) Lithography of base (b) Oxide Opening for base etching

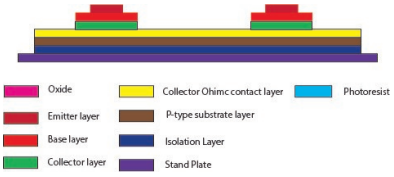
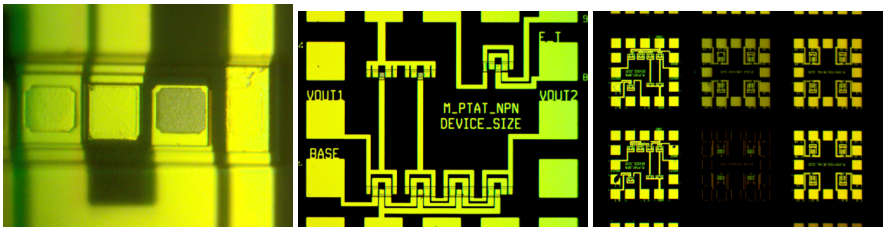


Figure 4.8: Device outlook after collector ohmic cycle

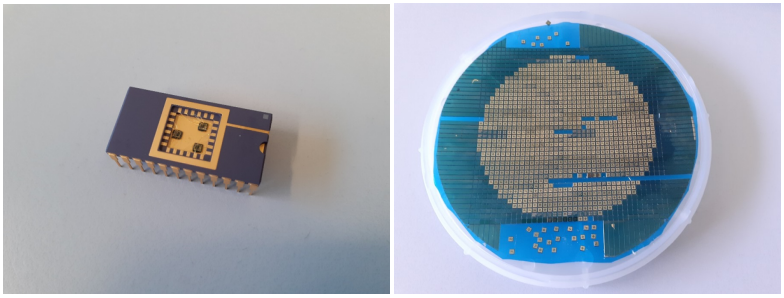
4.4. PRODUCT OVERVIEW

Outside the cleanroom the wafer is diced into dies in MEMS lab. Dies with minimal contamination and delamination are packaged. Gold is used as the bonding wire in consideration of high temperature application, and each metal pad holds three wires to improve reliability. In the future, the packaged device will be plugged into development as a demonstrator for the EU project.



(a) Wall structures of the BJT (b) One die (c) Overview of several dies

Figure 4.9: Microscope images of the wafer



(a) One packaged device (b) The diced wafer

Figure 4.10: Current product overview

5

DEVICE CHARACTERIZATION

This chapter reports characterization phase of the research. First the measurement set up is described in section 5.1. Following that performance of difference devices is presented in section 5.2. The BJT temperature sensor showed good operation up to 200℃ . One example showed a sensitivity of 1.3 mV/℃ with a R2 value of 0.9965. The test to 400℃ requires a 5-probe measurement which is not available in the writer's measurement lab. However, we did one device for single output, and this showed 0.6 mV/℃ , with a R2 value of 0.9521. As a comparison, a Schottky diode's temperature performance was characterized; its sensitivity is 4.8 mV/℃ , the R2 value is 0.9963. Performance of the fabricated PNP devices is good.

5.1. MEASUREMENT SETUP

As stated in the problem formulation, the goal of this project is to develop a temperature sensor with measurement range up to 400 Degree Celsius. Such a high temperature demands test set up of high thermal tolerance. In this research work, microbe probe station (MPS) bought from NEXTRON is used as the testing platform. It consists of four micro-probes, a hotplate and a pressure chamber. The hotplate has a temperature range up to 750 °C , it is the heating source for the sensor. Four micro-probes are interfaced to Keithley source meter, which applies electrical citation.

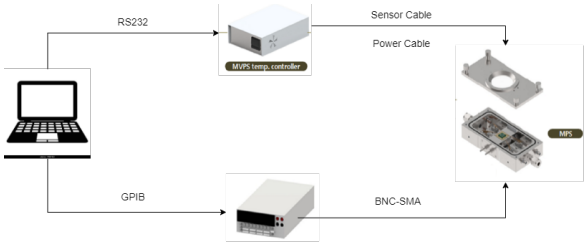
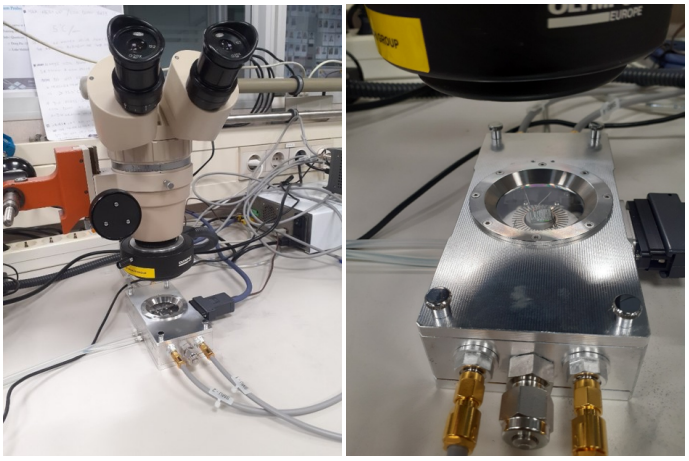


Figure 5.1: Diagram for diode temperature sensor's measurement

Control of temperature is achieved with the MVPS temperature controller connected to operation PC. Temperature profiles are input from the writer; electrical citation are applied during plateaus of temperature rising. Collected electrical output in regard to temperature is plotted to verify the temperature sensor's linearity. Figure 5.1 sketches the set up. Since the die's size is 1.5 mm, a microscope is needed to place the micro-probe on the die's metal pads.



(a) Microscope (b) NEXTRON MPS

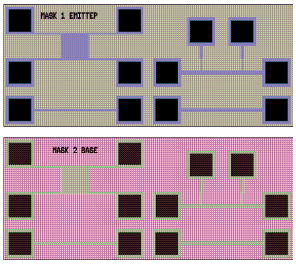
Figure 5.2: Measurement set up

(a) Keithley source meter (b) Cascade 33 probe station

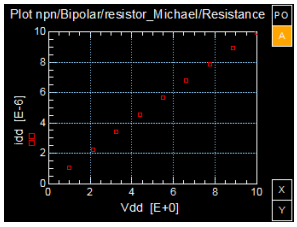
Figure 5.3: Equipment used in device characterization

5.2. MEASUREMENT RESULT

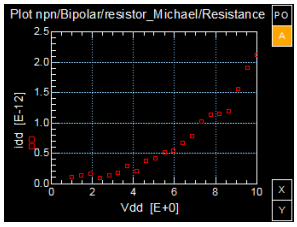
As discussed in chapter 4, the doping specifications from the vendor is not per required. Hence the ohmic behavior of P layer and that of N layer are tested with cascade probe station, see figure 5.4. In the vendor's report the doping of the emitter ohmic layer is



(a) Test structure of the contacts



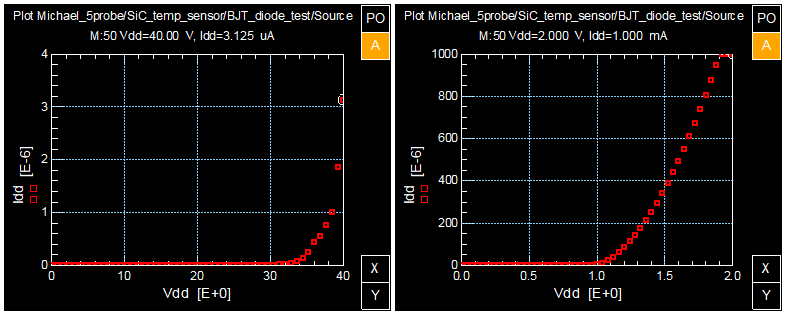
(b) I-V curve of P type contact, ohmic behavior observed



(c) I-V curve of N type contact, schottky behavior observed

Figure 5.4: Ohmic test of the contacts

10^{18} $1/cm^3$ instead of 3×10^{19} $1/cm^3$. Such a low doping results in the schottky barrier behavior. After verification of ohmic resistance, the two diodes of the NPN BJT are tested separately, they both work but for the high conduction voltage at in the base collector diode. The reasoning is that the high doping at the emitter creates the schottky diode behavior between emitter metal and emitter.



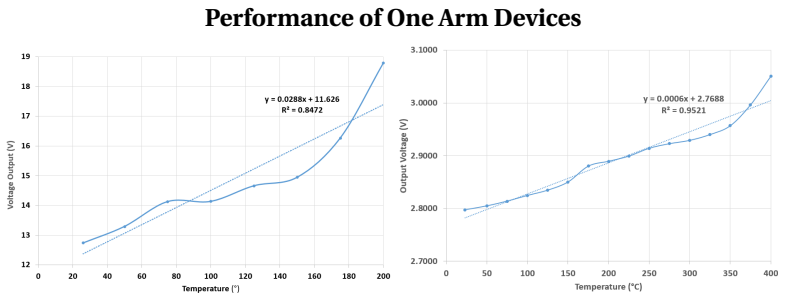
(a) Base emitter diode conducting behavior (b) Base collector diode conducting behavior

Figure 5.5: Conduction of the two diodes inside the BJT

With the test and ohmic contact and PN diodes ready, the writer conducted the temperature tests of the fabricated sensors. Their performance is presented in figure 5.7 and 5.6. Table 5.1 gives a summary.

Table 5.1: Overview of Devices' Performance

Devices	Linearity (R2)	Sensitivity (mV/°C)	Range (°C)
One arm NPN	0.8472	28.8	200
One arm PNP	0.9521	0.6	400
Differential PNP	0.9965	1.3	200
Reference Diode	0.9963	4.8	400

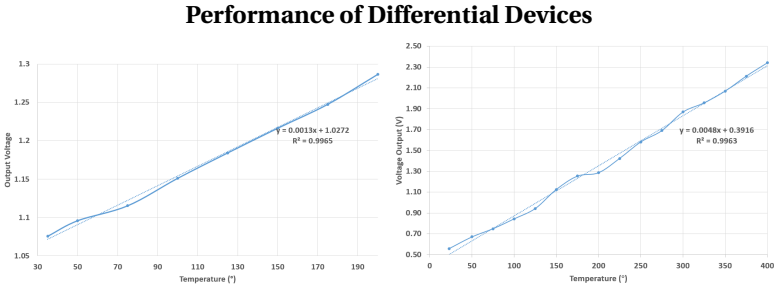


(a) One arm NPN device. R2 value: 0.8472
Sensitivity: 28.8 mV/°C Range: 200°C

(b) One arm PNP device. R2 value: 0.9521
Sensitivity: 0.6 mV/°C Range: 400°C

Figure 5.6: One arm devices' Performance

Figure 5.7b gives the radiometric output voltage of the Schottky diode sensor for reference purpose. The biasing currents for those two diode branches are 1 mA and 5 mA respectively. The sensitivity is 4.8 mV/°C, and the R^2 value for linear regression analysis is 0.9963.



(a) Differential PNP device. R2 value: 0.9965 Sensitivity: 1.3 mV°C Range: 200°C

(b) Schottky diode. R2 value:0.9963 Sensitivity: 4.8 mV°C Range: 400°C

Figure 5.7: Temperature sensors' performance

Compared with the reference device, Different PNP sensor in figure 5.7a has higher linearity. The limited range is because of the absence of 5-probe measurement station at high temperature. One arm NPN device's relative poor linearity is a result of the schottky diode barrier at the emitter. At higher temperature the intrinsic carrier concentration increase significantly; therefore the voltage increases dramatically at temperature higher than 180 °C . The one arm PNP sensor's sensitivity and linearity are worse than the differential one, although its measurement range is up to 400 °C .

6

CONCLUSION AND FUTURE WORK

This chapter reviews the research objectives proposed in the introduction. In section 6.2 recommendations for future research are presented.

6.1. CONCLUSION

The objectives of this thesis work were: 1) developing a BJT device level model, based on SiC epitaxial structures; 2) Introduce the SiC epitaxial based BJT technology to writer's clean-room; and 3) Fabricate a working BJT based PTAT temperature sensor.

The first Objective was achieved by using TCAD Sentaurus in combination with various existing models of the various physics involved. One of the BJT examples developed gives the highest beta of 209 at 8 V collector bias, and 10.5 uA base bias. Here, mainly the surface effects show that that the beta is significantly reduced with an increase in surface states. This effect can be reduced by annealing, and careful fabrication, e.g. cleaning and damage removal after etching.

The second objective was achieved in the EKL lab. Here first wafers were obtained from an external vendor, although with specifications which are not as required. The etching of the thin epitaxial structures was carefully developed, along with a high topography. Next to that, ohmic contacts were achieved by using different metalization schemes, and post RTA annealing in different ambient gasses and temperatures. The used metallization for the n-type is Ni, annealed in N2 ambient at 950°C . After this, the p-type metalization was done, with a stack of Ni/Ti/Al, annealed in three steps in Ar ambient at 800°C . Here, we used test structures, and these showed good ohmic behaviour. In the fabrication, the challenges were the etching, ohmic contacts, and final metallisation. The latter had to to do with delamination because of the thick metal required, due to the large topography. This was solved by changing metal schemes, and keeping the deposition temperature within a temperature range of 35-75°C . The latter is achieved by interval depositions instead of one prolonged deposition.

The third objective, was to develop a working BJT based temperature sensor. This was also achieved, although not as ideal as was initially aimed for. This was due to the specifications of the used wafers. As stated in Chapter 4, the issues with obtaining wafers with the required specifications has a long lead time than what the project duration allows for. Despite this, the BJT temperature sensor showed good operation up to 200°C . One example of the devices showed a sensitivity of 1.3 mV/°C with a R2 value of 0.9965. The test to 400°C requires a 5-probe measurement which is not available in our measurement lab. However, we did measure one device for single output, and this showed 0.6 mV/°C , with a R2 value of 0.9521. In Future work, for the demonstrator in a EU project, the device will be used with a development board, hence the temperature will be measured up to 400°C . Next to this, we also compared this work with a diode based PTAT temperature sensor, a sub-objective of this work. It has a sensitivity of 4.8 mV/°C , and an R2 value of 0.9963. Both devices have a reasonable linearity.

6.2. FUTURE WORK

In the simulation phase of the research it is discovered that metal position of BJT changes its Gummel characteristics: metal deposited between the edge of collector ohmic layer and that of collector layer gives the device the highest current gain. Such a discovery remains to be validated by data collected from fabricated device. Further investigation might result in discovery in SiC semiconductor physics theory.

Also, the developed BJT's characteristics remain to be further tested. Characteriza-

tion data can be used to develop spice model of this processing technology. Those models provide the foundation for further SiC electronics' system level design. Moreover, physics models in the TCAD simulation can be verified and calibrated with the characterization data from the fabricated device.

What is more, the sensor's reliability is not verified. In the future it should be placed inside an industrial oven and undergo prolonged thermal cycles to confirm its lifetime.

For the fabrication, future work will involve using wafers with the right specifications. Next to this, reducing surface states will also be investigated using the simulations on how to improve the devices without requiring the post-annealing steps after passivation.

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A

APPENDIX A

This appendix presents the working paper to be submitted.

A High sensitivity 4H-SiC temperature sensor based on an array of Schottky diodes

Brahim el Mansouri, Chengshang Yuan, Henk van Zeijl, G.Q. Zhang

Abstract

Applications such as oil and gas exploration, geothermal energy sources, health monitoring in aircraft engines, and industrial processes require sensors and electronics to operate in extremely high temperatures, typically beyond 500 ºC where silicon technology is not adequate. Therefore, in this paper we propose a temperature sensor based on an array of Schottky diodes, to achieve a sensitivity with minimum non-linearity. The forward bias characteristics of the devices were obtained by sweeping the bias voltage from 0 to 5 V. The temperature measurements were carried out at intervals of 10 degC while biasing in each case two individual diodes in the array to obtain a proportional to absolute temperature (PTAT) voltage. All the measurements were done with respect of the center diode. This method allowed for the highest sensitivity of ~16.53mV/ºC for four diode measurements in the range of 30 to 200 ºC. The non-linearity error was …. The ideality factor and series resistance of an individual diode are about …and …, respectively. By lumping several diodes in parallel, the series resistance can be reduced, which in turn reduces the nonlinearity at higher temperatures where the series resistance voltage drop is significant. Lumping five devices resulted in a series resistance of ~…Ω. The PTAT voltage is then obtained for two lumps of diodes giving an improved sensitivity of ~… mV/ºC, and an error in linearity of …. The temperature sensor showed good repeatability after measuring several times during various days.

Introduction

Sensors based on 4H-SiC have the advantage of operating at high temperatures, while offering the possibility of monolithic integration with SiC electronics for signal processing […]. Silicon based sensors have been developed but don't operate at higher temperatures due to the extrinsic and intrinsic carrier concentrations approaching one another, making them unsuitable for temperatures exceeding 130 ºC […]. Furthermore, leakage current increases with temperature. Other harsh environments such as radiative conditions, tend to degrade silicon devices over time […]. SiC devices are able to operate at high temperatures thanks to their wide bandgap while being chemically highly stable […]. Diodes are commonly used as the basis of temperature sensors thanks to technological maturity and ease of fabrication […].

In this paper we present a highly linear temperature sensor based on an array of Schottky diodes integrated on a single chip. To best of knowledge, this is the first device based on an array to increase the linearity a temperature sensor with a PTAT output voltage.

Two types of devices can be used, 1) pn junction based, and 2) Schottky contact based. SiC pn diodes have been shown to operate at temperatures well above 600 ºC thanks to their …[…]. Moreover, the pin diode has a lower saturation current as compared to their Schottky counterparts, allowing for higher linearity at a wider temperature range […]. However, pin diodes show a lower sensitivity because of … […]. Moreover, the non-linearity w.r.t. the saturation current in the single Schottky devices can be reduced to obtain improved linearity while a higher sensitivity is maintained […]. To further increase this effect, an array of Schottky diodes can be used to reduce the series resistance, hence an improved linearity at higher temperatures. This work focused on using an array of diodes to obtained a highly linear PTAT voltage.

First, the IV forward characteristics of the diodes is used to calculate the ideality factor and series resistance using Cheung's method […]. Here we also determine the bias current condition. Second, the forward characteristics (IV-T) at intervals of 10 oC in

a range of 30 to 200 oC are obtained for pairs of single and parallel diodes. The thermal plot is obtained from these measurements where the sensitivity was extracted from. Next to this, multiple pairs of devices are also used to see the effect on the linearity. Lastly, annealed devices are investigated to see the effect on the diode parameters and how this affects the IV-T characteristics.

Device realization

Figure 1 shows the cross section of the fabricated diode array. The diodes were fabricated on a highly doped $325\,\mu m$ thick 4^o off axis n-type 4H-SiC substrate with a resistivity of $0.0216\,\Omega \cdot cm$. For the device, three epitaxial layers were used where the first is a buffer layer, the second is for ohmic contacting, and the third is for the Schottky contact. The layers have a thickness/doping of $0.5\,\mu m/1 \cdot 10^{18} cm^{-3}$, $1\,\mu m/1 \cdot 10^{19} cm^{-3}$, and $5\,\mu m/1 \cdot 10^{14} cm^{-3}$, respectively.

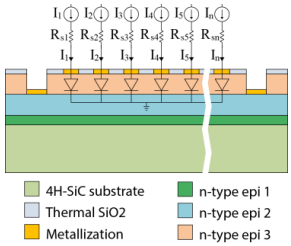

Figure 1: Cross section of the 4H-SiC Schottky barrier diode array.

The fabrication of the devices started with a standard cleaning. Lithography was to form the device pattern for the etch and deposition steps. First a reactive ion etching (RIE) step was done to open contact windows to the highly doped layer. A thin silicon oxide was thermally grown followed by a PECVD SiO_2 deposition to passivate the device. Another etching step was done to open contact windows to the epi layers. The contact openings were done using wet etching to reduce any surface damage. Finally metallization was done using sputtering of a thin Mo layer to form $180x180\,\mu m^2$ Schottky contacts, followed by an evaporation step of Cr/Au $(15/150\,nm)$ to form the overlay of the devices. Figure 2 shows the fabricated device. The anode contacts are the middle pads while one general cathode is used at the perimeter of the device.

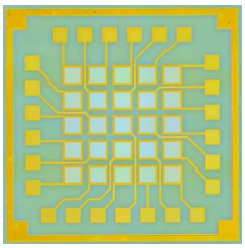

Figure 2: Image of the fabricated 4H-SiC Schottky barrier diode array.

Experimental Results and Discussions

The current transport in Schottky diodes is based on thermionic emission (TE) theory, which is expressed as

$$I_D = I_S \exp\left(\frac{V_D - R_S I_D}{\eta V_{Th}}\right) \quad (1)$$

With

$$I_S = AA^{**}T^2 \exp\left(-\frac{\emptyset_B}{V_{TH}}\right) \quad and \quad V_{Th} = \frac{kT}{q} \quad (2)$$

Where I_S is the saturation current, V_{Th} is the thermal voltage, A is the diode area, A^{**} is the Richardson constant, $\emptyset_B$ is the Schottky barrier height. Taking the series resistance into account, the voltage drop across a forward biased diode is expressed as

$$V_D = V_{TH}\eta \ln\left(\frac{I_D}{I_S}\right) + R_S I_D \quad (3)$$

Where η is the ideality factor and R_S is the parasitic series resistance.

As can be seen from the equations, single diodes have a voltage drop which is proportional to temperature, either by the thermal voltage, or the saturation current. Aside from these two, the ideality factor and series resistance are also a function of temperature […]. The thermal voltage is the only parameter changing linearly with temperature. The ideality factor nonlinearity can be solved by using higher biasing currents, whereas for the series resistance, the opposite is true […]. To obtain a linear diode voltage drop, the proposed solution is to use higher biasing

currents to avoid the nonlinearity of the ideality factor and pair of diodes to obtain a PTAT voltage, independent of the saturation current. The series resistance nonlinearity at higher temperatures can be reduced by using lumped parallel diodes.

First, to determine the biasing currents, the IV characteristics of a single diode was determined for the temperature range of interest. The IV-T characteristics were measured using a probestation in combination with thermal heating of the chuck, and connected to a B1500A Semiconductor Analyzer from Keysight. The DC sweep was done for the range of 0 to 3 V in steps of 1 mV for the temperature range between 30 and 200 ℃ in steps of 10 ℃. For the range of 200 ℃ to 500 ℃, a Keithley … was used Figure … shows this.

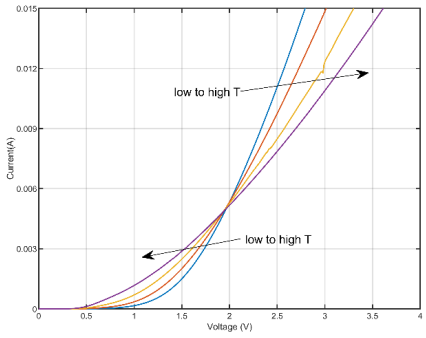

Figure 3: Forward IC characteristics of a single diode for low to high temperatures. This illustrates how to select the biasing current for maximizing the sensitivity.

From Figure3 it shows that the IV crossing point is at 5 mA. The diode voltage drop below this value decreases with temperature, while it increases for biasing above the crossing point. This means that the PTAT voltage can be maximized by choosing the biasing currents at the extremes with respect to the crossing point. Hence, the sensitivity is then maximized […]. Looking at the single diodes, Figure … shows the IV characteristics of some of the diodes from the array. Its shows that the diodes have nearly the same IV characteristics, which is to be expected as the devices are on the same substrate, fabricated using the same materials and steps. Therefore we assume that the diode parameters are similar.

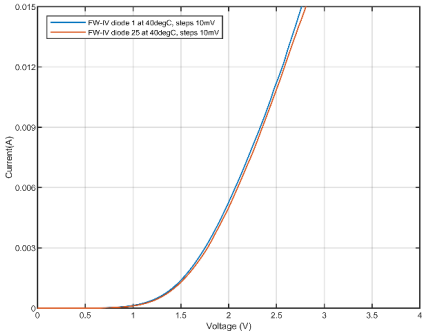

Figure 4: Forward IC characteristics of two diodes. The IV response is nearly similar.

……
……
add here the forward characteristics. We used these to extract the series resistance and ideality factors of the diodes. This measurements need to be redone

In our experiment, the diodes have nearly identical IV characteristics, which is to be expected since the diodes were fabricated on the same substrate using the same materials and steps. This is shown in Figure ….

Place holder

The ideality factor series resistance at different temperatures were obtained using Cheung's method […].
……
……

To obtain the PTAT voltage, two diode voltage drops are to be subtracted from one another, hence the non-linearity arising from the saturation current can be removed. This difference is according to equation

$$V_O = V_{D2} - V_{D1} = V_{TH}\eta \ln\left(\frac{I_{D2}}{I_{D1}}\right) + R_S(I_{D2} - I_{D1}) \quad (4)$$

The series resistance current product at low temperatures is negligible and the ideality factor is nearly constant. By controlling the current ratio Id2/Id1, the sensitivity can be made very high […]. However, this would also affect the series resistance current product, giving rise to a non-linear output.

To properly select the biasing current ratio, the determination (R^2) was used to evaluate the linearity and sensitivity were R^2 should be close to 1 […]. Figure … shows the R^2 as function of the current ratio as well as the sensitivity.

Figure ….: …

As can be seen, the best sensitivity at the highest degree of linearity is achieved for the current ratio $r = \cdots$ … where $R^2 = \cdots$ and $I_{D1} = \cdots\ mA$. The corresponding sensitivity is $S = \cdots\ mV/℃$ … mV/°C with an error in linearity of … The error is shown in Figure ….

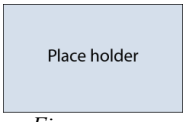

Figure ….: …

Figure … shows the VT curve for different current ratios for a high R^2.

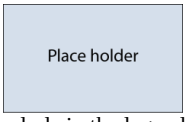

Figure ….: … include in the legend for each curve what the R^2 is

As can be seen, the devices show a high degree of linearity. The best tradeoff between sensitivity and linearity is in the range of …. An additional constraint for selecting a current ratio is power consumption. …

As an observation, R_s gives rise to is nonlinearity at higher temperatures, as for higher biasing currents, where its voltage component becomes significant […]. On the other side of the curve for lower currents, lower R^2 is caused by nonlinear behavior of η. This sets a tradeoff constraint on the current ratio. When measuring temperatures > 200 ℃, non-linearity increases due to R_s again. To reduce the non-linearity at higher temperatures without having to sacrifice linearity at lower current ratios, more diodes in the array could be lumped together to reduce R_s. This is an effective method of scaling the diode area, hence reducing the resistance. This is illustrated in Figure ….

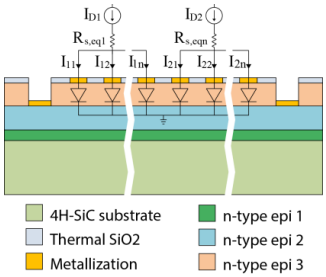

Figure ….: Illustration of diodes lumped together to reduce the series resistance.

Since the diodes are in in parallel, the voltage difference is then according to

$$V_O = V_{D2} - V_{D1} = V_{TH}\eta \ln\left(\frac{I_{2n}}{I_{1n}}\right) + R_{seq}(I_{D2} - I_{D1}) \quad (5)$$

The nonlinearity at higher temperatures is then dependent on the number of parallel diodes in each branch. Figure … shows the PTAT voltages as a function of temperature. As can be seen, the linearity increases for lumped diodes when compared to a two diode measurement. Each branch is composed of … diodes. R_S has been calculated using Cheung's method […]. This was done for a single diode and two lumped diodes giving values of … Ω and … Ω, respectively.

……

Using averaging over the entire die reduces the error which increases the reliability of the voltage output. This was also repeated for different days and showed nearly identical characteristics.

The sensor can be used according to the circuit shown in Figure …. Two IC devices are required to bias and to take the voltage differences to produce a highly linear PTAT output voltage with a high sensitivity.

Figure …: …

The devices which have been used so far are as deposited. To see the effect of post-thermal annealing, several devices were annealed at $650\,℃$ and $800\,℃$ for at N_2H_2 ambient for $1\,hour$. Additionally, rapid thermal annealing (RTA) was done at $850\,℃$ for three minutes at N_2 ambient. Figure … shows the IV characteristics of single diodes for each annealing step.

Figure …: …

As can be seen… The calculated R_s and η for each step are listed in Table 1.

Table 1: …

Annealing conditions	R_s [Ω]	η
As deposited		
$650\,℃$ at N_2H_2 ambient for $1\,hour$		
$800\,℃$ at N_2H_2 ambient for $1\,hour$		
$850\,℃$ at N_2 ambient for $3\,minutes$ (RTA)		

The series resistance … while the ideality factor …. Figure … shows the temperature behavior in a single pair for each of the annealing steps.

Figure …: …

As can be see…

Conclusion

A highly sensitive and highly linear temperature sensor for high temperature applications was fabricated and characterized. The device was fabricated using a 4H-SiC substrate with epitaxial layers to define the array of Schottky diodes. The characterization was done for a temperature range of 30 to 700 ºC and showed high linearity (R^2 = …) and high sensitivity (S = … mV/ºC). Furthermore, the device showed good repeatability and its output is even more reliable thanks to the averaging possibility. … Lumped diodes …. The wide range of operation combined with the high sensitivity makes it very attractive for industrial applications.

Acknowledgment

This work is supported by the staff at the ECTM group and the cleanroom. The EU funding …

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B

Appendix B

This appendix presents the flowchart.

4H-SiC BJT devices for temperature sensors

Flow chart

Version
01 July 2022
Michaël C. Shang

Run number: ……
Process engineer: Brahim el Mansouri
Start: 01 July 2022
Contamination: Yes, after contacts stage
Labs: CR100, CR10000, MEMS

EKL(Else Kooi Laboratory)
DELFT UNIVERSITY OF TECHNOLOGY
Address : Feldmannweg 17, 2628 CT Delft, The
P.O. Box : 5053, 2600 GB Delft, The Netherlands
Phone : : +31 - (0)15 - 2783868
Fax : : +31 - (0)15 - 2622163
Website : http://ekl.tudelft.nl/EKL/Home.php

Detailed information about possible contamination:

Place/Clean Rooms used in process:

- **Write the sequence of used labs from start to finish.**
- **Which (Non-standard) materials or process steps**
- **What kind of process or machine was used?**
- **The other materials that wafers contain that are also processed on this machine**

Lab/Clean room	(Non-standard) material/ process steps	Process/Machine/	Other materials used in machine
CR100	Red metals: Ni	Trikon Sigma (or CHA Evaporator in CR10000)	
CR10000	Red metal: Ni, Cr/Au	CHA Evaporator	
CR10000	NMP lift-off	At wet bench (new lines)	
CR1000	Yes, Cr/Au	CHA Evaporator	Cr, Au, Ta, Pt

If other labs are used:

- Write the steps number: Possible contamination issues/materials.

  Kavli ab will be used. Here we have a Rapid Thermal Annealing (RTA) step after each deposition of Ni. The contamination is from our own lab after Ni deposition.

If there are non-standard processing steps in a standard process:

- Write down the steps number, the material and machine that is used.

STARTING MATERIAL

Use **single side polished process wafers**, with the following specifications:

Type:	4H-SiC n-type
Orientation:	1-0-0, 0 deg off orientation
Resistivity:	0.021 Ωcm
Thickness:	356 μm
Diameter:	100.0 ± 0.2 mm

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure. Wafers taken out of an unopened wafer box do not have to be cleaned before processing.

1. PRE-PROCESS STEPS

Location: (Class 100 clean room)

Si+ cleaning	This is required for wafers from outside. Only allowed if there are no steps performed on the wafer which could be contaminating.
Rs	Sheet resistance measurement to verify the silicon and carbon sides of the SiC wafer. Do a quick cleaning step after this to prevent any particles from sticking on the wafer.
BS Al	Backside aluminium deposition. This is needed for optical detection of the wafers in the processing machines (SiC wafers are transparent). Use a ccarrier wafer to process in Trikon Sigma. An Al(1%) or Al layer of 1um is sufficient. Deposit at lower temperatures, e.g. 50degC.

2. FS COATING– SPR3012 – zero layer

Location: (Class 100 clean room)

Use the EVG120 system to coat the wafers with **(1.4µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **SPR3012 positive resist**, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program **"C0 – 3012 – zero layer"** on the coating station

Note: Possibly the machine still requires manual HMDS and no EBR. In this case do a 10min HMDS step, and use the appropriate recipes.

3. FS EXPOSURE ASM PAS 5500 – Use jobs for exposing stepper and contact aligner markers

Location: (Class 100 clean room)

Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

First exposure is for zero layer to be used for stepper without developing!!!

Expose the wafer using the appropriate job. **This is in the job manual of the stepper. Do the exposure with an energy of 120mJ/cm^2 and focus 0.**

4. FS Dev - Single puddle

Location: (Class 100 clean room)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.

Use program **"Dev_SP"** on the developer station.

5. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

6. FS DRY ETCHING: SIC_3mu

Location: (Class 100 clean room)

Use the Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.

Use sequence **SIC_3mu** (with a platen temperature set to **25 °C**) to etch 120 nm deep structures into the SiC.

Note: this recipe is used to etch 3 µm deep which means that the time constant needs to be changed. Only etch 120 nm deep URKs otherwise the stepper may not detect them if the reflection peak is off target. Change the time constant back to its original value after etching is done.

7. Resist stripping: TEPLA Program 1

Location: (Class 100 clean room)

Plasmastrip — Use the Tepla plasma system to remove the photo resist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.

Use program 1

8. CLEANING PROCEDURE: HNO3 100% (metal)

Location: (Class 100 clean room)

Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger "rinser/dryer" (metal) with the standard program.
Note:	No 65% HNO3 cleaning step!

9. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Emitter layer etching process

10. Hard mask: PECVD SiO2 hard mask deposition in Novellus – deposit required value

Location: (Class 100 clean room)

Use the Novellus Concept 1 for required thickness (~1nm/sec etch rate, so about 1um for each 1um etched in SiC plus 50% more for insurance) SiO2 deposition
Check Gases. Follow the operating instructions from the manual when using this machine.

Use recipe: .xxxSiOstd to deposit the required SiO2 thickness. Change time according to logbook.

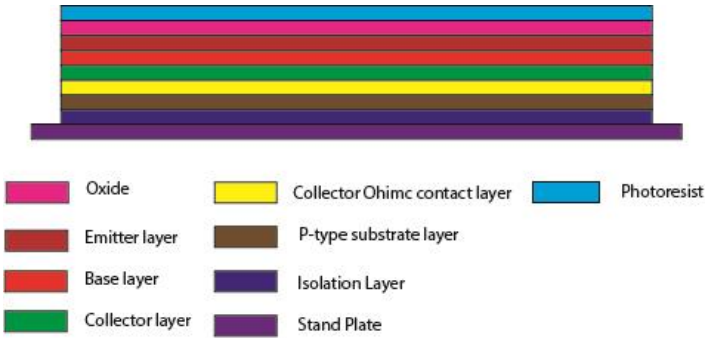
Note: If photoresist is applicable, then the hard mask is not needed.

Note: Use a Si test wafer for deposited SiO2 layer thickness measurement.

11. FS COATING– POSITIVE PHOTORESIST – Mask 1: emitter layer

Location: (Class 100 clean room)

Use the EVG120 system to coat the wafers with **(1.4µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **SPR3012 positive resist**, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.



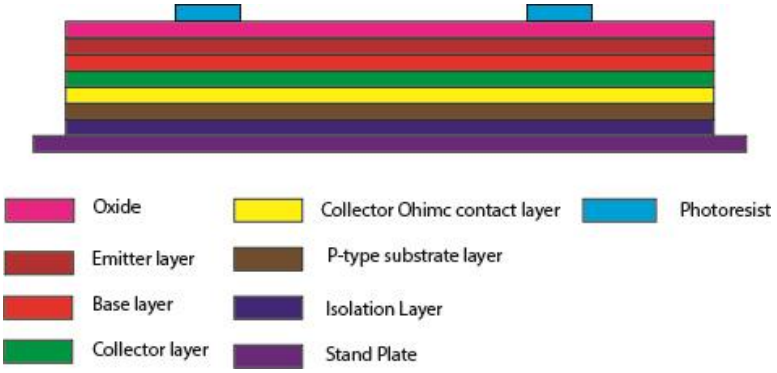
12. FS EXPOSURE CONTACT ALIGNER – Mask 1: emitter layer

Location: (Class 1000 clean room)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 1 emitter layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. This should be ~8-10sec



13. FS Dev – Single puddle

Location: (Class 100 clean room)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Dev-SP "**

14. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Inspect Measure step height with the surface profiler. Note this value to compare with the step height after SiO2 etch process.

15. EMITTER LAYER DEFINITION IN SIO2 HARD MASK FOR RAPIER ETCHING – WET ETCHING

Location: (Class 100 clean room)

BHF Emitter layer definition in the SiO2 hard mask using BHF.

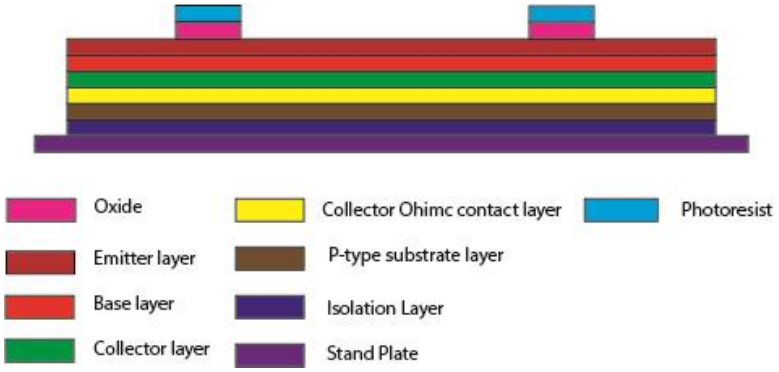
See etch rates BHF in etch manual on the wall next to wet benches and do 20 seconds of overetch to make sure no SiO2 residues remain.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the manual dryer.

Inspect Check under the microscope. Measure step height with the surface profiler.

Note: Remove photoresist and do the standard cleaning if the hard mask is used.



16. INSPECTION: SIO2 HARD MASK OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects. Additionally, measure with DekTak surface profiler to see if the expected value has been obtained. Compare with the previously measured values for the deposited SiO2 hard mask and photoresist coating.

17. Resist stripping: TEPLA Program 1

Location: (Class 100 clean room)

Plasmastrip — Use the Tepla plasma system to remove the photo resist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.

Use program 1

18. CLEANING PROCEDURE: HNO3 100% (metal)

Location: (Class 100 clean room)

Cleaning — 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.

QDR — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying — Use the Avenger "rinser/dryer" (metal) with the standard program.

Note: — No 65% HNO3 cleaning step!

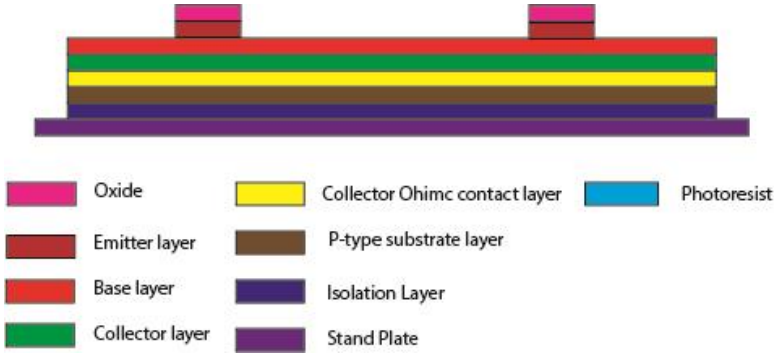
19. EMITTER LAYER DEFINITION ON THE 4H-SIC WAFER – RAPIER

Location: (Class 100 clean room)

Dry etch — Emitter layer etching in SiC epitaxial layer.

Use recipes of Brahim optimized for 4H-SiC. Selectivity is less than 1 for SiO2.

Inspect — Measure step height with the DekTak surface profiler. Ensure more than the functional layer thickness has been etched. The overetch should be approximately 50nm, thus 50seconds of overetch. Use the etch rate value of SiO2 and 4H-SiC to calculate the new etched structure. ETCH MORE IF NEEDED.

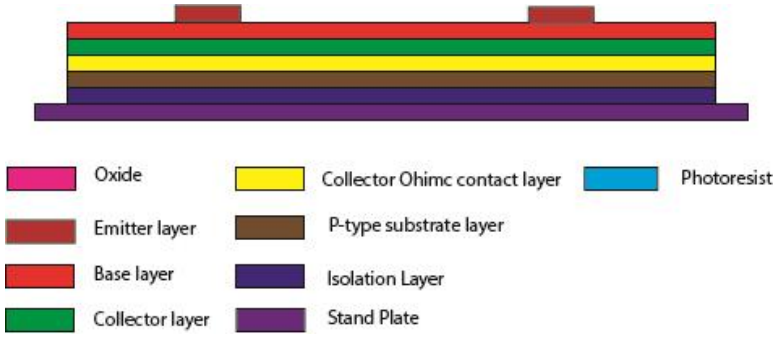


20. SIO2 HARD MASK REMOVAL – WET ETCHING

Location: (Class 100 clean room)

BHF	SiO2 hard mask removal using BHF. See etch rates BHF and do 3min of overetch to make sure no SiO2 residues remain.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.

Note: The aluminium BS layer also gets etched in the BHF solution. If the layer is etched too much (becomes transparent at different spots), then deposit an additional layer (see pre-processing step).



21. INSPECTION

Location: (Class 100 clean room)

Inspect	Measure step height with the surface profiler. A step height higher with about 50nm than the specified thickness of the epitaxial emitter layer should be the resulting height.

Base_Collector layers etching process

22. Hard mask: PECVD SiO2 hard mask deposition in Novellus – deposit required value

Location: (Class 100 clean room)

Use the Novellus Concept 1 for required thickness (~1nm/sec etch rate, so about 1um for each 1um etched in SiC plus 50% more for insurance) SiO2 deposition
Check Gases. Follow the operating instructions from the manual when using this machine.

Use recipe: .xxxSiOstd to deposit the required SiO2 thickness. Change time according to logbook.

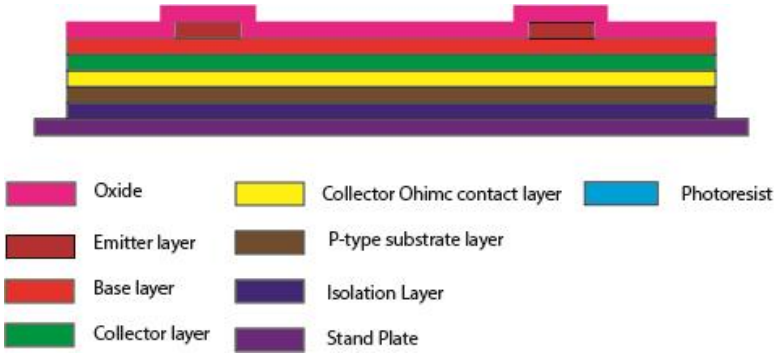
Note: If photoresist is applicable, then the hard mask is not needed.

Note: Use a Si test wafer for deposited SiO2 layer thickness measurement.

23. FS COATING– POSITIVE PHOTORESIST – Mask 2: Base_Collector layer

Location: (Class 100 clean room)

Use the EVG120 system to coat the wafers with **(2.1µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **SPR3012 positive resist**, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

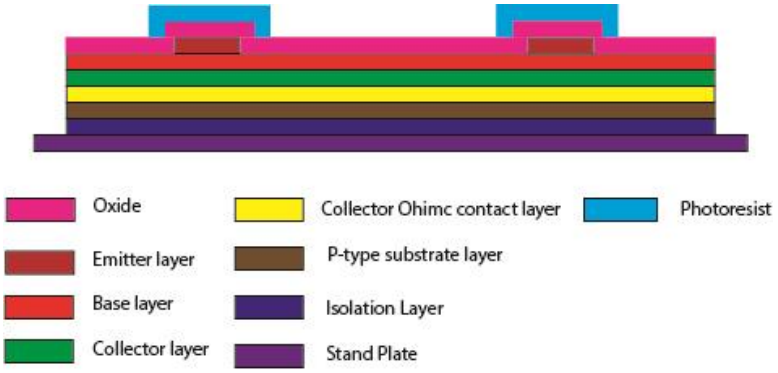


24. **FS EXPOSURE CONTACT ALIGNER – Mask 2: Base_Collector layer**
Location: (Class 1000 clean room)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 2 Base_Collector layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. This should be ~8-10sec. For thicker resist layers, the exposure duration should be higher.



25. FS Dev – Single puddle

Location: (Class 100 clean room)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Dev-SP "**

26. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

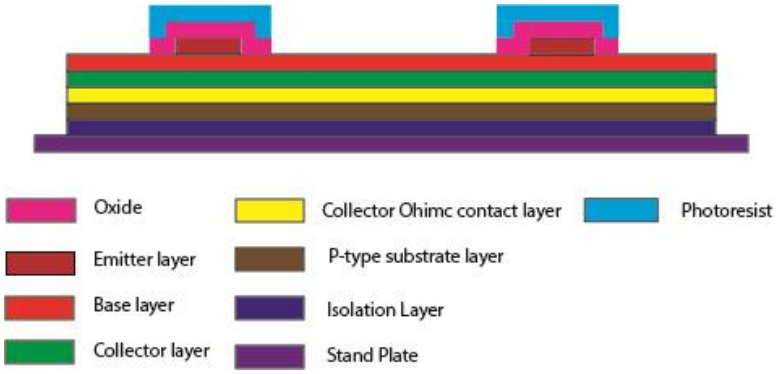
Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Inspect	Measure step height with the surface profiler. Note this value to compare with the step height after SiO2 etch process.

27. BASE_COLLECTOR LAYERS DEFINITION IN SIO2 HARD MASK FOR RAPIER ETCHING – WET ETCHING

Location: (Class 100 clean room)

BHF	Base_Collector layers definition in the SiO2 hard mask using BHF. See etch rates BHF in etch manual on the wall next to wet benches and do 20 seconds of overetch to make sure no SiO2 residues remain.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.
Inspect	Check under the microscope. Measure step height with the surface profiler.
Note:	Remove photoresist and do the standard cleaning if the hard mask is used.



28. INSPECTION: SIO2 HARD MASK OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects. Additionally, measure with DekTak surface profiler to see if the expected value has been obtained. Compare with the previously measured values for the deposited SiO2 hard mask and photoresist coating.

29. Resist stripping: TEPLA Program 1

Location: (Class 100 clean room)

Plasmastrip	Use the Tepla plasma system to remove the photo resist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
	Use program 1

30. CLEANING PROCEDURE: HNO3 100% (metal)

Location: (Class 100 clean room)

Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger "rinser/dryer" (metal) with the standard program.
Note:	No 65% HNO3 cleaning step!

31. BASE_COLLECTOR LAYERS DEFINITION ON THE 4H-SIC WAFER – RAPIER

Location: (Class 100 clean room)

Dry etch — Base_Collector layers etching in SiC epitaxial layer.

Use recipes of Brahim optimized for 4H-SiC. Selectivity is less than 1 for SiO2.

Inspect — Measure step height with the DekTak surface profiler. Ensure more than the functional layer thickness has been etched. The overetch should be approximately 50nm, thus 50seconds of overetch. Use the etch rate value of SiO2 and 4H-SiC to calculate the new etched structure. ETCH MORE IF NEEDED.

32. SIO2 HARD MASK REMOVAL – WET ETCHING

Location: (Class 100 clean room)

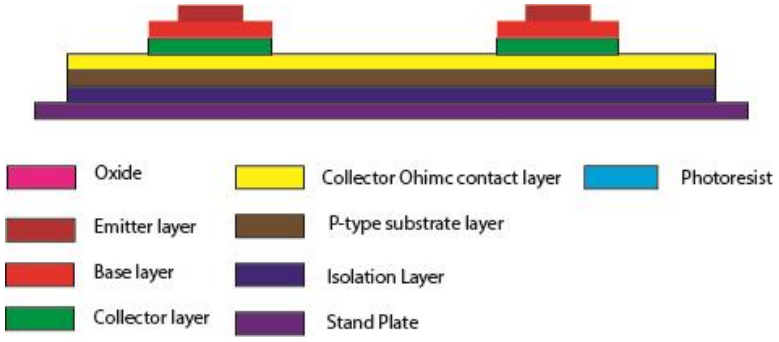
BHF — SiO2 hard mask removal using BHF.

See etch rates BHF and do 3min of overetch to make sure no SiO2 residues remain.

QDR — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying — Use the manual dryer.

Note: The aluminium BS layer also gets etched in the BHF solution. If the layer is etched too much (becomes transparent at different spots), then deposit an additional layer (see pre-processing step).



33. INSPECTION

Location: (Class 100 clean room)

Inspect — Measure step height with the surface profiler. A step height higher with about 100nm than the specified total thickness of the epitaxial Base_Collector layers should be the resulting height.

Collector_Ohmic layer etching process

34. Hard mask: PECVD SiO2 hard mask deposition in Novellus – deposit required value

Location: (Class 100 clean room)

Use the Novellus Concept 1 for required thickness (~1nm/sec etch rate, so about 1um for each 1um etched in SiC plus 50% more for insurance) SiO2 deposition
Check Gases. Follow the operating instructions from the manual when using this machine.

Use recipe: .xxxSiOstd to deposit the required SiO2 thickness. Change time according to logbook.

Note: If photoresist is applicable, then the hard mask is not needed.

Note: Use a Si test wafer for deposited SiO2 layer thickness measurement.

35. FS COATING– POSITIVE PHOTORESIST – Mask 3: Collector_Ohmic layer

Location: (Class 100 clean room)

Use the EVG120 system to coat the wafers with **(2.1µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **SPR3012 positive resist**, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

36. **FS EXPOSURE CONTACT ALIGNER – Mask 3: Collector_Ohmic layer**
Location: (Class 1000 clean room)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 3 Collector_Ohmic layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. This should be ~8-10sec. For thicker resist layers, the exposure duration should be higher.

37. FS Dev – Single puddle

Location: (Class 100 clean room)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Dev-SP "**

38. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Inspect Measure step height with the surface profiler. Note this value to compare with the step height after SiO2 etch process.

39. COLLECTOR_OHMIC LAYER DEFINITION IN SIO2 HARD MASK FOR RAPIER ETCHING – WET ETCHING

Location: (Class 100 clean room)

BHF Collector_Ohmic layer definition in the SiO2 hard mask using BHF.

See etch rates BHF in etch manual on the wall next to wet benches and do 20 seconds of overetch to make sure no SiO2 residues remain.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the manual dryer.

Inspect Check under the microscope. Measure step height with the surface profiler.

Note: Remove photoresist and do the standard cleaning if the hard mask is used.

40. INSPECTION: SIO2 HARD MASK OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects. Additionally, measure with DekTak surface profiler to see if the expected value has been obtained. Compare with the previously measured values for the deposited SiO2 hard mask and photoresist coating.

41. Resist stripping: TEPLA Program 1

Location: (Class 100 clean room)

Plasmastrip Use the Tepla plasma system to remove the photo resist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.

Use program 1

42. CLEANING PROCEDURE: HNO3 100% (metal)

Location: (Class 100 clean room)

Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger "rinser/dryer" (metal) with the standard program.
Note:	No 65% HNO3 cleaning step!

43. COLLECTOR_OHMIC LAYER DEFINITION ON THE 4H-SIC WAFER – RAPIER

Location: (Class 100 clean room)

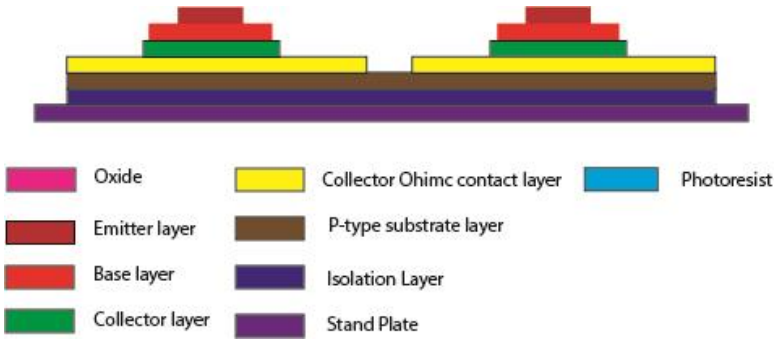
Dry etch	Collector_Ohmic layer etching in SiC epitaxial layer. Use recipes of Brahim optimized for 4H-SiC. Selectivity is less than 1 for SiO2.
Inspect	Measure step height with the DekTak surface profiler. Ensure more than the functional layer thickness has been etched. The overetch should be approximately 50nm, thus 50seconds of overetch. Use the etch rate value of SiO2 and 4H-SiC to calculate the new etched structure. ETCH MORE IF NEEDED.

44. SIO2 HARD MASK REMOVAL – WET ETCHING

Location: (Class 100 clean room)

BHF	SiO2 hard mask removal using BHF. See etch rates BHF and do 3min of overetch to make sure no SiO2 residues remain.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.

Note: The aluminium BS layer also gets etched in the BHF solution. If the layer is etched too much (becomes transparent at different spots), then deposit an additional layer (see pre-processing step).



45. INSPECTION

Location: (Class 100 clean room)

Inspect	Measure step height with the surface profiler. A step height higher with about 100nm than the specified total thickness of the epitaxial Collector_Ohmic layer should be the resulting height.

Mesa layer etching process

46. Hard mask: PECVD SiO2 hard mask deposition in Novellus – deposit required value

Location: (Class 100 clean room)

Use the Novellus Concept 1 for required thickness (~1nm/sec etch rate, so about 1um for each 1um etched in SiC plus 50% more for insurance) SiO2 deposition
Check Gases. Follow the operating instructions from the manual when using this machine.

Use recipe: .xxxSiOstd to deposit the required SiO2 thickness. Change time according to logbook.

Note: If photoresist is applicable, then the hard mask is not needed.

Note: Use a Si test wafer for deposited SiO2 layer thickness measurement.

47. FS COATING– POSITIVE PHOTORESIST – Mask 4: Mesa layer

Location: (Class 100 clean room)

Use the EVG120 system to coat the wafers with **(2.1µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **SPR3012 positive resist**, and a soft bake at 95 °C for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

48. **FS EXPOSURE CONTACT ALIGNER – Mask 4: Mesa layer**
Location: (Class 1000 clean room)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 4 Mesa layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. This should be ~8-10sec. For thicker resist layers, the exposure duration should be higher.

49. FS Dev – Single puddle

Location: (Class 100 clean room)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Dev-SP "**

50. INSPECTION: LINEWIDTH AND OVERLAY

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Inspect	Measure step height with the surface profiler. Note this value to compare with the step height after SiO2 etch process.

51. MESA LAYER DEFINITION IN SIO2 HARD MASK FOR RAPIER ETCHING – WET ETCHING

Location: (Class 100 clean room)

BHF	Mesa layer definition in the SiO2 hard mask using BHF. See etch rates BHF in etch manual on the wall next to wet benches and do 20 seconds of overetch to make sure no SiO2 residues remain.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.
Inspect	Check under the microscope. Measure step height with the surface profiler.
Note:	Remove photoresist and do the standard cleaning if the hard mask is used.

52. INSPECTION: SIO2 HARD MASK OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects. Additionally, measure with DekTak surface profiler to see if the expected value has been obtained. Compare with the previously measured values for the deposited SiO2 hard mask and photoresist coating.

53. Resist stripping: TEPLA Program 1

Location: (Class 100 clean room)

Plasmastrip	Use the Tepla plasma system to remove the photo resist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use program 1

54. CLEANING PROCEDURE: HNO3 100% (metal)

Location: (Class 100 clean room)

Cleaning	10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger "rinser/dryer" (metal) with the standard program.
Note:	No 65% HNO3 cleaning step!

55. MESA LAYER DEFINITION ON THE 4H-SIC WAFER – RAPIER

Location: (Class 100 clean room)

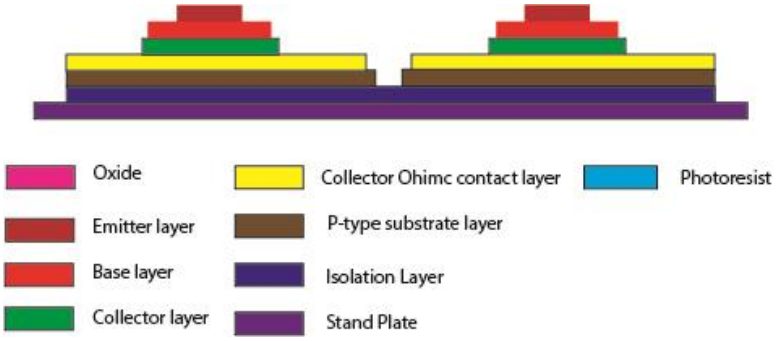
Dry etch	MESA layer etching in SiC epitaxial layer. Use recipes of Brahim optimized for 4H-SiC. Selectivity is less than 1 for SiO2.
Inspect	Measure step height with the DekTak surface profiler. Ensure more than the functional layer thickness has been etched. The overetch should be approximately 50nm, thus 50seconds of overetch. Use the etch rate value of SiO2 and 4H-SiC to calculate the new etched structure. ETCH MORE IF NEEDED.

56. SIO2 HARD MASK REMOVAL – WET ETCHING

Location: (Class 100 clean room)

BHF	SiO2 hard mask removal using BHF. See etch rates BHF and do 3min of overetch to make sure no SiO2 residues remain.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.

Note: The aluminium BS layer also gets etched in the BHF solution. If the layer is etched too much (becomes transparent at different spots), then deposit an additional layer (see pre-processing step).



57. INSPECTION

Location: (Class 100 clean room)

Inspect — Measure step height with the surface profiler. A step height higher with about 100nm than the specified total thickness of the epitaxial Mesa layer should be the resulting height.

Device Passivation/Insulation process

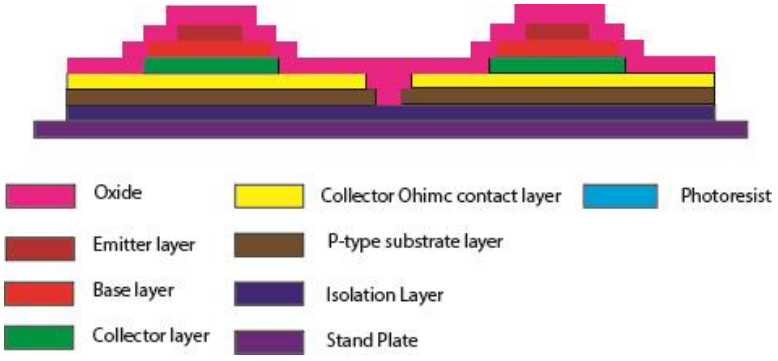
58. Passivation layer: PECVD SiO2 hard deposition in Novellus – deposit required value

Location: (CR100)

Use the Novellus Concept 1 for required thickness SiO2 deposition
Check Gases. Follow the operating instructions from the manual when using this machine.

Use recipe: .xxxSiOstd to deposit the required SiO2 thickness. Change time according to logbook.

Note: Use a Si test wafer for deposited SiO2 layer thickness measurement. This will be later needed to determine the actual etch rate as the etch rate of the wet etch baths are not accurate.



N-Type Metal Layer process

59. FS COATING– NLOF PHOTORESIST 2020 – Mask 5: N-Type Metal Layer

Location: (CR100)

Use the EVG120 system to coat the wafers with **(3.5µm)** photoresist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with **NLOF 2020 negative resist**, and a soft bake at 95 °C for 60 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use program **"C0 – Topo - NLOF – 3.5µm no EBR"** on the coating station

Note: see the instructions on the machine regarding HMDS and EBR steps.

60. **FS EXPOSURE CONTACT ALIGNER – Mask 5: N-Type Metal layer**
Location: (CR100)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 5 N-Type Metal layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. For thicker resist layers, the exposure duration should be higher. Note that the exposure energy for positive and negative photoresist differs.

61. FS Dev – NLOF baking and development process – N-Type Metal layer

Location: (CR100)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Only - X-link bake"** for x-link baking. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

Use program **"xDense - Dev - lift-off extra rinse"** for development. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

62. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Note: measure the thickness of the photoresist using the DekTak surface profiler. This value is needed for later use to see if the contact openings in the passivation layer have been done successfully.

63. N-TYPE METAL LAYER DEFINITION IN SIO2 PASSIVATION LAYER FOR CONTACT OPENINGS – WET ETCHING

Location: (CR100)

BHF	Contact openings in the SiO2 passivation layer using BHF. See etch rates BHF and do at least 10 seconds of overetch to make sure no SiO2 residues remain. First use the test wafer from the previous passivation deposition step to make sure what the thickness is of the layer and what the actual etch rate should be.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the manual dryer.

64. INSPECTION: SIO2 PASSIVATION LAYER OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects. Additionally, measure with DekTak surface profiler to see if the expected value has been obtained. Compare with the previously measured values for the deposited SiO2 passivation layer and photoresist coating.

65. NICKEL DEPOSITION – N-TYPE METAL LAYER – LIFT-OFF PROCESS PART 1

Note: wafers become contaminated from this step onwards.

Location: (CR100 clean room or CR10000)

Ni	Nickel deposition. This is step 1 of the lift-off process performed for N-Type Metal Layer.

Use the Trikon Sigma. Target is in dep C. Target is on request. PLAN WELL!!!

Note: Use carrier wafers for contaminated wafers after this step.

Follow the operating instructions from the manual when using Trikon Sigma machine.

Requirements: First do a LUR (Leak Up Rate) test. This is required to see how the photoresist is reacting in the sigma to prevent polymer contamination in the chamber.

In case of CHA Evaporator usage:
Note: If Target is not available soon enough, use CHA Evaporator for this.

Use machine: CHA Evaporator. Follow the operating instructions from the manual when using this machine.

Check the target in the machine. There should be enough material in the holder. Use sequence Ni sequence.

66. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

67. NICKEL DEPOSITION – N-TYPE METAL LAYER – LIFT-OFF PROCESS PART 2

Location: (CR10000)

Lift-off Use NMP at 70 °C to remove the photoresist in ultrasonic bath. Use for 10 minutes.

Rinse and dry Rinse in DI water and dry in the manual dryer

Tip: start warming the NMP in the ultrasonic holder before starting the evaporation. This way when the evaporation is done, the NMP will have warmed up.

68. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

P-Type Metal Layer process

69. FS COATING– NLOF PHOTORESIST 2020 – Mask 6: P-Type Metal Layer

Location: (CR100, polymer lab)

Use Manual coating @ polymer lab and follow the instructions specified for this equipment. Steps are:

1- Bake out the wafer to remove any water layer. Time: …… Temperature: ……
2- 10 minutes HDMS treatment. Use contaminated carrier/cassette.
3- Coat the wafer with 3.5 µm NLOF photoresist (2020). RPM: 1000
   - Use contaminated chuck.
   - Take the photoresist out of the refrigerator at least **2 hours** prior to deposition. Ask Hitham for the best recipe.
4- Soft bake for 1 minute @ 95 °C. Use contaminated hotplate.

Always check the relative humidity (48 ± 2 %) in the room before coating.

70. **FS EXPOSURE CONTACT ALIGNER – Mask 6: P-Type Metal layer**
Location: (CR100)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 6 P-Type Metal layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. For thicker resist layers, the exposure duration should be higher. Note that the exposure energy for positive and negative photoresist differs.

71. FS Dev – NLOF baking and development process – P-Type Metal layer

Location: (CR100)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Only - X-link bake"** for x-link baking. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

Use program **"xDense - Dev - lift-off extra rinse"** for development. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

72. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

Note: measure the thickness of the photoresist using the DekTak surface profiler. This value is needed for later use to see if the contact openings in the passivation layer have been done successfully.

73. P-TYPE METAL LAYER DEFINITION IN SIO2 PASSIVATION LAYER FOR CONTACT OPENINGS – WET ETCHING

Location: (CR10000)

Note: Wafers are contaminated. Use your own BHF batch in CR10000. Follow instructions from Hitham.

BHF	Contact openings in the SiO2 passivation layer using BHF. See etch rates BHF and do at least 10 seconds of overetch to make sure no SiO2 residues remain. First use the test wafer from the previous passivation deposition step to make sure what the thickness is of the layer and what the actual etch rate should be.
QDR	Rinse in DI water for at least 10min.
Drying	Use the manual dryer. Use contaminated chuck.

74. INSPECTION: SIO2 PASSIVATION LAYER OPENING CONFIRMATION

Location: (Class 100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay. No SiO2 residues allowed on areas where this should not be the case. Inspect if there is any discoloration effects.

75. NICKEL STACK DEPOSITION – P-TYPE METAL LAYER – LIFT-OFF PROCESS PART 1

Location: (CR100 clean room or CR10000)

Ni Nickel stack deposition. This is step 1 of the lift-off process performed for P-Type Metal Layer.

Use the Trikon Sigma. Target is in dep C. Target is on request. PLAN WELL!!!

Note: Use carrier wafers for contaminated wafers after this step.

Follow the operating instructions from the manual when using Trikon Sigma machine.

Requirements: First do a LUR (Leak Up Rate) test. This is required to see how the photoresist is reacting in the sigma to prevent polymer contamination in the chamber.

In case of CHA Evaporator usage:
Note: If Target is not available soon enough, use CHA Evaporator for this.

Use machine: CHA Evaporator. Follow the operating instructions from the manual when using this machine.

Check the target in the machine. There should be enough material in the holder. Use sequence Ni sequence.

76. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

77. NICKEL DEPOSITION – N-TYPE METAL LAYER – LIFT-OFF PROCESS PART 2

Location: (CR10000)

Lift-off Use NMP at 70 °C to remove the photoresist in ultrasonic bath. Use for 10 minutes.

Rinse and dry Rinse in DI water and dry in the manual dryer

Tip: start warming the NMP in the ultrasonic holder before starting the evaporation. This way when the evaporation is done, the NMP will have warmed up.

78. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

Overlay Metal Layer process

79. FS COATING– NLOF PHOTORESIST 2020 – Mask 7: Overlay Metal Layer

Location: (CR100, polymer lab)

Use Manual coating @ polymer lab and follow the instructions specified for this equipment. Steps are:

5- Bake out the wafer to remove any water layer. Time: …… Temperature: ……
6- 10 minutes HDMS treatment. Use contaminated carrier/cassette.
7- Coat the wafer with 3.5 µm NLOF photoresist (2020). RPM: 1000
   - Use contaminated chuck.
   - Take the photoresist out of the refrigerator at least **2 hours** prior to deposition. Ask Hitham for the best recipe.
8- Soft bake for 1 minute @ 95 °C. Use contaminated hotplate.

Always check the relative humidity (48 ± 2 %) in the room before coating.

80. **FS EXPOSURE CONTACT ALIGNER – Mask 7: Overlay Metal Layer**
Location: (CR100)

Follow the operating instructions from the manual when using this machine.

Expose the wafer using the contact aligner: **Mask 7 Overlay Metal Layer @ 55mJ/cm^2.**

Calculate the exposure time based on the notes in the contact aligner manual and optical power in the list on the wall next to the contact aligner. For thicker resist layers, the exposure duration should be higher. Note that the exposure energy for positive and negative photoresist differs.

81. FS Dev – NLOF baking and development process – Overlay Metal layer

Location: (CR100)

Use the EVG120 system to develop the wafer, and follow the instructions specified for this equipment.

Use program **"Only - X-link bake"** for x-link baking. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

Use program **"xDense - Dev - lift-off extra rinse"** for development. Ask tool owner about the recipe. In the past there were some issues with the residues and the EKL processing team was solving this.

82. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100)

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

83. Cr/Au DEPOSITION – OVERLAY METAL LAYER – LIFT-OFF PROCESS PART 1

Location: (CR100 clean room or CR10000)

Cr/Au Chrome/gold deposition. This is step 1 of the lift-off process performed for Overlay Metal Layer.

Use machine: CHA Evaporator. Follow the operating instructions from the manual when using this machine.

Check the target in the machine. There should be enough material in the holder.

Use sequence Cr10nm/Au200nm to deposit 10nm of chrome and 200 nm of gold on the substrate. Chrome is used as an adhesion layer.

84. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

85. Cr/Au DEPOSITION – OVERLAY METAL LAYER – LIFT-OFF PROCESS PART 2

Location: (CR10000)

Lift-off Use NMP at 70 °C to remove the photoresist in ultrasonic bath. Use for 10 minutes.

Rinse and dry Rinse in DI water and dry in the manual dryer

Tip: start warming the NMP in the ultrasonic holder before starting the evaporation. This way when the evaporation is done, the NMP will have warmed up.

86. INSPECTION: LINEWIDTH AND OVERLAY

Location: (CR100 clean room)

Visually inspect the wafers through a microscope, and check line width and overlay.

87. DICING OF WAFER

Location: (MEMS lab)

Dice the wafer into individual dies.