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4-output Programmable Spin Wave Logic Gate

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Abstract*—To bring Spin Wave (SW) based computing paradigm into practice and develop ultra low power Magnonic circuits and computation platforms, one needs basic logic gates that operate and can be cascaded within the SW domain without requiring back and forth conversion between the SW and voltage domains. To achieve this, SW gates have to possess intrinsic fanout capabilities, be input-output data representation coherent, and reconfigurable. In this paper, we address the first and the last requirements and propose a novel 4-output programmable SW logic gate. First, we introduce the gate structure and demonstrate that, by adjusting the gate output detection method, it can parallelly evaluate any 4-element subset of the 2-input Boolean function set {(N)AND, (N)OR, and X(N)OR} . Furthermore, we adjust the structure such that all its 4 outputs produce SWs with the same energy and demonstrate that it can evaluate Boolean function sets while providing fanout capabilities ranging from 1 to 4. We validate our approach by instantiating and simulating different gate configurations such as 4-output AND/OR, 4-output XOR/XNOR, output energy balanced 4-output AND/OR, and output energy balanced 4-output XOR/XNOR by means of Object Oriented Micromagnetic Framework (OOMMF) simulations. Finally, we evaluate the performance of our proposal in terms of delay and energy consumption and compare it against existing state-of-the-art SW and 16 nm CMOS counterparts. The results indicate that for the same functionality, our approach provides 3× and 16× energy reduction, when compared with conventional SW and 16 nm CMOS implementations, respectively.Index Terms*—Spin-wave, Programmable Logic Gate, Energy**

I. Introduction

Processing the enormous amount of row data, which resulted due to the past decades information technology revolution, requires efficient computation platforms and CMOS downscaling has been sufficient to keep improving processing performance to match this requirements [1], [2]. However, due to the technological difficulties: (i) leakage wall [2], (ii) reliability wall [2], and (iii) cost wall [2], CMOS downscaling becomes very difficult at the nanoscale, which eventually will soon lead to the end of Moore's law. Therefore, new technologies have been explored to find an alternative for CMOS, e.g. memristors, graphene devices, and spintronics [3]. Magnonics, a subset of spintronics, exploits Spin Waves (SWs) interactions to perform logic operations and appears to be a promising technology because of its attractive features [1], [3]: (i) low power consumption as it doesn't need charge movement, (ii) acceptable delay, (iii) scalability down to the nm range.

Different spin wave logic gates have already been demonstrated [4], [5]. The first experimental spin wave logic gate was designed based on the Mach-Zender interferometer [4]. In contrast to the aforementioned scheme, which encode information in amplitude, another proposal make use of spin wave phase to encode the information [5]. Consequently, buffer, inverter, (N)AND, (N)OR, XOR and Majority gates were built by embedding information in the spin wave phase and using both amplitude and phase to detect the information at the output [5]. Despite these magnonics technology steps forward, state-of-the-art gates provide only one output thus they cannot provide fanout capabilities, which are crucial for the effective implementation of large practically relevant circuits. Note that, if the output of such a gate should be fed to multiple following gates inputs, it must be multiple times replicated, which results in substantial area and energy consumption overheads.

The problem of fanout is solved in this paper. This work main contributions are:

- Development and design of a 4-output balanced and unbalanced PLG, which can evaluate any 4-element subset of the 2-input Boolean function set {(N)AND, (N)OR, and X(N)OR}. For example, one such PLG gate can parallelly evaluate the set of 2-input logic functions {OR, NOR, XOR, XNOR} on the same input combination. The balanced 4-output structure generates output SWs with the same energy, which implies intrinsic fanout capability. Therefore, the same function, e.g., X(N)OR, can be captured at different outputs and an up to 4 fanout can be achieved without requiring gate replication.
- Functional validation and performance evaluation. We simulate different gate configurations, i.e., 4-output AND/OR, 4-output XOR/XNOR, output energy balanced 4-output AND/OR, and output energy balanced 4-output XOR/XNOR by means of OOMMF simulations. Also, we compare our proposal with the state-of-the-art work functionally equivalent counterparts and demonstrate that our approach provides 3× and 16× energy reduction, when compared with the conventional SW and CMOS implementations, respectively.

The rest of the paper is organized as follows. Section II explains SW fundamentals. Next, Section III introduces the proposed 2-input 4-output PLG structures. Then Section IV presents the simulation platform and provides the simulation results. Finally, Section V concludes the paper.

II. Spin-Wave Based Technology Basics

In a magnetic material, the magnetization can be exploited for memory or computation purposes. For example, in a magnetic equilibrium state, the magnetization is static which can be utilized to design spintronic memory devices. When

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the magnetization is out of equilibrium, it is subjected to a dynamical motion due to the magnetic torque. The mathematical description of this magnetization dynamics is given by the Landau-Lifshitz-Gilbert (LLG) equation [6]: $\frac{d\vec{M}}{dt} = -|\gamma|\mu_0\left(\vec{M}\times\vec{H}_{eff}\right) + \frac{\alpha}{M_s}\left(\vec{M}\times\frac{d\vec{M}}{dt}\right)$, where γ is the gyromagnetic ratio, α the damping factor, M the magnetization, M_s the saturation magnetization, and H_{eff} the effective field which contains the different magnetic interactions the external field, the exchange field, the demagnetizing field, and the magneto-crystalline field.

For small magnetization perturbations LLG Equation can be linearised and has wave-like solutions. These weak wave-like solutions are called Spin Waves and can be seen as a collective excitation of the magnetization.

During SW excitation, its amplitude and phase can be utilized to encode information. This can be done simultaneously at different spin wave frequencies [7], which potentially allows for parallel data processing. The interaction between SWs in the same waveguide is governed by the interference principle. To explain the interference principle, we make use of two SW interference as discussion vehicle. The interference result is constructive when they have the same phase $\Delta\phi = 0$, whereas if they are out of phase $\Delta\phi = \pi$, the interference is destructive. Consequently, if more than two waves coexist in the waveguide, the majority principle governs the interference result. For example, if 3 SWs are present in a waveguide and at most one SW has phase π while the others have phase 0 the interference result will be a SW with $\phi = 0$, whereas a SW with $\phi = \pi$ will be the result if two or all SWs have phase π.

III. 4-output Programmable Logic Gate

Unbalanced* 4*-output Programmable Logic Gate*:* Figure 1a presents the proposed 2-input 4-output PLG. The structure has a ladder shape with two data inputs I_1 and I_2, and two controls inputs C_1 and C_2. The outputs O_1, O_2, O_3, and O_4 correspond to the detection cells where the gate results are obtained. The excitation and detection stages can be voltage-encoded (or current-encoded) depending on the utilized excitation/detection method. As mentioned previously, there are multiple options for the SWs excitation and detection, e.g., microstrip antennas, and magnetoelectric cells [8].

In principle, the structure is generic and functions correctly if the input SWs have the same amplitude A, wavelength λ, and frequency f regardless of their values, while the chosen λ, and f values determine its dimensions. To guarantee a proper behaviour, the structure dimensions must be precisely determined. For example, if SWs should interfere constructively when they have the same phase and destructively for opposite phases the dimensions must be $d_3 = d_4 = d_5 = \ldots = d_8 = n \times \lambda$ (where n=0, 1, 2, 3, ...). When the opposite behaviour is desired, SWs interfering constructively when they are out of phase and destructively when they are in phase, then the dimensions should be $d_3 = d_4 = d_5 = \ldots = d_8 = (n+\frac{1}{2})\times\lambda$.

Moreover, two ways of output detection exist: (i) Phase Detection (PD) and (ii) Threshold Detection (TD). Depending on a predefined phase, PD is performed as follows: if output SW phase is $\phi = 0$ the output is logic 0 and logic 1 if $\phi = \pi$. For TD the SW magnetization is measured and compared with a predefined threshold value such that if the magnetization is larger than the threshold, the output is logic 1, and logic 0 otherwise.

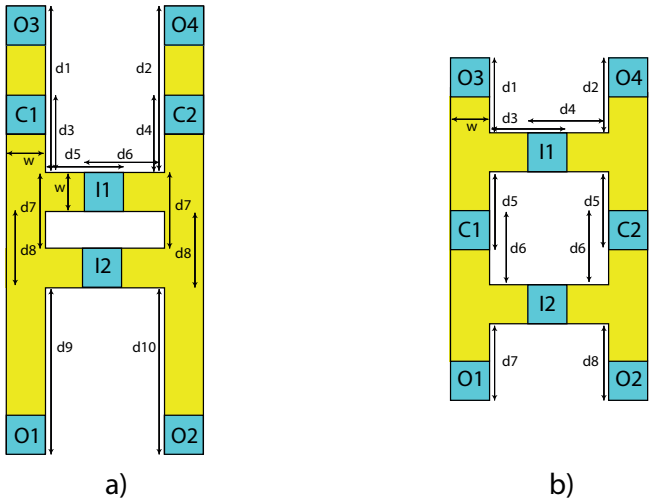

Fig. 1. a) 2-input 4-output SW Programable Logic Gate b) 2-input 4-output Output Energy Balanced SW Programable Logic Gate

Further, the position of the PLG outputs O_1, O_2, O_3, and O_4 must be also accurately determined to obtain the desired results at the outputs. If the used detection method is phase detection, the result can be the logic gate output itself or its inverted version depending on the position. If the direct logic function is of interest, the distances must be $d_1 = d_2 = d_9 = d_{10} = n \times \lambda$ whereas if the complement is of interest, the distances should be $d_1 = d_2 = d_9 = d_{10} = (n + \frac{1}{2}) \times \lambda$. Whereas if the used detection method is threshold detection, the output should be as close as possible from the last interference point to have strong spin wave. In this case, if the complement is of interest, then the aforementioned condition can be flipped such that if magnetization is less than the threshold, the output is logic 1, and logic 0 otherwise.

If PD is utilized, (N)AND and/or (N)OR gates are implemented. In contrast, XOR and/or XNOR gates are obtained if TD is utilized. Furthermore, both mechanisms can be utilized in the same time, i.e., some outputs can PD captured and others TD captured. Therefore, some outputs can be (N)AND or (N)OR gate and the others can be XOR or XNOR gate. However, the XOR/XNOR functionality cannot be obtained at O_3 and O_4 because they receive amplitude unbalanced SW due to the fact that I_3 and I_4 are closer to O_3 and O_4 than to O_1 and O_2. The unbalance SW amplitude also causes unbalance in the output energy as it clarified in Section IV. Therefore, to enable full gate flexibility a balance PLG design is needed as will be introduced in the following subsection. Depending on the desired functionality the PLG can simultaneously evaluate up to 4 2-input different basic Boolean functions. Note that the structures in Figure 1 can be extended and can have multiple inputs.

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Balanced* 4*-output Programmable Logic Gate: As previously mentioned due to the lack of symmetry the 4 outputs are not fully equivalent in terms of computation capabilities. To circumvent this limitation we proposed a symmetric energy balanced 4-input PLG depicted in Figure 1b. To balance the output energies and be able to capture the result of all possible logic functions at all outputs, we relocate the control inputs in the middle of the vertical waveguide such that each gate input is located at the same distance from all the four gate outputs. Therefore, the waves propagate towards O_1, O_2, O_3, and O_4 on equal length paths, which means that the rich the outputs with the same (amplitude) energy. The previously described design procedures are in place and all logic functions are feasible at each outputs. An extra advantage of this structure is that when computing the same function it can provide a clean maximum fanout of 4, or when computing 2 functions each of them can be produced with a fanout of 2.

IV. Simulation Setup, Results and Discussion

A. Simulation Setup

The Object Oriented MicroMagnetic Framework (OOMMF) [9] is used to validate the proposed structures. $Fe_{60}Co_{20}B_{20}$ is utilized as waveguide material and its parameters are as follows; Magnetic saturation M_s is 1.1×10^6 A/m, perpendicular anisotropy constant k_{ani} is 8.3177×10^5 J/m^3, damping constant α is 0.004, and exchange stiffness A_{exch} is 18.5 pJ/m [3]. The width of the waveguide is 50 nm and the thickness is 1 nm. The static magnetization is out-of-plane by Perpendicular Magnetic Anisotropy (PMA) and no external magnetic field is require as the PMA field is larger than the magnetic saturation [3]. The spin wave wavelength of $\lambda = 110$ nm is chosen to be larger than the width of the waveguide. Once, the wavelength is determined, the distances can be calculated and become $d_3 = d_4 = d_5 = d_6 = d_7 = d_8 = 110$ nm for the structure in Figure 1a and $d_3 = d_4 = d_5 = d_6 = 110$ nm for the structure in Figure 1b. Also, as $\lambda = 110$ nm, and $k = 2\pi/\lambda = 57$ rad/μm, the SW frequency becomes $f = 9$ GHz according to the dispersion relation.

B. Simulation Results

2*-input* 4*-output AND/OR gates:* Figure 2a presents simulation results for the 2-input 4-output AND/OR gates for 4 cases $I_1I_2 = \{00\ 01\ 10\ 11\}$. The outputs O_1, O_2, O_3, and O_4 are placed at d_1=d_2=d_9=d_{10}=220nm (n=2). As it is clear in Figure 2a, the left arm provides the AND gate functionality at outputs O_1 and O_3, whereas the right arm provides the OR gate functionality at outputs O_2 and O_4. Taking O_1 and O_3 as an example, if inputs I_1I_2=00, I_1I_2=01, I_1I_2=10, then the outputs O_1=0 and O_3=0. In contrast, O_1=1 and O_3=1 for the input combination I_1I_2=11. The OR gate functionality is obtained from O_2 and O_4. In addition, NAND and NOR gates can be captured by changing the reading positions to be at $3\lambda/2$, i.e., d_1=d_2=d_9=d_{10}=165nm (n=1). Therefore, the structure can provide AND, NAND, OR, and NOR gate functionalities while each gate column being able to provide

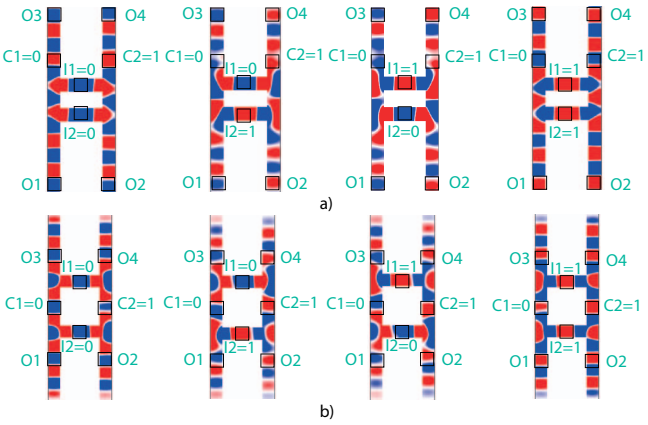

Table I 4-output Gates Normalized Output Magnetizations

C1=C2	I2	I1	O1	O2	O3	O4	O1	O2	O3	O4
0	0	0	0.9	0.9	1	1	1	1	1	1
0	0	1	0.25	0.25	0.45	0.43	0.33	0.33	0.33	0.33
0	1	0	0.32	0.32	0.26	0.27	0.3	0.3	0.3	0.3
0	1	1	0.38	0.38	0.33	0.33	0.43	0.43	0.43	0.43
			4-output Gate a) Normalized Output Magnetization				4-output Balanced Gate b) Normalized Output Magnetization			

Fig. 2. a) 2-input 4-output AND/OR Gate b) 2-input 4-output balanced AND/OR Gate

AND (OR) in its direct and inverted format or in the same format with a fanout of 2.

2*-input* 4*-output XOR/XNOR gates:* Table I in Figure 2 presents normalized magnetizations at the outputs O_1, O_2, O_3, and O_4 for C_1=C_2=0 and for different inputs combination $I_1I_2 = \{00\ 01\ 10\ 11\}$ for the structure in Figure 1a. Note that the results for the cases $C_1C_2 = \{01\ 10\ 11\}$ are exhibiting the same behaviour.

Table I in Figure 2 indicate that the outputs O_1 and O_2 can provide XOR or XNOR logic gates if an appropriate threshold is set to detect logic 0 and logic 1. On the other hand, O_3 and O_4 cannot provide these logic gates. As it can be observed from the table, the XOR gate can be implemented at O_1 and O_2 by averaging the O_1 and O_2 normalized magnetizations for input combinations 10 and 11, which is 0.35. The XOR gate can be obtained by setting the condition that the normalized magnetization is greater than 0.35 for logic 0 and logic 1, otherwise. By reversing the condition, the XNOR gate is obtained at O_1 and O_2. As it is clear from the Table, the four outputs don't have the same magnetization and cannot provide XOR and XNOR functionalities (only O_1 and O_2 can). Thus, to balance the output energies and to enable XOR and XNOR in all four outputs, we place the control inputs as depicted in Figure 1b.

2*-input* 4*-output balanced AND/OR gates:* The simulation results for 2-input 4-output balanced AND/OR gate for 4 cases $I_1I_2 = \{00\ 01\ 10\ 11\}$ are presented in Figure 2b. By inspecting Figure 2b, the left arm provides the AND gate functionality in the two outputs O_1 and O_3. On the other hand, the right arm provides the OR gate results in the two outputs O_2 and O_4. These are placed with O_1 and O_3 at distances d_1=d_2=d_7=d_8=110nm (n=1). The same line of thinking as the previous 2-input cases can be followed to analyze the results. Taking O_1 and O_3 as an example, if the inputs are

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I_1I_2=00, I_1I_2=01, I_1I_2=10, then the outputs becomes O_1=0 and O_3=0. Also, O_1=1 and O_3=1 for the input combination I_1I_2=11. The OR gate result is obtained from O_2 and O_4. In addition, NAND and NOR gates can be captured by placing the reading positions at $\lambda/2$, i.e., d_1=d_2=d_7=d_8=55nm (n=0). Therefore, the structure can provide AND, NAND, OR, and NOR gates and each gate column is able to provide AND (OR) in its direct and inverted format or in the same format with a FO2.

2-input 4-output balanced XOR/XNOR gates: Table I in Figure 2 presents the normalized magnetizations at the outputs O_1, O_2, O_3, and O_4 for C_1=C_2=0 and for different inputs combination $I_1I_2 = \{00\ 01\ 10\ 11\}$ for the balanced 4-output structure. Note that the cases $C_1C_2 = \{01\ 10\ 11\}$ results are exhibiting the same behaviour. Table I in Figure 2indicates that XOR and XNOR can be now implemented at all four outputs by making use of the same threshold value 0.38 obtained by averaging the normalized O_1, O_2, O_3, and O_4 magnetization for input combinations 01 and 11. To implement the XOR gate, the condition must be: if the normalized magnetization is larger than 0.38, then outputs equal to logic 0 and logic 1, otherwise. The XNOR gate can be captured by flipping the condition. Therefore, the structure can provide different combinations of XOR, XNOR and enable a fanout value up to 4.

C. Discussion

We evaluated the proposed 4-output PLG structure in terms of energy and delay, and compare it with state-of-the-art SW [10] and 16 nm CMOS [11] functionally equivalent designs. We followed the assumptions made in [10] to make a fair comparison: (i) SW excitation and detection cells are ME cells, which have an area of 48 nm $\times$ 48 nm, (ii) pulse signals are used to excite spin waves, (iii) No energy and delay are accounted for the output ME cell because the structures output are fed to the following SW gates, (v) 0.42 ns ME cell switching delay, C_{ME} = 1 fF, V_{ME} = 119 mV, Energy=$I \times C_{ME} \times V_{ME}^2$ (where I is the number of excitation cells), and SW $\lambda = 48$ nm, (vi) The SW propagation delay is negligible. Note that the made assumptions might not reflect the reality of the current spin wave based technology due to the early stage development of the technology, but their discussion is not part of this paper. Moreover, we assumed that AND, OR, XOR, and XNOR 16 nm CMOS logic gates constitute CMOS PLG. Also, the energy and delay numbers were estimated based on the energy and delay numbers for the logic gates, which were taken from [11].

Our evaluation results indicates that 16 nm PLG CMOS consume 923 aJ while having a delay of 0.047 ns whereas our 4-output structure consumes 57.6 aJ while having a delay of 0.42 ns ns. Also, the design in [10] consumes 43.3 aJ while having a delay of 0.42 ns. As it is clear, compared to 16 nm CMOS, the proposed gate is 11x slower and consumes 16x less energy. In addition, the design in [10] is performing slightly better in performance, but the Majority gate in [10] can provide maximally one output. Therefore, if more outputs are needed, the circuit must be replicated multiple times, thus needs more energy. For instance, when using the design in [10], if the output is needed 4 times the structure must be replicated 4 times leading to an energy consumption of 173 aJ. Our 4-output structure consumes 57.6 aJ, therefore it needs 3x less energy for the same computation without encoring any delay overhead.

V. Conclusions

In conclusion, a novel ladder shaped 2-input 4-output programmable logic gate structure was proposed. We introduced the gate structure and demonstrated that, by adjusting the gate output detection method, it can parallelly evaluate any 4-element subset of the 2-input Boolean function set {(N)AND, (N)OR, and X(N)OR}. Furthermore, we adjusted the structure such that all its 4 outputs produce SWs with the same energy and demonstrated that it can evaluate Boolean function sets while providing fanout capabilities ranging from 1 to 4. We validated our approach by instantiating and simulating different gate configurations such as 4-output AND/OR, 4-output XOR/XNOR, output energy balanced 4-output AND/OR, and output energy balanced 4-output XOR/XNOR by means of OOMMF simulations. We evaluated the performance of our proposal in terms of delay and energy consumption and compared it against existing state-of-the-art SW and 16 nm CMOS counterparts. The results indicated that, for the same functionality, our approach provides 3$\times$ and 16$\times$ energy reduction, when compared with state-of-the-art SW and CMOS implementations, respectively.

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References

[1] A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Cotofana, and S. Hamdioui, "2-output spin wave programmable logic gate," in *ISVLSI*, 2020, pp. 60–65.

[2] D. Mamaluy and X. Gao, "The fundamental downscaling limit of field effect transistors," *APL*, vol. 106, no. 19, p. 193503, 2015.

[3] A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui, and S. Cotofana, "Fan-out enabled spin wave majority gate," *AIP Advances*, vol. 10, no. 3, p. 035119, 2020.

[4] M. P. Kostylev, A. A. Serga, T. Schneider, B. Leven, and B. Hillebrands, "Spin-wave logical gates," *APL*, vol. 87, no. 15, p. 153501, 2005.

[5] A. Khitun and K. L. Wang, "Non-volatile magnonic logic circuits engineering," *JAP*, vol. 110, no. 3, p. 034306, 2011.

[6] T. L. Gilbert, "A phenomenological theory of damping in ferromagnetic materials," *IEEE Trans. Magn.*, vol. 40, no. 6, pp. 3443–3449, Nov 2004.

[7] A. Mahmoud, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Cotofana, and S. Hamdioui, "n-bit data parallel spin wave logic gate," in *DATE*, 2020, pp. 642–645.

[8] A. V. Chumak, A. A. Serga, and B. Hillebrands, "Magnonic crystals for data processing," *JP D: AP*, vol. 50, no. 24, p. 244001, 2017.

[9] M. J. Donahue and D. G. Porter, "Oommf user's guide, version 1.0," *Interagency Report NISTIR 6376*, Sept 1999.

[10] O. Zografos and et al., "Design and benchmarking of hybrid cmos-spin wave device circuits compared to 10nm cmos," in *IEEE-NANO*, July 2015, pp. 686–689.

[11] Y. Chen, A. Sangai, M. Gholipour, and D. Chen, "Schottky-barrier-type graphene nano-ribbon field-effect transistors: A study on compact modeling, process variation, and circuit performance," in *NANOARCH*, July 2013, pp. 82–88.

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