Beyond ADPLLs for RF and mm-Wave Frequency Synthesis

Watching out for new techniques: oversampling-reference and charge-sharing locking

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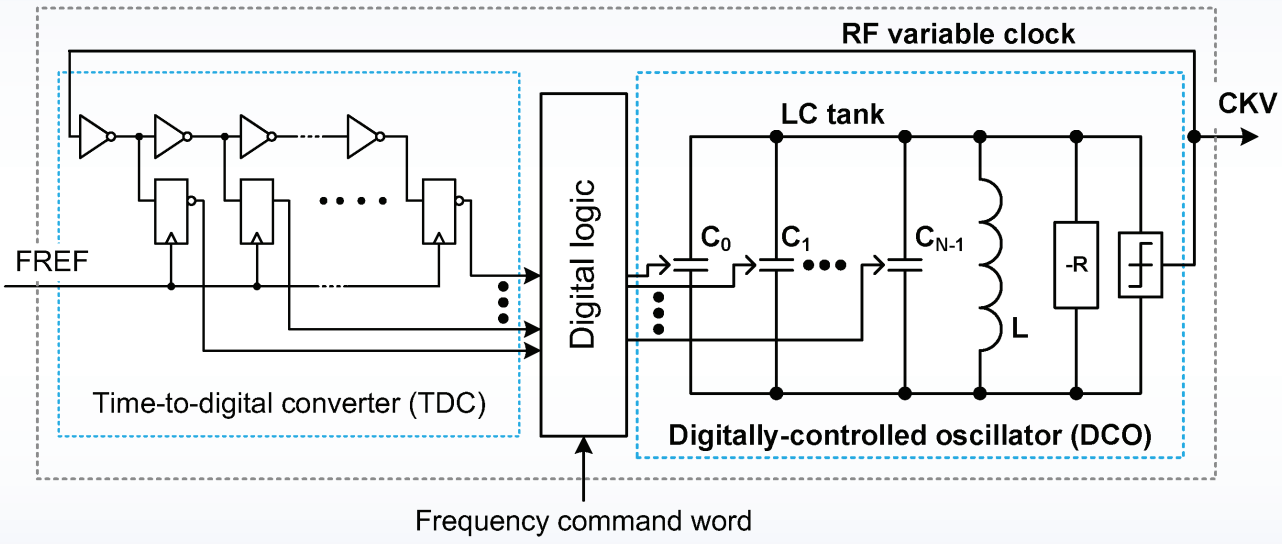

To address the relentless increase in data rates in wireless communication systems employing advanced modulation schemes, such as 5G frequency range (FR) 2 [see Figure 1(a)], generating mm-wave signals with minimal integrated phase noise (PN) or RMS jitter is of paramount concern [1]. Figure 1(b) specifies the required jitter to achieve the targeted EVM performance. For instance, for an EVM of less than 3.5%, as needed by a 256-QAM 28-GHz carrier, the RMS jitter contributed by the LO must be below 200 fs. As the carrier frequency or the symbol constellation density increases, the required RMS jitter becomes even more stringent. For example, 1024 QAM at 39 GHz demands an RMS jitter of <50 fs [2], [3], [4].

To reach such good performance, two major noise sources, i.e., the oscillator PN and noise associated with the phase detection mechanism in a PLL,

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should be carefully considered. Under the optimal loop bandwidth, the overall jitter should be equally contributed by the oscillator and PD. Note that the in-band (IB) PN of a PLL is typically dominated by its PD and the preceding reference path, i.e., the XO and its low-noise reference buffer [5], [6].

In this article, architectures of low-jitter RF and mm-wave PLLs, with special emphasis on ADPLLs, are reviewed. Finally, PLL benchmarking and the future outlook will be discussed.

PLL Architectures

To address the stringent jitter requirements of 5G systems, various techniques have been proposed in the past decade. Traditional analog charge pump (CP)-based PLLs targeting low jitter mainly rely on the precise design of high-current CP circuitry with accurate up/down current matching [I_1 and I_2 in Figure 2(a)] and large analog loop filter components (C_1, C_2, and R_1). Moreover, these issues become increasingly challenging in advanced CMOS nodes (e.g., below 28 nm) [7], [8], [9]. Additionally, in a fractional-N operation, the nonlinearity in the CP as well as in the PFD, exacerbated by the associated delta-sigma modulator (DSM), will result in a worse IBPN [10]. To overcome these difficulties, ADPLLs are often utilized, as they are more compatible with CMOS scaling [11], [12]. Additionally, digital calibration and compensation techniques can be easily employed to maintain performance across PVT variations [13]. However, the conventional ADPLL approaches often encounter RMS jitter constraints resulting from the resolution and linearity limitations of the inverter-delay-based TDC, which in turn leads to a less competitive IBPN and IB fractional spurs in 5G applications [14], [15].

In response, more complex phase detection methods, such as using a digital-to-time converter (DTC) to prealign the reference and variable clocks for the ultimate high-resolution (but short-range) detection, have been proposed [16], [17], [18], [19]. As another example, a subsampling (SS) PD leverages the high slew rate of the oscillator feedback signal by sampling it with sharp edges of the reference frequency (f_{ref}) clock [20], [21], [22]. This yields a high PD gain with extremely high resolution. However, due to the limited linearity of the oscillator waveform, the PLL may lose lock in the presence of oscillator perturbations [23], necessitating an additional frequency-locked loop (FLL) to ensure reliable locking [24]. Alternatively, a reference sampling (RS) PLL utilizes a frequency-divided signal from the oscillator feedback path to directly sample the reference sinusoidal XO waveform [25]. The wide linear range and limited slew rate of a typical low-cost XO (below 50 MHz) provide excellent locking robustness over a broad locking range. However, this introduces challenges related to resolving the issue of the low gain of the time-to-voltage conversion [26].

Due to the practical limitations in the PN performance of oscillators at mm-wave frequencies, a fairly large PLL bandwidth is necessary to achieve jitter below 100 fs. However, there is a tradeoff between the achievable PLL bandwidth and f_{ref}, and therefore, the authors of [27], [28], [29], and [30] take advantage of using rather "exotic" XOs with an extremely high reference frequency (e.g., >250 MHz). To keep the use of an inexpensive XO with ≤50 MHz, various reference multiplication techniques have been introduced. Unfortunately, these methods typically require an additional delay chain and calibration for the proper phase relationship, leading to increased power consumption and area [31], [32], [33]. Recently, a more efficient solution

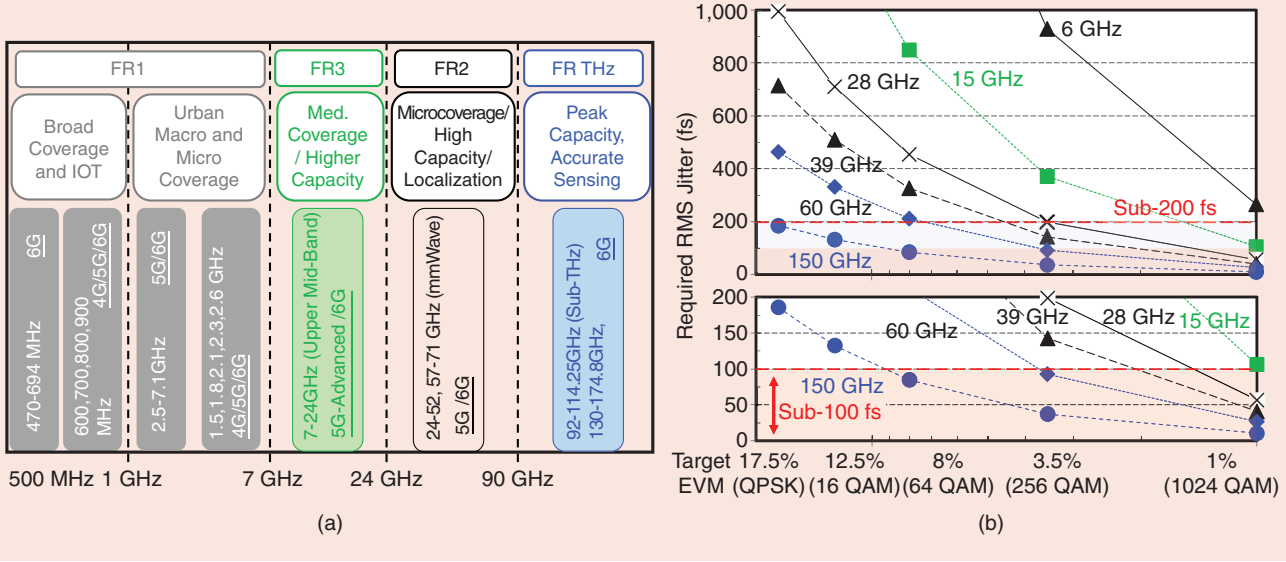

FIGURE 1: (a) 5G/6G communication standards at various FRs [FR1–FR3 and FR terahertz (THz)] and (b) the target RMS jitter for various types of complex modulation schemes and carrier frequencies.

points to the oversampling of the frequency reference waveform source, which can enhance the PD rate beyond FREF. This is achieved by not only locking at the zero-crossing points of the sinusoidal reference waveform but also by distributing the locking points across the entire reference period [34], [35], [36], [37], [38].

In the following section, we review the counter-based and DTC-assisted ADPLL architectures before discussing the evolution leading to the oversampling-based ADPLLs. We then conclude with implementation examples.

ADPLL

Figure 2(b) is a block diagram of the natively fractional-N ADPLL-based frequency synthesizer, which operates in a digitally synchronous fixed-point phase domain [39].[1] The variable phase signal PHV[i] is generated by counting the rising edges of the DCO's clock through a digital counter. For fine phase detection, a TDC measures and digitizes the phase difference (ϵ) between the reference clock (FREF) and the oscillator feedback signal (CKV). Meanwhile, the reference phase signal PHR[k] is derived by accumulating the frequency command word (FCW)[2] at each rising edge of the retimed FREF clock. The synchronous arithmetic PD computes the difference between the sampled variable phase and the reference phase to determine the phase error (PHE) PHE[k]. This can be mathematically modeled as $\mathrm{PHE}[k] = \mathrm{PHR}[k] - \mathrm{PHV}[k] + \epsilon$. The digital PHE is processed by a simple digital loop filter and then normalized by the DCO gain (K_{DCO}) to produce the oscillator tuning word (OTW). This approach ensures that the extensive digital logic is clocked after the quiet phase of the PHE detection by the TDC.

[1]Note that it is also common for digital PLL architectures to utilize a multimodulus divider (MMD) with a DSM in the feedback path to achieve the fractional-N operation [17], [18]. For a more detailed comparison between the two approaches, see [40].
[2]Historically, this is referred to as "N."

Figure 3 provides more details on how the reference phase PHR[k] (shown in green) aligns with the variable phase (shown in red) when the latter is perfectly locked, lagging, or leading against the former. For the sake of illustration, the FCW, which denotes the expected frequency multiplication ratio, is 3.2. Since the oscillation time period is an inverse of the oscillating frequency, there will be 3.2 clock cycles of CKV per single cycle of FREF. Also, we assume that the initial phase is zero (i.e., the FREF and CKV rising edges are aligned at time zero).

It can be observed that in the fractional-N operation, the fractional relation between the reference phase and the variable phase changes across one oscillator period. Therefore, this sets the required range for the fractional phase measurement via a TDC, which is the key component to ensure low quantization noise. The

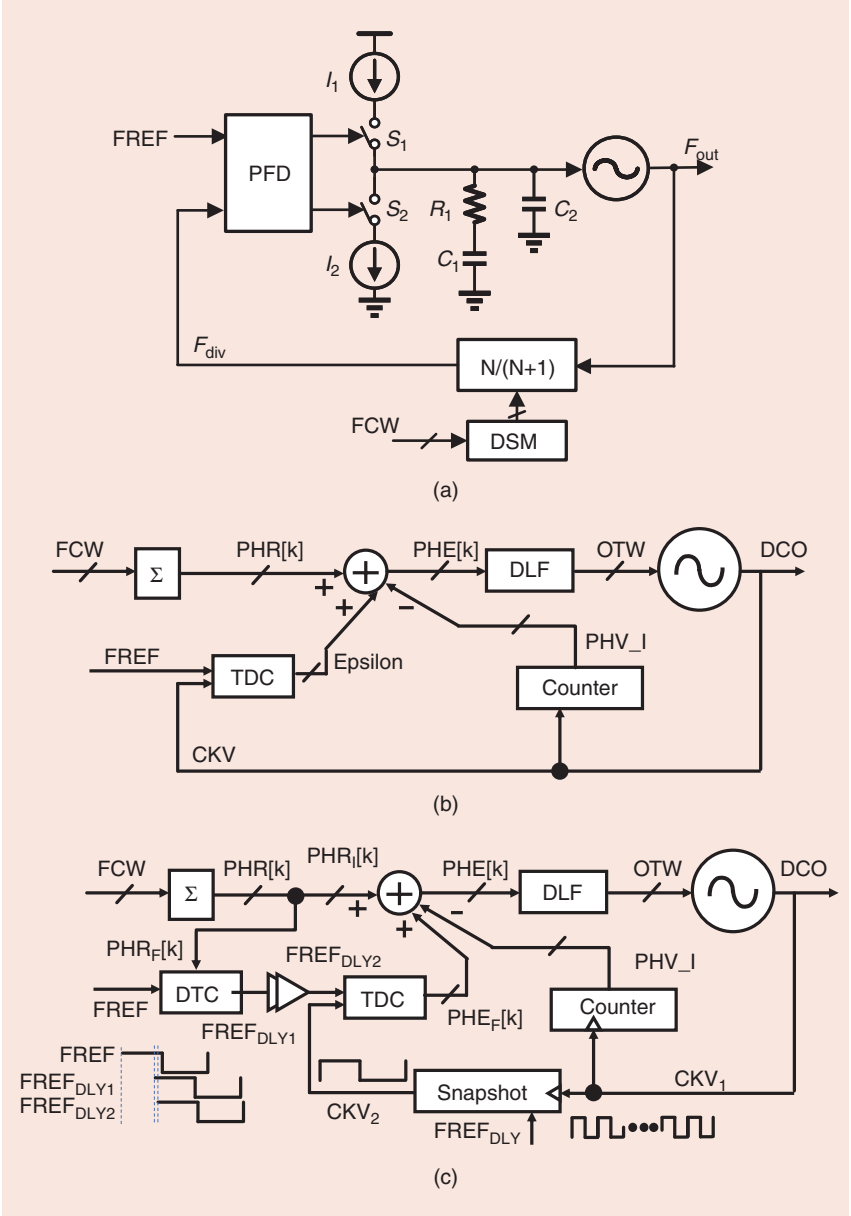

FIGURE 2: Simplified PLL block diagrams: the (a) conventional PFD/CP PLL, (b) counter-based ADPLL, and (c) ADPLL with digital-to-time converter (DTC) assistance to ease the TDC range. FCW: frequency command word; OTW: oscillator tuning word; PHE: phase error; DLF: digital loop filter.

IBPN due to the TDC quantization can be modeled as

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{\text{res}}}{T_V}\right)^2 \frac{1}{f_R} \qquad (1)$$

where $\mathcal{L}$ is the PN contributed by the TDC resolution Δt_{res} and T_V is the period of the DCO signal fed back into the TDC.

As shown in Figure 4, as the CMOS technology scales down from the 90-nm node to 28 nm, the typical resolution of a delay line-based TDC [39], [41] is reduced from 20 to 10 ps but can further go down to 2–3 ps in advanced FinFETs (and GAA nodes) [42]. This results in a reduction of the IBPN from −75 to −81 dBc/Hz when considering a 30-GHz carrier. However, to further lower the total RMS jitter below this limit, alternative techniques must be considered. In the past two decades, there have been various techniques proposed to lower Δt_{res}, e.g., Vernier delay lines, time amplifiers, and so on. The downside of such high resolution is the need to cover the whole oscillator period, resulting in either high power consumption or poor nonlinearity causing high fractional spurs.

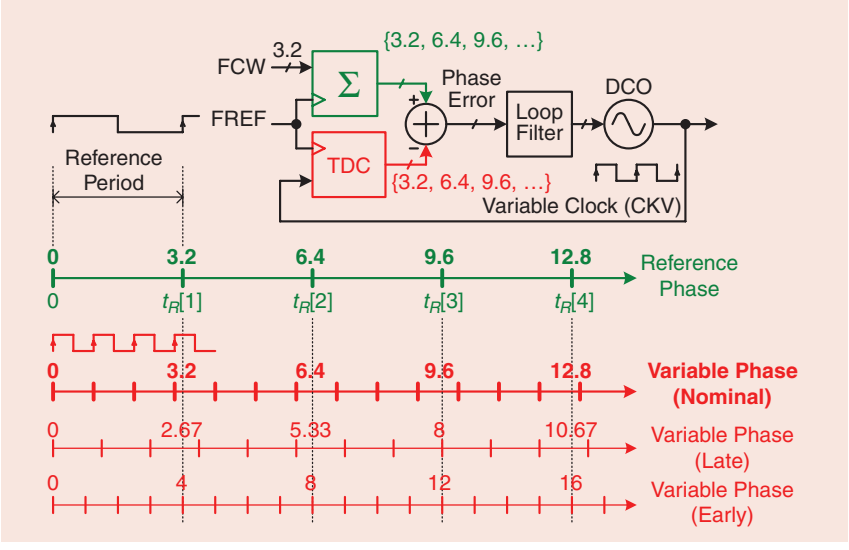

FIGURE 3: A conceptual block diagram of a phase-domain ADPLL with the evolution of phase signals.

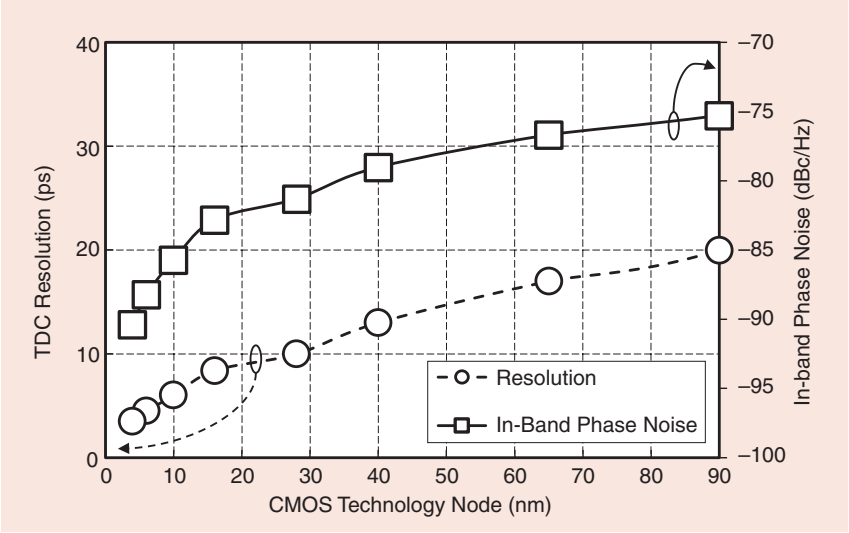

FIGURE 4: The theoretical IBPN limit of a 30-GHz carrier due to the TDC resolution of the corresponding CMOS technology nodes.

As a means to alleviate the above issue, Figure 2(c) illustrates a DTC-assisted ADPLL architecture. The DTC can be controlled by the fractional part of the accumulated reference phase ($\text{PHR}_F[k]$) to delay the edge of the reference clock ($\text{FREF}_{\text{DLY2}}$) in order to align it with the oscillator feedback signal (CKV). Note that due to the much higher rate of the oscillator feedback signal clock, a snapshot circuit is introduced to allow only the important edges of the feedback signal (i.e., CKV_2) to proceed to the TDC. This approach greatly reduces the required range of the TDC. However, achieving a high-resolution DTC with excellent linearity now becomes crucial [43], [44], [45]. Consequently, several new techniques, such as oversampling-based TDCs, have been developed.

Evolution of Phase Detection: From Sub-Sampling and Sampling to Oversampling

To achieve excellent jitter with high power efficiency, leading to a high FOM of a PLL, SS/bang–bang (BB) PDs have been promoted [24], [30], [46]. They exploit the intrinsically high time-to-voltage gain provided by the high slope of the oscillator waveform and sharp edges of the reference clock in order to reduce the PD noise, but at the expense of a narrow locking range [see Figure 5(a) and (b)]. As the sampling clock of the comparator input, the reference signal from the XO needs to translate its "gentle" sinusoidal waveform into sharp edges through an LNB, but that consumes significant power.

Alternatively, the XO waveform can be used directly as an input without requiring a buffer, while the sampling edge is generated from the divided oscillator output via a feedback clock generator (CG). This approach, known as the *RS-PD* [25], is examined in Figure 5(c) and (d). Although the PD gain from the input slope (K_{RSPD}) is lower, the phase detection range is significantly wider, allowing it to detect various disturbances

and enhance robustness against PVT variations. Additionally, compared to the SS approach, the slew rate requirement of the sampling clock is more relaxed.

To reduce the PD's noise contribution to the output, a higher reference frequency (f_{ref}) is typically employed, as it gives a lower N [6]. However, the 100–500-MHz XOs used for this purpose are rather expensive and consume excessive power. Another approach to boost the effective reference frequency with a standard-frequency XO calls for an additional reference multiplier (doubler/quadrupler/octrupler) [31], [32], [33] or cascaded PLLs [47]. This requires a duty cycle calibration (DCC) and/or additional circuits, which increase the overall power and area. Arguably, the best approach would be to extract the information contained in the reference sinusoidal XO waveform, S_{ref}, by sampling it by the oscillator clock edges [26]. This allows the possibility of increasing the PD rate, and consequently, N, by, for example, 4× oversampling, as in Figure 5(e) and (f) [34], [35], [37], [38], [48].

Figure 6 presents a detailed analysis of PN considerations associated with the SSPD and RS-PD when using a standard XO providing a sinusoidal waveform as the reference [2], [26], [49]. With an ideal clock edge of the sliced reference (CKR), the PD noise in the SSPD can be minimized to a negligible level [20]. This is achieved because the sampled thermal voltage noise and input-referred noise (IRN) of the gain stage G are converted

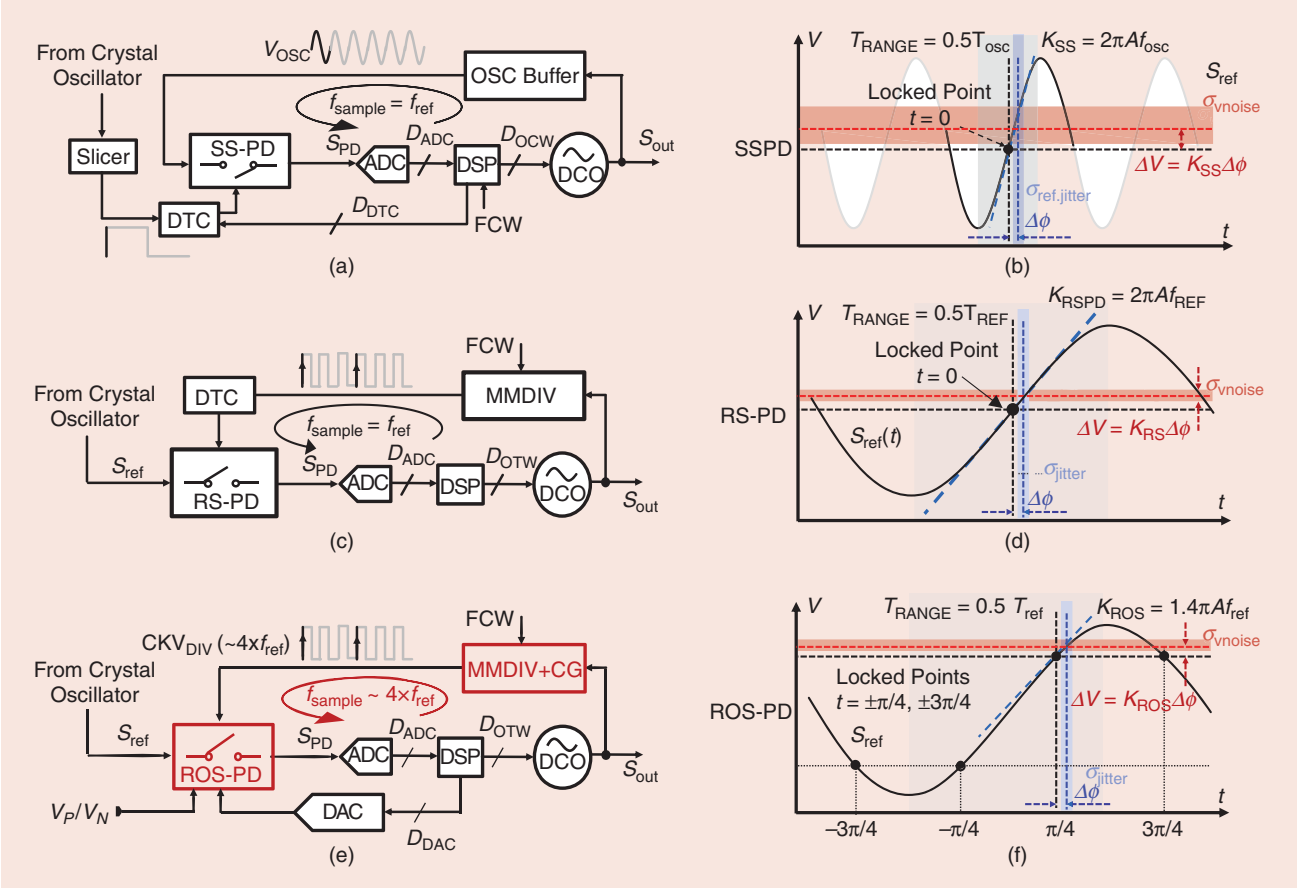

FIGURE 5: Simplified diagrams of digital PLL architectures using the (a) SSPD, (c) RS-PD, and (e) reference oversampling (ROS) PD, together with their corresponding PD characteristics of the (b) SSPD, (d) RS-PD, and (f) ROS-PD. CG: clock generator.

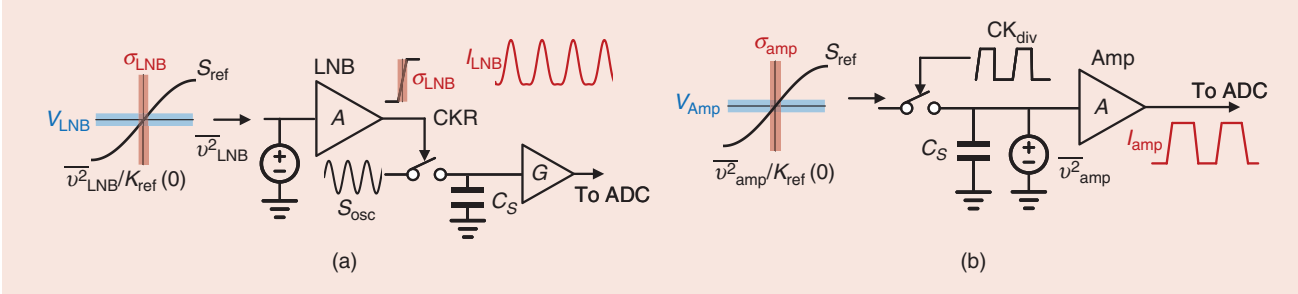

FIGURE 6: A comparison of PN contributions in the (a) SSPD and (b) RS-PD.

to time jitter via a steep slope of $2\pi A_{osc} f_{osc}$, where A_{osc} and f_{osc} represent the oscillator's amplitude and frequency, respectively. Note that the LNB plays an important role in translating the relatively slow sinusoidal input waveform into "super"-sharp clock edges for sampling, but considerations of the on-chip LNB are usually neglected in the literature. The IRN of the LNB ($\overline{v^2}_{LNB}$) can actually dominate the SSPD jitter, due to the gentle slope of $2\pi A_{ref} f_{ref}$, where A_{ref} is the reference waveform amplitude. The variance of timing uncertainty in the SSPD can be derived as

$$\sigma^2_{SSPD} = \frac{\overline{v^2}_{LNB}}{(2\pi A_{ref} f_{ref})^2} + \frac{KT/C_S + \overline{v^2}_{IRN\text{-}G}}{(2\pi A_{osc} f_{osc})^2}. \quad (2)$$

In contrast, in the RS-PD [Figure 6(b)], the sampling clock is obtained from an MMD in the oscillator feedback path (CK_{div}), which naturally features sharp edges. The reference sinusoidal waveform is now directly sampled on the sampling capacitor C_S without any buffer but at the expense of a slow slope of $2\pi A_{ref} f_{ref}$ of the incoming S_{ref}. To address this, an isolation buffer is employed with amplification A to help with the quantization noise downstream. The variance of timing uncertainty in the RS-PD can be derived as

$$\sigma^2_{RSPD} = \frac{\overline{v^2}_{amp} + KT/C_S}{(2\pi A_{ref} f_{ref})^2} \quad (3)$$

where $\overline{v^2}_{amp}$ is the amplifier's IRN. When using a sufficiently large capacitor C_S (in picofarads), its thermal noise can be neglected compared to the IRN of the LNB or amplifier.

The PN in radians ($\sigma^2_{\phi SSPD}$ and $\sigma^2_{\phi RSPD}$) can be obtained by normalizing with an oscillator period and multiplying by 2π. Further, the magnitude of PN spectra at the ADPLL RF output can be calculated by normalizing $\sigma^2_{\phi SSPD}$ and $\sigma^2_{\phi RSPD}$ by the phase detection rate f_{PD}, which is equal to the reference clock f_{ref} for the RS-PD. The output PN contributed by the SSPD and RS-PD can be derived as

$$\begin{cases} \mathcal{L}_{SSPD} \approx \dfrac{\overline{v^2}_{LNB}}{f_{ref}} \cdot \dfrac{f^2_{out}}{A^2_{ref} f^2_{ref}} \\ \mathcal{L}_{RSPD} \approx \dfrac{\overline{v^2}_{amp}}{f_{PD}} \cdot \dfrac{f^2_{out}}{A^2_{ref} f^2_{ref}}. \end{cases} \quad (4)$$

It can be observed that the jitter in both the SSPD and RS-PD can be dominated by the LNB and amplifier, respectively. For the output PN contributed by the RS-PD, the IRN of an inverter-based amplifier ($\bar{v}_{amp}$) adopted in [37] is 34.75 μV_{RMS} while consuming 122 μW. Considering an A_{ref} of 0.5 V, f_{ref} of 50 MHz, and f_{out} of 9.6 GHz, the theoretical IBPN can be estimated by (4), yielding –114.48 dBc/Hz. On the other hand, an inverter can operate as an LNB that converts a reference waveform into the RS edges used in the SSPD. Considering an f_{ref} of 50 MHz and an input swing of ~1 V_{pp}, the simulated PN shows a reference floor of around –160 dBc/Hz when consuming a similar power of 120 μW. Note that this level of PN at 50 MHz is equivalent to –114 dBc/Hz when it refers to an output frequency of 9.6 GHz. Therefore, it can be concluded that the jitter performance limited by either an LNB or amplifier in the SSPD and RS-PD is quite similar under the constraint of similar power consumption.

The RS-PD architecture has recently been gaining interest thanks to its natural capability of beneficially increasing the phase detection rate f_{PD} in (4) beyond f_{ref} [35], [36]. With an example of 4× oversampling, four points are chosen at $\pm\pi/4, \pm 3\pi/4$ positions on S_{ref}, which keep the PD gain (i.e., sampling slope) at $(1/\sqrt{2}) A_{ref} f_{ref}$. Taking advantage of the 4× PD rate, the output PN contributed by the reference oversampling (ROS) PD is

$$\mathcal{L}_{ROSPD} \approx \frac{\overline{v^2}_{amp}}{4 f_{ref}} \cdot \frac{2 f^2_{out}}{A^2_{ref} f^2_{ref}}. \quad (5)$$

The net result is a 2× improvement in jitter power compared to a single-sampling RS-PD. Table 1 summarizes the theoretical jitter and power consumption numbers in 1× sampling and 4× oversampling PLLs. Under the 4× ROS, the amplifier consumes 4× higher power. The amplifier amplifies the sampled voltage and charges the ADC's capacitor. This operation can be gated off outside of the tracking phase, thereby allowing power saving by a factor γ (e.g., 0.5). Comparing the FOM_{jitter} in Table 1, which is defined as $10\log_{10}(\sigma_t^2) + 10\log_{10}(P_{dc})$ [20], the first jitter term in the ROS-PD is lowered by a factor of 1/4 (1.25 dB), while the second power term is increased by $10\log_{10}(1+3\beta)$, where $\beta = P_{PD}/P_{dc}$ represents the fraction of the full PD path power to the total. For example, in [50], $P_{PD} \approx 0.22$ mW (PD,

TABLE 1. THE PERFORMANCE OF THE RS-PD (SINGLE SAMPLING) VERSUS THE ROS-PD (4× SAMPLING).

	SINGLE SAMPLING		4× OVERSAMPLING	
PARAMETER	**EQUATION**	**VALUE**	**EQUATION**	**VALUE**
$I_{D,RMS}$	$\gamma I_{D,RMS}$	I_1	$4\gamma I_{D,RMS}$	$4I_1$
σ_{amp}	$\frac{\bar{v}_{amp}}{2\pi A f_{ref}}$	σ_{amp1}	$\frac{\bar{v}_{amp}}{2\pi A f_{ref} \sin\frac{\pi}{4}}$*	$\sqrt{2}\sigma_{amp1}$
$\sigma_{\phi-amp}$	$\frac{\bar{v}_{amp} f_{out}}{A f_{ref}}$	$\sigma_{\phi-amp1}$	$\sqrt{2}\frac{\bar{v}_{amp} f_{out}}{A f_{ref}}$	$\sqrt{2}\sigma_{\phi-amp1}$
P_{PD}	$\gamma V_{DD} I_{D,RMS}$	P_{PD1}	$4\gamma V_{DD} I_{D,RMS}$	$4P_{PD1}$
σ_t^2†	$\sigma^2_{PD} + \sigma^2_{OSC}$	σ^2_{t1}	$\frac{1}{2}\sigma^2_{PD} + \sigma^2_{OSC}$	$\frac{3}{4}\sigma^2_{t1}$
P_{dc}	$P_{PD} + P_{HS}$	P_{dc1}	$4P_{PD} + P_{HS}$	$P_{dc1} + 3P_{PD}$

*The 4× oversampling PD samples the slope at four ±π/4 positions.
†Under optimum bandwidth, the jitter contributed by the PD and oscillator are equal.

ADC, digital) of the 1× sampling, and $P_{dc} \approx 12$ mW. As a result, the FOM_{jitter} improvement of 4× ROS can be $1.25 - 10\log_{10}(1 + 30.22/12) = 1.01$ dB.

Selected PLL Examples

RS-PLL

A system diagram of the featured RS-PLL appears in Figure 7(a). The outputs from the DCO are buffered to generate digital clock signals. One of them is divided by the MMD, whose phases are then resampled by standard-cell *D* flip-flops to eliminate the MMD noise. The CG produces S_{LO} and the three phases for the RS-PD switches. The S_{LO} signal carries the oscillator's phase information, decimated to a rate close to the reference frequency, and directly samples the reference XO's waveform through the bottom plate sampling capacitor. The sampled signal is then converted into voltage, representing the PHE, and amplified by the two-stage amplifier. A compact SAR-ADC digitizes the amplified signal, S_{RSPD}, into an 8-b digital output, D_{ADC}. In the DSP block, the PHE calculator converts D_{ADC} into D_{PHE}, applying dc offset compensation. The digital loop filter, implemented with proportional-integral (PI) control, uses adjustable α and ρ factors for optimization. The digital nature of the loop allows easy programming and optimization of the loop bandwidth and stability, which are crucial for minimizing the integrated jitter by fine-tuning the α and ρ parameters. The DCO decoder manages the DCO gain (K_{DCO}) and generates the OTW for the switched-capacitor banks, helping to minimize the DCO PN.

The circuit implementation of the RS-PD is depicted in Figure 7(b). The reference sinusoidal waveform (S_{REF}) from the XO is directly sampled by the high-speed bootstrap switch, triggered by the divided oscillator edges from the CG block. The left and right plates of the bottom-plate sampling capacitor $C_S = 2$ pF are preset to the common-mode voltage (V_{cm}) and threshold voltage (V_{th}), respectively, both of which are automatically generated by a self-bias inverter with a minimum transistor width and the same length as used in the G_{m1} stage. The preset switches are implemented using CMOS transmission gates to ensure low on-resistance.

As mentioned earlier, the sampled signal must be amplified prior to digitization to compensate for the low time-to-voltage gain (K_{RSPD}), which is due to the slow slope of the reference signal. This amplification is handled by the two-stage amplifier (G_{m1} and G_{m2}). For an accurate voltage transfer during the bottom plate sampling, the input parasitic capacitance of G_{m1} must be kept small, limiting the gain of the first stage. Additionally, input node B of G_{m1} carries voltage information

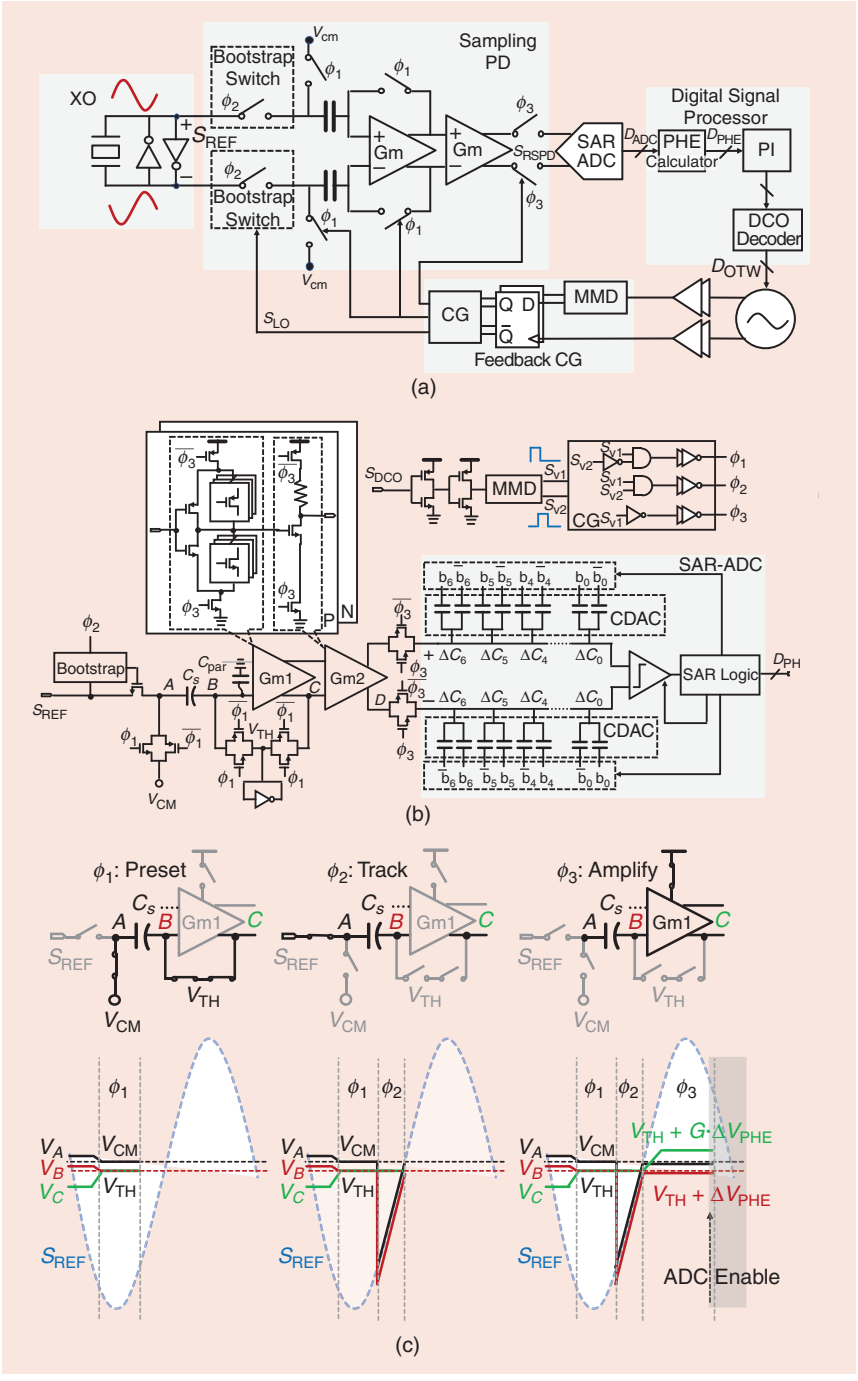

FIGURE 7: An RS ADPLL: the (a) top-level diagram, (b) schematic of the RS phase digitization, and (c) timing diagram of the sampling phases.

Generating mm-wave signals with minimal integrated phase noise or RMS jitter is of paramount concern.

derived from S_{DCO}, which has a low transfer gain due to the slope of S_{REF}. This imposes a strict noise constraint, necessitating a low IRN for G_{m1}. An inverter-based structure is employed for G_{m1}, with the transistor length optimized to 120 nm to minimize the flicker noise and achieve a low IRN. Eight parallel PMOS and NMOS units are used to control both the gain (~6) and the output common-mode voltage. Additionally, power saving functionality is integrated through gated PMOS and NMOS transistors controlled by $\bar{\phi}_3$ and ϕ_3. With this gated design, G_{m1} consumes less than 60 μW while maintaining a low IRN of 122 μV_{RMS} when integrated up to 160 MHz, corresponding to an IBPN limit of –122 dBc/Hz. The second stage, G_{m2}, is a common-source amplifier that provides higher gain and improved driving capability to charge the CDAC in the subsequent SAR-ADC stage. Since G_{m1} dominates the overall IRN, G_{m2} is designed with a minimum transistor length of 30 nm to enhance the settling speed. It delivers a gain of 10 when driving a 120-fF CDAC load, with a settling time of under 5 ns. In addition, G_{m2} incorporates gated PMOS and NMOS switches at the top and bottom to reduce the power consumption. Once the amplified signal has fully settled on the bottom plates of the CDAC, two CMOS switches between G_{m2} and the 8-b SAR-ADC open, initiating the ADC's conversion process. It is worth noting that even in the presence of significant frequency perturbations, the sampled voltage remains within a large monotonic range centered around the locking point. Even at the saturation point, the loop will maintain the proper negative feedback for accurate phase and frequency tracking, unlike in the prior art, such as [2] and [20].

The Reference Sampling process consists of three operational phases, as depicted in Figure 7(c). When operating at an f_{ref} of 80 MHz, ϕ_1 provides a ~4-ns window to preset the voltages on the top and bottom plates of C_s. During this phase, V_A is set by the common-mode voltage V_{CM}, and V_B is set by V_C, which is self-biased at the threshold voltage (V_{th}) of G_{m1}. This configuration helps to eliminate any offset caused by mismatches between the common-mode voltage of S_{ref} and the threshold voltage of G_{m1}.

The second phase (ϕ_2) is for tracking, during which there is a 2-ns window that allows V_A to follow the input waveform S_{ref} The bottom plate sampling operation ensures that V_B tracks the changes in V_A. Once ϕ_2 is complete, the sampled voltage held at V_B (on the ground capacitance of the bottom plate of C_S at node B) represents the voltage $V_{th} + \Delta V_{PHE}$, where ΔV_{PHE} contains the PHE information translated from the time-to-voltage conversion at the sampling instant $0 + \Delta\phi$

In the final phase, ϕ_3, V_C is amplified and settles at $V_{th} + G_1 \cdot \Delta V_{PHE}$. MM] The second-stage amplifier G_{m2} further amplifies this signal with an additional gain G_2 at node D before charging the CDAC capacitors in the SAR-ADC. The ADC enable signal, triggered by ϕ_1, initiates the ADC conversion process. It is critical to ensure that the end of ϕ_2, which marks the time-to-voltage conversion, is not interrupted by any other phase. To prevent any such interference, a small delay is introduced at the rising edge of ϕ_3. Additionally, the CMOS switches preceding the SAR-ADC must open before the shutdown of G_{m2} during phase ϕ_3.

The proof-of-concept RS-PLL was fabricated in Taiwan Semiconductor Manufacturing Company (TSMC) 28-nm LP CMOS. A standard external 80-MHz XO was employed as the reference. The output PN at 2.4 GHz, corresponding to a frequency multiplication factor of $N = 30$, shows that the optimal bandwidth is around 2 MHz, and the IBPN reaches –115 dBc/Hz. The integrated jitter, measured from 10 kHz to 30 MHz, is 355 fs. Additionally, the main reference spur measures –60 dBc. The total power consumption is 1.1 mW. The passive sampling switches and gated operation in the G_m stages consumes a low power consumption of 120 μW. The compact-sized SAR-ADC consumes 60 μW while operating at 80 MHz. The RS-PLL remains locked even under a DCO supply modulation ranging from the original 0.2 up to 0.6 V, demonstrating the architectural robustness, without requiring any additional FLL.

ROS-PLL

By sampling more points along the accurate sinusoidal waveform S_{REF} of the XO, we can increase the PLL's phase correction rate beyond the reference frequency, f_{ref} A higher oversampling ratio ($M = f_{sample}/f_{ref}$) can expand the loop bandwidth, accelerating the locking process and reducing the IBPN contributed by the PD. An oversampling ratio of $M = 4$ [see Figure 5(f)] is a balance between the direct sampling [$M = 1$ in Figure 5(c)] used in [26] and other conventional PLLs/ADPLLs and an excessively high M, which could lead to 1) variations in the oversampling PD gain (K_{ROS}) across the reference waveform, with the gain peaking at zero crossings and dipping near peaks/troughs; 2) a reduced monotonic PD range; and 3) increased power consumption.

The 4× ROS-PD results in four locking points with a phase increment of $2\pi/4$ in an integer-N operation. In a fractional-N mode, the sampled voltage tracks the entire extent of S_{REF}. Consequently, the next-stage quantizer would normally need to handle the full-scale ~1-V input range, necessitating an extremely high-resolution ADC to achieve a low IBPN. Such a high-resolution ADC would require significant power, especially at conversion speeds in the hundreds of megahertz.

To avoid the above issue, a bottom plate sampling circuit (similar to the

one used in the RS-PD) is now assisted by a voltage zero-forcing technique, as in Figure 8. This technique relaxes the required range by removing the dc offset, i.e., $\pm A\sin(\pi/4)$, at each locking point by means of V_P and V_N. Additionally, a fine-resolution/small-range CDAC, placed at the top plate, can be programmed to further compensate for any fractional voltage residues. The net result is that the voltage on the top plate (right side) of C_S represents the ideally bias-free PHE, proportional to $K_{ROS} \cdot \Delta\phi$. Since the required input range is much smaller, the requirements on subsequent circuits can be relaxed to achieve low noise while maintaining low power.

The operation of the ROS-PD, which is at the heart of the ROS-PLL in Figure 9(a), occurs in three distinct phases, as demonstrated in Figure 9(b). In the first phase, ϕ_1, having a clock pulsewidth of 1.3 ns, presets node A to the expected S_{REF} of 0.85 V (i.e., V_P) and node B to a V_{TH} of 0.5 V. At the end of this presetting phase, the voltage across the top and bottom plates of C_S is 0.35 V. In the second phase, ϕ_2, a brief pulse of approximately 0.7 ns allows the bottom sampling (BS) circuit to track the incoming S_{REF}. This action charges the capacitance at node A, which primarily comprises the CDAC input. While the charge on C_S remains conserved, the voltage at node B tracks the S_{REF} trajectory with the previously established offset of 0.35 V. Simultaneously, A_1 amplifies the voltage at node B with a gain of 15. The third phase, ϕ_3, halts the input tracking to establish the sampling point. To adjust for a fractional-N operation, the DSP alters the CDAC code to modify the load capacitance at node A, allowing the voltage at nodes A and B to be programmed to eliminate any voltage residue. At the same time, the second-stage amplifier, A_2, drives the 6-b SAR-ADC and amplifies the sampled voltage from the input CDAC of the SAR-ADC. This phase is allocated a duration of 3 ns.

The showcased 4× ROS-ADPLL was realized in TSMC 28-nm LP CMOS. The

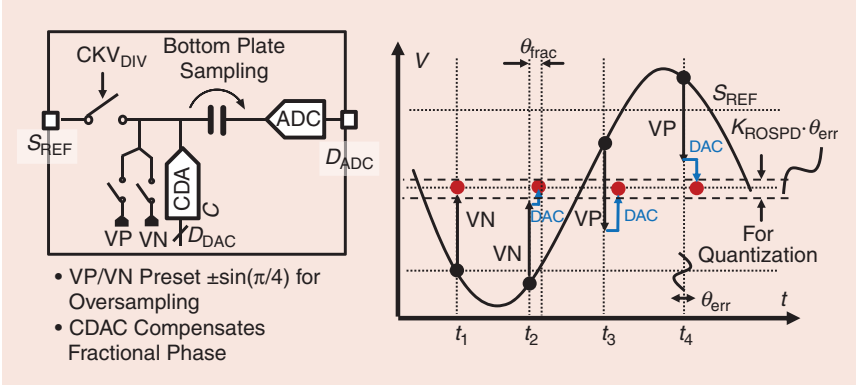

FIGURE 8: Reference waveform oversampling using bottom plate (over) sampling with zero forcing [26], [37], [38].

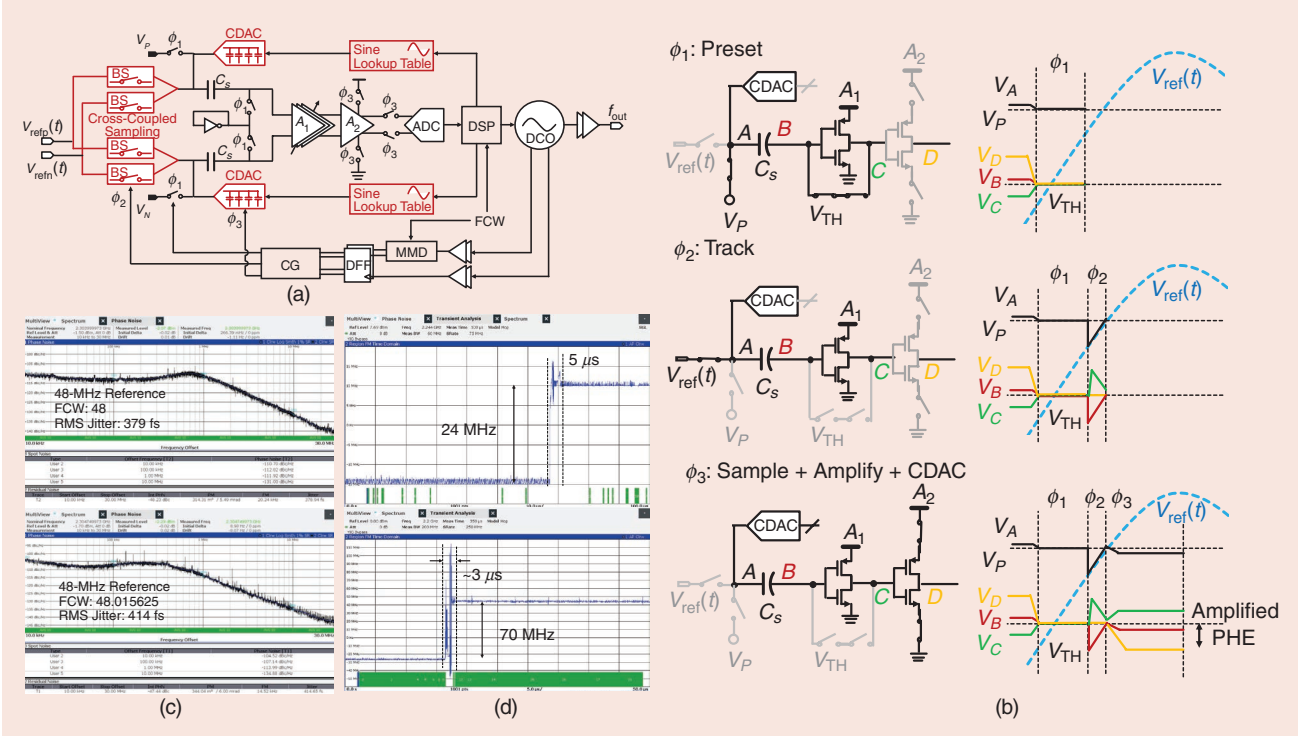

FIGURE 9: The ROS-PLL: the (a) top-level diagram, (b) timing diagram of the sampling process, (c) measured PN in integer-*N* and fractional-*N* operation at 2.2 GHz, and (d) measured transient locking.

oscillator accounts for the majority of the ADPLL's active area, occupying 0.16 mm^2 out of the total 0.24 mm^2. Due to the large bandwidth provided by the 4× oversampling of f_{ref}, the PN requirement of the DCO is less stringent, allowing for power savings. Specifically, the DCO and its buffer consume only 380 μW. The MMD and clock generation circuits use 200 μW while operating at a CKV_{DIV} rate of 200 MHz. The ROS-PD, which includes bootstrapped switches, low-noise amplifiers A_1 and A_2, CDAC buffers, and other passive switches, consumes 300 μW at 200 MHz. Overall, the total power consumption of the ADPLL is just 1.15 mW. In an integer-N operation, this 4× ROS-ADPLL was tested with a 48-MHz reference frequency and FCW_I of 48. Figure 9(c) presents the PN plot at 2.304 GHz. The IBPN is as low as –113 dBc/Hz, with an integrated RMS jitter of 379 fs over the 10 kHz to 30 MHz range. For a fractional-N operation, the PN at a carrier frequency of 2.30475 GHz, with an FCW of 48.015625, is also shown in Figure 9(c). With optimal bandwidth settings, the integrated RMS jitter is 414 fs. With a power budget of ~1 mW, this results in one of the best FOMs for jitter, FOM_{jitter}, of 247 dB among fractional-N ADPLLs consuming less than 5 mW. The wide monotonic PD range of this architecture eliminates the need for an FLL, which is typically required in SS-PLLs for locking robustness and fast settling. This is validated by the transient measurement results in Figure 9(d). Under a 1-MHz loop bandwidth, the ADPLL settles to a new frequency 24 MHz away within 5 μs. Increasing the loop bandwidth to approximately 5 MHz reduces the settling time to 3 μs for a 70-MHz frequency step. The measured relocking behavior aligns well with simulation results, demonstrating the robustness of the system. Consequently, this architecture's inherent phase and frequency tracking can effectively counter various environmental perturbations, such as supply and temperature variations or interference from strong power amplifiers.

mm-Wave ROS-PLL

The presented architecture has been adapted to support mm-wave frequencies, as described in Figure 10(a). The reference waveform (S_{REF}) is likewise directly oversampled by the divided oscillator clock (the outputs of CG) using cross-coupled bottom plate sampling switches. A programmable PI controller functions as a loop filter and tunes the 30-GHz class F_{23} DCO with a third-harmonic extractor (H3E). The DCO provides a fundamental 10-GHz component to the ÷4 frequency divider, MMD, and CG, which produces the clocks for the ROS-PD and digital blocks. A schematic of the class F_{23} oscillator

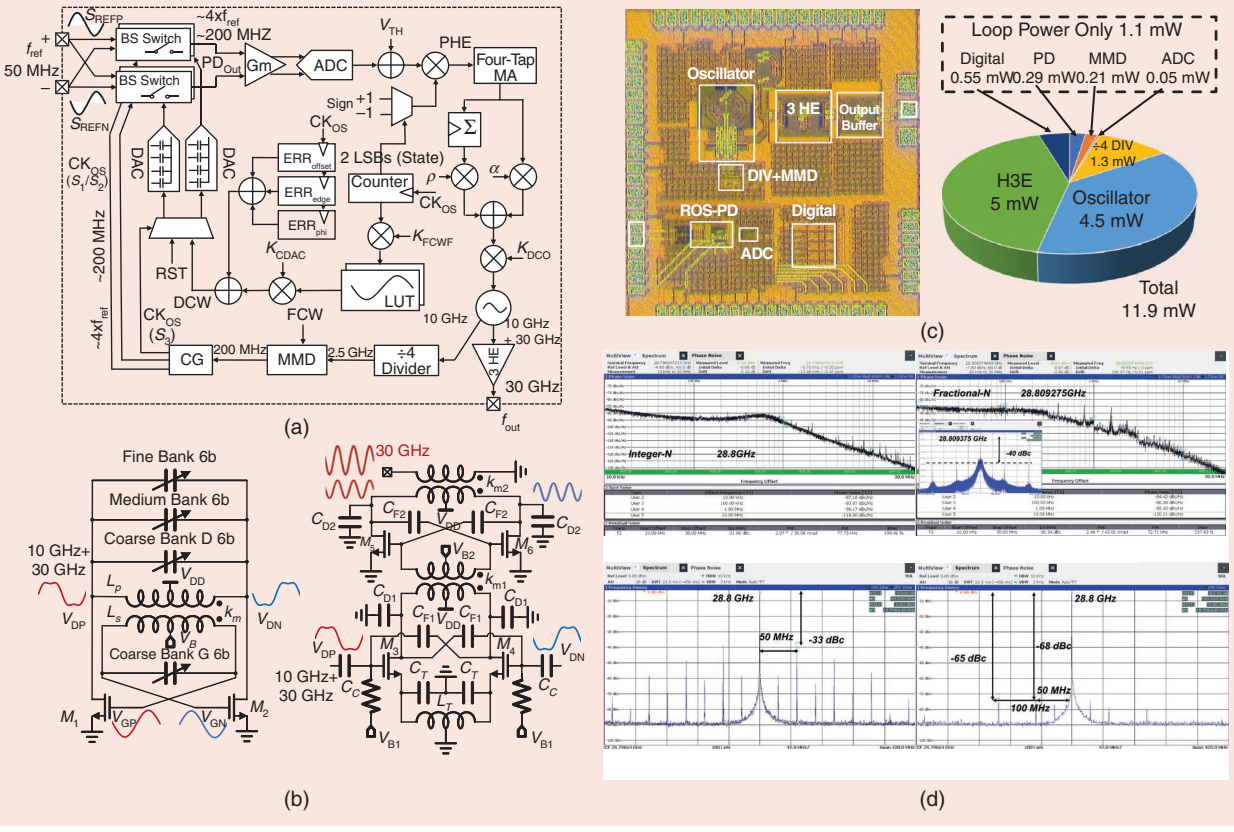

FIGURE 10: The mm-wave ROS-ADPLL (mm-wave ROS-PLL): the (a) top-level block diagram, (b) schematic of the mm-wave oscillator and its harmonic extractor, (c) chip microphotograph and breakdown of the measured power consumption, and (d) measured PN and spectrum. MA: moving average; RST: resit; DCW: digital-control word.

is presented in Figure 10(b), which includes the H3E and a second-stage output buffer designed to drive a 50-Ω load [52], [53]. The source inductor L_T in the H3E is tuned to resonate at 10 GHz, effectively filtering out the fundamental harmonic current. The 10-GHz signal from the oscillator gate node is divided by two ÷2 dividers to produce a 2.5-GHz signal with high reliability.

The mm-wave ROS-ADPLL is also implemented in 28-nm CMOS, covering an active area of 0.3 mm^2 and consuming just 11.9 mW, with 80% of this power allocated to the DCO and H3E [see Figure 10(c)]. The measured PN and spectral plots are given in Figure 10(d). With a 50-MHz reference input, the system achieves an RMS jitter of 199 fs in the integer-*N* mode and 237 fs in the fractional-*N* mode when synthesizing a 28.8-GHz carrier. By enabling the digital calibration loop, reference spurs and their harmonics can be reduced by 32 dB, bringing them down to −65 dBc [38]. In the fractional-*N* mode, the typical fractional spur is −40 dBc. The ADPLL's wide PD range allows it to settle within 15 μs after a 62-MHz frequency jump, demonstrating the robustness of the design. This system achieves exceptionally low jitter and power consumption for ADPLLs operating above 10 GHz, using a standard 50-MHz reference—the lowest among recent state-of-the-art PLLs/ADPLLs. Without relying on high reference frequencies or additional cascading PLLs, this ADPLL delivers an FOM of −241.7 dB and a record $FOM_{jitter\text{-}N}$ [54] of −269.3 dB for mm-wave ADPLLs.

Charge-Sharing Locking PLLs

An entirely different technique of exploiting a digitally friendly approach to simultaneously achieve ultralow jitter, low power consumption, and robustness is revealed in Figure 11(a). A new technique of charge-sharing locking (CSL) with an implicit digital frequency tracking loop (FTL) exploits a minimalistic SAR-ADC (0.1 mW). In contrast to the conventional subharmonic injection locking (IL), in which the switch is used to preset the oscillator waveform to the ac ground,[3] a sharing capacitor C_{share} (1 pF) with a DAC-controlled preset voltage is employed for charge sharing with the resonant *LC* tank (realizing a phase-correcting proportional path), while the resulting charge residue on C_{share} (which mainly represents the frequency error after the charge sharing) is then sampled and processed by the digital FTL (including a SAR-ADC, an IIR filter, and an integrator) for frequency tracking (integral path). The CSL technique offers the following advantages: 1) thanks to the C_{share} recording of how much charge was used to correct the PHE caused by the frequency error and intrinsic DCO PN, the timing–race problem can be effectively mitigated; 2) the SAR-ADC-based digital FTL consumes ultralow power and occupies a tiny area; and 3) the fine switched-capacitor tuning bank in the DCO is used only for frequency tracking rather than phase correction in the ADPLL or digital SS-PLL, thus relieving the tough requirements on the resolution, usually requiring a high-speed DSM, and the linearity of the switched capacitor. The timing diagram is in Figure 11(b). First, C_{share} is preset by the DAC (when the reference pulse is high and S_1 is on). After that, S_1 is off, and S_2 is on. This results in a charge injection into the oscillator (when the clock signal–CSL is high). Figure 11(c) shows the effect of charge-sharing injection on the oscillator's phase when there is a frequency mismatch. The leftover charge on C_{share} is fed back to the SAR-ADC to ensure that the intrinsic frequency of the oscillator (f_{osc}) is equal to $N \times f_{ref}$. Thus, a robust locking operation can be ensured. The prototype in [55] achieves a low RMS jitter of 75 fs at 26.25 GHz, while the reference spur is −45 dBc at a 250-MHz offset. The total power consumption of the whole system is 16.5 mW.

> ***As the carrier frequency or the symbol constellation density increases, the required RMS jitter becomes even more stringent.***

Despite the low RMS jitter achieved, the realized prototype in [55] still requires manual calibration of the pulsewidth (τ_{pulse}), due to its sensitivity to PVT variations. A narrow pulse may reduce the injection time, leading to a lower bandwidth, while a wider pulse increases the time that the *LC* tank is loaded by C_{shared}, complicating the performance optimization at mm-wave frequencies. To address these challenges, a ping-pong (PP) CSL technique was introduced in [56] and is illustrated in Figure 12(a). Instead of relying on the narrowest achievable τ_{pulse}, this technique uses a 50% duty cycle reference clock (ϕ_1) and its complement (ϕ_2) in a ping-pong manner. During each clock phase, either C_{shared} or C'_{shared} connects to the *LC* tank, thereby minimizing loading variation. The extended duration of the charge-sharing operation, due to a longer τ_{pulse}, improves the injection efficiency independent of the *RC* time constant of C_{shared}, resulting in a wider achievable bandwidth. The charge residues on the disconnected capacitor can be read out during ϕ_1^s (or ϕ_2^s) to gather the oscillator state information. This information can then be used for the DCC and FTL. The PP operation inherently provides a 2× reference multiplication without the need for explicit multiplier circuitry operating directly at 2× f_{REF}, thus reducing the IBPN of the PLL. Additionally, the common-mode

[3]Since traditional IL requires an ac ground (either single ended or differential) to inject the adjusting signal, it can natively support only an integer-*N* operation (unless assisted by an additional DTC). On the other hand, CSL can allow an injection at any point along the voltage waveform, and thus, it can inherently support the fractional-*N* operation.

precharging DAC found in prior designs is replaced by simply connecting the complementary phases of the PP operation during ϕ_1^R(or ϕ_2^R), which enables automatic common-mode acquisition. A detailed timing diagram and corresponding phase relationships are shown at the bottom of Figure 12(a).

Figure 12(b) presents a chip micrograph of this PLL fabricated in TSMC 28-nm HPC+ CMOS, with an active area of 0.21 mm^2. The measured PN demonstrates a lower RMS jitter of 42 fs (integrated from 10 kHz to 30 MHz) using a 250-MHz reference. The measured spur is –60 dBc at an offset of f_{ref} around the 27-GHz carrier, highlighting the effectiveness of the employed FTL and DCC calibration when compared to the spur level of –29 dBc without any calibration. The PLL consumes only 14 mW, with 90% of this power allocated to the DCO and H3E. The low-noise reference path and calibration loop, including the FTL, consume only 1 and 1.2 mW, respectively. This results in an FOM_{jitter} of –256.3 dB.

PLL Benchmark and Future Outlook

To fairly benchmark the performance of low-jitter PLLs, the work in [6] has proposed a PLL FOM defined

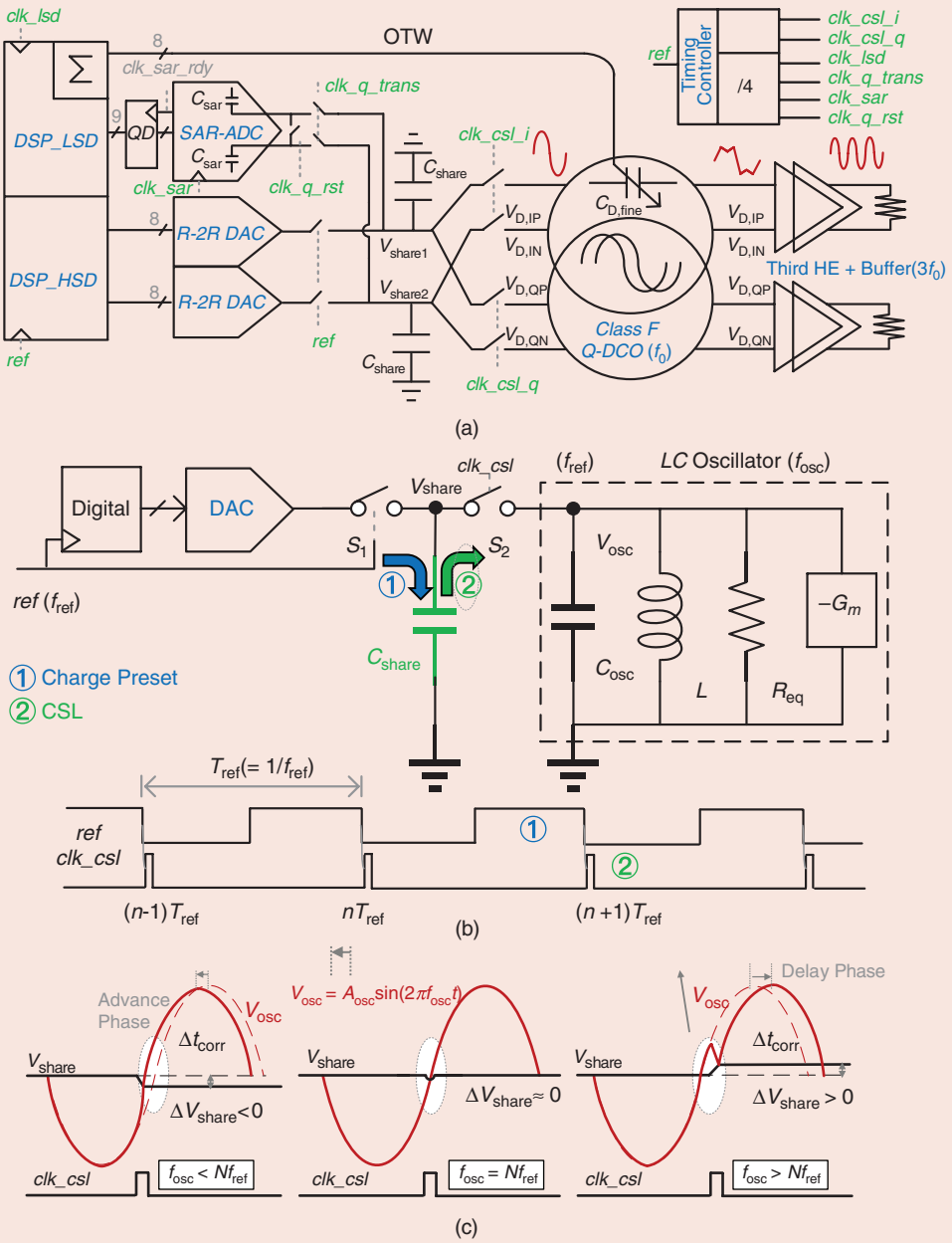

FIGURE 11: A charge-sharing locking (CSL) PLL [55]: the (a) top-level diagram, (b) timing diagram of the CSL operation, and (c) oscillator waveform after the CSL injection applied. LSD: low-speed digital; HSD: high-speed digital; HE: harmonic extractor.

as $20(\log_{10}(\sigma_t/1s)) + 10(P_{dc}/1mW)$, where σ_t and P_{dc} are the integrated PN or RMS jitter and power consumption, respectively. Figure 13(a) surveys the jitter variance versus the power consumption of integer-*N* PLL/ADPLLs. In the past two decades, various techniques have been proposed to push the PLL FOM performance. It can be observed that integer-*N* PLLs adopting the SSPD with the higher slew rate of the PD input signal, either from the reference clock or oscillator feedback path, can achieve a high PD gain with low intrinsic noise, which leads to an exceptional FOM of below −250 dBc/Hz [57], [58], [59]. Alternatively, CSL PLLs also show competitive FOM performance due to the improved injection efficiency and low latency [55], [56]. Recently, approaches using ROS techniques [34], [36], [37] have gained interest and offer plenty of room to push the FOM limit while maintaining the reference frequency below 100 MHz.

For fractional-*N* PLLs [see Figure 13(b)], it can be observed that most of the high-performance ADPLLs adopt the DTC-assisted architecture with the BB-PD but with the reference above 200 MHz [33], [45]

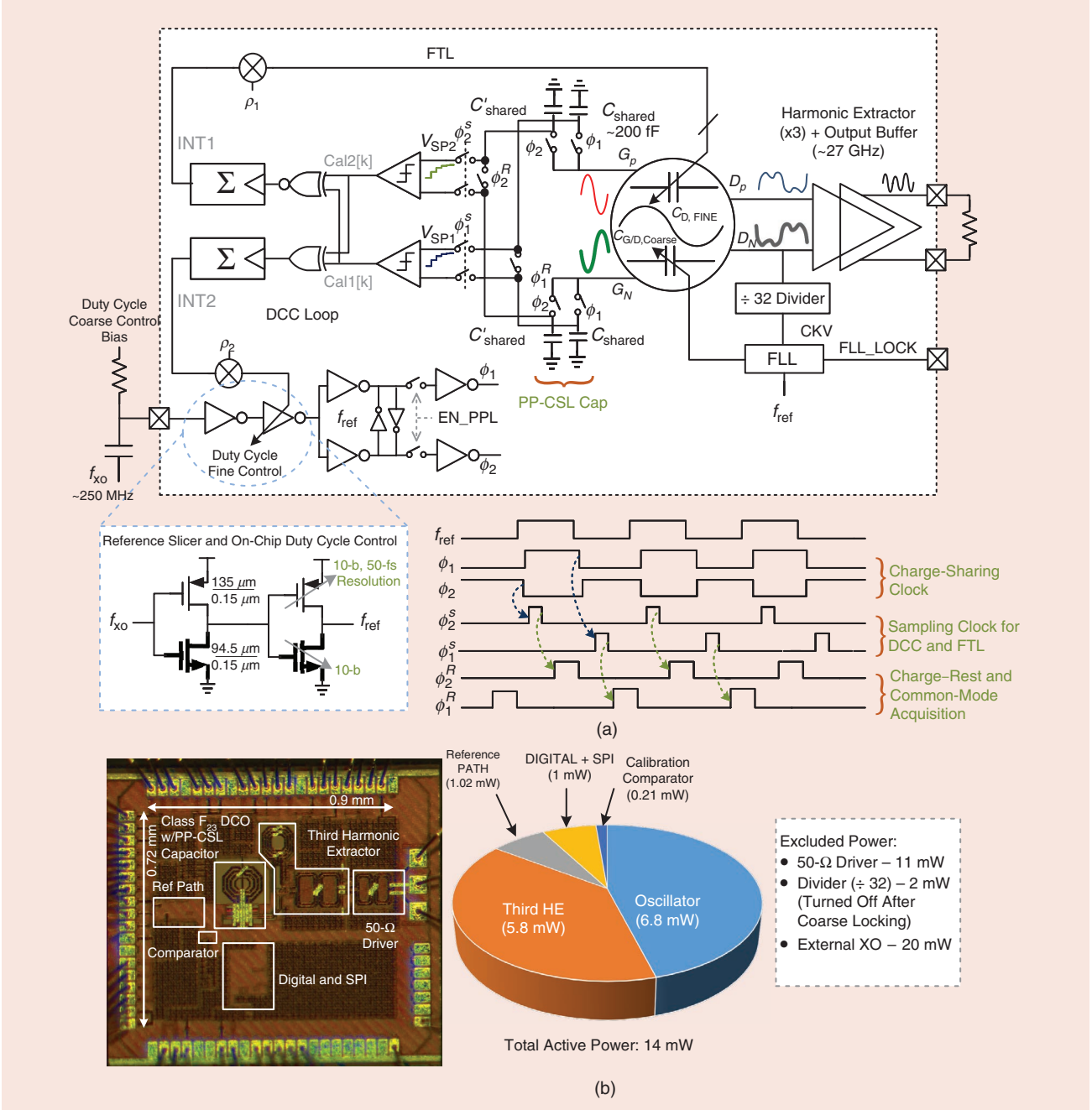

FIGURE 12: A PP CSL-PLL (PP-CSL) [56]: the (a) top-level diagram and its clocking scheme and (b) chip photo and measured power breakdown.

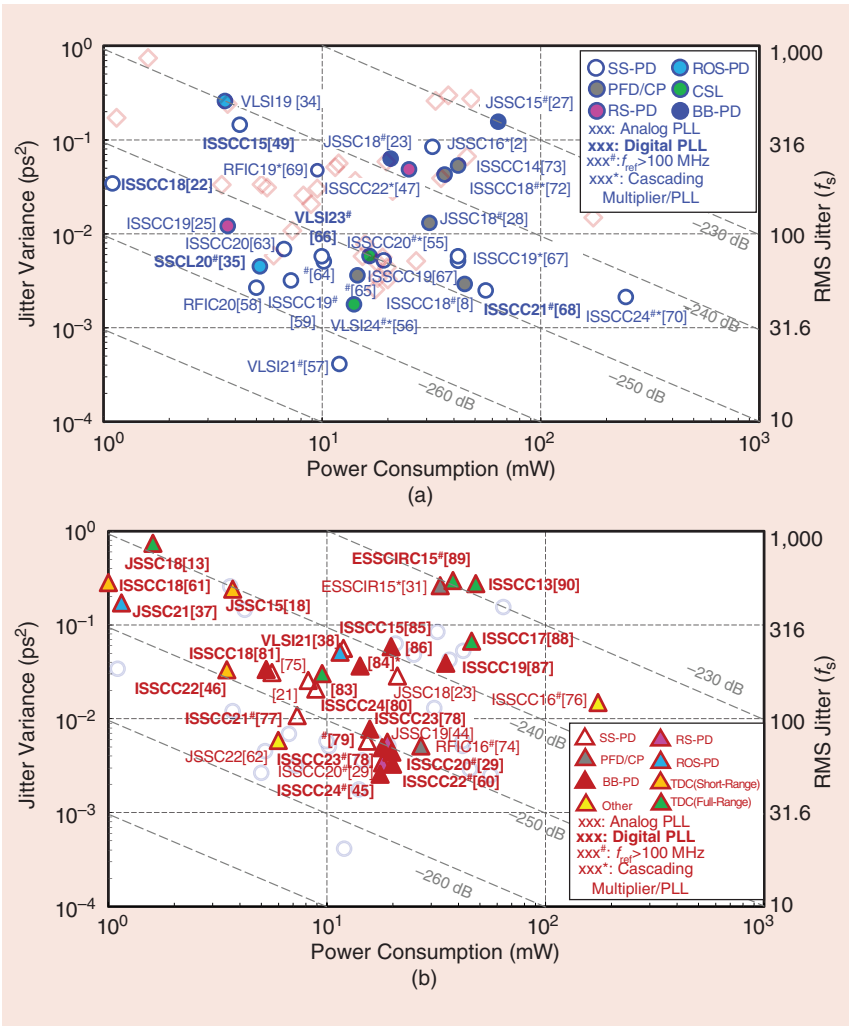

FIGURE 13: PLL/ADPLL benchmarking in terms of the jitter variance (σ^2) versus the power consumption in (a) integer-*N* and (b) fractional-*N* operation. VLSI: Symposium on VLSI Technology and Circuits; *JSSC*: *IEEE Journal of Solid-State Circuits*; ISSCC: IEEE International Solid-State Circuits Conference; RFIC: IEEE Symposium on Radio Frequency Integrated Circuits; *SSC-L*: *IEEE Solid-State Circuits Letters*; ESSCIRC: European Conference on Solid-State Circuits.

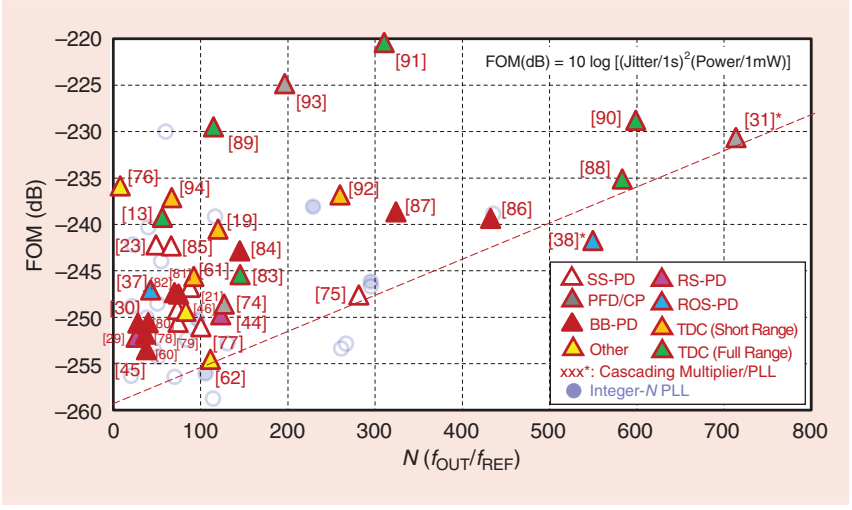

FIGURE 14: Fractional-*N* PLL/ADPLL benchmarking considering the FOM versus the *N* (f_{out}/f_{ref}) ratio.

or use other short-range high-resolution TDCs [18], [46], [61]. Alternative methods using harmonic mixing phase locking can achieve excellent performance [62]. Figure 14 conveys the PLL FOM performance for different *N* ratios. It can be observed that, when the effect of the output frequency and reference frequency is taken into account, techniques using the reference multiplier [31] or oversampling PDs [38] together with the output frequency multiplier can break the trend line. From the above PLL surveys, it can be observed that there is still room to further push the PLL FOM while maintaining a low reference clock, i.e., lower than 100 MHz.

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