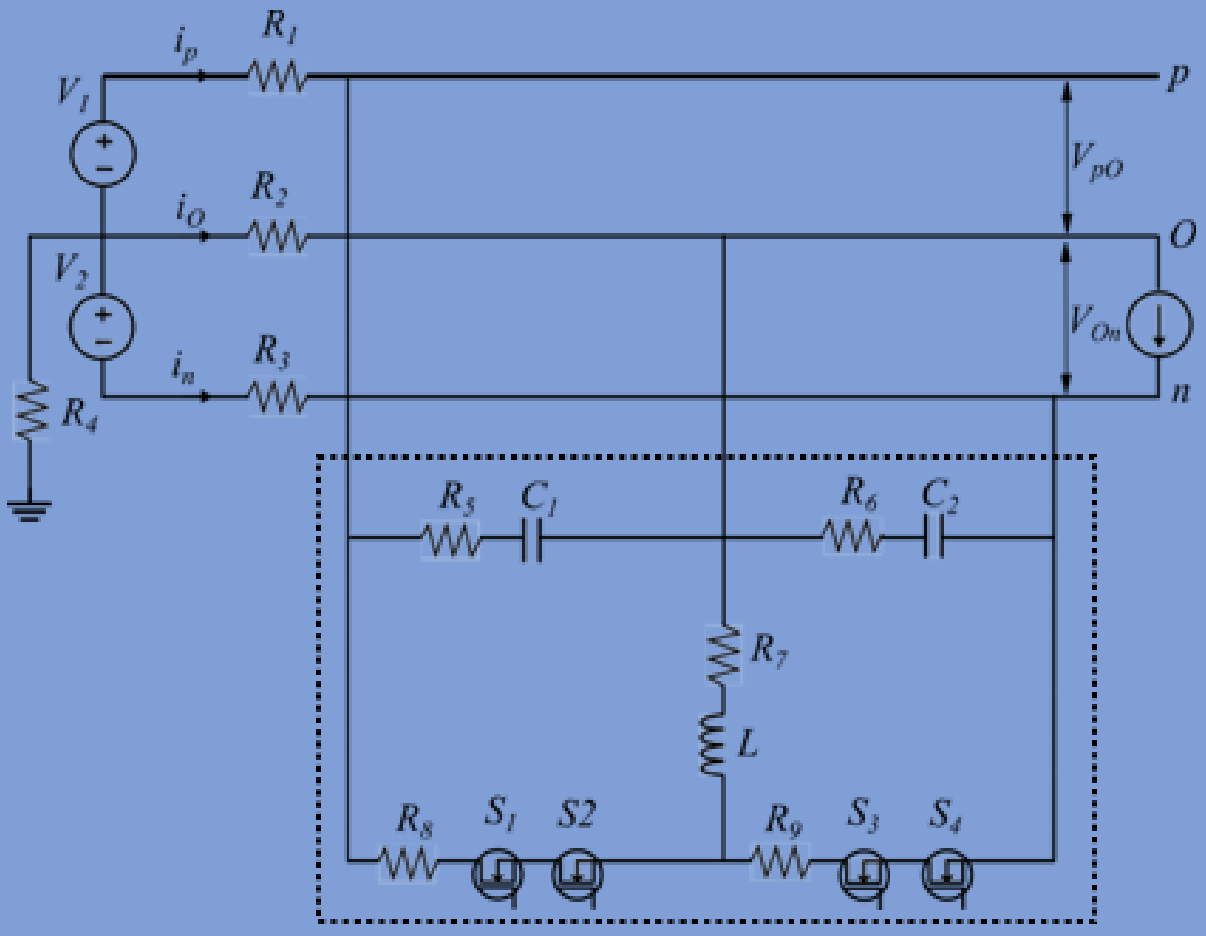
Design of Balancing Converter for Bipolar DC Grids Using Series Connected MOSFET Switches

Pooja Sinha



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DCE&S

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Design of Balancing Converter for Bipolar DC Grids Using Series Connected MOSFET Switches

by

Pooja Sinha

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TU Delft

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Each of us has cause to think with deep gratitude of those who have lighted the flame within us

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Pooja Sinha
Delft, December 2022

Abstract

Global electricity usage has been increasing exponentially over the last 40 years and with the current pace of population and economic growth, the same trend will continue in the coming years. However, the current electricity generation is predominantly fossil fuels based, which makes the overall process unsustainable and polluting, and is contributing directly to the menace of global warming. The need of the hour is to transition to renewable and sustainable sources of electricity generation such as solar, wind, etc.

However, the major bottleneck in the large-scale implementation of renewable energy sources (RESs) is the intermittent availability and their integration into existing AC grids as the RESs are predominantly DC sources. In order to tackle the issue of intermittency various energy storage solutions are being developed. Further, as a solution to the issue of integrating RESs into the current electricity distribution system, DC distribution grids are being developed.

The DC distribution architecture is of two types, Unipolar and Bipolar distribution systems characterized by the number of wires used for power transmission; 2 wires for unipolar and 3 wires for Bipolar. Out of the two, Bipolar systems have inherent advantages of flexibility, stability, and efficiency over unipolar systems.

Current thesis focuses on series connected switch configuration of voltage balancing converter for bipolar DC power distribution systems.

For this thesis, various topologies of voltage balancers for bipolar dc distribution systems were studied and a buck-boost based series connected switch voltage balancer topology was chosen for the final design. For this topology, using MATLAB, the parameterization and optimization of magnetic components of the converter were performed. The optimized configuration was then modeled and simulated using LTSpice.

Post this, a comparison between different methods adopted to account for the unbalanced voltage sharing across the series connected switch configuration of the balancing converter owing to the non-linearities present in the circuit was done. Based on this study, the most prominent of the methods is then integrated into the LTSpice model.

Contents

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Nomenclature

Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
CO_2	Carbon Dioxide
DC	Direct Current
DSP	Digital Signal Processing
EV	Electric Vehicles
LED	Light Emitting Diode
NO_x	Nitrogen oxides
RES	Renewable Energy Source
SO_x	Sulphur Oxides
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RC	Resistive-Capacitive
SEPIC	Single-Ended Primary Inductance Converter
SiC	Silicon Carbide
ZVS	Zero Voltage Switching

1 Introduction

In this chapter, the issue of global warming and bottlenecks with renewable energy sources (RES) is briefly presented followed by the introduction of DC distribution grids for facilitating RES implementation. Lastly, the research objectives and research questions are presented.

1.1. Electricity: Need for sustainability

Electricity today is an integral part of our daily life, with electrical appliances becoming ubiquitous and indispensable in carrying out our daily activities. Further, with the current pace of economic growth and the advent of the digital economy, the global electricity demand is expected to rise exponentially.[1].

Electricity in itself is a clean source of energy; however, the current methods of its production are primarily fossil fuel-based, mainly coal and gas which accounts for more than 60% of global electricity production [2] as shown in Figure 1.1. The major issues with using carbon-intensive fossil fuels, as a source of electricity generation are mentioned below:

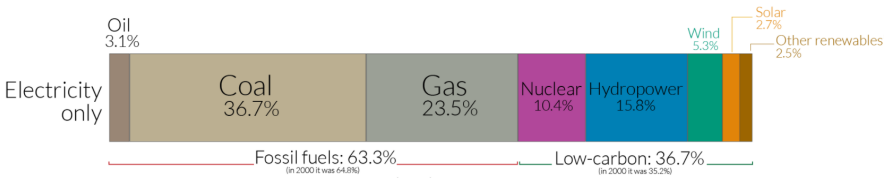


Figure 1.1: Global Electricity generation sources (2019) [2]

- **Global Warming:** Burning of fossil fuels leads to the emission of greenhouse gases such as CO_2, SO_x, and NO_x among others. The rise in CO_2 levels in the atmosphere is directly linked to the unprecedented warming up of the atmosphere, land, and oceans[3]. The same is shown in Figure 1.2 below. This is adversely affecting all life forms on earth, and if this continues unabated, then it will lead to catastrophic consequences for the earth's climate.

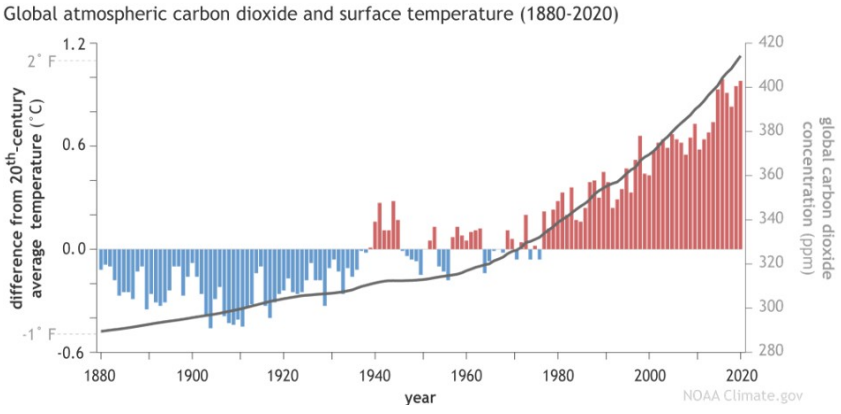


Figure 1.2: The rise in global temperature is directly linked to the increase in CO_2 level in the atmosphere due to the increased burning of fossil fuels[3]

- **Unsustainable:** Fossil fuel reserves are limited in their supply and hence, it is not sustainable to depend on fossil fuels as the main energy source. Thus, it is imperative that a transition be made to renewable/sustainable sources of energy.

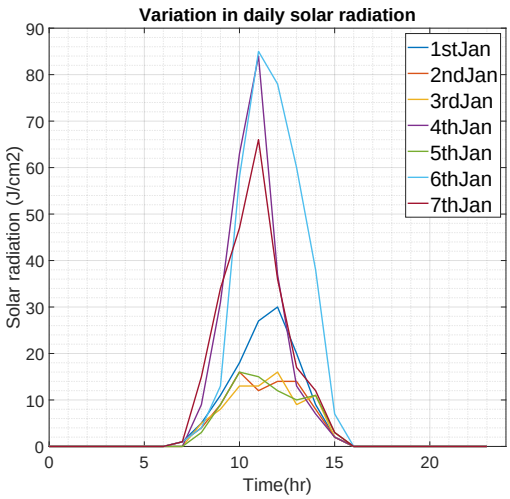
Therefore, the decarbonization of the electricity sector is the central element of current global climate policies. As per IPCC report 2021[4], limiting global temperature rise to 1.5^{o}C would require rapid and far-reaching transitions in terms of energy generation and improvement in the efficiency of current electricity sources. Thus, a rapid transition towards RES is imperative in resolving the climate crisis.

Although RES have been around for quite some time, their contribution towards electricity supply is still restricted to $\approx$ 11% even in 2019 (see Figure 1.1). This is mainly because RES have certain limitations which restrict their integration in the current electricity infrastructure. The same is discussed in the next section.

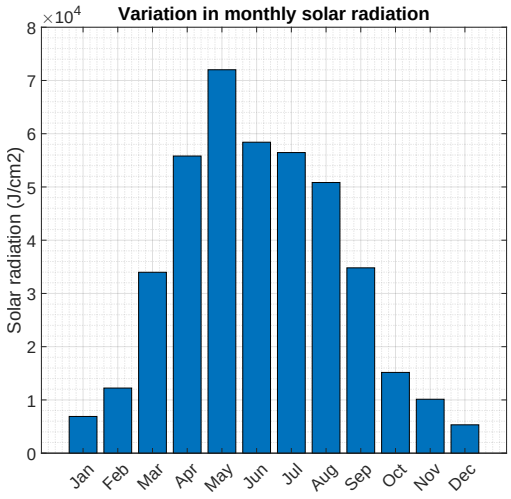
1.2. Issues with the Renewable sources of Energy

The major hindrances in the large-scale implementation of RES are as below:

- **Availability:** One of the major drawbacks of renewable sources of energy is the availability of energy. Wind, Solar energy, etc., suffer from the issue of intermittent availability. This intermittency can vary on a short time hourly variation to the long time scale of seasonal variation. Figure 1.3a and 1.3b below show the daily and monthly variation in available solar energy over Rotterdam [5]. Furthermore, there is also often a mismatch between energy availability and demand which further hinders their usage.



(a) Variation in available solar energy over a week in January 2020 in Rotterdam. [5]



(b) Variation in available solar energy over the year 2020 in Rotterdam. [5]

Figure 1.3: Daily and Monthly variation in availability of Solar energy

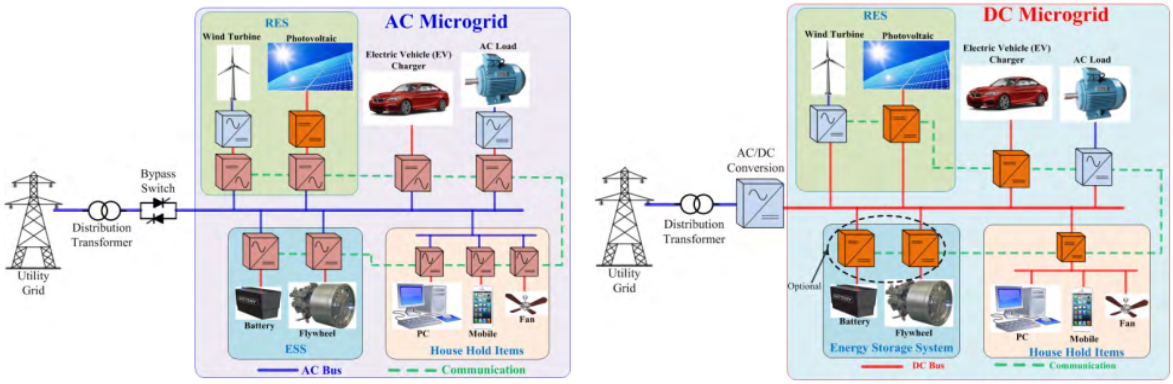
- **Integration into existing grids:** AC distribution system is inextricably woven into our power system. However, to accommodate RES and other distributed generation resources to the existing power system, the incorporation of power electronic interfaces is needed as many renewable power sources are inherently DC supplies. Wind energy too can be better optimized if at least part of the wind generator's capacity is coupled through power electronic conversion that includes a DC bus [6]. However, these distributed generation sources when integrated into the present AC utility grid can cause voltage rise and protection issues which then challenge the security, reliability, stability, and quality of the utility grid. Along with this, their integration will require multiple conversion stages making the system more complicated and prone to additional conversion power losses thus making it less efficient.

1.3. Mitigation of bottlenecks

In order to mitigate the bottlenecks discussed in previous sections, various solutions are being developed.

- **Availability**: To tackle the issue of intermittent availability of renewable sources, various energy storage systems are being developed. These systems can help overcome the issue of intermittency and can help offset the demand-supply mismatch. Some of the prominent energy storage systems which are being used are mentioned below:
  - **Battery**: Advancement in Lithium-ion and Redox flow batteries has been a major achievement in battery technology and has resulted in their large-scale deployment, especially with the global push for electric vehicles. However, in order to be economically viable for large-scale energy storage, more development in terms of energy capacity improvement and cost reduction is required [7].
  - **Hydrogen**: Using renewable electricity to generate hydrogen via electrolysis and then using this hydrogen in a fuel cell to get back electricity as per demand is another strategy that is being deployed to tackle the issue of demand-supply mismatch. However, in the current state of technology, the cost of generation of hydrogen using renewable energy sources is much higher as compared to fossil-based sources [8]. Further, the overall system efficiency with hydrogen is still not very high for such systems.
  - **Super-capacitors**: Super-capacitors are also being developed to store energy. These capacitors can release the stored energy in a very short time and hence can be very useful. However, the low energy density and high cost of super-capacitors are limiting its large-scale implementation [9].
- **DC Distribution system**: To mitigate the issues of integration of renewable sources into the AC grid, a DC active grid at the distribution level is being adopted. There are varied applications of DC distribution system including, datacenters, electric vehicle charging infrastructure, commercial buildings, shipboard microgrids, etc. Along with the benefit of integration, there are multiple advantages of switching from AC to DC distribution grids as mentioned below:
  - In the DC distribution grid, RES can be fully utilised because of their compatibility with the DC-based system. RES and power electronic loads can be supplied more effectively and efficiently by choosing a suitable voltage level that will in turn reduce the number of conversion stages [10]. DC distribution system has simplified power conversion stages which require less number of components and complexity. For instance, integrating a DC load to a DC bus via a DC-DC converter is simpler and more efficient than integrating the same to an AC line via inverters [11], [12].
  - Less conductor material is required to transfer the same amount of power in the DC distribution system as compared to AC which controls the total conduction losses of the DC line [13].
  - The increased penetration of DC sinks such as computers, laptops, LEDs, battery chargers, etc., which represents 50 % of electronic loads in many commercial and residential buildings [14], makes using DC distribution systems more appealing. Therefore, considerable attention has been given to the DC distribution system which converts and delivers DC power directly to the DC loads. This enhances energy efficiency by reducing conversion and power losses from 15-40% to 10-15% [15].

    Figure 1.4a and 1.4b below compares the number of conversion stages involved in an AC and DC microgrid respectively [16].



(a) Conversion stages of a AC distribution system [16]

(b) Conversion stages of a DC distribution system [16]

Figure 1.4: Conversion stages of an AC and DC distribution system

- Present AC systems have virtually no storage thus making them susceptible to interruptions in power supply. These limitations are taken care of in the DC distribution system by introducing various energy storage systems (ESS). ESS can also come in handy during peak shaving, load leveling, absorbing regenerative power, etc.

- DC distribution systems are also suitable for AC supply RES. Integration of wind turbines with the AC grid requires back-to-back power conversion from AC to DC and back to AC to synchronize and adjust the voltage and output frequency level. It is easier to adopt a DC-DC converter than an AC-DC inverter.

- To maintain the power stability in an AC utility grid, both voltage and frequency are required to be monitored and controlled whereas, in DC distribution lines, only voltage needs to be monitored. Along with this, DC distribution lines are free of reactive power issues, AC losses, and skin effects and thus have lower control complexity and smaller footprints (fewer filters) [17].

- There is a possibility of potential health concerns from human exposure to 60 Hz distribution lines and thus switching to DC grids will have long-term benefits on the health of human beings as well as animals.[18]

1.4. DC Distribution Architecture

In order to integrate new technologies such as RES, modifications in the existing DC architectures are required to further enhance their flexibility and controllability. Electric power in a DC distribution system can be transmitted either over a two-wire or three-wire system configuration.

According to the number of buses, the existing DC distribution network system can be categorized into two types of DC bus frames: Unipolar and Bipolar DC bus configuration [19].

- **Unipolar**: A unipolar (also known as monopolar) DC distribution system comprises two DC wires providing a single DC voltage level between the two conductors. The majority of DC installations adopt this configuration. Though this architecture is easier to control and is less complex, it lacks the reliability and resilience of a three-wire Bipolar DC distribution.

- **Bipolar**: A Bipolar DC distribution system is a three-wire system that provides two voltage levels across those three wires [20] and thus provides more flexibility and reliability than unipolar systems.

  Figure 1.5 below shows a schematic representation of a unipolar and bipolar DC distribution grid.

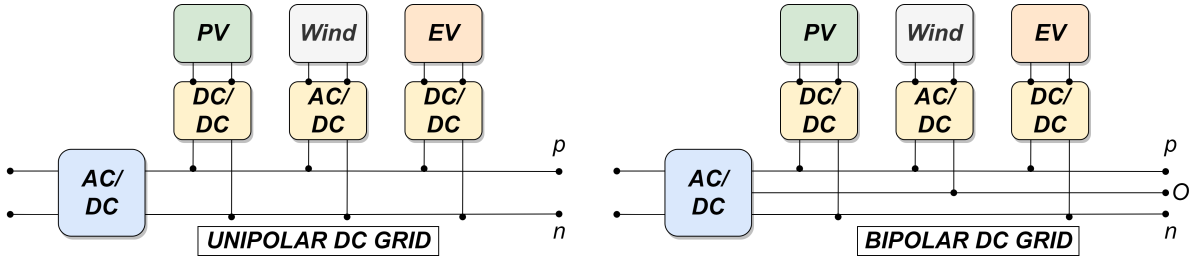


Figure 1.5: A Unipolar and Bipolar DC distribution grid

The advantages of using a bipolar DC distribution system over a unipolar system are as follows:

- The bipolar architecture of the DC distribution system provides two voltage levels to choose from with fewer buses. Therefore, a device can be connected between pole-to-neutral or pole-to-pole depending on its end-use application. More voltage levels make the system more connection-friendly between DC sources and DC loads.

- RES, EV charging stations, and green buildings can be flexibly integrated to efficiently utilize the DC power supply system, reducing the conversion stages even further. Fewer buses for transfer mean lower transmission losses [13].

- With the presence of three DC lines, system stability, reliability, flexibility, and efficiency can be improved. Independent operation of the DC buses protects the system against failure. In case of operational failure in one DC line, the power continuity can be ensured by using the other two lines of the bipolar grid, thus ensuring the system's reliability.

- Short circuit faults and grounding issues are some of the major challenges associated with DC systems. The presence of a neutral conductor in Bipolar DC configuration provides an easier and faster method for clearing these faults ([21], [22]), and thus makes Bipolar DC configuration more suitable than unipolar DC grids.

- Bipolar architecture allows a reduction in the distribution voltage with respect to the ground, thereby improving safety [23].

Despite the various advantages of the Bipolar DC distribution system, it has its own share of limitations:

- Asymmetrical operation due to the unbalanced power distribution is caused by drawing or injecting different power levels in the two poles. For instance, unbalanced load distribution and/or integration of ESS leads to an unbalanced neutral line current. This further leads to voltage imbalance between the phases leading to deterioration of power quality and increase voltage stress of semiconductor devices [20].

- The power losses in the system are increased due to unbalanced voltages. Further, the lifetime of the devices is also adversely affected due to these unbalanced voltages [24].

Due to the tremendous potential that bipolar DC grids hold for the development of DC distribution systems, it is essential to regulate the unbalanced voltage in the bipolar DC distribution network by adopting a voltage balancer circuit. Voltage balancer improves the quality and flexibility of the power supply in a bipolar DC distribution system by balancing the bus voltage and current to ensure that the system operates safely within the rated range.

This thesis pertains to the development of a voltage balancer for a DC Distribution system focusing on the Bipolar DC Distribution system. The specification for the same is provided in Table 1.1 below:

Table 1.1: Voltage Balancer Design Specification

Parameter	Description	Value	Unit
V_{Grid}	Grid Voltage	1400	V
P_{Out}	Output Power	5	kW

Further, through this research, the application of a series connected switch configuration will also be explored and its performance will be evaluated over a single switch configuration.

1.5. Research Objectives

The main objective of the thesis is to design a balancing converter that can be used to keep the phase voltages of a bipolar DC grid balanced and the neutral line current to zero to account for the unbalances in the system.

The research objectives can be summarised below:

- Identifying a suitable topology for balancing converter through literature research
- Modelling and simulation of the balancing converter for the single switch and series connected switches configuration using MATLAB and LTSpice.
- Comparison of various methods for driving series connected MOSFET switches and implementation of the most suitable method in the LTSpice simulation model.

1.6. Research Questions

To achieve the research objectives, the following are the research questions this thesis aims to answer:

1. What are the promising topologies that have been developed for voltage balancing of a Bipolar DC distribution system?
2. What is the optimum design for the chosen topology of the voltage balancer?
3. What is the impact of series switch configuration in the optimized design of voltage balancer?
4. What are the available methods to account for voltage imbalance in series connected switch configuration?

1.7. Structure of the thesis

The thesis addresses each of the research questions in separate chapters. The chapters are arranged as follows:

- **Chapter 2:** It provides an overview of the literature research into the working of Bipolar DC distribution systems, existing topology for voltage balancer of DC distribution system, and the design considerations for the chosen voltage balancer topology for this thesis. This chapter also delves into the possibility of using series-connected switches to enable the balancer converter model for high-voltage applications.

- **Chapter 3:** This chapter elaborates on the modeling of the voltage balancing converter design using MATLAB. This encapsulates the switch selection for single and series-connected configurations of voltage balancer topology, comparison of the two configurations based on their losses, parameterization of the components of the configuration chosen, optimization of the magnetic design, and calculation of total converter loss.

- **Chapter 4:** This chapter discusses the LTSpice simulation model of the optimized series connected switch configuration of the voltage balancing converter for bipolar DC grid operation. Further, non-linearities are introduced in the configuration to address the issue with the series-connected switch configuration of the voltage balancer. LTSpice simulation results of the same are also discussed.

- **Chapter 5:** It covers the comparison between different methods adopted to account for the unbalanced voltage sharing across the series-connected switch configuration of the balancing converter owing to the non-linearities introduced in the previous chapter. The most prominent of the methods is then employed in the LTSpice model. An analytical derivation to interpret the degree of voltage unbalance is also provided for the employed method.

- **Chapter 6:** In the final chapter the conclusions from this thesis and the recommendations for further research are presented.

2 Background

In this chapter the background information required to achieve the research objectives of the thesis is presented. At first, the Bipolar DC distribution system and its working are explained in detail, followed by an overview of the existing voltage balancer topologies used for Bipolar systems. After this, the chosen topology, i.e., the Buck-Boost system is explained. Lastly, the series switch configuration of buck-boost topology as a voltage balancer is presented.

2.1. Bipolar DC Distribution System

The expansion of RESs, ESS, and the large-scale implementation of electronics in most appliances have resulted in the development and implementation of DC distribution systems [25]. Within the DC power grids, Bipolar DC distribution systems are more favorable than unipolar grids (established in Section 1.4).

The Bipolar DC grids, based on their connection with the utility grid, can further be sub-divided into the following categories:

- **Grid Connected:** In this configuration, the AC utility voltage is converted to DC with the use of distribution transformer and an active rectifier. At the DC level, the system adopts a three-wire structure composed of a positive conductor (p), a negative conductor (n), and a neutral conductor (O). Although the three-wired structure looks complex, it provides a clear advantage over the two-wired unipolar structure. The two voltage levels of a bipolar configuration allow penetration of a wide set of distributed generators, energy storage systems, and loads with different voltage levels and power rating combinations in a single DC network. A schematic of this configuration is shown in Figure 2.1 below:

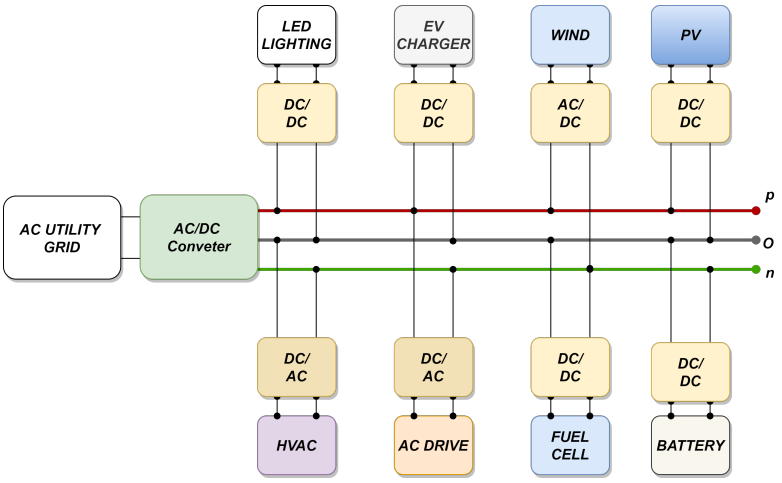


Figure 2.1: Grid connected DC distribution system

- **Islanded Mode:** In this configuration, the DC grid is connected to a DC power system which can be a DC Energy storage system or RES which directly generates DC power through a DC-DC

converter stage. At the DC level, the connection is similar to as shown for grid connected DC grid in Figure 2.1. A schematic of this configuration is shown in Figure 2.2 below.

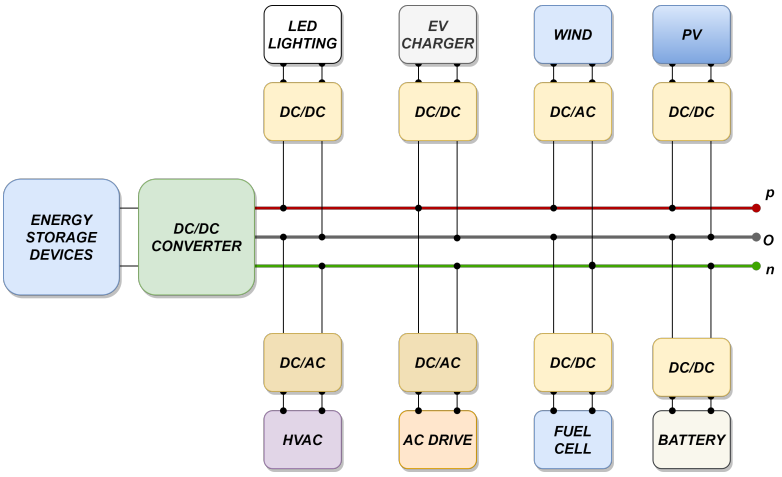


Figure 2.2: Islanded mode DC distribution system

2.2. Bipolar DC Grids: Challenges

The Bipolar DC grid system offers multiple advantages of increased flexibility, reliability, efficiency, etc. However, the DC Bipolar grid connection has its own set of challenges as well (Section 1.4).

Of these challenges, the issue of voltage imbalance between the bipolar poles is the major deterrent for the Bipolar DC grid system.

2.2.1. Voltage Imbalance: Bipolar DC Grid

The issue of voltage imbalance between the poles of the Bipolar DC grids arises due to the asymmetric operation between the poles of the grid. This can arise due to unbalanced load distribution between the connections and result in neutral line unbalanced current and voltage unbalance in the phases.

The situations that can result in asymmetric operation and voltage imbalance are shown in Figure 2.3 below [25].

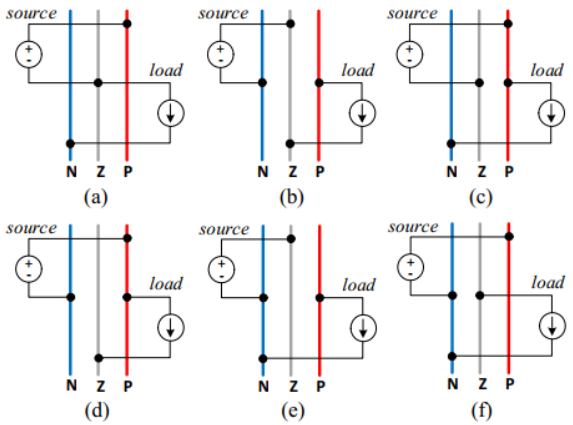


Figure 2.3: Voltage imbalance in Bipolar DC grids can arise due to 6 different types of asymmetric operation/connection. Image taken from the works of Pires et al.[25]

It is essential to account for these imbalances which arise in the grid. These imbalances not only result in poor power quality and inefficient operation of loads and assets connected to the grid but in cases of high voltage spikes can result in damage to the power electronic devices in converters.

2.3. Voltage Balancer:

To stabilize the Bipolar DC grids, without compromising on system reliability, an additional converter for balancing the voltage is integrated into the bipolar DC grid system. This balancing converter is called the Voltage balancer.

Voltage balancer works by actively redistributing the unbalanced power in the system and thereby protects the semiconductor devices and the overall grid operation from unbalanced voltage stress due to the asymmetric operation of the grid.

Depending on the connection method, the Voltage balancers configuration can be broadly categorised as below:

- **Centralised Architecture:** In this configuration, the voltage balancing Tos connected directly to the grid connection line before connection to the loads. Thus, a single balancer takes care of any voltage imbalance in the system.

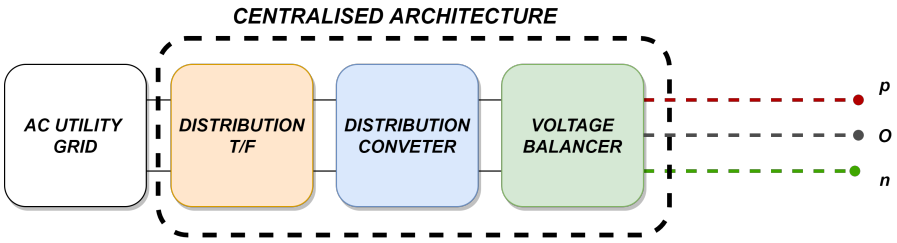


Figure 2.4: Centralised architecture of DC distribution system

- **De-centralised Architecture:** In this configuration, the voltage balancing converters are connected individually to each load connected to the grid. Thus, for each individual load, a separate balancer is required.

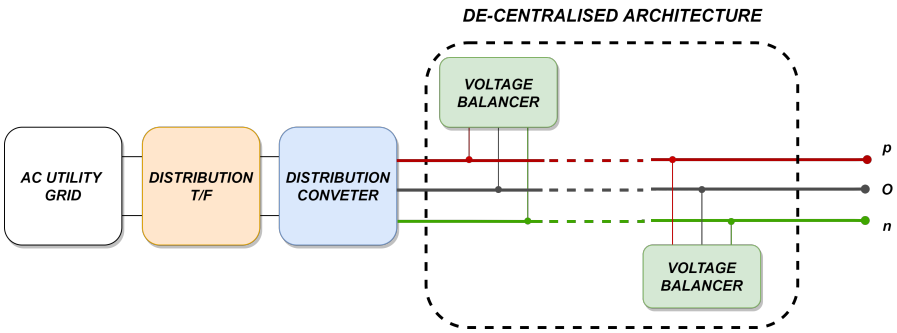


Figure 2.5: De-centralised architecture of DC distribution system

In the work by Pires et al [25], it has been suggested that de-centralised architecture for voltage balancing is more advantageous and practical than centralised architecture. The main reasoning behind the argument is that in DC grids with long transmission lines, voltage imbalance will arise due to voltage drop along the lines. Thus using multiple voltage balancers connected at locations with maximum voltage imbalance will be much more advantageous in ensuring a stable distribution system. However, the cost of the system will go up owing to the installation of multiple voltage balancers.

For the current thesis, a decentralised voltage balancer architecture was considered for the design and thus the same has been explored in detail in the next sections.

2.4. Existing topologies

This section addresses the major DC-DC converter topologies for decentralised voltage balancer architecture which are used with bipolar DC distribution networks to achieve desired voltage balancing.

2.4.1. Buck-Boost Topology

A buck-boost topology is the simplest non-isolated topology that is used for voltage balancing in a Bipolar DC grid system. The circuit diagram of a typical Buck-Boost topology is shown in Figure 2.6 below:

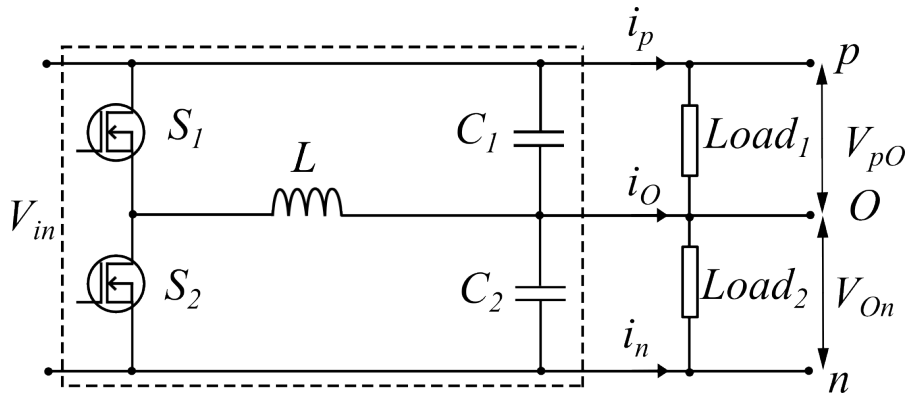


Figure 2.6: Buck-Boost voltage balancer topology

The main advantages of Buck-boost topology are listed below:

- It uses the minimum number of components out of all voltage balancer topologies available for bipolar DC grids [25].
- It is simpler in implementation and as mentioned above, uses a smaller number of components. Both these factors combined make the buck-boost topology highly cost-efficient.

The buck-boost topology also has its own set of limitations. The major ones are listed below:

- It generally uses a large filter size in order to balance the voltage in the bipolar grid and thus is prone to electromagnetic interference issues.
- The overall efficiency of the buck-boost topology is low owing to higher losses that arise due to higher reactive current in the circuit [25].
- The buck-boost topology also suffers from the issue of shoot-through and thus requires to have dead time between the operation of the two switches used in the system.

2.4.2. Dual-Buck Half Bridge Voltage Balancer Topology:

A dual buck half-bridge converter is a bridge-type converter dispersedly used to convert a unipolar DC grid to a bipolar DC grid and to balance the voltage across the phases of the three-wire configuration [26]. Figure 2.7 below shows the electrical circuit of a dual-buck half-bridge topology.

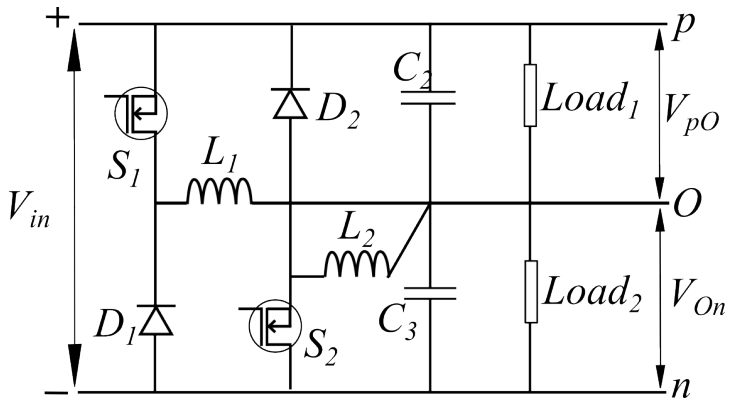


Figure 2.7: Dual-Buck Half Bridge voltage balancer topology

The main advantages of using this topology are mentioned below:

- The dual buck half-bridge topology does not have a shoot-through problem. [26].
- It has the ability to control the output voltage while operating under varying input voltage conditions with unbalanced and transient loads [26].

The main drawbacks of using this topology are listed below:

- Using conventional complementary driving technology for the half-bridge switches causes additional power losses since the two inductors are conducting during a switching period.
- The control strategy used for implementing the topology results in a slow dynamic response of the converter.
- It is more expensive and has a high volume footprint because of the higher number of components involved [27].

2.4.3. Super SEPIC type Voltage Balancer Topology

Super SEPIC (Single Ended Primary Inductor Converter) is a high order converter that was proposed in the works of Wang et al. [28] (derived from a bi-directional SEPIC type conveter [29],[30]). The equivalent circuit of the same is shown in Figure 2.8 below.

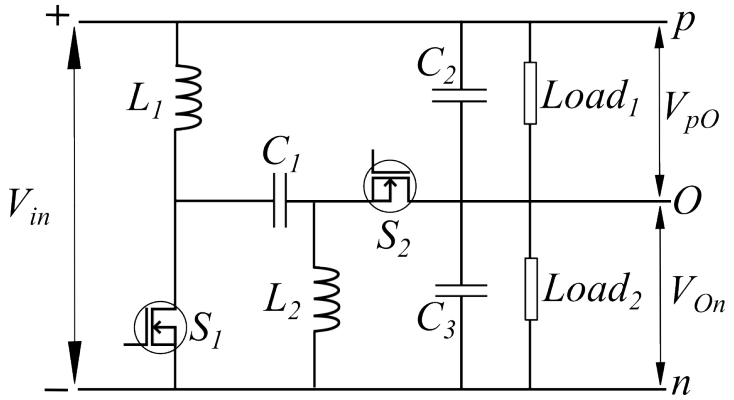


Figure 2.8: Super SEPIC type voltage balancer topology

The major advantages of the Super-SEPIC topology are mentioned below:

- The super SEPIC topology is a high order converter and does not have the issue of shoot through and thus does not require complex gate driver control for its implementation. [28]

The main limitations of the topology are as listed below:

- The topology uses multiple inductors and capacitors along with the switches and thus has higher cost and volume footprint.
- It results in high voltage stress on the switches [27].

2.4.4. Super-ZETA Voltage Balancer Topology:

Similar to Super SEPIC topology, Wang et al. [28] proposed a Super-ZETA topology derived from bi-directional ZETA topology from the works of Tymerski et al [29]. The equivalent circuit for the same is shown in Figure 2.9 below:

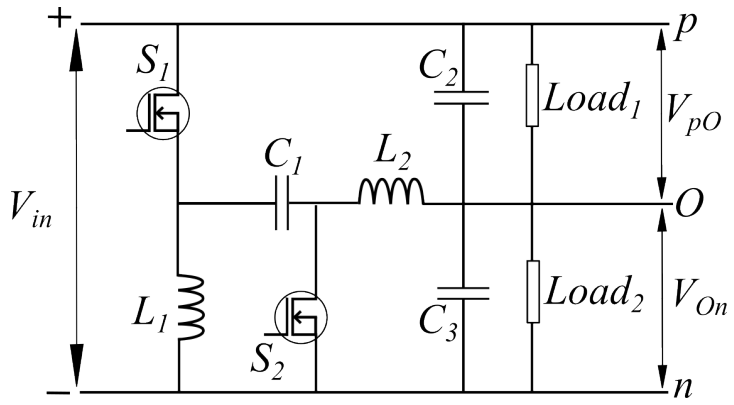


Figure 2.9: Super ZETA type voltage balancer topology

The main advantage of Super-ZETA topology are listed below:

- It has no shoot through concerns and thus does not require complex gate driver control for operation of switches [27], [28].

The main disadvantage of the ZETA topology is listed below

- It uses large capacitors and thus has higher current stress [27].
- It has lower power rating and induces higher voltage stress on the switches [28], [27].

2.4.5. Cuk Type Voltage Balancer Topology:

Cuk type voltage balancer topology provides successful voltage balancing across the phases of bipolar DC converter. It generally operates with a lower inductor current as the same is split over the two inductors used in this configuration. A typical Cuk-type voltage balancer is shown in Figure 2.10 below.

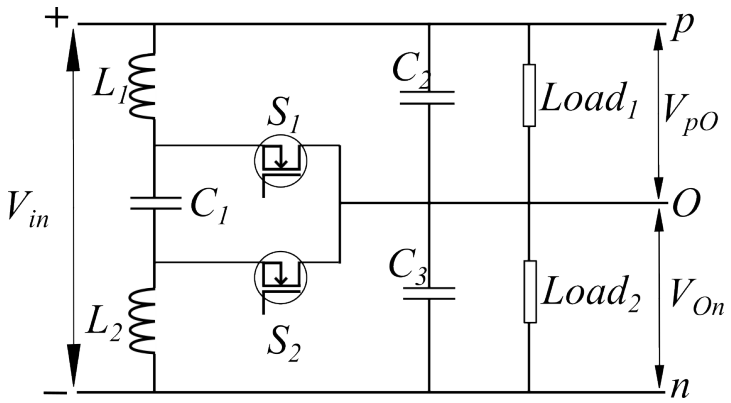


Figure 2.10: Cuk Type voltage balancer topology

The main advantages of using Cuk type voltage balancer are listed below:

- It has no shoot though concerns in its operation.
- The major benefit of using the Cuk voltage balancer topology is the continuous input and output current that is obtained from its operation [25].

However, the Cuk voltage balancer has its challenges as well. The same are listed below:

- It involves a large number of reactive components in its implementation and thus has more failure points and can have reliability issues [27].
- Its implementation is expensive and is not suitable for applications with a power output higher than 5kW [27].

2.4.6. Three-level converter Topology:

The three-level converter topology used for voltage balancing is a highly sophisticated and effective solution for voltage balancing of bipolar DC grids. Figure 2.11 below depicts a typical 3-level voltage balancer topology that is employed for voltage balancing.

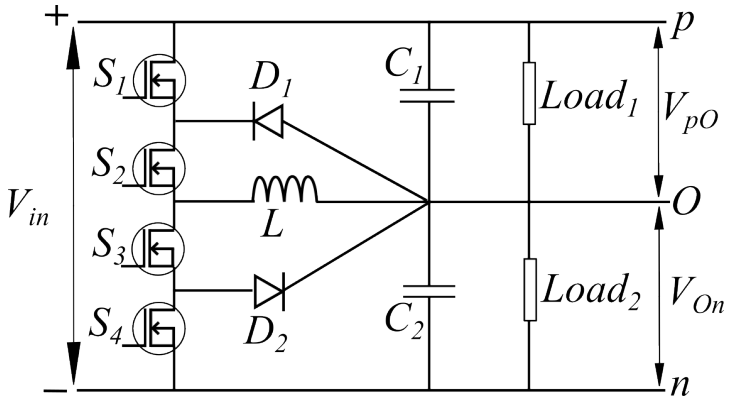


Figure 2.11: Three-level voltage balancer topology

The main advantages of this topology are mentioned below:

- The voltage stress over the switches in this configuration is very less.
- 3-level converter topology can be implemented over a very wide range of power applications and can be scaled even with reduced power ratings.

The 3-level converter topology has its own set of limitations which are listed below:

- It involves a very large number of components in its applications and thus is more expensive and complex to implement and operate [27].

Based on the above summary it was seen that there are multiple voltage balancer topologies that have been researched and explored, each with its own set of advantages and challenges. There is no single configuration that can meet all the criteria for finalizing a particular topology for a voltage balancer application. For this thesis, a synchronous buck-boost topology was selected for further design and analysis. The next section elaborates on the same.

2.5. Buck-Boost Topology

A synchronous buck-boost converter is adopted for the voltage balancer topology and is shown in Figure 2.12. The voltage balancer selection is based on a simpler structure, fewer passive components, and higher cost efficiency of the buck-boost topology.

It constitutes two switches (S_1 and S_2) and passive elements such as an inductor (L) and capacitor (C1 and C2). Synchronous configuration employs an active switch (S_2) in place of a rectifying diode which is used in a non-synchronous buck-boost converter.

The synchronous configuration is preferred because the voltage drop across switch S_2 (the product of current flowing through it and its on-resistance) is lower than the forward voltage drop of the rectifying diode. This results in a reduction of conduction losses. This configuration is called synchronous as the operation of switch S_2 is synchronized to the operation of switch S_1. The commutation of both switches is complementary to each other. SIC MOSFETS are used as switches in this converter.

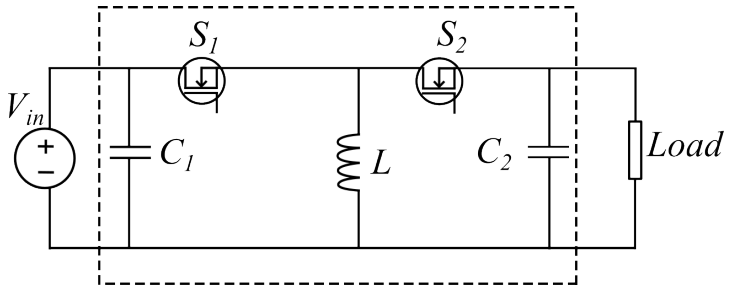


Figure 2.12: Synchronous Buck-Boost Converter

2.5.1. SiC MOSFET

An n-channel SiC MOSFET is shown in Figure 2.13. It constitutes of a diode and three capacitors connected between the three terminals of the device [31], namely:

- C_{gd}: Gate-drain capacitance
- C_{gs}: Gate-source capacitance
- C_{ds}: Drain-source capacitance

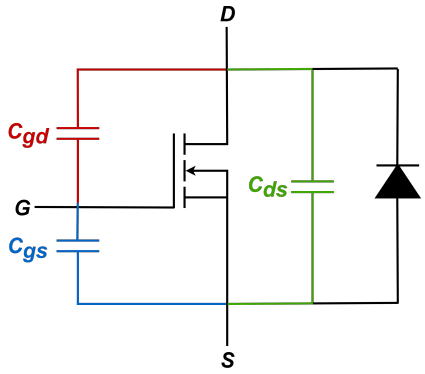


Figure 2.13: Device model of SiC MOSFET. D, G, and S are Drain, Gate, and Source terminals respectively.

The pn junction between the drain (D) and source (S) forms the diode which is also called the body/-parasitic diode. During the off state of the MOSFET, this diode provides a path for the inductive load current to bypass the MOSFET [31].

The capacitors, which are also called parasitic or stray capacitances are formed as the mobile charges within the MOSFET structure come too close or separate out. The parasitic capacitances affect the switching speed of the MOSFET. This effect is minimal at low frequencies but can be very significant at high-frequency operations [31]. The value of these capacitances is indirectly obtained from the datasheet of the MOSFET by analyzing the C_{iss}, C_{oss}, and C_{rss} parameters.

Details of these parameters are given below:

- C_{iss}**: Input Capacitance** It is the capacitance of the MOSFET as seen from the input to the MOSFET. It is calculated by the addition of gate-source capacitance (C_{gs}) and the gate-drain capacitance (C_{gd}). It is necessary to charge C_{iss} for the MOSFET to operate (Turn ON) and the amount of charge required for charging up the C_{iss} is called gate charge, Q_g [31].

- C_{oss}**: Output Capacitance** It is the total capacitance on the output side, obtained by the addition of drain-source capacitance C_{ds} and the gate-drain capacitance C_{gd}. The switching speed (both Turn On and Turn Off) of the MOSFET is directly influenced by C_{oss}, with a higher value of C_{oss} resulting in a slower switching speed of the MOSFET [31].

- C_{rss}**: Feedback capacitance:** It is the same as gate-drain capacitance C_{gd} and it also impacts the switching speed of the MOSFET. A larger value of C_{rss} increases the switching time of the MOSFET by increasing the delay in the rise and fall during gate turn On and turn-off respectively, The amount of charge required to drive the C_{rss} is called Q_{gd} [31].

The same is summarised in Table 2.1 below:

Table 2.1: Description of MOSFET Capacitance

Parameter	Description	Expression
C_{iss}	Input Capacitance	C_{gs}+C_{gd}
C_{oss}	Output Capacitance	C_{ds}+C_{gd}
C_{rss}	Feedback Capacitance	C_{gd}

These capacitance values are non-linear in nature i.e., their value depends upon the operating point or the drain-source voltage V_{DS} of the MOSFET. For the usual operation of the MOSFET, these capacitance values decrease with an increase in V_{DS} [31].

2.5.2. Operation of synchronous buck-boost converter

The output capacitance, C_{oss} gets charged up to the DC link voltage value V_{in} when the MOSFET is in the 'OFF' state. A positive gate pulse signal is sent to the gate-source terminal of the MOSFET to turn it on. This gate pulse initializes the gate current i_g [31].

When MOSFET is turned on, current flows through it from the supply to charge the inductor and energy is stored in the inductor's magnetic fields. Since there is a possibility of shoot-through in the converter, a dead time is provided between the operation of the switches. During this dead time, the output capacitance of switch 1 is charged to DC link voltage whereas, the output capacitance of switch 2 is discharged to zero before it turns on. This is called zero voltage switching. After discharging the capacitor, the current from the inductor flows through the body diode of switch 2 until the dead time is over. After switch 2 is turned on, the energy stored in the inductor is released through it to provide power to the load.

2.5.3. Losses in synchronous buck-boost converter

The losses in the buck-boost converter can be divided into two broad categories, namely: switch loss and magnetic loss. Semiconductor switches such as MOSFETs dissipate energy in terms of heat when they are operational. These losses can be further divided into switching loss and conduction loss. Whereas, the magnetic loss happens in the inductor element which is made up of insulated wires that are wound into a coil around a core. Hence, the magnetic loss includes winding loss and core loss.

MOSFET Conduction loss:

The conduction loss of MOSFET is defined as the loss that occurs during the steady-state condition of the device. The conduction power loss can be modeled by using the equivalent on-resistance of the MOSFET as shown in Equation 2.1.

$$P_{MOS-conduction} = I_{Drms}^2 \cdot R_{DSon} \tag{2.1}$$

Where:

Symbol	Parameter	Unit
$P_{MOS-conduction}$	MOSFET Conduction Loss	[W]
I_{Drms}	Drain RMS Current	[A]
R_{DSon}	Equivalent drain to source resistance	[Ω]

MOSFET switching loss:

The switching losses of the MOSFET are defined as the losses that occur during the dynamic transition from the conduction state to the blocking state and vice versa. The switching power losses of the MOSFET are modeled using equation 2.2.

$$P_{MOS-switching} = (E_{on} + E_{off}) * f_s \tag{2.2}$$

Where:

Symbol	Parameter	Unit
$P_{MOS-switching}$	MOSFET Switching Loss	[W]
E_{On}	Turn on energy loss	[J]
E_{Off}	Turn Off energy loss	[J]
f_s	Switching frequency	[Hz]

Magnetic loss:

Magnetic loss is categorized as core loss and winding loss. Core loss is further classified into hysteresis loss and eddy current loss. Figure 2.14 below depicts the same.

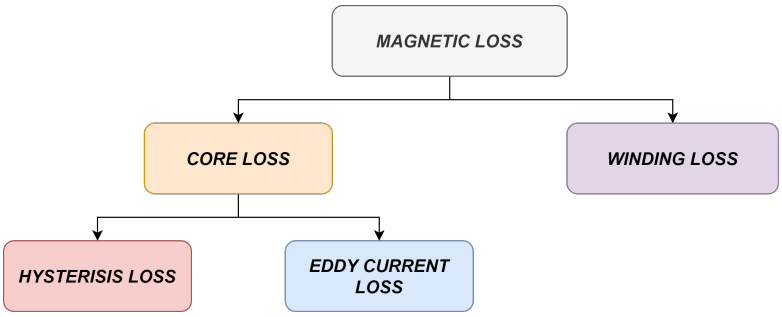


Figure 2.14: Magnetic loss is primarily of two types, Core and Winding loss. Core loss can be further subdivided into Hysteresis and Eddy current loss

- **Hysteresis Loss:** For magnetic circuits, hysteresis can be described as the delay in the change of magnetic flux density (B) of a material as the magnetic field strength (H) changes through the medium. Figure 2.15 below shows the typical hysteresis curve for a magnetic material. It can be seen that as H increases, B increases (1 $\rightarrow$ a); however when H is then reduced B doesn't reduce at the same rate and when H reaches 0, there is a residual positive value of B left (a $\rightarrow$ b), which is called retentivity. In order to reduce B to 0, H has to be increased in the negative direction (b $\rightarrow$ c), and this value of H is called coercivity. The area of this curve depicts the energy required to complete a cycle of magnetisation-demagnetisation, and gives the hysteresis loss of the material.

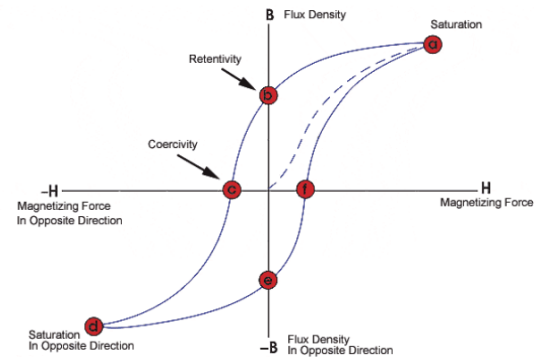


Figure 2.15: Hysteresis curve for a magnetic material. The magnetic field density does not increase or decrease at the same rate when the magnetic field strength across it changes direction. (Image taken from [32])

- **Eddy current loss:** Any change in current flowing through a conductor coil, either in magnitude or direction induces a voltage in the material, as described by Faraday's law [31]. If the core material is electrically conductive, then the induced voltage results in circulating currents within the material. These currents are called Eddy currents. The resistive power loss (I^2*R) due to this current is called Eddy current losses. Figure 2.16 below shows Eddy current circulating through a solid and a laminated core.

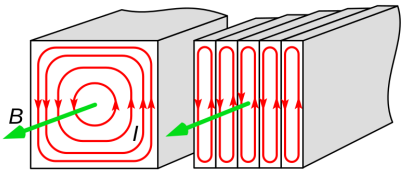


Figure 2.16: Eddy current losses in solid and laminated cores. (Image taken from [33])

- **Winding loss:** The losses incurred due to current flow through the wires of the magnetic core winding are referred to as winding loss. These losses are due to the resistance of the core wires and can be calculated as I^2*R.

  However, the resistance of the core wire increases with the frequency of the current flowing through it. This phenomenon is referred to as the "skin effect" [34]. It occurs when the magnetic field induced by the current flow through the wire force the electrons to the outside of the wire. Thus for higher-frequency applications, the winding losses are also higher.

2.6. Series Connected Switches

Series connected switch configuration for voltage balancer, as the name suggests, involves connecting switches in series in the voltage balancer configuration. The main advantages of using a series-connected switch configuration for a voltage balancer are given below:

- **Higher voltage operation:** Series connection of MOSFET switch in the voltage balancer allows for higher voltage operation with the low voltage MOSFETs [35].

- **Lower Cost:** The cost of a MOSFET increases with an increase in the blocking voltage of the MOSFET. Thus, by using low voltage switches in series it is possible to achieve higher voltage operation at a lower cost as compared to using a single switch of higher voltage capacity [36].

- **Lower output capacitance:** The output capacitance of the switches with higher breakdown voltage is more than switches with lower breakdown voltage. With the higher value of output capacitance, more current will be required to charge or discharge it. Whereas by connecting lower breakdown voltage MOSFETS in series to equate the same breakdown voltage as a single switch, the individual output capacitances of the switch are lower and the series summation of each makes the value even lower. This helps in speeding up the charging and discharging and hence the speed of the device.

However, using a series-connected switch in the voltage balancer has its own set of challenges as well. Some of the major challenges are mentioned below:

- **Non-linearities:** MOSFETs have non-linearities in them i.e., two MOSFETs of the same configuration will have some deviation in terms of their internal resistance, capacitance, and inductance values. These deviations if not accounted for, can introduce additional imbalances in the system [35], [37]. The main causes of non-linearity in MOSFET are listed below:

  - **Tolerance in external gate resistance:** When MOSFETs are connected in series, then the tolerance in the resistance value of the external gate resistor can become an issue, resulting in unequal voltage sharing between the switches.

  - **Parasitic capacitance:** The intrinsic parasitic capacitances of the MOSFET, parasitic capacitance introduced by the gate drive circuit, and the parasitic capacitance of the packaging of the MOSFET are the main sources of parasitic capacitance in MOSFETs. Non-linearity in these capacitances can result in unequal voltage sharing, and alteration of switching speed among other issues in series-connected MOSFETs.

  - **Gate delay:** Any variation in the gate driver circuits of series-connected MOSFETs can result in non-linearity in terms of gate switching time initialisation. This can result in unequal voltage sharing, voltage spikes, and even damage to the MOSFET in case the device blocking voltage is exceeded.

- **Complexity:** Adding additional components in the voltage balancer configuration introduces additional complexity in the control and operation of the converter. Further, the addition of components introduces more failure points in the system and thus a more robust control system is required for reliable and safe operation.

2.7. Summary:

- Through the literature research, the various configurations of Bipolar DC grid systems were identified along with different configurations of the voltage balancer used for these grids.

  Current work will focus on decentralized architecture for a grid-connected Bipolar DC grid system.

- For the decentralized architecture, different topologies used for voltage balancing converters were researched. Based on a simpler design structure and higher cost efficiency, synchronous buck-boost topology was finalized for further design in this thesis.

- Series connected switch configuration for voltage balancer was also researched on account of its possible application for high voltage application with low voltage switches and cost efficiency.

  An evaluation of series-connected and single-switch configurations for voltage balancers will be performed in the next chapter to identify the better design choice for this thesis.

3
Design and Optimisation

In this chapter the design process for the Buck-Boost Voltage balancing converter is described. At first, the switch selection methodology is presented which was used to finalize the switches for single and series-connected switch buck-boost topology. Post this, a comparison of conduction and switching losses for single and series-connected switches topology were made to finalize the number of switches in the configuration. Following that, the magnetic design and optimization process is presented through which the inductor specification was finalized. Finally, the total converter losses were calculated and compared and the design was optimized.

3.1. MOSFET Selection:

MOSFETs are ubiquitous and are extensively used for varied applications in almost all modern-day electronic appliances. There is a plethora of MOSFETs available for usage depending on specific applications and the selection of a particular MOSFET for an application requires a comprehensive evaluation of multiple MOSFET parameters. Some of these parameters are described below:

3.1.1. MOSFET selection parameters:

- **Maximum drain to source breakdown voltage (V_{DSS}):** It is the maximum voltage that can be applied to a drain-source MOSFET terminal in the Off state. In order to account for voltage overshoots, it is desirable to select a MOSFET with a higher drain-source voltage than the terminal voltage.

- **Drain to source resistance ($R_{ds(on)}$):** When the MOSFET starts conducting in the ohmic region, it behaves as a resistor, the value of which is given by the on-resistance parameter in the datasheet of MOSFET. The drain-to-source resistance dictates how much heat is dissipated by the device when it is conducting and thus determines the conduction loss. Hence, a MOSFET with lower $R_{ds(on)}$ is preferred.

- **Gate charge (Q_g):** Q_g indicates the amount of charge that needs to be fed to the gate for the device to turn on. In high-frequency applications, this parameter holds a critical position as it directly correlates with the time taken to turn on and turn off the MOSFET. The lower the Q_g of a MOSFET, the more efficient a high-frequency switching application can be.

- **Coss:** As described in Chapter 2 Section 2.5.1, C_{oss} is the parasitic capacitance associated with a MOSFET. It is a valuable parameter when it comes to the switching operation of MOSFET. During hard switching, C_{oss} is used to calculate the additional power loss that will incur in the switch due to discharging of the capacitance in every switching cycle. Whereas, in soft switching conditions, C_{oss} is used to determine the transition time required to establish ZVS (zero voltage switching). The lesser the output capacitance, the lesser will be the time taken in its charging and discharging.

- **Cost:** For any project, the cost of components is an important consideration. Since the MOSFET is a significant component of the voltage balancer design, it is important to choose the most economical MOSFET among the ones which meet all the performance criteria of the design.

3.1.2. Single switch vs Series connected switch configuration:

From Section 2.6, series connected low voltage switch configuration can have the advantage of being more efficient and cost-effective over a single high voltage switch configuration.

In order to evaluate the same, efficiency and cost-based comparison of a single switch and two series-connected switches was done for the current application.

Since the defined grid voltage for operation is selected to be 1400 V, MOSFETS with a drain-source breakdown voltage of 1700 V was taken up for selection evaluation for single switch configuration of buck-boost voltage balancer topology, and MOSFETs with 900 V drain-source breakdown voltage were selected for further scrutiny for two series connected switch configuration. The detailed comparison table based on parameters mentioned in Section 3.1.1 for MOSFET selection is shown in Table A.1 and Table A.2 in Appendix A. Using these tables, the following MOSFETs were selected for evaluation.

- **For single MOSFET configuration: C2M0045170P**
- **For series MOSFET Configuration: C3M0030090K**

3.1.3. MOSFET Loss Calculation:

MOSFETs C2M0045170P and C3M0030090K were evaluated for conduction and switching loss to determine the more efficient configuration.

Conduction Loss Calculation:

For evaluation of Conduction loss of the MOSFET, Equation 2.1 was used, which in turn required determination of I_{Drms} and $R_{(DS)on}$ for the MOSFET.

- **I_{Drms}:** For determination of RMS drain current, Equation B.4 was used from Appendix B.

  For the same the required parameters were determined as described below:

  - **Duty Cycle (D):** The duty cycle (D) for the MOSFET was assumed to be 0.5
  - **Average output current (I_o):** For determination of average current, the voltage and power rating of the balancer (from Section 1.1) was used.

    Using the P_{out} and V_{grid} value of 5 kW and 700 V (voltage across inductor) respectively, the maximum current was found to be $\approx$ 8A. The lower value of current was taken as 2A.

    Using these, the required parameters for rms drain current calculation were determined.

- **R_{DSon}:** For determination of on-resistance, the datasheet of the MOSFET was used. Figure 5 from [38] and [39] shows the on resistance plot of MOSFET C2M0045170P and C3M0030090K vs Drain source current for different temperatures respectively. Using drain-source current in the range of 2A-8A (as described above), the on-resistance was determined.

With I_{Drms} and $R_{(DS)on}$ values known, the conduction loss for both the switches was calculated.

Switching Loss: For calculation of winding loss, equation 2.2 was used, which in turn required determination of E_{On} (Turn-on energy loss), E_{Off} (Turn-off energy loss) and f_s (switching frequency).

- **E_{On}:**For the operation of the MOSFET, it was decided to employ ZVS (Zero Voltage Switching) method during MOSET turn-on i.e., to ensure the voltage across MOSFET drops to zero before gate pulse is provided to turn-on the MOSFET. For this, a negative current of 2A was set to discharge the C_{oss} and achieve ZVS. This negative current value was set after confirmation from LTSpice simulation. Thus, during turn-on, there will be no loss in the MOSFET and therefore E_{on} was neglected.

- **E_{Off}:** For turn off energy loss calculation, Figure 24 from MOSFET datasheet [38] and [39] was used. It shows the switching energy loss for MOSFET as function of drain source current. Using drain-source current in the range of 2A-8A (as described above), the turn off energy loss was determined.

- **f_s:** The switching frequency was determined using Equation B.5, where the inductance (L) value was varied from 500 to 800 μH.

With the required parameters known, the switching loss for both MOSFETs was calculated.

Losses Comparison: Single vs Series connected MOSFET

For these calculations it has been assumed that for both configurations, there are no non-linearities in the system.

Figure 3.1 and Figure 3.2 shows the Winding and Conduction losses for single and series connected MOSFET for 700 μH inductance value as a function of switching frequency.

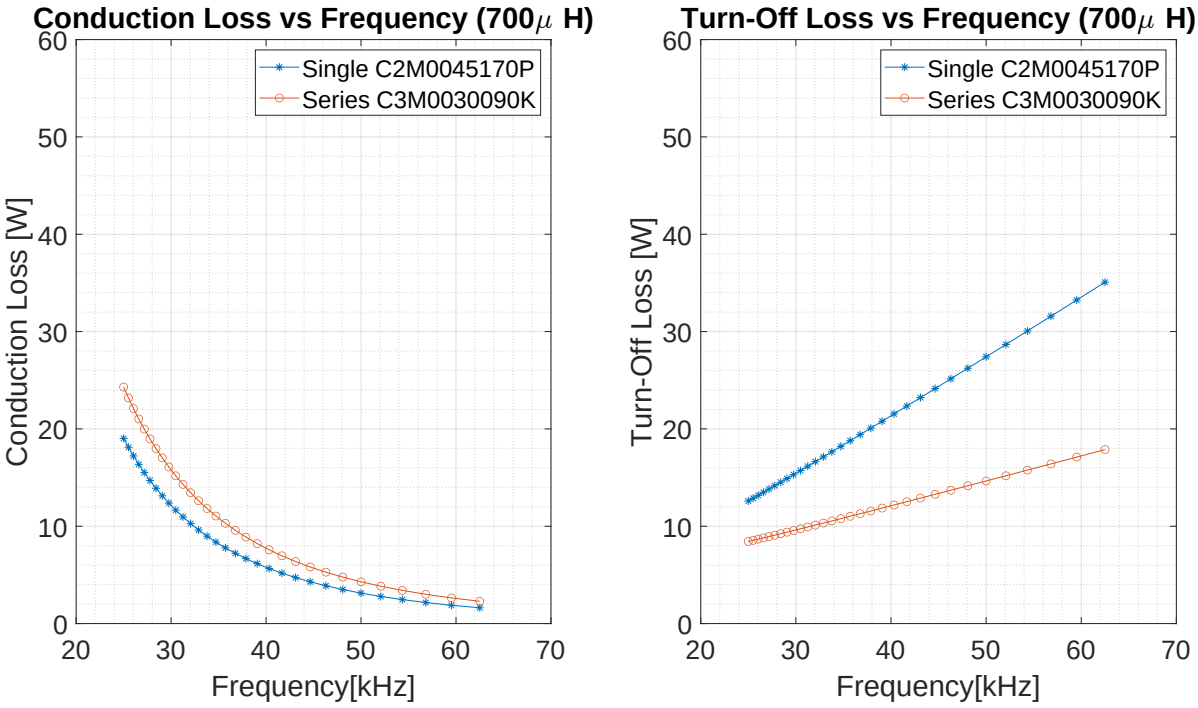


Figure 3.1: Conduction and Turn-off loss vs Frequency for single and series connected MOSFET for 700 μH inductance value. The conduction loss for series connected MOSFET is higher than for single MOSFET. However, Turn-off loss for single MOSFET is much higher than for series connected MOSFET.

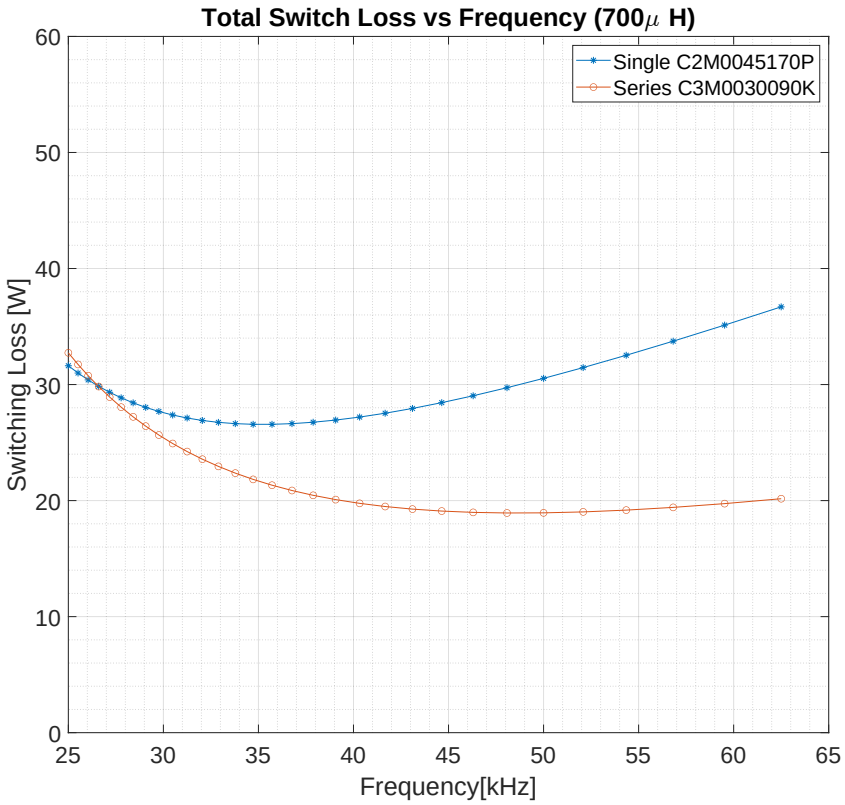


Figure 3.2: Total switch loss vs Frequency for single and series connected MOSFET for 700 μH inductance value. The total switching loss (sum of Conduction and Turnoff loss) for single connected MOSFET is much higher than for series connected MOSFET

Based on MOSFET loss comparison, it can be concluded that series connected MOSFET (C3M0030090K) has lower switching loss than single connected MOSFET (C2M0045170P).

Hence, **MOSFET C3M0030090K connected in series** was finalised as the switch for the voltage balancer design.

3.2. Inductor design: Parameterisation and Optimisation of magnetic circuit

In this section the inductor design, which includes the inductor core material selection, core selection, and the magnetic circuit design is covered.

3.2.1. Core Material Selection:

In order to design the magnetic core for an inductor, majorly two broad classes of materials are used, which are described below:

- **Magnetic steel**: It is an alloy of Iron with small amounts of Chrome and Silicon. Its main characteristics are listed below:
  i. It has high electrical conductivity as its major constituent is Iron.
  ii. It has high values of saturation flux density, near to 1.8T [31].
  iii. It has two types of losses: hysteresis loss and eddy current loss.

iv. Since it has high electrical conductivity, the eddy current loss is significant in magnetic steel. Consequently, its usage is usually limited to low-frequency applications.

v. It requires lamination of the core in order to reduce eddy current losses even at a modest frequency of 60Hz.

- **Ferrites**: It is a mixture of Iron oxide and other magnetic elements such as Zinc, Nickel, Barium, etc. Its main characteristics are listed below:

  i. It has high electrical resistivity.

  ii. It has low saturation flux densities, typically about 0.3T [31].

  iii. It has only hysteresis loss. Since it has large electrical resistivity, the eddy current induced is minimal thus resulting in no significant eddy current loss.

  iv. It is suitable for high-frequency operation (greater than 10kHz) because of low eddy current loss.

  v. Further, no lamination is needed because of the high resistivity of the material thus making it more compact than magnetic steel cores.

For the current project, it is intended to operate the voltage balancer at high frequency ($\geq$ 10kHz). Consequently, the magnetic steel cores will not be suitable for the current application, as they are susceptible to high eddy current losses at high-frequency operation. Based on this factor, Ferrite materials were finalised as the core material for the magnetic design of the inductor.

Further under the ferrite materials, different materials are available for magnetic design purposes. In order to further identify the most suitable material amongst the Ferrite group for the magnetic design, the available materials were evaluated for the following parameters:

i. **Frequency of operation:** Target operation range : 10-100kHz

ii. **Performance factor plot:** Figure A.3 shows the Performance factor plot for various ferrite core materials for the specific power loss of 500 mWcm^{-3} [40]. It can be seen that for the frequency range of up to 100kHz, 3C90, 3C94, and 3C96 materials are suitable.

Also, 3C92 material has been recommended for inductor applications with frequency operation $\leq$200 kHz.

Based on above factors, ferrite materials **3C90**, **3C92**, **3C94** and **3C96** were used for further evaluation and inductor design.

3.2.2. Core Selection:

The overall process used for the design of the magnetic circuit, which was to finalise the core and core material is shown in Figure 3.3 below.

The following parameters and constants were pre-defined for the core selection process and the same was included in the MATLAB code (C.1.2) as constant values.

Symbol	Parameter	Unit	Value
J_{rms}	RMS value of current density	[Amm^{-2}]	4
k	Filling factor	[-]	0.3

Symbol	Parameter	Unit	Value
B	Magnetic flux density	[mT]	225
μ	permeability of free space	[H$m^{-}1$]	$4\pi10^{-7}$
A_{cu}	Cross-sectional area of copper winding	[mm^2]	5
ρ	resistivity of copper	[Ωm]	1.72*10^{-8}
k,α, β	Steinmetz Coefficient	[-]	from [41]

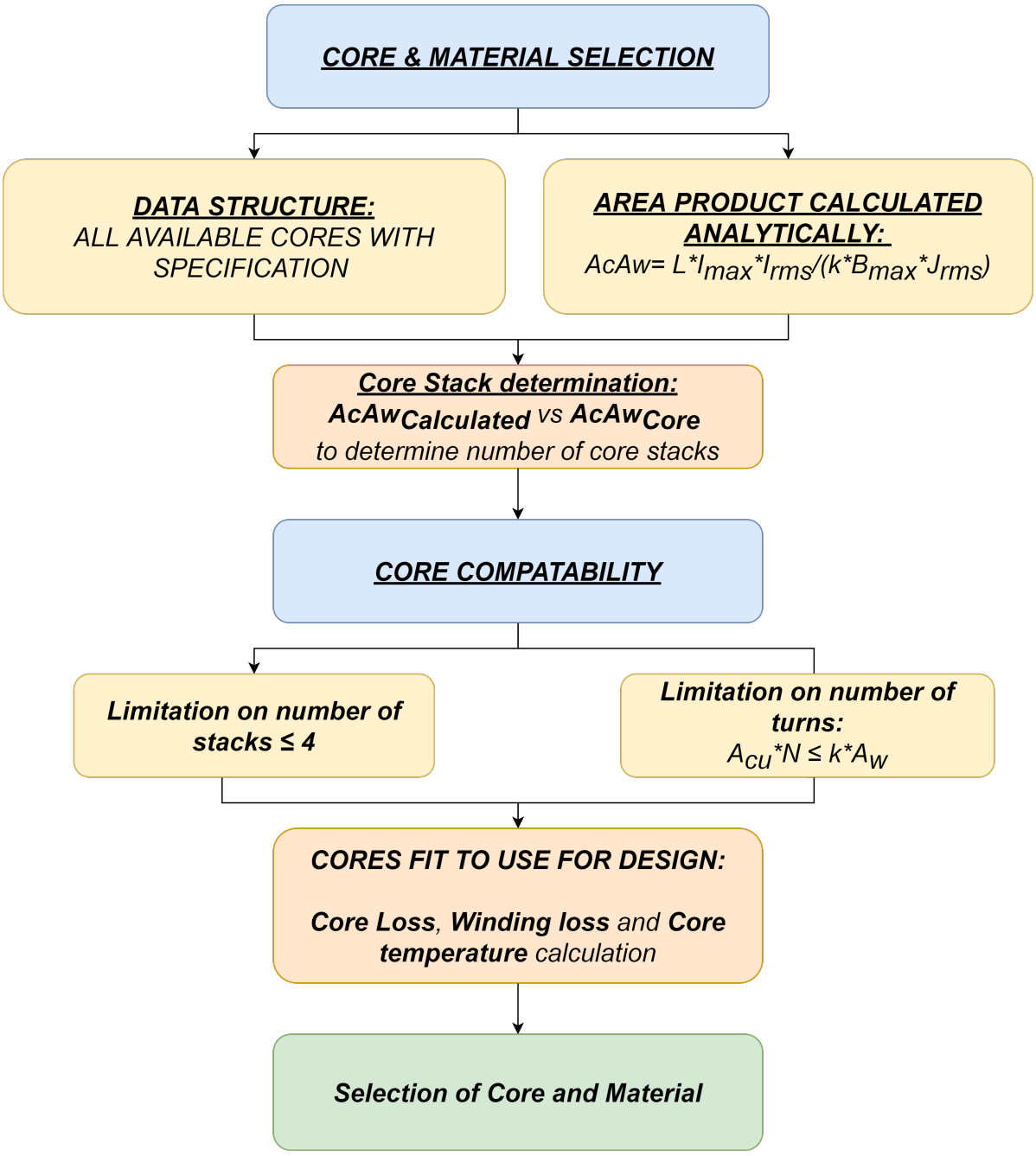


Figure 3.3: Magnetic circuit design procedure used for parameterization and Optimisation of the design

The process and the results are explained in detail below:

Data Structure:

For the first step, a data structure matrix with core specification details and dimensions for different core types was prepared. Depending on the core compatibility criteria,(explained later in the next steps) the final core was chosen from this core data matrix.

Figure 3.4 shows the data matrix for EE Core type depicting the core specification and dimensions which were collated in the data matrix for different core types. The data for this matrix was collected from [42].

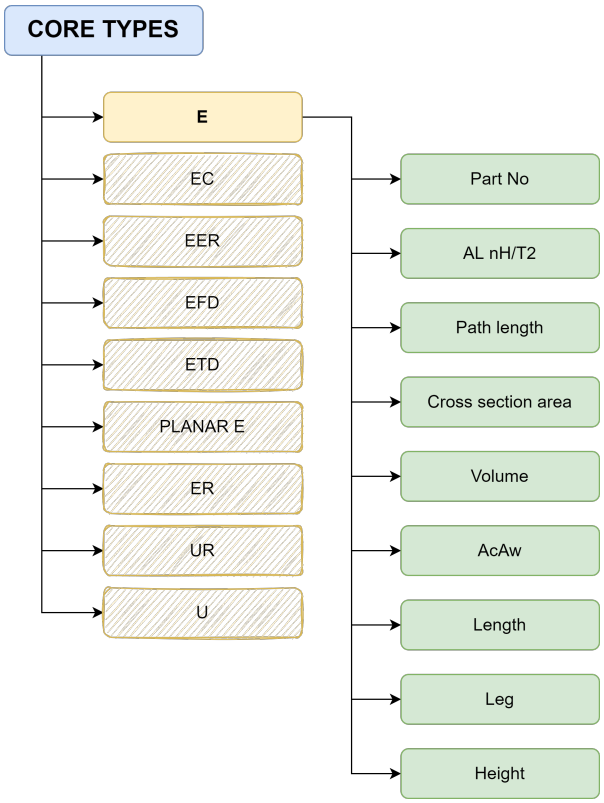


Figure 3.4: Schematic representation of the data matrix showing the core specification and data collated for **'E'** core type to be used for finalising core type for the magnetic circuit design

Calculation of Area product (A_cA_w) parameter:

There are two limits adhered by the inductor design process namely:

- Saturation limit given by the relation:

$$LI_{\text{max}} = NB_{\text{max}}A_c \tag{3.1}$$

- Thermal limit given by the equation below:

$$NI_{\text{rms}} = kA_wJ \tag{3.2}$$

The area product relation is obtained by combining Equation 3.1 and 3.2. To design an inductor, a core is needed in which the area of the magnetic path (A_c) and area of the core window (A_w) satisfy this relation.

$$AcAw = \frac{L^* I^*_{max} I_{rms}}{k * B_{max} * J_{rms}} \tag{3.3}$$

where:

Symbol	Parameter	Unit
A_cA_w	Area Product Parameter	[m^4]
L	Inductance	[H]
I_{max}	Peak current in the circuit	[A]
I_{rms}	RMS current in the circuit	[A]
k	Filling factor	[-]
B_{max}	Maximum magnetic flux density	[Wb m^{-2} or T]
J_{rms}	RMS value of current density	[Am^{-2}]

The area product was calculated for three scenarios: for load corresponding to maximum frequency, highest load, and an operating load point which was somewhere in between these two extremes. The maximum of the three area products obtained was chosen. This was done to take the worst-case scenario and choose the core accordingly. Same has been implemented in the MATLAB code in C.1.2, Appendix C.

Comparison of Area product:

The next step was to compare the calculated Area product parameter with the Area product of the different cores from the core data structure matrix 3.2.2.

For a core to be used in the magnetic circuit the following condition should hold.

$$(A_cA_w)_{calc} \leq (A_cA_w)_{core} \tag{3.4}$$

where:

Symbol	Parameter	Unit
$(A_cA_w)_{calc}$	Area Product Parameter calculated	[m^4]
$(A_cA_w)_{core}$	Area Product Parameter of core	[m^4]

However, for the case where equation 3.4 does not hold, it was calculated how many of the cores will have to be stacked together in order to meet the criteria of equation 3.4. For this, Equation 3.5 was used.

$$N_{stacked} = Roundup(\frac{(A_cA_w)_{calc}}{(A_cA_w)_{core}}) \tag{3.5}$$

where:

Symbol	Parameter	Unit
$N_{stacked}$	Number of cores stacked together	[-]

Core Compatibility:

The core compatibility was determined based on the two criteria mentioned below:

1. **Limitation on stack numbers:** For the current project it was decided to limit the maximum number of cores stacked together to 4.

Note: It should be noted that the number of stacks can be higher and can be decided based on the volume requirement of the inductor to be designed. For this thesis, the number was chosen to be 4.

2. **Limitation on the number of turns:** The next criteria was based on the limitation on the number of turns of wire in the core. The number of turns should be such that the total copper area must be less than the window area of the core. The same was calculated using equation 3.6 below:

$$A_{cu} * N_{turns} \leq k * A_w \tag{3.6}$$

where

Symbol	Parameter	Unit
A_{cu}	Area of copper wire used for winding	[m^2]
N_{turns}	Number of turns in winding	[-]
k	Filling factor	[-]
A_w	Window area of the core	[m^2]

Based on the above two parameters, the cores compatible with the design criteria are identified from the core data matrix.

Core Compatibility Results:

Out of all the cores in the data structure considered for the designing of the inductor, only a few part numbers of the E core were classified for further scrutiny.

Core and Winding loss calculation:

For the cores compatible with the design criteria the losses, i.e., Core loss and Winding loss are calculated.

For **Core loss** calculation Steinmetz equation 3.7 below is used:

$$P_{core} = V_e * k * f^{\alpha} * B^{\beta} \tag{3.7}$$

where

Symbol	Parameter	Unit
P_{core}	Core loss	[W]
V_e	Volume of core	[m^3]
k,α, β	Steinmetz Coefficient	[-]
f	Frequency	[Hz]
B	Magnetic flux density	[Wm^{-2} or T]

However, equation 3.7 is applicable for only sinusoidal current waveforms flowing through the inductor coil. For the current work, the current waveform is triangular, for which the Steinmetz coefficient k is modified to k_i as given in equation 3.8 below:

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{3.8}$$

where

Symbol	Parameter	Unit
k_i	Modified Steinmetz coefficient	[-]
θ	-	[radian]

Using equation 3.7 and 3.8, the following equation 3.9 for core loss is obtained:

$$P_{core} = \frac{V_e}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{3.9}$$

where

Symbol	Parameter	Unit
T_s	Time period of switch	[s]

Equation 3.9 is further simplified to give equation 3.10, which is then used to calculate the core loss.

$$P_{core} = V_e \frac{k_i (\Delta B)^{\beta-\alpha}}{T_s} \cdot \left(\left| \frac{\Delta B}{D T_s} \right|^{\alpha} D T_s + \left| \frac{\Delta B}{(1-D) T_s} \right|^{\alpha} (1-D) T_s \right) \tag{3.10}$$

where

Symbol	Parameter	Unit
ΔB	Change in Magnetic flux density	[Wm^{-2} or T]
D	Duty Cycle	[-]

For calculation of ΔB, equation 3.11 and 3.12 are used, which gives the final equation 3.13 for ΔB:

$$v_L = \frac{d\phi}{dt} = L \frac{di}{dt} \tag{3.11}$$

where

Symbol	Parameter	Unit
v_L	Voltage across inductor	[V]
$\frac{d\phi}{dt}$	Rate of change in flux	[Ws^{-1}]

$$\Delta B = \frac{1}{N \cdot A_c} \int_0^{DT} v_L dt \tag{3.12}$$

where

Symbol	Parameter	Unit
N	Number of turns	[]
A_c	Area of core	[m^2]

$$\Delta B = L\frac{\Delta i_L}{N \cdot A_c} \tag{3.13}$$

where

Symbol	Parameter	Unit
ΔB	Change in flux density	[Wm^{-2} or T]
L	Inductance	[Farad]
ΔI_L	Change in inductor current	[A]

Winding loss: Due to its high conductivity and ductility, copper is chosen as the material of choice for inductor winding. High conductivity and ductility ensure minimizing the volume and weight of the windings by minimizing the amount of copper needed for the windings. The heat dissipated in these windings is calculated using the equation 3.14 below:

$$P_{winding} = I_{RMS}^2 \cdot R_{DC} \tag{3.14}$$

where

Symbol	Parameter	Unit
$P_{winding}$	Winding loss	[W]
I_{rms}	RMS Current	[A]
R_{DC}	Resistance of copper wire	[Ω]

Core Temperature calculation:

For core temperature calculation, the rise in core temperature (ΔT_{core}) is calculated by using the equation 3.15. This ΔT_{core} is added to the initial core temperature to calculate the final core temperature as given in equation 3.16.

$$\Delta T_{core} = (\Sigma P_{loss} * A_{core})^{0.833} \tag{3.15}$$

where

Symbol	Parameter	Unit
ΔT_{Core}	Rise in core Temperature	[K]
ΣP_{loss}	Total power loss	[W]
A_{core}	Surface area of core	[m^2]

$$T_{Core} = T_{initial} + \Delta T_{core} \tag{3.16}$$

where

Symbol	Parameter	Unit
T_{Core}	Final core Temperature	[K]
$T_{initial}$	Initial core temperature	[K]

For the core temperature calculation an iterative loop was developed in MATLAB (see Appendix C. An initial temperature at the start of the loop is assumed which is updated to the calculated core temperature at the end of the calculation loop. The loop continues till the calculated converter loss value converges to a defined threshold (1W).

3.3. Magnetic design results:

3.3.1. Converter loss calculation:

Using Equation 3.10, Equation 3.14, Equation 2.2, and Equation 2.1 the core loss (P_{core}), winding loss ($P_{winding}$), Turn off switching loss ($P_{MOS-switching}$) and conduction loss ($P_{conduction}$) are determined respectively. These losses are then added to get the total converter loss as shown in Equation 3.17 below:

$$P_{converter} = P_{core} + P_{winding} + P_{MOS-switching} + P_{winding} \tag{3.17}$$

The equations for loss calculations in the converter, described in the previous sections (3.1.3, 3.2.2) were modeled in MATLAB. Using the MATLAB model, the total converter loss for series switch configuration, for different core materials (finalized for inductor design, i.e., 3C90, 3C92, 3C94, and 3C96 (see section 3.2.1) are calculated for different operating frequencies and inductance values.

The results of these calculations are shown below:

Figure 3.5 shows the total converter loss as a function of switch operating frequencies for different inductance values and different E core part numbers for 3C90 and 3C92 ferrite core material.

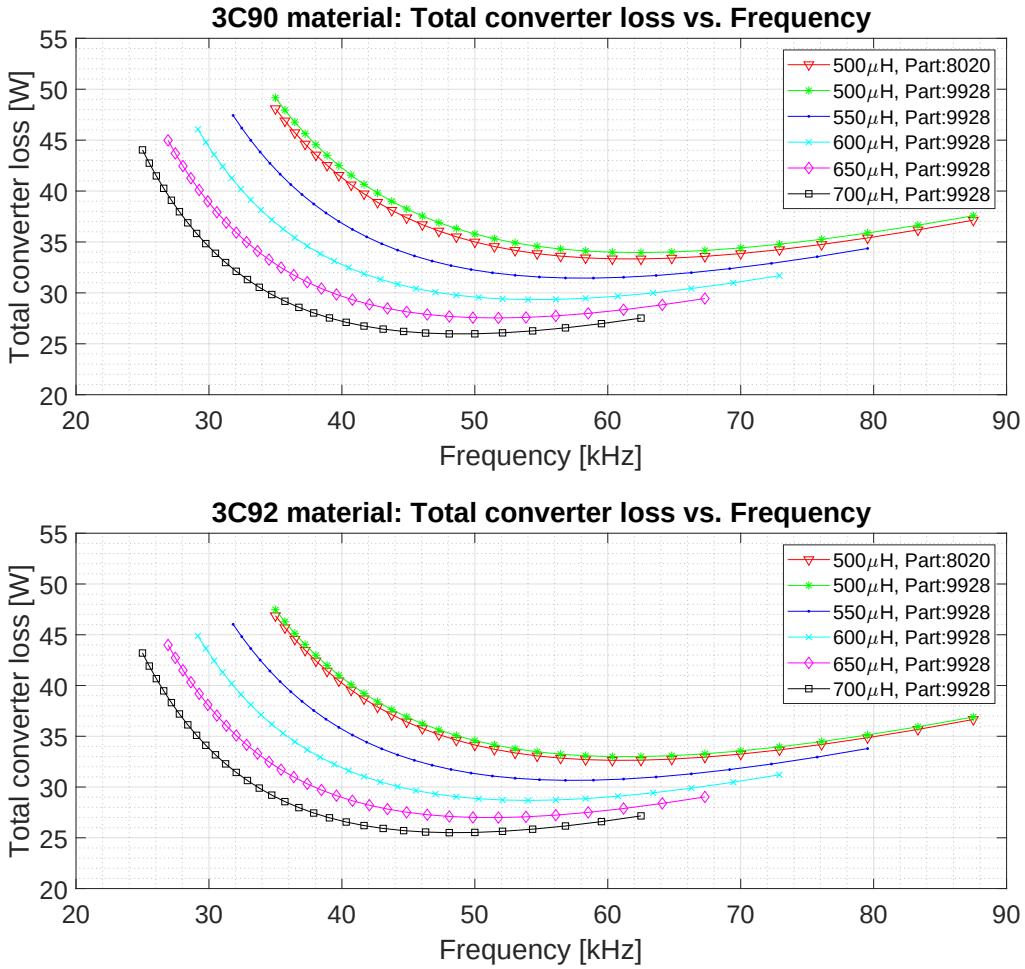


Figure 3.5: Total Converter Loss vs Frequency for 3C90 and 3C92 material for EE core. It can be observed that for both materials 3C90 and 3C92, total converter loss initially decreases with an increase in frequency, reaches a minimum value, and then again starts increasing. Further, the minimum power loss is observed for the highest inductance value of 700μH and part number 9928 for both 3C90 and 3C92 material

Similar to Figure 3.5, in Figure 3.6, total converter loss as a function of switch operating frequencies are shown for different inductance and E core part numbers for 3C94 and 3C96 core material.

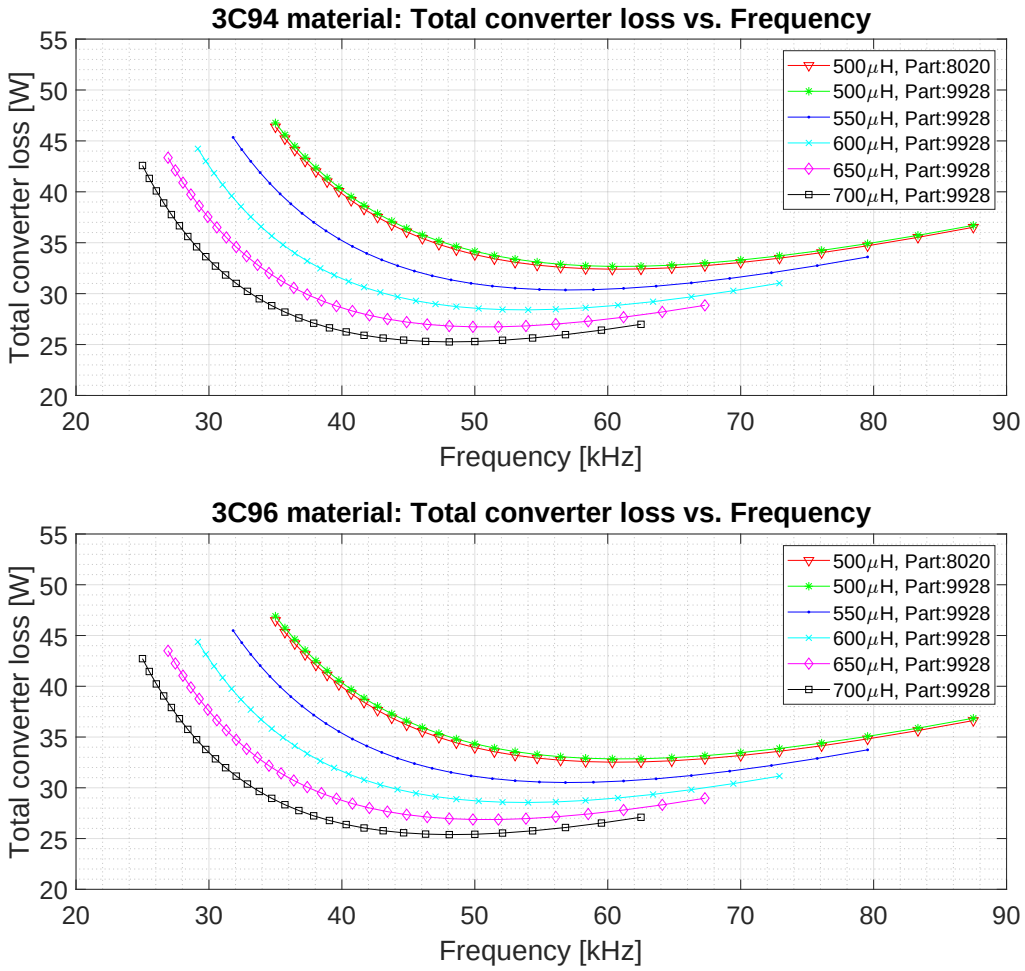


Figure 3.6: Total Converter Loss vs Frequency for 3C94 and 3C96 material for EE core. It can be observed that for both materials 3C94 and 3C96, total converter loss initially decreases with an increase in frequency, reaches a minimum value, and then again starts increasing. Further, the minimum power loss is observed for the highest inductance value of 700μH and part number 9928 for both 3C94 and 3C96 material

From Figure 3.5 and Figure 3.6 following inferences were drawn:

- Total converter loss for all core materials and inductance values show a similar trend. The loss value initially decreases with an increase in frequency, reaches a minimum value, and then starts increasing for a higher operating frequency.

- For all core materials and part numbers, the minimum converter loss was obtained for the highest compatible inductance value of 700μH.

Since the minimum converter loss was obtained for an inductance value of 700μH for all core materials and part numbers so, in order to identify the most suitable core for the inductor, the converter loss value for 700μ for all materials, i.e., 3C90, 3C92, 3C94, and 3C96 as seen in Figure 3.5 and Figure 3.6 were compared. The same is shown in Figure 3.7 below:

From Figure 3.7, the minimum converter loss was observed for core material 3C94 and part number 9928 for E core configuration.

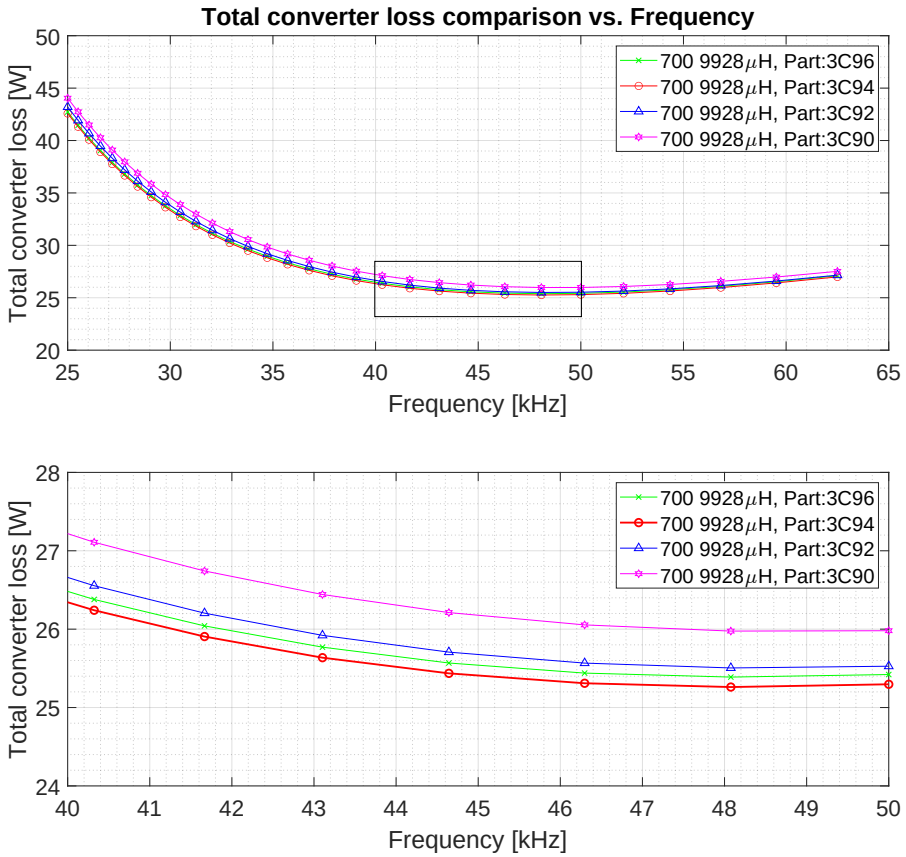


Figure 3.7: Total Converter loss vs Frequency for 700μH and part no 9928 for 3C90,3C92,3C94 and 3C96 material. The minimum converter loss obtained for each material, as seen in Figure[3.5] and Figure[3.6 are compared and it can be seen that for 3C94 material the total converter loss is observed to be the minimum at all operating frequencies.

Final core temperature was also determined for all the core materials for 'E' core 9928, as described in section 3.2.2. The results of the same are presented in Figure 3.8 below;

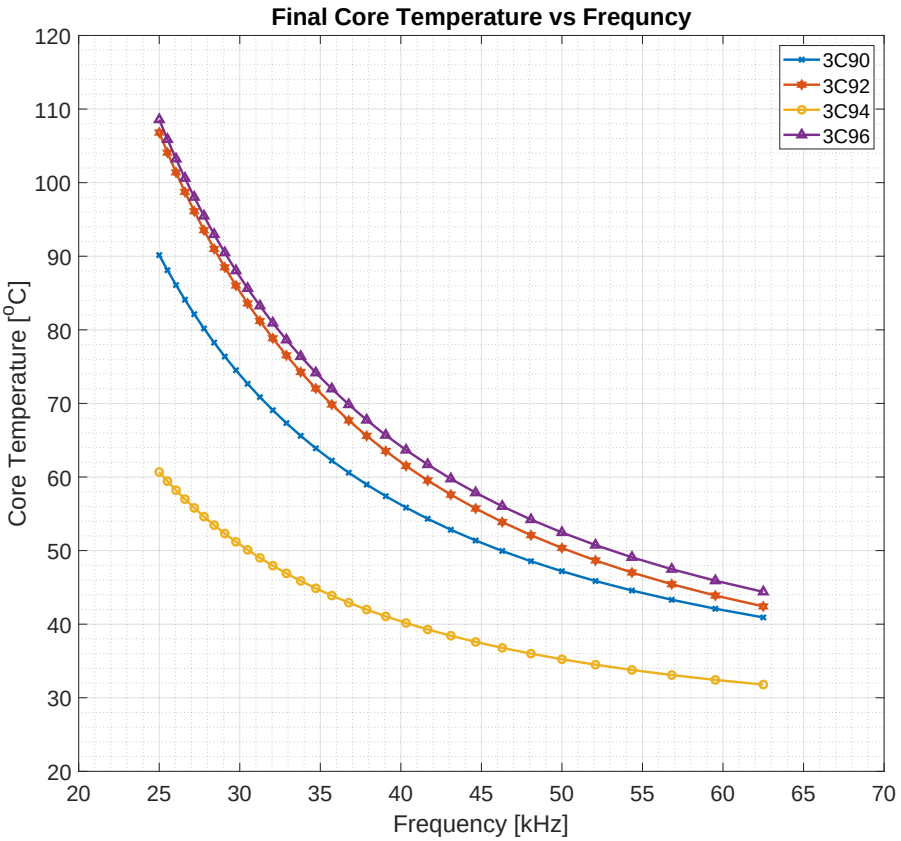


Figure 3.8: Final core temperature for all core materials

The final design for the magnetic circuit is shown in Table[3.16] below:

Table 3.16: Final Inductor design parameters

Parameter	Value	Unit
Inductance	700	μH
Core Material	Ferrite Core: 3C94	-
Core Shape	E Core	-
Core Part	Part No: 9928	-

For the final design, to understand the contribution of different magnetic losses towards total converter loss, the different losses were plotted in a stacked bar graph as shown in Figure 3.9 below.

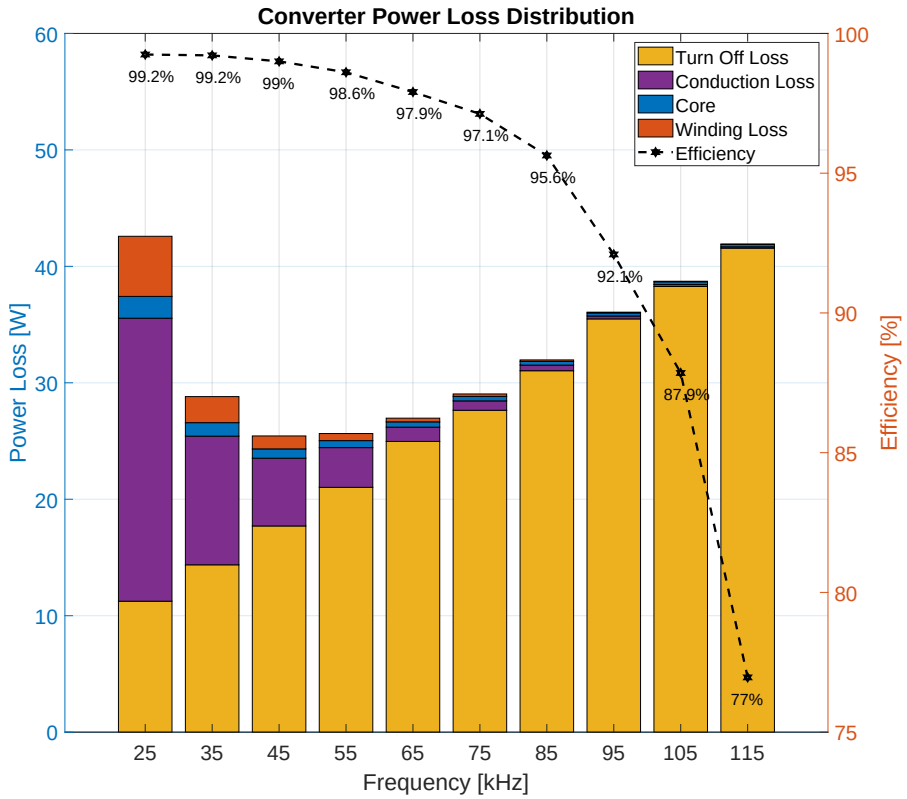


Figure 3.9: Converter loss distribution and Efficiency (displayed at the top of each bar) for different operating frequencies

It can be seen that turn-off loss and conduction loss are the dominant sources of losses in the magnetic design. Further, apart from turn-off losses all other types of losses decrease with an increase in frequency, while turn-off loss increases with the frequency of operation. Moreover, the efficiency of the converter decreases with an increase in frequency or with light loads.

4
LTSpice Simulation:

In this section the LTSpice simulation performed on the different configurations of the series-connected synchronous buck-boost voltage balancer is presented. The simulations performed for different non-linearities present in the circuit are also presented.

4.1. Series Connected Voltage Balancer:

The equivalent circuit for the series-connected synchronous buck-boost voltage balancer converter, modeled on LTSpice is shown in Figure 4.1.

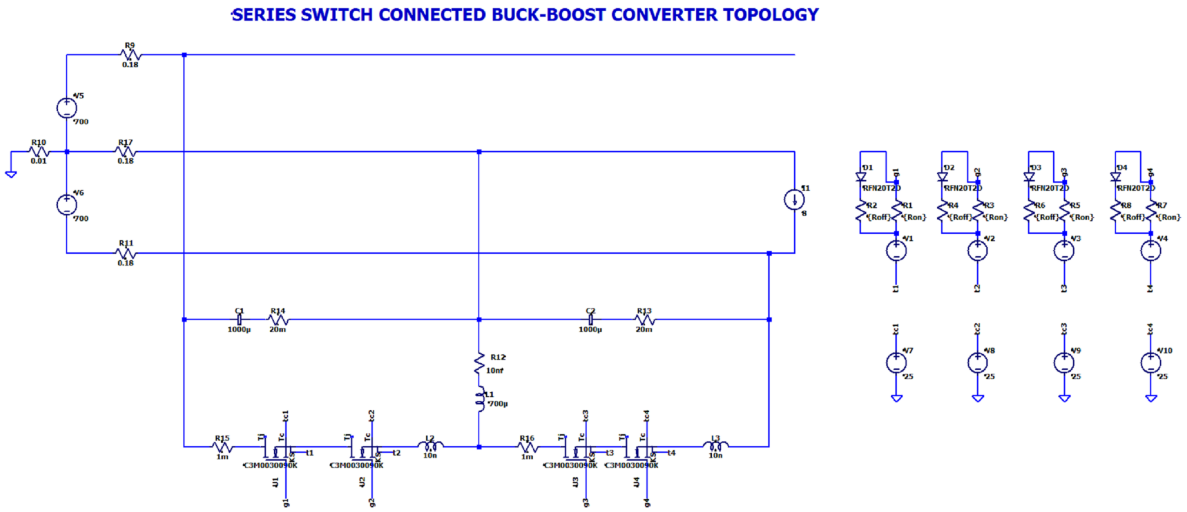


Figure 4.1: Equivalent circuit of the series connected synchronous voltage balancer topology

The simulation is performed with the following operating conditions (Table 4.1):

Table 4.1: Operating parameters for the LTspice simulation:

Parameter	Value	Unit
Frequency	24.65	**kHz**
Duty Cycle	0.5025	**-**
Dead Time	220	**ns**

A starting value of frequency was chosen from the MATLAB result corresponding to 8A load and 700 μH inductance. This was obtained as 25 kHz. Frequency was then adjusted to 24.65kHz to balance the phase voltages and currents and to limit the neutral current to less than 30mA for human safety [43]. Dead time was set to obtain ZVS at turn-on and the duty cycle was set so as to get the negative current of 2A which is then used to completely discharge the C_{oss} during dead time.

4.2. Voltage Balancer without non-linearity:

Figure 4.2 and Figure 4.3 below show the Phase voltages, phase currents, and switch voltages across switches 1-2 and switch 3-4 during turn-on respectively. The condition presented here is for no non-linearity in the circuit.

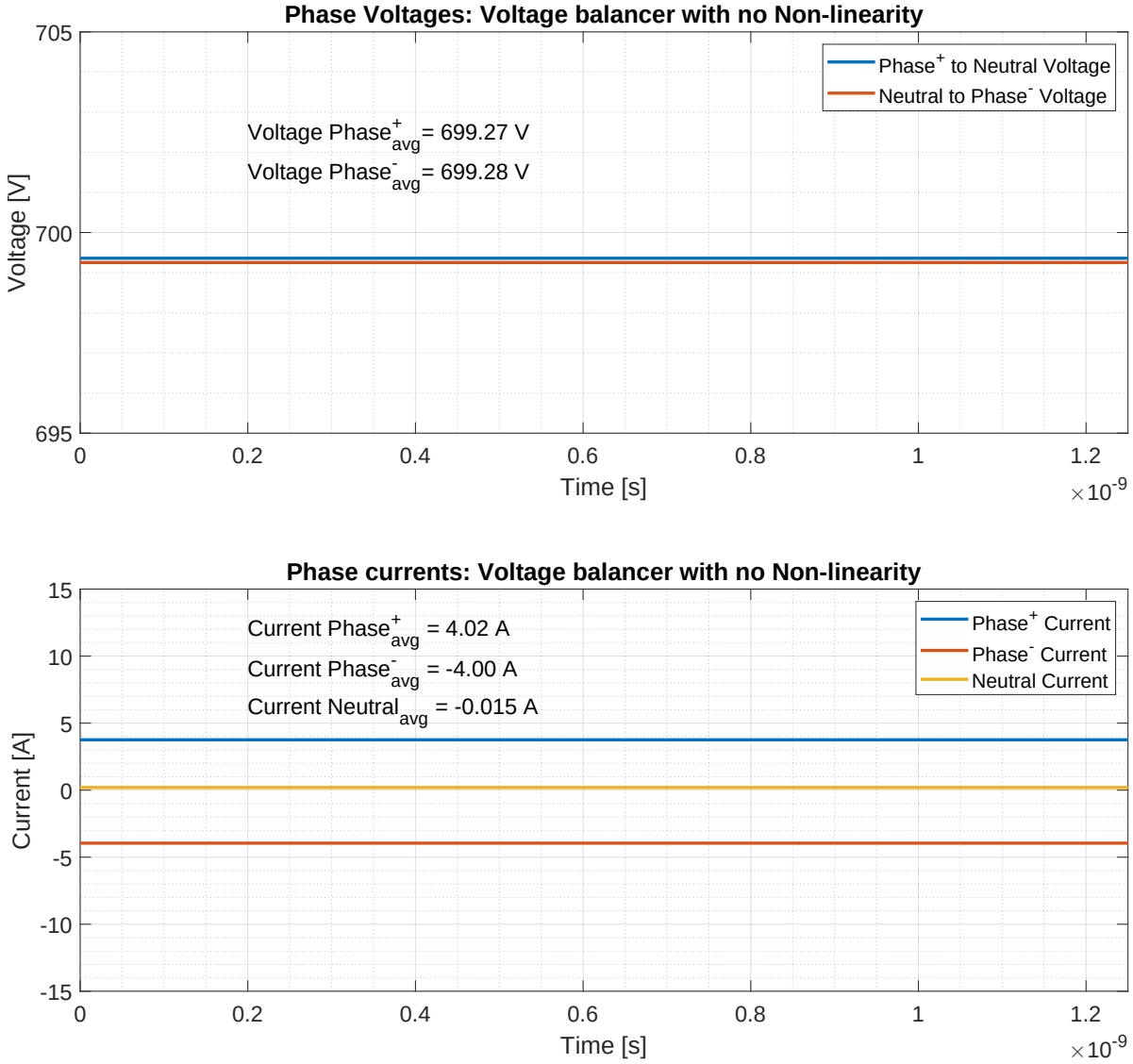


Figure 4.2: Phase voltage and current in series connected voltage balancer without non-Linearity. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are in balance. Further, the neutral line current is practically zero.

Table 4.2: LTSpice simulation results of phase voltage and current for series connected voltage balancer without non-linearity

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.27	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.28	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.02	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	-0.015	A

As can be seen in Figure 4.2 and Table 4.2, the voltage across both positive to neutral and neutral to negative phase lines is well balanced (Voltage difference $\leq$ V). Additionally, the current through the neutral line is negligible ($\leq$ 0.03A), indicating a well-balanced system.

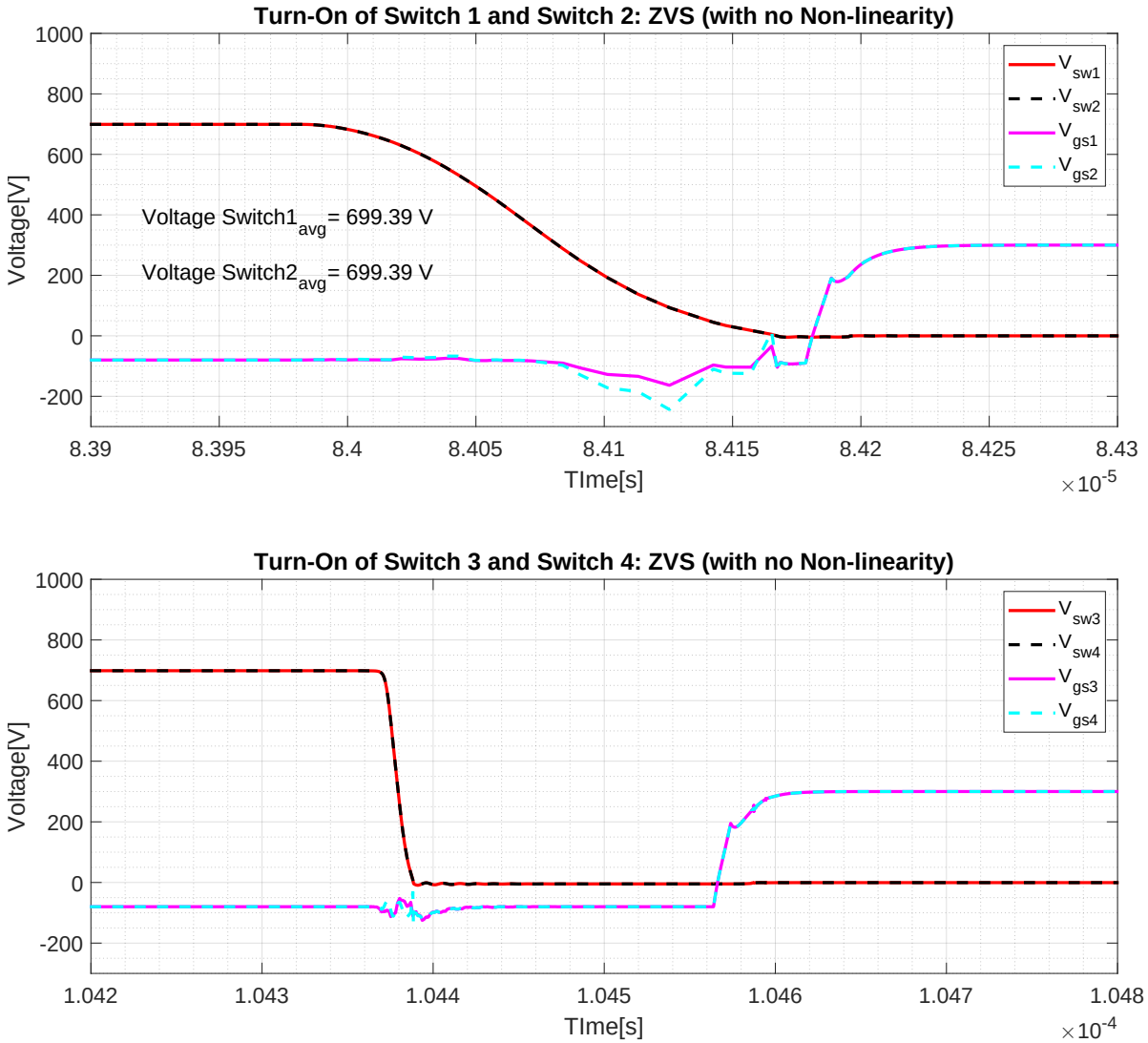


Figure 4.3: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer without non-Linearity. It can be observed that for both Switches 1-2 and Switches 3-4, ZVS at Turn-on is being achieved. Further, the average voltage over Switch 1 and Switch 2 is the same, indicating that voltage is equally distributed between the switches

Table 4.3: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer without non-linearity

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	699.39	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	699.39	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

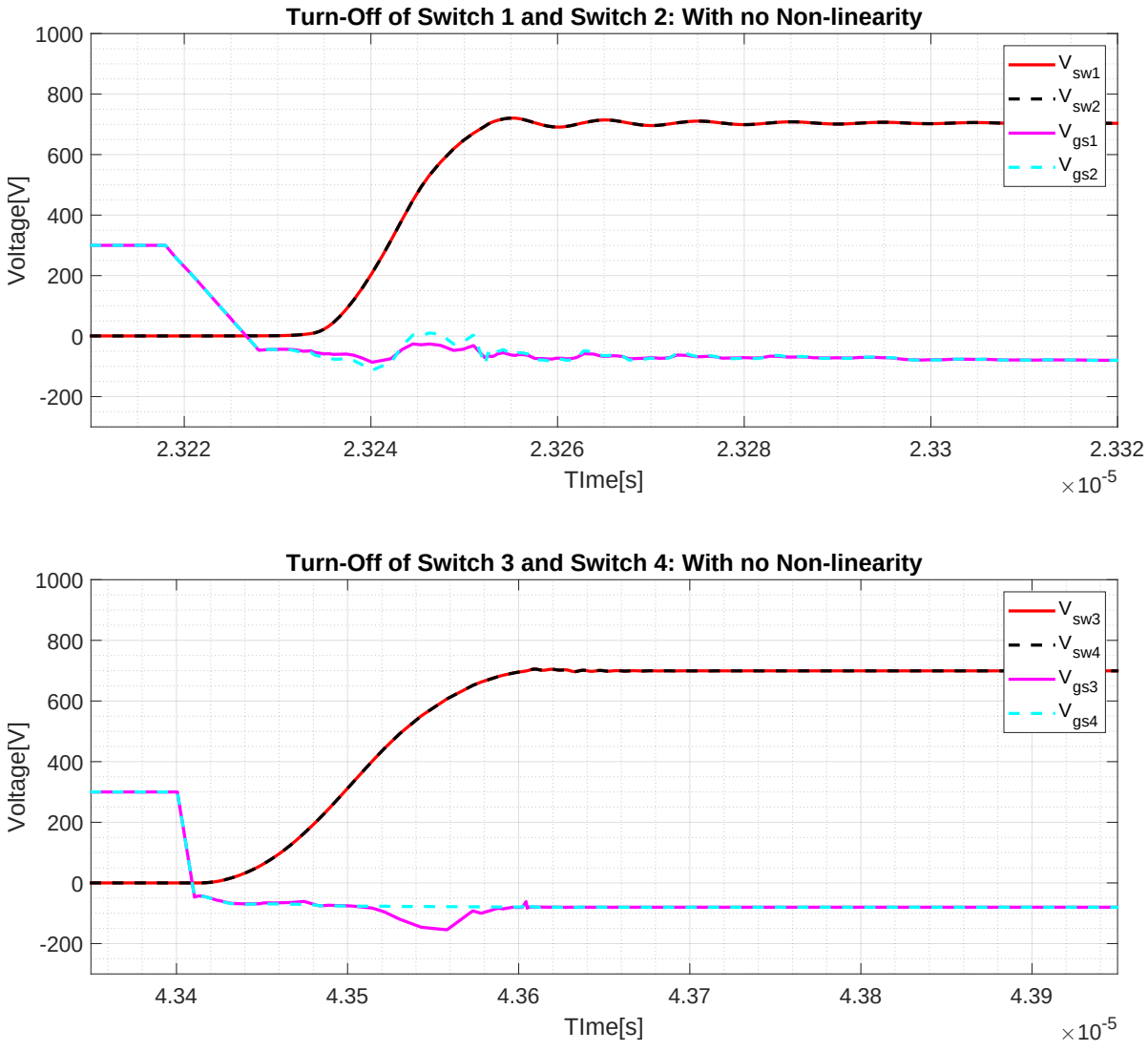


Figure 4.4: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer without Non-linearity

From Figure 4.3 and Table 4.3 it can be seen that the voltage across both series connected switches, Switch 1-2 and Switch 3-4 is well balanced and ZVS is ensured at Turn-on. Figure 4.4 shows the system behaviour at Turn-Off condition and as can be seen, the voltage across the switches is well balanced.

4.3. Series Connected Voltage Balancer with Non-Linearity

In this section, LTSpice simulation results for series connected voltage balancers with different non-linearity are presented. The same was briefly discussed in section 2.6.

4.3.1. R_{on}= 2.5 Ω with $\pm$ 5% tolerance

In this section, the system behaviour due to non-linearity arising in the circuit owing to tolerance in resistors used in external gate resistance of the MOSFET is presented. The tolerance value was selected based on data from [36] and was chosen as $\pm$ 5 % for 2.5 Ω resistor. For Switch 3-4, no non-linearity was considered.

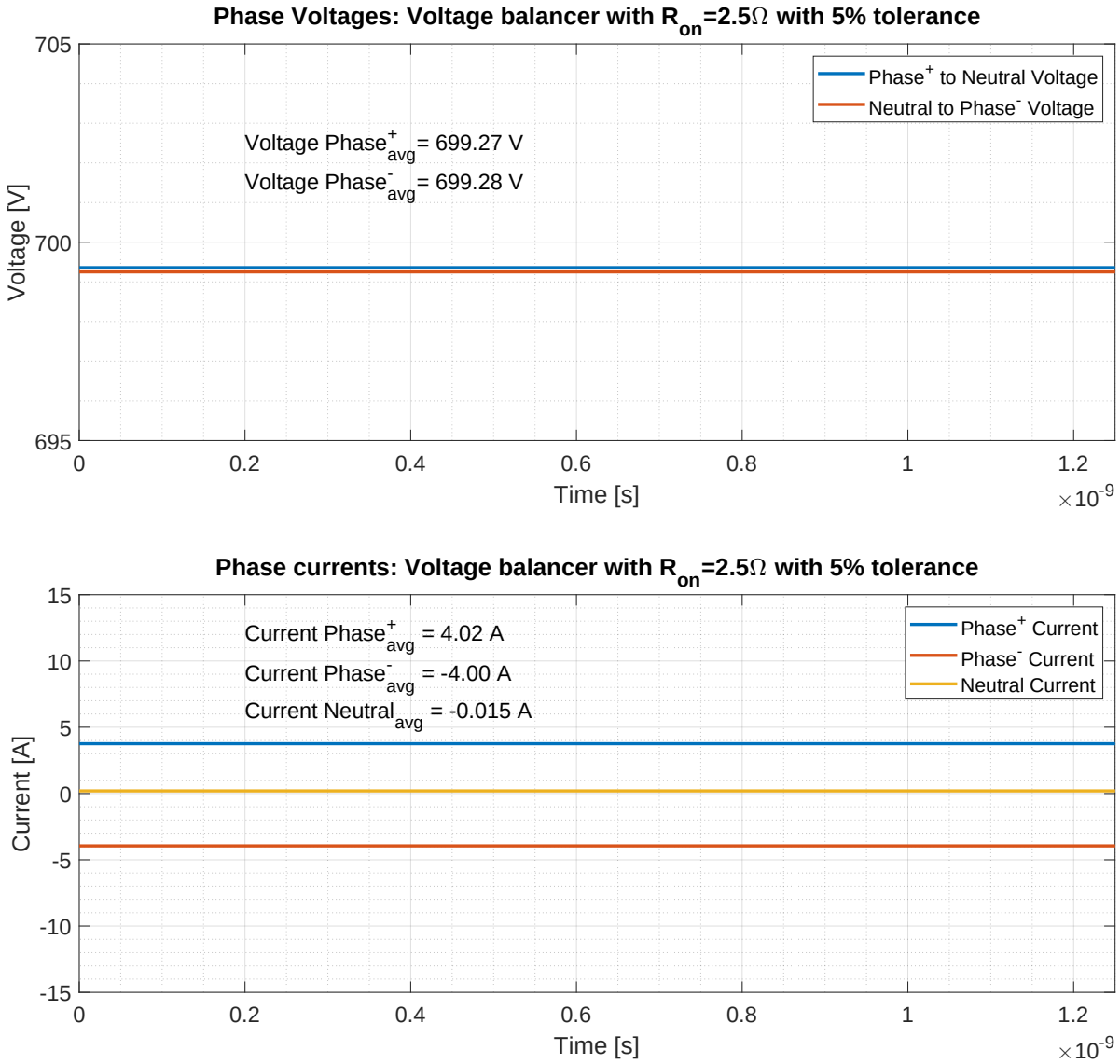


Figure 4.5: Phase voltage and current in series connected voltage balancer with non-Linearity: R_{on}= 2.5 Ω with $\pm$ 5% tolerance. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are in balance. Further, the neutral line current is practically zero.

Table 4.4: LTSpice simulation results for series connected voltage balancer with non-linearity: R_{on}= 2.5 Ω with ± 5% tolerance

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.27	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.28	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.02	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	-0.015	A

As can be seen from Figure 4.5 and Table 4.4, the voltage across both positive to neutral and neutral to negative phase lines is well balanced. Additionally, the current through the neutral line is negligible ($\leq$ 0.03A), indicating a well-balanced system.

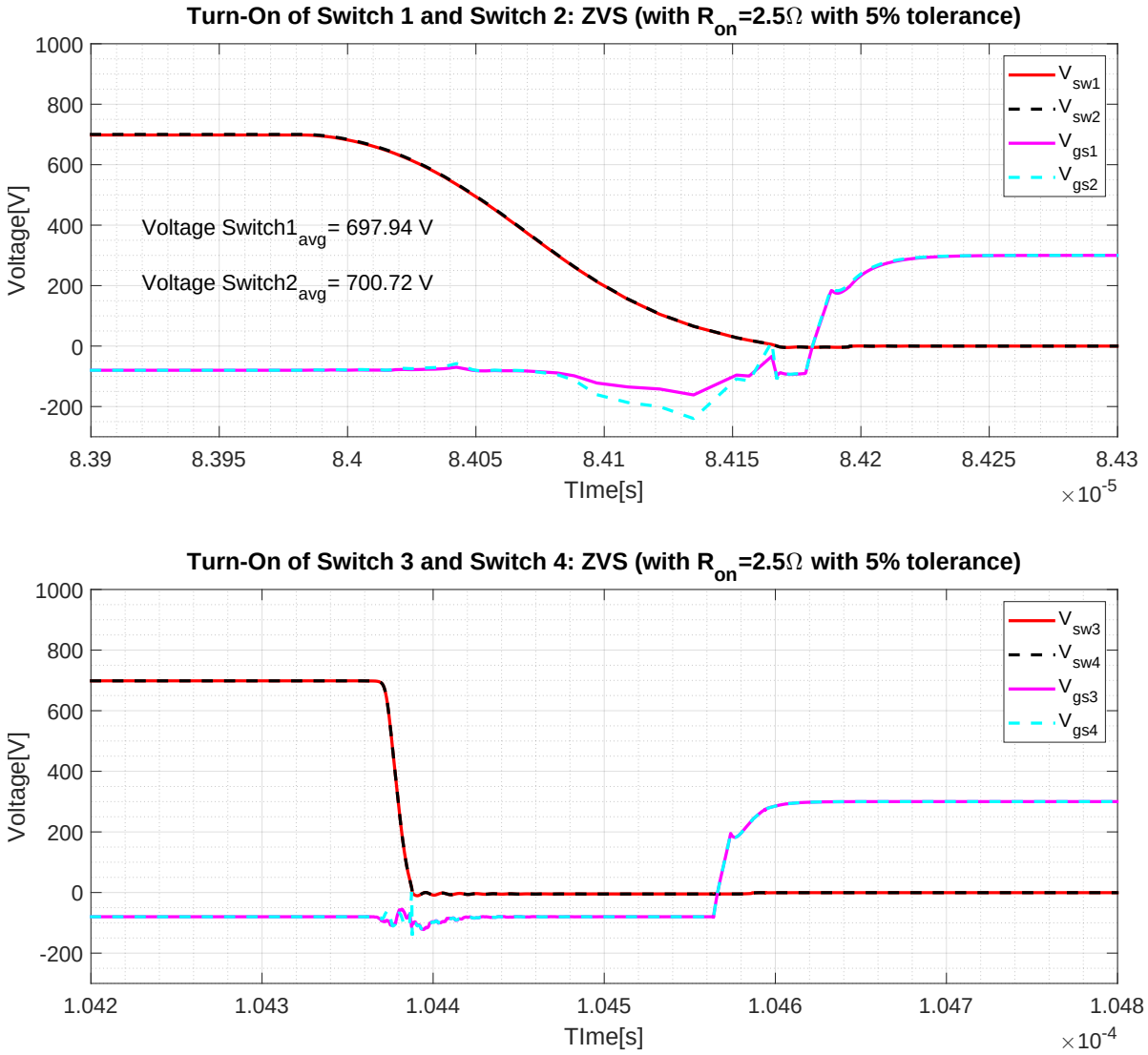


Figure 4.6: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: R_{on}=2.5 Ω. It can be observed that for both Switches 1-2 and Switch 3-4, ZVS at Turn-on is being achieved. Further, the average voltage over Switch 1 and Switch 2 is the same for 1 time period indicating that voltage is equally distributed between the switches.

Table 4.5: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity:R_{on}= 2.5 Ω with $\pm$ 5% tolerance

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	699.39	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	699.39	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

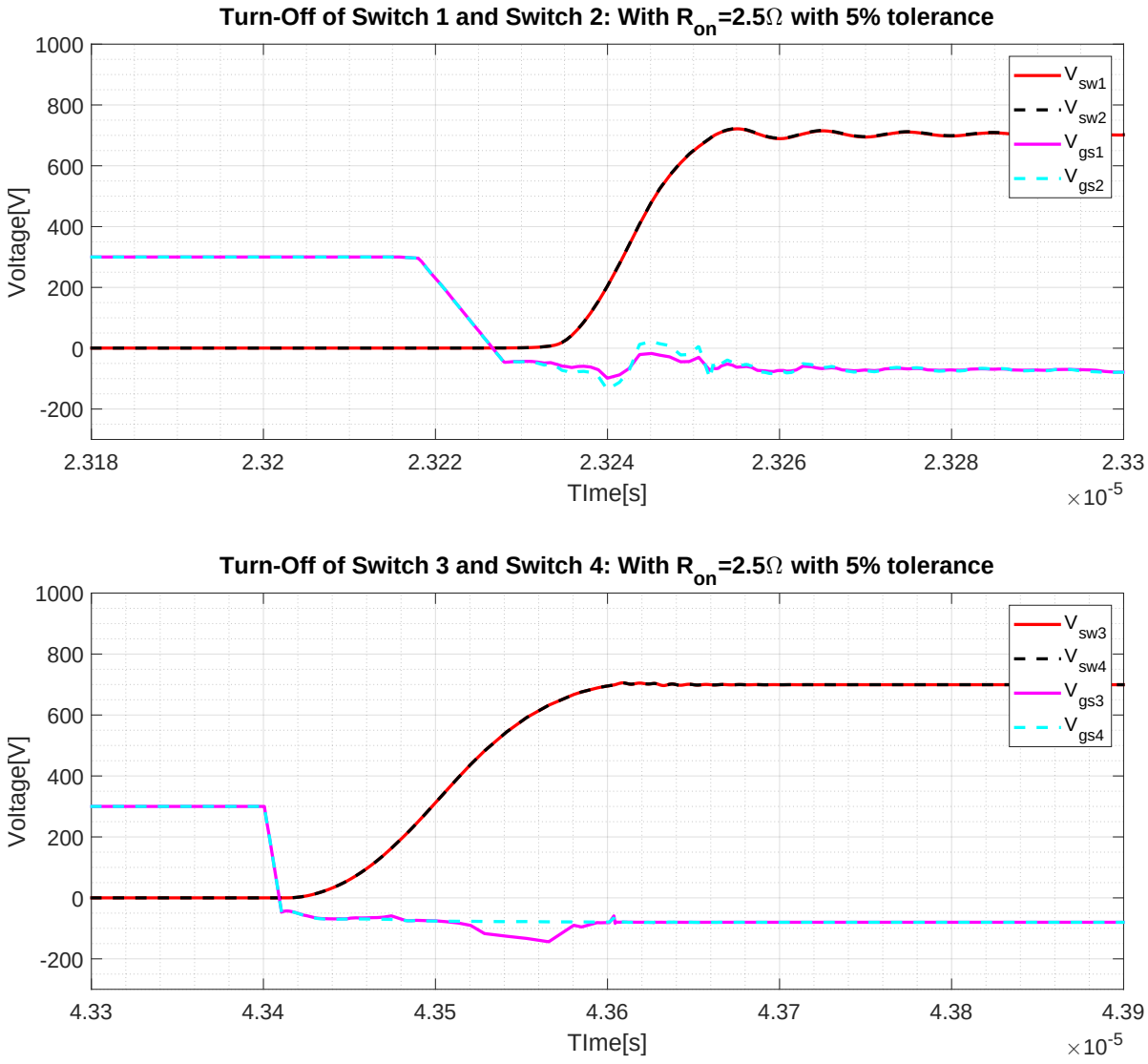


Figure 4.7: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity R_{on}=2.5Ω

As seen from Figure 4.6 and Table 4.5, the voltage across both series connected switches, Switch 1-2 and Switch 3-4 is well balanced and ZVS is ensured at Turn-on.

Figure 4.13 shows the system behaviour at Turn-Off and as can be seen the voltage across the switches is well balanced.

Thus it can be concluded that non-linearity arising due to tolerance in external gate resistance has a negligible effect on the voltage balancer performance.

4.3.2. Parasitic Capacitance: 20pF

The MOSFET has three capacitors connected between the three terminals of the device (Figure 2.13). However, there are multiple parasitic capacitances that are also present between different connections within the MOSFET package, external gate drivers, and ground. These parasitic capacitors can alter the system behaviour and the same was simulated using LTSpice. Below, the results for the Parasitic capacitance value of 20pF across Switch 1-2 (Figure 4.1) are presented. For Switch 3-4, no non-linearity was considered.

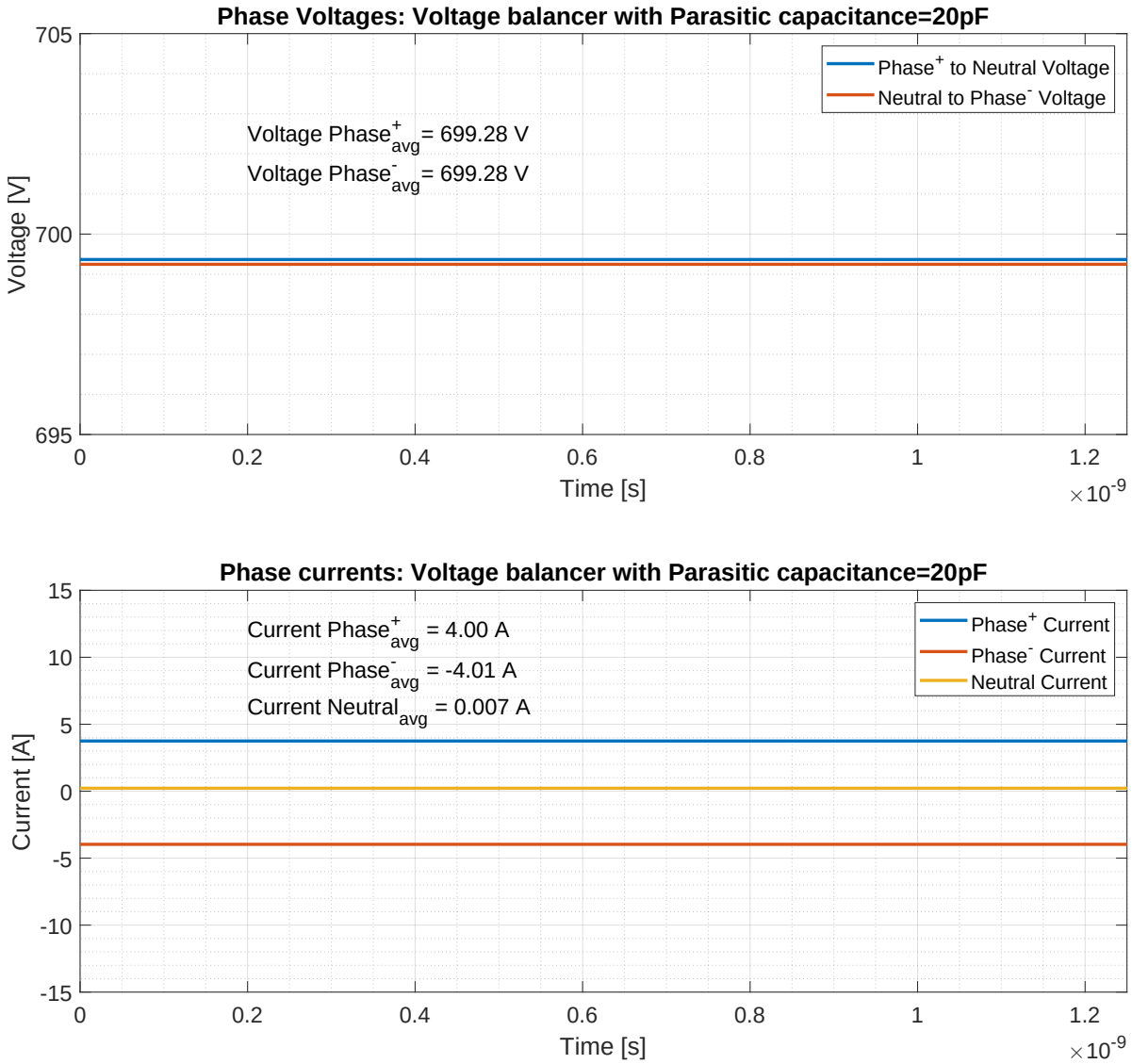


Figure 4.8: Phase voltage and current in series connected voltage balancer with non-Linearity: Parasitic Capacitance:20pF. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are in balance. Further, the neutral line current is practically zero.

Table 4.6: LTSpice simulation results for series connected voltage balancer with non-linearity: Parasitic capacitance=20pF

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.28	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.28	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.0	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.01	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	0.007	A

As can be seen from Figure 4.8 and Table 4.6, the voltage across both positive to neutral and neutral to negative phase lines is well balanced. Additionally, the current through the neutral line is negligible ($\leq$ 0.03A), indicating a well-balanced system.
However, as compared to the case with no non-linearity and with external gate resistance non-linearity (Table 4.4 and Table 4.2), the direction of current through the neutral line is reversed.

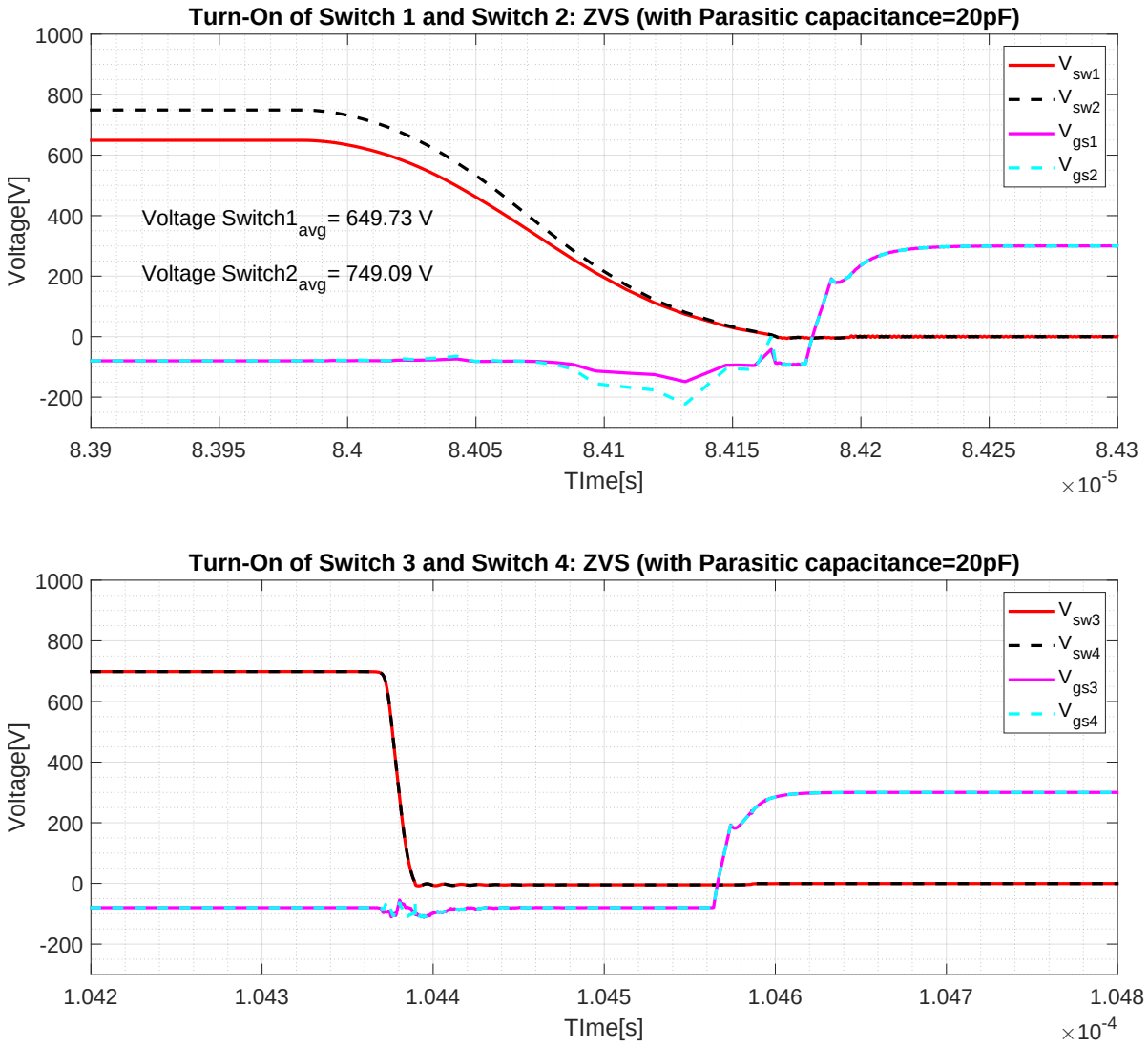


Figure 4.9: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Parasitic Capacitance:20pF. It can be observed that for both Switches 1-2 and Switch 3-4, ZVS at Turn-on is being achieved. However, the average voltage over Switch 1 and Switch 2 is different.

Table 4.7: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Parasitic capacitance=20pF

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	649.73	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	749.09	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

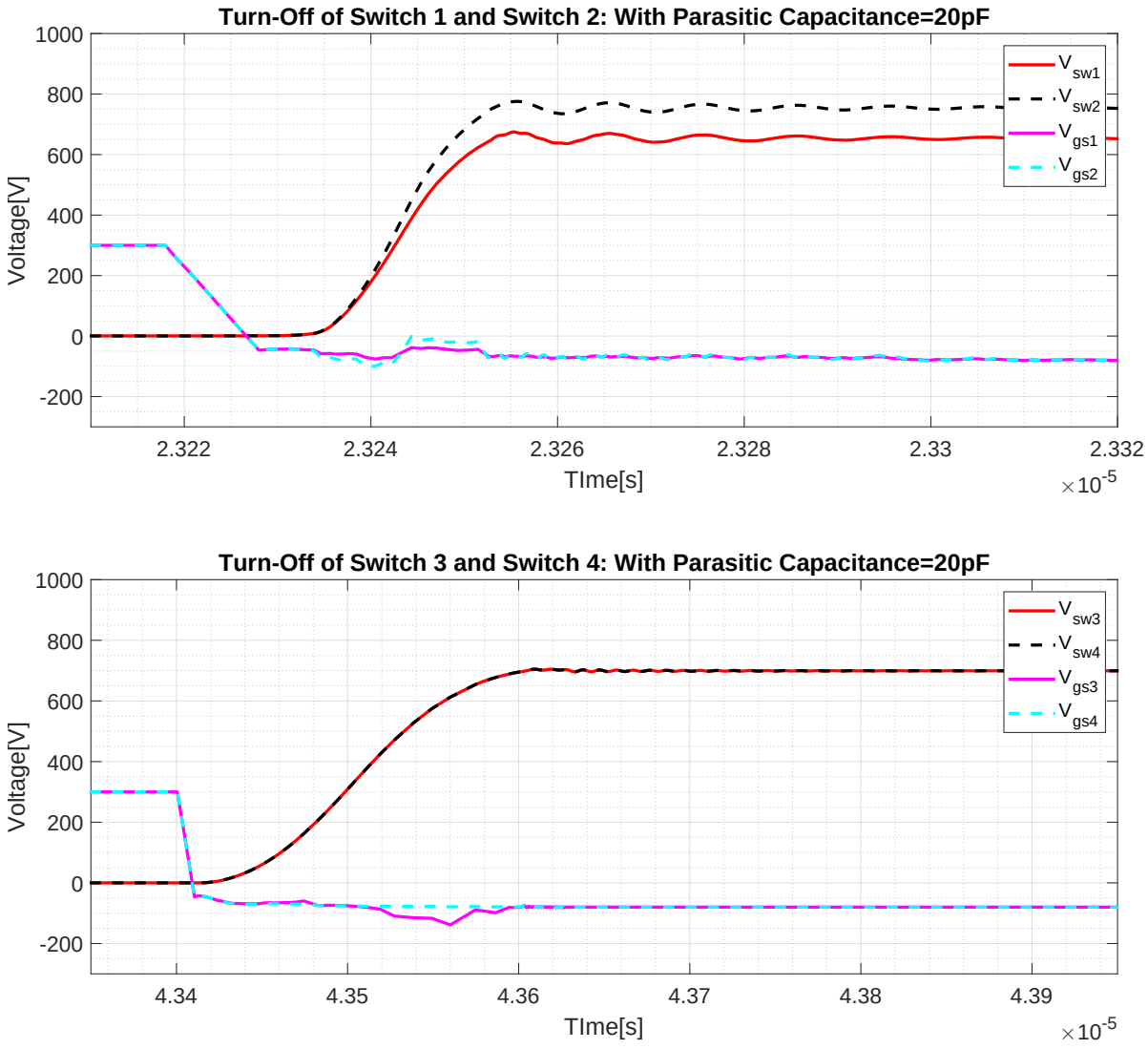


Figure 4.10: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity Parasitic capacitance 20pF

As seen from Figure 4.9 and Table 4.7, the voltage across Switch 1-2 is no more balanced, although ZVS at Turn-on is still ensured. For Switch 3-4, the voltage is balanced.

Figure 4.10 shows the system behaviour at Turn-Off and similar to Turn-on, the voltage across Switch 3-4 is balanced, but an un-equal voltage sharing can be observed across Switch 1-2.

4.3.3. Parasitic Capacitance: 100pF

For this case, the simulation was performed for a higher parasitic capacitance of 100pF across Switch 1 and 2. The results are presented below. For Switch 3-4, no non-linearity was considered.

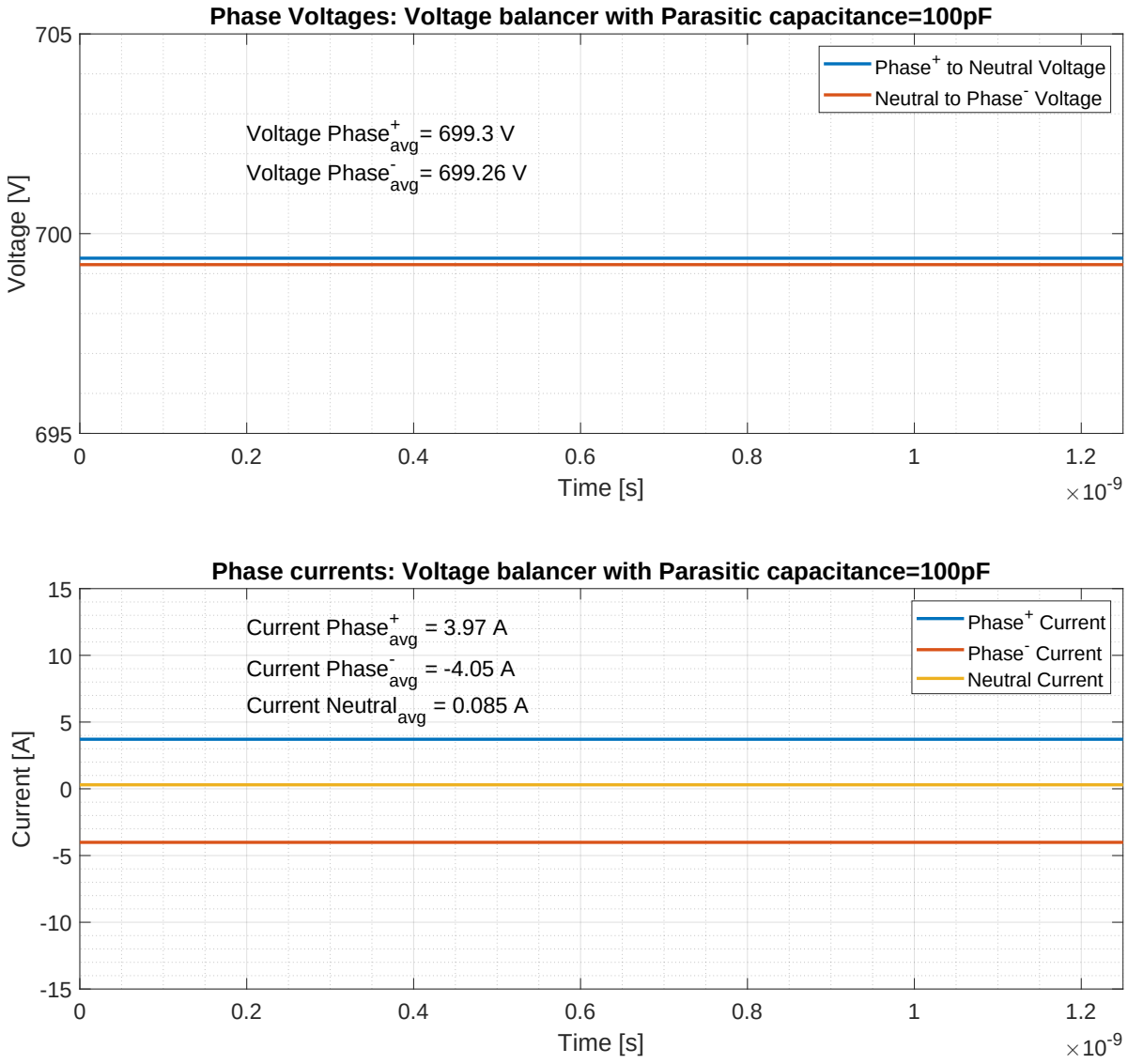


Figure 4.11: Phase voltage and current in series connected voltage balancer with non-Linearity: Parasitic Capacitance:100pF, shown for 1 time period. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are in balance. Further, the neutral line current is practically zero.

Table 4.8: LTSpice simulation results for series connected voltage balancer with non-linearity: Parasitic capacitance=100pF

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.3	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.26	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	3.97	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.05	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	0.085	A

As can be seen in Figure 4.11 and Table 4.8, the voltage across both positive to neutral and neutral to negative phase lines is no more balanced ($DeltaV$ between positive and negative phase 0.3V).

Additionally, the current through the neutral line is now higher than 0.03A, indicating an unbalanced system. Further, the current through the positive and neutral line are no longer equal in magnitude.

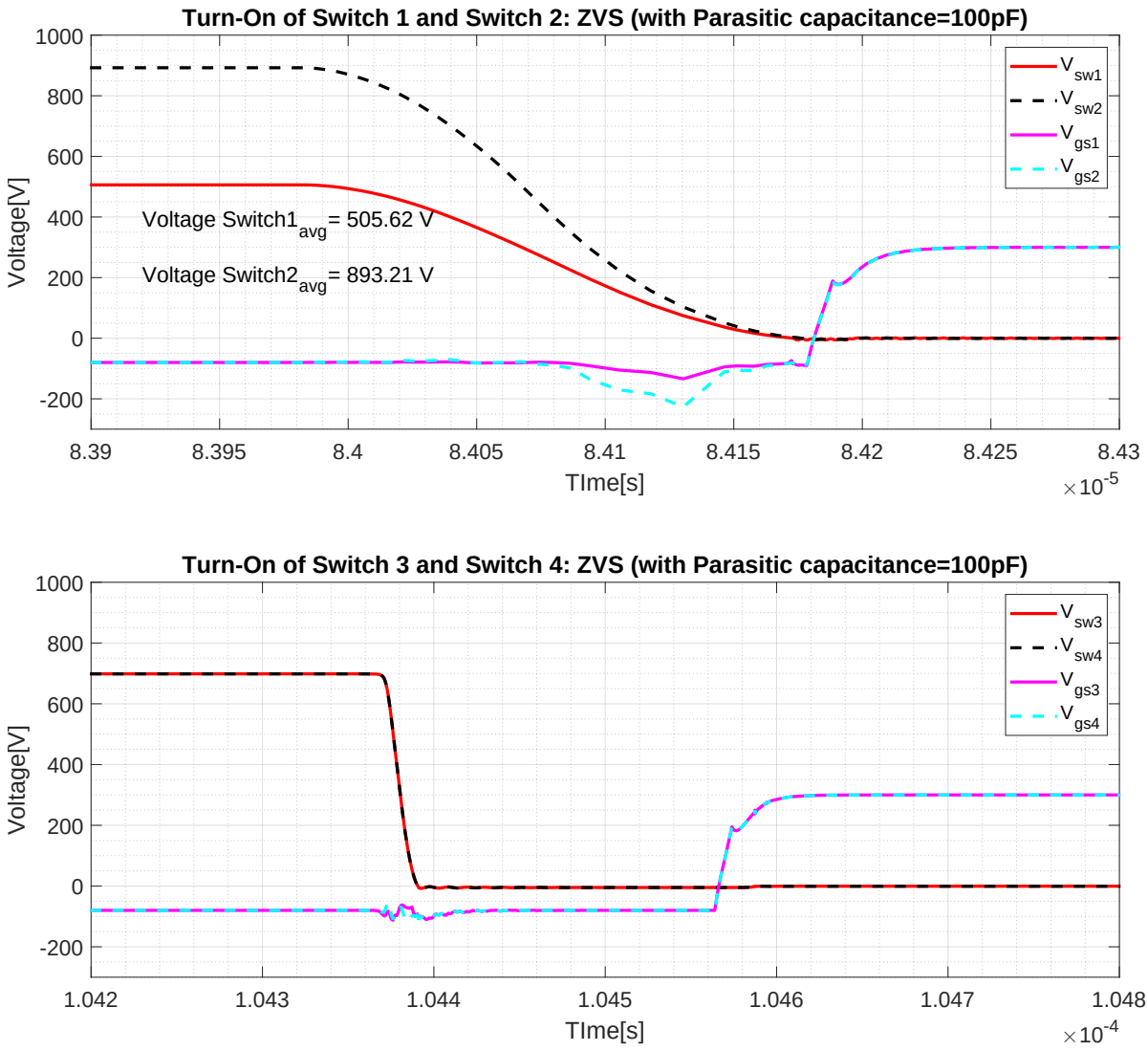


Figure 4.12: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Parasitic Capacitance:100pF. It can be observed that for both Switches 1-2 and Switch 3-4, ZVS at Turn-on is being achieved. However, the average voltage over Switch 1 and Switch 2 is different.

Table 4.9: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Parasitic capacitance=100pF

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	505.62	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	893.21	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

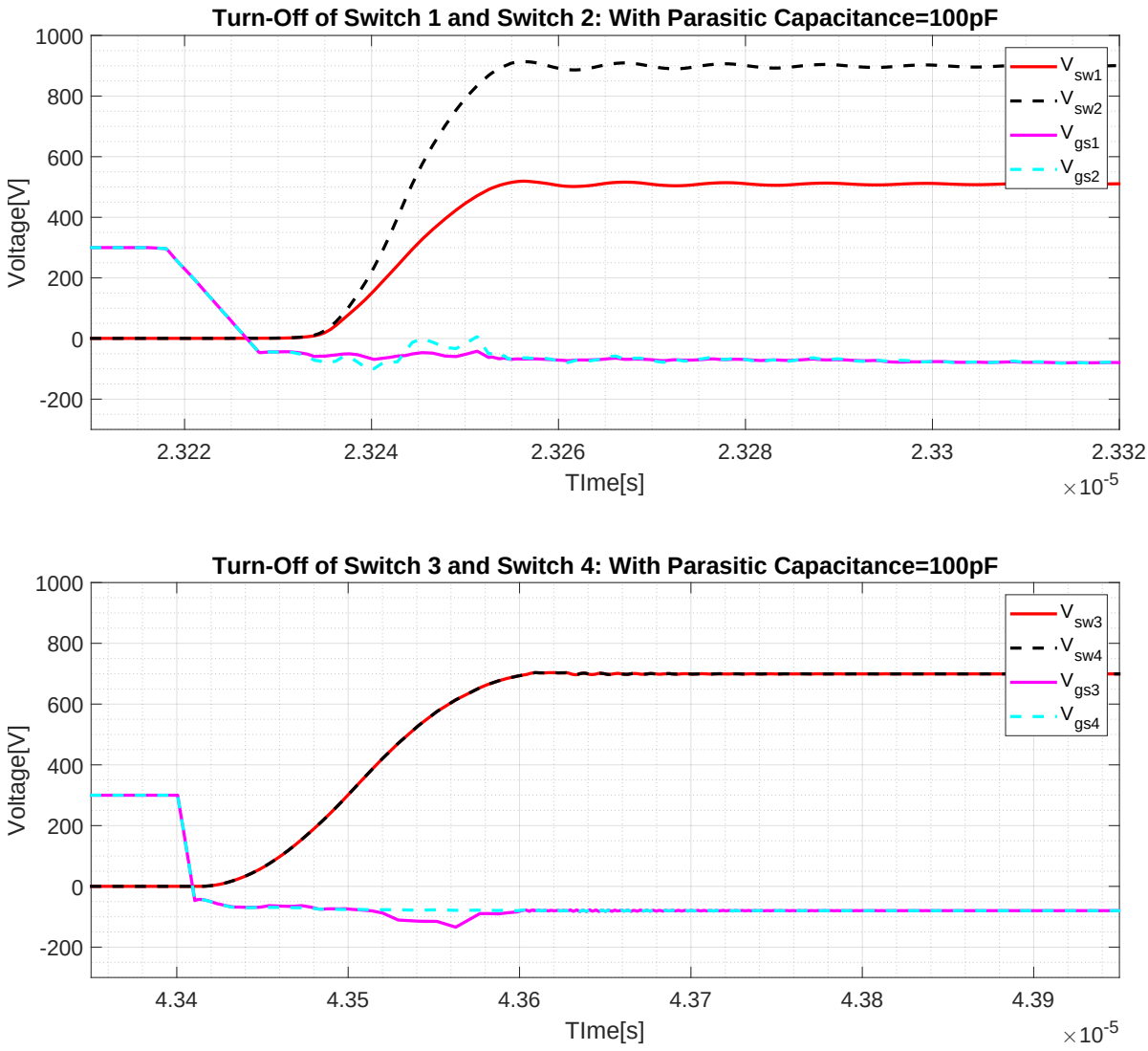


Figure 4.13: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity Parasitic capacitance 100pF

As seen from Figure 4.12 and Table 4.9, the voltage across Switch 1-2 is no more balanced, and a rather large voltage difference across them can be observed. ZVS at Turn-on is still ensured for Switch 1-2. For Switch 3-4, the voltage is balanced and ZVS at turn-on is ensured.

Figure 4.13 shows the system behaviour at Turn-Off and similar to Turn-on, the voltage across Switch 3-4 is balanced, but a large voltage difference across Switch 1-2 can be seen.

Thus, it can be concluded that parasitic capacitance can have a significant impact on the performance of the voltage balancer and voltage sharing across the series connected switches. Figure 4.14 shows how the voltage difference across the series-connected MOSFET increases with an increase in parasitic capacitance obtained using LTSpice simulation.

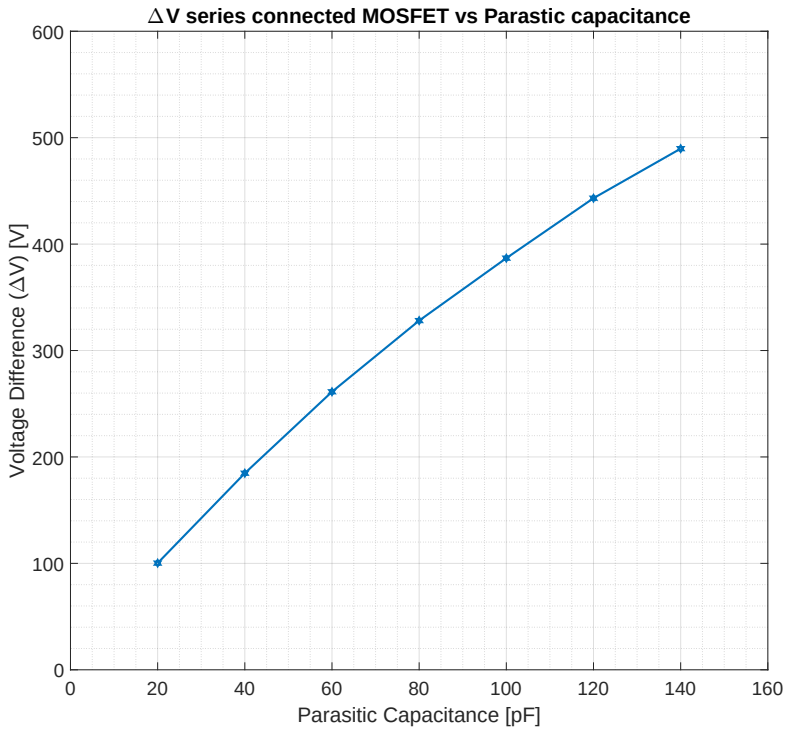


Figure 4.14: LTSpice simulation results depicting how the voltage difference across the series connected MOSFET increases with an increase in parasitic capacitance across switch1

However, parasitic capacitance across one set of series-connected switches doesn't affect voltage sharing across the other set of switches.

4.3.4. Gate Delay in Switch2: 10ns

The last non-linearity simulated was the system behaviour with different gate driver initialisation times, which results in a delay in the turn-off and turn-on instant of one of the switches connected in series with each other. Below, the simulation results for a gate delay of 10ns in Switch 2 with respect to switch 1 are presented. For Switch 3-4, no non-linearity was considered.

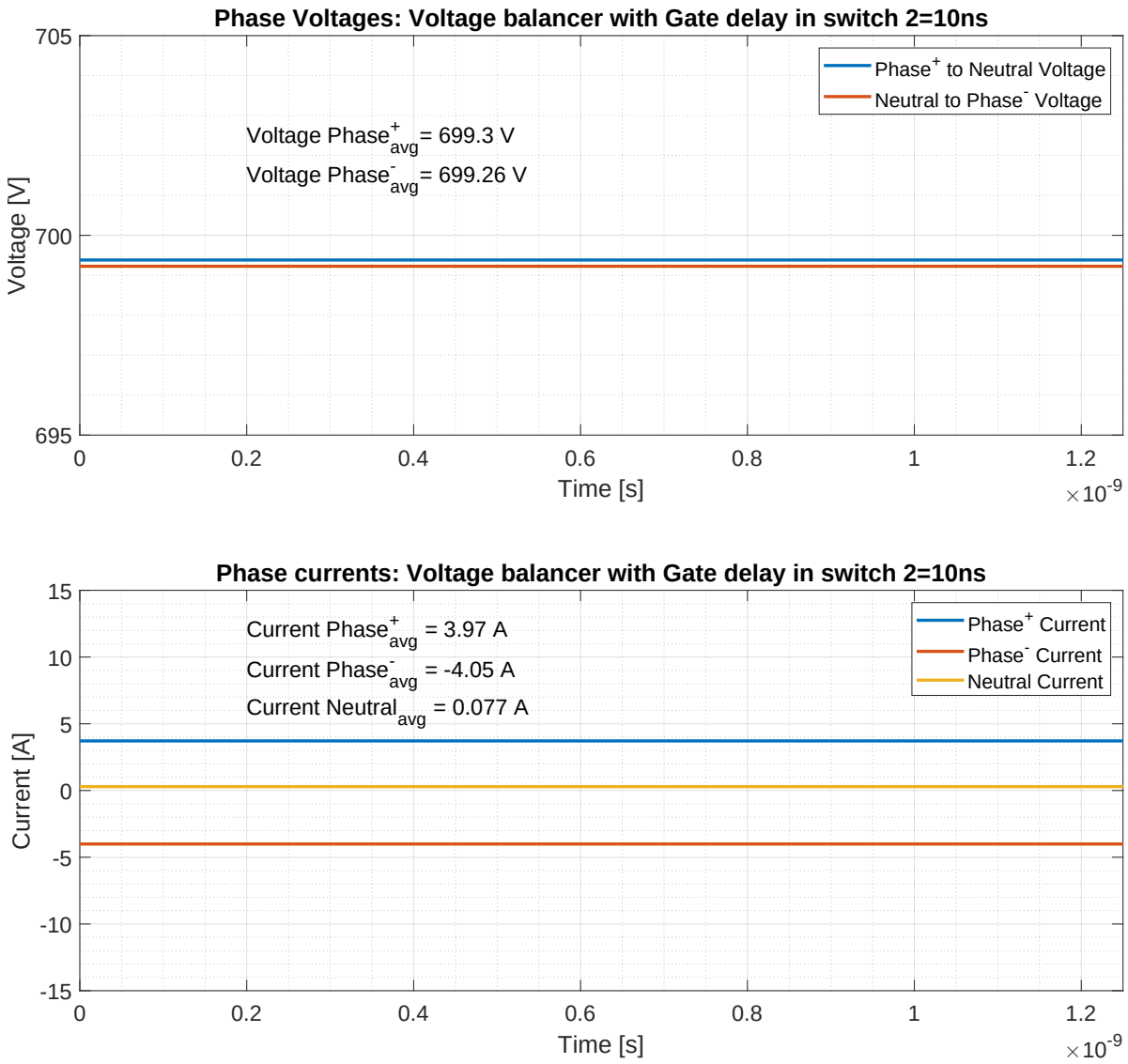


Figure 4.15: Phase voltage and current in series connected voltage balancer with non-Linearity: Gate delay in switch2: 10ns, shown for 1 time period. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are in balance. Further, the neutral line current is practically zero.

Table 4.10: LTSpice simulation results for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.3	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.26	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	3.97	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.05	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	0.077	A

As can be seen in Figure 4.15 and Table 4.10, the voltage across both positive to neutral and neutral to negative phase lines is no more balanced. Further, the current through the neutral line is also not balanced (> 0.03A) and the current through the positive and negative lines are also not equal in

magnitude, indicating an unbalanced system.

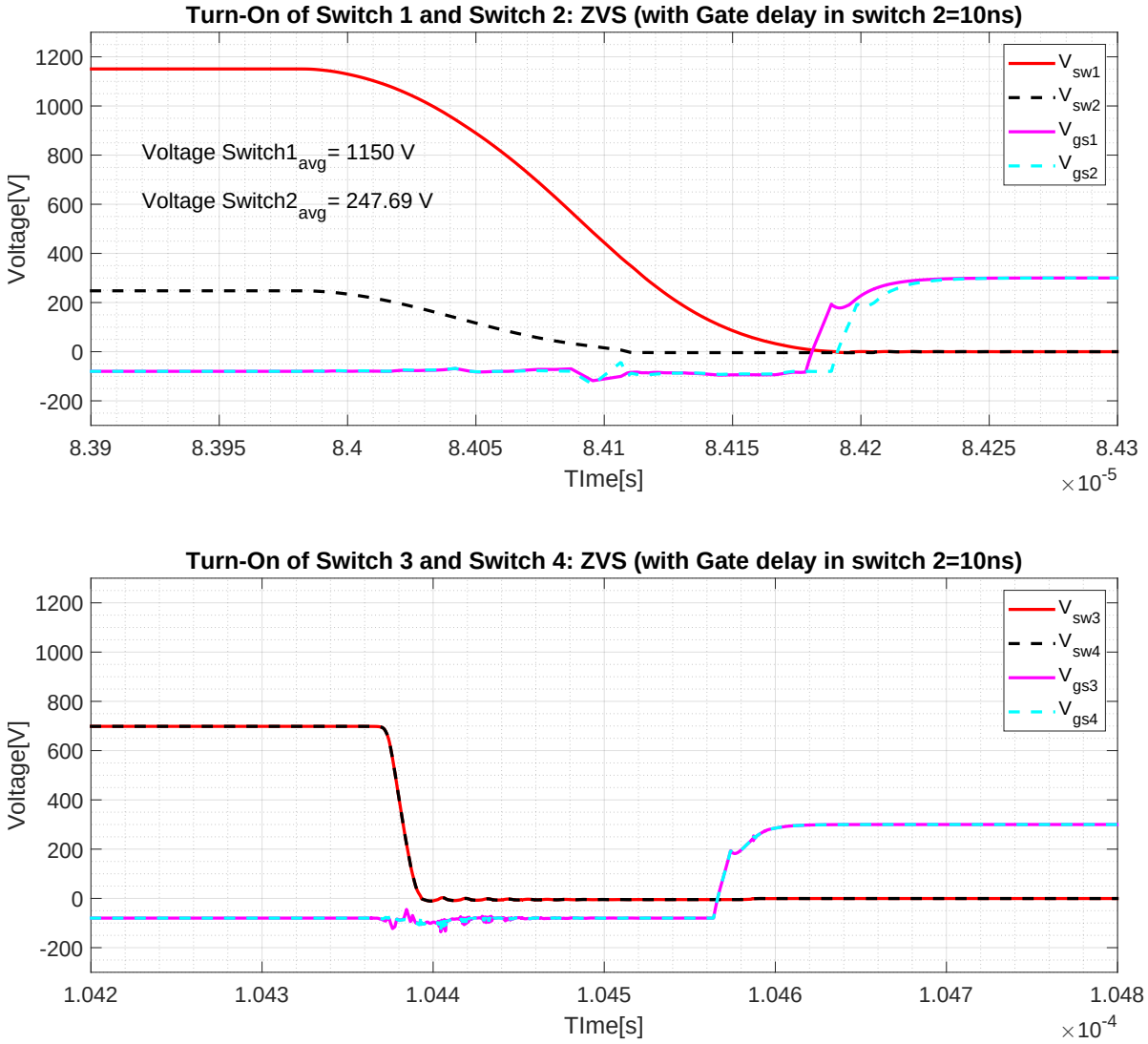


Figure 4.16: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Gate delay in switch 2. It can be observed that for both Switches 1-2 and Switch 3-4, ZVS at Turn-on is being achieved. However, the average voltage over Switch 1 and Switch 2 is different.

Table 4.11: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	1150	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	247.69	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

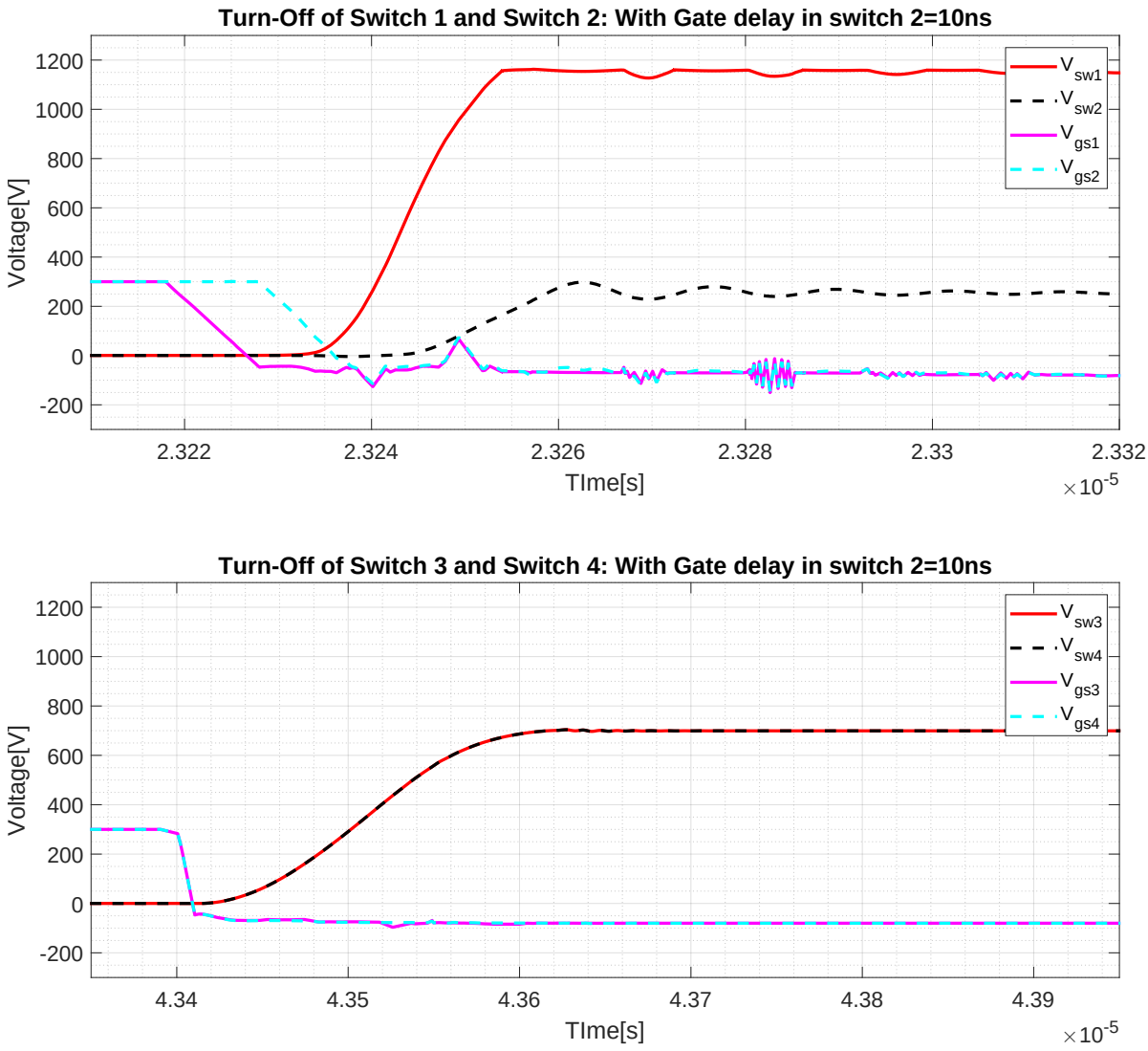


Figure 4.17: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity Gate delay in switch 2=10ns

As seen from Figure 4.16 and Table 4.11, the voltage across Switch 1-2 is no more balanced, and a rather large voltage difference across them can be observed. Moreover, the voltage across Switch 1 is $\approx$ 1150 V, which is higher than the blocking voltage of the MOSFET (900V [39]), and thus it will result in damage to the semiconductor and hence the converter.

For Switch 3-4, the voltage is balanced and ZVS at turn-on is ensured.

Figure 4.13 shows the system behaviour at Turn-Off and similar to Turn-on, the voltage across Switch 3-4 is balanced, but a large voltage difference across Switch 1-2 can be seen. Again the voltage across Switch 1 is higher than the blocking voltage of the MOSFET and will result in damage to the voltage balancer.

Therefore, among the non-linearities considered, gate delay across the switch has the maximum impact on system performance and can even result in damage to the converter. However, as seen with other cases, non-linearity in 1 set of series switches doesn't affect the performance of the other set of switches.

5
Voltage Balancing:

In this chapter the different methods used to account for unequal voltage sharing across the series connected switches in voltage balancing converters, arising due to non-linearities in the system are presented. The different methods are qualitatively compared and finally simulation results along with analytical analysis of RC snubber circuit voltage balancing across switches are presented.

5.1. Voltage sharing of series-connected SiC MOSFETS:

The voltage sharing between the series-connected MOSFET devices is mainly affected by the below parameters [44], [45]:

- Non-uniformity in device parameters such as gate resistance etc., resulting in non-uniform behaviour of the series connected MOSFETs.
- Mismatch in gate driver signal due to non-uniformity in gate driver device parameters, resulting in a mismatch in the switching behaviour of the MOSFETs.
- Non-uniformity arising out of parasitic capacitance of device and surroundings.

As a consequence of the above parameters, the voltage sharing across the series-connected MOSFETs is adversely affected resulting in unbalanced voltage distribution between the MOSFETs. For instance, the switch in the series connection that turns off earlier (due to gate delay induced by one or more of the factors mentioned above), will block a higher amount of DC bus voltage, resulting in unbalanced voltage sharing across the switches. This will result in a voltage spike across the switch and in case this voltage exceeds the voltage rating of the switch, it can result in device failure.

A mismatch in different parts of the gate driver systems can result in a time shift for the gate driving signals of the series of connected switches. It is clear that non-simultaneous switching will result in unequal voltage sharing among series-connected semiconductors (mismatch in device turn-off times due to delay of external gate drive circuit). The same was also seen through LTSpice simulation with a gate delay of 10ns across one of the switches in Section 4.3.4.

5.2. Techniques for voltage balancing across series connected MOSFET:

In order to account for and ensure equal distribution of voltage across series connected MOSFETs different control techniques have been developed. Figure 5.1 below presents the prominent methods that can be found in the literature [35], [37], [44], [46].

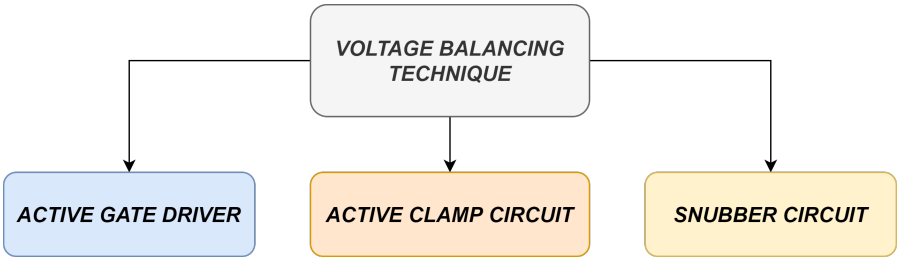


Figure 5.1: Different techniques used for voltage balancing [35]

5.2.1. Active Gate Driver:

Multiple configurations based on active gate driver control to account for unequal voltage sharing across series connected MOSFET in voltage balancing converters have been explored [35], [37].

Gate drive signal time deviation control:

Wang et al. [37] proposed an integrated gate driver with an active delay control method to control the voltage sharing across series connected MOSFET switches. The proposed method aims to control gate drive signal time deviation by accounting for differences in signal propagation delay time through the gate driver circuits.

The working of the control is described below:

- The method estimates gate delay by analysing dynamic and steady-state voltage deviation of the slew rate of voltage change ($\frac{dv}{dt}$) change and the final voltage difference between the switches.
- Based on this analysis, it uses a controller to adjust the gate driver accordingly to ensure that both switches get activated at the same time. Figure 5.2 below shows the circuit of the control method proposed by Wang et al. [37].

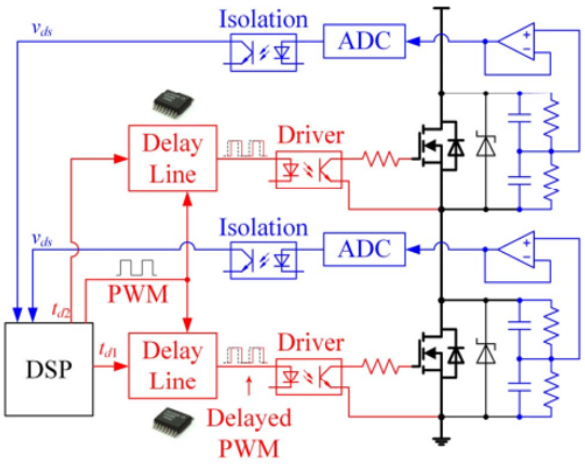


Fig. 5 The proposed driver schematic of two series connected SiC MOSFETs.

Figure 5.2: The control method proposed by Wang et al. [37] uses an ADC to acquire the voltage signal from the MOSFET, which is then sent to DSP to adjust the gate driver accordingly and ensure that both switches get activated at the same time

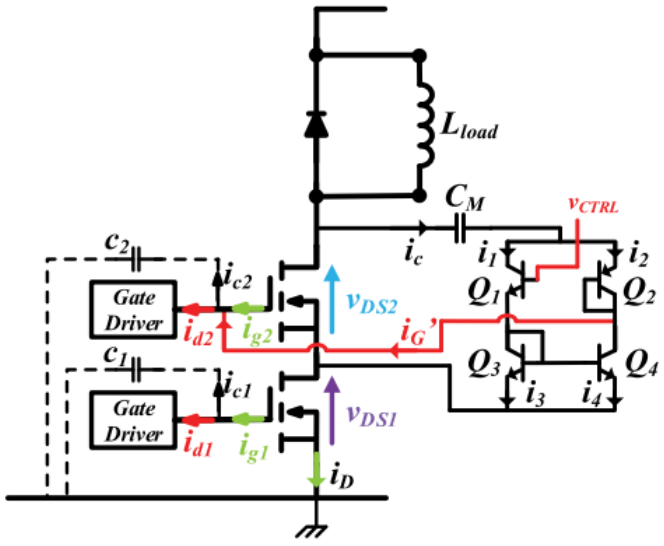
- The ADC (Analog Digital Converter) first acquires the voltage signal from the MOSFETs through an RC voltage divider.
- Voltage from ADC goes to DSP (Digital signal processor) as input. DSP processes it and provides the required gate drive signal modulation via a silicon delay line IC.

Challenges:

- The active gate driver control method makes the system highly complex and requires additional design effort for the design of the circuit to integrate ADC and DSP for voltage balance control.
- Acquisition of voltage data from MOSFET for the ADC requires an additional RC voltage divider, which has parasitic inductance. This inductance can affect the performance of the circuit resulting in voltage spikes than can damage the circuit itself, if not designed carefully.
- The DSP controller clock frequency needs to be aligned with the gate signal delay time for the voltage balancer. A mismatch of a few nano-seconds can result in large voltage deviations in the circuit. In order to account for this, a silicon delay line IC needs to be used. This increases the complexity of the control even further.
- Further the results obtained by Wang et al [37], showed a steady state voltage deviation of 50V, even with the implementation of the sophisticated control methodology.

Active Gate-Driver With $\frac{dv}{dt}$ Controller

Another method to control the voltage sharing over the series connected MOSFET switches using active gate driver control was proposed by Marzoughi et al [35]. The proposed method works to eliminate dynamic voltage imbalance between the MOSFET due to the difference in the voltage slew rate $\frac{dv}{dt}$ of MOSFETs at Turnoff condition. Figure 5.3 below shows the proposed technique and the control method.



[H]

Figure 5.3: The method proposed by Marzoughi et al [35], uses a miller capacitor and BJT network to divert a part of miller current to the MOSFET with higher parasitic capacitance current in order to control the voltage slew rate $\frac{dv}{dt}$ of the MOSFET

The method works as described below:

- The method works by introducing an additional miller capacitor which provides extra current to MOSFET with a lower $\frac{dv}{dt}$ rate in order to match the dynamic voltages across the MOSFETs.
- A part of miller current (current drawn by miller capacitor) is directed to the MOSFET in order to account for the current through parasitic capacitances and thereby compensate for $\frac{dv}{dt}$ of the MOSFET.

- It uses a BJT (bi-junction transistor) network in order to determine the current flow to the MOSFET and the same is controlled using the control voltage to the BJT.

The challenges encountered with this proposed control method are listed below:

- It requires a complex gate driver and BJT network to direct a part of the miller current back to MOSFET for $\frac{dv}{dt}$ control. The addition of multiple components introduces more failure points in the circuit.

- During Turn On, the auxiliary circuit results in additional capacitance between the ground and gate terminal resulting in higher turn-on losses for this control method.

Active gate control for voltage balancing:

Kim et al [47] proposed an active gate control method for voltage balancing across series connected MOSFET devices. The method works by using an auxiliary circuit to provide compensation current to the gate driver with delay to ensure voltage balance across the MOSFET devices in series during turn-on and turn-off. The equivalent circuit used for this method is shown in Figure 5.4 below.

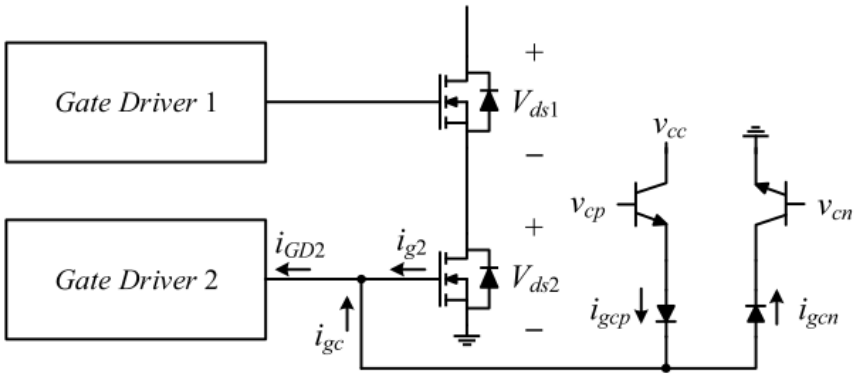


Figure 5.4: Active gate control method for voltage balance across series connected MOSFET devices proposed by Kim et al[47]. The method uses an auxiliary circuit to provide compensation current to the gate driver with delay

The auxiliary circuit proposed by Kim et al [47], (seen in Figure 5.4) comprises of BJTs governed by control voltage signal. In order to control the BJT, the proposed technique requires an additional voltage sensing circuit and a control circuit. The voltage sensing circuit is a network of resistors and capacitors to scale down and filter the voltage signal across the MOSFET, while the control circuit is a PI controller which is fed with voltage deviation signal as input to control the BJT output current.

The main advantage of the current voltage balance control method are listed below:

- The proposed method is able to control the voltage sharing across the series connected MOSFET devices in an effective way.

- It does not lead to any additional losses or switching speed reduction, which is encountered with using passive elements such as RC snubber etc.

The limitations of the proposed technique are listed below:

- It requires additional circuits for voltage measurement and control of the BJT auxiliary circuit. This makes the implementation highly complex and costly.

- Additional components increases the volume footprint and increases the failure points in the system.

Single gate driven topology for voltage balance:

Wang et al. [48] proposed a single gate driven topology for voltage balancing across series connected MOSFET devices. The proposed circuit for the technique is shown in Figure 5.5 below:

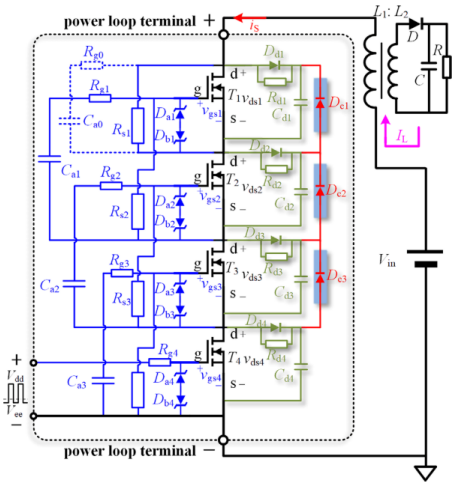


Figure 5.5: Single gate driven topology for voltage balance across series connected MOSFET devices as proposed by Wang et al [48]

The major advantages of using the proposed technique are listed below:

- The methos uses a single gate driver to operate the series connected MOSFETs and thus is highly cost efficient.
- The voltage balancing is achieved using passive components and thus it does not require any complex controls for its operation.

The limitations of the proposed method are listed below:

- The proposed method is limited for high voltage low powered application.
- The method uses large number of components to achieve voltage balancing across the MOSFET devices and thus its design and implementation is complicated and complex.
- The high component count increases the volume footprint and makes the system more prone to failure.

5.2.2. Active Clamp circuit:

Multiple topologies using Active clamp circuit for voltage balance across series connected MOSFET devices has been explored [49], [50],[51]. The proposed methods generally work by clamping either gate drain or drain source voltage of the MOSFET in order to restrict the drain source voltage across the device and control the voltage sharing.

Active voltage clamp for series connected MOSFET:

In the work of Rahman et al [49], an active voltage clamp method to control the voltage sharing across the series connected MOSFET devices has been proposed. Figure 5.6 below shows the equivalent circuit of the proposed method for voltage balance.

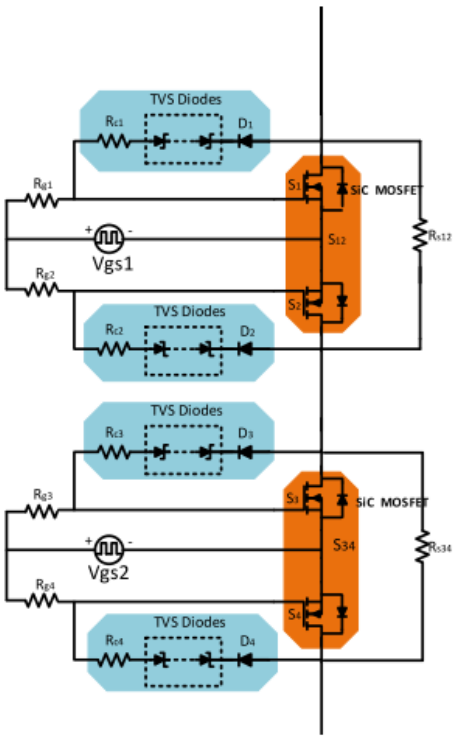


Figure 5.6: Active clamp control for voltage balance across series connected MOSFET devices as proposed by Rahman et al [49]

The method works by using diodes to clamp the voltage across the MOSFET in case of voltage spikes during turn off. Further, the clamping current is injected to the gate and thereby controlling the voltage imbalance arising out of non-linearity in gate driver initialisation.

The main advantages of the current method are listed below:

- It does not require complex control systems for its operation and thus its implementation is relatively simpler.
- It uses passive components for control and thus is a reliable and robust method for voltage balance.

The main limitations of the current technique are listed below:

- It involves usage of large number of components thus making the design and implementation process highly complex.
- The large component count exposes the proposed method to more failure points and also results in large volume requirement for the system.

Single external gate drive with RCD voltage clamping:

Wu et al[51] proposed an RCD active clamping method based on single gate drive for voltage balancing across series connected MOSFET devices. Figure 5.7 below shows the equivalent circuit of the proposed method.

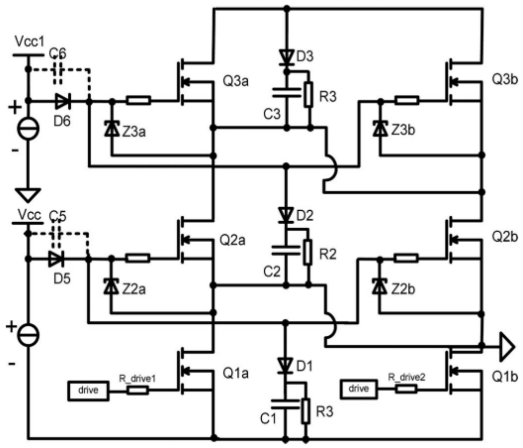


Figure 5.7: Wu et al. [51] proposed an RCD active clamping method with single gate driver to control the voltage balance across series connected MOSFET devices

The main advantages of using the proposed method for voltage balance are listed below:

- The method uses a single gate driver for MOSFET and thus is more economical.
- It does not require any additional active control system for operation and thus is more robust and reliable.

The limitations of the proposed method are listed below:

- For the proposed method, the transient voltage behaviour across the MOSFET is not completely balanced resulting in thermal losses and reliability issues.
- The method involves use of large number of components resulting in higher volume requirement and makes the system more prone to failures.

5.2.3. RC Snubber circuit:

Using RC snubber circuits for voltage balancing across series connected MOSFET is a popular choice on account of its simplicity, reliability and low-cost [52]. However, the use of snubber circuits slows down the switching speed of series-connected devices and introduces extra snubber loss. These drawbacks make the snubber circuit unsuitable for high-frequency and high-efficiency applications.

Nevertheless multiple research have been conducted to incorporate passive RC snubber circuits for voltage balancing. Some of these are introduced below in brief.

Voltage balancing using RC snubber circuit

Vechalapu et al. [52] presented a method to balance the voltage sharing across series connected MOSFET using a passive RC snubber circuit. Figure 5.8 below shows the equivalent circuit for the proposed technique.

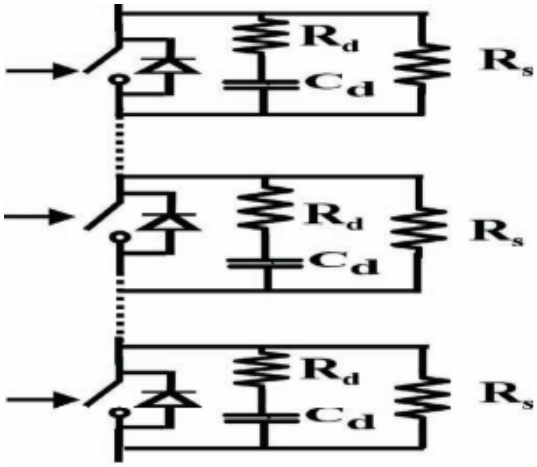


Figure 5.8: Equivalent circuit of the proposed RC snubber circuit for voltage balance across series connected MOSFET devices[52]

The main advantages of using the proposed method are listed below:

- It is simple in its implementation and does not require complex control algorithms for the operation and is a highly cost-effective solution for voltage balancing in series connected MOSFET [53].
- It is a passive technique and therefore is extremely reliable and fail-proof.

The proposed technique also has its own share of limitations. The same are listed below:

- The turn-on losses are increased as the snubber capacitor also gets discharged during the MOSFET turn-on, and the same occurs as resistive loss through series resistance and the MOSFET device [54].
- It reduces the switching frequency of the system as compared to a device without a snubber circuit [52].

Using energy recovery snubber circuit for voltage balancing:

Zhnag et al. [46] proposed an energy recovery snubber circuit as a solution to the issue of unequal voltage sharing across series-connected MOSFET configurations. Figure 5.9 below shows the proposed equivalent circuit.

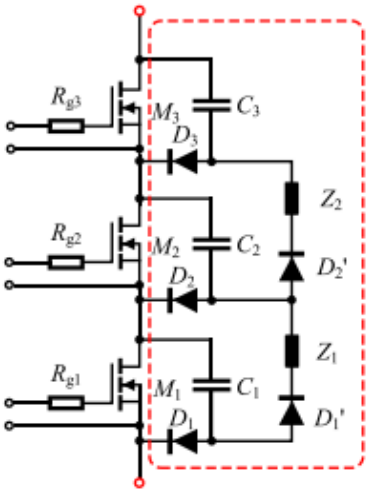


Figure 5.9: Energy recovery snubber circuit proposed as a solution for unequal voltage sharing across series connected MOSFET by Zhang et al [46].

The main advantages of the proposed circuit by Zhang et al [46] are listed below:

- A self-balancing technique is used for the operation of the snubber circuit. This greatly simplifies the system by eliminating the requirement of complex algorithms for the control of individual switches.
- The snubber capacitor voltage is maintained at a constant level at the device blocking voltage. This prevents the capacitor from discharging completely at turn-on, thus reducing losses.
- The energy recovery circuit is able to return excess energy back to the DC bus. This makes the proposed method more efficient than conventional snubber circuits.

While being highly effective, the proposed method also has certain limitations which are listed below:

- The circuit complexity in comparison with a conventional RC snubber is greatly increased, along with an increase in the number of operational components.
- Additional components imply higher cost and volume requirements for the proposed technique.
- Further, additional components also imply an increase in the overall risk of failure for the system.

Modified RC snubber with coupled inductor:

Li et al [53], [55] proposed a modified RC snubber with a coupled inductor as an improvement on the traditional RC snubber for voltage balancing across series connected MOSFET devices. The equivalent circuit of the proposed method is shown in Figure 5.10 below:

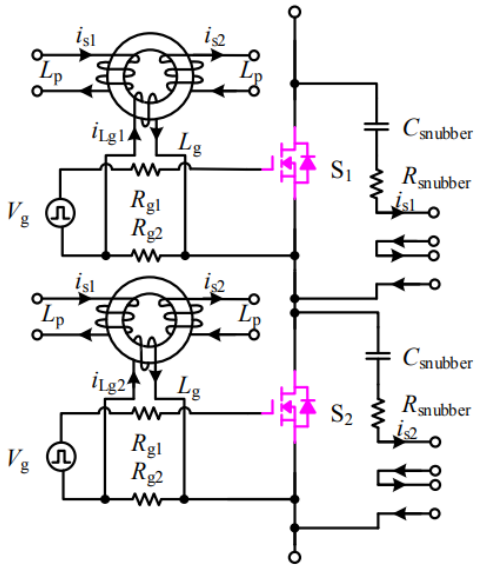


Figure 5.10: Modified RC snubber with a coupled inductor for voltage sharing across series connected MOSFET devices as proposed by Li et al [53],[55]

The imbalance between the MOSFET devices connected in series results in unequal snubber circuit current. Consequently, the voltage transition during Turn-on and Turn-off at MOSFET drain-source results in magnetisation of the inductor inducing current in the secondary coil of the coupled inductor. This induced current/voltage is then added to the gate driver through a parallel gate driver resistance, and in this way the system is balanced.

The main advantages of using this technique are listed below:

- It is an improvement on RC snubber circuit and enables using lower capacitance values in the snubber circuit. Lower snubber capacitance implies higher switching speeds.
- It uses only passive components and thus is a robust and is easy to implement.

Some drawbacks of this technique are listed below:

- Addition of coupled inductor the RC snubber results in an increase in the overall size of the system.
- It makes the system much more complex than the conventional RC snubber in terms of its assembly and control.

5.2.4. Summary:

The various methods used to balance the voltage sharing across series connected MOSFET devices have been explored in the previous sections. The discussed methods are summarised in Table 5.1 below, in terms of their advantages and limitations.

Table 5.1: Summary of different methods used for voltage balancing across series connected MOSFET devices

Method		Advantages	Limitations
Active Gate Drive	Gate drive signal time deviation control [37]	Lower losses	Complex control system and prone to reliability issues
		Good voltage balance control	Complex, High volume and costly
	Active Gate-Driver With dv/dt control [35]	Perfect voltage sharing across MOSFET	Complex gate driver for control
		Low losses and High switching frequency	Complex, High volume and costly
	Active gate control for voltage balancing [47]:	Perfect voltage sharing across MOSFET	Complex control system and prone to reliability issues
		Low losses and High switching frequency	Complex, High volume and costly
	Single gate driven topology [48]	Uses Single gate driver: Cost effective	Limited for high voltage- low power application
		No additional active control required	High volume, More failure points
Active Clamp Circuits	Active voltage clamp for series connected MOSFET [49]	No additional active control required	Large component count: Complex design and assembly
		Uses only passive components: Reliable and robust	High volume, More failure points
	Single external gate drive with RCD voltage clamping [51]	Uses Single gate driver: Cost effective	Transient response not good
		No additional active control required	Large component count: Complex design and assembly
RC Snubber	Voltage balancing using RC snubber circuit [52]	Simple design and implementation	Higher losses
		Uses passive components: Reliable and robust	Reduced switching frequency
	Energy recovery snubber circuit [46]	Self-balancing technique	Complex in design and implementation
		Lower losses	High volume, More failure points
		More efficient with energy recovery circuit	Higher cost
	Modified RC snubber with coupled inductor [53]:	Lower capacitance than RC snubber: Higher switching speed	High volume, More failure points
		Uses passive components: Reliable and robust	Complex in design and implementation

5.3. RC Snubber:

For the current thesis, it was decided to proceed with a simple RC snubber circuit to balance the voltage sharing across the series connected MOSFET devices. The simplicity of the RC snubber in terms of its design and implementation for simulation was the main consideration for this selection. The same is discussed in the next sections.

5.3.1. Gate Delay in Switch2: 10ns with Snubber

Based on the analysis of literature on the use of RC snubber circuits to control voltage distribution across series connected MOSFETs, the following conditions were listed for the selection of R and C values of the RC snubber.

- **Capacitance:** As per [46], [52], the capacitance value for the RC snubber circuit should be 5-10 times higher than the output capacitance (C_{oss}) of the MOSFET. The C_{oss} of the chosen MOSFET is 144pF [39] therefore, based on this, an initial value of **$C_{snubber}$= 0.72nF** was chosen for the RC snubber simulation.

- **Resistance:** For resistance value selection, two criterions were suggested [52].

  - The R value should be selected such that the time constant, R*C, value should be lower than the on-time of the MOSFET.

  - If the above criteria is satisfied, then the value of R should be selected to minimise the resistive loss through the snubber during turn on and turn off.

  Based on the above factors, an initial value of **$R_{snubber}$=1** Ω was chosen for the snubber resistor for LTSpice simulation.

5.3.2. Simulation Results:

Case 1:

Operating Parameters:

- **Frequency:**24.65 kHz

- **Duty Cycle:** 0.5025

- **Dead Time:** 220 ns

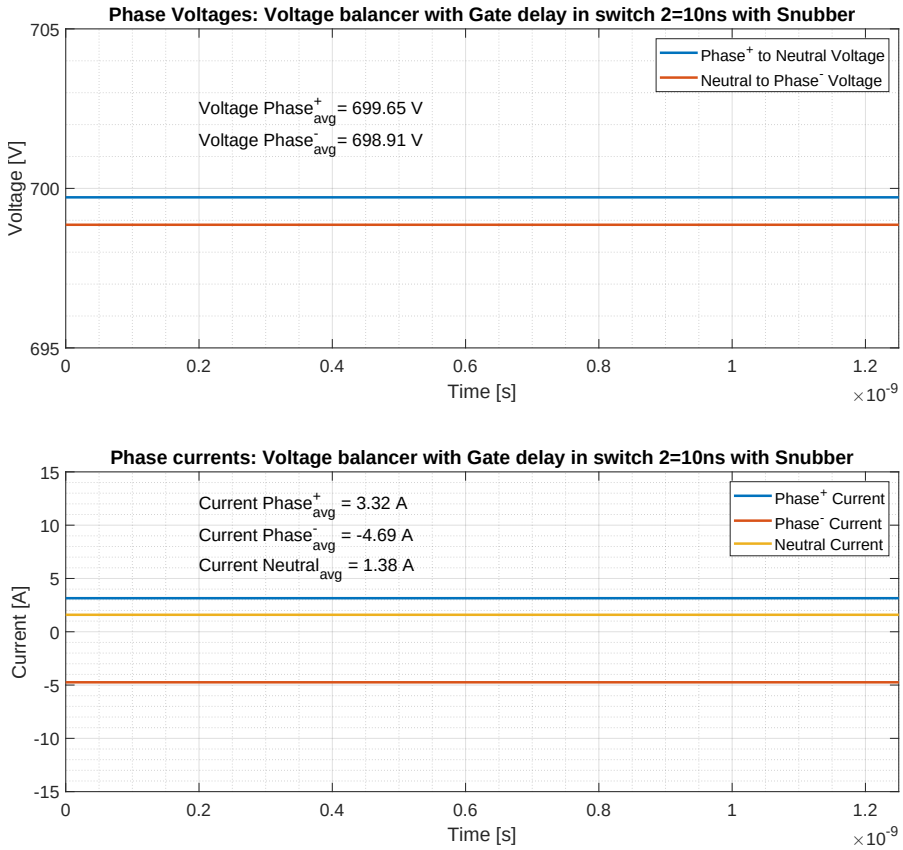


Figure 5.11: Phase voltage and current in series connected voltage balancer with non-Linearity: Gate delay in switch2: 10ns with snubber circuit, shown for 1 time period. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are not balanced. Further, the neutral line current is also high

Table 5.2: LTSpice simulation results for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.65	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	698.91	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	3.32	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.69	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	1.38	A

As can be seen from Figure 5.11 and Table 5.2, the introduction of the snubber circuit did not improve the voltage balance across positive to neutral and neutral to negative line. Further, the neutral current magnitude has also increased with respect to the case without the snubber circuit (Section 4.3.4).

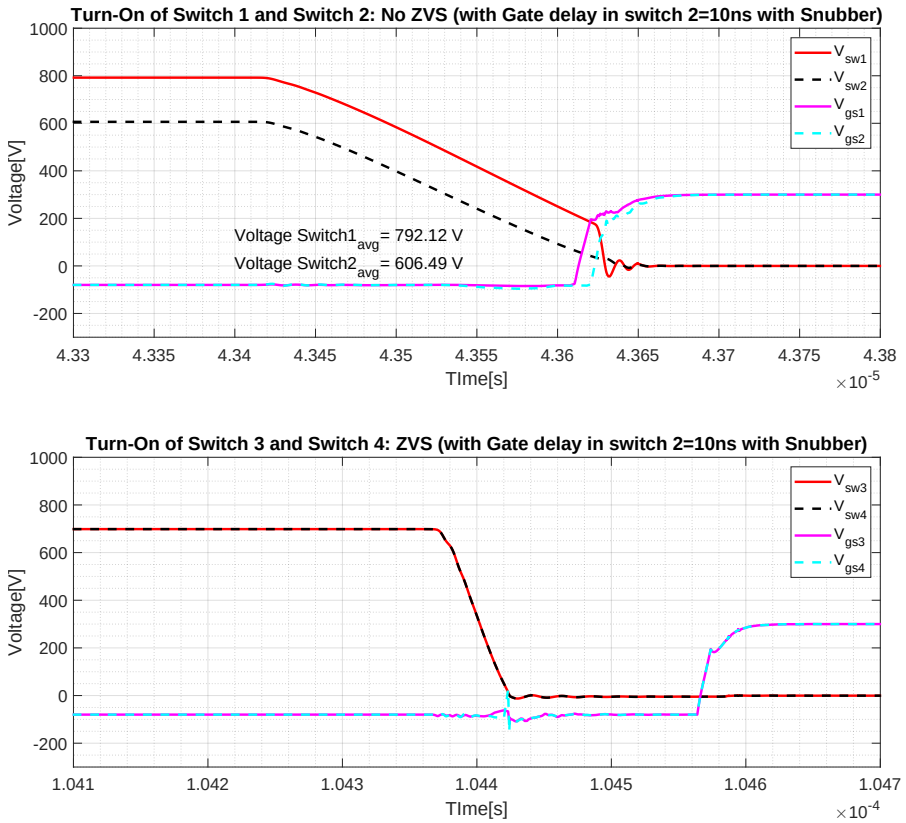


Figure 5.12: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Gate delay in switch 2 with snubber circuit. It can be observed with the snubber circuit, the voltage across switch 1 and switch 2 have improved as compared to without the snubber circuit (Figure 4.16), however with this, ZVS at turn on is not being achieved for Switch 1-2. For Switches 3-4 ZVS at turn-on is being achieved.

Table 5.3: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	792.12	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	606.49	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	No	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

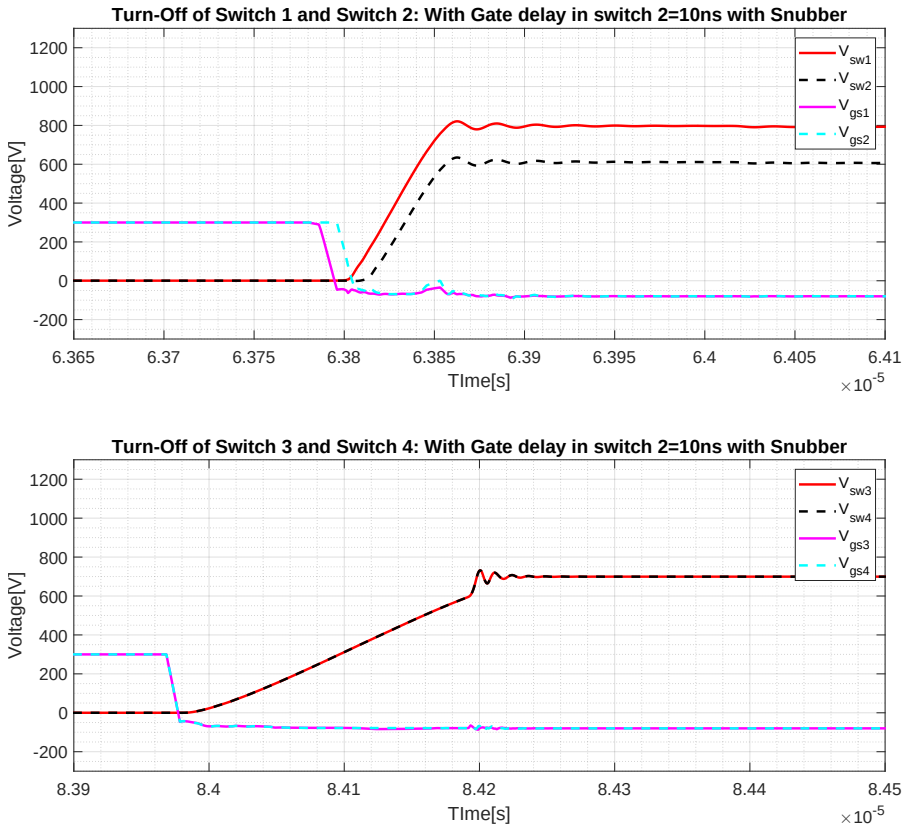


Figure 5.13: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity gate delay in switch 2=10ns with snubber circuit

As can be seen from Figure 5.12 and Table 5.3. for switches 1 and 2, with switch 2 having a gate delay of 10ns wrt switch 1, the voltage sharing has improved remarkably to the case without the snubber (Section 4.3.4). However, with the introduction of the snubber circuit ZVS at turn-on for switches 1 and 2 is no longer getting achieved.

Furthermore, from Figure 5.12 and Figure 5.13, it can be seen that for Switch 3 and 4, there is no impact on voltage sharing and ZVS at turn-on because of gate delay and addition of snubber circuit on switch 1 and 2.

Case 2:

In order to balance the circuit with the RC snubber, the operating frequency of the simulation was varied. Below are the simulation results.

Operating Parameters:

- **Frequency:**21.35 kHz
- **Duty Cycle:**0.5025
- **Dead Time:**220ns

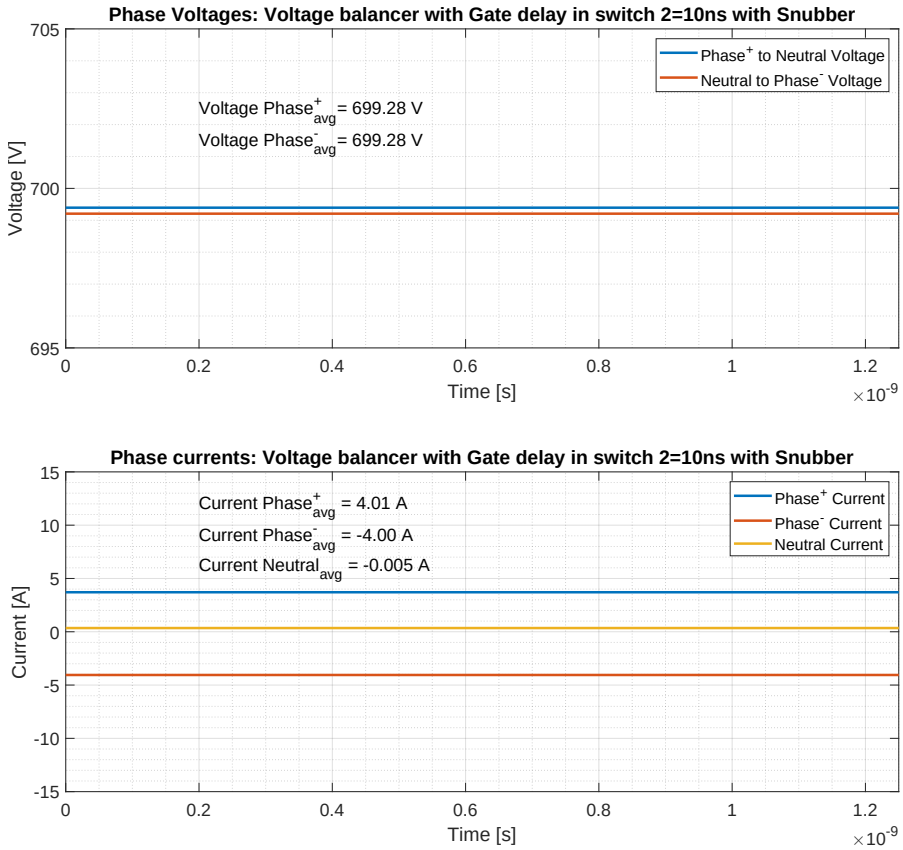


Figure 5.14: Phase voltage and current in series connected voltage balancer with non-Linearity: Gate delay in switch2: 10ns with snubber circuit with frequency changed to 21.35 kHz shown for 1 time period. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines are now balanced. Further, the neutral line current is also balanced ($\leq$ 0.03A)

Table 5.4: LTSpice simulation results for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber with frequency changed to 21.35kHz

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.28	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.28	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.01	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.00	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	-0.005	A

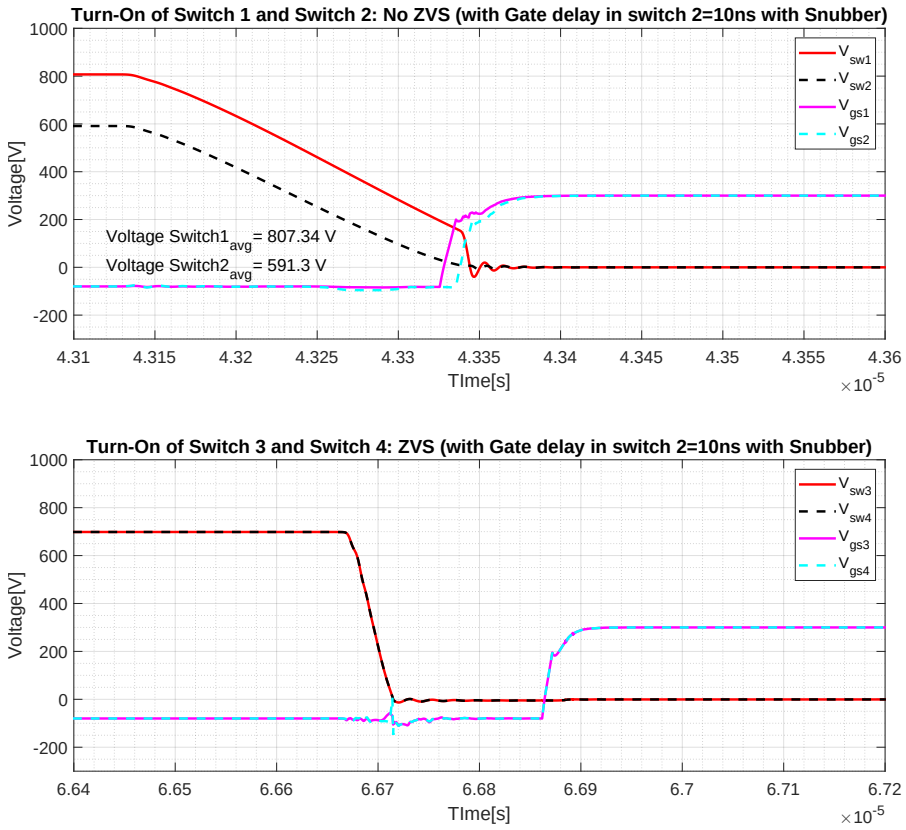


Figure 5.15: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Gate delay in switch 2 with snubber circuit with frequency changed to 21.35kHz. It can be observed with the snubber circuit, the voltage across switch 1 and switch 2 is unbalanced

Table 5.5: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	807.34	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	591.3	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	No	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

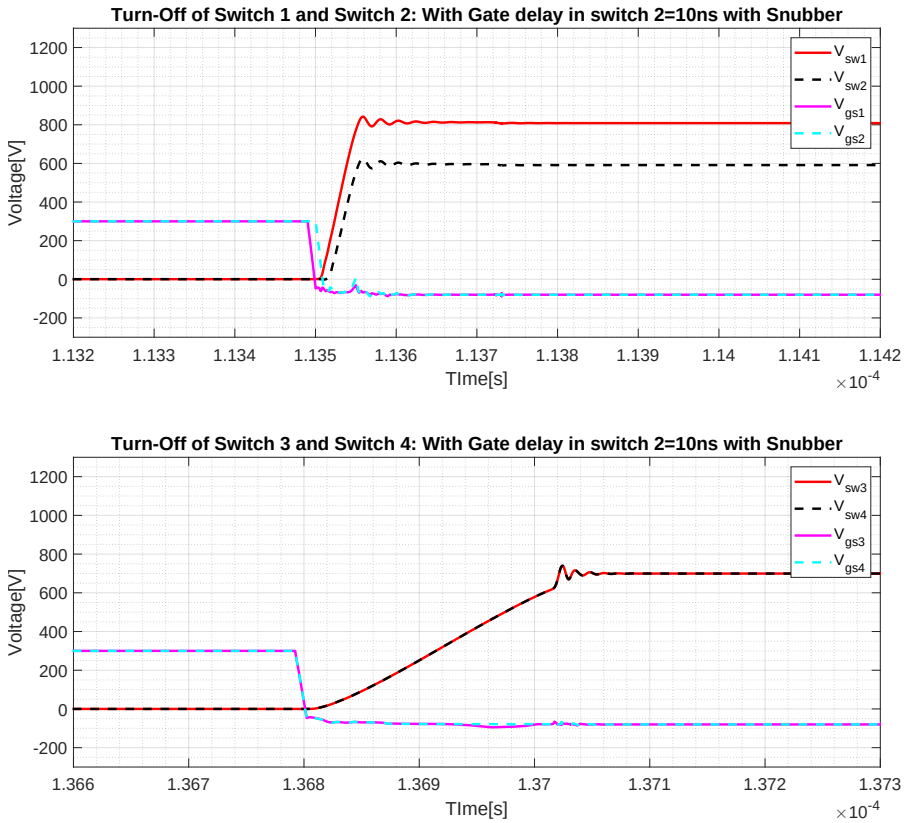


Figure 5.16: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity gate delay in switch 2=10ns with snubber circuit with frequency changed to 21.35kHz

Case 3:

Although case 2 resulted in balanced phase voltages and currents, ZVS was still not ensured. To further improve the system performance the dead time of the MOSFET is changed to 300ns.
Operating Parameters:

- **Frequency:**21.25 kHz
- **Duty Cycle:**0.5025
- **Dead Time:**300 ns

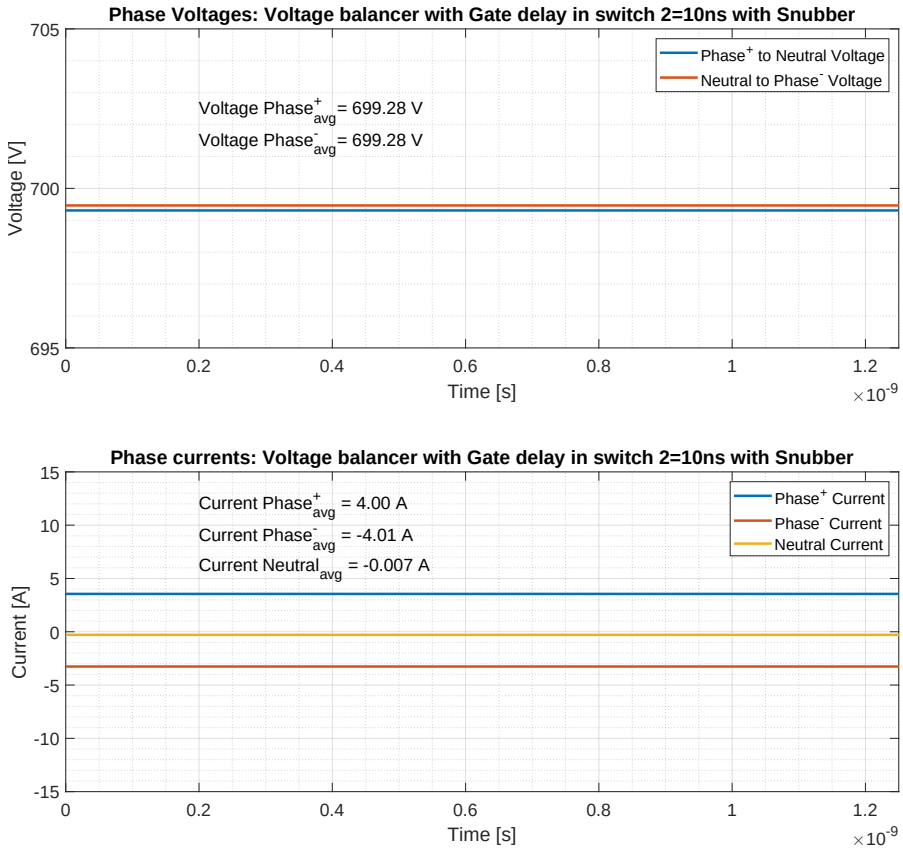


Figure 5.17: Phase voltage and current in series connected voltage balancer with non-Linearity: Gate delay in switch2: 10ns with snubber circuit with dead time 300ns, shown for 1 time period. It can be seen that the average Phase voltage for positive to neutral and neutral to negative lines and the neutral line current are all balanced

Table 5.6: LTSpice simulation results for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.28	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.28	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.00	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.01	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	-0.007	A

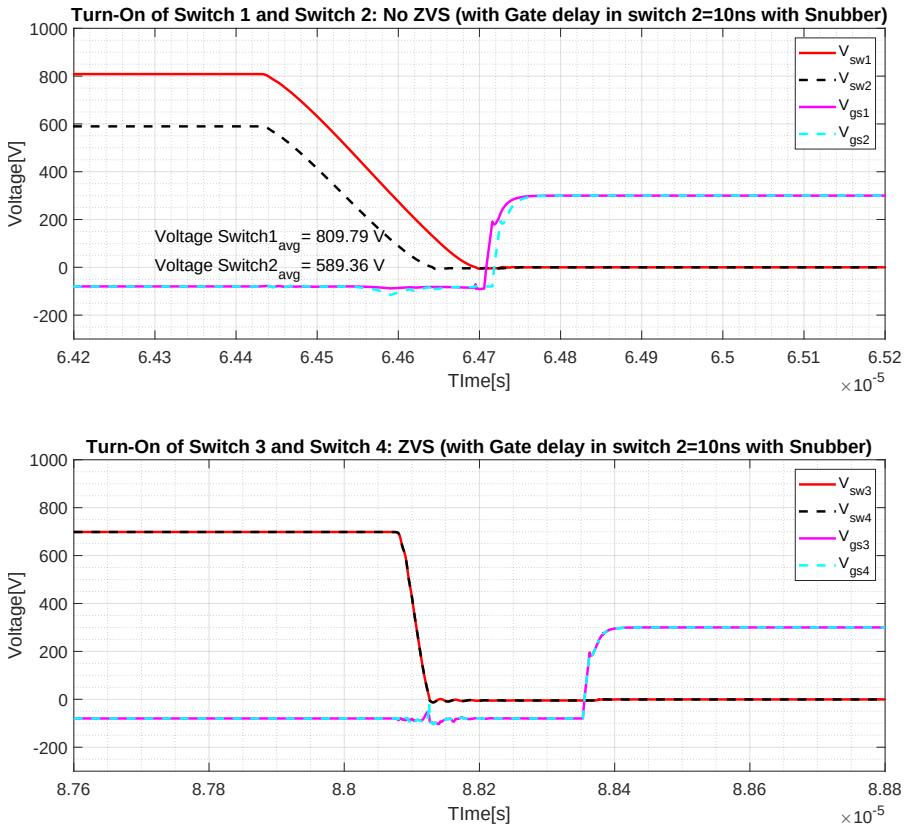


Figure 5.18: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Gate delay in switch 2 with snubber circuit with dead time 300ns. It can be seen that with this configuration ZVS at turn-on is being achieved for both the series switches

Table 5.7: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	809.79	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	589.36	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

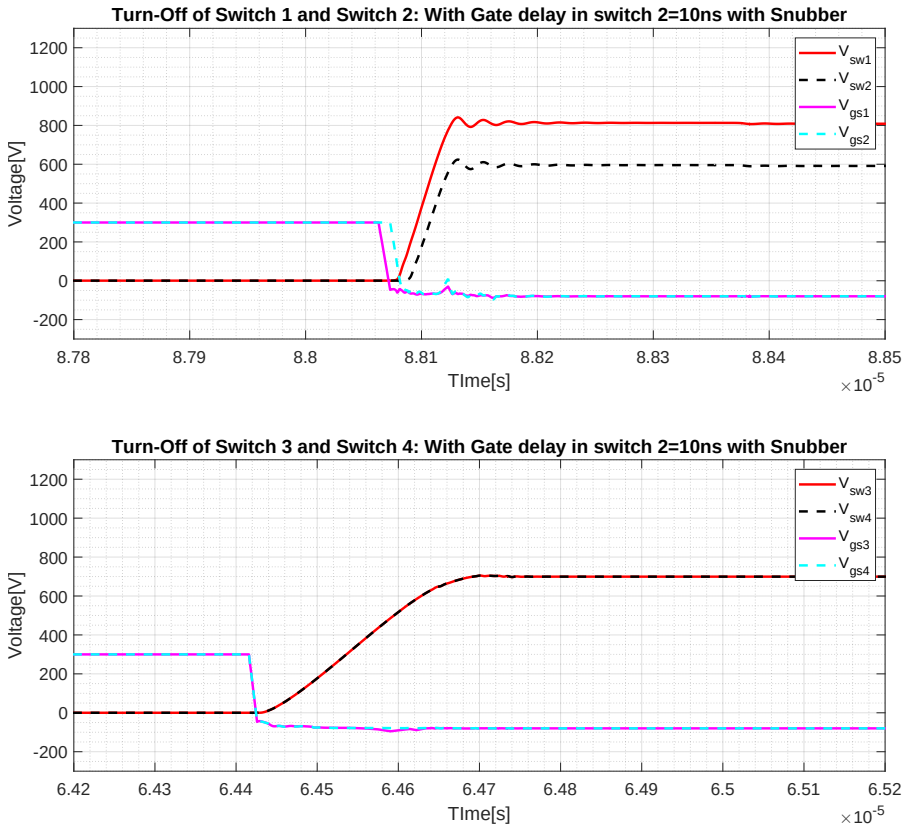


Figure 5.19: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity gate delay in switch 2=10ns with snubber circuit and dead time 300ns

Case 4:

In this simulation frequency is changed to 16kHz and Duty cycle is changed to 0.501 while keeping dead time to 220ns to achieve ZVS.
Operating Parameters:

- **Frequency:**16 kHz
- **Duty Cycle:**0.501
- **Dead Time:**220 ns

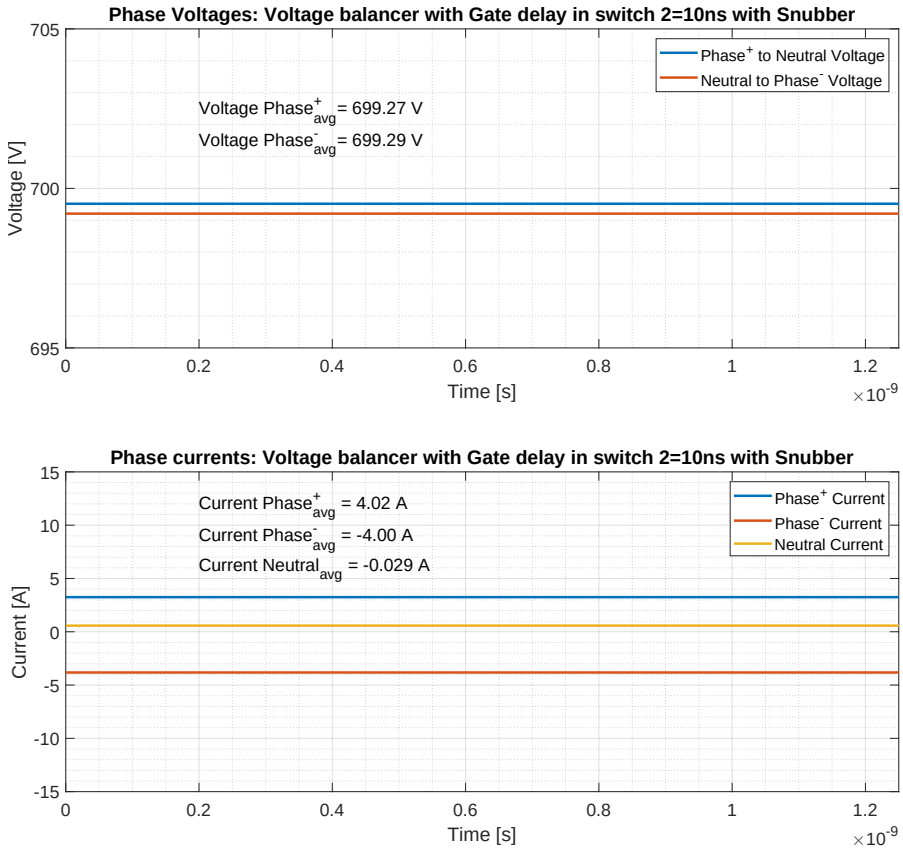


Figure 5.20: Phase voltage and current in series connected voltage balancer with non-Linearity: Gate delay in switch2: 10ns with snubber circuit with frequency 16kHz and Duty cycle 0.501, shown for 1 time period.It can be seen that voltage across positive to neutral, neutral to negative and neutral line current are all balanced.

Table 5.8: LTSpice simulation results for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber

Parameter	Description	Value	Unit
$\mathbf{V}^{+}_{Phaseavg}$	Average positive phase voltage	699.27	V
$\mathbf{V}^{-}_{Phaseavg}$	Average negative phase voltage	699.29	V
$\mathbf{i}^{+}_{Phaseavg}$	Average positive phase current	4.02	A
$\mathbf{i}^{-}_{Phaseavg}$	Average positive phase current	-4.00	A
$\mathbf{i}_{Neutralavg}$	Average neutral phase current	-0.029	A

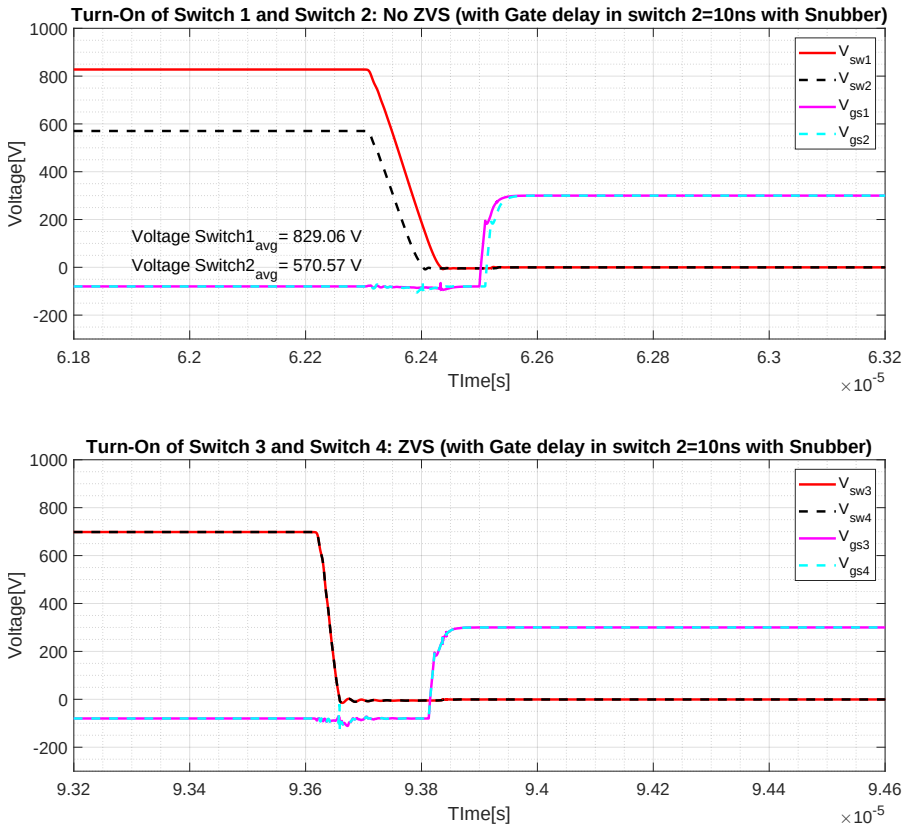


Figure 5.21: ZVS Turn-On of Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-Linearity: Gate delay in switch 2 with snubber circuit with frequency 16kHz and Duty cycle 0.501. It can be seen that with current operating condition, ZVS at turn-on in both switch is getting achieved.

Table 5.9: LTSpice simulation results of ZVS at turn-on of switch 1-2 and switch 3-4 for series connected voltage balancer with non-linearity: Gate delay of 10ns in switch 2 with RC snubber with frequency 16kHz and Duty cycle 0.501

Parameter	Description	Value	Unit
$\mathbf{V}_{sw1avg}$	Average switch 1 voltage	829.06	V
$\mathbf{V}_{sw1avg}$	Average switch 2 voltage	570.57	V
$\mathbf{ZVS}_{sw1-2}$	ZVS at Turn-on switch 1-2	Yes	-
$\mathbf{ZVS}_{sw3-4}$	ZVS at Turn-on switch 3-4	Yes	-

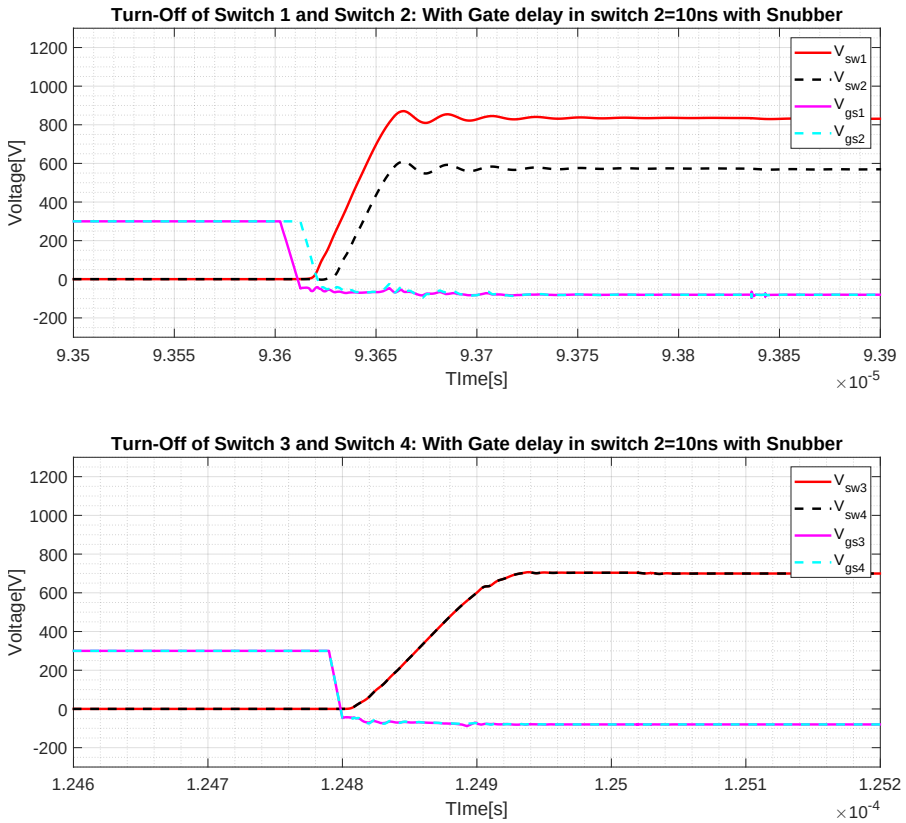


Figure 5.22: Turn-off behaviour in Switch 1-2 and Switch 3-4 in series connected voltage balancer with non-linearity gate delay in switch 2=10ns with snubber circuit with frequency 16kHz and Duty cycle 0.501

From case 3 and case 4 it can be inferred that to achieve ZVS either the dead time is increased or the duty cycle is reduced. Both the scenarios resulted in an increase in voltage unbalance across the switches. Case 4 of decreasing the duty cycle to ensure ZVS also resulted in significant drop of frequency (compared to case 1 & 2) in order to balance the phase voltages and currents. Therefore, there is a trade-off between switch voltage unbalance and ZVS.

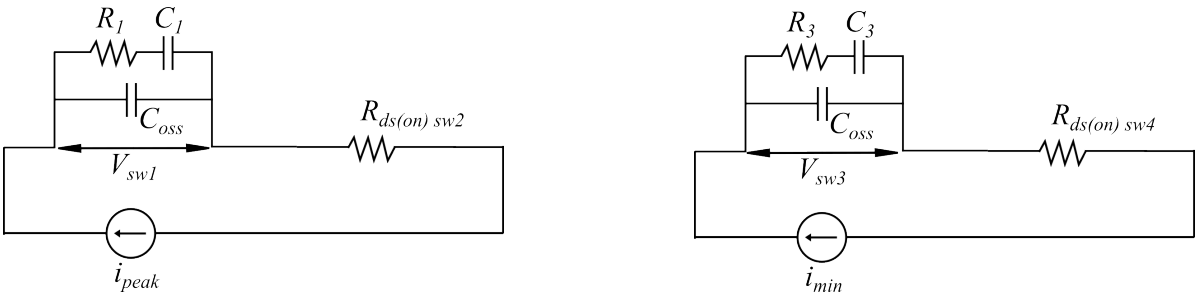
In order to further describe the system behaviour, it was decided to analytically determine a relationship between snubber circuit parameters, the voltage difference across switches 1 and 2, and ZVS at turn-on. The analytical relationship developed will be validated using the LTspice simulation model. The same is described in the next sections.

5.4. Analytical calculation: Optimization of the RC snubber design for series connection

5.4.1. For estimating voltage difference across the switches with different snubber resistance and capacitance values

Assumption: It is assumed that the current flowing through the snubber circuit and C_{oss} will be split according to the ratio of the capacitance on the respective lines.

For time = 0 to 10 ns



(a) Equivalent circuit with switch 1 turned off 10 ns before switch2

(b) Equivalent circuit with switch 3 turned off 10 ns before switch4

Figure 5.23: Equivalent circuit with gate delay in switch 2 (10ns) at turn-off

At turn-off, the current flowing through switch 1 and switch 2 during dead time is the peak current i_{peak}. The voltage across switch 1 during turn-off 10ns before switch 2 (because of gate delay in switch 2) is given by Equation 5.25 below.

$$V_{sw1} = V_{C_1} + V_{R_1} \tag{5.1}$$

where:

Symbol	Parameter	Unit
V_{swi}	Voltage across switch i	[V]
V_{Ci}	Voltage across capacitance i	[V]
V_{Ri}	Voltage across resistor i	[V]

This can be simplified as below:

$$V_{sw1} = \frac{i(t_g)}{C_1} + iR_I$$

where:

Symbol	Parameter	Unit
i	Current flowing through snubber circuit	[A]
t_g	Gate delay in switch 2 =10 n	[s]
C_i	Capacitance of snubber circuit switch i	[F]
R_i	Resistance of snubber circuit switch i	[Ω]

Equation 5.25 is further simplified to give Equation 5.2 below:

$$V_{sw1} = \frac{1}{C_1}\left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right)(t_g) + \left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right)R_1 \tag{5.2}$$

where:

Symbol	Parameter	Unit
C_{oss}	Output capacitance of switch	[F]
i_{peak}	Peak current flowing through the circuit during turn-off	[A]

Meanwhile, the voltage across switch 2 during this time is given below, which is simplified to give final expression for switch 2 voltage as Equation 5.26

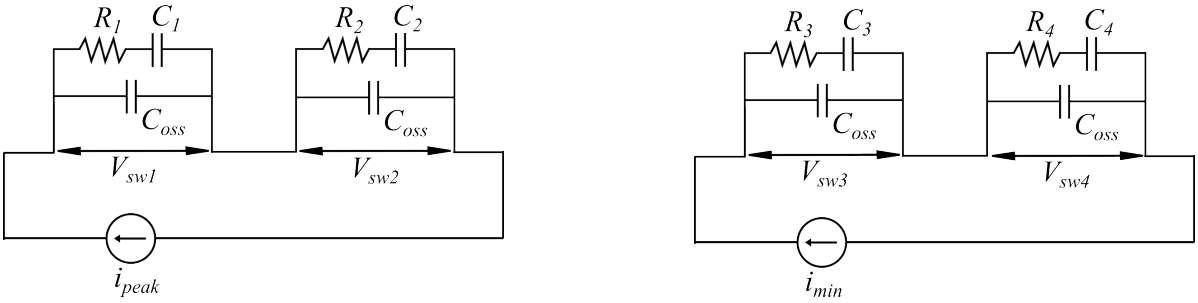
$$V_{sw2} = iR_{\text{ds(on)}sw2}$$

$$V_{sw2} = \left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right) R_{\text{ds(on)}sw2} \tag{5.3}$$

where:

Symbol	Parameter	Unit
$R_{ds(on)swi}$	Resistance of switch i at turn on	[Ω]

For time t= $10ns^+$ till voltage across switch 1 and 2 stabilise (T)



(a) Equivalent circuit with switch 1 turned off 10 ns before switch2

(b) Equivalent circuit with switch 3 turned off 10 ns before switch4

Figure 5.24: Equivalent circuit with gate delay in switch 2 (10ns) turn-off after time: 10ns

Voltage across switch 1 and switch 2 is given by Equation 5.4 and Equation 5.5 below:

$$V_{sw1} = \frac{1}{C_1}\left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right)(T) + \left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right) R_1 \tag{5.4}$$

$$V_{sw2} = \frac{1}{C_2}\left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right)(T) + \left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right) R_2 \tag{5.5}$$

where:

Symbol	Parameter	Unit
T	Time from 10ns$^+$ till V_{sw1} and V_{sw2} get stabilised	[s]

Since, for the current configuration the input voltage is 1400 V (Section 1.1), using this we get Equation 5.6.

$$1400 = V_{sw1} + V_{sw2} \tag{5.6}$$

Using Equation 5.4. 5.5 and 5.6. we get the following:

$$1400 = \left[\frac{1}{C_1}\left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right)(t_g) + \left(i_{\text{peak}} \times \frac{C_1}{C_1 + C_{\text{oss}}}\right) R_1 + \frac{1}{C_1}\left(i_{\text{peak}} \times \frac{C_1}{c_1 + C_{\text{oss}}}\right)(T)\right] + \left[\left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right) R_{\text{ds(on)}sw2} + \frac{1}{C_2}\left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right)(T) + \left(i_{\text{peak}} \times \frac{C_2}{C_2 + C_{\text{oss}}}\right) R_2\right] \tag{5.7}$$

Similarly, for switch 3 & switch 4 we get Equation 5.8:

$$1400 = V_{sw3} + V_{sw4} \tag{5.8}$$

Which is simplified similar to Equation 5.7 to give Equation 5.9

$$1400 = \left[\frac{1}{C_1}\left(i_{\text{min}} \times \frac{C_3}{C_3 + C_{\text{oss}}}\right)(t_g) + \left(i_{\text{min}} \times \frac{C_3}{C_3 + C_{\text{oss}}}\right) R_3 + \frac{1}{C_3}\left(i_{\text{min}} \times \frac{C_3}{C_3 + C_{\text{oss}}}\right)(T)\right] + \left[\left(i_{\text{min}} \times \frac{C_4}{C_4 + C_{\text{oss}}}\right) R_{\text{ds(on)}sw4} + \frac{1}{C_4}\left(i_{\text{min}} \times \frac{C_4}{C_4 + C_{\text{oss}}}\right)(T) + \left(i_{\text{min}} \times \frac{C_4}{C_4 + C_{\text{oss}}}\right) R_4\right] \tag{5.9}$$

where:

Symbol	Parameter	Unit
i_{min}	Minimum current flowing through C1 and R1 during turn-off	[A]

Figure 5.25 and 5.26 below show the comparison between the voltage across switches 1 and 2 at turn-off calculated analytically using the above equation and LTspice simulation results.

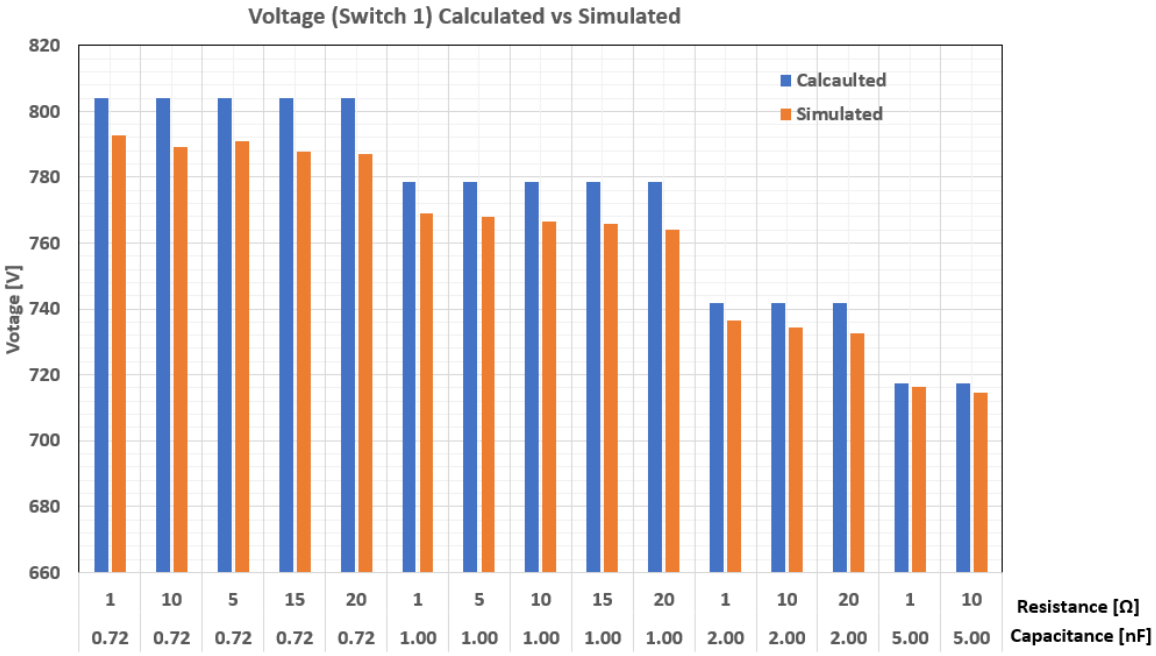


Figure 5.25: Analytically calculated voltage across switch 1 at turn off vs LTspice simulation results

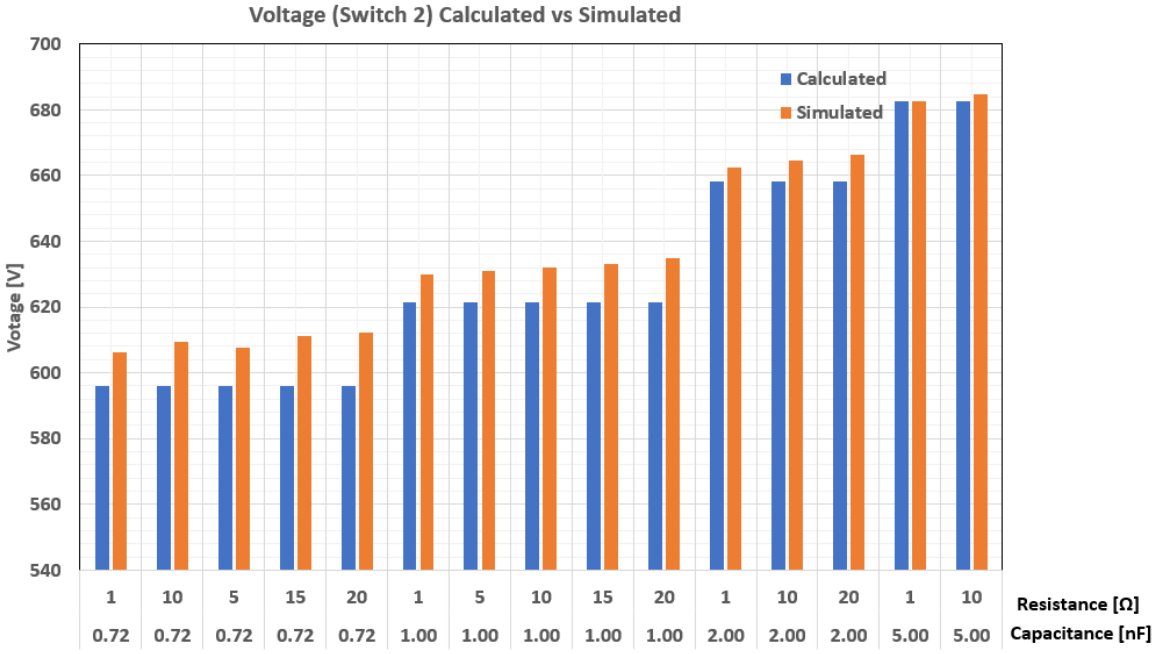


Figure 5.26: Analytically calculated voltage across switch 2 at turn off vs LTspice simulation results

Thus it can be seen that the analytical calculation correlates well with LTspice simulation results.

With the correlation established, the analytical calculation was used to check the performance of the system with varying snubber capacitance values. The same is shown in Figure 5.27 below.

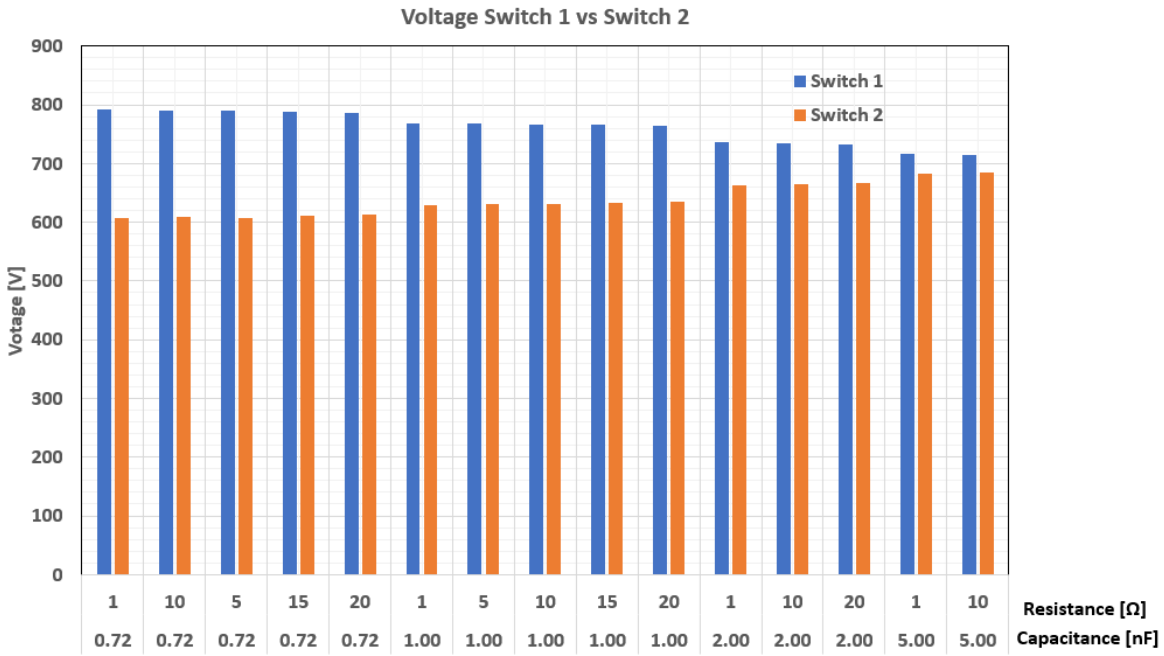
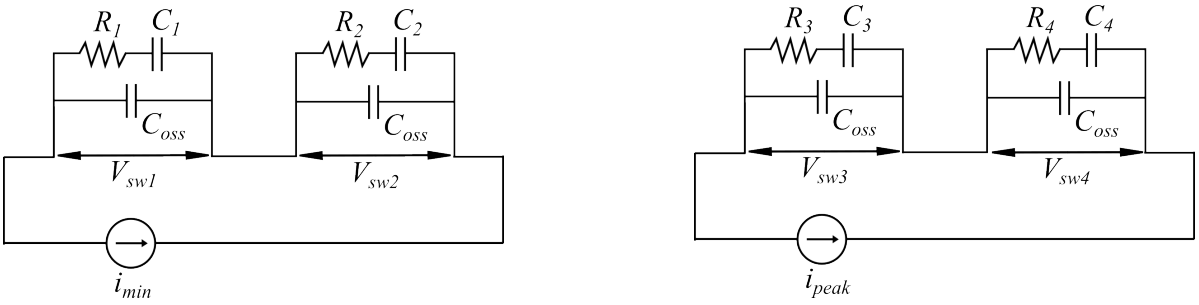


Figure 5.27: Voltage across switches 1 and 2 at the turn-off. It can be seen that voltage difference across switches reduces with an increase in capacitance values. However, with higher capacitance, the discharge time of the capacitor increases which negates the possibility of ZVS at turn-on

5.4.2. For estimating the possibility of ZVS

To achieve ZVS it is important that the voltage across the switch drops to zero before the switch is turned on i.e., the discharging of the snubber capacitor should happen within the dead time.



(a) Equivalent circuit just before turning on switch 1 & 2

(b) Equivalent circuit just before turning on switch 3 & 4

Figure 5.28: Equivalent circuit before turning-on

For voltage across capacitor 1, the following equation 5.10 holds.

$$V_{\text{sw1}} - V_{\text{R1}} = V_{C_1} \tag{5.10}$$

Equation 5.10 can be further simlified to equation 5.11

$$V_{\text{sw1}} - \left(i_{\text{min}} \times \frac{C_1}{C_1 + C_{\text{oss}}} \right) R_1 = V_{C_1} \tag{5.11}$$

Using $i = C\frac{dv}{dt}$ for calculating dt we get:

$$dt = \frac{C \times dV}{i}$$

Using equation 5.11 and current distribution between capacitors, we get equation 5.12 below:

$$dt_1 = \frac{C_1\left[V_{\text{sw1}} - \left(i_{\text{min}} \times \frac{C_1}{C_1+C_{\text{oss}}}\right)R_1\right]}{\left(i_{\text{min}} \times C_1 \times \frac{1}{C_1+C_{\text{oss}}}\right)} \tag{5.12}$$

Similarly for switch 2, 3 and 4, we get equation 5.13, 5.14 and 5.15 as below:

$$dt_2 = \frac{C_2\left[V_{\text{sw2}} - \left(i_{\text{min}} \times \frac{C_2}{C_2+C_{\text{oss}}}\right)R_2\right]}{\left(i_{\text{min}} \times C_2 \times \frac{1}{C_2+C_{\text{oss}}}\right)} \tag{5.13}$$

$$dt_3 = \frac{C_3\left[V_{\text{sw3}} - \left(i \times \frac{C_3}{C_3+C_{\text{oss}}}\right)R_3\right]}{\left(i \times C_3 \times \frac{1}{C_3+C_{\text{oss}}}\right)} \tag{5.14}$$

$$dt_4 = \frac{C_4\left[V_{\text{sw4}} - \left(i \times \frac{C_4}{C_4+C_{\text{oss}}}\right)R_4\right]}{\left(i \times C_4 \times \frac{1}{C_4+C_{\text{oss}}}\right)} \tag{5.15}$$

5.4.3. For estimating power loss in snubber

For estimating the power loss in the snubber circuit during turn-on and turn-off the following equation 5.16 can be used.

$$P_{snubber} = I_{rms}^2 \times R_{snubber} \tag{5.16}$$

The rms current through the snubber circuit can be determined using equation 5.17 and 5.18 below:

$$i_{rms-sw1} = \sqrt{\frac{\left(i_{\text{peak}} \times \frac{c_1}{c_1+c_{\text{oss}}}\right)^2 (t_g+T) + \left(i_{\text{min}} \times \frac{c_1}{c_1+c_{\text{oss}}}\right)^2 (dt_1)}{\text{Time period}}} \tag{5.17}$$

$$i_{rms-sw2} = \sqrt{\frac{\left(i_{\text{peak}} \times \frac{c_2}{c_2+c_{\text{oss}}}\right)^2 (T) + \left(i_{\text{min}} \times \frac{c_2}{c_2+c_{\text{oss}}}\right)^2 (dt_2)}{\text{Time period}}} \tag{5.18}$$

Figure 5.29 and 5.30 below show the comparison between snubber losses calculated analytically using equation 5.17,5.18 and 5.16 and LTspice simulation.

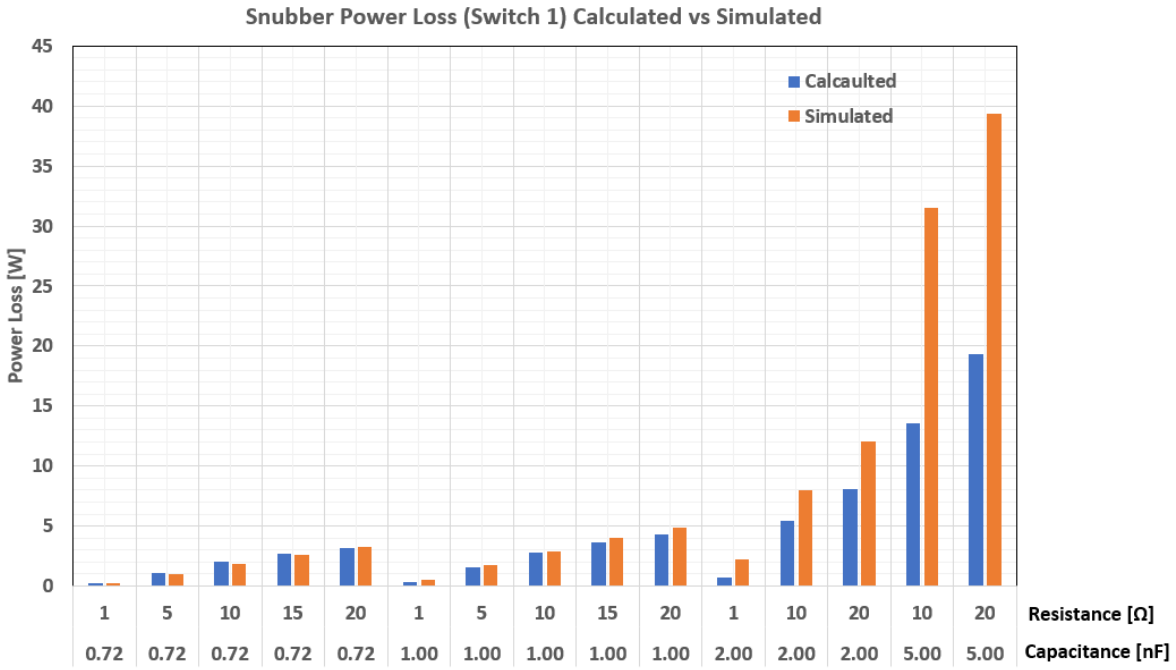


Figure 5.29: Analytically calculated snubber losses vs LTspice simulation results for Switch 1

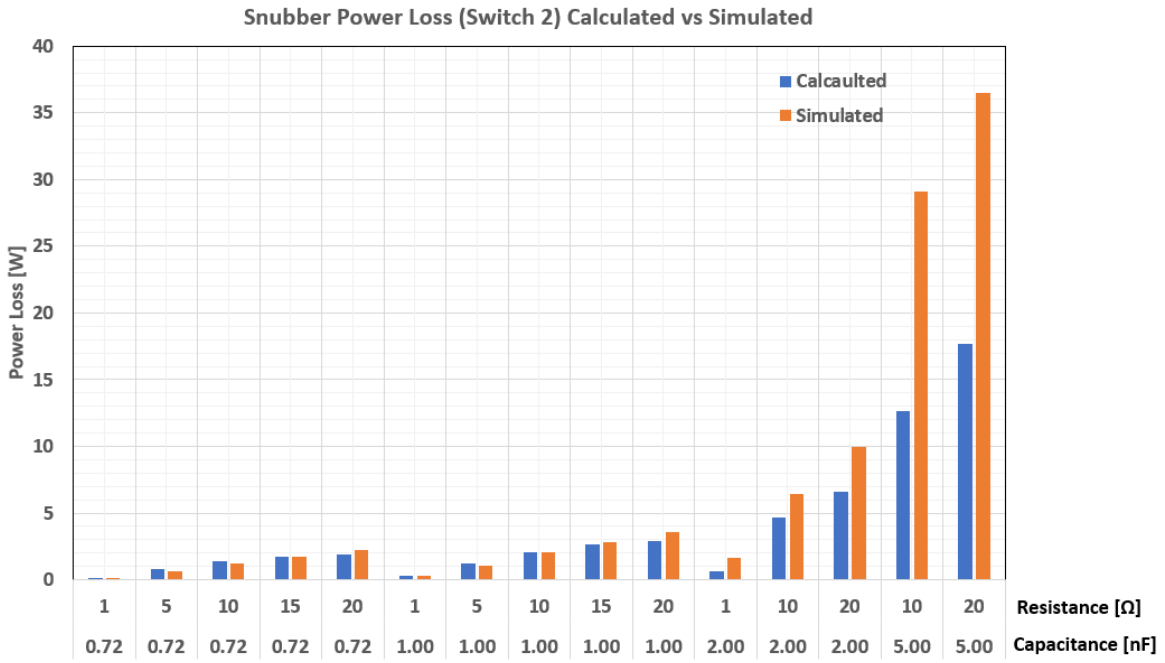


Figure 5.30: Analytically calculated snubber losses vs LTspice simulation results for Switch 2

It can be seen from the Figures that the correlation between the analytical solution and simulation holds good at lower capacitance values, but deviates at higher capacitance values. Also, it is better to select a small resistance value to limit extra losses due to the snubber element. Moreover, larger capacitance value should be avoided to ensure its complete discharge to achieve ZVS.

6
Conclusion and Recommendations

6.1. Conclusion

6.1.1. Voltage Balancer Topology:

Multiple topologies for the decentralised architecture of grid-connected voltage balancers were researched and the final voltage balancer topology selection was based on a simpler structure, fewer passive components, and higher cost efficiency of the **Synchronous buck-boost topology** shown in Figure 6.1 below:

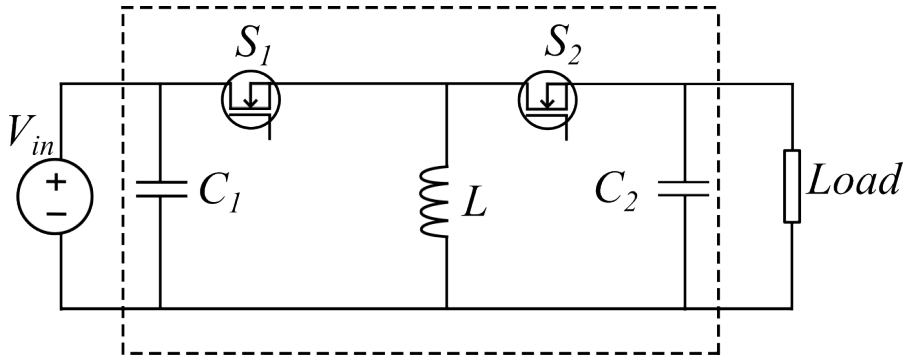


Figure 6.1: Synchronous Buck-Boost voltage balancer Topology

6.1.2. Switch Selection:

Main inferences from the Switch selection for voltage balancer design are as follows:

- **MOSFET selection:** The main parameters identified for MOSFET selection for an application are as below:

  1. Drain-source breakdown voltage
  2. Drain-source voltage
  3. Gate charge
  4. Package
  5. Output Capacitance
  6. Cost

  Based on the above parameters following MOSFETs were found to be suitable for the voltage balancer design for this project:

  - **Single MOSFET configuration: C2M0045170P**
  - **Series MOSFET Configuration: C3M0030090K**

- **Switching Loss:** The two MOSFETs were evaluated for switching losses for the intended operating conditions for the target voltage balancer and based on the results, **series connected C3M0030090K** was found to be more efficient than C2M0045170P MOSFET (Figure6.2).

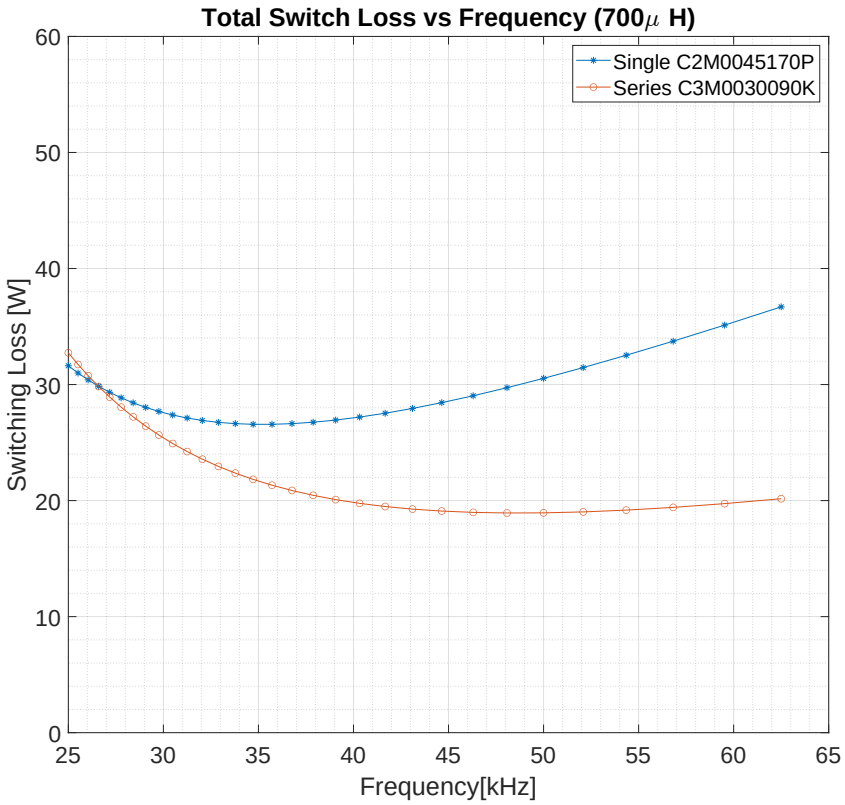


Figure 6.2: Total switching loss vs Frequency for single and series connected MOSFET for 700 μH inductance value. The total switching loss for single connected MOSFET is much higher than for series connected MOSFET for all switching frequency

- **Cost:** In terms of cost as well, **series connection of C3M0030090K** MOSFET was more economical than C2M0045170P MOSFET (see Table A.2 and Table A.1)

6.1.3. Inductor Design:

The main takeaways from the Inductor design process are as below:

- **Core Material:** Based on qualitative analysis of Ferrite and Magnetic steel core behaviour for high-frequency operation ($\geq$ 10kHz), the **Ferrite core** was finalised.

  Ferrite cores have high electrical resistance unlike Magnetic steel cores and thus are not susceptible to Eddy current losses.

  Among Ferrite core, materials **3C90, 3C92, 3C94, and 3C96** were chosen for further evaluation based on their applicability for switching frequency range of 10-100kHz and performance factor (f*B_{max}) evaluation.

- **Core Type: E** was found to be compatible based on core stack number limitation for achieving the required Area product (A_cA_w) value.

- **Core losses:** Core losses including Switch Conduction, Switch Turn-off, Winding, and Core losses were calculated for all the compatible core choices and core material.

- Conduction and Turn-off loss dominate the total converter loss, together contributing $\approx$. 85% of total converter loss at low frequency to $\approx$ 97% at high frequencies (Figure 3.9).

- At low frequencies, Conduction loss values are higher and it decreases with an increase in frequency. On the other hand, Turn-off losses increase with an increase in frequency.

- Winding loss and Core loss both decrease with an increase in frequency.

Based on the total converter loss evaluation shown in Figure 6.3 below, the final design for the Inductor was as given in Table 6.1.

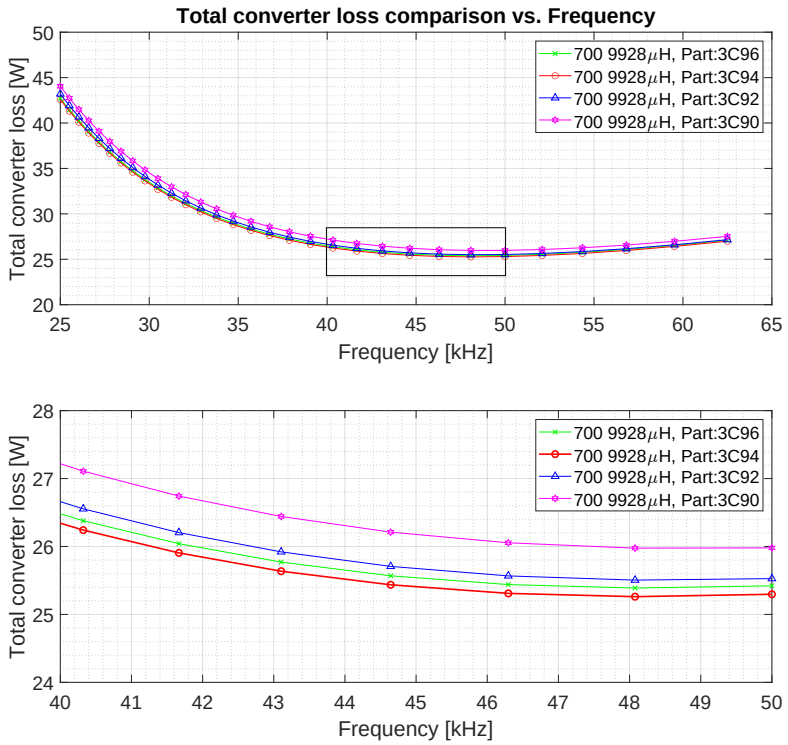


Figure 6.3: Total Converter loss vs Frequency for 700μH and part no 9928 for 3C90,3C92,3C94 and 3C96 material. The minimum converter loss obtained for each material, as seen in Figure[3.5] and Figure[3.6 are compared and it can be seen that for 3C94 material the total converter loss is observed to be the minimum at all operating frequencies.

Table 6.1: Final Inductor design parameters

Parameter	Value	Unit
Inductance	700	μH
Core Material	Ferrite Core: 3C94	-
Core Shape	E Core	-
Core Part	Part No: 9928	-

6.1.4. Voltage balancer simulation :

The main takeaways from the simulation of a series connected synchronous buck-boost voltage balancer on LTSpice are as below:

- **Unbalanced Load without non-linearity:** The series-connected synchronous buck-boost topology voltage balancer without any non-linearities is able to ensure voltage balance in a Bipolar DC grid with an unbalanced load across the poles. Further, the neutral line current balance is also ensured along with ZVS operation at the Turn-On of switches 1 and 2.

- **Unbalanced Load with non-linearity:**
  - **Turn on gate resistance R_{on}:** For non-linearity in voltage balancer of unequal turn on gate resistance across switch 1 and 2, the response of voltage balancer remains unaffected and balanced.

    The voltage across the pole line and switches remains balanced along with the neutral line current. Further at the turn-on of switches 1-2, ZVS is achieved.
  - **Parasitic capacitance:** For non-linearity in terms of the parasitic capacitance of up to 100pF across one of the switches, the voltage balancer was able to balance the phase voltage and neutral line current.

    However, the voltage across the switches became unbalanced, although ZVS at turn-on of switches 1-2 was achieved.
  - **Gate delay:** For non-linearity in terms of gate delay of 10ns across switch 2, the voltage balancer was able to balance the phase voltage. However, the neutral line current and the voltage distribution across switches 1-2 were unbalanced. Although, ZVS at turn-on was achieved (albeit barely).
- **Voltage balancing with RC snubber circuit:** For voltage balancer configuration with non-linearity of gate delay of 10ns in switch 2, the introduction of an RC snubber circuit results in an improvement in voltage distribution across the switches as compared to without the snubber circuit as seen from Fig 4.16 and 5.12. However, the trade-off is that for turn-on of switch 1-2 ZVS does not take place.

  In order to ensure ZVS at turn-on with RC snubber, the dead time between switches in the half-bridge configuration needs to be increased or the duty cycle needs to be decreased. However, at this instant, the neutral line current remains unbalanced.

  In order to improve the neutral line current, the switching frequency needs to be reduced, which further increases the voltage difference across the switches. The same was shown through LT-Spice simulation results in section 5.3.2.

  In conclusion, there exists a trade-off between voltage balance across the switches and neutral line current balance if ZVS at turn-on is ensured.

6.1.5. Analytical calculation model:

An analytical calculation model to estimate the voltage sharing across the series connected MOSFET switches at turn-off, the possibility of ZVS at turn-on, and power loss across the snubber resistance was developed.

The main takeaways from this model are listed below:

- The analytical model predicts the voltage sharing across the series connected switches at turn-off with non-linearity of gate delay in one of the switches very well. The analytical results correlate well with LTspice simulation results. (Figure 5.25 and Figure 5.26).
- Using analytical calculation, it was seen that with an increase in snubber capacitance-voltage difference across the series connected MOSFET switches goes down. However, with an increase in capacitance the discharge time of the capacitor increases, which limits the chances of achieving ZVS at turn-on. (Figure 5.27).

- The estimation of power loss across snubber resistors correlates well with LTspice simulation results for lower capacitance values. However, the deviation increases at higher capacitance values (Figure 5.29, 5.30).

6.2. Recommendations:

The recommendations for further research on the current topic are listed below:

- **MOSFET thermal model:** A thermal model to estimate and simulate the thermal behaviour of the MOSFET under different operating conditions should be developed. This will allow a better and more accurate estimation of the losses incurred in the system.

- **LTSPice Simulation model:** The LTSpice model should be improved to incorporate the effects of multiple non-linearities across 1 or more switches in the configuration.

- **Analytical calculation model:** The analytical model for power loss estimation deviates at higher capacitance values. The estimation of rms current should be evaluated in more detail to improve the model accuracy for all operating conditions.

- **Experimental validation:** The simulation results obtained for this work show promising results in using a voltage balancer for bipolar DC grids using synchronous buck-boost topology with series connected MOSFET and RC snubber circuit for voltage balancing. The simulation results need to be experimentally validated as the next step in this direction.

- **Topology:** Different topologies have been developed which have been found to be more efficient than the synchronous buck-boost topology chosen for this thesis. They should be explored in more detail to identify possibilities for implementation and efficiency improvement.

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A
Appendix:

A.1. MOSFET On Resistance vs Drain-Source Current

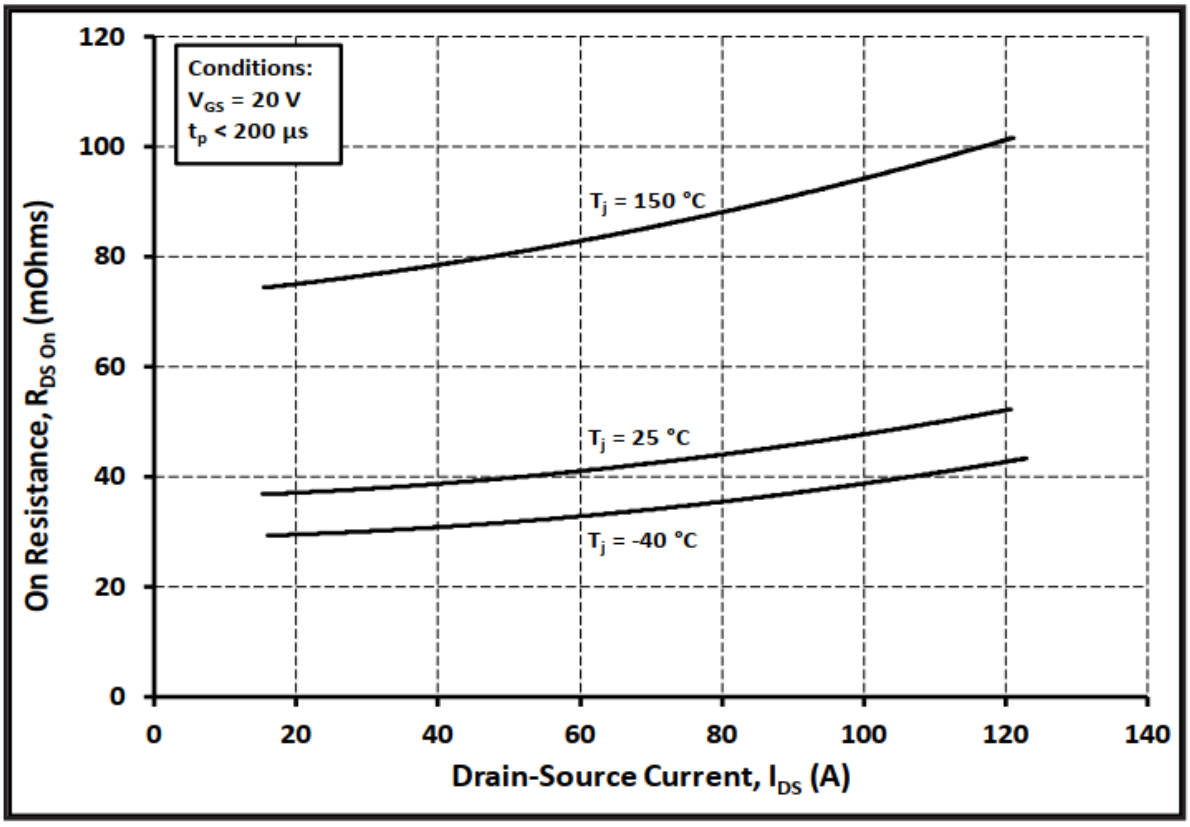

Figure A.1: $R_{(DS)on}$ vs I_{DS} for MOSFET C2M0045170P for different temperatures

A.2. MOSFET Switching Loss vs Drain-Source Current

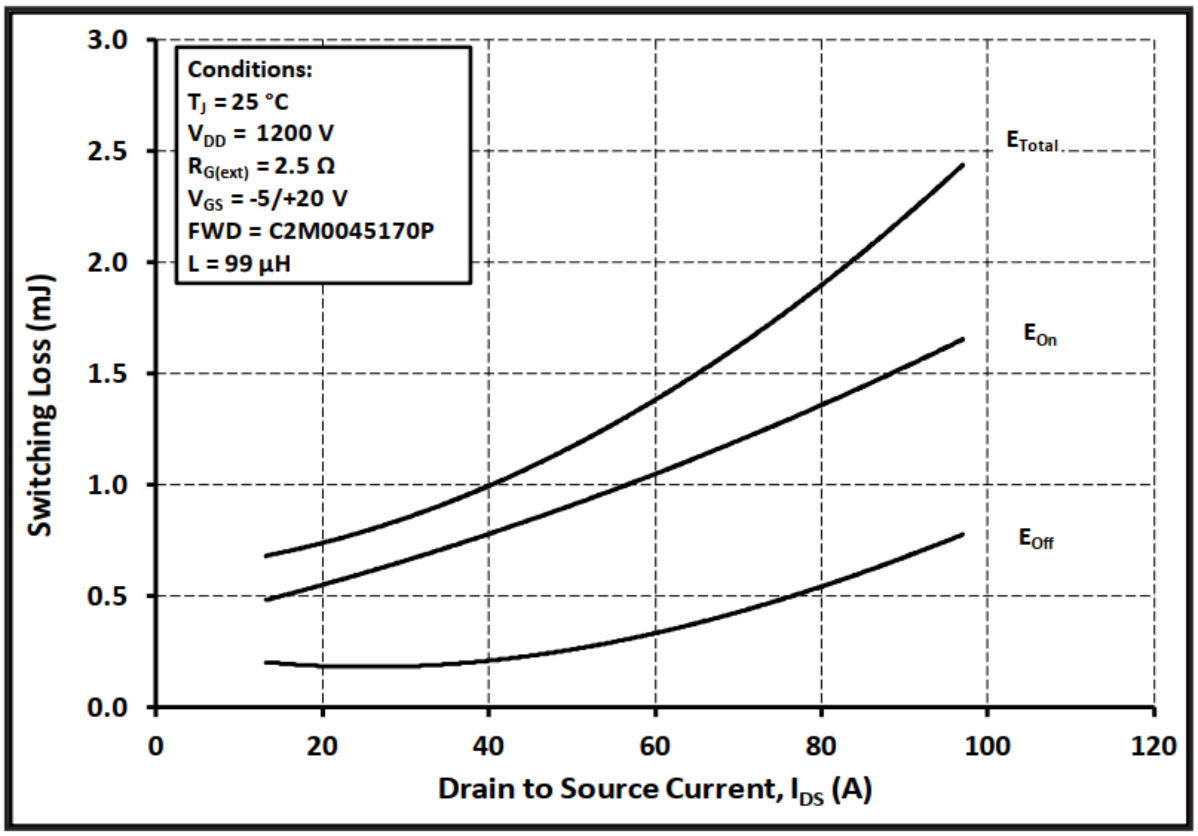

Figure A.2: Switching loss vs drain-source current for MOSFET C2M0045170P

A.3. Performance Factor plot for Ferrite core materials:

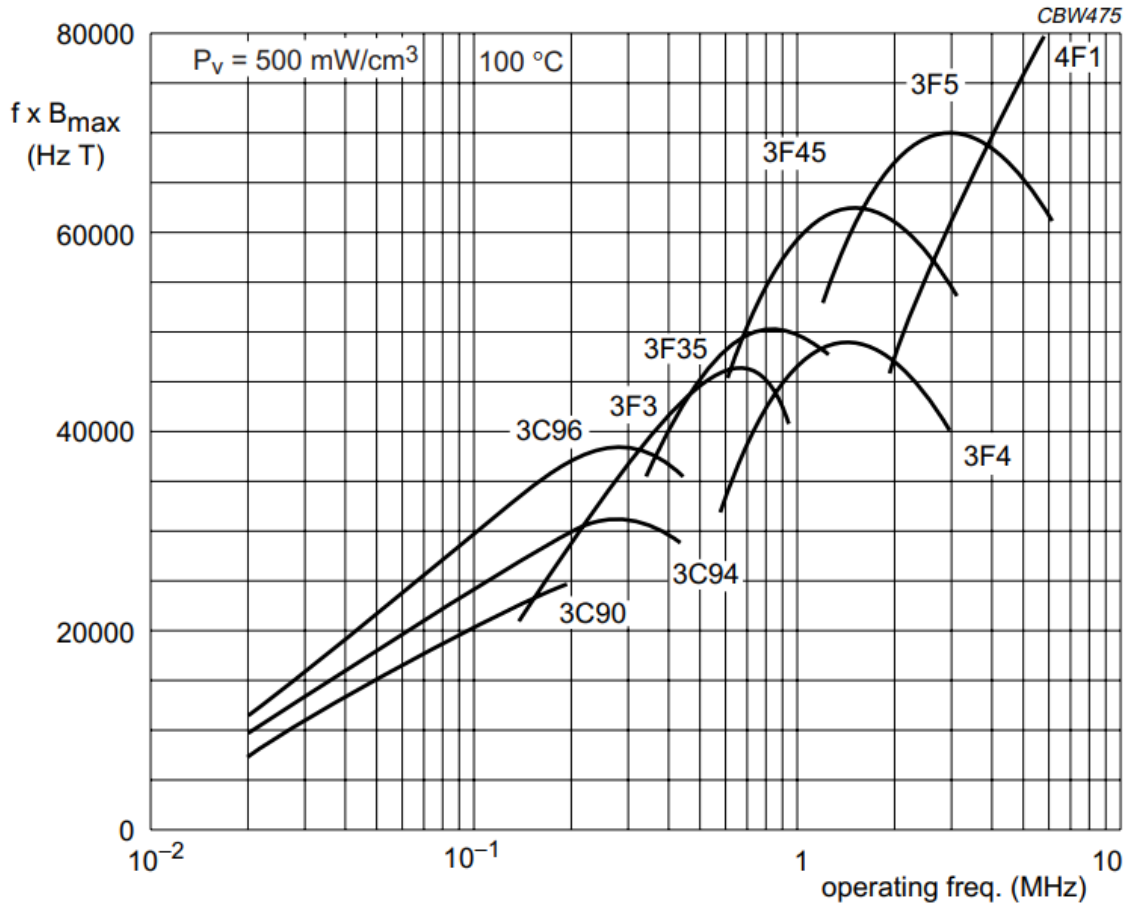

Figure A.3: Performance factor plot for different ferrite materials for the specific power loss of 500 $mWcm^{-3}$ [40]

A.4. Comparison of compatible MOSFETs for series connected configuration

Table A.1: Comparison of compatible MOSFETs for series connected configuration

Product	Blocking voltage	$R_{DS(on)}$ @25^{o}C	Current rating	Total Gate Charge	Output capacitance	Cost (per piece)	Total power dissipation	Max Temp	Package
	(V)	(mΩ)	(A)	(nC)	(pF)	(€)	(W)	(^{o}C)	
NTHL020N090SC1	900	28	118	196	296	40.75	503	175	TO-247-3
NVHL020N090SC1	900	28	118	196	296	49.5	503	175	TO-247-3
C3M0030090K	900	30	63	87	144	35.35	149	150	TO-247-4
NVHL060N090SC1	900	60	46	87	113	22.81	221	175	TO-247-3
NTHL060N090SC1	900	60	46	87	113	15.38	221	175	TO-247-3
NTH4L060N090SC1	900	60	46	87	113		221	175	
C3M0065090D	900	65	36	30	66	15.75	125	150	TO-247-3
C3M0120090D	900	120	23	17	40	10.85	97	150	TO-247-3
C3M0280090D	900	280	11.5	9.5	20	5.7	54	150	TO-247-3

A.5. Comparison of compatible MOSFETs for single connected configuration

Table A.2: Comparison of compatible MOSFETs for single connected configuration

Product	Blocking Voltage	RDS(on) @25oC	Current Rating	Total Gate Charge	Output Capacitance	Total power dissipation	Max junction Temp	Package
	(V)	mΩ	(A)	(nC)	(nF)	(W)	(^{o}C)	
G3R20MT17K	1700	20	101	256	205	569	175	TO-247-4
MSC035SMA170B4	1700	35	68	178	150	370	175	TO-247-4
G3R45MT17D	1700	45	52	106	86	364	175	TO-247-3
G3R45MT17K	1700	45	48	106	86	284	175	TO-247-4
C2M0045170D	1700	45	72	188	171	520	150	TO-247-3
MSC035SMA170B	1700	45	68	178	150	370	175	TO-247-3
C2M0045170P	1700	45	72	188	171	520	150	TO-247-4
G3R160MT17D	1700	160	17	29		138	175	TO-247-3
G3R450MT17D	1700	450	7	13		70	175	TO-247-3
MSC750SMA170B4	1700	750						TO-247-4
MSC750SMA170B	1700	750	5	11		68	175	TO-247-3
G2R1000MT17D	1700	1000	5	11		44	175	TO-247-3
LSIC1MO170E0750	1700	1000	6.2	13		60	175	TO-247-3
UF3C170400K3S	1700	1070	7.6	27.5		100	175	TO-247-3
C2M1000170D	1700	1400	4.9	13	19	69	150	TO-247-3

B
Formulas

B.1. Conduction Loss of MOSFET

$$P_{MOS-conduction} = \frac{1}{T_{sw}} \int_0^{T_{Sw}} \left(R_{DS(on)} \cdot i_D^2(t) \right) dt \tag{B.1}$$

Since,

$$I_{D_{rms}} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_D^2 dt} \tag{B.2}$$

$$\frac{1}{T_{sw}} \int_0^{T_{Sw}} \left(R_{DS(on)} \cdot i_D^2(t) \right) dt = R_{DS(on)} \cdot I_{Drms}^2 \tag{B.3}$$

Where,

$$I_{Drms} = \sqrt{D \left(\left(\frac{I_o}{1-D} \right)^2 + \frac{\Delta I_L^2}{12} \right)} \tag{B.4}$$

T_{sw}	Time period
$R_{DS(on)}$	On-resistance
i_D	Drain current
I_{Drms}	Root mean square of drain current
I_o	Average output current
ΔI_L	Inductor current ripple
D	Duty cycle

$$f = \frac{V_{in} * (1-D)}{L * \Delta I_L} \tag{B.5}$$

C
MATLAB Scripts:

C.1. MATLAB scripts

C.1.1. MATLAB script to calculate conduction and switching losses of single switch configuration of bipolar DC voltage balancer using MOSFET: C2M0045170P

```
%% Clear All
clc;
close all;
clearvars;

%% Construct structure
C2M0045170P = xlsread('C2M0045170P_FetchedDataRevised.csv');

%Initialising the structure
Switch=[];

%Parse data
first_field= C2M0045170P(:,1);                                  %I_DS
second_field= C2M0045170P(:,3);                                 %Eoff linearized
third_field= C2M0045170P(:,5);                                  %On-resistance @25
fourth_field= C2M0045170P(:,6);                                 %On-resistance @150
fifth_field= C2M0045170P(:,14);                                 %Third quad-resistance @25
sixth_field= C2M0045170P(:,10);                                 %Third quad-current @150
seventh_field= C2M0045170P(:,16);                               %Coss
eighth_field= C2M0045170P(:,12);                                %Third quad-current

%Remove NaNs
first_field(isnan(first_field))=[];
second_field(isnan(second_field))=[];
third_field(isnan(third_field))=[];
fourth_field(isnan(fourth_field))=[];
fifth_field(isnan(fifth_field))=[];
sixth_field(isnan(sixth_field))=[];
seventh_field(isnan(seventh_field))=[];
eighth_field(isnan(eighth_field))=[];

%Add data to structure
Switch.OnState.I_DS= first_field;
Switch.TurnOff.E_off=second_field;
Switch.OnState.R_DSon_At25= third_field;
Switch.OnState.R_DSon_At150= fourth_field;
Switch.ThirdQuad_resistance_At25=fifth_field;
Switch.ThirdQuad_resistance_At150=sixth_field;
Switch.OutputCapacitance=seventh_field;
Switch.ThirdQuad_current=eighth_field;
Switch.OnState.tj= [25 150];
Switch.TurnOff.tj=[25 150];
Switch.Thermal.juncTocase=0;
Switch.Thermal.juncThermalCap=0;

%% Mosfet losses
D=0.5;                                                          %Duty cycle
Vin= 700;
numOfSwitchesInSeries=1;
L= 500*10^-6:50*10^-6:800*10^-6;                                %Inductance [H]
Effective_capacitance= 8/3*Switch.OutputCapacitance;            %[F] 2 switches, set of 2 in series and
↪  parallel to each other

Iout=2:0.2:8;
r=zeros(1, length(Iout));
Rds=zeros(1, length(Iout));
Eoff=zeros(1, length(Iout));
s=zeros(1, length(Iout));
Rds_thirdQuad=zeros(1, length(Iout));
I_peak=zeros(length(L), length(Iout));
f=zeros(length(L), length(Iout));
```

```
delI=zeros(length(L), length(Iout));
I_Drms=zeros(length(L), length(Iout));
Pconduction=zeros(length(L), length(Iout));
Pconduction_switch2=zeros(length(L), length(Iout));
Total_conduction_loss=zeros(length(L), length(Iout));
Turn_off=zeros(length(L), length(Iout));
Loss_switch=zeros(length(L), length(Iout));

for ij= 1:length(L)

    dead_time= 200*10^-9;                                                   %[s]
    Icap(ij)= sqrt(8*39*10^-6/L(ij));                                      %Alternative formula for I_cap calculation
    I_cap(ij)= (sqrt((Effective_capacitance*Vin^2)/L(ij)));
    I_cap1(ij)= Effective_capacitance*Vin/dead_time;
    I_cap2(ij)=2;
    %dead_time(ij)= Effective_capacitance*Vin/I_cap2(ij);


    for j= 1:length(Iout)
        r(j)=find(abs(Switch.OnState.I_DS-Iout(j))<1e-6);
        Rds(j)=Switch.OnState.R_DSon_At150(r(j));
        Eoff(j)=second_field(r(j));
        s(j)=find(abs((Switch.ThirdQuad_current*-1)-Iout(j))<1e-6);
        Rds_thirdQuad(j)=Switch.ThirdQuad_resistance_At150(s(j));
        I_peak(ij,j)= 2*Iout(j)+I_cap2(ij);                                 %Ipeak-Icap/2=Iout(avg)
        Eoff_u(j)=Eoff_calc(I_peak(ij,j))*(7/6);
        Eoff_l(j)=Eoff_calc(I_cap2(ij))*(7/6);
        f(ij,j)= Vin*(1-D)/(L(ij)*(I_peak(ij,j)));                          %Frequency calculated at peak current
        delI(ij,j)=I_peak(ij,j)+I_cap2(ij);
        I_Drms(ij,j)= sqrt(D*((Iout(j)/(1-D))^2+((delI(ij,j))^2/12)));

        Pconduction(ij,j)=numOfSwitchesInSeries*I_Drms(ij,j).^2*Rds(j)*10^-3;
        Pconduction_switch2(ij,j)= numOfSwitchesInSeries*I_Drms(ij,j).^2*Rds_thirdQuad(j);
        Total_conduction_loss(ij,j)=Pconduction(ij,j)+Pconduction_switch2(ij,j);

        Turn_off(ij,j)= 2*Eoff(j)*10^-6*(f(ij,j))*2;                        %2* to account temp & RG(ext) dependency
        Turn_off_u(ij,j)= 2*Eoff_u(j)*10^-6*(f(ij,j))*1;
        Turn_off_l(ij,j)= 2*Eoff_l(j)*10^-6*(f(ij,j))*1;

        Loss_switch(ij,j)=Turn_off_u(ij,j)+Turn_off_l(ij,j)+Total_conduction_loss(ij,j);
        Turnoff_total(ij,j)=Turn_off_u(ij,j)+Turn_off_l(ij,j);
    end
end
```

C.1.2. MATLAB script to calculate total converter loss of series connected switch configuration of bipolar DC voltage balancer using MOSFET: C3M0030090K

```
%% Clear All
clc;
close all;
clearvars;

%% Construct structure
C3M0030090K = xlsread('C3M0030090K_FetchedDataRevised.csv');

%Initialising the structure
Switch=[];

%Parse data
first_field= C3M0030090K(:,1);                                              %I_DS
second_field= C3M0030090K(:,3);                                             %Eoff linearized
third_field= C3M0030090K(:,5);                                              %On-resistance @25
fourth_field= C3M0030090K(:,6);                                             %On-resistance @150
fifth_field= C3M0030090K(:,14);                                             %Third quad-resistance @25
sixth_field= C3M0030090K(:,10);                                             %Third quad-current @150
seventh_field= C3M0030090K(:,16);                                           %Coss
eighth_field= C3M0030090K(:,12);                                            %Third quad-current

%Remove NaNs
first_field(isnan(first_field))=[];
second_field(isnan(second_field))=[];
third_field(isnan(third_field))=[];
fourth_field(isnan(fourth_field))=[];
fifth_field(isnan(fifth_field))=[];
sixth_field(isnan(sixth_field))=[];
seventh_field(isnan(seventh_field))=[];
eighth_field(isnan(eighth_field))=[];

%Add data to structure
Switch.OnState.I_DS= first_field;
Switch.TurnOff.E_off=second_field;
```

```
Switch.OnState.R_DSon_At25= third_field;
Switch.OnState.R_DSon_At150= fourth_field;
Switch.ThirdQuad_resistance_At25=fifth_field;
Switch.ThirdQuad_resistance_At150=sixth_field;
Switch.OutputCapacitance=seventh_field;
Switch.ThirdQuad_current=eighth_field;
Switch.OnState.tj= [25 150];
Switch.TurnOff.tj=[25 150];
Switch.Thermal.juncTocase=0;
Switch.Thermal.juncThermalCap=0;

%% Mosfet losses
D=0.5;                                                          %Duty cycle
Vin= 700;
numOfSwitchesInSeries=2;
L= 500*10^-6:50*10^-6:800*10^-6;                                %Inductance [H]
%Effective_capacitance= 8/3*Switch.OutputCapacitance;           %[F] 2 switches in parallel hence 8/3
Effective_capacitance= 4/3*Switch.OutputCapacitance;            %[F] 4 switches, set of 2 in series and
    ↪  parallel to each other

%I_cap=zeros(1, length(L));
%I_cap2=zeros(1, length(L));
%dead_time=zeros(1, length(L));
Iout=2:0.2:8;
r=zeros(1, length(Iout));
Rds=zeros(1, length(Iout));
Eoff=zeros(1, length(Iout));
s=zeros(1, length(Iout));
Rds_thirdQuad=zeros(1, length(Iout));
I_peak=zeros(length(L), length(Iout));
f=zeros(length(L), length(Iout));
delI=zeros(length(L), length(Iout));
I_Drms=zeros(length(L), length(Iout));
Pconduction=zeros(length(L), length(Iout));
Pconduction_switch2=zeros(length(L), length(Iout));
Total_conduction_loss=zeros(length(L), length(Iout));
Turn_off=zeros(length(L), length(Iout));
Loss_switch=zeros(length(L), length(Iout));
%Rg=2.5;
% T=150;
for ij= 1:length(L)

    I_cap(ij)= sqrt(8*39*10^-6/L(ij));                          %Alternative formula for I_cap calculation
    I_cap2(ij)=2;
    I_capp(ij)= (sqrt((Effective_capacitance*Vin^2)/L(ij)));
    dead_time= 200*10^-9;                                       %Value should be when series connected and no
    ↪  non-linearities exist
    I_cappp(ij)= Effective_capacitance*Vin/dead_time;
    %dead_time(ij)= Effective_capacitance*Vin/I_cap2(ij);


    for j= 1:length(Iout)
        r(j)=find(abs(Switch.OnState.I_DS-Iout(j))<1e-6);
        Rds(j)=Switch.OnState.R_DSon_At150(r(j));
        Eoff(j)=second_field(r(j));
        s(j)=find(abs((Switch.ThirdQuad_current*-1)-Iout(j))<1e-6);
        Rds_thirdQuad(j)=Switch.ThirdQuad_resistance_At150(s(j));
        I_peak(ij,j)= 2*Iout(j)+I_cap2(ij);                     %Ipeak-Icap/2=Iout(avg)
        Eoff_u(j)=Eoff_calc(I_peak(ij,j))*(7/6);
        Eoff_l(j)=Eoff_calc(I_cap2(ij))*(7/6);
        f(ij,j)= Vin*(1-D)/(L(ij)*(I_peak(ij,j)));              %Frequency calculated at peak current
        delI(ij,j)=I_peak(ij,j)+I_cap2(ij);
        I_Drms(ij,j)= sqrt(D*((Iout(j)/(1-D))^2+((delI(ij,j))^2/12)));

        Pconduction(ij,j)=numOfSwitchesInSeries*I_Drms(ij,j).^2*Rds(j)*10^-3;                   %Include
    ↪  numOfSwitchesInSeries variable to line 80&81 later
        Pconduction_switch2(ij,j)= numOfSwitchesInSeries*I_Drms(ij,j).^2*Rds_thirdQuad(j);
        Total_conduction_loss(ij,j)=Pconduction(ij,j)+Pconduction_switch2(ij,j);

        Turn_off(ij,j)= 2*Eoff(j)*10^-6*(f(ij,j))*4;            %2* to account temp & RG(ext) dependency, add
    ↪  numOfSwitchesInSeries variable later
        Turn_off_u(ij,j)= 2*Eoff_u(j)*10^-6*(f(ij,j))*2;
        Turn_off_l(ij,j)= 2*Eoff_l(j)*10^-6*(f(ij,j))*2;
        Turn_off_total(ij,j)= Turn_off_u(ij,j)+ Turn_off_l(ij,j);
        %Turn_off2(ij,j)= [[(0.0535*I_Drms(ij,j).^2 - 0.4722*I_Drms(ij,j)+ 42.437)+((16.9867*Rg+(48.084+(0.0001*T^2 +
    ↪  0.0465*T-0.90755)))-91.4475)]*(700/600)]*(f(ij,j))*4;
      Loss_switch_2(ij,j)=Turn_off(ij,j)+Total_conduction_loss(ij,j);
        Loss_switch(ij,j)=Turn_off_u(ij,j)+Turn_off_l(ij,j)+Total_conduction_loss(ij,j);
    end
end
%% Magnetic loss
Cores = load('COREstructure.mat');
Core_options=[];

```

```
114 %Area product calculation for core selection
115
116 % %Worst cases: Maximum avg current(8A), Maximum frequency(2A), Somewhere
117 % in between(5A) respectively
118 [I_Peak,DelI,I_DRMS,AcAw]= AreaProduct_function(8,I_cap,D,L,constants.J,constants.k,constants.B);
119 [I_Peak_WC2,DelI_WC2,I_DRMS_WC2,AcAw_WC2]= AreaProduct_function(2,I_cap,D,L,constants.J,constants.k,constants.B);
120 [I_Peak_WC3,DelI_WC3,I_DRMS_WC3,AcAw_WC3]= AreaProduct_function(5,I_cap,D,L,constants.J,constants.k,constants.B);
121 AcAw_max= max(max(AcAw, AcAw_WC2),AcAw_WC3);
122
123 %Core selection--> E core
124
125 for kk=1:length(AcAw_max)
126     No_of_parts_stacked_E= ceil(AcAw_max./Cores.Cores.E_core.WaAccm4);
127     Total_volumeObtained_E=No_of_parts_stacked_E.*Cores.Cores.E_core.VeVolumemm3;
128     windowArea_E= Cores.Cores.E_core.Awmm2;
129     CoreArea_E= No_of_parts_stacked_E.*Cores.Cores.E_core.AeCrossSectionmm2;
130     A_E= Cores.Cores.E_core.Amm;
131     B1_E= Cores.Cores.E_core.B1mm;
132     C_E= No_of_parts_stacked_E.*Cores.Cores.E_core.Cmm;
133     D1_E= Cores.Cores.E_core.D1mm;
134     F_E= Cores.Cores.E_core.Fmm;
135     M_E= Cores.Cores.E_core.Mmm;
136     L_E= Cores.Cores.E_core.Lmm;
137     Core_options.Core_options_E(:,:,kk) =[Cores.Cores.E_core.Part, No_of_parts_stacked_E(:,kk),
    ↪  Total_volumeObtained_E(:,kk),windowArea_E, CoreArea_E(:,kk), A_E, B1_E, C_E(:,kk), D1_E, F_E, M_E, L_E];
138 end
139
140 %Core selection--> E core fit to use after limitation on stack number
141 c = find (Core_options.Core_options_E(:,2,:) <=4);
142 [x ,y, z] = ind2sub(size(Core_options.Core_options_E(:,2,:)),c);
143 bb=1;
144 cc=0;
145
146 for aa=1:length(x)
147     if z(aa)==bb
148         cc=cc+1;
149     else
150         cc=1;
151     end
152     Core_options.CoresFit2use_Ecore(cc,:,z(aa))=[Core_options.Core_options_E(x(aa),1,z(aa))
    ↪  Core_options.Core_options_E(x(aa),2,z(aa)) Core_options.Core_options_E(x(aa),3,z(aa))
    ↪  Core_options.Core_options_E(x(aa),4,z(aa)) Core_options.Core_options_E(x(aa),5,z(aa))
    ↪  Core_options.Core_options_E(x(aa),6,z(aa)) Core_options.Core_options_E(x(aa),7,z(aa))
    ↪  Core_options.Core_options_E(x(aa),8,z(aa)) Core_options.Core_options_E(x(aa),9,z(aa))
    ↪  Core_options.Core_options_E(x(aa),10,z(aa)) Core_options.Core_options_E(x(aa),11,z(aa))
    ↪  Core_options.Core_options_E(x(aa),12,z(aa))];
153     bb=z(aa);
154 end
155 [RowsCoresFit2use_Ecore,numColsCoresFit2use_Ecore] = size(Core_options.CoresFit2use_Ecore);
156 %%Core loss calculation
157 T=25;
158 P_vold = 100000;
159 P_v = 0;
160 wl1=1;
161 while abs(P_v-P_vold)>1000 && T<200
162     P_vold = P_v;
163     [k_3C96,ki]= Ki_generatorFunction(constants.Cm, constants.ct2, constants.ct1, constants.ct, T, constants.alpha,
    ↪  constants.beta);
164     [k_3C94,ki_3C94]= Ki_generatorFunction(constants.Cm_3C94, constants.ct2_3C94, constants.ct1_3C94, constants.ct_3C94,
    ↪  T, constants.alpha_3C94, constants.beta_3C94);
165     [k_3C92,ki_3C92]= Ki_generatorFunction(constants.Cm_3C92, constants.ct2_3C92, constants.ct1_3C92, constants.ct_3C92,
    ↪  T, constants.alpha_3C92, constants.beta_3C92);
166     [k_3C90,ki_3C90]= Ki_generatorFunction(constants.Cm_3C90, constants.ct2_3C90, constants.ct1_3C90, constants.ct_3C90,
    ↪  T, constants.alpha_3C90, constants.beta_3C90);
167
168
169
170     for nn1=1:length(L)
171         for mm1=1:RowsCoresFit2use_Ecore
172             Aw_E(mm1,nn1)= Core_options.CoresFit2use_Ecore(mm1,4,nn1);
173             Ac1(mm1,nn1)= Core_options.CoresFit2use_Ecore(mm1,5,nn1)*10^-6;%[m2]
174         end
175     end
176
177     N_Ecore= ceil(L.*I_Peak./(constants.B.*Ac1));
178
179     A_cu=5*10^-6;                                                    %[m^2]
180     % Ng=4;
181     % l_air_fringing= Ac./(((constants.B.*Ac)/(N.*constants.mu_0.*I_Peak))-((C+F)./Ng));
182     rho=1.72*10^-8;                                                  %[ohm m]
183     diameter= sqrt((A_cu*4)/pi)*10^3;
184
185     %Compatibility of number of turns with the core selected
186     check_compatibility= A_cu*10^6.*N_Ecore <= constants.k.*Aw_E;          %[areas in mm2]
```

```
187     Maximum_N_Ecore= floor((constants.k.*Aw_E)/(A_cu*10^6));              %[areas in mm2]
188     %*************************************************************************************************************
189     [rows,columns]=find((check_compatibility)==1);
190     for pp=1:length(rows)
191         Core_options.CoresFit2use_Ecore_AfterCompatibility(pp,:,columns(pp))=Core_options.CoresFit2use_Ecore
    ↪   (rows(pp),:,columns(pp));
192         s=columns(pp);
193     end
194
195
196     [rowsCoresFit2use_Ecore,NumColsCoresFit2use_Ecore, L_CoresFit2use_Ecore] =
    ↪   size(Core_options.CoresFit2use_Ecore_AfterCompatibility);
197
198     for nn=1:L_CoresFit2use_Ecore
199         for mm=1:rowsCoresFit2use_Ecore
200             Ve(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,3,nn)*10^-3;          %[cm3]
201             Aw_E1(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,4,nn);
202             Ac(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,5,nn)*10^-6;          %[m2]
203             A(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,6,nn);                 %[all values in mm]
204             B1(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,7,nn);
205             C(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,8,nn);
206             D1(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,9,nn);
207             F(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,10,nn);
208             M(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,11,nn);
209             L1(mm,nn)= Core_options.CoresFit2use_Ecore_AfterCompatibility(mm,12,nn);
210         end
211     end
212     L_compatible=L(1:L_CoresFit2use_Ecore);
213     N= ceil(L_compatible.*I_Peak(1:L_CoresFit2use_Ecore)./(constants.B.*Ac));
214     % NumberOfTurns= ceil(N);
215     %delB=(1./(N.*Ac)).*L.*delI;
216     delB=(constants.B*delI(1:L_CoresFit2use_Ecore, :))./I_Peak(1:L_CoresFit2use_Ecore)';
    ↪   %N*Ac= (L*I_Peak)/B from N formula
217     lair= (N.^2.*constants.mu_0.*Ac)./(2*L_compatible);
218     Maximum_N= floor((constants.k.*Aw_E1)/(A_cu*10^6));
219
220     % Core_options.CoresFit2use_Ecore_AfterCompatibility=;
221     %Winding losses
222     MidLeg_length= (2*D1+lair*10^3);                                      %[mm]
223     num_of_conductors = (MidLeg_length)/diameter;
224     num_of_layers=ceil(N./num_of_conductors);
225     l_previous=2*(2*M+C+F)*10^-3.*N;                                      %[m]
226     l=2*((2*(num_of_layers*diameter)+F)+(C+2*(num_of_layers*diameter)))*10^-3.*N;  %[m]
227     Rdc=rho*l/A_cu;                                                       %[ohm]
228
229     Extension_area=(2*(num_of_layers*diameter)+F).*MidLeg_length*2;
230     At= 2*(A.*C)+4*(B1.*C)+4*(A.*(B1-D1))+8*(D.*L1)+ Extension_area;      %[mm2]
231     %At= 2*(A.*C)+2*((2*B1+lair).*C)+4*(A.*(B1-D1))+8*(D.*L1)+ Extension_area;  %[mm2]
232
233     %J_check=I_DRMS/A_cu;
234     %A_cu_calculated=I_DRMS/constants.J
235
236     %g=zeros(1, length(Iout));
237     Pcore_loss_3C96=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
238     Pcore_loss_3C94=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
239     Pcore_loss_3C92=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
240     Pcore_loss_3C90=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
241     Ts=zeros(L_CoresFit2use_Ecore, length(Iout));
242     loss=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
243     Pwinding=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
244     Total_Magneticloss_3C96=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
245     Total_Magneticloss_3C94=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
246     Total_Magneticloss_3C92=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
247     Total_Magneticloss_3C90=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
248     Total_Converterloss_With3C96=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
249     Total_Converterloss_With3C94=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
250     Total_Converterloss_With3C92=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
251     Total_Converterloss_With3C90=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
252     delT_3C96=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
253     delT_3C94=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
254     delT_3C92=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
255     delT_3C90=zeros(rowsCoresFit2use_Ecore, length(Iout), L_CoresFit2use_Ecore);
256
257
258     for oj=1:L_CoresFit2use_Ecore
259         for z= 1:length(Iout)
260             for zz= 1:rowsCoresFit2use_Ecore
261                 Ts(oj,z)= 1/f(oj,z);
262                 Pcore_loss_3C96(zz,z,oj)=Coreloss(delB(oj,z),constants.alpha,constants.beta,Ve(zz,oj),D,Ts(oj,z),ki);
263
    ↪   Pcore_loss_3C94(zz,z,oj)=Coreloss(delB(oj,z),constants.alpha_3C94,constants.beta_3C94,Ve(zz,oj),D,Ts(oj,z),ki_3C94);
264
    ↪   Pcore_loss_3C92(zz,z,oj)=Coreloss(delB(oj,z),constants.alpha_3C92,constants.beta_3C92,Ve(zz,oj),D,Ts(oj,z),ki_3C92);
```

```
265
    ↪ Pcore_loss_3C90(zz,z,oj)=Coreloss(delB(oj,z),constants.alpha_3C90,constants.beta_3C90,Ve(zz,oj),D,Ts(oj,z),ki_3C90);
266                 %Pcore_loss=min(min(min(Pcore_loss_3C90,Pcore_loss_3C92),Pcore_loss_3C94),Pcore_loss_3C96);
267
268                 Pwinding(zz,z,oj)= I_Drms(oj,z)^2*Rdc(zz,oj)*1000;
269
270                 Total_Magneticloss_3C96(zz,z,oj)= Pcore_loss_3C96(zz,z,oj)+Pwinding(zz,z,oj);
271                 Total_Magneticloss_3C94(zz,z,oj)= Pcore_loss_3C94(zz,z,oj)+Pwinding(zz,z,oj);
272                 Total_Magneticloss_3C92(zz,z,oj)= Pcore_loss_3C92(zz,z,oj)+Pwinding(zz,z,oj);
273                 Total_Magneticloss_3C90(zz,z,oj)= Pcore_loss_3C90(zz,z,oj)+Pwinding(zz,z,oj);
274
275                 Total_Converterloss_With3C96(zz,z,oj)=Loss_switch(oj,z)*1000+Pcore_loss_3C96(zz,z,oj)+Pwinding(zz,z,oj);
276                 Total_Converterloss_With3C94(zz,z,oj)=Loss_switch(oj,z)*1000+Pcore_loss_3C94(zz,z,oj)+Pwinding(zz,z,oj);
277                 Total_Converterloss_With3C92(zz,z,oj)=Loss_switch(oj,z)*1000+Pcore_loss_3C92(zz,z,oj)+Pwinding(zz,z,oj);
278                 Total_Converterloss_With3C90(zz,z,oj)=Loss_switch(oj,z)*1000+Pcore_loss_3C90(zz,z,oj)+Pwinding(zz,z,oj);
279
280
281                 delT_3C96(zz,z,oj)= ((Total_Magneticloss_3C96(zz,z,oj)./(At(zz,oj)*10^-2))).^0.833;
    ↪ %[degree C]
282                 delT_3C94(zz,z,oj)= ((Total_Magneticloss_3C94(zz,z,oj)./(At(zz,oj)*10^-2))).^0.833;
283                 delT_3C92(zz,z,oj)= ((Total_Magneticloss_3C92(zz,z,oj)./(At(zz,oj)*10^-2))).^0.833;
284                 delT_3C90(zz,z,oj)= ((Total_Magneticloss_3C90(zz,z,oj)./(At(zz,oj)*10^-2))).^0.833;
285
286
287
288             end
289
290         end
291     end
292
293     %To find the optimal temperature
294     P_v= max(Pcore_loss_3C96(:,end,end));
295     %P_v= max(Pcore_loss_3C94(:,end,end));
296     %P_v= max(Pcore_loss_3C92(:,end,end));
297     % P_v= max(Pcore_loss_3C90(:,end,end));
298     PV(wl1)=P_v;
299     Ploss = P_v + max(Pwinding(:,end,end));
300
301     P_LOSS(wl1)=Ploss;
302     disp("core loss= "+num2str(P_v*10^-3)+" W");
303     disp("magnetic loss= "+num2str(Ploss*10^-3)+" W");
304     delT= ((Ploss/(max(At(:,end))*10^-2)))^0.833;
305     DT(wl1)=delT;
306     T1(wl1)=T;
307     T = T+delT;
308     wl1=wl1+1;
309     disp("Temperature= "+num2str(T)+char(176)+"C");
310
311     % disp(num2str(ceil(P_v)))
312 end
313
314 %% Plot
315 figure(1)
316 yyaxis left
317 hold on
318
319 for ii=1:L_CoresFit2use_Ecore
320     plot(f(ii,:)/1000,Total_Converterloss_With3C96(:,:,ii))
321     ylabel("Loss [mW]")
322     xlabel("Frequency [kHz]")
323 end
324 yyaxis right
325 for ii=1:L_CoresFit2use_Ecore
326     plot(f(ii,:)/1000,Iout)
327     ylabel("Iout [A]")
328 end
329 legend(num2str(Core_options.CoresFit2use_Ecore_AfterCompatibility(:,1,:)))
330 title("Variation of total converter loss 3C96 material with Io&f for all the cores for L=",L(ii)*10^6)
331
332
333 %% 3D plot for Total_Converterloss_With3C94 material
334 figure(2)
335 plot3(f(1,:)/1000, Iout, Total_Converterloss_With3C94(:,:,1));
336 hold on
337 for ii=2:L_CoresFit2use_Ecore
338     plot3(f(ii,:)/1000, Iout, Total_Converterloss_With3C94(:,:,ii));
339 end
340 xlabel("Frequency [kHz]")
341 ylabel("Iout [A]")
342 zlabel("Total converter loss 3C94 [mW]")
343 title('3D representation of Frequency vs. Iout vs. Total converter loss for 3C94 material')
344
345 %2D plot for Total_Converterloss_With3C94 material
346 figure(3)
```

```
plot(f(1,:)/1000, Total_Converterloss_With3C94(:,:,1));
hold on
for ii=2:L_CoresFit2use_Ecore
    plot(f(ii,:)/1000, Total_Converterloss_With3C94(:,:,ii));
end
xlabel("Frequency [kHz]")
ylabel("Total converter loss 3C94 [mW]")
title('2D representation of Frequency vs. Total converter loss for 3C94 material')


%% Plot for Total_Converterloss vs. Frequency

%Material: 3C90
figure(4)
xx_3C90 = 1;
marker='o+x*ds^ph<>';
for n_3C90=1:L_CoresFit2use_Ecore
    for m_3C90 = 1:rowsCoresFit2use_Ecore
        if ~isnan(Total_Converterloss_With3C90(m_3C90,1,n_3C90))
            plot(f(n_3C90,:)/1000, Total_Converterloss_With3C90(m_3C90,:,n_3C90)*10^-3,'Marker',marker(m_3C90))
            hold on
            legend_3C90(xx_3C90,1) = L(n_3C90);
            legend_3C90(xx_3C90,2) = Core_options.CoresFit2use_Ecore_AfterCompatibility(m_3C90,1,n_3C90);
            xx_3C90 = xx_3C90 + 1;
        end
    end
end
rrr_3C90=num2str(legend_3C90(:,1)*10^6);
qqq_3C90=num2str(legend_3C90(:,2));
legend(strcat(rrr_3C90,32,qqq_3C90),'fontsize',11)
xlabel("Frequency [kHz]")
ylabel("Total converter loss [W]")
title('3C90 material: Total converter loss vs. Frequency')

%Material: 3C92
figure(5)
xx_3C92 = 1;
marker='o+x*ds^ph<>';
for n_3C92=1:L_CoresFit2use_Ecore
    for m_3C92 = 1:rowsCoresFit2use_Ecore
        if ~isnan(Total_Converterloss_With3C92(m_3C92,1,n_3C92))
            plot(f(n_3C92,:)/1000, Total_Converterloss_With3C92(m_3C92,:,n_3C92)*10^-3,'Marker',marker(m_3C92))
            hold on
            legend_3C92(xx_3C92,1) = L(n_3C92);
            legend_3C92(xx_3C92,2) = Core_options.CoresFit2use_Ecore_AfterCompatibility(m_3C92,1,n_3C92);
            xx_3C92 = xx_3C92 + 1;
        end
    end
end
rrr_3C92=num2str(legend_3C92(:,1)*10^6);
qqq_3C92=num2str(legend_3C92(:,2));
legend(strcat(rrr_3C92,32,qqq_3C92),'fontsize',11)
xlabel("Frequency [kHz]")
ylabel("Total converter loss [W]")
title('3C92 material: Total converter loss vs. Frequency')

%Material: 3C94
figure(6)
xx_3C94 = 1;
marker='o+x*ds^ph<>';
for n_3C94=1:L_CoresFit2use_Ecore
    for m_3C94 = 1:rowsCoresFit2use_Ecore
        if ~isnan(Total_Converterloss_With3C94(m_3C94,1,n_3C94))
            plot(f(n_3C94,:)/1000, Total_Converterloss_With3C94(m_3C94,:,n_3C94)*10^-3,'Marker',marker(m_3C94))
            hold on
            legend_3C94(xx_3C94,1) = L(n_3C94);
            legend_3C94(xx_3C94,2) = Core_options.CoresFit2use_Ecore_AfterCompatibility(m_3C94,1,n_3C94);
            xx_3C94 = xx_3C94 + 1;
        end
    end
end
rrr_3C94=num2str(legend_3C94(:,1)*10^6);
qqq_3C94=num2str(legend_3C94(:,2));
legend(strcat(rrr_3C94,32,qqq_3C94),'fontsize',11)
xlabel("Frequency [kHz]")
ylabel("Total converter loss [W]")
title('3C94 material: Total converter loss vs. Frequency')

%Material: 3C96
figure(7)
xx_3C96 = 1;
marker='o+x*ds^ph<>';
for n_3C96=1:L_CoresFit2use_Ecore
    for m_3C96 = 1:rowsCoresFit2use_Ecore
```

```
        if ~isnan(Total_Converterloss_With3C96(m_3C96,1,n_3C96))
            plot(f(n_3C96,:)/1000, Total_Converterloss_With3C96(m_3C96,:,n_3C96)*10^-3,'Marker',marker(m_3C96))
            hold on
            legend_3C96(xx_3C96,1) = L(n_3C96);
            legend_3C96(xx_3C96,2) = Core_options.CoresFit2use_Ecore_AfterCompatibility(m_3C96,1,n_3C96);
            xx_3C96 = xx_3C96 + 1;
        end
    end
end
rrr_3C96=num2str(legend_3C96(:,1)*10^6);
qqq_3C96=num2str(legend_3C96(:,2));
legend(strcat(rrr_3C96,32,qqq_3C96),'fontsize',11)
xlabel("Frequency [kHz]")
ylabel("Total converter loss [W]")
title('3C96 material: Total converter loss vs. Frequency')

%% Plot for Total_Converterloss vs. Frequency
figure(8)
mn=min(min(min(Total_Converterloss_With3C96)));
pj=find(abs(Total_Converterloss_With3C96-mn)<1e-6);
[xx1 ,yy1, zz1] = ind2sub(size(Total_Converterloss_With3C96(:,:,:)),pj);
l1=strcat(rrr_3C96,32,qqq_3C96);
l1_3C96=l1(xx1,:);

mn_3C94=min(min(min(Total_Converterloss_With3C94)));
pj_3C94=find(abs(Total_Converterloss_With3C94-mn_3C94)<1e-6);
[xx1_3C94 ,yy1_3C94, zz1_3C94] = ind2sub(size(Total_Converterloss_With3C94(:,:,:)),pj_3C94);
l2=strcat(rrr_3C94,32,qqq_3C94);
l2_3C94=l2(xx1_3C94,:);

mn_3C92=min(min(min(Total_Converterloss_With3C92)));
pj_3C92=find(abs(Total_Converterloss_With3C92-mn_3C92)<1e-6);
[xx1_3C92 ,yy1_3C92, zz1_3C92] = ind2sub(size(Total_Converterloss_With3C92(:,:,:)),pj_3C92);
l3=strcat(rrr_3C92,32,qqq_3C92);
l3_3C92=l3(xx1_3C92,:);


mn_3C90=min(min(min(Total_Converterloss_With3C90)));
pj_3C90=find(abs(Total_Converterloss_With3C90-mn_3C90)<1e-6);
[xx1_3C90 ,yy1_3C90, zz1_3C90] = ind2sub(size(Total_Converterloss_With3C90(:,:,:)),pj_3C90);
l4=strcat(rrr_3C90,32,qqq_3C90);
l4_3C90=l4(xx1_3C90,:);

plot(f(n_3C96,:)/1000, max(Total_Converterloss_With3C96(:,:,zz1))*10^-3,'DisplayName',strcat(l1_3C96,32,'3C96'))
hold on
plot(f(n_3C94,:)/1000, max(Total_Converterloss_With3C94(:,:,zz1_3C94))*10^-3,'DisplayName',strcat(l2_3C94,32,'3C94'))
plot(f(n_3C92,:)/1000, max(Total_Converterloss_With3C92(:,:,zz1_3C92))*10^-3,'DisplayName',strcat(l3_3C92,32,'3C92'))
plot(f(n_3C90,:)/1000, max(Total_Converterloss_With3C90(:,:,zz1_3C90))*10^-3,'DisplayName',strcat(l4_3C90,32,'3C90'))
hold off
legend()
xlabel("Frequency [kHz]")
ylabel("Total converter loss [W]")
title('Material total converter loss comparison vs. Frequency')

%% Plot of Total converter loss vs. load current & T+DelT1 vs load current for L=800uH, core material: 9928
figure(9)
plot(Iout, Total_Converterloss_With3C90(:,:,end)*10^-3);
xlabel("Load current [A]")
ylabel("Total converter loss 3C90 [W]")
title('Plot of Total converter loss vs. load current for material: 3C90')

figure(10)
plot(Iout, (max(delT_3C90(:,:,end))+25) );
xlabel("Load current [A]")
ylabel("Temperature+delT1 [degree C]")
title('Plot of Temperature+delT vs. Load current for material: 3C90')

figure(11)
plot(Iout, Total_Converterloss_With3C92(:,:,end)*10^-3);
xlabel("Load current [A]")
ylabel("Total converter loss 3C92 [W]")
title('Plot of Total converter loss vs. load current for material: 3C92')

figure(12)
plot(Iout, (max(delT_3C92(:,:,end))+25) );
xlabel("Load current [A]")
ylabel("Temperature+delT1 [degree C]")
title('Plot of Temperature+delT vs. Load current for material: 3C92')

figure(13)
plot(Iout, Total_Converterloss_With3C94(:,:,end)*10^-3);
xlabel("Load current [A]")
ylabel("Total converter loss 3C94 [W]")
title('Plot of Total converter loss vs. load current for material: 3C94')
```

```
515
516 figure(14)
517 plot(Iout, (max(delT_3C94(:,:,end))+25) );
518 xlabel("Load current [A]")
519 ylabel("Temperature+delT1 [degree C]")
520 title('Plot of Temperature+delT vs. Load current for material: 3C94')
521
522 figure(15)
523 plot(Iout, Total_Converterloss_With3C96(:,:,end)*10^-3);
524 xlabel("Load current [A]")
525 ylabel("Total converter loss 3C96 [W]")
526 title('Plot of Total converter loss vs. load current for material: 3C96')
527
528 figure(16)
529 plot(Iout, (max(delT_3C96(:,:,end))+25) );
530 xlabel("Load current [A]")
531 ylabel("Temperature+delT1 [degree C]")
532 title('Plot of Temperature+delT vs. Load current for material: 3C96')
```

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