A High-speed Amplifier And Loop Filter Architecture For A GHz Sampling Sigma-Delta ADC

by

Xin.Zhan

Supervisors:
Dr.Muhammed Bolatkale,NXP Semiconductor
Dr.Fabio Sebastiano,TU Delft
Pierluigi Cenci,TU Delft

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Abstract

This thesis presents the design and implementation of a low power 3^{rd}-order loop filter and a low power, compact, high-speed inverter-based amplifier designed in 28nm HPC for a GHz sampling $\Sigma\Delta$ modulator.

In the earlier design, the size of the pMOS in an inverter was found to be nine times larger than the nMOS which is not practical to obtain a compact design.

The proposed 4by4 inverter structure in a kind of matrix form achieves a gain of minimum 25dB and maximum 28dB at the worst corner and best corner without loading resistor respectively. The designed inverter amplifier is found to be relatively tolerant over PVT without an LDO. The simulation of the modulator system is implemented with an ideal quantizer and resistive DAC. The simulation results of the modulator shown an ENOB of 10bits with 0.41mW power consumption in the worst case and an ENOB of 10.7bits with 0.53mW power consumption in the best case.

Preface

It has been a wonderful experience for the past two years I have spent in Delft and Eindhoven. Few words in the acknowledgements cannot fully express my gratitude to the people who taught me, guided me and supported me.

Firstly, I would like to thank Dr.Muhammed Bolatkale for giving me an opportunity to work on my thesis at NXP and for his detailed supervision through the internship and thesis period. Without him, the internship would not have been possible. It was really a pleasure and honour to work as his student.

I would like to thank my daily supervisor, Pierluigi Cenci for guiding me and teaching me for the very detailed technical problems. In spite of his busy and stressful work, he has been always patient and enthusiastic for discussions. Those discussions have greatly helped me to understand the theory, figure out the implementation issues and improve my thesis.

I would also like to express my special thanks to Prof.Lucien Breems and Dr.Fabio Sebastiano. They have helped me during all the phases of my thesis. Their valuable feedbacks during the weekly meeting make me always on the right track and move forward.

Finally, I would like to thank all of my friends in China and the Netherlands for all the encouragement and support. I will cherish them for the rest of my life.

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Chapter 1

Introduction

This thesis work includes the theory, system-level design and implementation of the loop filter of a 3^{rd}-order $\Sigma\Delta$ modulator for Bluetooth application. The focus of this work is on designing a modulator with 70dB dynamic range while consuming only 1mW power. This introduction will also present the relative application of this work, the motivation of this design as well as the system specifications. The organization of this thesis is presented at the end of this chapter.

1.1 Bluetooth

The well known short distance communication standard Bluetooth was firstly introduced by telecom vendor Ericsson in 1994 [1]. It is designed for connecting separated devices and realizing short distance data exchange. Bluetooth operates at frequencies between 2402 and 2480MHz and it is based on the principle of a radio technology named frequency-hopping spread spectrum (FHSS) as is shown in Figure 1.1. By using FHSS, the signal is spread into sections of sub-frequencies bands. Each frequency band has a bandwidth of 1MHz. The signal hops among frequencies based on the predetermined order and the combination of the frequencies achieve the effective wide bandwidth of 80MHz. Therefore, the system benefits from FHSS as it eliminates severe signal degradation from narrow-band interference.

A corporation called Bluetooth Special Interest Group (SIG) is responsible for developing Bluetooth standard and licensing it to producers. It was formally established in 1988 and has witnessed the evolution of Bluetooth since then. The next generation Bluetooth standard or Bluetooth 5 was unveiled on June.2016 and it has threefold benefits concerning range, speed, and bandwidth. It offers the twice the speed or bandwidth for BLE (Bluetooth Low Energy), while expanding the range over four times of the predecessor and the data broadcasting capacity has been increased by 800% [2]. Instead of diving the band into packets with each assigned 1MHz, now the band is merely halved so each channel has a bandwidth of 40MHz. However, the increase of bandwidth burdens the design of blocks in Bluetooth receiver. For instance in Bluetooth 5, the receiver converts low bandwidth state information and the frequency hopping is in the digital domain, so the mixer is always at the same frequency.

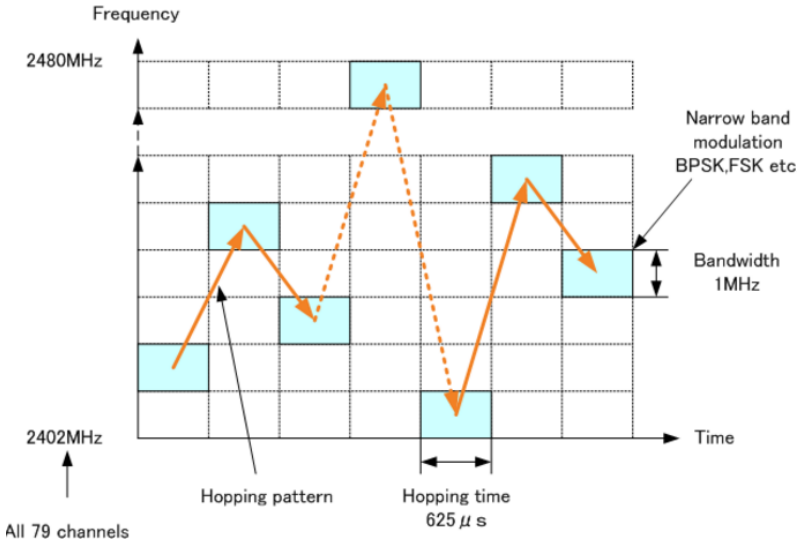

Figure 1.1: Frequency Hopping Spread Spectrum Scheme

1.2 ADCs for Bluetooth Receiver

A receiver structure for Bluetooth application is shown in Figure 1.2. The information signal is firstly collected by an antenna and then it is processed by a low noise amplifier (LNA) and a mixer to help filter out the unwanted signal and convert it from high frequency to baseband. It is essential to convert the received analog signal to digital signal concerning the ease of processing in the digital domain and this is achieved by an analog-to-digital converter (ADC).

Shifting the ADC closer to the RF front end indicates more digital integration in the baseband processors. This is attractive since more external analog circuitry can be now implemented on the chip digitally. It is well known that the digital circuitry is more power efficient than its analog counterpart. However, this comes with the expense of more burden on the design of ADC since it has to process noisy, large bandwidth signals. In modern communication systems such as Bluetooth, the bandwidth of the input signal could go over MHz. The demanding market of battery-powered portable devices and development of telecommunication drives the design of wireless communication system. A portable device is always required to have a receiver to communicate with the outside world. Therefore, the ADC is often required to have high dynamic range, wide bandwidth with low power consumption.

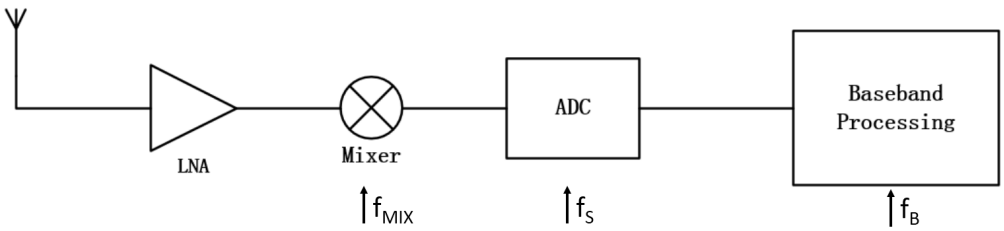

Figure 1.2: A Bluetooth Receiver Structure

Murmann's Figure 1.3 has summarized the ADCs been published for the past two decades. Both CT ΣΔ and SAR ADCs are capable of achieving an SNR of 70dB in 10-40 MHz bandwidths with low power. Compared to its counterpart such as SAR ADCs, CT ΣΔ modulators take advant-

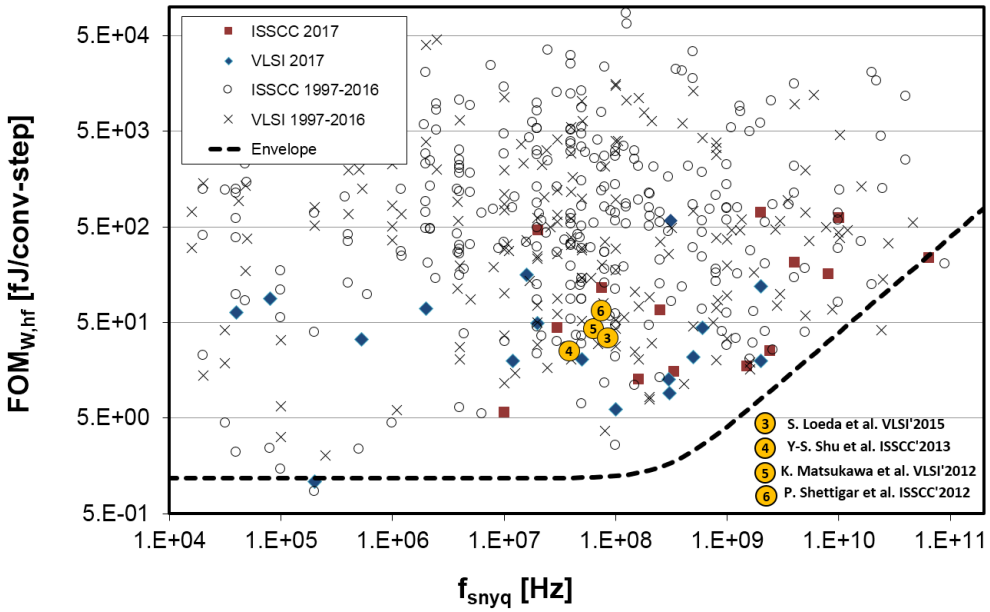

Figure 1.3: ADC Performance Survey 1997-2017

age of relaxed anti-aliasing input filtering requirements with power-hungry sampling-input driving load [3]. The theory of the ΣΔ modulator will be explained in the next chapter. The combination of noise shaping and oversampling permit the inherent anti-aliasing filtering as well as a high dynamic range of the ΣΔ ADC. However, CT ΣΔ modulators are more sensitive to clock jitter, excess loop delay (ELD) and make the design of high resolution, high dynamic range with low power challenging.

Hence the design implemented in SAR ADCs are firstly filtered out shown in Figure 1.4. The requirement of an SNDR over 68dB together with the targeting bandwidth 40MHz help us further limit our options and priority will be given to those achieving lower FoM. Eventually, four among them have been selected as a reference for our design shown in Table 1.1 and marked in Figure 1.3 and Figure 1.4.

$$FOM = \frac{Power}{2^{ENOB} \cdot 2BW} \tag{1.1}$$

The figure of merit of a modulator can be calculated regarding power, bandwidth, effective number of bits (ENOB) and expressed as is shown in Eq.(1.1). Paper [4] has achieved the most efficient CT ΣΔ modulators by far with a FOM of 28fJ/conv-step. It is utilizing the principle of tracking quantizer and the quantizer only accounts for less than 10% of the total power consumption. However, the larger out of band signal transfer function (STF) peak could degrade the performance of the system.

The majority of the modulators with wide bandwidths have used multi-bit quantizers [7][8][9][5]. With a multibit quantizer, it is possible to achieve a comparable SQNR with smaller OSR which indicates less power consumption as the sampling frequency is lower, however, note that the reduction of the sampling frequency is not proportional to the increase of quantizer levels. It is therefore attractive to instead reduce the quantizer levels while compensating the loss of SQNR by increasing the sampling frequency.

A single bit design takes advantages of simple implementation, lower power consumption from

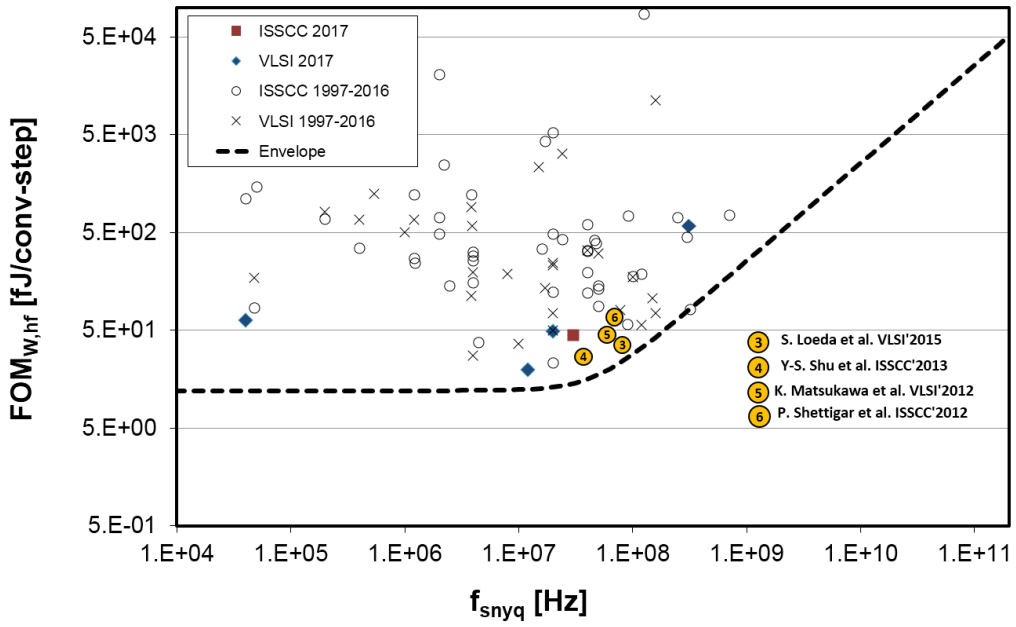

Figure 1.4: ADC Performance Survey 1997-2017 (CT ΣΔ modulators only)

Specs	[4]	[3]	[5]	[6]
Process	28nm	40nm	55nm	90nm
Power	3.9mW	5.25mW	13mW	15mW
SNDR	73.6dB	66.9dB	75.1dB	70.9dB
Bandwidth	18MHz	40MHz	30MHz	36MHz
Sampling frequency	0.64GHz	2.4GHz	0.83GHz	3.6GHz
FoM(fJ/conv)	27.6	36.3	46.6	72.7

Table 1.1: State-of-the-art Sigma-Delta Modulator

quantizer and a linear feedback DAC. However, a crucial concern existed in a wideband single-bit modulator is the data-dependent jitter resulted from comparator metastability [10]. It is therefore attractive to combine the features of a single-bit and multi-bit design, for instance, by designing a single-bit modulator with FIR DAC as the feedback block [3]. However, since the data jitter has not been considered as a major issue in our design, the design with FIR DAC will not be considered.

1.3 Motivation

The content of this project is to design a high-speed amplifier and a loop filter architecture for a GHz sampling CT ΣΔ ADC.

The main motivation of this project is the requirement of high performance, low power ADC for the application of Bluetooth receivers. For an ADC with high dynamic range and broad bandwidth, it enables a higher degree of digital integration. The increase of digital integration could help reduce costs, device size, and power. Therefore, the ADC is designed with a focus on targeting high dynamic range of up to 70dB and exploring the lowest power consumption at around 1 mW.

Previous research has done a lot of work on reducing power consumption from the comparator, for instance, by utilizing the concept of tracking quantizer or by benefiting the essence of a combination of single bit and multi-bit operation such as FIR DAC [11]. It would be attractive to explore the loop filter further, therefore, a 3^{rd}-order loop filter with an integrator and a single-opamp resonator has been studied in this work.

In modern broadband wireless communication systems, the battery-powered system make the low power design extremely essential. As well known the bottleneck of reducing the power consumption of a modulator is the number of opamps. In practice, the opamps are with limited GBW which could lead to excess loop delay for chains of opamps. To enhance the GBW also consume extra power. Therefore, it is attractive to study the loop filter structures with fewer opamps and check if the reduction of power would come with any trade-offs regarding the performance of the modulator. Similarly, for the power concern, inverter-based implementation of OTAs is tempting for low-power amplifier design. However, in nano-meter technology, inverter-based amplifiers are always with high sensitivity to process corners and temperature variations [12]. Hence, it is of necessities to design a process-tolerant OTA to avoid any degrading of system performance over process corners.

It is essential to announce that this project is attached to the project of a Ph.D. candidate Pierluigi Cenci and with a focus only on the design of the loop filter. The whole system simulation is based on the implementation of loop filter but the rest of the system are ideal blocks. Based on the previous research, the specification for the CTΣΔ ADC has been proposed in Table 1.2. The derivation of specifications for the sub-blocks is presented in Chapter 2.

1.4 Specifications of ADC

The specifications of the system are listed in Table 1.2.

The FOM of the proposed ADC is calculated as 8.5fJ/conv-step based on Eq.(1.1) and plotted on the ADC survey shown in Figure 1.5.

Specifications	Value
ENOB	10.8bits
SNDR	66.7dB
HD3	68dB
Bandwidth	40MHz
Power	< 1mW
Sampling frequency	2.4GHz
Supply voltage	0.9V
Process	28nm HPC
FOM	8.5fJ/conv

Table 1.2: Specifications of the Modulator System

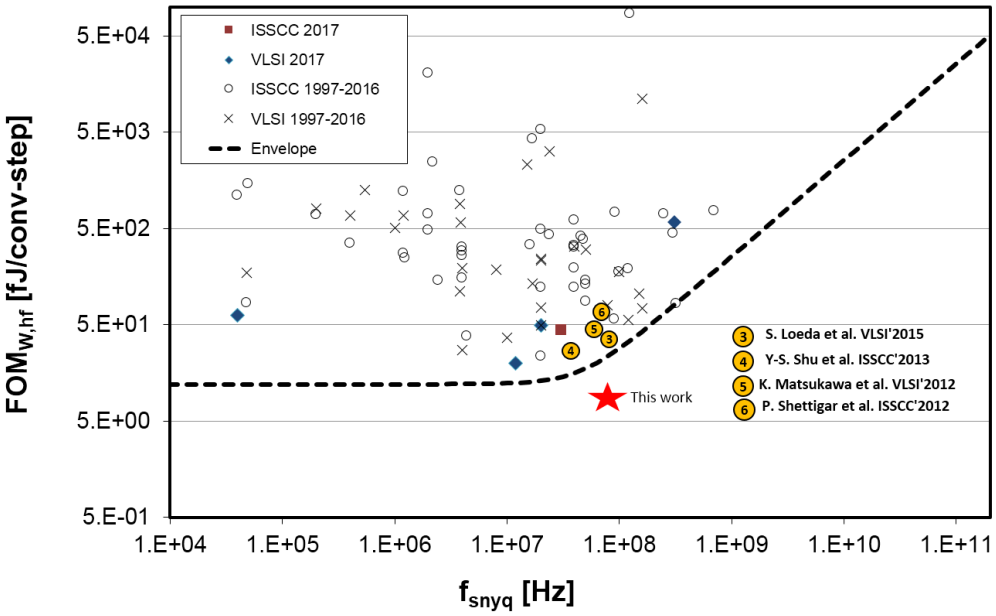

Figure 1.5: ADC Performance Survey 1997-2017 Including the Target

1.5 Organization of the Thesis

The organization of this thesis will be as follows: Chapter 2 will introduce the theory of $\Sigma\Delta$ modulation then it will explain the designing of a higher-order loop filter. In Chapter 3, the system level design is treated. It will start by presenting two 3^{rd}-order filter structures and the frequency compensation scheme. Then the factors determining modulator performance such as thermal noise, quantization noise, harmonic distortion, and power will be modeled. Besides, non-idealities such as excess loop delay, finite GBW introduced from real implementation will be considered and analyzed. The focus of Chapter 4 is on describing the implementation of a 3^{rd}-order CT $\Sigma\Delta$ modulator with focus on the loop filter and amplifiers design. The aim of this work is to minimize power consumption hence inverter based amplifiers will be studied in details as opamps are always the bottleneck in reducing power consumption of the modulator. To verify the system performance, system simulations are also performed with the help of ideal quantizer and resistive DAC. In the last chapter, the main conclusions will be shown. The performance of the system will be described and compared to the specifications requirement.

Chapter 2

Fundamentals of Sigma-Delta Modulation

There are generally two main branches of analog-to-digital converters: Nyquist-rate converters and Oversampling converters [13]. The Nyquist ADC is often suitable for systems targeting large bandwidth since the sampling frequency is at a rate at least twice the highest sine-wave Fourier signal frequency (Nyquist frequency), while oversampling data converters could sample up to few times of Nyquist frequency.

The chapter will begin with describing the Nyquist theorem. The resolution of the data converter could be improved by increasing sampling frequency hence the oversampling scheme is developed. To further enhance resolution, in-band quantization noise can be alleviated by removing it to a high frequency where the band is out of interest and that is called noise shaping. $\Sigma\Delta$ modulation combines the benefits of oversampling and noise shaping and generates $\Sigma\Delta$ modulators.
The order of the noise-shaping mechanism is dependent on the order of the loop filter, certain compensation techniques have to be treated for ensuring the stability of the system.

2.1 Basics of Analog To Digital Conversion

2.1.1 Sampling

The common technique to transform a continuous-time analog signal to a discrete-time digital signal is by sampling and quantization. It is well known that the digital signals are robust to noise and interference, and it is highly efficient to process signals in the digital domain since the power can be optimized with digital scaling.

The sampling process defines the value of a signal on a predetermined frame-of-time moment. There exists a time frame T_s between each sampling moment and the sampling frequency can be determined as,

$$f_s = \frac{1}{T_s} \tag{2.1}$$

A sampling process with a f_s of 20MHz is shown in Figure 2.1. It is demonstrated that with a signal of 1MHz, the sampled discrete signal could almost construct its analog form. Once the input signal has been raised to a certain extent, the sampled frequency is too slow to follow the signal.

To mathematically describe the sampling process, the Dirac function has to be applied. The Dirac

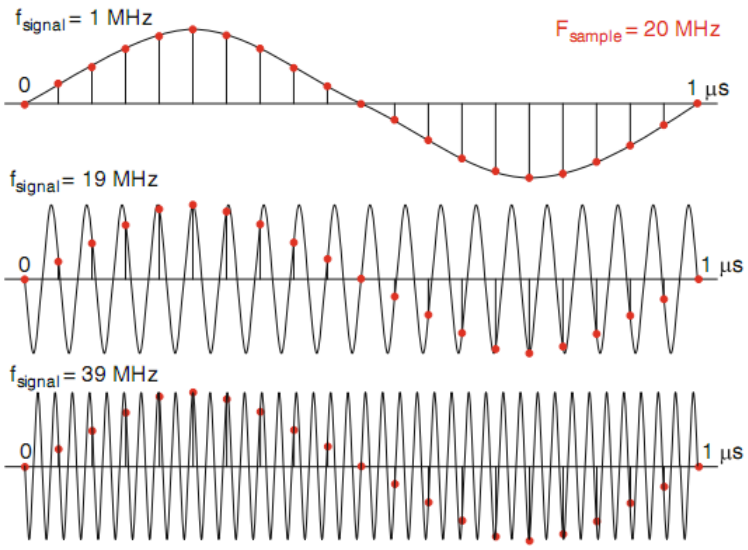

Figure 2.1: Sampling Three Time-continuous Signals: 1MHz, 19MHz, and 39MHz Sine Waves Result After Sampling with 20Ms/s in the Same Sampled Data Sequence

function has a constraint that the function has to be used under the integral form. Therefore, the result of the integral is

$$\int_{t=-\infty}^{\infty} f(t)\delta(t-t_0)dt = f(t_0) \tag{2.2}$$

A train of impulses have Fourier transform, the sampling of a continuous-time signal in the time signal is effectively a convolution process in the frequency domain. The convolution process would results in replicas of the spectrum by integer multiples of f_s. It is of importance to consider the existence of aliasing when the bandwidth of the signal increases. As is presented in Figure 2.2, with the increase of the signal bandwidth, the bandwidth of mirrored replicas will follow. The expanding of bandwidth could eventually lead to an overlap of the signal after sampling and this phenomenon is called aliasing. This phenomenon is clearly unwanted as the information contained in the signal is mixed. Therefore, a condition must be retained during sampling which is called Nyquist theorem 2.3, the bandwidth of the signal is limited up to half of the sampling frequency.

$$f_b \leq \frac{f_s}{2} \tag{2.3}$$

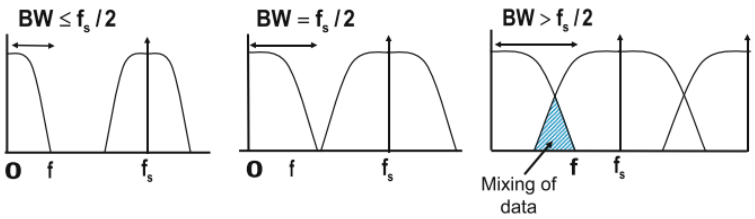

Figure 2.2: The Explanation of the Nyquist Theorem

The sampling rate achieving Nyquist theorem is called Nyquist frequency and this condition is often enforced by applying a so-called anti-aliasing filter preceding the sampling process.

2.1.2 Quantization

The main operation after sampling is quantization. The quantization process takes each sampled analog signal and round it to a set of discrete values. The digital representation of the original analog signal is always in binary formats, where the bits take two values (0,1). The quantization operation is realized by comparing the signal to a set of reference values; the quantized value is rounded to the nearest level. There are some parameters associated with the quantization process shown in Figure 2.3, the term LSB stands for the least significant bit and this value defines the smallest step between each quantization level. Accordingly, the most significant bit determines the highest term of a digitized signal. The total number of bits N used to represent signal is limited by the resolution of the quantization circuit. Therefore, the analog signal is now mapped to a digitized signal with 2^N discrete levels and the converter is considered to have B bits of resolution. The output range is defined as full scale, the term LSB can be expressed as [14],

$$A_{LSB} = \frac{FullScale}{2^B - 1} \tag{2.4}$$

The transition from analog to digital form is inevitably impaired with some errors and this so-called quantization error is a key in judging the quality of a modulator system. The quantization error is also known as quantization noise. The error is nonlinear so certain approximation should be applied to model it and obtain its power. A linearized model of quantization error is developed in Figure 2.4. The assumption that the quantization noise is white can derive:

- The probability density function of the error signal is assumed to distribute uniformly between -0.5 and +0.5 LSB
- The power spectral density of the error signal is flat in the band of interest
- The quantization error is random
- The quantization error is uncorrelated with the input signal

With the help of the above assumptions, the random quantization error has become linear quantization noise. Therefore, the quantization power can be expressed as in Eq.(2.5), where A_{LSB}, A_{error} refer to the magnitude of the signal.

$$Q^2 = \frac{1}{A_{LSB}} \int_{\varepsilon=-0.5A_{LSB}}^{\varepsilon=0.5A_{LSB}} A_{error}^2(\varepsilon) d\varepsilon = \frac{A_{LSB}^2}{12} \tag{2.5}$$

Hence the quantization noise power is equal to $\frac{A_{LSB}^2}{12}$ under the case of a uniform distribution over $\pm 0.5 A_{LSB}$. The signal-to-noise ratio (SNR) of a converter can be defined as:

$$SNR = 10 \cdot log_{10} \left(\frac{P_{sig}}{P_{noise}} \right) \tag{2.6}$$

or in voltage domain,

$$SNR = 20^{10} log\left(\frac{V_{signal\ rms}}{V_{noise\ rms}}\right) \tag{2.7}$$

Note the above definition only consider the quantization noise as the only source of the noise. In fact, there are other error sources such as thermal noise, distortion, and it is often to describe the behavior considering whole noise sources by,

$$SINAD = \frac{Power\ of\ first\ harmonic}{Power\ of\ all\ unwanted\ components} \tag{2.8}$$

It is also often in a ADC system to express SNR in terms of effective number of bits (ENOB),

$$ENOB = \frac{SNDR - 1.76dB}{6.02} \tag{2.9}$$

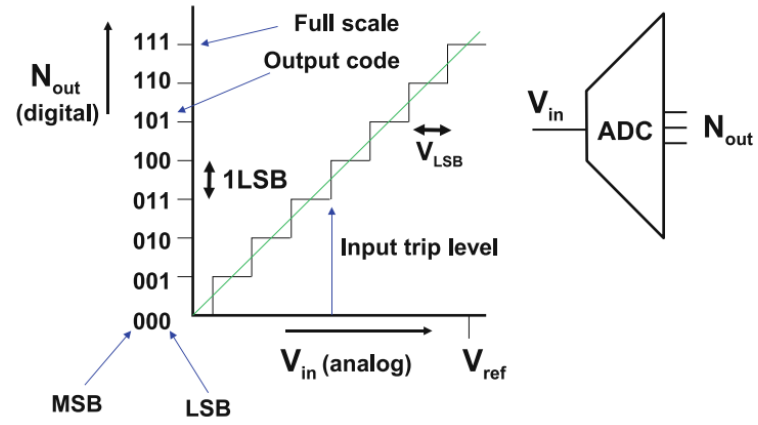

Figure 2.3: Parameters Associated with Quantization Process

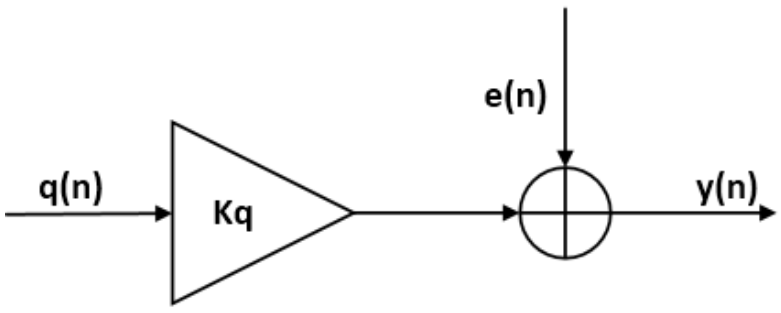

Figure 2.4: Linearized Quantizer Model

In addition to quantization errors, real ADC implementation can introduce other imperfections such as integral linearity (INL), differential linearity (DNL), offset and gain errors. INL indicates the maximum deviation of the conversion from the ideal function and it could be expressed as,

$$INL = \frac{A(i) - i \cdot A_{LSB}}{A_{LSB}} \tag{2.10}$$

While DNL determines the deviation of each conversion step from the ideal step 1 LSB and is defined as,

$$DNL = \frac{A(i+1) - A(i)}{A_{LSB}} - 1 \tag{2.11}$$

Note that the harmonic distortion is correlated with INL, as the obtained transfer curve is shaped by the effects of INL and the magnitude of the specified harmonic components are determined by INL.

2.1.3 Performance Parameters

Apart from the quantization noise associated SNR mentioned in the previous section, there are more terms to be defined for an ADC system. These parameters such as thermal noise, flicker noise, harmonic distortion, and jitter can be used to judge the performance of the system.

Thermal noise It is well known that the flow of electrons generates noise [15]. Among them, thermal noise has been considered as the most common one which is due to the Brownian motion of charge carriers in a conductor. Usually, thermal noise could be modeled by a voltage source in series to the resistive component or a current source in parallel. When quantifying the effects of thermal noise on a system it is often to refer the noise to the input, that is, the noise contribution from following stages will be shaped by the gain of the preceding stage.

Flicker noise Flicker noise or 1/f noise. It is commonly recognized as a result of charge trapping process. A corner frequency is often defined for flicker noise and it determines the region where flicker noise dominates. And a knee frequency defines where the thermal noise takes control. It is a noise originated from Bipolar, carbon resistors and MOSFETs device. Note that the noise is described by power and it depends on gate-area (1/WL) of a MOSFET.

Harmonic distortion The introduction of the non-linear device could generate harmonic distortion. The deviation from the ideal response is described by harmonic coefficients. If the modulator is assumed to be implemented differential, there will be no even order harmonics and the 3rd harmonic is often assumed to be dominant.

Jitter Jitter is defined as the random variation in the timing of the clock transitions concerning the ideal clock signal. In CT $\Sigma\Delta$ modulators, clock jitter affects feedback DAC pulses and the jittered DAC pulse is summed with input plus quantization noise, leading to increasing noise consequently.

2.2 Theory of Sigma-Delta Modulation

2.2.1 Oversampling

Figure 2.5 presents a basic model of a single loop $\Sigma\Delta$ modulator. The modulator is composed of a loop filter which is generally an accumulator or integrator. The output of the loop filter is then

sampled and quantized by an A/D converter. The quantized signal is converted back to an analog signal by a D/A converter and subtracted from the analog input.

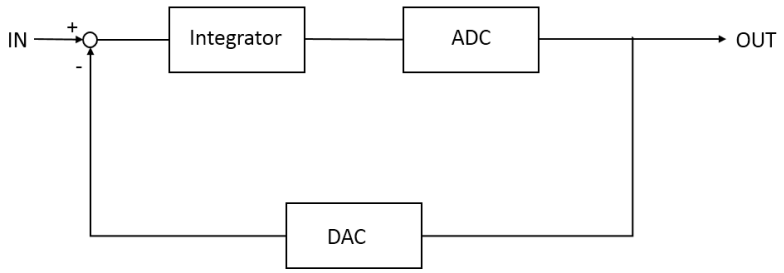

Figure 2.5: Modeling of a Single Loop ΣΔ Modulator

In data converters, an error signal E could be generated during the sampling and quantization process and this error signal has a fixed amount of power [16],

$$E^2 = \frac{V_{LSB}^2}{12} \tag{2.12}$$

The noise power is modeled as white and its power spectral density is evenly distributed between 0 and $\pm f_s/2$. The power spectral density of the error signal is shown in Eq.(2.13), where f_s is the sampling frequency.

$$E(f) = \frac{V_{LSB}^2}{6f_s} \tag{2.13}$$

Based on Eq.(2.13) shown above, one can obtain the relationship between quantization noise power and sampling frequency. If the sampling frequency of the system is improved from where the Nyquist criterion can be satisfied to a new sampling rate f_s the noise spectral density is reduced. Figure 2.6 shows the reduction of noise power density with rising f_s and this depicts the idea of oversampling.
We can now define a ratio between sampling frequency (f_s) and Nyquist bandwidth (f_b) as an oversampling ratio,

$$OSR = \frac{f_s}{2f_b} \tag{2.14}$$

Recall that the total noise power in a Nyquist converter is $\frac{V_{LSB}^2}{12}$ and the noise spectral density is $\frac{V_{LSB}^2}{6f_s}$ if the noise source is assumed to be evenly distributed between 0 and $\pm f_s/2$. Hence the total in-band noise power can be found by integrating the noise power density from o to f_b, the total noise power in a fixed bandwidth is inversely proportional to the increase of sampling rate.

$$Q^2 = \frac{V_{LSB}^2 f_b}{6f_s} = \frac{V_{LSB}^2}{12} * \frac{1}{OSR} \tag{2.15}$$

Thus in oversampling converter the SNR is increased to:

$$SNR = 6.02N + 1.76 + 10logOSR \tag{2.16}$$

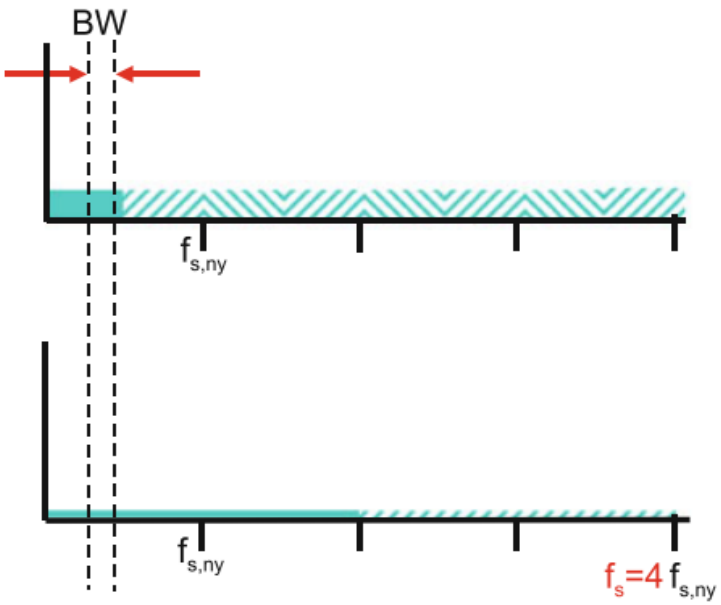

Figure 2.6: Oversampling Scheme(From Marcel.P)

Where the additional term comes from the oversampling ratio. The resolution can be improved by 6dB or 1bit for every quadrupling of the oversampling ratio. The improvement does not look profitable since the increase the sampling frequency comes with the expense of a loss in conversion speed or extra power consumption. The other way to enhance the resolution is to make the bandwidth of the signal less than the sampling frequency to increase OSR, that is, trade bandwidth for precision.

The above two methods neither looks effective. Nonetheless, a combination of oversampling and noise shaping mechanism can combine the benefits of both. Oversampling is helpful considering the extra frequency range it has created between the band of interest and the alias band, relaxing the design of anti-aliasing filter. Then the extra frequency range can be used by noise-shaping to remove the unwanted signal to the band out of interests.

2.2.2 Noise-Shaping

As has been mentioned above, the oversampling mechanism is not profitable on it own but the extra frequency range it has created is useful and can be utilized by noise shaping to shift the quantization noise out of the band of interests.

The idea as its name indicates is to shape the noise to certain frequencies where it can be filtered out. A basic structure of the noise shaper circuit is shown in Figure 2.7. The quantization error is extracted by subtracting the input and output of the quantizer; then the error is fed to filter and summed up with the input signal. To achieve the effects of noise shaping, the error signal is delayed and reversed by the transfer function of loop filter. The quantization error at low frequency is therefore heavily suppressed with its majority been shaped to high frequency.

The transfer function of the noise shaper model can be derived in z-domain, the filter function $J(z)$ is chosen to be a unit delay z^{-1} [16].

$$Y(z) = X(z) + [1 - J(z)]N_Q(z) \tag{2.17}$$

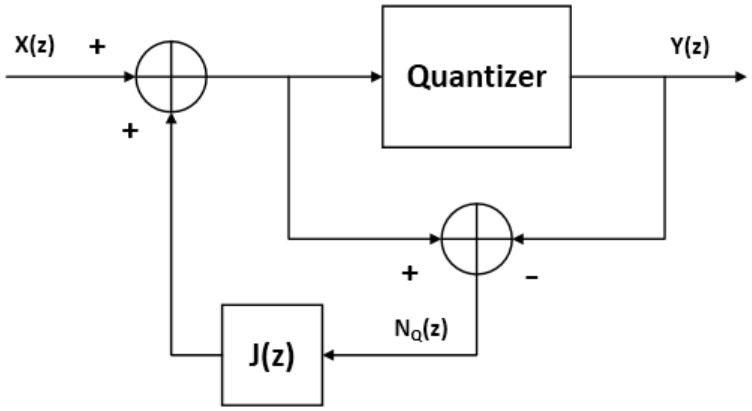

Figure 2.7: A Structure of the Noise Shaper Circuit

By applying Laplace transform ($z \leftrightarrow e^{jwT}$), $J(w) = e^{-jwT}$. The transfer function can be rewritten in frequency domain,

$$Y(w) = X(w) + [1 - e^{-jwT}]N_Q(w) \tag{2.18}$$

Therefore the NTF can be determined,

$$|NTF(w)|^2 = \left|\frac{Y(w)}{N_Q(w)}\right|^2 = \left|1 - e^{-jwT}\right|^2 = 2 - 2cos(wT) \tag{2.19}$$

Now the quantization noise is shaped with the NTF $2 - 2cos(wT)$ which is intuitively shown in Figure 2.8. The total noise power can be obtained by integrating original the noise power density $\frac{V_{LSB}^2}{6f_s}$ times the noise shaping function $2 - 2cos(wT)$ over the band from 0 to $f_s/2$.

$$\int_0^{f_s/2} \frac{V_{LSB}^2}{6f_s} \left(2 - 2cos(2\pi f/f_s)\right) df = \frac{V_{LSB}^2}{6f_s} \tag{2.20}$$

Note the quantization noise power has been doubled with noise shaping. This can be explained by the structure of the noise shaper circuit shown in Figure 2.7. The quantization error is delayed and summed up with the input and presented at the output. Therefore, the output is inherently a combination of the present and delayed quantization error and the total quantization noise power doubles.
The shaped noise power density

$$\frac{V_{LSB}^2}{6f_s} \left(2 - 2cos(2\pi f/f_s)\right)$$

can be approximated as

$$\frac{V_{LSB}^2}{6f_s} \left(\frac{2\pi f}{f_s}\right)^2$$

with cosine approximation $cos(x) \approx 1 - x^2/2$. It can be noted the noise power density is greatly compressed while at $f_s/2$ the noise power density is four times the Nyquist power density. Hence it can be concluded the noise shaping does not cancel noise but remove it to a frequency out

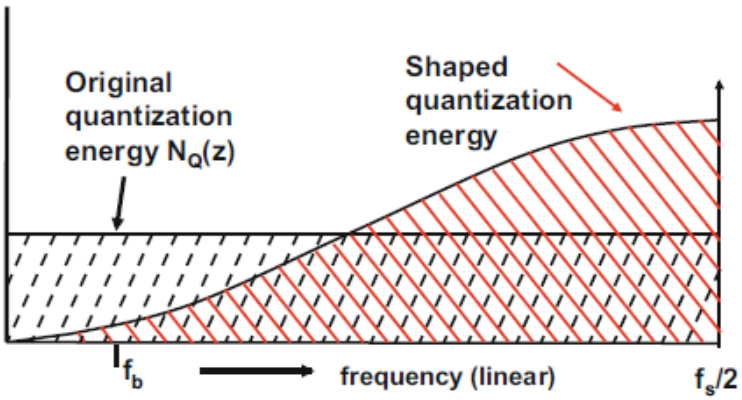

Figure 2.8: Quantization Power Distribution Before and After Noise Shaping (from Marcel.P)

of interests. The function $2\pi f/f_s$ corresponds to a 1^{st}-order frequency response, and the noise shaping can be improved with the order of the loop filter.
The total in-band noise power with noise shaper is calculated as,

$$\int_0^{f_b} \frac{V_{LSB}^2}{6f_s}\left((1-e^{-jwT})^2\right) df = \frac{V_{LSB}^2}{3}\left[\frac{f_b}{f_s} - \frac{sin(2\pi f_b/f_s)}{2\pi}\right] \tag{2.21}$$

$$\approx \frac{V_{LSB}^2}{12}\frac{\pi^2}{3}(\frac{2f_b}{f_s})^3 = \frac{V_{LSB}^2}{12}\frac{\pi^2}{3OSR^3} \tag{2.22}$$

Similarly, the maximum achievable SNR could be found as:

$$SNR = 6.02N + 1.76 - 5.17 + 30logOSR \tag{2.23}$$

Compared to the design with pure oversampling $\frac{V_{LSB}^2}{12} * \frac{1}{OSR}$, the total in-band noise power has been reduced by OSR cube. The introduced OSR^2 term originates from the noise shaping loop with one OSR term from oversampling. In this case, a doubling of the oversampling ratio can improve the resolution by 9dB or 1.5 effective number of bits. Hence noise shaping seems to be a profitable method to enhance the resolution of a converter.

2.2.3 Sigma-Delta Modulation

Note the discussion by now is still open loop, the output is expected to follow its input command and influenced by the noise signal. The output does not affect the control of the input signal. Thus it is attractive to introduce a feedback loop to close the loop and search the performance under closed-loop control.

A ΣΔ modulator is formed by a loop filter, a quantizer and a DAC in the feedback path. Since the quantizer is a non-linear component, it is necessary to model it as a linear component for the ease of analysis. A quantizer could be approximated as a linear gain together with an error signal. A possible model of a ΣΔ modulator can be developed as is shown in Figure 2.9, with the effective gain of the quantizer and the DAC modeled as c and d respectively.
In a linear model of a continuous-time ΣΔ modulator, the transfer functions of the modulator can be expressed as signal transfer function (STF) and noise transfer function (NTF).

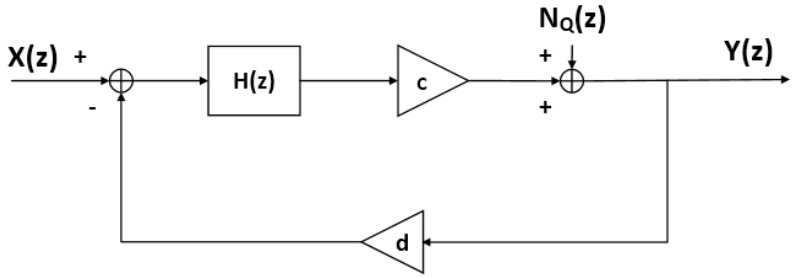

Figure 2.9: A Possible Model of a ΣΔ Modulator

An ideal design is to obliterate the noise inside the signal bandwidth, while the gain of the NTF can be high outside that band as the signal is not affected anymore. That corresponding to an ideal low-pass filter for the STF and to an ideal high-pass filter for the NTF.

$$Y(z) = \frac{cdH(z)}{1 + cdH(z)} \cdot X(z) + \frac{1}{1 + cdH(z)} \cdot N_Q(z) \tag{2.24}$$

where H(z) stands for the loop filter transfer function and E(z) indicates the errors signal introduced from quantizer. The Eq.(2.24) can be written as [14],

$$Y(z) = STF \cdot IN(z) + NTF \cdot N_Q(z) \tag{2.25}$$

$$STF = \frac{cdH(z)}{1 + cdH(z)} \tag{2.26}$$

$$NTF = \frac{1}{1 + cdH(z)} \tag{2.27}$$

The term STF describes signal transfer function while NTF is the noise transfer function. The poles of the loop filter are the zeros of NTF. It can be seen with a DC gain higher than 1, the STF approaches unity and the input signal can be well preserved. Meanwhile, NTF approaches zero which dramatically attenuates the quantization error. Therefore, design a filter with very high gain at signal band is necessary. For higher frequencies, the quantizer error starts to increase due to the reduction of gain from loop filter, but this could be removed by the post-filtering stage with negligible effect on the signal. That is, the noise function is shaped by the transfer function and this is the principle of noise shaping.
Figure 2.10 shows a model of a linearized 1^{st}-order ΣΔ modulator. The transfer function of an integrator in z-domain is $z^{-1}/(1 - z^{-1})$. With the comparator gain c assumed to be large enough and effective DAC gain unity, the STF and NTF become,

$$STF = \frac{cH(z)}{1 + cdH(z)} \approx z^{-1} \tag{2.28}$$

$$NTF = \frac{1}{1 + cdH(z)} \approx 1 - z^{-1} \tag{2.29}$$

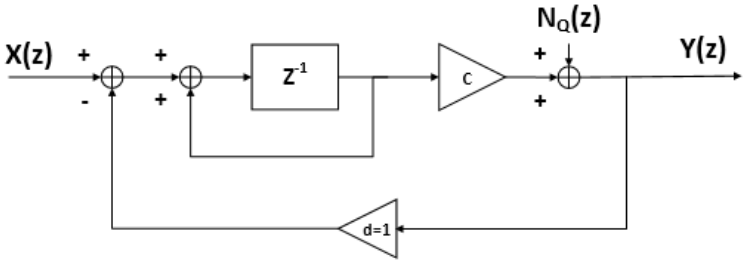

Figure 2.10: A Model of a 1^{st}-order $\Sigma\Delta$ Modulator

2.2.4 Higher-order Modulators

To reduce in-band quantization noise, several techniques could be applied. One way could be to increase the oversampling ratio. However, this way always comes with the expense of increasing power consumption as a result of faster circuits [17]. Also in modern technology where the target base-band is beyond 1GHz, the improvement of the OSR is often limited with a minimum OSR around 4.

Besides, multi-bit quantization design has been applied in $\Sigma\Delta$ modulators. The increase of quantizer resolution can help reduce quantization noise power, but the number of comparators consumes extra power.

The design with single-bit, single-loop architectures have been proved to be less susceptible to circuit non-idealities. A higher order loop filter generates more aggressive noise-shaping and obtains better signal-to-quantization noise ratio. The higher-order loop filter can be realized in the ways commonly used as: group of integrators with distributed feedback; chain of integrators with distributed feedback and feedforward; chain of integrators with weighted feedforward summation; chain of integrators with feedforward summation and local resonator feedbacks. The details of the above topologies will be treated in the following contents accordingly. The more aggressive noise shaping seems attractive but notes that the higher order NTF could result in higher out-of-band gain which could overload the quantizer and cause instability. The definition of stability is often defined as bounded outputs with bounded input signals [8]. The issue is often solved by scaling the loop gain in the system.

In order to meet the Barkhausen stability criterion at oscillation frequency or $f_s/2$ [18],

$$|G_{quantizer} \cdot H_{loopfilter}(s) \cdot H_{DAC}(s)| = 1 \tag{2.30}$$

$$\angle G_{quantizer} \cdot H_{loopfilter}(s) \cdot H_{DAC}(s) = 2\pi \tag{2.31}$$

where $G_{quantizer}$, $H_{loopfilter}$ and H_{DAC} indicates the transfer function of quantizer, loop filter and DAC, respectively. The system requires a closed loop gain of unity and total phase shift of 360^o. That is, the loop filter and DAC should contribute 90^o each while the summation part takes over the rest 180^o. However, the phase shift of loop-filter is proportional to the order of itself by $(\pi/2) \cdot N$ hence the Barkhausen criterion does not hold anymore. A certain method should be used to compensate the extra 90^o phase shift. Therefore, it is possible to implement high-order filters as long as the filter could turn back to a 1^{st}-order at around $f_s/2$ which corresponds to 90^o phase shift. A more aggressive noise shaping with stable operation at oscillation frequency can hence be realized.

The uncompensated 2^{nd}-order filter can be made stable by introducing a zero which compensates the extra phase shift from the filter. For instance, for a 2^{nd}-order loop-filter a zero could be introduced and this can be realized by adding a feed-forward path in the loop-filter.

A topology of a 2^{nd}-order modulator with feedforward summation is presented in Figure 2.11. $A1$ $A2$ are called feed-forward coefficients and the ratio of $A1/A2$ decides the zero location introduced by the feed-forward path. The value of this ratio is an overall decision from stability, SNR, and processing spread consideration. The location of the added zero is controlled by altering the ratio of coefficients A1/A2. Usually, A1,A2 with values of 2,1 are chosen [19].

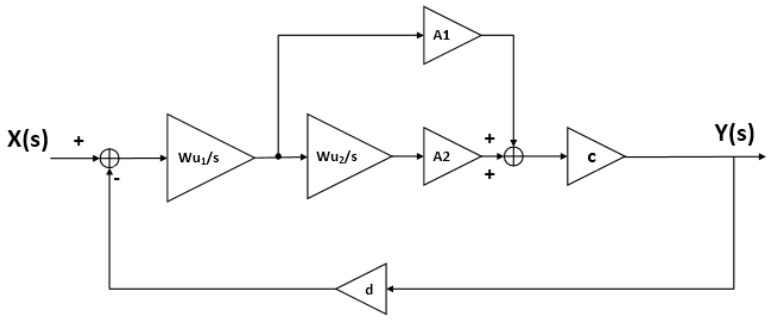

Figure 2.11: Block Diagram of Feedforward Structure

The higher-order filters can also be implemented in other ways. Figure 2.11 gives an example of the feedback structure. The Textbook [17] has proposed the technique by cascading chains of integrators in the forward path while feeding the output of the quantizer with certain weights to the input of each integrator. The coefficients c1,c2 are called feedback coefficients.

Both feedforward and feedback topology satisfy the stability requirement, but neither comes with no expenses. A significant disadvantage of the distributed feedback structure comes from the critical swing capabilities of integrators since the DAC signal tracks the input signal and the outputs of the integrators carry a significant amount of input signal. To prevent the integrators from overloading, the scaling coefficients are required to be low. Scaling down the coefficients in continuous-time modulator indicates smaller transconductance of integrators, causing more circuit noise.

However, this issue does not exist on the feed-forward topology hence relaxes the requirement on the integrator signal swing capability. However, for a feed-forward structure, the STF contains peaking due to the non-ideal compensation of poles and zeros. The peaking indicates the maximum tolerable input signal at this frequency must be scaled down by the same level as the peaking. This problem can be alleviated by adding a local feedback network, an example is shown in Figure 2.13.

Recall the noise shaping mechanism is only aggressive at very low frequencies while the quantization noise quickly increases at the edge of the signal band. If a feedback loop is added around two integrators, the gain would be spread more evenly in the signal band which could help suppress quantization noise especially at the end of the signal band. The gain notch generated by the resonator provide flat quantization noise spectrum in the signal band, but at high frequencies, the spectrum is barely shaped compared to the feed-forward case without local feedback.

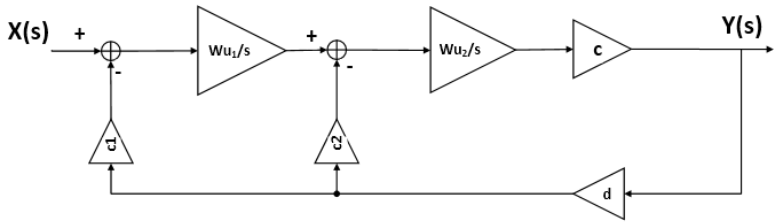

Figure 2.12: Block Diagram of Feedback Structure

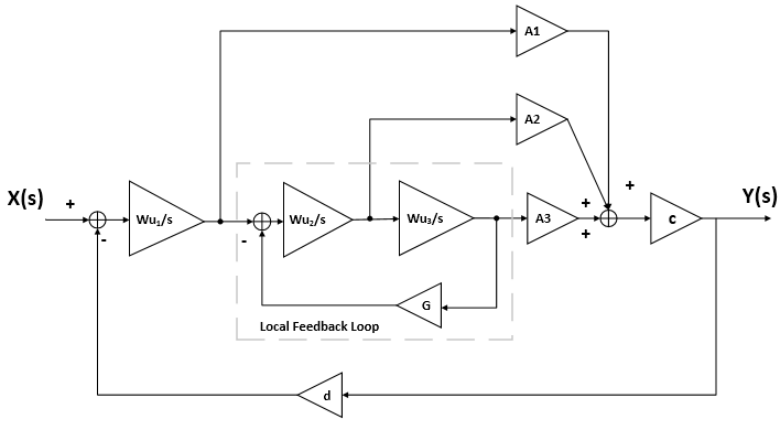

Figure 2.13: Block Diagram of Local Feedback Structure

2.3 Summary

In this chapter, the operation of an analog to digital converter is first introduced. The ADC theory started with Nyquist converter and expanded with oversampling, noise shaping mechanism for achieving a higher SQNR. A combination of oversampling and noise-shaping is found to deliver higher resolution in limited bandwidth. Then the theory continues with the modeling of a first order continuous-time $\Sigma\Delta$ converter. The possible high-order filter scheme and corresponding compensation methods are presented at the end of this chapter.

Chapter 3

Modeling of Implementation

Chapter 2 has given sufficient introduction and background for understanding a ΣΔ modulator. Based on that, a model of the designed 3^{rd}-order continuous time ΣΔ modulator with feedforward summation and local-feedback resonator will be presented and analyzed in this chapter. The topology of the modulator will be shown at the first place and a 3^{rd}-order loop filter with a single-opamp resonator and an integrator will be introduced which is more power efficient compared to the conventional design.

Then the non-idealities such as noise, the nonlinearity of amplifiers will be discussed and one can obtain the design requirements of the loop filter based on the results of the analysis. In previous sections, the ideal model of the modulator often assumes an infinite gain and bandwidth which are impractical to design, hence, it is necessary to consider the degradation of the system performance due to these issues including finite gain-bandwidth product (GBW) and technology spread. Also, the excess loop delay (ELD) which strongly affects the stability of the modulator is considered and a compensation method is introduced.

3.1 A 3^{rd}-order Continuous Time ΣΔ Modulator

3.1.1 Conventional 3^{rd}-order ΣΔ Modulator with Chains of Integrators

A typical diagram of a 3^{rd}-order feedforward CT ΣΔ ADC is illustrated in Figure 3.1. The ADC realizes a 3^{rd}-order low pass filtering with a flash ADC. The feedforward coefficients are summed passively which could save power and it is inherently linear. The flash ADC is implemented as a single bit quantizer in this design. Also, resistive DAC is employed to reduce power dissipation.

However, few issues have remained. For instance, there is still a lot of power consumed in opamps. It is well known that the number of opamps is the limiting factor in reducing total power consumption [20]. Besides, the phase shift introduced by opamps can lead to instability.

The most popular structure for realizing low power loop filter is realized by single feedback with feedforward architecture [21]. That is, the output of each integrator is fed forward and summed at the output of the loop filter. Another local feedback path is added between the output of the third integrator and the input of the second integrator. A 1^{st}-order RC integrator is placed as the first stage, a resonator is used instead of integrators at the second and the third stage.
If we express the integrator in the form of,

$$H(s) = (\frac{w_{un}}{s}), (n = 1, 2, 3...) \tag{3.1}$$

where w_{u1},w_{u2},w_{u3} are the unity gain frequency of three integrators respectively, also the output of each integrator is assigned to X1(s),X2(s),X3(s) accordingly. The position before the quantizer

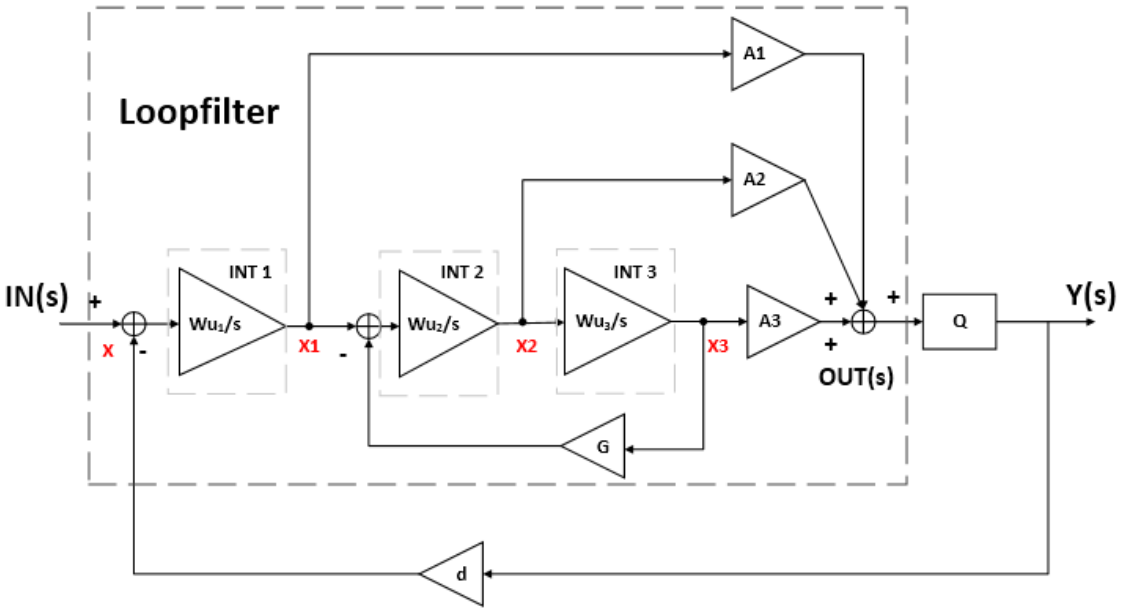

Figure 3.1: Block Diagram of a Conventional 3^{rd}-order CT Σ Δ ADC

is labeled as Out(s). Therefore, it is possible to derive the transfer function of the loop-filter based on Figure 3.1. We can obtain,

$$X1(s) = \frac{w_{u1}}{s} \cdot (IN(s) - X(s)) \tag{3.2}$$

$$X2(s) = (X1(s) - X3(s) \cdot G) \cdot \frac{w_{u2}}{s} \tag{3.3}$$

$$X3(s) = X2(s) \cdot \frac{w_{u3}}{s} \tag{3.4}$$

$$OUT(s) = X1(s) \cdot A1 + X2(s) \cdot A2 + X3(s) \cdot A3 \tag{3.5}$$

By combining and simplifying from Eq.(3.2) to Eq.(3.5), it is possible to have,

$$\frac{X2(s)}{IN(s)} = \frac{w_{u1}w_{u2}}{s^2 + G \cdot w_{u2}w_{u3}} \tag{3.6}$$

$$\frac{X3(s)}{IN(s)} = \frac{w_{u1}w_{u2}w_{u3}}{(s^2 + G \cdot w_{u2}w_{u3}) \cdot s} \tag{3.7}$$

$$\frac{Out(s)}{IN(s)} = \frac{s^2 \cdot w_{u1} \cdot A1 + s \cdot w_{u1}w_{u2} \cdot A2 + w_{u1}w_{u2}w_{u3} \cdot (A1 \cdot G - A3)}{(s^2 + G \cdot w_{u2}w_{u3}) \cdot s} \tag{3.8}$$

The actual transfer function can be obtained by replacing $W_{un} = 1/sRnCn$, n=[1,2,3] and G=Rf/R2. The resistor Rf is used to implement the local feedback path while R2 in the input resistor of the second integrator.

$$\frac{Out(s)}{IN(s)} = \frac{Rf}{R2} \frac{(\frac{A2}{A3} sC3R3 + 1)}{sR1C1(1 + s^2RfR3C2C3)} A3 \tag{3.9}$$

The frequency response of the conventional 3^{rd}-order CT ΣΔ ADC is shown in Figure 3.2. There is a pair of complex conjugate poles on the y-axis which corresponding to the existence of resonance in the loop filter. Also, the resonance is confirmed with the peaking in the frequency response of the loop filter.

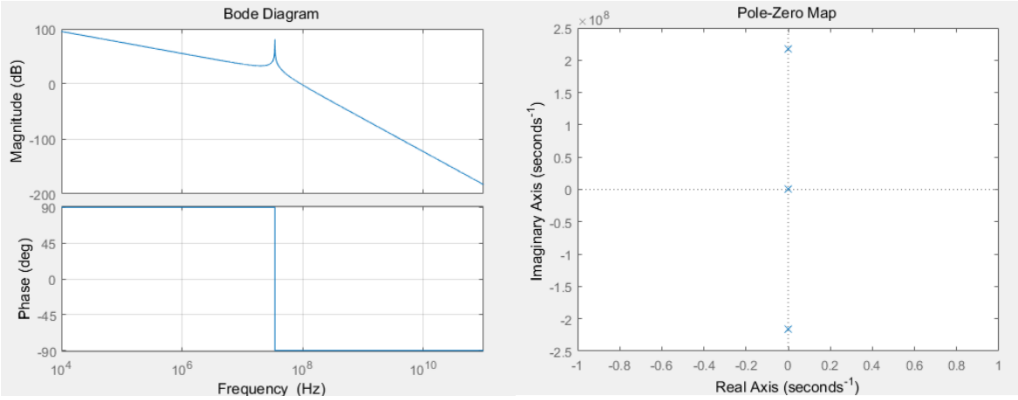

Figure 3.2: Frequency Response of Ideal Conventional 3^{rd}-order CT ΣΔ Modulator

3.1.2 A 3^{rd}-order ΣΔ Modulator with an Integrator and a Single Opamp Resonator

Figure 3.3 illustrates the block diagram of the proposed 3^{rd}-order CTΣΔ ADC with a single-opamp resonator. Instead of using two opamps to realize the resonance function, only one opamp is used in this case. The feed-forward coefficient A2 becomes the internal gain. The rest two feed-forward coefficients remain the same. The transfer function of the modulator with single opamp is expected to be equivalent to the conventional topology. The matching is verified by comparing the frequency behavior of two topologies shown in Figure 3.2 and Figure 3.4. The mapping process will be described in Section 4.1.

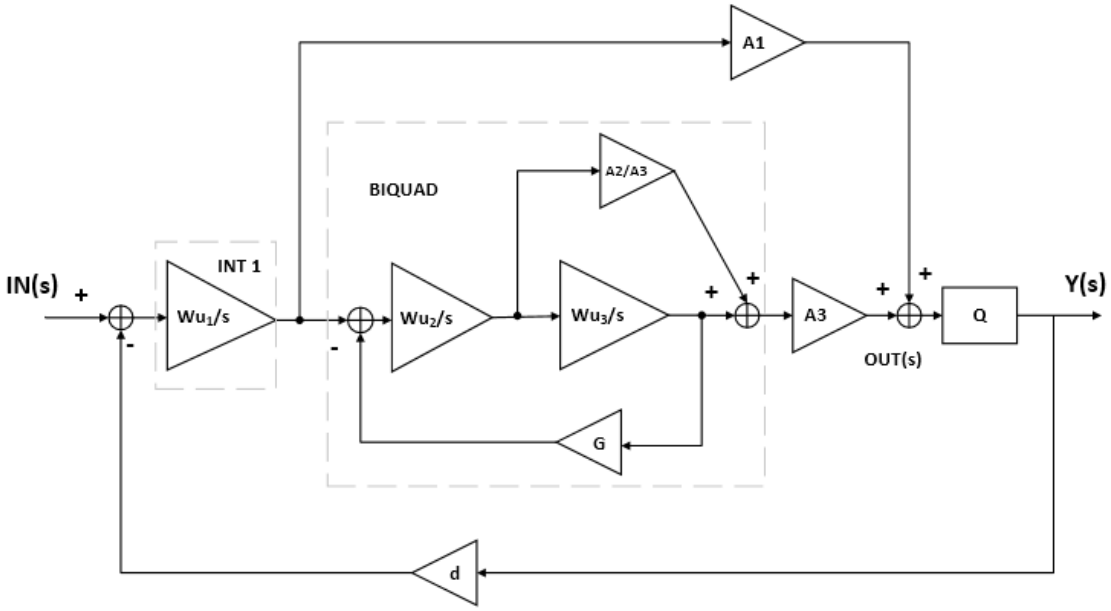

Figure 3.3: Block Diagram of a 3^{rd}-order CT Σ Δ ADC with a Single Opamp Biquad

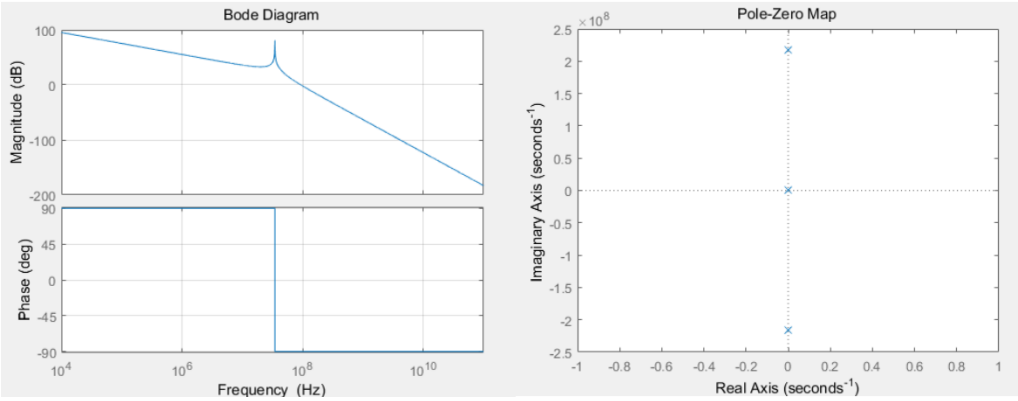

Figure 3.4: Frequency Response of a 3^{rd}-order CT ΣΔ Modulator with a Single Opamp Biquad

3.2 Modeling of an Integrator

The block diagram of the designed CT ΣΔ modulator is presented and transfer functions are derived in the previous section. Before discussing the non-idealities which affect the performance of the system, it is necessary to clarify the modeling of the blocks that will be used in the following chapter.

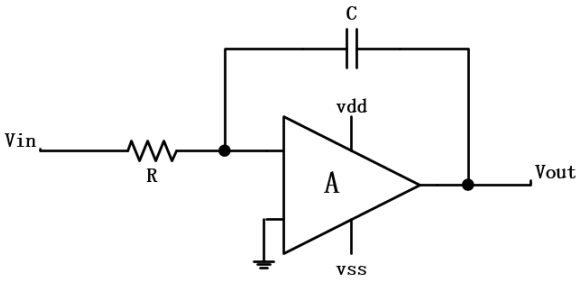

Figure 3.5: Modeling of an Ideal Opamp Integrator

Amplifiers are highly used as active elements in the blocks such as loop filter and quantizer. The modeling of the ideal opamp integrator is shown in Figure 3.5. An ideal integrator opamp model is assumed to have infinite gain and finite unity-gain frequency, the frequency behavior is shown in Figure 3.6. Its transfer function can be expressed as,

$$H(s) = \frac{1}{sRC} \tag{3.10}$$

It can be noticed there is one pole generated by input resistor and feedback capacitor and this pole is at DC hence the bandwidth is zero.

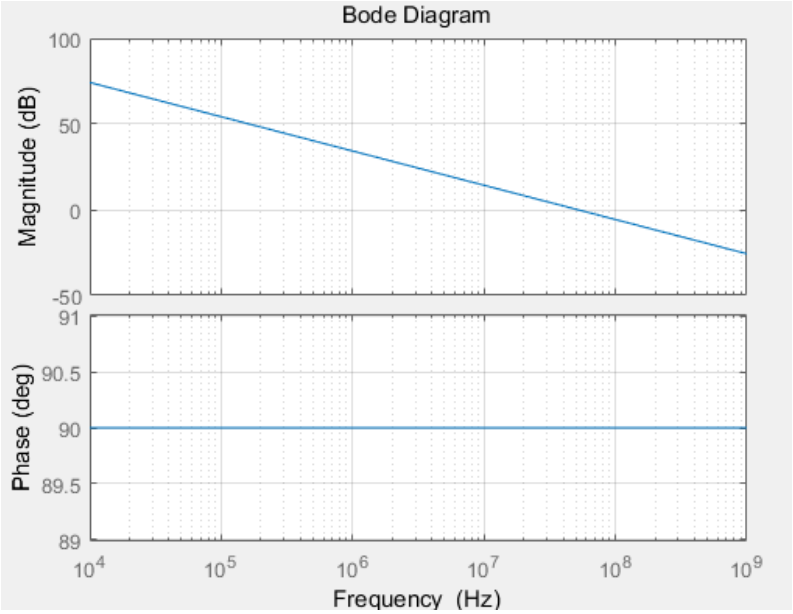

Figure 3.6: Frequency Response of an Ideal Opamp Integrator

To model the implementation of opamp, following model shown in Figure 3.7 has been used.

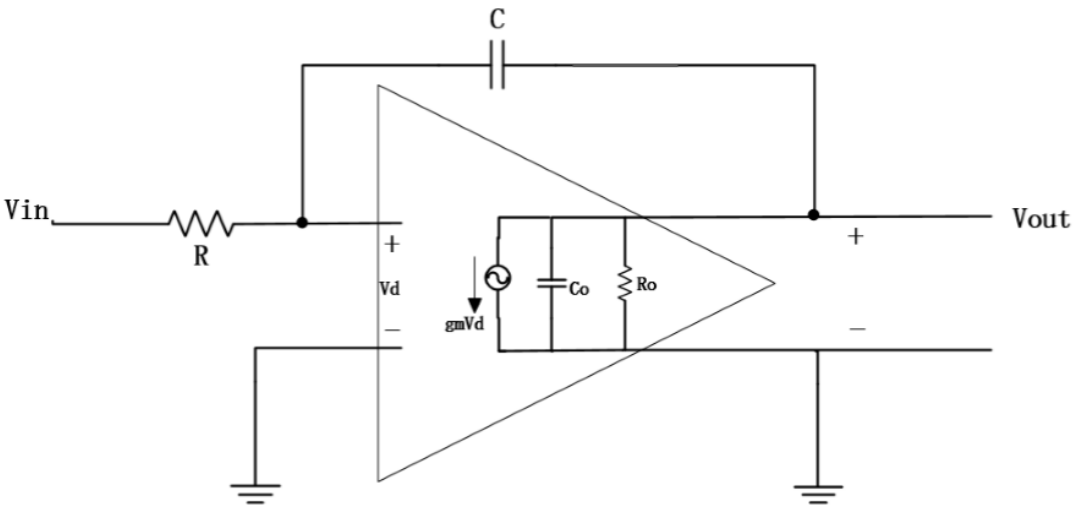

Figure 3.7: Modeling of a Real Opamp Integrator without Zero Compensation

Based on that model, it is possible to write KCL at nature ground node of the opamp.

$$\frac{V_{in} - V_d}{R} = \frac{V_d - V_{out}}{1/(sC)} \tag{3.11}$$

$$\frac{V_d - V_{out}}{1/(sC)} = g_m V_d + sC_o V_{out} + V_{out}/r_o \tag{3.12}$$

Hence the transfer actual function of the opamp integrator based on the model in Figure 3.7 can be derived as,

$$\frac{V_{out}}{V_{in}} = \frac{(CR_o)s - g_m R_o}{CC_o RR_o s^2 + (CR + CR_o + R_o C_o + Cg_m RR_o)s + 1} \tag{3.13}$$

Now the DC gain becomes finite and it is set to 30dB and it is the product of the transconductance gm(1.8mS) and output impedance r_o(18k). The output impedance is expressed as gm/(2πUGB) with the UGB set to 5.5GHz.

The corresponding frequency response is given in Figure 3.8. It can be noticed there are two poles with one dominant pole from RC pair and the other high-frequency pole from the opamp. With input resistance set to 10k and feedback capacitance set to 280f, two poles are located at around 6GHz and 1.6MHz. Additionally, a zero is introduced from gm and the feedback capacitor C and is located at around 1GHz. Unfortunately, this zero is located in the right half plane which is a sign of an unstable system hence certain compensation technique must be applied.
A standard way is to add a resistor of 1/gm in series with the capacitor to generate an extra pole to cancel off the effects of zero as is shown in Figure 3.9. The transfer function of the integrator now becomes,

$$\frac{V_{out}}{V_{in}} = \frac{(CR_o - Cg_m R_f R_o)s - g_m R_o}{(CC_o RR_o + CC_o R_f R_o)s^2 + (CR + CR_f + CR_o + R_o C_o + Cg_m RR_o)s + 1} \tag{3.14}$$

The frequency response is presented in Figure 3.10. With Rf=1/gm, the right half zero has been cancelled.

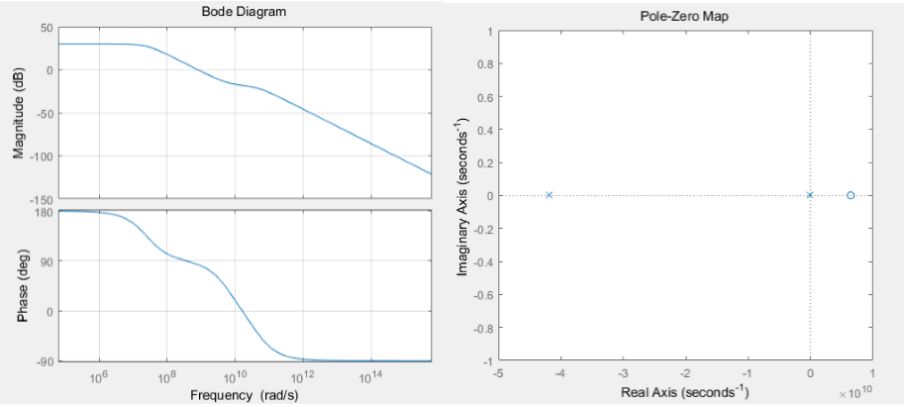

Figure 3.8: Frequency Response of a Real Opamp Integrator without Zero Compensation

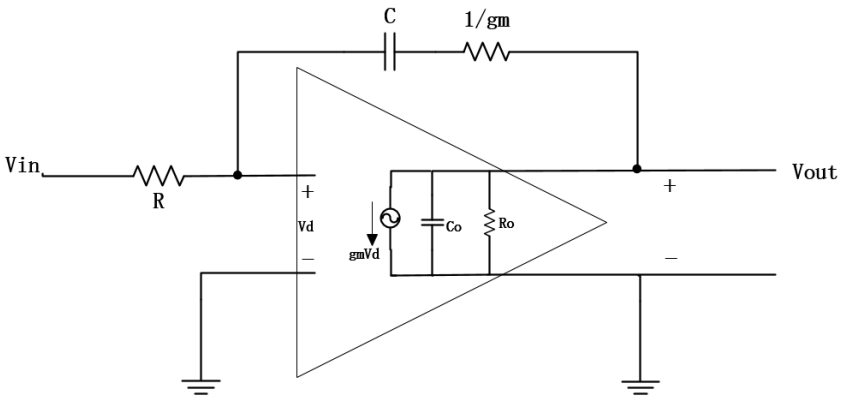

Figure 3.9: Modeling of a Real Opamp Integrator with Zero Compensation

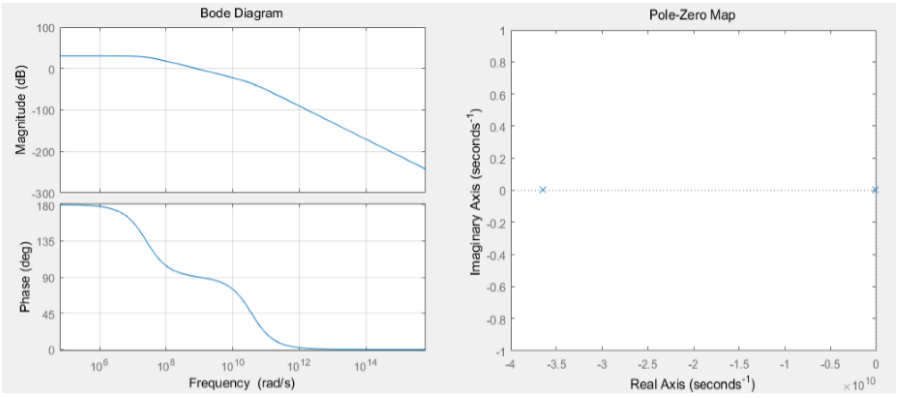

Figure 3.10: Frequency Response of a Real Opamp Integrator with Zero Compensation

3.3 Non-Idealities

In Section 3.1, the architecture of the purposed modulator is presented with power-efficient single-opamp and an integrator. The designed modulator shows a good match with the transfer function of the conventional design. Now the system nonidealities such as noise, nonlinearity and excess loop delay should be studied to check if the system could operate successfully under the system specifications. Noise is a random signal generally caused by random motion of electrons in the resistive material, random recombinations of holes and electrons in semiconductors or holes and electrons diffusing through a potential barrier [22]. The random fluctuation of a signal is a representation of noise and it is the limiting factor in determining the SNR of the system. The most common noises are thermal noise, quantization noise, and jitter. Nonlinearity in a converter system is commonly defined as the deviation from the ideal response. The SNDR is determined by nonlinearity. Besides, it is necessary to investigate the performance of the implementation. The design requirements can therefore be obtained as a summary of the investigation.

The modulator is assumed to be linear in our model. However, in reality, a slightly non-linear system has some fluctuations between the straight line and this variation is called non-linearity. Non-linearity can degrade the SNDR. As the first stage has the most stringent requirements of noise and distortion, its power consumption is therefore the dominant contributor to the total power consumption of the $\Sigma\Delta$ modulator. Hence, the power consumption of the first stage will be estimated as low power is the key issue for our design. Another unwanted source of non-ideality is excess loop delay (ELD) that is caused by the time of the comparator and this delay could affect the stability of the system. Apart from the nonidealities, in real implementation blocks such as opamps can only be designed to have limited gain and bandwidth which both were assumed to be infinite when modeling. The limited GBW could cause stability issue and this necessitates the investigation of finding the design requirements of the blocks of the modulator.

3.3.1 Noise

In an ideal $\Sigma\Delta$ modulator, the maximum SNR that can be achieved is often determined by the total quantization noise. But in the real implementation, both resistive blocks and transistors can contribute thermal noise hence degrade the overall SNR. Flicker noise is also a problem exists in MOSFETs and it is inversely proportional to the size of the transistors. Later will show the flicker noise is part of the reason for designing the matrix inverter structure in 30nm instead of 120nm as pMOS is too big compared to nMOS.

The techniques for minimizing quantization noise has been well-studied. But the upper limit of the overall SNR is determined by the amount of thermal noise in the modulator [23][24].

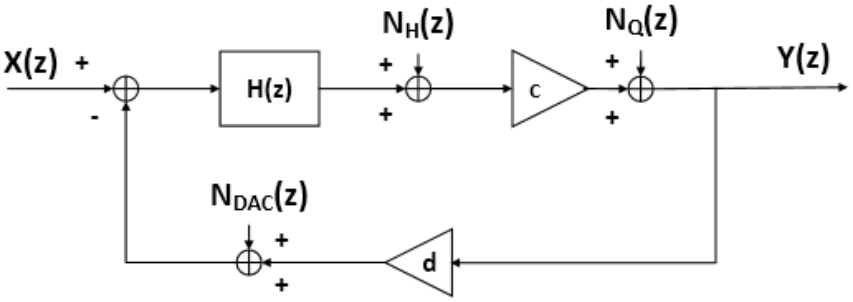

Figure 3.11: Modeling of the Modulator System for Noise Study (from Muhammed.B)

A model of the modulator for noise study is shown in Figure 3.11. Blocks such as loop filter, DAC, and quantizer are the main contributors. Among them, the thermal noise of the quantizer is less

dominating as it is shaped by the transfer function of the loop filter when input-referred while the DAC and loop filter contribute the most.

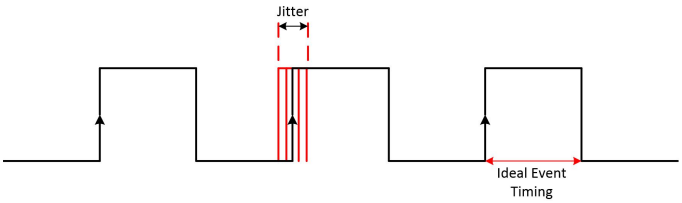

Figure 3.12: The DAC Feedback Signal with Jitter

Apart from thermal noise, the phase noise generated from the deviation of the phase of the feedback signal could further degrade the SNR. This degradation results from the fact the random phase modulation of the feedback signal is integrated due to the nature of the continuous time $\Sigma\Delta$ modulator, causing integration error and increasing noise floor. In addition to the error in the feedback signal, the sampled signal in the quantizer is also affected by the phase noise but it is heavily suppressed. It is common to define the amount of phase noise in the frequency domain as jitter specification and the effects of jitter can be expressed comparable to quantization noise as signal-to-jitter-noise-ratio (SJNR). In our design, the SJNR specification is set to 79dB.

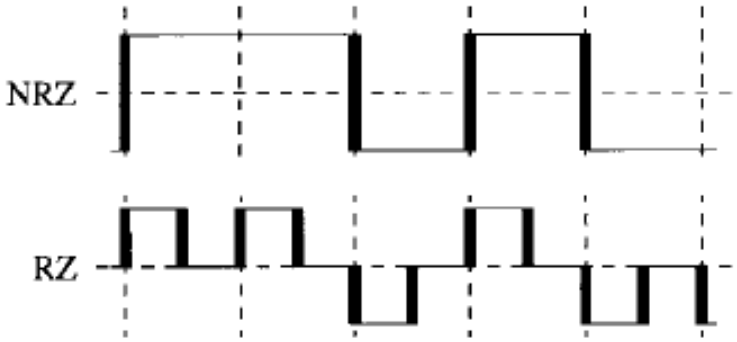

Figure 3.13: The Different DAC Pulses with Jitter

In addition to the purity of the clock source, the way to implement the DAC is also a factor determining jitter. There are two common shapes of DAC pulses, return to zero (RZ) or nonreturn to zero (NRZ). The difference between two pulses is that the NRZ pulse only switches when the data pulse switches hence it is less susceptible to jitter shown in Figure 3.13. Therefore NRZ pulse is often preferred in CT $\Sigma\Delta$ modulators.
Since the maximum SNR is limited by the amount of thermal noise, it is essential to optimize the power consumption within the range of noise specification. As is mentioned the loop filter and DAC are the main contributors to thermal noise, a model of them is presented in Figure 3.14. There are three blocks such as the input resistor, DAC resistor and the opamp generating thermal noise and these noises are assumed to be uncorrelated. Note all the noise sources are input referred and can be expressed as [25],

$$V_{nR} = \sqrt{4kT \cdot R \cdot BW} \tag{3.15}$$

$$V_{nRdac} = \sqrt{4kT \cdot Rdac \cdot BW} \tag{3.16}$$

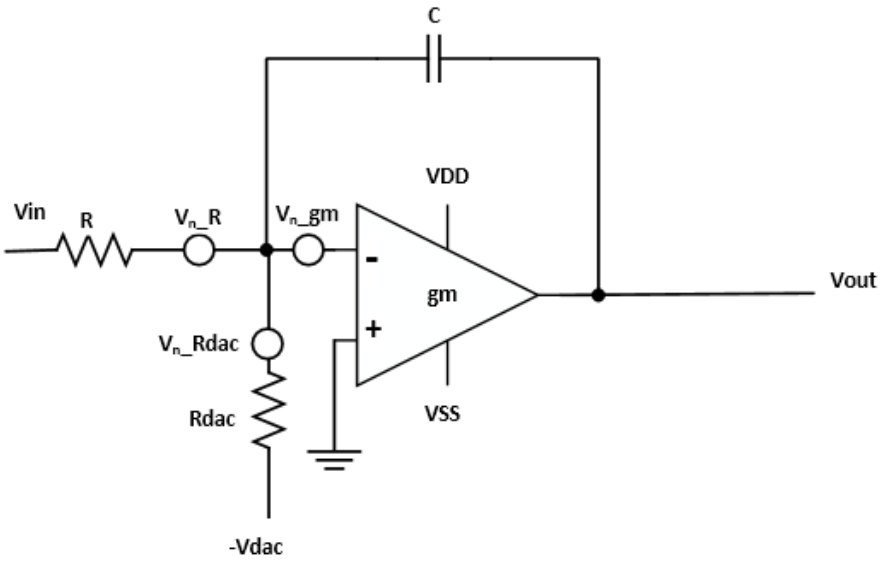

Figure 3.14: Modeling of an Integrator for Noise Estimation

$$V_{ngm} = \sqrt{\frac{4kT \cdot BW}{gm}} \tag{3.17}$$

Since the overall SNR is set to 67dB and quantization noise SNR is 69dB and the jitter noise is assumed to be 10dB higher than quantization noise which is 79dB. Also, the resistance of Rin and Rdac are equivalent and the opamp is modeled as a transconductor. The total input-referred voltage noise then is a sum of:

$$V_{N1}^2 = 2(V_{nR}^2 + V_{nRdac}^2(R^2/R^2{}_{dac})) + 2V_{ngm}^2(1 + R/R_{dac})^2 \tag{3.18}$$

With the assumption that the input resistance R_{in} is equivalent to DAC resistance R_{dac}, the only two variables left are R_{in} and gm. Therefore it is possible to find a relationship between R_{in} and gm by,

$$V_{ngm} = sqrt(V_N^2 - 4V_{nR}^2)/2 \tag{3.19}$$

A figure can be generated by varying the value of input resistance and find the change of transconductance,
Figure 3.15 presents the relationship between the resistance of the input resistor and the transconductance of the first amplifier. From our previous study, a gm of 1.8mS seems to be an appropriate value for meeting the system requirements. Besides, a larger input resistance reduces the power consumption hence the maximum resistance of the input resistor should be found within allowed thermal noise level. To obtain a gm of 1.8mS, the corresponding maximum Rin equals to 3.7kΩ.

The noise contribution from the second stage can be calculated in a similar way. A modeling of the input stage and the single-opamp resonator is shown in Figure 3.16. Assuming that all noise sources are all input-referred, thermal noise of the second stage is first referred to the output and shaped by the transfer function of the path it is transferring to the input. The total thermal noise then is in the form of,

$$V_{N2}^2 = V_{N1}^2 + 2V_{R2}^2(R/C)^2 + 2V_{gm2}^2(1 + R_2/R_n)^2(R/C)^2 \tag{3.20}$$

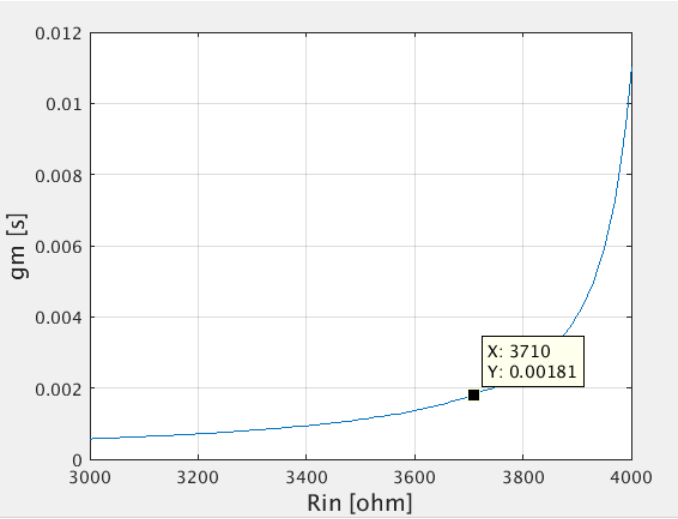

Figure 3.15: Gm2 vs R Simulation of the First Stage Integrator

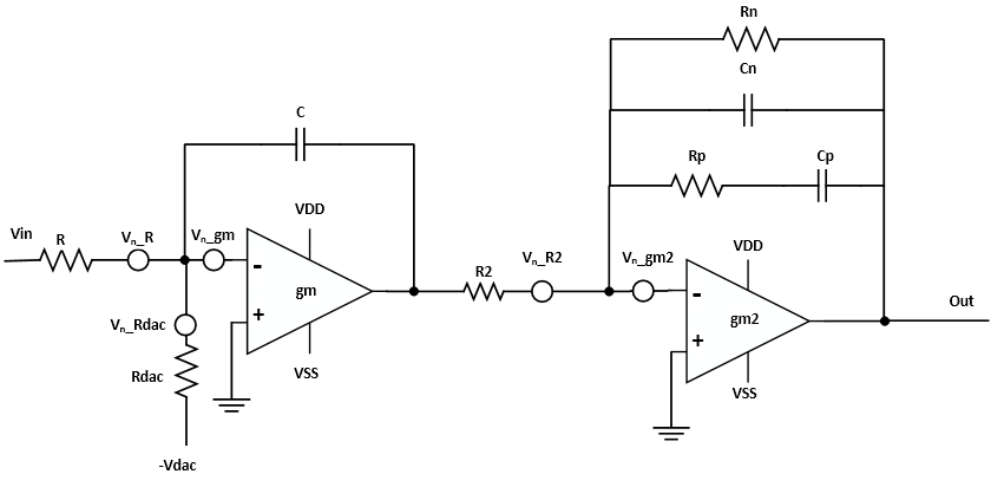

Figure 3.16: Modeling of an Integrator and a Biquad for Noise Study

$$V_{ngm2} = sqrt((V_{N2}^2 - V_{N1}^2 - 2V_{R2}^2(R/C)^2)/(2 * (1 + R_2/R_n)^2(R/C)^2) \tag{3.21}$$

$$V_{nR2} = \sqrt{4kT \cdot R_2 \cdot BW} \tag{3.22}$$

$$V_{ngm2} \propto \sqrt{\frac{4kT \cdot BW}{gm2}} \tag{3.23}$$

The input resistance of the first stage has been found from the previous discussion hence the thermal contribution of the first stage is fixed, the input resistance of the second stage can be found by plotting the relationship between transconductance and input resistance shown in Figure 3.17. A resistance of $18.6k\Omega$ is found corresponding to a gm 1.8mS.

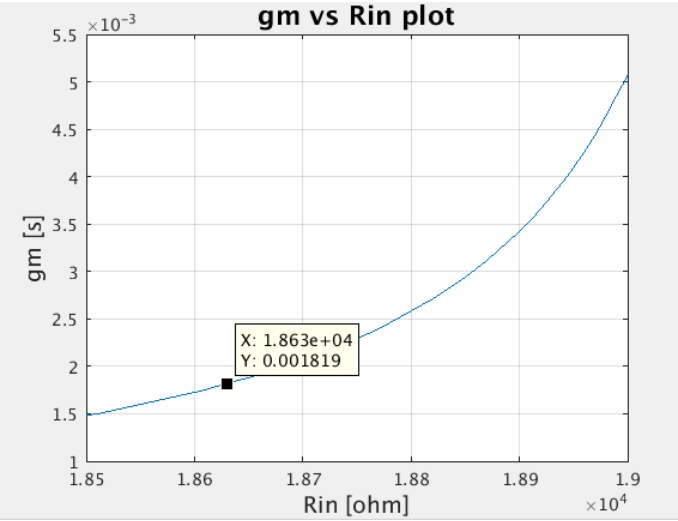

Figure 3.17: Gm vs $R2$ Simulation of the Single-opamp Biquad

In addition to quantization noise, the circuitry could generate thermal noise and the noisy clock source make the edges of the feedback DAC signal undefined. Both noise sources degrade SNR but the thermal noise considers to be the bottleneck of achieving a higher SNR. Hence a detailed study was given to the thermal noise modeling the loop filter and DAC, especially the first stage of the modulator. The input resistor and transconductor are the two main factors in determining thermal noise, with an appropriate value of the transconductance have been defined from the previous study of 1.8mS for both OTAs the input resistances of both stages are found to be $3.7k\Omega$ and $18.6k\Omega$. Later discussion will show that the transconductance gm is also a critical factor in determining the harmonic distortion of the loop filter. The result is found based on the noise specification shown in Table 3.1,

3.3.2 Non-Linearity

Section 3.3.1 has summarized the determinants to achieve a maximum achievable signal-to-noise ratio. Another performance of interests is non-linearity where in real implementation the system is not perfectly linear. In the designed single-bit CT $\Sigma\Delta$ modulator, the DAC is inherent linear hence the loop filter is the main block causing non-linearity. The effects of non-linearity generated from active elements in the loop filter would introduce harmonic distortion. Therefore the

Specifications	Value
SNR	66.7dB
SNR_Q	69dB
SJNR	79dB
Bandwidth	40MHz

Table 3.1: Specifications of the Noise

relationship between the nonlinearity of the loop filter and the harmonic distortion of the ΣΔ modulator is presented in this section.

It is well perceived that the first integrator non-linearity affects the system performance most significantly. The active-RC integrator implementation is preferred concerning its high linearity. In an ideal model, the input node of the opamp is assumed to be virtual ground as the opamp gain is high, and the input resistor as well as the DAC resistor could perform linear voltage to current operation. Due to limited opamp gain, there exists a residual voltage at the input node, and this voltage signal was subtracted by the input signal and DAC signal, generating an error signal and present at the output through the capacitor.

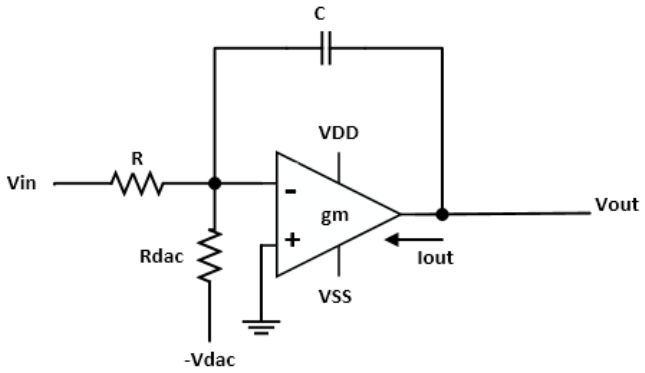

Figure 3.18: Modeling of the First Stage RC Integrator for HD3 Study

The model of the input integrator is shown in Figure 3.18. The transconductor is assumed to be weakly nonlinear and passive elements are linear. Only odd-order harmonics are dealt with due to the differential implementation [26]. Hence we have,

$$I_{out} = g_m \cdot v_d - g_{m3} \cdot v_d^3 \tag{3.24}$$

where g_m and g_{m3} are the fundamental and third harmonic transconductance respectively. By applying KCL,

$$\frac{V_{in} - V_d}{R_{in}} - \frac{V_{dac} + V_d}{R_{dac}} = g_m v_d - g_{m3} v_d^3 \tag{3.25}$$

Hence V_d can be derived in the form of,

$$V_d = \frac{(V_{in} - V_{dac})}{g_m R + 2} + \frac{g_{m3} R (V_{in} - V_{dac})^3}{(g_m R + 2)^4} \tag{3.26}$$

The output of the integrator is therefore,

$$V_{out} = \frac{-1}{C} \int_0^t (\frac{g_m (V_{in} - V_{dac})}{g_m R + 2} - \frac{2 g_{m3} (V_{in} - V_{dac})^3}{(g_m R + 2)^4}) dt \tag{3.27}$$

Applying the square-law model of the MOS transistor [27], the transconductance of the input transistor can be derived as,

$$g_{m3} = \frac{g_m^3}{64I_d^2} \tag{3.28}$$

where I_d is the bias current of the transistor and g_m is the transconductance of the input amplifier. Then the harmonic distortion is,

$$HD3 = \frac{g_m^2}{32I_d^2(2 + g_m R)^3} \tag{3.29}$$

Different values of third-harmonic distortion are listed in Table 3.2. It can be noticed that a gm of 1.8mS could meet the system requirement of HD3. A gm higher than 1.8mS looks attractive but it is not practiced to implement with our proposed inverter based amplifier.

gm	HD3
1.2mS	62.5dB
1.8mS	68dB
3.6mS	72dB
7.2mS	73.3dB

Table 3.2: HD3 Estimation with Different Transconductance Gm

The distortion component could also be suppressed at the edge of the signal band by the essence of the local feedback path where the resonator gain is evenly distributed in the signal band and to obtain a more flat quantization noise floor in band [19].

The aim of this design to meet the system requirements with minimum power consumption. The power consumption of the loop filter is further optimized in this work with the help of the single-opamp resonator. But the first stage still dominates the power consumption of the loop filter.

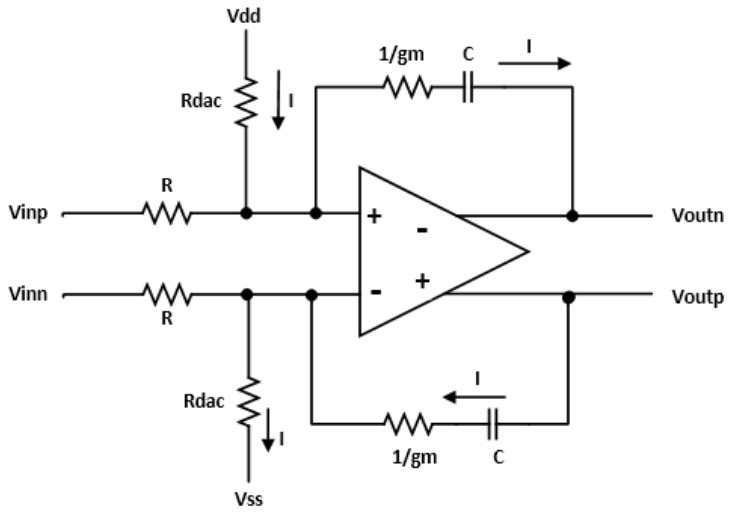

Figure 3.19: Modeling of the First Integrator for Power Estimation

A model for estimating the power consumption is presented in Figure 3.19. It is assumed that there is no current flowing from the input and flowing into the opamp. Hence the only current available is from the DAC resistor where the input of the DAC is switching between +Vdd and -Vdd and that is the effective current of the first stage. Therefore the power of the first stage can be estimated as, where I_{dd} the current drawing from V_{dd}

$$Power = I_{dd} \cdot V_{dd} \tag{3.30}$$

3.3.3 Excess Loop Delay Compensation

In the ideal 1^{st} order loop filter model, it is assumed that the loop filter, DAC and the sign inversion at the input contribute 90^0, 90^0 and 180^0 phase shift respectively. But in practical implementation, the non-zero switching time of the transistors could result in comparator delays and introduce latency in the DAC [28][29]. These effects introduce excess loop delay (ELD). ELD could cause extra phase shift to the system hence the system does not meet Barkhausen stability criterion anymore, and the system could become unstable with the increase of ELD.

A varied range of compensation methods has been purposed to reduce the effects of ELD [30]. The basic idea is to introduce an extra zero at fs/2 to bypass the loop filter at that frequency and this is often realized by adding a weighted path from the DAC to the input of the quantizer.

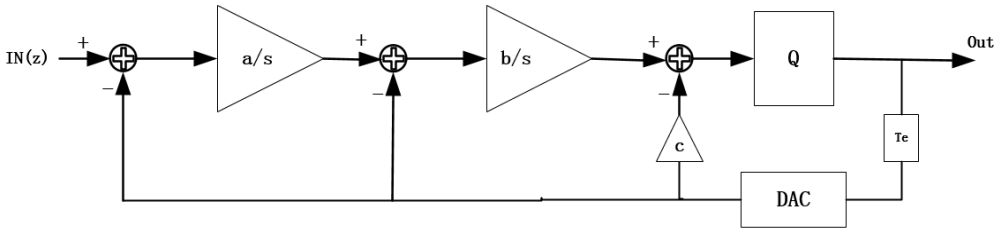

Figure 3.20: Block Diagram of the System with ELD Compensation

An example of the conventional ELD compensation technique is shown in Figure 3.20. The transfer function of an ideal second order $\Sigma\Delta$ modulator is described as,

$$H(s) = \frac{ab}{s^2 + bs + ab} \tag{3.31}$$

If the delay is introduced and modeled as e^{-st}, then the transfer function becomes the following using Taylor series,

$$H(s) = \frac{ab}{s^2 + be^{-st}s + abe^{-st}} \approx \frac{ab}{s^2(1 - bt + abt^2/2) + s(b - abt) + ab} \tag{3.32}$$

The higher order terms are neglected as the coefficients before they are relatively small. The idea of the ELD compensation is to preserve the transfer function when the system confronts extra delay. Apparently, the second order coefficient is not close to one hence an extra coefficient c is added and the transfer function becomes,

$$H(s) = \frac{ab}{s^2 + be^{-st}s + abe^{-st}} \approx \frac{ab}{s^2(1 - bt + abt^2/2 + c) + s(b - abt) + ab} \tag{3.33}$$

Therefore, the coefficients can be mapped from the original design by equating terms in the transfer function. $1 - bt + abt^2/2 + c = 1$, $b - abt = b^{'}$ and $ab = a^{'}b^{'}$ yield

$$a^{'} = \frac{a}{1 + at} \tag{3.34}$$

$$b^{'} = b(1 + at) \tag{3.35}$$

$$c = bt(1 + at/2) \tag{3.36}$$

To implement the ELD path, a direct method is to use active adder with the help of an extra amplifier. But this way comes with the expense of more power consumption due to the extra amplifier which should process high speed and large swing signals. An ideal way for this design is to implement the adder passively. Since passive adder is inherently linear and no extra power is consumed. The implementation will be explained in Chapter 4.

3.4 Circuit Implementation Issues

The previous sections discussed the non-idealities that need to be considered for designing a solid, well performed $\Sigma\Delta$ modulator. To implement the blocks of the modulator, some issues are common to be encountered during the design phase such as the limited gain and bandwidth of amplifiers. Besides, there exists certain deviation of accuracy when fabricating the device, and this is often called technology spread. The loop coefficients shift due to the process variations, the system could become unstable as a result of that.

3.4.1 Finite GBW of Opamps

In the ideal model, an amplifier is assumed to have unlimited gain as well as infinite bandwidth. However real amplifiers have only limited gain bandwidth product (GBW) and could degrade the performance of the modulator by reducing the phase margin of the amplifier. Besides, the loop delay caused by finite GBW could also be regarded as a kind of ELD.

To find the effects of finite DC gain, the model of the amplifier with finite DC gain, unlimited bandwidth is first studied. As there are two opamps in the loop filter, the degradation of performance due to limited DC gain can be found by reducing one of the opamp DC gain while fixing the rest DC as before.

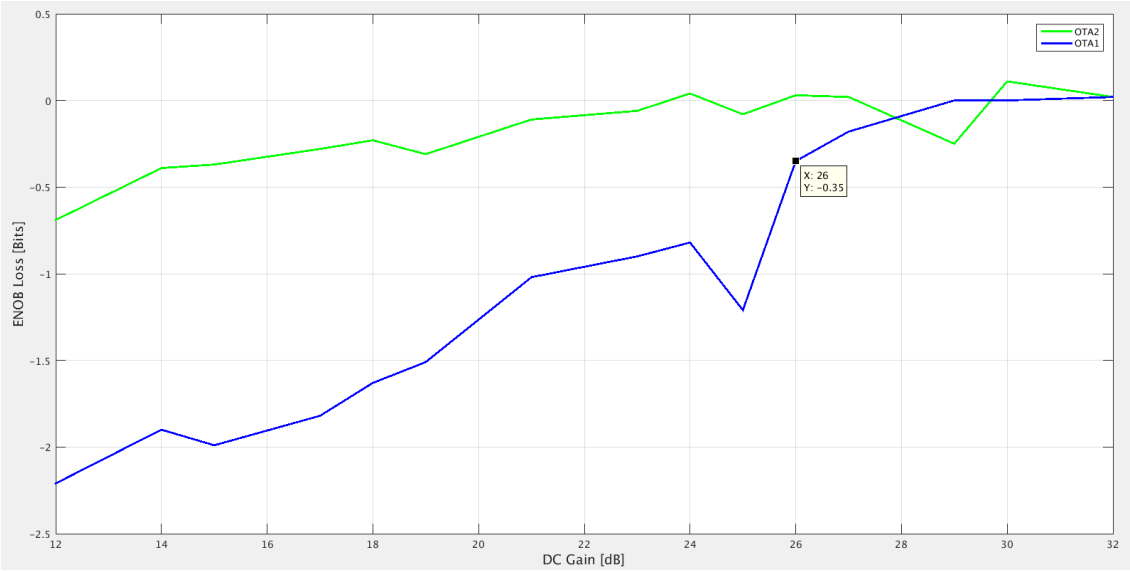

Figure 3.21: DC Gain vs ENOB Loss Simulation

As has been demonstrated in Figure 3.21, the DC gain of the first stage amplifier has more impacts on the ENOB of the modulator. It is required to have a DC gain of 26dB for the first stage to

obtain acceptable degradation of performance. The effects of second stage DC gain are less severe compared to the first stage, a DC gain of 20dB would meet the requirement because the first stage can compensate the loss of gain of the following stage. Note the DC gain only defines the gain over relative low frequencies, there is no drastic change on the SQNR of the modulator.

For analyzing the effects of finite GBW, a model of the amplifier with finite GBW has been used. The amplifier is modeled as a 1^{st}-order model with a single pole. The transfer function of can be expressed as 3.37, where A_0 defines DC gain w_0 describes the location of the pole.

$$A(s) = \frac{A_0}{1 + \frac{s}{w_0}} \tag{3.37}$$

$$GBW = A_0 \cdot w_0 \tag{3.38}$$

$$A(s) = \frac{GBW}{s + w_0} \tag{3.39}$$

The plot 3.22 presents the ENOB loss of the modulator as a function of the finite GBW. It can be noticed that the first stage has the most demanding requirement of GBW where a GBW of 2GHz is necessary. The domination is since the phase margin of the loop filter is profoundly affected by the limited GBW of the first stage while this effect is less effective in the second amplifier. Therefore, the requirement of second amplifier GBW is more relaxed as is also shown in the plot. The expected GBW of the second stage is around 1.5GHz.

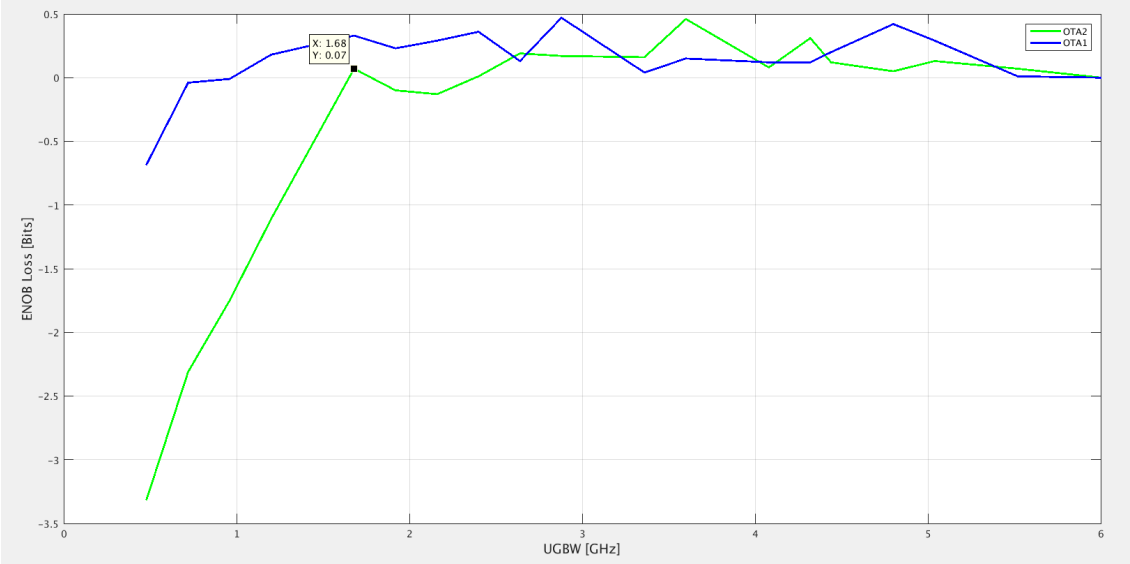

Figure 3.22: GBW vs ENOB Loss Simulation

From the above study, the specifications of the two OTAs in the loop filter are listed in Table 5.2. With the transconductance of both amplifiers set to 1.8mS, it is required to obtain a DC gain of 26dB for the first while having a DC gain of 20dB for the single-opamp biquad. The GBW of the two OTAs is expected to beyond 2GHz, 1.5GHz.

3.4.2 Technology Spread

With the advancing of CMOS technologies, the effects of process variation should be taken into consideration in nano-meter scale [31]. Because in $\Sigma\Delta$ modulators, the cutoff frequency and RC

Blocks	Specifications	Value
OTA1	gm	1.8mS
	DC gain	26dB
	GBW	2GHz
OTA2	gm	1.8mS
	DC gain	20dB
	GBW	1.5GHz

Table 3.3: Specifications of the OTAs

time constant of the loop filters in the modulator are often required to be precise. The RC time constant spread could go up to ±40%. To prevent using extra passive components which could bring up costs and device size, often an on-chip tuning network is applied.

Figure 3.23 presents the model for analyzing device process variation. To model the process variation, it is assumed to have ±20% process variation contributed equally from passive components. D1, D2, D3 are the coefficients describing the RC time constant spread of three integrators respectively. The result of the system SNR responding to the spread of ±20% is given in Figure 3.24. Recall that the modulator requires an SNR of 68dB, a closer look at the plot is shown in Figure 3.25. Hence for the first integrator, the system is able to handle ±10% spread, that is, ±5% from the resistor and ±5% from the capacitor if an active RC integrator is used.

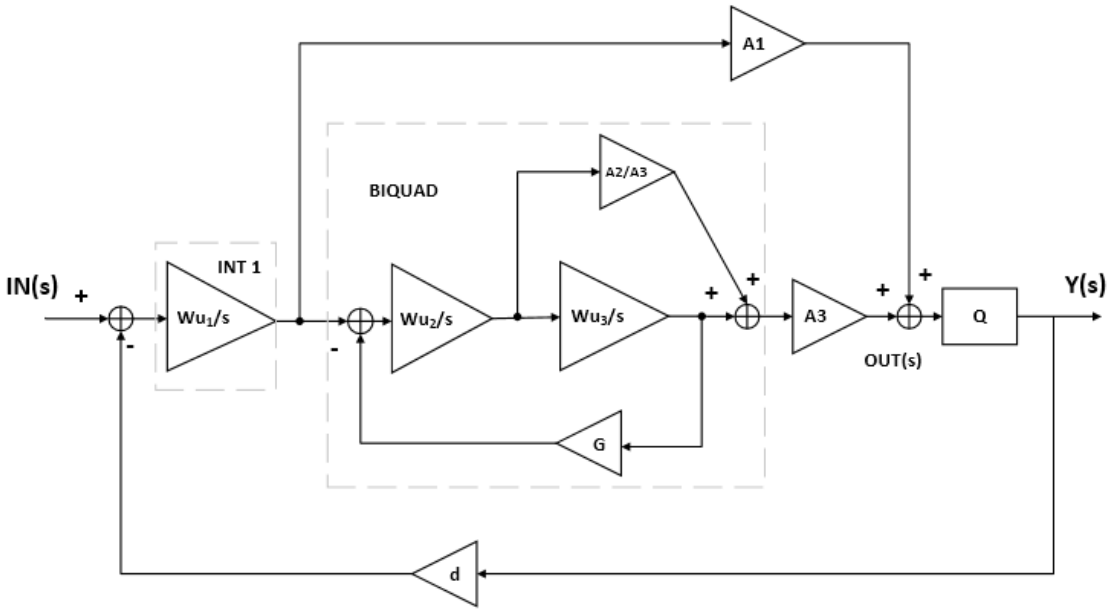

Figure 3.23: Block Diagram of the Modulator with a Single-opamp Biquad

For passive tuning system, it has been proved to better calibrate capacitors than resistors. Also, capacitor tuning performs high linearity since the capacitance does not vary with the voltage across it. The change of capacitance does not have any effects on the operation points of the transistors. Therefore, the passive capacitor bank implementation will be presented in the next chapter.

To find the number of bits for a precise tuning system, the maximum error between the theoretical capacitor and real implementation is of concern. If we assume a ±40% RC spread and C tuning structure will be used, the capacitor bank structure can be expressed with a maximum

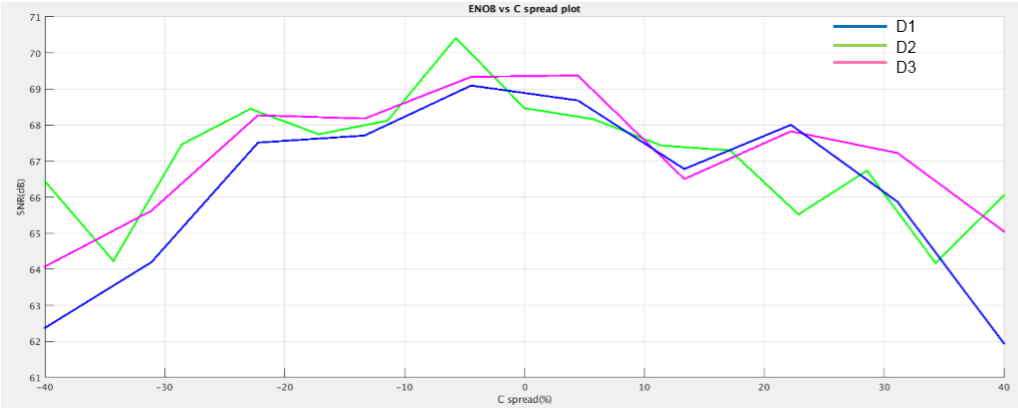

Figure 3.24: System Performance Response of RC Spread

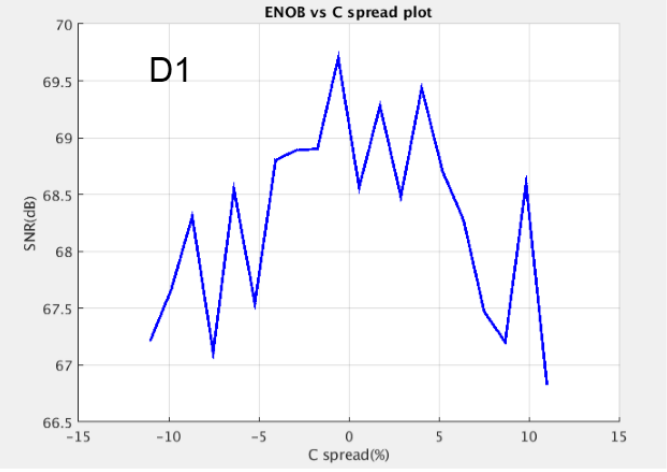

Figure 3.25: System Performance Response of RC Spread of the First Integrator

capacitor and a unit capacitor,

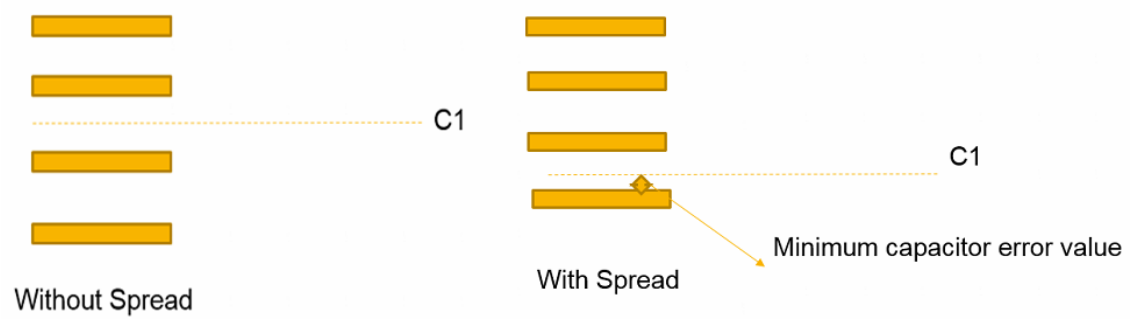

Figure 3.26: Capacitor Bank Structure with/without RC Spread

$$C_{main} = \frac{C1}{0.6} \tag{3.40}$$

$$C_{unit} = \frac{C1}{1.4} \tag{3.41}$$

$$C_{step} = \frac{C_{main} - C_{unit}}{2^{bit} - 1} \tag{3.42}$$

The number of different capacitance values this tuning system can provide is based on the number bits. Based on the simulation results shown in Figure 3.27 and Figure 3.28, it can be noticed that with a 4bits structure, a maximum capacitor error could reach 4% while the error is around 2% with a 5bits resolution.

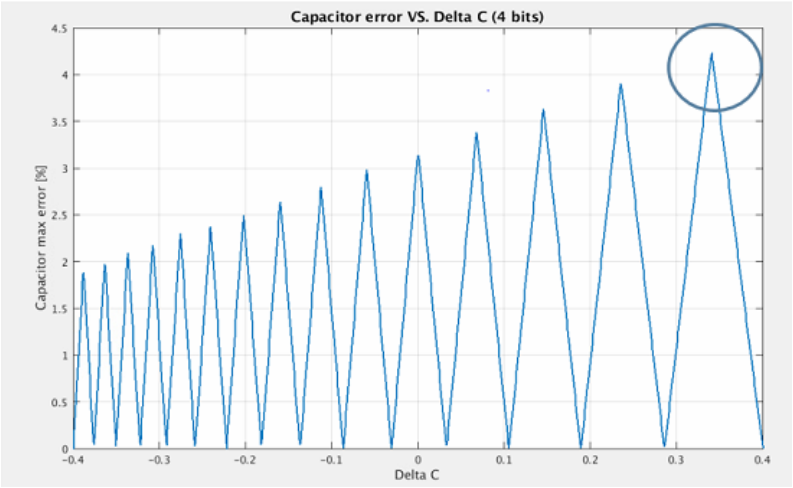

Figure 3.27: Capacitor Error with Four-bits Capacitor Bank

A similar analysis could be applied to the resonator. Assume ±40% RC spread and both R and C have the same contribution. Note that the D2 coefficient becomes the inherent coefficient if the biquad is implemented by a single-opamp resonator. Therefore, the variation of coefficient D3 has been found with respect to technology spread. As a result of the simulation shown in Figure 3.28 and Figure 3.29. The system can handle ±10% RC spread without loss of SNR hence the 5bit C tuning structure can sustain the requirement.

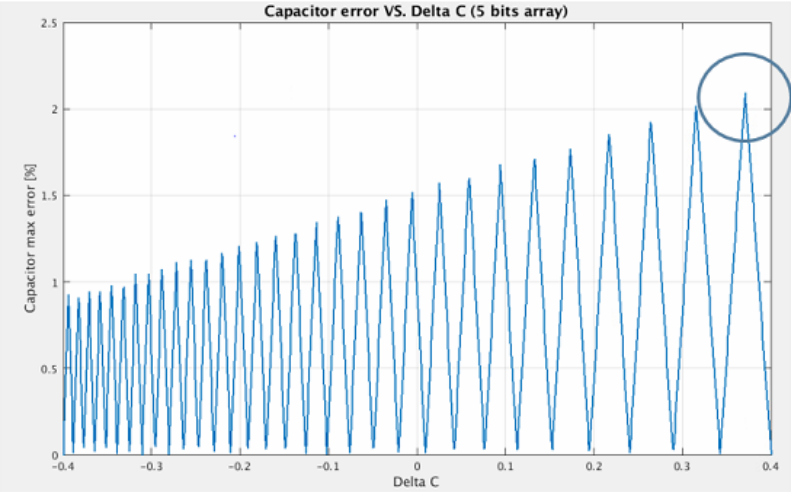

Figure 3.28: Capacitor Error with Five-bits Capacitor Bank

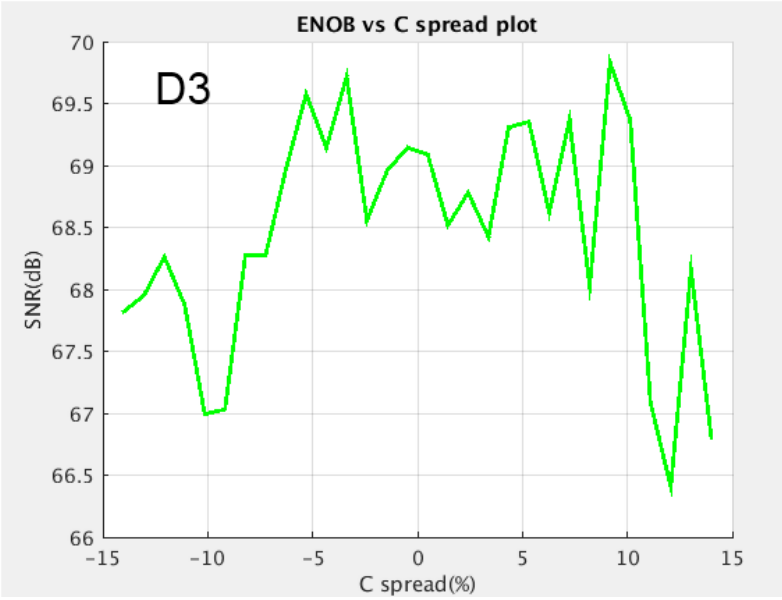

Figure 3.29: System Performance Response of RC Spread from the Single-opamp Biquad

3.5 Summary

This chapter presents the system-level design of a 40MHz 3^{rd}-order $\Sigma\Delta$ with 68dB dynamic range. The structure of a conventional 3^{rd}-order modulator with resonator has been shown initially and it was followed by the structure of a 3^{rd}-order modulator with single opamp where one opamp has been eliminated for the concern of a low power design. Then, system non-idealities such as noise,non-linearity were considered for three stages. As is well known that the non-linearity of the modulator is dominated by the first stage so the effects of the following stage on non-linearity can be ignored. In practice, the opamps are implemented with limited GBW and limited GBW could degrade system performance. Besides, finite GBW could cause excess loop delay which could result in an unstable modulator and certain compensation method has to be applied.

Chapter 4

Implementation

In this chapter, the loop filter implementation of a 3^{rd}-order continuous-time $\Sigma\Delta$ modulator will be presented. The high-speed amplifier topology and loop filter architecture are developed based on previous sections. The 3^{rd}-order feedforward summation with local resonator feedback loop filter is initially implemented by three integrators with resistive summation. The loop filter was later replaced by an integrator followed by a single-opamp biquad. As the new resonator structure eliminates one opamp, the power consumption is greatly decreased. To demonstrate the theory, the loop filter is implemented targeting a 2.4GHz 3^{rd}-order single bit continuous-time $\Sigma\Delta$ modulator with 40MHz bandwidth and it is based on the 28nm HPC process with a supply voltage of 0.9V. The single-bit quantizer is implemented in VerilogA and the DAC is implemented with ideal components. Besides, the ELD compensation is realized by adding a resistive DAC around the quantizer. The modulator can overall achieve an ENOB over 10bits, corresponding to an SNDR over 60dB. The HD3 measured is higher than 70dB over three process corners. The power consumption of the designed loop filter is around 0.5mW with a 0.9 V supply.

4.1 Architecture Overview

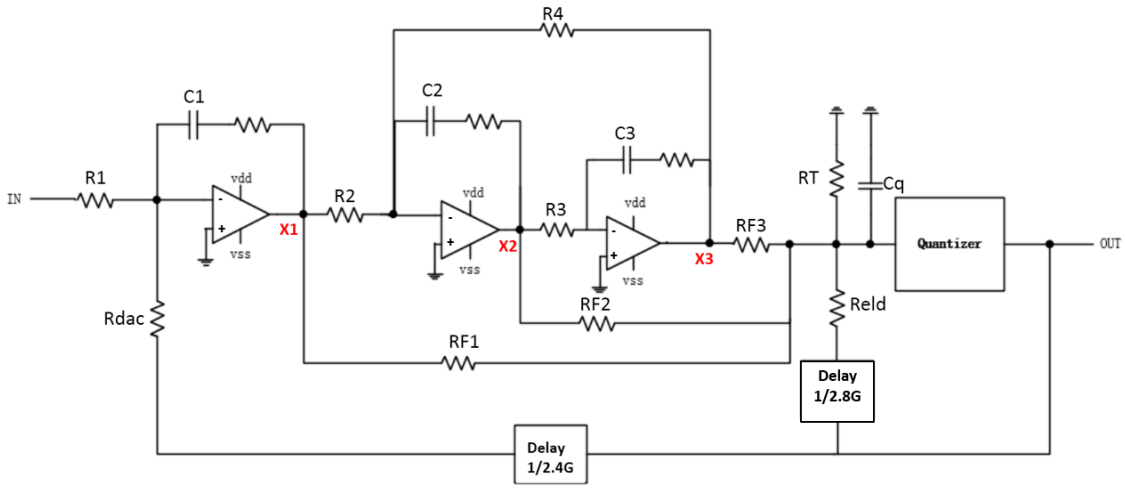

Figure 4.1: Implementation of the Conventional 3^{rd}-order Loop filter

Figure 4.1 shows the implementation of a 3^{rd}-order CT $\Sigma\Delta$ modulator with feed-forward and local feedback. All three integrators are RC integrator due to the high linearity they can provide [32]. A

resistor is added in series with the capacitor in the feedback path and it is used to compensate the right half plane zero (gm/C) introduced from the amplifier. A resonator is achieved by forming a local feedback path around the second and third integrator. The existence of the resonance can help spread the gain more evenly in the band and suppress quantization noise more heavily because otherwise, all the poles are in the origin.

The transfer function of each output can then be derived as Eq.(4.1) to Eq.(4.3), where H1(s) describes the transfer function between the input and the output of the first integrator, while H2(s) and H3(s) defines the transfer function between its input and output.

$$H_1(s) = \frac{X1(s)}{IN(s)} = \frac{1}{sR1C1} \tag{4.1}$$

$$H_2(s) = \frac{X2(s)}{X1(s)} = \frac{sR3C3R4}{R2(1 + s^2C2C3R3R4)} \tag{4.2}$$

$$H_3(s) = \frac{X3(s)}{X2(s)} = \frac{1}{sR3C3} \tag{4.3}$$

The combination of second, third integrator and the local feedback path realizes a resonator as is shown in Figure 4.2. The transfer function of the resonator can be obtained as,

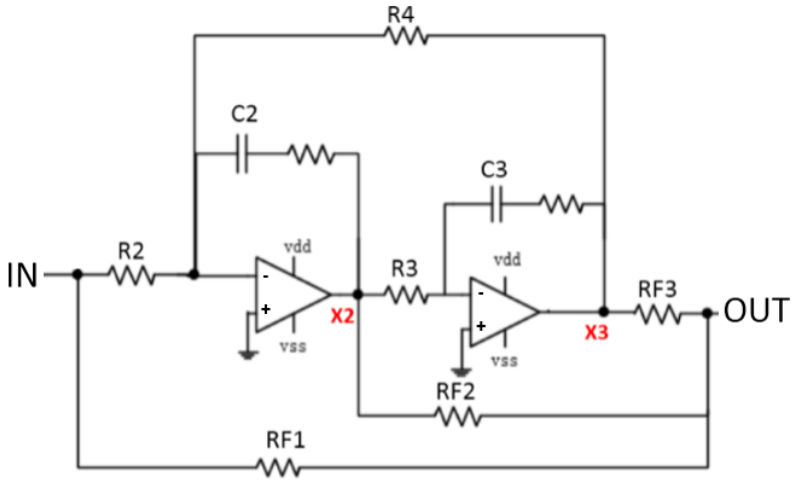

Figure 4.2: The Resonator in the Conventional 3^{rd}-order Loop filter

$$H_{resonator}(s) = \frac{X3(s)}{X1(s)} = \frac{X2(s)}{X1(s)}\frac{X3(s)}{X2(s)} = \frac{R4}{R2}\frac{1}{(1 + s^2R4R3C2C3)} \tag{4.4}$$

The transfer function of the biquad after the summer is,

$$H_{resonator}(s) = \frac{R4}{R2}\frac{A3(sR3C3\frac{A2}{A3} + 1)}{(1 + s^2R4R3C2C3)} \tag{4.5}$$

The pole and zero are in the form of,

$$w_z = \frac{A3}{A2}\frac{1}{R3C3} \tag{4.6}$$

$$w_p = \frac{1}{\sqrt{R4R3C2C3}} \tag{4.7}$$

Although the passive summation meets the idea of low power design, there is still a lot of power consumed in the opamps. Additionally, since the opamps are with limited GBW, the loop phase delay introduced by opamps reduces the stability range of the modulator [33]. Therefore a new loop filter with a single-opamp biquad is proposed shown in Figure 4.3.

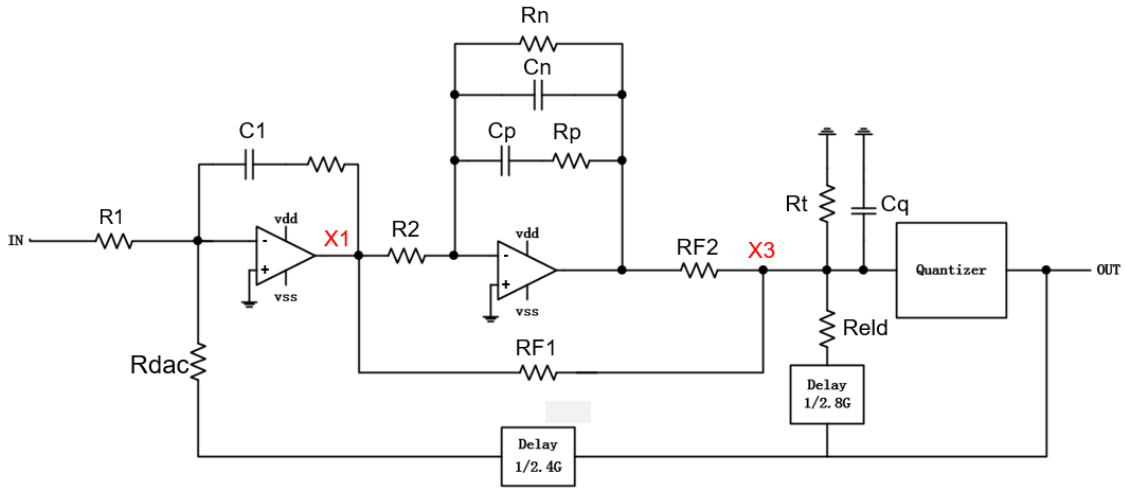

Figure 4.3: Implmentation of the 3^{rd}-order Loopfilter with a Single-opamp Biquad

In the proposed new loop filter topology, the first stage is implemented the same way as an RC integrator while the previous second and third stage is replaced by a single-opamp resonator. Note that the feed-forward coefficient A2 is now inherent in the resonator hence one feedforward path has been omitted.

To map the network from the conventional loop filter to the new loop filter, the transfer function of the single opamp resonator is derived based on Figure 4.4,
Here the amplifier is assumed to be ideal hence no current flows into the amplifier and the currents of different branches can be derived as,

$$I_{in} = \frac{V_{In} - V_X}{R2} \tag{4.8}$$

$$I_1 = \frac{V_X - V_{Out}}{Rn} \tag{4.9}$$

$$I_2 = (V_X - V_{Out})sC_n \tag{4.10}$$

$$I_3 = \frac{(V_X + V_{Out})}{Rp + \frac{1}{sCp}} \tag{4.11}$$

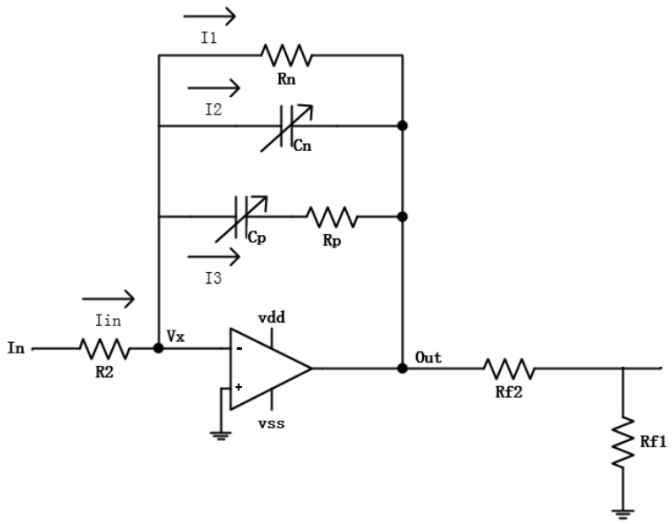

Figure 4.4: Schematic of the Single-opamp Resonator

By applying KCL, the transfer function of the single opamp resonator including the summation node becomes,

$$H_{resonator}(s) = \frac{V_{out}}{V_{in}} = \frac{Rn}{R2}\frac{A3(sCpRp(A2/A3)+1)}{1+s^2CnCpRpRn} \tag{4.12}$$

where the pole and zero are in the form of,

$$w_z = \frac{1}{RpCp} \tag{4.13}$$

$$w_p = \frac{1}{\sqrt{RnRpCnCp}} \tag{4.14}$$

The transfer function of the loop filter is then derived as,

$$H_{loopfilter}(s) = \frac{Rn}{R2}\frac{sRpCp+1}{-s^2CnRnCpRp - s\left(RnCn - RnCp - RpCp\right) - 1}A3 \tag{4.15}$$

To ensure resonance, the 1^{st}-order term in the denominator should be equal to zero which gives the resonance condition,

$$-CnRn + RnCp + RpCp = 0 \tag{4.16}$$

Therefore, the network can be mapped by checking the pole, zero location together with ensuring the resonance condition. Note this is based on the condition of an ideal opamp, for the application it is necessary to re-do the mapping to compensate for the loss of gain also the location shift of the resonance. Also, the resistors and capacitors used are from the 28nm HPC process, so all the parasitics are taken into consideration.

4.2 Inverter Based Amplifiers

4.2.1 Inverter Study

It is well known that the opamps are the most limiting component in minimizing the power consumption [20]. Nonetheless, a low-voltage operation is always required, making it hard to achieve

a high DC gain. A diversified way of implementing the OTAs have been reported in the literature. For instance, Uneo [34] has purposed the pseudo-differential pair where the tail current source is omitted to save some voltage headroom as well as some cascading gain stages for improving DC gain shown in Figure 4.5. However, the cascading structure complicates the circuit stability. It is also possible to realize a power efficient, large DC gain opamp with the help of negative resistance shown in Figure 4.5. It is achieved by cross-coupling transistors to improve output resistance and effective gain [35][36].

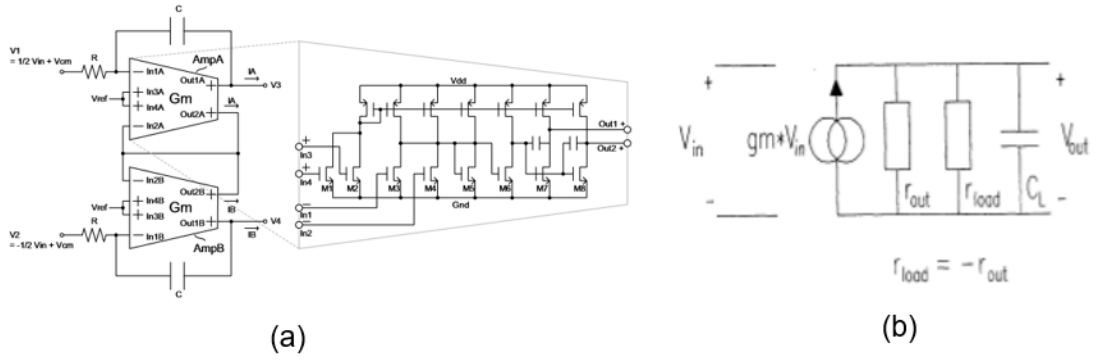

Figure 4.5: (a)Pseudodifferential Pair Eliminating the Tail Current Source
(b)Loading the Output of the OTA with a Negative Resistance to Make Infinite Gain

It is also attractive to build opamps by inverters [37]. By keeping both nMOS and pMOS in the saturation region, it can obtain the topology of the CMOS digital inverter but operated at a common mode voltage. The main disadvantage of inverter-based amplifiers is their high sensitivity to PVT corners and temperature as their gain and GBW can vary drastically over different conditions. Recall that the reduction of DC gain of an amplifier could degrade noise performance since the noise floor is raised up [17]. Also, the limited GBW could introduce ELD which affects the modulator system stability [14].

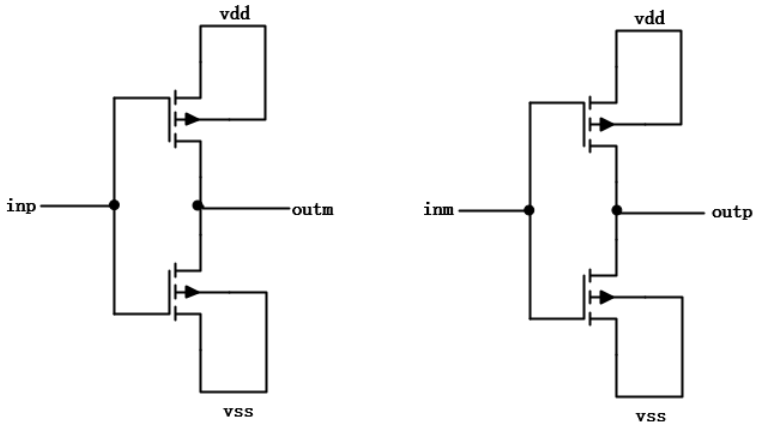

Figure 4.6: Schematic of an Inverter Based OTA

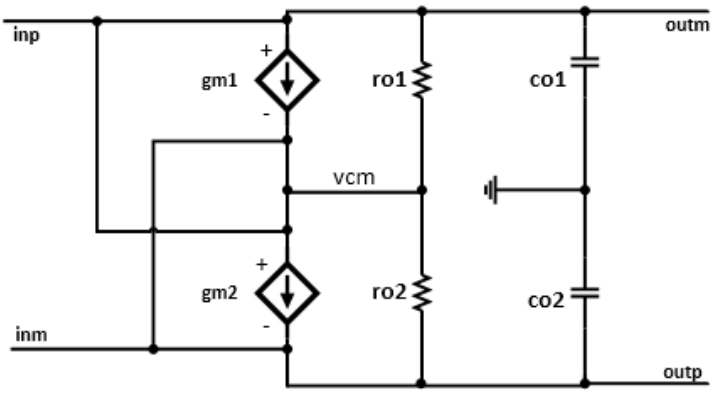

Figure 4.7: Small Signal Model of the Inverter

The inverter design commenced with a channel length of 120nm. From system-level design, it is required to have a gain over 26dB and a GBW of 2GHz with effective gm of 1.8mS for the first stage amplifier. The aim of the design was initially to set the input and output common mode at half supply for optimal swing. Since both transistors are in the saturation region, small signal parameters of a single transistor can be expressed as [38],

$$g_m = \frac{uC_{ox}WV_{gt}}{L} \tag{4.17}$$

$$r_o = \frac{2L^2}{\lambda\mu C_{ox}WV_{gt}^2} \tag{4.18}$$

$$A_o = \frac{2L}{\lambda V_{gt}} \tag{4.19}$$

$$GBW = \frac{\mu C_{ox}WV_{gt}}{LC_{tot}} \tag{4.20}$$

The small signal model of the inverter pair is shown in Figure 4.7. It can be found the effective gm of the inverter pair doubles the single inverter but with output impedance halved. To obtain an intrinsic common mode at the half supply voltage, the pMOS is made larger than nMOS, and the W/L ratio is found by targeting a total gm of 1.8mS as well as a DC gain over 26dB. The parameter of the designed inverter is shown in Table 4.1.

The definition of intrinsic common mode value is presented in Figure 4.8, where an inverter is input-output connected and the output is followed by a voltage controlled voltage source with a copy of the first inverter. The voltage at the input of the second inverter is defined as the trip point which presents the intrinsic common mode of the inverter.

The simulation results of the inverter shown in Table 4.1 demonstrates that DC gain, UGB, intrinsic common mode and effective gm have met the requirements successfully. However, the pMOS is around ten times larger than nMOS and this is not practical to design. Besides, the size of the nMOS is so small that it could contribute a significant number of flicker noise which is the

	Inverter
Wp/Lp(nm)	9800/120
Wn/Ln(nm)	1050/120
Gain Intrinsic(dB)	30
Gain(20k loading)(dB)	24.6
GBW(GHz)	7.2
-3dB frequency(MHz)	600
1/f noise(v^2/Hz) @0.22MHz	4.16e-9
Current(uA)	64.2
Gmp/Gmn(mS)	1.25/0.55
Intrinsic common mode(mV)	450

Table 4.1: Inverter Parameter Table

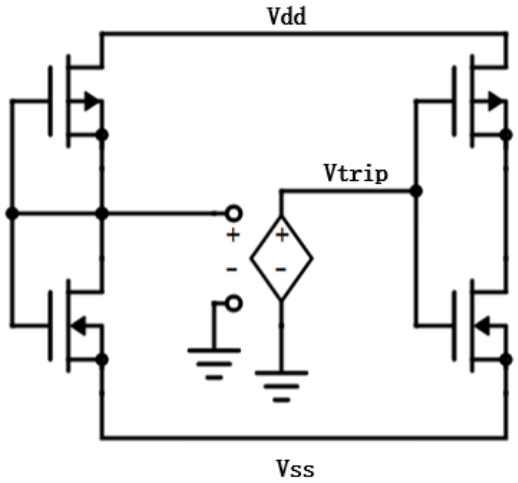

Figure 4.8: Intrinsic Common Mode Value Circuit

	Inverter1	Inverter2
Wp/Lp(nm)	9800/120	2800/120
Wn/Ln(nm)	1050/120	2800/120
Gain Intrinsic(dB)	30	30
Gain(20k loading)(dB)	24.6	24.5
GBW(GHz)	7.2	14
-3dB frequency(MHz)	600	1200
1/f noise(v^2/Hz) @0.22MHz	4.16e-9	5e-9
Current(uA)	64.2	66.6
Gmp/Gmn(mS)	1.25/0.55	0.9/0.9
Intrinsic common mode(mV)	450	380

Table 4.2: Inverter Parameter Table of Two Inverters with Different Size

main source of noise at low frequency. Therefore with this configuration, to minimize flicker noise the size of transistors have to be large and that consume a lot of power. A new inverter topology has to be designed to pay less expense for better performance.
Table 4.2 gives a comparison of the two inverters we have studied. It can be found that both inverters can meet the OTA requirements with comparable DC gain and similar current consumption. The major difference falls on the transistor size ratio and its intrinsic common mode value. For inverter2, a comparable transistor size is wanted but the intrinsic common mode value is far away from 450mV. The results motivate the study of looking for a structure which has comparable transistors size also with intrinsic common mode voltage approaching 450mV.

4.2.2 Common Mode Feedback Circuit

In practice, the output common mode level of an amplifier is not always fixed. Due to mismatches or device properties, any differences in the input common mode will be amplified and present at the output. Therefore, it is necessary to introduce a common mode feedback circuit (CMFB) to sense the difference at the output common mode and fix the variation by controlling the amplifier's bias network [39].

A basic CMFB is composed of three parts: a sensing block detecting the output common mode level, a comparing circuit which compares the sensed output common mode level to the ideal common mode level and the other block is used to deliver the feedback signal. An ideal CMFB model is shown in Figure 4.9,

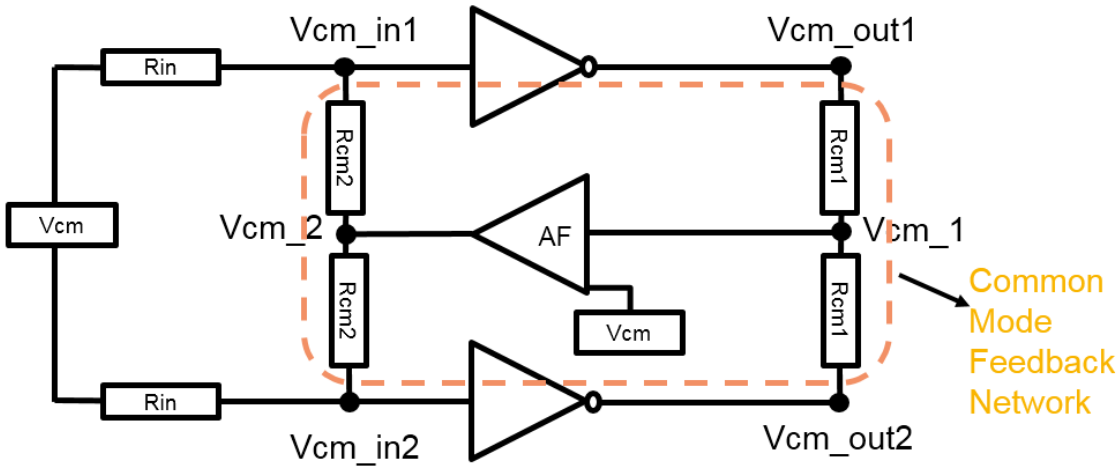

Figure 4.9: Ideal CMFB Implementation

Assuming the OTAs are with infinite gain and GBW, the sensing network can be described as,

$$V_{cm1} = \frac{R_{cm1}V_{cmout1} + R_{cm1}V_{cmout2}}{2R_{cm1}} \tag{4.21}$$

$$V_{cm1} = \frac{V_{cmout1} + V_{cmout2}}{2} \tag{4.22}$$

f R_{cm1} must be much greater than the output impedance of the amplifier to avoid loading of the OTA and lowering the loop gain. The comparing block is a positive feedback circuit and is often implemented by two inverters. The network at the input can be described as,

$$Vcm_{in} = (V_{cm} - V_{cm2})\frac{R_{cm2}}{R_{cm2} + R_{in}} \tag{4.23}$$

Eq.(4.23) describes that the input common mode of the amplifier is a portion of the difference between the ideal common mode and feedback common mode from the CMFB. For an ideal CMFB circuit, the voltage controlled voltage source is used as the amplifier in the feedback loop. From previous sections, the inverter has an intrinsic common mode of 450mV but the W/L ratio of pMOS and nMOS is not practical to design.

Before looking for the optimized parameter, it is attractive to check if the CMFB could provide some regulation range on its own. For instance, with an inverter of an intrinsic common mode few mV away from 450mV the CMFB could regulate both the input and output common mode to be back to 450mV. In that case, an analysis based on ideal CMFB is performed by varying the CMFB gain AF and error signal returning resistor R_{cm2} shown in Figure 4.9.

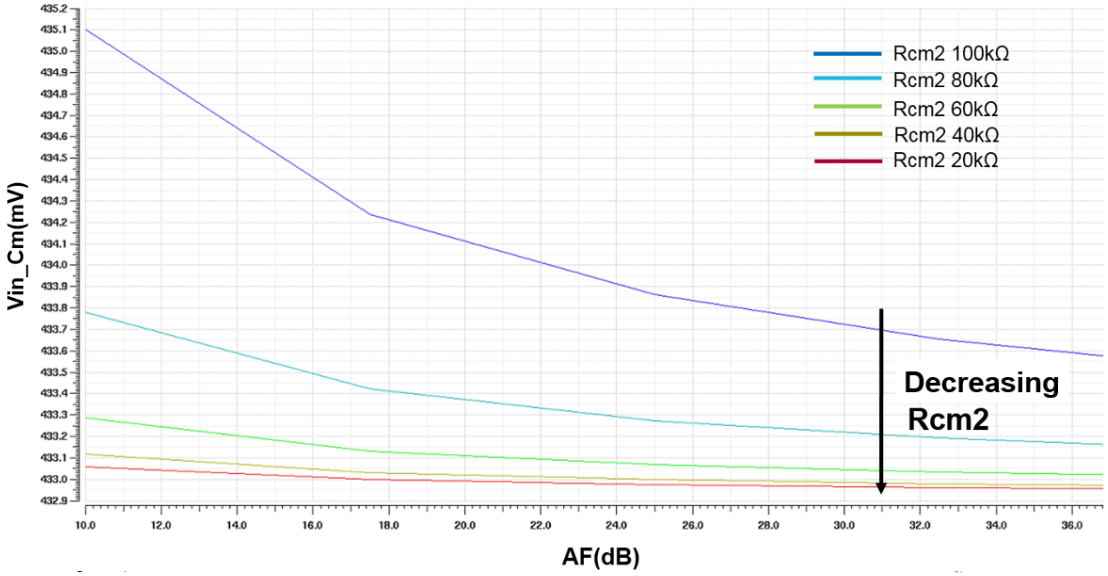

Figure 4.10: Common Mode Regulation Range Study

Figure 4.10 presents the variation of the input common mode when the amplifier gain AF is swept from 10 to 40dB. Besides, different sets of R_{cm2} from 1kΩ to 80kΩ are applied on top of that. The results show minor variations ($fewmV$) on the input common mode when both gain AF and resistor R_{cm2} are swept over a broad range. The circuit tends to maintain the output mode at 450mV by amplifying the error signal at the input.

Therefore, It is essential to design an inverter with its intrinsic common mode voltage at 450mV since the CMFB is only able to perform very limited regulation even the input common mode has been over 20mV away from the expected value.

The practical CMFB circuit is shown in Figure 4.11, a compensation capacitor is added in parallel with the resistor in the CMFB to compensate the pole from the resistor and input capacitor of the amplifier. For the two inverters in the feedback path, a finger ratio two by one is often applied. The details of implementation will be shown in the following section.

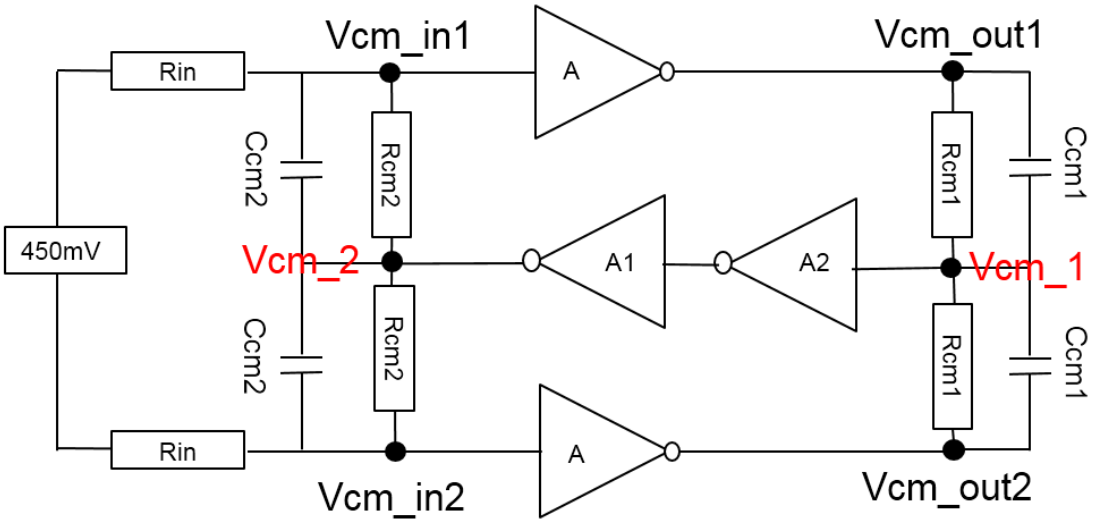

Figure 4.11: Practical CMFB Implementation

4.2.3 Four-by-four Inverter Scheme

In previous sections, the study of the inverter-based amplifier has been developed from a single inverter with ideal CMFB to real implementation. It is found that the inverter needs to achieve an intrinsic common mode value of 450mV with comparable transistor W/L ratio. However, in most cases the intrinsic common mode is away from 450mV when using transistors of similar size. It is therefore attractive to use shorter channel length L=30nm instead of L=120nm to explore the performance of amplifiers.

	Inverter1	Inverter2	Inverter3
Wp/Lp(nm)	9800/120	2800/120	1155/30
Wn/Ln(nm)	1050/120	2800/120	875/30
Gain Intrinsic(dB)	30	30	19
Gain(20k loading)(dB)	24.6	24.5	13.5
GBW(GHz)	7.2	14	38
-3dB frequency(MHz)	600	1.2	4
1/f noise(v^2/Hz) @0.22MHz/2.2MHz	4.16e-9	5e-9	2e-10
Current(uA)	64.2	66.6	100
gmp/gmn(mS)	1.25/0.55	0.9/0.9	1/0.9
Intrinsic Common Mode(mV)	450	380	450

Table 4.3: Amplifier Parameter Table

In Table 4.5, an extra column is added for inverter3. The inverter3 is using a channel length of 30nm and it achieves comparable effective gm as the other two cases. The inverter3 meets the requirements of GBW and intrinsic common mode voltage but the gain drops drastically. Recall that the gain is proportional to device channel length. It is therefore reasonable to connect four transistors with L of 30nm in series to obtain an effective L of 120nm and compensate for the loss of gain.

When connecting four transistors in series, it has been found the effective gm of pMOS and nMOS is not merely a sum of them. A small signal model of connecting four nMOS in series is shown in Figure 4.13. It is possible to derive equations by writing KCL,

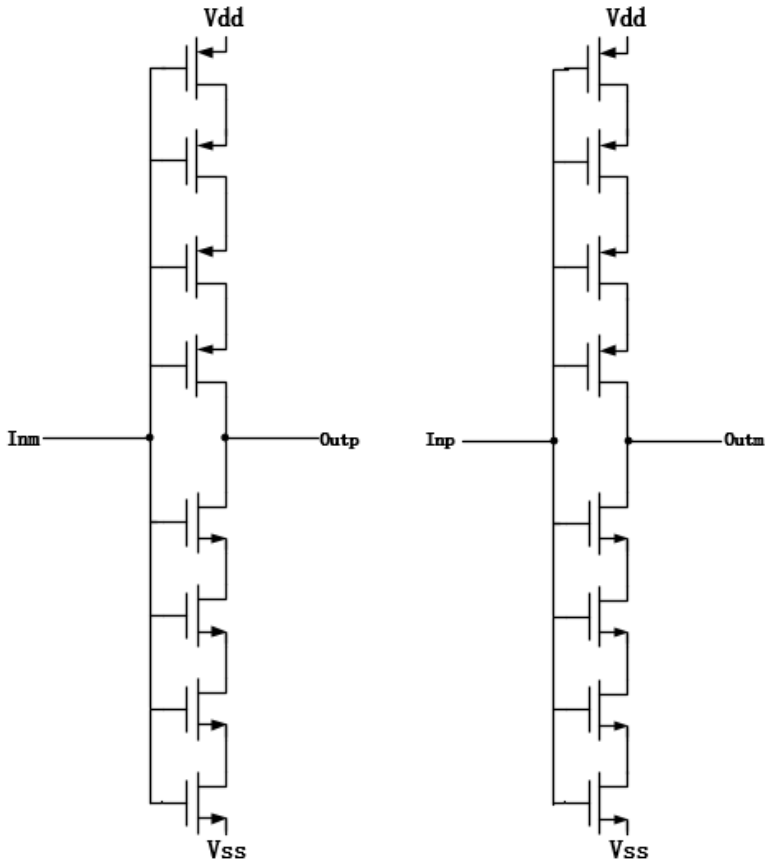

Figure 4.12: Four-by-one Inverter Structure

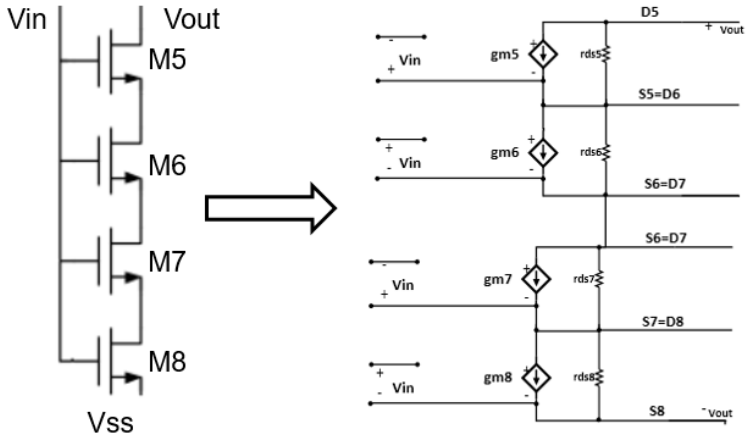

Figure 4.13: Small Signal Model of Four nMOS In Series

	Inverter1	Inverter2	Inverter4
Wp/Lp(nm)	9800/120	2800/120	1155/30
Wn/Ln(nm)	1050/120	2800/120	875/30
Gain Intrinsic(dB)	30	30	20
Gain(20k loading)(dB)	24.6	24.5	14.5
GBW(GHz)	7.2	14	18
-3dB frequency(MHz)	600	1.2	1.8
1/f noise(v^2/Hz) @0.22MHz/2.2MHz	4.16e-9	5e-9	10e-9
Current(uA)	64.2	66.6	70
gmp/gmn(mS)	1.25/0.55	0.9/0.9	0.97/0.73
Intrinsic Common Mode(mV)	450	380	385

Table 4.4: Amplifier Parameter Table

$$I_{out} - g_{m5}V_{in} = g_{ds5}(V_{out} - V_{s5}) \tag{4.24}$$

$$g_{ds5}(V_{out} - V_{s5}) + g_{m6}V_{in} = g_{ds5}V_{ds6} \tag{4.25}$$

$$g_{ds6}V_{ds6} + g_{m7}V_{in} = g_{ds7}V_{ds7} \tag{4.26}$$

$$g_{ds7}V_{ds7} + g_{m8}V_{in} = r_{ds8}I_{out} \tag{4.27}$$

And it can be noticed that the effective gm of four nMOS in series is not a linear function. The effective gm can be found by sweeping a DC signal at the input with relatively small steps, then take the output current and find its derivative. As the transconductance is defined as the ratio of the change in drain current to the change in gate voltage over a specified, arbitrarily small interval on the drain-current-versus-gate-voltage curve, the value of its derivative at Vin of 450mV can be regarded as the effective gm.

By adding extra three transistors to make four transistors in series, the DC gain has improved to some extent but not sufficient. Also, the intrinsic common mode of 450mV does not retain any more. That generally motivates the design of further stacking four transistors in parallel to make the four-by-four inverter structure. The size and inverter properties are listed in Table 4.5. The results show by stacking another four transistors in parallel with four transistors in series; the intrinsic common mode issue can be solved, also the loss of gain is compensated. Although the GBW has dropped a lot, it still meets the GBW requirement. Besides, the topology is tested over SS process corner with a temperature of 110^o, FF process corner with a temperature of -10^o and TT corner with 65^o. It can be concluded that in all three cases, the inverter performance meets the requirements of system requirements.

It is of necessities to mention that the inverter is simulated without an LDO and results show that the inverters show a low sensitivity of performance to process corners and temperature variations, where the dc gain of OTAs designed in [40] presents significant deviations across the process corners. It is a valuable asset of this design as no extra tuning circuit is required as in [41] and [31].

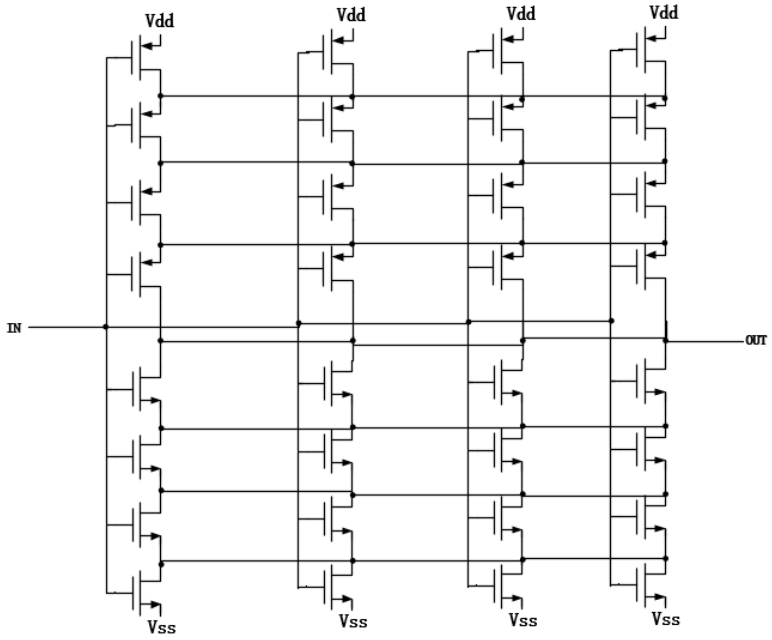

Figure 4.14: Four-by-four Inverter Structure

	Inverter1	FourbyFour(TT)	FourbyFour(SS)	FourbyFour(FF)
Wp/Lp(nm)	9800/120	1750/30	1750/30	1750/30
Wn/Ln(nm)	1050/120	875/30	875/30	875/30
Gain Intrinsic(dB)	30	28	25	27
Gain(20k loading)(dB)	24.6	23	21	22
GBW(GHz)	7.2	4.5	3	6
-3dB frequency(MHz)	600	450	300	600
1/f noise(v^2/Hz) @0.22MHz/2.2MHz	4.16e-9	9e-9	12e-10	6e-10
Current(uA)	64.2	72	50	104
gmp/gmn(mS)	1.25/0.55	0.97/0.73	0.85/0.8	0.95/0.83
Intrinsic Common Mode(mV)	450	450	450	450

Table 4.5: Amplifier Parameter Table

4.3 RC Integrator

To implement the first stage RC integrator, the value of the resistors and capacitors are chosen based on the unity gain requirement of the first integrator. The passive capacitor tuning is achieved by a capacitor bank where a fixed capacitor is connected to a programmable bank. A complementary switch has been used for controlling the capacitor bank. The pole introduced from the switch and the unit capacitor has to be made at high frequencies to avoid affecting the frequency response. The value of the main capacitor and unit capacitor is found by checking the frequency response over process corners. For instance, the main capacitor is found at first over the worst corner SS where all the switches are turned off and the capacitor value is verified by comparing the frequency response of the first stage integrator with the ideal case. After that, the FF corner can be checked in the similar way where all the switches are ON and the capacitor bank delivers the maximum capacitance. Finally, the TT corner is double checked.

	temperature	Binary bits
TT corner	65°C	01010
SS corner	110°C	00000
FF corner	−10°C	11111

Table 4.6: Integrator Capacitor Bank

The application is examined by checking the GBW of the integrator together with the phase shift at $\frac{f_s}{2}$. Figure 4.15 and Figure 4.16 presents the comparing curves of the frequency and phase response of the first RC integrator in the ideal case and under three corners. Due to limited DC gain of the amplifier and extra poles and zeros introduced from implementation, the ideal 1^{st}-order response corresponding to constant 90° has been changed. It can be noticed that in the gain response, the curve sees a peak at around the resonance frequency of the following biquad filter and this is not shown in the ideal curve, this is due to the coupling mechanism from the passive summation node since by replacing the passive summation with an ideal summer, the peaking can be removed. The similar mechanism is recognized in the phase plot as the phase drops by 360^o at the resonance frequency. The phase shift at $\frac{f_s}{2}$ is summarized in Table 4.7 with the worst case 25° away from the ideal case. Recall that the extra phase shift could make the ΣΔ modulator system unstable but the phase response of the integrator is proved to be okay based on the phase response of the complete loop filter presented in Section 4.6.

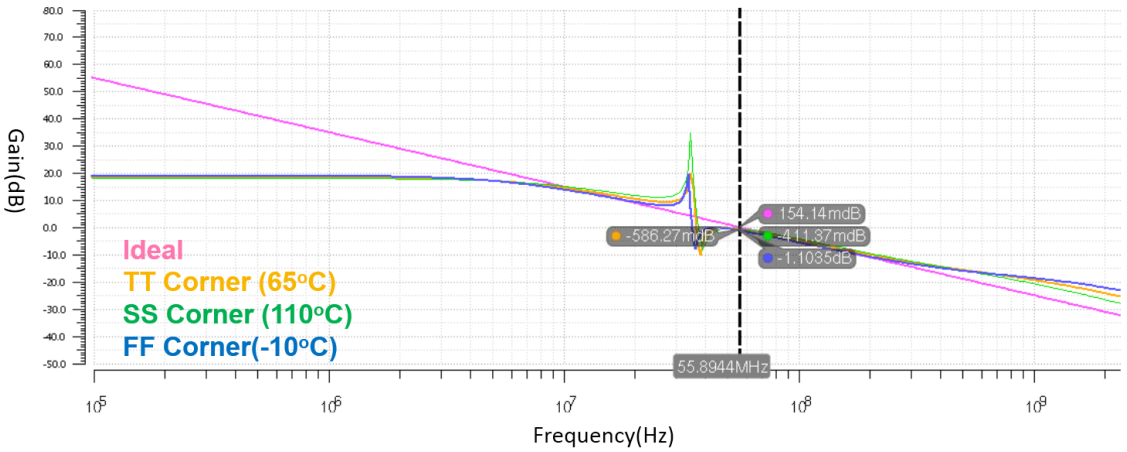

Figure 4.15: Amplitude Response of the RC Integrator

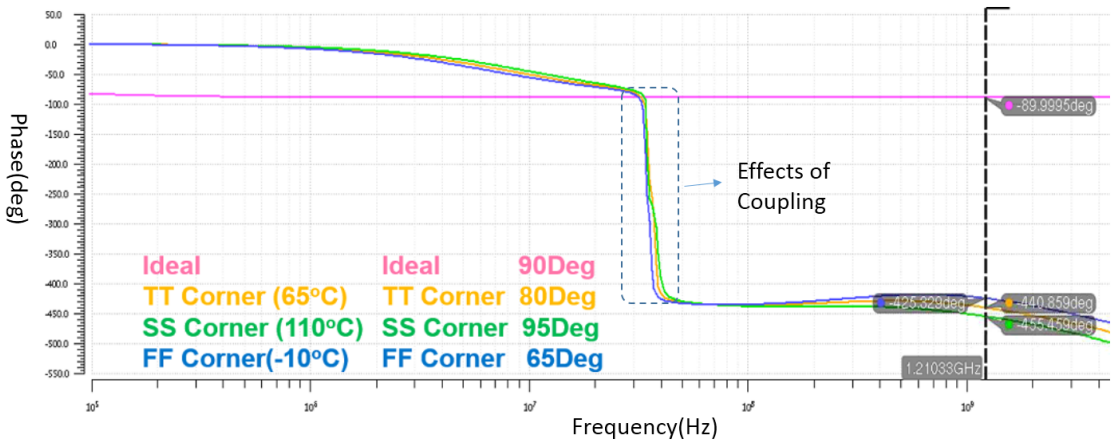

Figure 4.16: Phase Response of the RC Integrator

	phase shift @ $\frac{f_s}{2}$
Ideal	$-90°$
TT corner	$-80°$
SS corner	$-95°$
FF corner	$-65°$

Table 4.7: Phase Shift of the RC Integrator at $\frac{f_s}{2}$

It is also of necessities to check the stability of the CMFB over process corners. The way to test the CMFB stability is by breaking the CMFB loop and switching the input to zero. In that way, the stability of CMFB can be measured by examing the gain and phase margin of the CMFB loop. It is often required to have a phase margin over 60^o to ensure a stable design. The results of the CMFB stability is shown in Figure 4.17 and concluded in Table 4.8, the CMFB is found to be stable over three corners.

	gain margin	phase margin
TT corner	40dB@3.4GHz	72^o@114MHz
SS corner	35dB@3.4GHz	71^o@192MHz
FF corner	38dB@1.3GHz	70.5^o@70MHz

Table 4.8: CMFB Stability Summary of OTA1

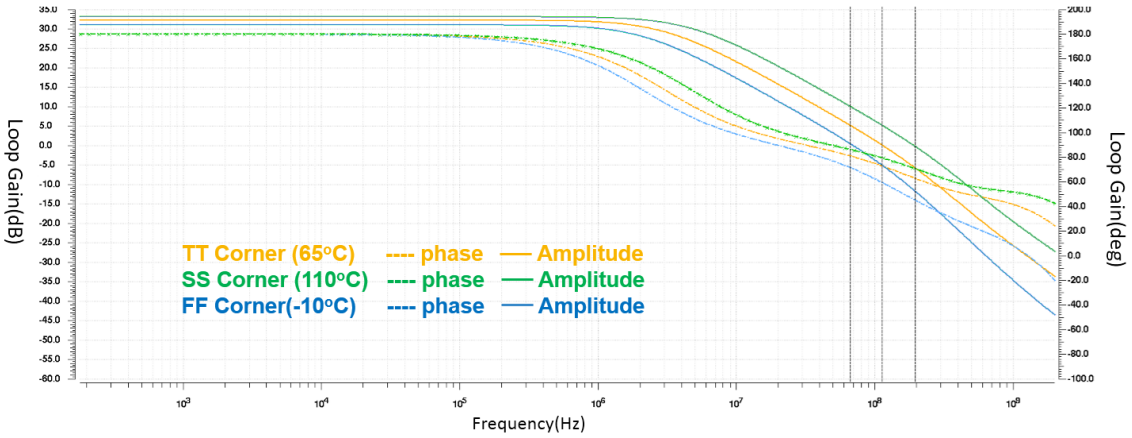

Figure 4.17: CMFB Stability Check of OTA1

4.4 Single Opamp Resonator

As has been presented in Section schematic overview 4.1, capacitors Cn and Cp in the feedback path are carried out by capacitor banks for compensating technology spread. The way to find the primary capacitor and unit capacitor follows the method mentioned for RC integrator. The design is checked over three process corners with specific order. The worst corner SS is first checked by tuning the capacitor bank with minimum capacitance where all the switches are open. Then the FF corner gives the value of unit capacitor when all the switches are closed. When both capacitors are found, the resonator is reviewed over TT corner.

	temperature	Binary bits
TT corner	−65°C	01010
SS corner	110°C	00000
FF corner	−10°C	11111

Table 4.9: Capacitor Bank Biquad

Figure 4.18 and Figure 4.19 compares the frequency and phase response of the single-opamp resonator in three corners with ideal case. In the ideal case, the opamp is with enough gain also with GBW set to infinite. The verification process checking the location of the resonance as well as the phase shift at $\frac{f_s}{2}$. The result is summarized in Table 4.10. In TT corner, the phase shift at $\frac{f_s}{2}$ is over 30◦ away from the ideal case. It looks like an issue for causing instability but latter in Section 4.6, the simulation results of the complete loop filter shows the phase response of the complete loop filter is acceptable based on the simulation result in Figure 4.22.

	phase shift @ $\frac{f_s}{2}$
Ideal	−180°
TT corner	−216°
SS corner	−250°
FF corner	−190°

Table 4.10: Phase Shift of the Biquad at $\frac{f_s}{2}$

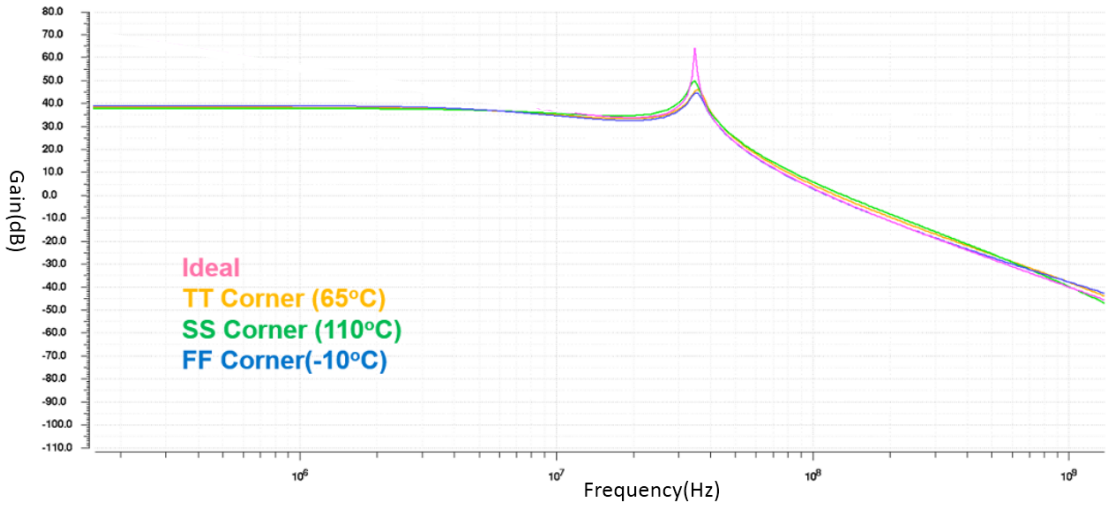

Figure 4.18: Gain Response of Biquad Loopfilter

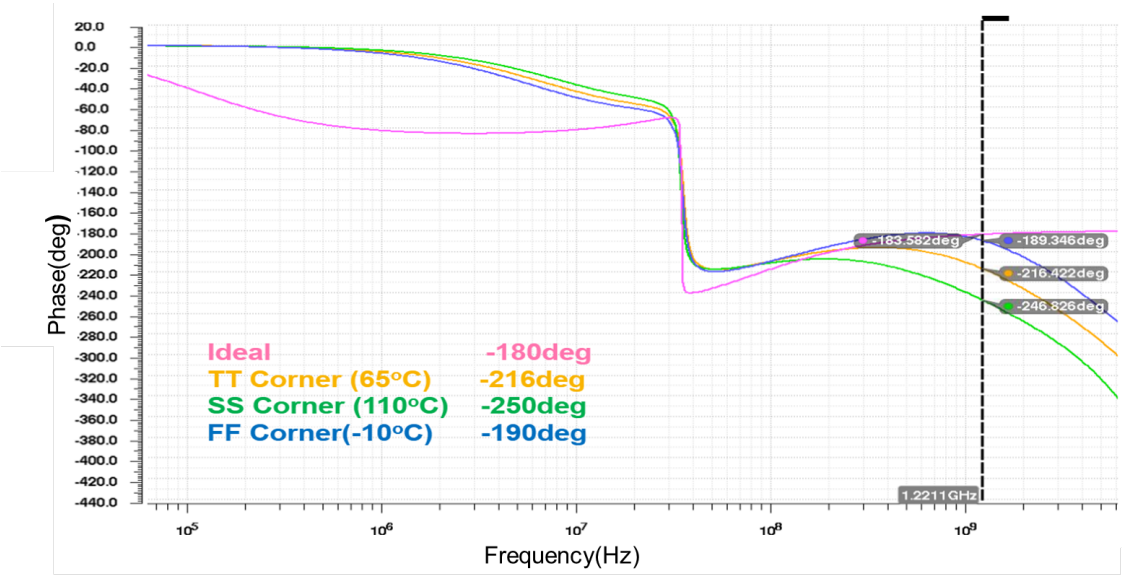

Figure 4.19: Phase Response of Biquad Loopfilter

4.5 3^{rd}-order Loop Filter

In this section, the implementation of the 3^{rd}-order loop filter is examined. As the loop filter is the combination of a first stage RC integrator and a single-opamp resonator, therefore the response of the complete loop filter should be the combination of both. Figure 4.20 and Figure 4.21 present the gain and frequency response of the loop filter. The simulation of the gain response over three corners shows some deviation from the ideal curve as a result of the loss of DC gain when implementing the amplifiers as well as the implementation of passive summer. But the resonance peak is aggressive enough and the location is approximately the same as ideal case as the peak is only dependent on the values of R and C. The results can be double confirmed by examining the phase response. It can be noticed that all four curves have a phase shift of $-180°$ at the resonance frequency. However, the total phase shift at $\frac{f_s}{2}$ show some discrepancy. The results are summarized in Table 4.11. Although there is a $24°$ deviation of phase shift at FF corner, the system is still found to be stable based on the simulation results shown in Figure 4.22. This simulation introduces extra phase shift at $\frac{f_s}{2}$ by intentionally introducing a pole in the loop and the results are found based on the $\Sigma\Delta$ modulator system simulation. The results in Figure 4.22 concludes that the system can handle $29°$ more phase shift at $\frac{f_s}{2}$ without loss of ENOB. Therefore, the simulation results of the loop filter response are acceptable and should produce stable outputs when running in the modulator system.

	phase shift @ $\frac{f_s}{2}$
Ideal	$-94°$
TT corner	$-100°$ $(6°)$
SS corner	$-114°$ $(20°)$
FF corner	$-86°$ $(-8°)$

Table 4.11: Phase Shift of the Loopfilter at $\frac{f_s}{2}$

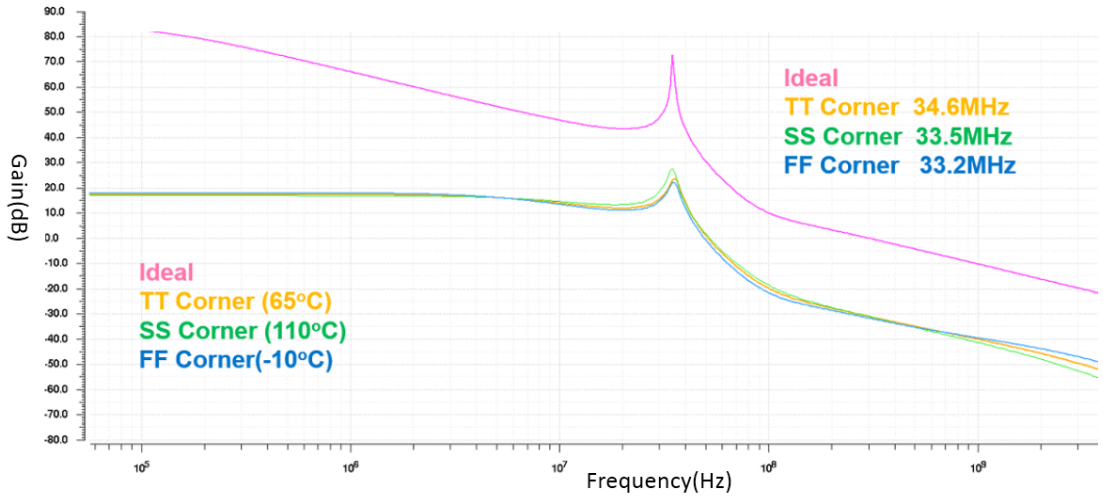

Figure 4.20: Gain Response of the 3^{rd}-order Loopfiler with Single Opamp Biquad

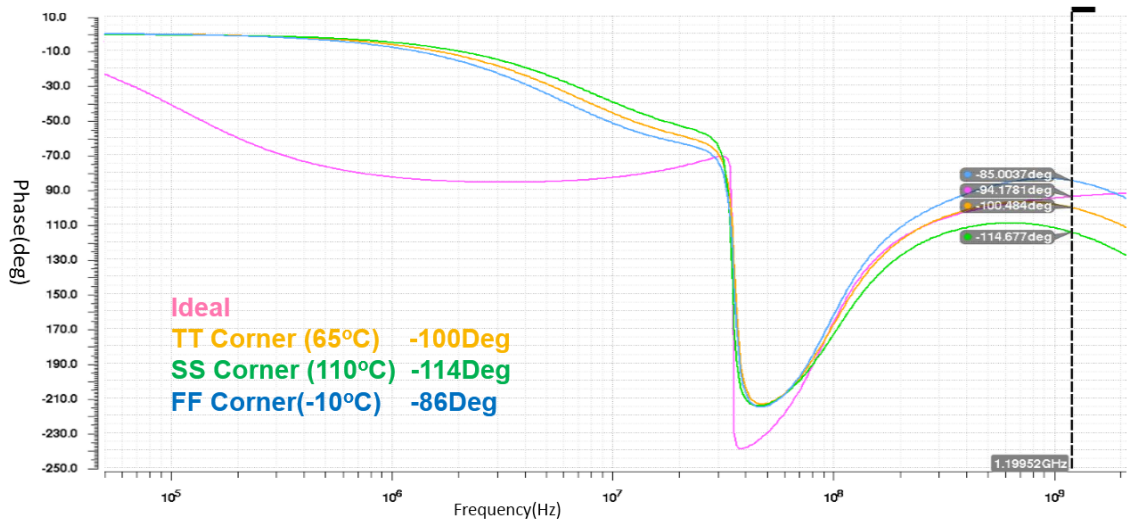

Figure 4.21: Phase Response of the 3^{rd}-order Loopfiler with Single Opamp Biquad

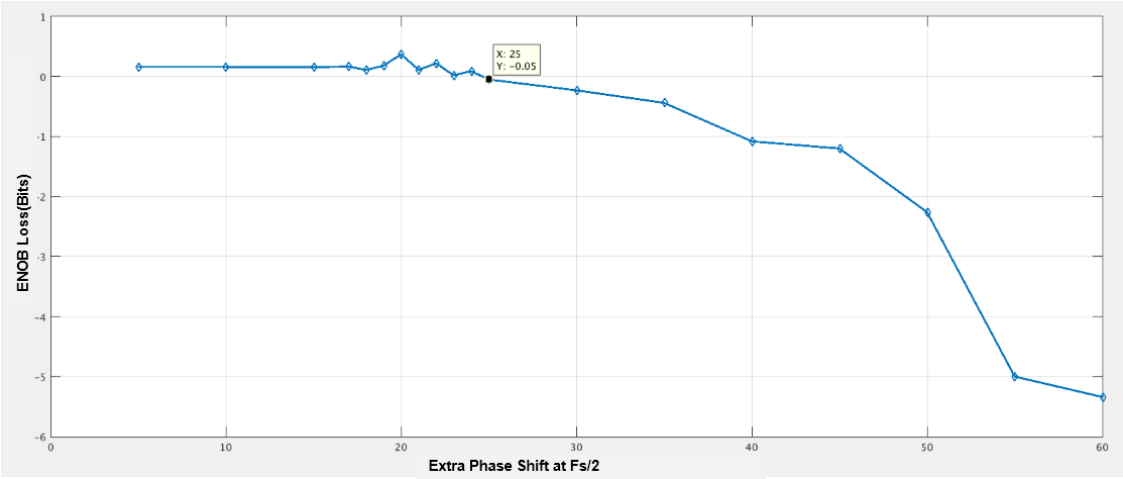

Figure 4.22: ENOB Loss vs Extra Phase Shift at $f_s/2$

4.6 Passive Summation and ELD Compensation

Often an active summer is employed for summing the outputs of integrators to the input of the quantizer [33]. The application of the active summer introduce extra opamps and opamps consume a lot power [32]. It is therefore more power efficient to use passive summation as is shown in Figure 4.23.

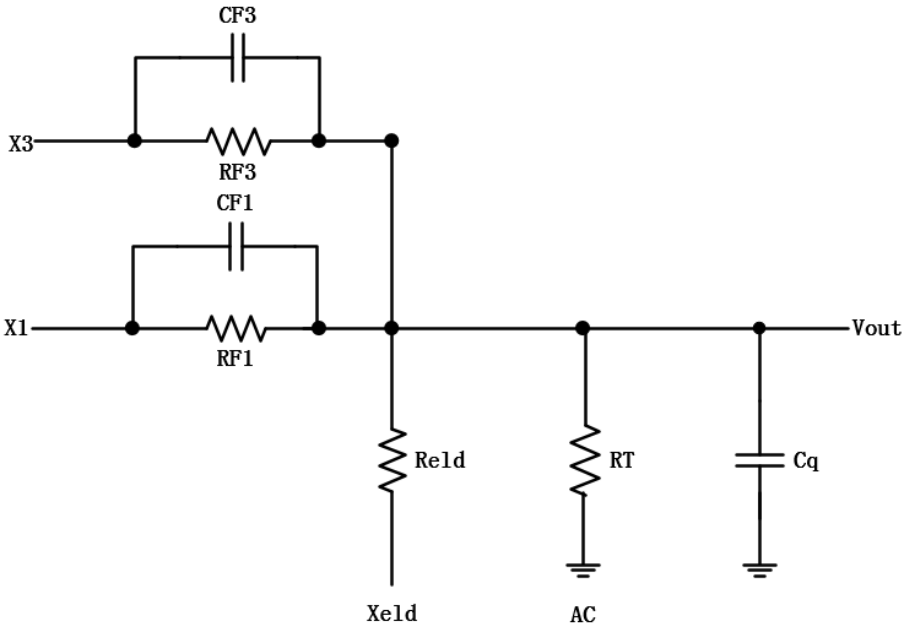

Figure 4.23: Implementation of the Passive Adder

The feed-forward coefficients A1, A2, A3 and ELD coefficient C have been found from system level design and listed in Table 4.12. Since passive summation is employed, the coefficients are realized by controlling the resistance ratio of the resistors. Hence the output of the summer can be expressed as a sum of the output of the first integrator, the output of the biquad and the output of the quantizer scaled by ELD coefficient,

$$V_{out} = A1 \cdot X1 + A3 \cdot X3 - A_{ELD} \cdot Xeld \tag{4.28}$$

Where the coefficients ratio are defined as,

$$\frac{A1}{A3} = \frac{Rf3}{Rf1} \tag{4.29}$$

$$\frac{A1}{Aeld} = \frac{Reld}{Rf1} \tag{4.30}$$

The sum of the coefficients is greater than unity which is not practical to achieve when using ratio-based passive summation. The effective coefficients are in fact a scaled value of the sum of three coefficients 4.33, but the gain of the quantizer compensates the loss of gain.

$$|A1| + |A3| + |Aeld| > 1 \tag{4.31}$$

$$|A1| + |A3| + |Aeld| = 9.15 \tag{4.32}$$

$$a1 = \frac{A1}{9.15}, a3 = \frac{A3}{9.15}, aeld = \frac{Aeld}{9.15} \tag{4.33}$$

The construction of the passive adder is shown in Figure 4.23. An extra termination resistor RT is introduced in parallel with the input capacitor of quantizer. The verification process compares the frequency response at node X1 and X3. Note that the existence of parasitic capacitor Cq from the quantizer and a pole could be generated from the Rf1, Rf2 and Cq pair. Therefore, it is necessary to compensate the pole by adding a capacitor in parallel with Rf1 and Rf2. The value of the resistors and capacitors used have been listed in Table 4.13.

Coefficient	Value
A1	5.48
A2	2.57
A3	2.73
c	0.94

Table 4.12: Feedforword and ELD Coefficients

Coefficient	Value
Rf1	20kΩ
Rf3	40kΩ
Reld	151kΩ
RT	4kΩ
Cf1	1f
Cf3	0.5f
Cq	5f

Table 4.13: Resistors and Capacitor Values in the Summer

4.7 System Transient Results

In this section, the CT ΣΔ modulator loop is completed by adding a VerilogA based ideal quantizer and a resistive DAC. The resistive DAC is chosen as it is more power-efficient than the current-steering DAC. The transient simulation is performed over three corners; the results are extracted and plotted by Matlab scripts. The results are summarized in Table 4.14. It can be found that at SS corner, the system achieves an ENOB around 1 bit less than the design target. In other two corners, the results are closer to the expected within the acceptable range. The simulation result in Figure 4.25 shows the FFT spectrum for SS corner, the notch is not as visible as in two other cases. But at all three corners, the power target is met and the low power design goal is followed well.

Corners	ENOB(bits)	SNDR(dB)	HD3(dB)	Power(mW)
Target	10.8	66.78	68	<1
SS	10	61.96	71	0.41
FF	10.65	65.88	71	0.78
TT	10.7	66.17	73	0.53

Table 4.14: System Performance Table

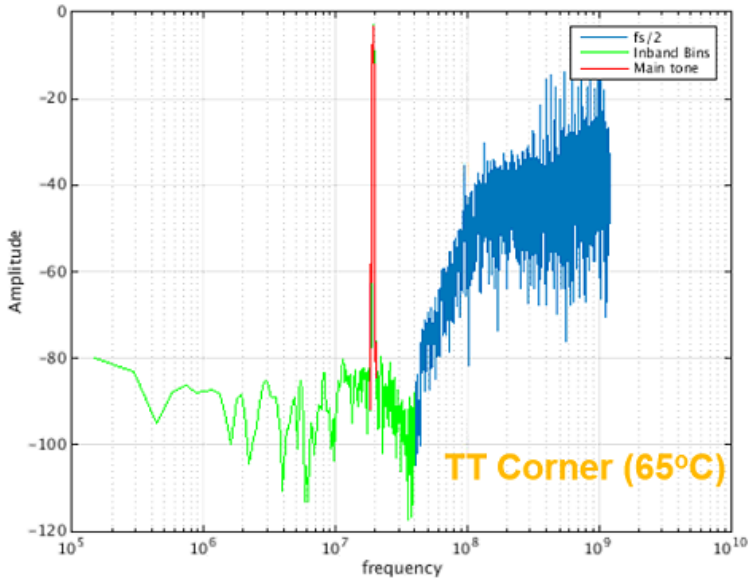

Figure 4.24: FFT Spectrum for TT Corner

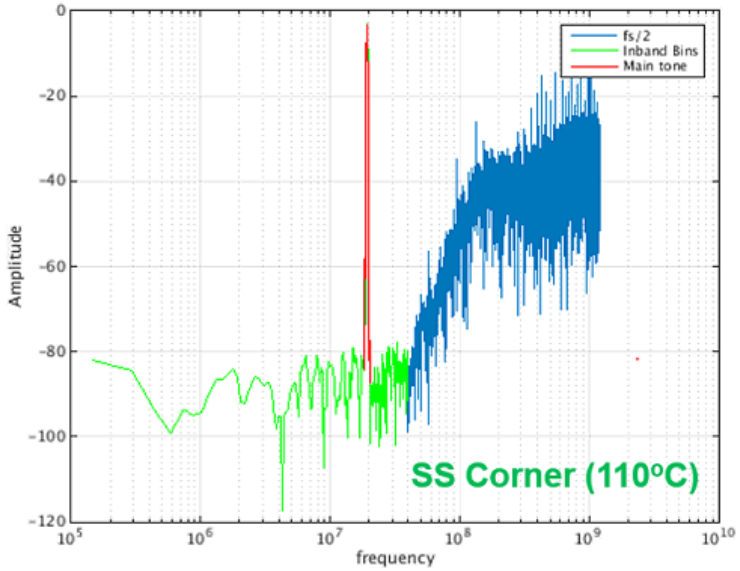

Figure 4.25: FFT Spectrum for SS Corner

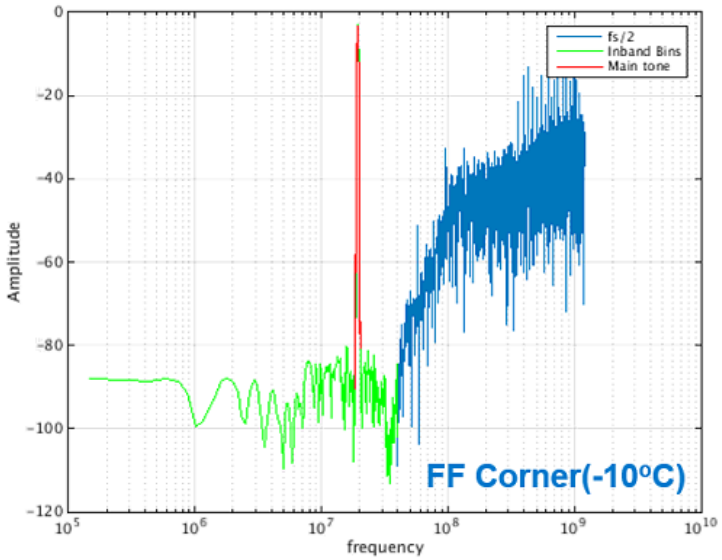

Figure 4.26: FFT Spectrum for FF Corner

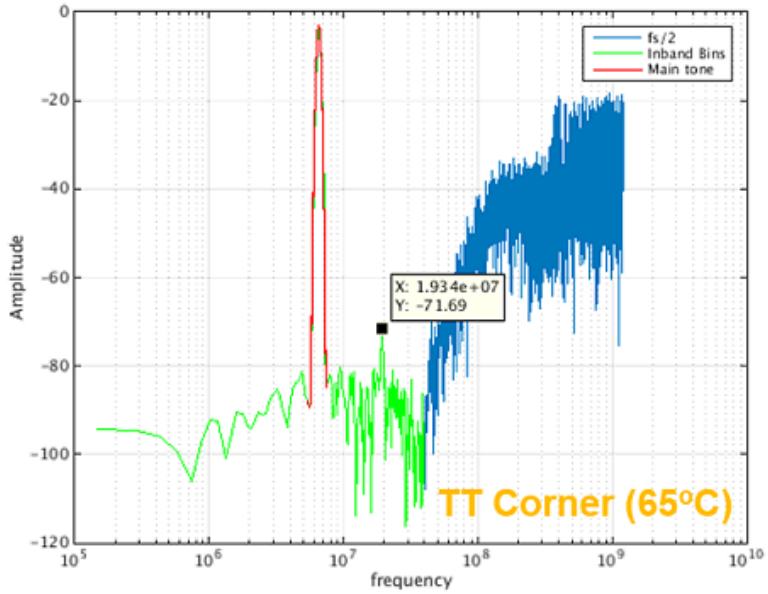

Figure 4.27: HD3 Test for TT Corner

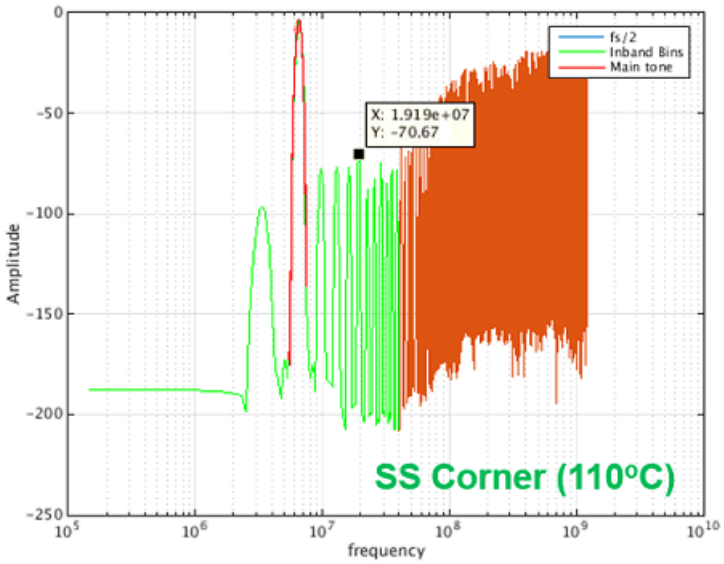

Figure 4.28: HD3 Test for SS Corner

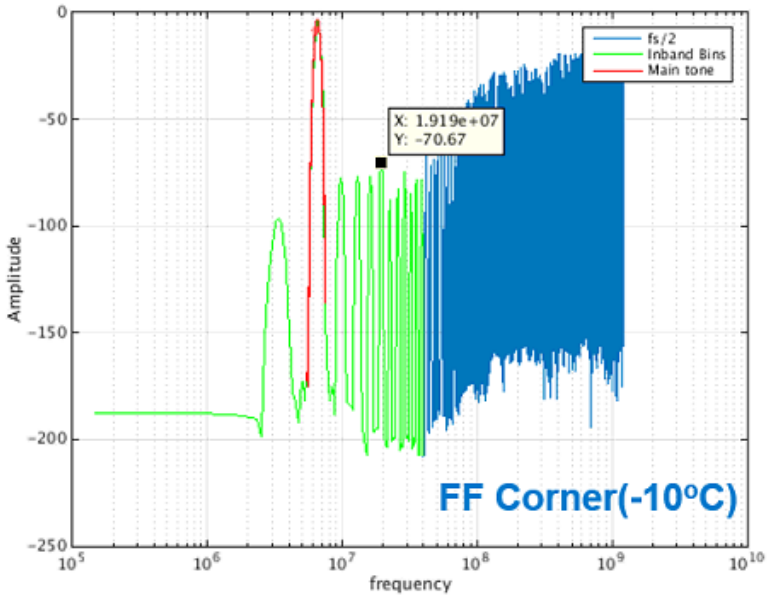

Figure 4.29: HD3 Test for FF Corner

4.8 Summary

The implementation of the loop filter of a 40MHz 3^{rd}-order CT has been shown in this chapter. The loop filter was designed with a first stage RC integrator and a single-opamp resonator. Inverter-based amplifiers are used for minimizing the power dissipation and area. A fourbyfour inverter structure has been proposed and it is constructed by putting four pairs of inverters in a kind of matrix form. The designed inverter can meet the OTA requirements from the system level design and the device ratio ensures a compact design. A detailed comparison of different inverter topology and their performance were given in this chapter. Passive summation is used due to its low power property. Furthermore, the loop filter design was examined over three process corners, SS FF TT with different temperatures. The verification process is taken by comparing the frequency response of the integrator, resonator and complete loop filter to the ideal curve respectively. To have a complete system transient simulation, the quantizer is realized by verilogA code, and resistive DAC has been used for the concern of a low power design. The system is found to attain an ENOB of 10bits which is equivalent to an SNDR over 62dB. The HD3 measured is beyond 71dB over three corners while consuming only 0.4mW power consumption.

Chapter 5

Conclusions

5.1 Contributions

In my thesis, the ADC theory and implementation of the loop filter in a CT $\Sigma\Delta$ modulator has been presented. The realization of a low power 3^{rd}-order loop filter is developed based on conventional loop filter structures with chains of RC integrators and improved by using an integrator and a single opamp resonator instead of three active RC integrators. Inverter-based amplifiers are employed considering the power efficiency and a four-by-four inverter structure with minimum length transistors are designed due to the overall consideration for system non-idealities such as noise, non-linearity, and power.

To obtain a lower power and high-resolution $\Sigma\Delta$ modulator sampling at GHz, the structure of the loopfilter described in Chapter 4 was proposed by my supervisors in NXP, Prof.Lucien Breems and Prof.Muhammed Bolatkale. I was supervised to study the conventional 3^{rd}-order loopfilter and inverter-based amplifiers. My supervisors directed me to design the loopfilter with a single opamp resonator and the four-by-four inverter structure was suggested to have comparable performance as obtained from a single inverter pair while achieving a more compact design.

- I have derived the Matlab model for studying the first stage concerning specifications (noise, non-linearity, and power). The modeling of the blocks from the ideal integrator to the complete loopfilter with nonideal opamps have been developed.
- The specifications of OTAs in the loopfilter have been defined by sweeping the gain and GBW of each OTA separately.
- Different inverter based amplifiers have been studied under two different CMOS processes (120nm & 28nm) and with different constructions. An inverter structure consists of four inverters in series with four inverters in parallel was proposed and it has been proved to be robust over three process corners.
- The common mode feedback circuit was studied in detail about its theory, ideal model and implementation. I have also checked if the CMFB could provide some regulation range. In the CMFB loop, frequency compensation topology has been employed to ensure a stable work.

5.2 Summary

The thesis started with the background of the Bluetooth application in Chapter1. The advancing of Bluetooth technology makes the design of the ADC in the Bluetooth low energy receivers more challenging as the signal bandwidth has been increased to 40MHz. Also, the design of high resolution, low power ADCs are essential as it is the major contributor to the power budget. The thesis continued with a survey of ADCs for high resolution, low power 40MHz bandwidth application based on ADC performance survey by Murmann. The CT $\Sigma\Delta$ modulator is chosen due to its high dynamic range and low power properties. With system specifications of 66.7dB SNDR and oversampling ratio 30, a single-bit 3^{rd}-order CT $\Sigma\Delta$ with feedforward summation and local resonator feedback was purposed. Section 1.3 gave a clear motivation of this work and the specifications of the ADC system was listed in section 1.4.

In Chapter 2, the fundamentals of analog to digital conversion was given. The theory was then expanded by introducing the mechanism of oversampling, noise-shaping and a sigma-delta loop. For achieving better noise performance without increasing the oversampling ratio on a broader bandwidth, the order of the loop filter should be improved. Nonetheless, to have a stable oscillation at the half sampling frequency, the higher-order behaviour of the loop filter should turn back to first order at high frequency hence certain compensation techniques such as feedforward, feedback and feedforward with local feedback are discussed in Section 2.2.4.

To obtain the design requirements of blocks in the loop filter, the modelling of OTAs and loop filter was studied in Chapter 3. The frequency behavior of the 3^{rd}-order loop filter with feedforward summation and local resonator feedback was presented. Since the power of the amplifiers is known to be the bottleneck in the loop filter power budget, a single-opamp biquad is introduced for saving one opamp while having the same resonance. The modeling of loop filter can help appreciate the behavior of the loop filter before implementation. It is possible to introduce non-idealities such as limited gain, gain bandwidth of the OTAs, technology spread of passive device and excess loop delay to the system and see how system response to these non-idealities. The first stage integrator of the loop filter is dominant in thermal noise, nonlinearity and power of the loop filter. From the nonlinearity model, the transconductance gm of OTAs was required to be higher than 1.8mS and this help defines the input resistance of integrators as gm as well as total noise budget has been fixed. The DC gain of the first stage was required to be higher than 26dB while 20dB for the second OTA. The GBW of two OTAs should be higher than 2GHz and 1.5GHz respectively. Besides, five-bits capacitor banks were necessary to compensate the technology spread of passive device.

Chapter 4 gave the details of the implementation. An in-depth study of inverter was presented first with a device channel length of 120nm. It was found that to have an intrinsic common mode at half the supply voltage, the device ratio of pMOS has to be over ten times greater than nMOS. The nMOS is so small that it could contribute lots of flicker noise which is the main source of noise at low frequency. Otherwise, the device has to be made bigger but that trade lower flicker noise for more power. The study of CMFB concludes the necessity of designing an inverter with intrinsic common mode voltage at half supply voltage since the CMFB is only able to provide a very limited regulation range. The design of the inverter was then developed with 28nm HPC for better performance and a four-by-four inverter structure was designed for meeting the design requirements and with a comparable device size ratio. Then the loop filter was implemented and frequency response of the first stage RC integrator, the single-opamp biquad and complete loop filter with passive summer were obtained. As is the main sign of a stable system, the phase shift at $\frac{fs}{2}$ was checked and the loop filter shows extra phase shift which is acceptable based on the system requirement. Furthermore, the sigma-delta loop was completed by designing the quantizer in VerilogA and ideal DAC. The system can achieve the best 10.7bits ENOB at TT corner and the worst case 10bits at SS corner. Compared to the design target of 10.8bits, the performance at TT and FF corner can be regarded as acceptable while further improvements are needed for

SS corner. However, the power dissipation at three corners meet the design hence the low-power design is well-followed.

5.3 Benchmark

	Specifications	Simulated (TT)	[4]	[42]
ENOB	10.8bits	10.7bits	11.9bits	10.9bits
SNDR	66.7dB	66.21dB	73.6dB	67.5dB
Bandwidth	40MHz	40MHz	18MHz	25MHz
Sampling frequency	2.4GHz	2.4GHz	640MHz	500MHz
Power of the loop filter	<1mW	0.53mW	3.5mW	3.59mW
Power of the modulator	<1mW	≈1mW	3.9mW	8.5mW
FoM	8fJ/conv	8fJ/conv	28fJ/conv	88fJ/conv

Table 5.1: System Performance Comparison Table

Table 5.1 has summarized the performance of the designed system and the state-of-the-art are listed for comparison. Generally speaking, the simulated results meet the design target and it outperform the best reported ΣΔ ADC by far. In [4], the power dissipation of the loop filter takes over 90% while it is around 50% in our design. But notice the simulation result of the loop filter is only pre-layout verification, also the total power of the modulator is based on an estimation of power dissipation of the quantizer and potential extra tuning circuit.

Specifications	Expected	Simulated (SS)	Simulated (FF)	Simulated (TT)
gm	1.8mS	1.65mS	1.78mS	1.8mS
DC gain	26dB	25dB	27dB	28dB
GBW	2GHz	3GHz	5GHz	6GHz

Table 5.2: OTA Performance Comparison Table

5.4 Improvement

- If time allows, the implementation of the comparator can be added to make a complete ΣΔ modulator design. It would help to better understand the ΣΔ system and analysis the non idealities introduced from the quantizer.
- Also, the schematic design can be laid out to see the effects of parasitics and it is of necessity to check the post-layout simulation is as expected.
- Although the resistive DAC is linear in theory, it is useful to check if the resistive DAC is robust to clock jitter as clock jitter could generate extra noise at the input of the modulator.

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