BI-DIRECTIONAL TUNING OF JOSEPHSON JUNCTION RESISTANCE

Master thesis

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Nothing has such power to broaden the mind
as the ability to investigate systematically and truly
all that comes under thy observation in life.

Marcus Aurelius

ABSTRACT

One of the main components used in superconducting quantum chips is the Josephson junction. Currently when fabricating Josephson junctions, the resistance uniformity at wafer-scale is not optimal. It is also known that an annealing process can alter the junction resistance and with it the qubit frequency. However, laser annealing has only shown to be able to increase the junction resistance. An equally effective and minimally invasive technique to decrease junction resistance is necessary to have full control on frequency targeting. Thermal annealing in a reducing environment is known to result in a global decrease in junction resistance. To get better control on frequency targeting the techniques could be combined. A die containing not-capped Manhattan type Josephson junctions has been annealed using forming gas at 200 °C for 2 minutes, based on a non-linear least squares reciprocal function fit to the data an asymptotic lower bound of 467 $\mu S \mu m^{-2}$ for the change in conductance per unit area has been found. Smaller junctions with an area of approximately 0.03 μm^2 undergo a bigger change in conductance per unit area of around 800 $\mu S \mu m^{-2}$. Annealing at higher temperatures such as 300 and 400°C results in a decrease of the conductance. There is no substantial change in yield of usable SQUIDs when using a rapid thermal annealing process.

ACKNOWLEDGEMENTS

This endeavour would not have been possible without Nandini Muthusubramanian my daily supervisor, her knowledge and expertise that she shared with me during the project have been invaluable in this journey. I also appreciate her patience in guiding me to become a better scientist and teach me the ways of the cleanroom, or how she jokingly likes to call it the "sweatshop." The numerous conversations we have had, both on and off topic ensured that I was in the right hands to write this thesis.

I am also extremely grateful to Leonardo DiCarlo, my responsible thesis supervisor. Or as most people know him: Leo! I first met Leo during the fundamentals of quantum information course project. It was there that my interest in the realization of quantum algorithms through creatively designed superconducting circuits started to grow. His constructive feedback and oversight during the project have steered me in the right direction during the project. I want to thank him for allowing me the chance to experience what it is like in academia. Both in the lab with a cup of coffee or while enjoying a beer down in the basement bar.

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OUTLINE

The goal of this project is to demonstrate bi-directional tuning of Josephson junction (JJ) resistance. This project is carried out to obtain the title of Master of Science at the master's program Applied Physics, track: Physics for Quantum Devices and Quantum Computing, provided at Delft University of Technology.

The experiments carried out in this project were first thought about by my supervisor Nandini Muthusubramanian. She supervised others before me and the project described here is an extension of the findings and outstanding goals which remained to be addressed from the earlier research projects "Wafer-scale fabrication of Josephson junctions" [1] and "Improving Frequency Targeting of Transmon Qubits Through Automated Laser Annealing" [2].

Josephson junctions are a key component in superconducting qubits as they behave as a non-linear inductor. The fabrication of superconducting qubits is compatible with current CMOS technology, which makes it one of the promising candidates for fault-tolerant quantum computing. This has also resulted in widespread adoption by industrial players like IBM and Google [1]. Josephson junctions are made of a three-layered stack of materials with a weak link sandwiched between two superconductors, resulting in a superconductor-insulator-superconductor (SIS) junction. Josephson junctions should be able to conduct without any dissipation below the critical temperature T_c of the material, since Cooper pairs should be able to quantum mechanically tunnel through the barrier. Any defects in the weak link or the interfaces between the metal leads and the barrier will impact the operation of the junction.

The materials used to form the junctions will be Al as a superconductor and AlO_x for the tunnel barrier. For this AlO_x a phenomenon called aging has been identified that refers to the change of the tunnel barrier during heat treatment [1]. In a paper written by Pop *et al.* [3] they distinguish two phenomena that they associate with junction aging. Diffusion of oxygen from the tunnel barrier to electrodes or possibly absorption and desorption of other atoms or molecules. Unintended aging during fabrication processes is currently a limiting factor for batch-to-batch reproducibility of junction resistance. Therefore, it is worthwhile to investigate the factors which influence the AlO_x tunnel

barrier with the goal of gaining more control over frequency targeting of qubits.

Achieving frequency targeting on multi-qubit devices such as Surface-17 developed at the DiCarlo lab is one of the important goals towards realizing fault-tolerant quantum computing. Prior research by the project supervisor (N. Muthusubramanian) has led to insights on factors which affect the uniformity of Josephson junction resistance when fabricated at wafer-scale [1]. The implications of these findings are that there are certain fundamental constraints on reducing the spread of junction resistance as the chip size increases. This necessitates the development of other strategies to modify the qubit frequencies. A detailed understanding on the reordering of the AlO_x tunnel barrier due to temperature and environmental changes is therefore necessary [4–7].

By utilizing an annealing process, the junction resistance can be altered [8–11]. Laser annealing has already been demonstrated as an effective non-invasive technique for selectively tuning junction resistance [8–10]. The caveat with laser annealing is that it has been demonstrated to only be capable of dialling down qubit frequencies, meaning junction resistance can only be increased with this method. Therefore, an equally effective and minimally invasive technique to decrease junction resistance is necessary to have full control on frequency targeting.

Thermal annealing in a reducing environment such as forming gas (90% N_2, 10% H_2) is known to result in global decrease in junction resistance [11]. Now we can consider that it is beneficial to take advantage of both techniques. First a baseline resistance alteration is made using a global rapid thermal anneal. Thereafter, the junction resistances could be further changed locally using the laser annealing process.

This thesis contains 5 chapters, in the next chapter an overview of relevant theory is given. After that materials & methods can be found in chapter 3. There the processes to fabricate devices and anneal them are described, the method used to measure junction conductances is also reported. Chapter 4 contains the results, and these are also discussed, based on the results certain effects are observed and analysed, possible origins of these phenomena are also proposed. At the end the conclusions drawn from this project are summarized and an outlook is given, some new questions are raised and for now still left unanswered.

2

PRIOR LITERATURE

In this chapter some basic concepts are reiterated. For those who are entirely new to *qubits* or would like a refresher a brief introduction can be found in appendix A. A more in-depth description of some of these topics can be found in for example "Quantum computation and quantum information" [12]. Later, in this chapter more advanced concepts pertaining to the project are discussed.

2.1. JOSEPHSON JUNCTION

To establish a physical qubit some quantum system which has at least two states available is required. If the spacing between the energy levels of these states is distinguishable specific state transitions can be more easily driven.

An essential component of a superconducting qubit is the Josephson junction. It is named after the physicist Brian David Josephson who first correctly described the tunnelling current for these junctions for which the Nobel Prize in Physics was awarded to him in 1973 [13]. The Josephson junction consists of two metal electrodes connected with each other via some barrier, in this example a thin insulator such as an oxide barrier as can be seen in figure 2.1.

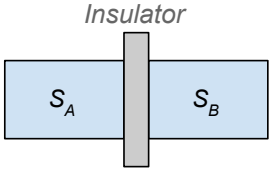


Figure 2.1: Simple schematic of a Josephson junction.

Below a certain temperature, called the critical temperature T_c, the metal becomes superconducting resulting in the formation of Cooper pairs, a quasiparticle formed by

2

two electrons that couple due to an attractive force mitigated by the electron-phonon interaction [14]. This coupling is only noticeable at certain environmental conditions such as extremely low temperature. The Cooper pairs inside the two superconducting electrodes condense into a macroscopic quantum state. The state of each condensate can be described by a single condensate wave function Ψ. These are written as:

$$\Psi_A = |\psi_A| e^{i\phi_A} \quad \text{and} \quad \Psi_B = |\psi_B| e^{i\phi_B} \tag{2.1}$$

The Josephson equations that characterise the current through the junction and the voltage across it are given as:

$$\begin{cases} I(t) = I_c \sin(\varphi(t)) \\ \dfrac{\partial \varphi}{\partial t} = \dfrac{2eV(t)}{\hbar} \end{cases} \tag{2.2}$$

In both equations the phase difference $\varphi = \phi_B - \phi_A$ across the junction appears. It should be noted that the Josephson junction is a nonlinear inductive element, this allows for the system to be driven from the ground state to the first-excited state without also accessing the higher-excited states. To understand how a Josephson junction might facilitate the formation of a physical qubit it should be placed in a simple circuit for which the energy levels can be calculated.

2.2. SUPERCONDUCTING QUBITS

2.2.1. CHARGE QUBIT

There are three main classes of superconducting qubits, charge, flux, and phase qubits [9]. The circuit diagram for a charge qubit, also know as a Cooper-pair box, is shown in figure 2.2.

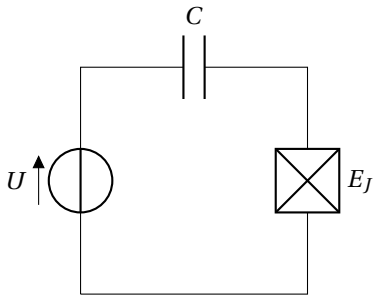


Figure 2.2: Charge qubit circuit.

The circuit consists of a capacitance C, a Josephson junction with energy E_J and the circuit is biased with a voltage U. A superconducting island forms between the capacitor and Josephson junction [15]. By applying an electric field Cooper pairs near the Josephson junction can tunnel on the island. The Hamiltonian for this system can be written as:

$$\hat{H} = 4E_C \left(\hat{n} - n_g\right) - E_J \cos\left(\hat{\phi}\right) \tag{2.3}$$

In this E_C is the charging energy, $\hat{n}$ is the number operator of Cooper pairs on the island, n_g is the effective offset charge of the device, E_J the Josephson energy and $\hat{\phi}$ is the phase operator. The charging energy is inversely proportional to the total capacitance in the following way:

$$E_C = \frac{e^2}{2C_\Sigma} \tag{2.4}$$

In this C_Σ is the total capacitance. For the Josephson energy the following can be written:

$$E_J = \frac{\Phi_0 I_c}{2\pi} \tag{2.5}$$

In this Φ_0 is the magnetic flux quantum and I_c the critical current. The Josephson equations from 2.2 show that if I and φ vary over time the voltage drop across the junction will also change over time. This behaviour can be described using a kinetic inductance known as the Josephson inductance L_J, which is given by the equation:

$$L_J = \frac{\Phi_0}{2\pi I_c} \tag{2.6}$$

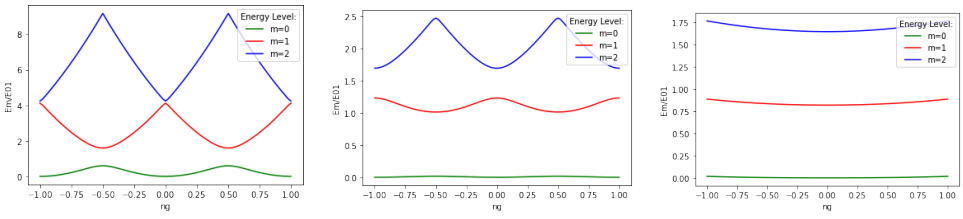
Using equation 2.5 and 2.6 it can be shown that the variables, E_J, L_J and I_c are related in the following way:

$$E_J = L_J I_c^2 \tag{2.7}$$

In the canonical quantization the number and phase operators satisfy the following canonical commutation relation:

$$[\hat{\phi}, \hat{n}] = i \tag{2.8}$$

From equation 2.3 the energy levels for the ground state and excited states can be calculated. The first 3 energy levels as a function of the effective offset charge normalized to the gap between the ground and the first excited state (at $n_g = 0.5$) are shown in figure 2.3a.



(a) $E_J/E_C = 1$ (b) $E_J/E_C = 5$ (c) $E_J/E_C = 50$

Figure 2.3: Qubit energy levels diagram for a charge qubit (a) to a transmon (c).

2.2.2. TRANSMON

For a charge qubit the system shows anharmonicity and charge dispersion of the energy levels [16]. The degree of anharmonicity and charge dispersion that the qubit has can be altered. This can be done by capacitively shunting the superconducting island of the Josephson junction [16]. Introducing this capacitance also means that the charging energy will decrease, as the total capacitance C_Σ in equation 2.4 changes. The dynamics of the qubit is governed by the dominant energy in equation 2.3 and can be reflected in the E_J/E_C ratio [17]. In the regime where $E_J \gg E_C$ the qubit will be less sensitive to charge noise, the qubits in this regime are also called Transmon qubits [17]. The anharmonicity of the Transmon qubit can still be sufficient to reduce the many-level system to a qubit [16].

2.2.3. SQUID

It is also possible to change the Josephson energy of a Transmon qubit. This is done by tuning the critical current of the system [14]. One way of changing this critical current is by changing the circuit and applying a magnetic field. Instead of using a single Josephson junction two junctions can be used in a loop as seen in figure 2.4.

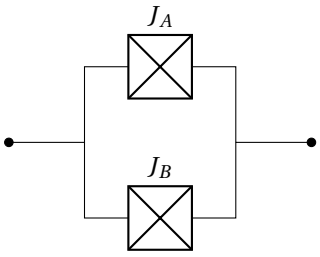


Figure 2.4: SQUID loop circuit component.

Applying a magnetic field can break time-reversal symmetry for the loop, essentially currents flowing through junction A or B acquire a different phase. This phase is proportional to the external magnetic flux Φ_{ext} that is applied. Logically the current can vary between being fully blocked or twice the current through a single Josephson junction. The superconducting quantum interference device (SQUID) has the following effective Josephson energy [18]:

$$E_{J,\,\text{eff}} = 2E_J \cos\left(\pi \frac{\Phi_{\text{ext}}}{\Phi_0}\right) \tag{2.9}$$

Where it is assumed that the Josephson junctions are identical and each separate junction on its own would have an energy E_J as calculated in equation 2.5. Here it is important to underline that the Josephson junctions should be identical, if they are not identical it would alter equation 2.9 and the effective Josephson energy will change accordingly. The SQUID allows for a tuneable effective Josephson energy making it a useful device in the design of a good quantum processor.

2.3. TUNNEL JUNCTION AND TRANSMON DESIGNS

2.3.1. DOLAN TYPE

The shadow evaporation technique or Niemeyer-Dolan technique is one of the early methods used to fabricate Josephson junctions [19]. An element of resist is suspended above the substrate, this in combination with film deposition from two opposing directions at angles not perpendicular to the substrate allows for two overlapping electrodes to be deposited. A 3D model showing such a Dolan type junction is shown in figure 2.5.

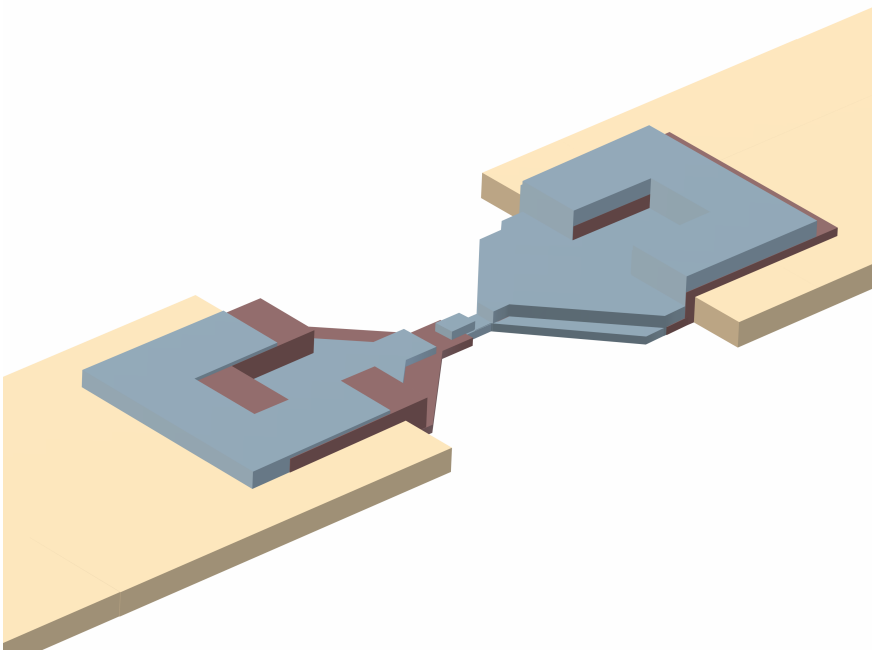


Figure 2.5: A Dolan type Josephson junction which is formed using a shadow evaporation technique. The yellow colour indicates the contacts, the first deposited layer of metal is red, the second layer which is deposited with a 180° rotation is coloured blue. Due to the shadowing technique the layers overlap at multiple places not just at the junction in the middle.

2.3.2. MANHATTAN TYPE

More recently, in 2001 the Manhattan type or cross-type Josephson junctions were first proposed by Potts *et al* [20]. This technique makes use of a thicker resist stack and instead of depositing the electrodes from opposing directions the electrodes meet at right angles. Using this technique there is great control on the junction area and it can be used to fabricate single electron transistors, charge-coherent qubits and also SQUIDs. A 3D model showing a Manhattan type junction is shown in figure 2.5.

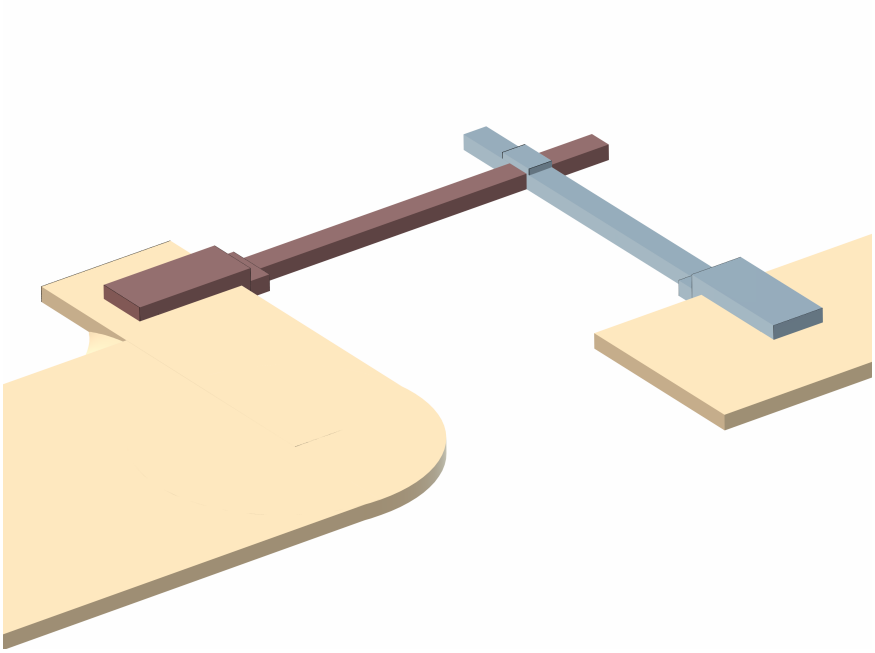


Figure 2.6: A Manhattan type Josephson junction which is formed using a top-heavy resist stack. The yellow colour indicates the contacts, the first deposited layer of metal is red, the second layer which is deposited with a 90° rotation is coloured blue. To make sure that there is a proper connection between the electrodes and the contacts the metal layers are deposited aiming towards the contacts. Because of this angle there is a slight shadowing effect near the junction.

TUNNELING IN AL-ALO$_x$-AL SIS JUNCTIONS

In this project the contacts are formed using either NbTiN or TiN and the electrodes are Al, with an AlO$_x$ tunnel barrier connecting them. Clean Al has an energy gap of $\Delta_{\text{Al}} \approx 180\,\mu\text{eV}$ ($T_c \approx 1.2\,\text{K}$), while oxygen-doped Al has a higher gap $\Delta_{\text{AlO}_x} \approx 280\,\mu\text{eV}$ ($T_c \approx 1.9\,\text{K}$) [21]. The superconducting gaps of two superconductors Δ_1 and Δ_2 and the normal state resistance R_n can be used to calculate the normal state tunneling current when a voltage $\frac{\pi}{2}\Delta$ is applied using the Ambegaokar-Baratoff relation [22].

$$I_c = R_n^{-1}\Delta_1(T)K\left(\left[1-\Delta_1^2(T)/{\Delta_2}^2(T)\right]^{1/2}\right) \tag{2.10}$$

This can be rewritten to the following form [23]:

$$I_c R_n = \frac{\pi}{2e}\Delta(T)\cdot\tanh\left(\frac{\Delta(T)}{2k_B T}\right) \tag{2.11}$$

This shows that the critical current can be calculated from R_n and the term on the right which depends on just Δ, the temperature T and the Boltzmann constant k_B.

The qubit transition frequency between the $|0\rangle$ and $|1\rangle$ state is given by the following approximation: $\omega_{01} \approx \left(\sqrt{8E_C E_J} - E_C\right)/\hbar$. The Josephson energy is related to the critical current but since that is not easily measured another calculation is done. Using the

equation for E_J 2.5 and the equation for $I_c R_n$ 2.11 the following equation is used to determine E_J

$$E_J = \frac{\Phi_0}{4eR_n}\Delta(T)\cdot\tanh\left(\frac{\Delta(T)}{2k_BT}\right) = \frac{M}{R_n} \tag{2.12}$$

In practice an experimental calibration is done to determine M [2].

2.3.3. TRANSMON DESIGN

An example of a transmon design is shown in figure 2.7. This device is also referred to as a starmon, it shows the relatively large capacitive elements which are used to shunt the SQUID, which is visible on the right side and forms the connection between the two capacitive elements.

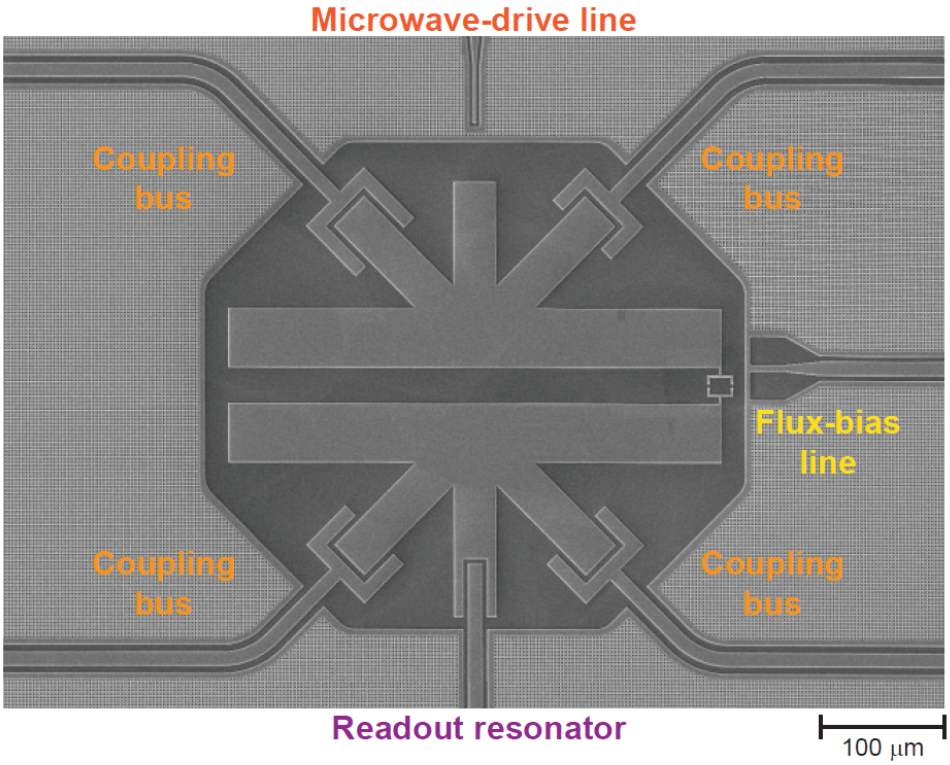


Figure 2.7: Starmon device, the red, orange, yellow and purple labels show the Microwave-drive line, coupling busses, flux-bias line and readout resonator respectively. Image from [24, p. 7].

2.4. SURFACE-CODE

Using the coupling busses, the starmon qubits can be coupled to their neighbours. In theory this way a surface-code fabric can be formed as shown in figure 2.8

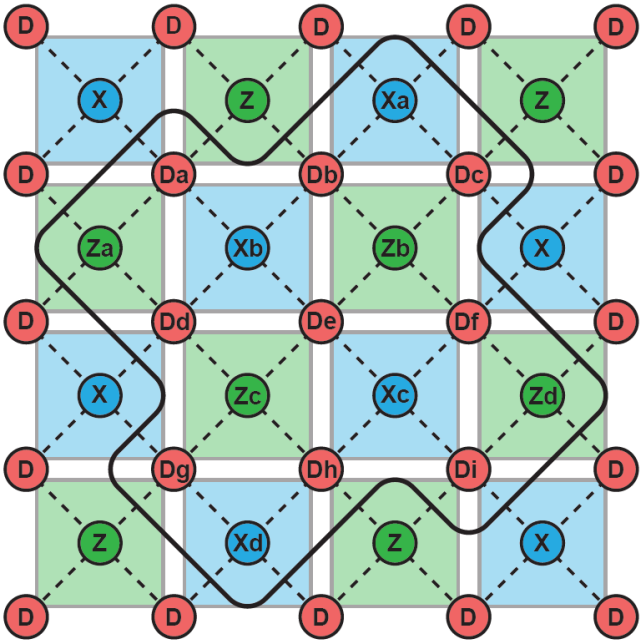


Figure 2.8: Surface-code fabric design, the red circles indicate data qubits, the blue and green circles indicate ancilla qubits which are used for error correction. The black boundary line surrounds a distance-3 planar logical qubit which is named Surface-17. Image from [24, p. 2]

When forming qubit states these also typically undergo decoherence, this can result in errors in the physical qubits due to unwanted interactions with the environment. One way to deal with this is through the use of surface codes, a two-dimensional network of physical qubits that together encode a logical qubit [24–26]. The idea is to use multiple physical qubits to achieve redundancy in the quantum information, creating a more resilient logical qubit. If a single error is found in one of the parts this error can be corrected. This means that the system can operate fault-tolerant for this kind of errors [27].

The D_i, Z_i and X_i qubits are split into 3 frequency groups to address them (low, mid, high). A problem that crops up in quantum circuits where frequency-multiplexing is being used is the unwanted idle crosstalk between neighbouring qubits whose frequencies are not sufficiently distinguishable [2]. They suffer from residual ZZ-crosstalk where correlations are established between qubits without the use of entangling gates, instead the qubits couple using the superconducting bus resonator. This crosstalk is responsible for dephasing of the logical qubits. To mitigate this as much as possible the qubit frequencies must be accurately addressed. This in turn means that the normal state resistance R_n needs to be precisely controlled, and ideally it would be tuneable in a bi-directional way.

2.5. THERMAL ANNEALING

Annealing is a heat treatment that alters the physical properties of a material. In the scope of this project the resistance of Josephson junctions is of interest. The objective is to learn what factors play a role in the increase or decrease of the resistance. The Al-AlO_x junctions serve a crucial role in the functioning of a transmon qubit, underlining the importance of getting more insight in the material science surrounding it. In particular the effect of subjecting the system to different temperatures and gaseous environments is of interest. Annealing can be done in different environments, for example under atmospheric conditions or in the presence of specific gaseous media such as forming gas which is a mixture of N_2 and H_2. Several studies have shown that the normal state resistance of Al-AlO_x junctions increases when heated to temperatures above 200 °C [9–11].

Besides the resistance changing due to annealing at high temperatures there has also been reports of variation in Josephson junction resistance while storing the samples at room temperature [3, 7, 28]. This effect is referred to as aging and could be explained by the nonthermal diffusion of oxygen through the AlO_x tunnel barrier [3]. Alternatively, the increase in resistance could also be explained by the absorption or desorption of other molecules. This leads to the resistance of Josephson junctions increasing with time, where in some cases the junction resistance even doubled in several days [6].

The reason that the resistance of the junction is so important is that it determines the frequency of the qubit. This means that as the junction ages the qubit frequency also drifts away from what it was initially designed at. Currently there is no good method to revert the junction to its initial frequency. Nonetheless, laser annealing can be used to tune the qubit frequency [2, 8–10]. Laser annealing can be used as a reliable tool to increase the resistance in a monotonic fashion.

However, there are also signs of qubit resistances decreasing [11]. This project also began after similar observations have been made during the fabrication process. The junctions showed a decrease in resistance after certain high-temperature processes. From these sporadic ascertainments the impression was made that 'anti-aging' of junctions, i.e. the decrease of junction resistance post thermal annealing, is possible. During this master's thesis the intent is to get an understanding of the mechanisms by which junction anti-aging can be achieved and work towards a reliable method of achieving on-demand aging of junctions in either direction.

2.5.1. RESULTS FROM LITERATURE

Let's take a closer look at what has been observed in the papers where thermal annealing of Al/AlO_x/Al junctions has been investigated. In the paper by J. B. Hertzberg et al. [10] they investigate laser annealing. Figure 2.9 shows the adaptive annealing of which they are capable.

If they increase the laser power they can tune the resistance stronger, they also take multiple steps of exposing so they can approach a target resistance without overshooting it. The blue, green and red colour correspond to laser powers of 1.74, 1.85 and 1.96 W, respectively. The single annealing steps take between 0.3 and 8 seconds. They find that using this technique they can tune R_n with a precision of 0.3%. The maximum relative shift that they found was 15%.

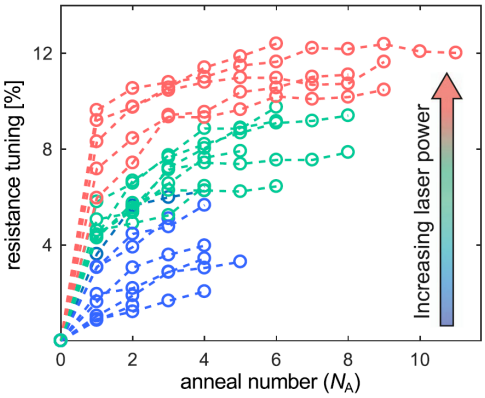


Figure 2.9: Adaptive annealing, figure from [10, p. 3].

In the paper by C. Granata et al. [8] they also investigate laser annealing, but for Nb/Al-AlO$_x$/Nb Josephson devices. They use an input power ranging from 2.00×10^5 to 2.22×10^5 W/cm^2, which heats the sample in between 160 °C to 170 °C after 2 minutes of heating. For one sample they heat it for 30 seconds at 170 °C and find that the critical current goes from 120 to 70 µA. For this experiment the normal resistance goes from 13.6 to 21.6 Ω.

In another paper by H. Scherer et al. [11] they investigate annealing in a forming gas atmosphere at different temperatures and for various durations. Figure 2.10 shows the forming gas annealing (FGA) that they have observed.

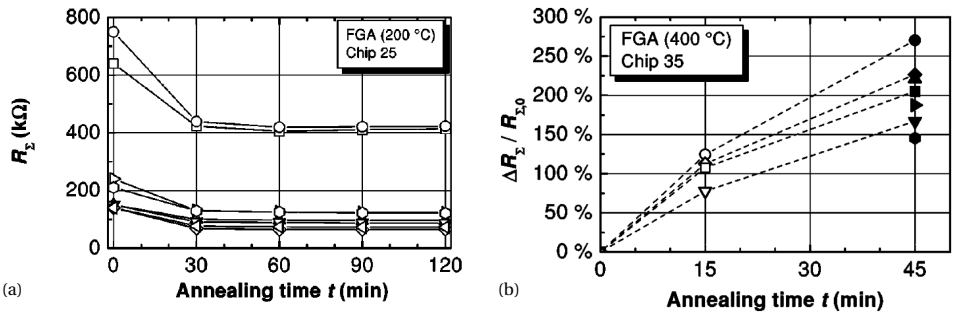


Figure 2.10: Annealing using forming gas, figures from [11, pp. 2529 & 2530]

In figure 2.10a they show the effect of decreasing sample resistance after FGA at 200 °C. They show this for annealing times from 30 to 120 minutes. Already after the first 30 minutes the maximum amount of resistance decrease has been reached. They find that the relative resistance change is about 30 to 40%. They also did FGA at 400 °C as shown in figure 2.10b. Here they find that after 15 minutes the samples had approximately doubled their resistance. Annealing even further at the 45 minute mark the resistances seem to have roughly tripled. They explain this increase of the resistance by an increase of the barrier thickness. They attribute this to unbound oxygen reacting with

the barrier, either it directly diffuses towards the barrier from the surrounding area, or it dissociates from aluminium hydroxides in the barrier.

In the paper by A. Bilmes et al. [7] they investigate annealing in air. Figure 2.11 shows the results that they found for annealing of three different device types .

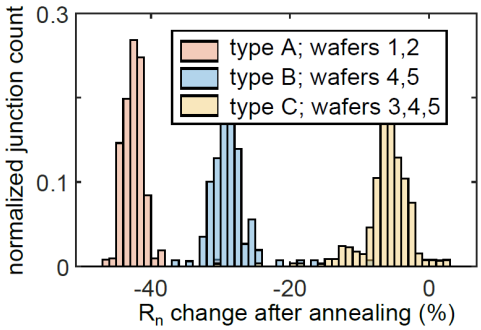


Figure 2.11: Change in resistance for three different device types after thermal annealing for 10 minutes in air of 200 °C, figure from [10, p. 3].

The difference between the devices is that unlike type A the type B and C junctions are oxidized in-situ after bandaging. Then for type C there is another additional oxidation step between junction formation and subsequent argon ion milling. The respective resistance drops after annealing for 10 minutes in air at 200 °C for the devices of type A, B and C were found to be 42 ± 2, 29 ± 2 and $6 \pm 3\%$.

2.5.2. PROJECT GOAL COMPARED TO RESULTS FROM LITERATURE

During this project, a controllable method of reducing junction resistance is sought after. As seen in the literature, annealing at 200°C allows for a reduction in R_n. But the problem is that the variation in this reduction is still rather large. When choosing a uniform detuning scale between the qubit frequency groups of $\Delta F \approx 1.2$ GHz the single-qubit gate error would be $\epsilon \approx 10^{-3}$ [24]. The frequency targeting should preferably be in the order of 50 MHz to be usable in real devices. During fabrication of real devices, the deposition is done first and afterwards the process for creating air bridges (AB) is done, it includes an annealing step. This means that preferably the tuning should occur after an AB anneal.

3

MATERIALS & METHODS

The first set of experiments that have been performed was to characterize the junctions at room temperature before and after annealing them. Conductances of SQUID (superconducting quantum interference device) test structure arrays containing junction pairs with different overlap areas are measured. Each die contains 272 test structures with SQUID loops, each superconducting loop containing the junctions can be characterized using their two contact pads. The 4 × 4 arrays are arranged in the shape of a Surface-17 device, the locations of the SQUID test structures are plotted in figure 3.1.

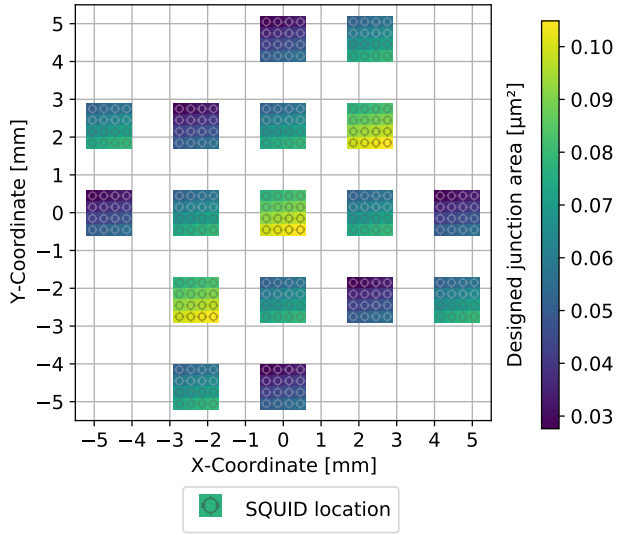


Figure 3.1: Heatmap showing the spatial coordinates of SQUID test structures, the colour of the squares indicates the designed junction area for Manhattan type junctions. The Dolan type junctions have a similar layout, but each JJ area would be slightly smaller.

There are quite some steps involved to prepare a die for an experiment and these have been structured in a flow chart as can be seen in figure 3.2. In the next section the fabrication of devices is discussed, describing the full process by going over each step in detail.

3.1. DEVICE FABRICATION

In this section further specifications for the processes as shown in the flow chart will be given. At the start a die with a base pattern prepared by my daily supervisor is selected. The base pattern is either compatible with the Dolan or Manhattan junction type.

3.1.1. BASE

For fabricating the base 100mm high resistivity single side polished wafers are used. Prior to deposition of the superconducting base layer, contaminants suchs as SiO_x are removed. It is also treated in a way to delay SiO_x formation. This is done by immersing the wafers in a solution of buffered oxide etch for 2 minutes. There are two techniques which have been used during this project to form the base layer, reactive magnetron sputtering and atomic layer deposition (ALD).

In the case of reactive magnetron sputtering the NbTiN base layer is deposited by bombarding a NbTi target using argon ions. Nb and Ti particles are released into the chamber, by additionally filling the process chamber with nitrogen a 200 nm NbTiN film can be formed on the substrate [1]. The typical sheet resistance of a 200nm thick film of NbTiN is 1.0 to 1.05 Ω/□.

The other material used for depositing the base layer is titanium nitride by ALD using tetrakis(dimethylamino)titanium (TDMAT) precursor. A 150 nm thick film of TiN is slowly grown by running 1900 ALD cycles. The sheet resistance for this film was measured to be 1.21 Ω/□. During ALD deposition a lot of particles from the chamber were deposited into the film, this was cleaned by ultrasonicating the wafer for 24 hours in PRS solution. During ALD, the sequentially introduced gases re-

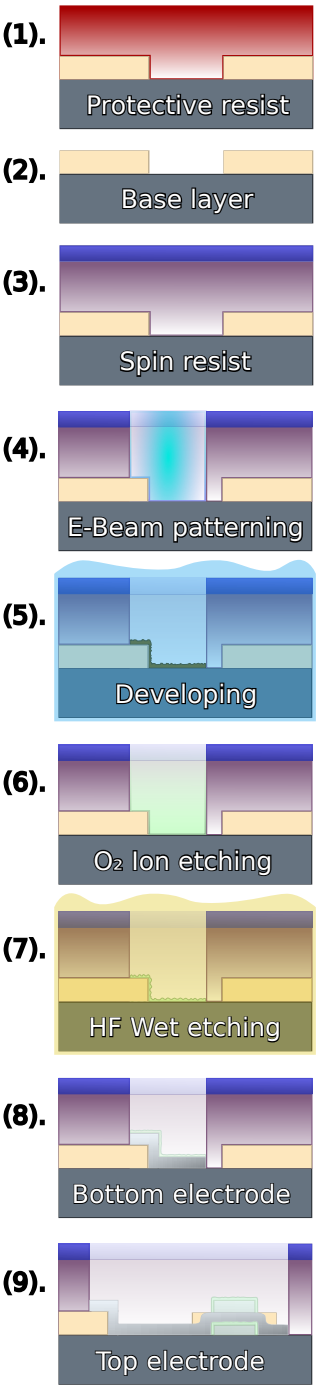


Figure 3.2: Fabrication process flow for a die with JJs, picture greatly inspired and adapted from [29, p. 21].

act with the surface in a self-limiting chemical process [30]. The films produced using this technique will be highly uniform with small thickness variations. But there are also downsides to using this technique, a longer deposition cycle and the inclusion of impurities in the base layer. Both techniques have been used in this project to form the base layer. After this, the next step is to remove the protective resist layer, which is on there to help prevent the substrate from getting contaminated during storage. This layer can be removed by immersing the sample in acetone at 52 °C for several minutes. A beaker of acetone is heated using a water bath placed on a hot plate.

3.1.2. SPINNING RESIST

Now that the substrate and base layer are exposed the sample is ready to be covered in new resist layers. There are several factors that play a role in the resulting thickness of the layers. For example, the resist viscosity as well as the speed at which it is spun. It is important that the thickness is also uniform over the sample. Luckily, the thickness is also somewhat visible to the naked eye. When light reflects off the resist the perceived colour is affected by the thin-film interference similarly to what happens with a thin oil film on top of water. This means that a non-uniform resist layer can be easily recognized, informing that the sample should be cleaned and respun.

The samples are spun by placing them on a chuck which has small holes so that a vacuum can keep the sample in place during spinning. The used devices can be seen in figure 3.3 There are two recipes which have been carefully organized. One each for the Dolan and Manhattan type junctions.

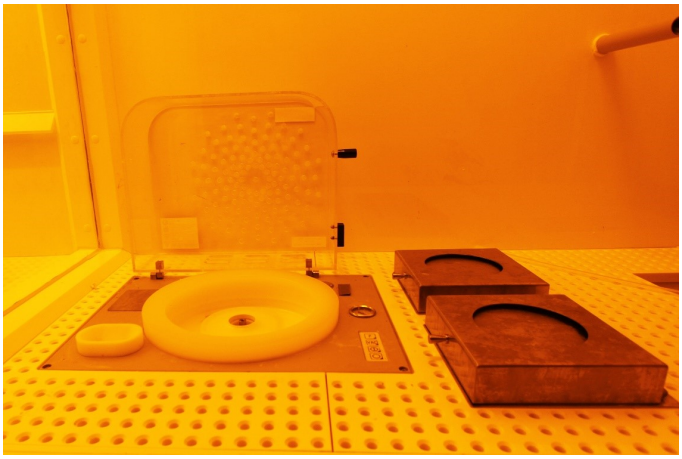


Figure 3.3: The setup used showing the spin coater and hotplate, picture from [31].

DOLAN RESIST SPINNING RECIPE

Two layers of resist are spun, the first being PMGI SF7, which consists of polydimethylglutarimide polymers in a blend of solvents. This is spun at 2000 rpm. After spinning the sample, it is baked using the hotplate at 185 °C for 5 minutes. To quickly cool the sample

the nitrogen gun can be used, so as to not melt any plastics. The expected thickness of this resist layer is approximately 400 nm.

The second layer consists of PMMA A3, polymethyl methacrylate, which is also spun at 2000 rpm. And again, the sample is baked at 185 °C for 5 minutes. The expected thickness of this resist layer is approximately 150 nm.

MANHATTAN RESIST SPINNING RECIPE

Again, two layers of resist are spun, the first being a mixture of PMGI SF7 and cyclopentanone in a 1:1 ratio. This is spun at 1500 rpm. After spinning the sample, it is baked using the hotplate at 185 °C for 5 minutes. The expected thickness of this resist layer is approximately 200 nm.

The second layer consists of PMMA A6, which is also spun at 1500 rpm. And again the sample is baked at 185 °C for 5 minutes. The expected tickness of this resist layer is approximately 600 nm.

3.1.3. EBEAM PATTERNING

Now that the die is covered in resist it is ready to be patterned using the Raith EBPG-5000+, an image of the machine can be found in figure 3.4.

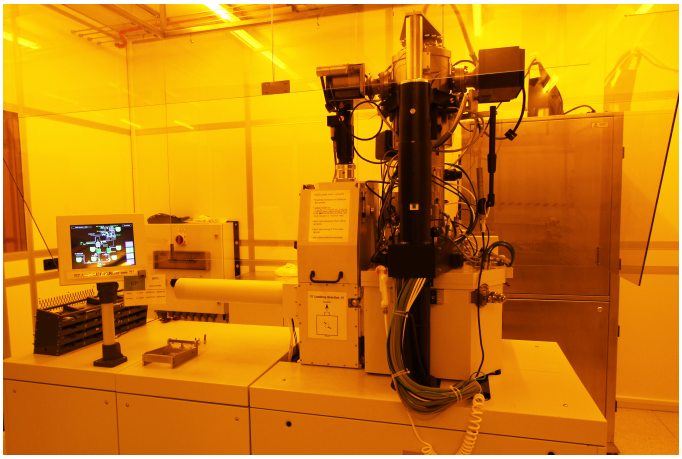


Figure 3.4: The setup used showing the Raith EBPG-5000+, picture from [31].

To load the sample, it is first placed on a holder where it is clamped down to secure it. The sample is oriented with the top (the title can be found here) on the right so that once loaded the top is parallel to the x-axis. Then the optical microscope is used for alignment, the alignment microscope can be seen in figure 3.5. The sample is locked in position on the microscope table. The alignment procedure is straightforward. Theta alignment is performed, the alignment of the sample can be checked using the markers in the corners of the sample. Then the sample is levelled to make sure that the height differences are within 10 nm throughout the sample. The height measurements are taken using a laser. It is also set to a level within 50 nm of the height of the reference on the

holder. Next to the reference plate there is a Faraday cup, the crosshair of the microscope is centred on this cup and then the coordinate system is zeroed. After this the x and y coordinates of one of the markers in the top left corner of the sample are taken. These are later used to inform the machine of the positioning of the sample.

A manual marker search is performed to inform the machine of the location of the corner markers. The machine goes to where it expects the marker to be and then this region can be scanned, and the system can manually be better aligned with these markers. After this procedure, the pattern as given in the job file will be exposed.

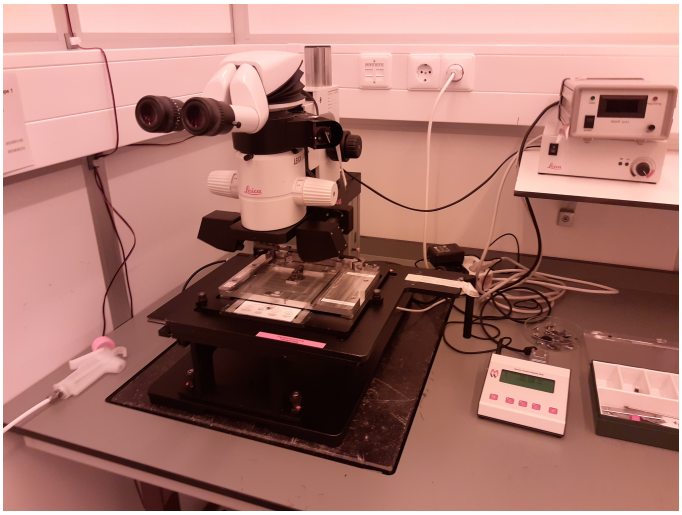


Figure 3.5: The setup used showing the alignment microscope, picture from [31].

3.1.4. DEVELOPING THE PATTERN

During the patterning step chemical and physical changes occur in the exposed areas of the resist layer. This exposure creates chain scission or (de-cross-linking) in the resists, changing the solubility of the material. This allows for selective removal of the exposed areas using a chemical developer. These kinds of resists are also called positive resists.

To develop the samples the following procedure is done. First the sample is immersed for 1 minute in a solution of MIBK (methyl isobutyl ketone) in IPA (isopropyl Alcohol) with a ratio of 1:3. This develops the layer of PMMA. Then the MIBK is rinsed of the sample using extra IPA and finally the sample is dried using a nitrogen spray gun.

Next the sample is immersed in water for 20 seconds and subsequently in MF 321 (an approximately 2% by mass dilute solution of Tetramethylammonium hydroxide in water) also for 20 seconds. This develops the layer of PMGI. The MF 321 is rinsed of using extra water. Again, the sample is dried using the nitrogen spray gun.

3.1.5. ETCHING

Before depositing the aluminium to form the junctions it is important to have an exceptionally clean surface. To create this, two etching steps are performed, dry and wet

etching.

DRY ETCHING

During the dry etching step material is removed by exposing the sample to a bombardment of ions. A plasma of reactive oxygen is used to dislodge residual resist scum from the exposed surface. This process is also referred to as reactive-ion etching (RIE). The etching process is anisotropic, which means that the rate of etching in the vertical direction is higher than the rate of etching in the lateral direction. This means that there should not be much undercut underneath the edges of the resist layer.

This step is essential as it has been shown through many tests that the O_2 cleaning step is crucial for increasing the yield of junctions. The pressure in the reaction chamber is 0.010 mbar and a voltage difference of 110 V is applied for 50 seconds. The machine used during this step is the Sentech Etchlab 200 of which an image can be seen in figure 3.6

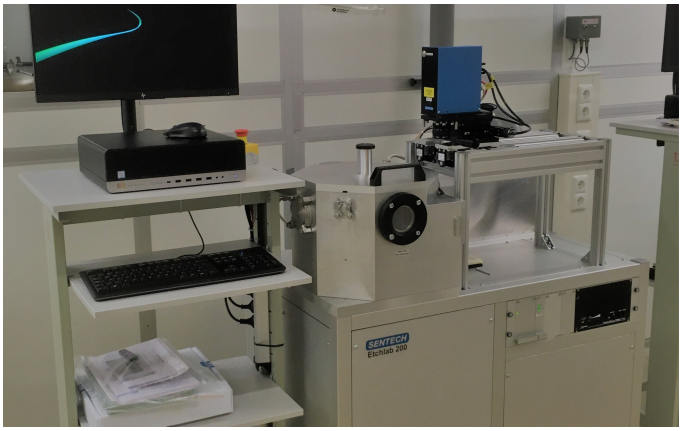


Figure 3.6: The setup used showing the Sentech Etchlab 200, picture from [31].

WET ETCHING

During the dry etching step, the sample has come in contact with oxygen. This means that there will be a lot of silicon dioxide at the substrate surface. To get rid of this we do a process referred to as buffered oxide etch (BOE). This process is based on the following chemical reaction [32]:

$$SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2\ H_2O$$

The H_2SiF_6 that is created is soluble in water. This reaction is done using a dilute solution of hydrofluoric acid (HF). The acid is buffered using NH_4F so that there is a constant supply of fluoride ions. If these are depleted the reaction would stop. Besides the silicon dioxide, silicon and silicon nitride are also etched at a slow rate. In this step BOE 7:1 is used, this is composed out of 87.5 wt.% ammonium fluoride and 12.5 wt.% hydrofluoric acid [32].

3.1.6. JUNCTION DEPOSITION & LIFT-OFF

After having done the etching steps the substrate surface is now clean. To keep it clean the sample should be quickly loaded in the deposition machine where it will be in a high vacuum around 10^{-7} mbar. However, it first needs to be placed on the sample holder and manually aligned using one of the optical microscopes. This means that here the substrate could potentially be contaminated again. The machine used for deposition of aluminium and the oxidation steps can be seen in figure 3.7.

Figure 3.7: The setup used showing the Plassys evaporation machine, picture from [31].

DEPOSITION STEPS

The steps for Dolan and Manhattan junctions are quite similar. First aluminium is deposited, in the case of Dolan junctions the sample is 15° from perpendicular and the azimuthal angle is in allignment with the opening in the resist. After deposition of a layer of aluminium the sample is oxidized. This is done by filling the chamber with O_2 until the pressure reaches 1.3 mbar and then statically keeping it at that pressure for 11 minutes. During this step, a layer of aluminium oxide forms on top of the aluminium electrode. The second layer of aluminium is also deposited under the same 15° zenith angle but with a 180° azimuth rotation. After this step, an additional capping oxidation can be done. This step would look the same as the oxidation step described before. For some samples, this step is skipped.

In the case of Manhattan junctions, the sample has a zenith angle of 35° during the first deposition of aluminium. In this step a 35 nm thick layer is deposited. Then the sample is oxidized in the same way as for Dolan junction. In the second deposition the

zenith angle is kept the same, but the sample is rotated to a 90° azimuth angle. The second layer that is deposited is 75 nm thick, this is thicker than the bottom layer and is done so that the aluminium can connect even though the bottom electrode creates a shadowing effect. In the end there is the option to do an additional capping oxidation step. This is used to cover the entire sample in a protective oxide layer. As is studied in this research it also effects the change in conductance that would ensue through an annealing process, more about this is discussed in chapter 4.

LIFT-OFF

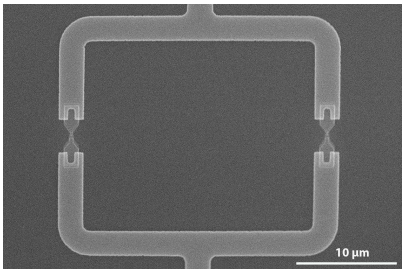
After depositing the aluminium layers and forming the tunnel barrier the next step would be lift-off. In this step the sample is immersed in a solvent. The solvent used is *N*-methylpyrrolidone (NMP). It is heated to about 88°C and the sample is kept in the solution for about 15 minutes. After this a glass pipette is used to spurt the NMP to the sample surface. This sudden stream of liquid promotes lift-off and flakes of aluminium separate from the sample. When most of the aluminium is detached from the surface the sample is cleaned using IPA and blown dry with the nitrogen spray gun. After this step, the Junctions are ready to be measured.

3.2. SEM IMAGES OF SQUIDS & JOSEPHSON JUNCTIONS

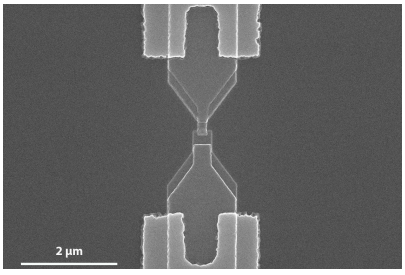
Using a scanning electron microscope (SEM) it is possible to take high-resolution images of the SQUID loops and the individual junctions. The surface of the samples is scanned using a focused beam of electrons, which interact with the atoms at the surface [33]. These atoms can go to an excited state and afterwards emit secondary electrons which can be detected to form an image.

SCAN OF A DOLAN DEVICE

Figure 3.8 shows two SEM images taken of the Dolan SQUID loop and an individual Dolan type JJ.



(a) SQUID loop with two Dolan type JJs

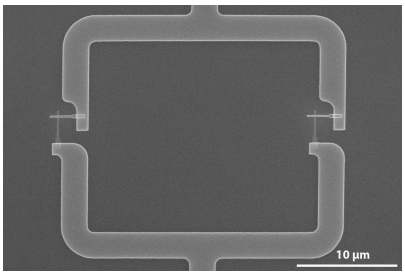


(b) The two overlapping electrodes of a Dolan type JJ

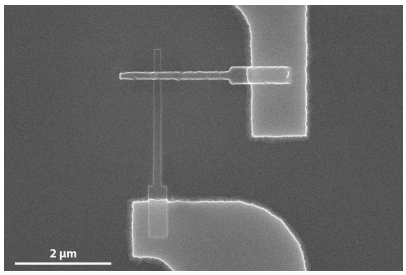
Figure 3.8: Figure 3.8a shows a SQUID loop with two Dolan type JJs taken with the SEM at ×4000 magnification, the scalebar shows a length of 10 µm. The contacts have a u-shape to ensure that besides the horizontal interface there is also a good vertical contact with the electrodes. Figure 3.8b shows a single Dolan type JJ taken with the SEM at ×20000 magnification, the scalebar shows a length of 2 µm. Notice that due to the deposition technique used, each electrode consists of two identical shapes overlapping each other. For the top electrode, the electricity has to flow through both layers to reach the JJ. This means there is also a large spurious junction near this top contact.

SCAN OF A MANHATTAN DEVICE

Figure 3.9 shows two SEM images taken of the Manhattan SQUID loop and an individual Manhattan type JJ.



(a) SQUID loop with two Manhattan type JJs

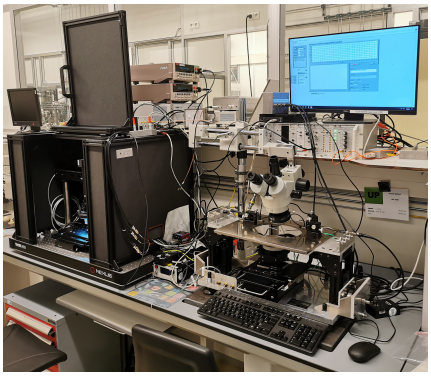


(b) The two overlapping electrodes of a Manhattan type JJ

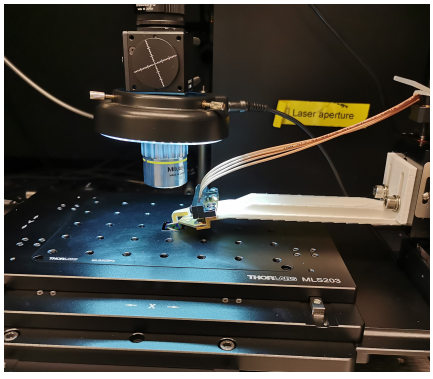
Figure 3.9: Figure 3.9a shows a SQUID loop with two Manhattan type JJs taken with the SEM at ×4000 magnification, the scalebar shows a length of 10 µm. Figure 3.9b shows a single Manhattan type JJ taken with the SEM at ×20000 magnification, the scalebar shows a length of 2 µm. In this case the orthogonal deposition technique allows for well defined single layer electrodes.

3.3. JUNCTION MEASUREMENT

To measure the conductances of the SQUID loops the samples are loaded onto the horizontal XY-stage of either the automatic probe station (APS) or the manual probe station (MPS). In figure 3.10a both systems can be seen, the APS on the left and the MPS on the right. The APS was a custom build setup for measuring junction resistances and closed loop laser annealing developed by members of the DiCarlo Lab and an in-depth overview on the system can be found in chapter 3 of the following thesis “Improving Frequency Targeting of Transmon Qubits Through Automated Laser Annealing” [2].



(a) The probe station.



(b) A die loaded on the horizontal XY-stage of the APS.

Figure 3.10: The setup showing the probe station, the black box on the left contains the APS of which a close-up picture is shown in figure 3.10b. The system on the right is used for manual 2-point measurements.

3.3.1. CIRCUIT DIAGRAM

The conductance measurements are done using either a 2-point or 4-point measurement. The circuit diagram for such a measurement setup can be seen in figure 3.11. The difference is that with the 4-point measurement a more accurate resistance can be measured. With the 2-point measurement the contact resistances are included, so it is best to try and avoid using it when the 4-point measurement setup is available. The only reason for using the 2-point setup is because of lack of availability of a better system at times.

With the MPS only 2-probe measurements have been taken. The APS allows for both 2-point and 4-point measurements, even at the same time. This way datasets can always be compared to others gathered in the same way, so that never underestimated conductance values are compared with another more accurate dataset taken at a later time. Otherwise, the change in conductances would be structurally misjudged between those datasets. The yield and general trends and differences in conductances, can still be determined when comparing datasets which have both been taken with a 2-point measurement setup.

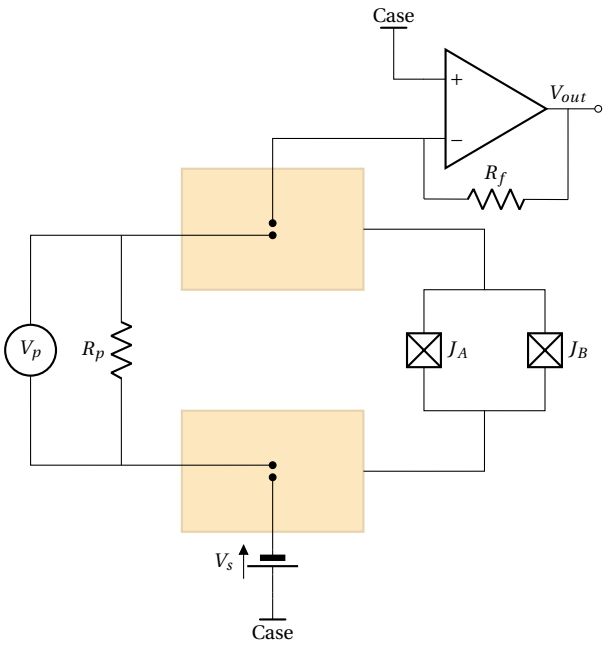


Figure 3.11: Circuit diagram showing the 4-point resistance measurement setup. The SQUID loop is connected to two contact pads shown in tan here. One probe is used to apply voltage over the SQUID loop using the source V_s. The second probe is used to connect the SQUID to an operational amplifier with feedback resistor R_f, this is used to determine the current through the SQUID loop and thus the resistance can be measured. Using just these two outer probes is enough to do a 2-point measurement. However, the measured current is influenced by the contact resistances of the probe needles, so the resistance measured is excessive. To determine the precise voltage drop over the SQUID loop a high-impedance differential amplifier V_p can be connected using a second pair of probe needles.

After deposition, the SQUID loop test structures have a resistance between 4 to 10 kΩ, or equivalently the conductances ranges from 250 to 100 µS respectively. But unlike most other simple resistance measurements, the Josephson junctions could be shorted when measured with high currents [2]. The voltage source V_s as shown in the circuit diagram in figure 3.11 supplies a voltage of roughly 10 mV resulting in a current of about 1 µA, which is low enough for this not to happen. In general, the resistance of the SQUID can be calculated as:

$$R_{SQUID} = \frac{V_s}{I_s} \tag{3.1}$$

with I_s being the current going through the SQUID. The operational amplifier (op amp) is connected in such a way that there is a closed feedback loop using the feedback resistance R_f which is set to 100 kΩ. The input signal at the negative-port (−) is at the same potential as the positive-port (+), which is grounded to the case of the measurement box. The potential at − is also referred to as a virtual ground. This means that the closed loop gain of the inverting amplifier can be determined by the ratio of the two external resistors in the following way:

$$V_{out} = -\frac{R_f}{R_{SQUID}} V_s \tag{3.2}$$

where V_{out} is the voltage output after the amplifier that is measured using a Keithley 2000 multimeter. Only R_{SQUID} is unknown in this equation and with a 2-point measurement setup can be calculated from the other values. However, as mentioned before it is better to use a 4-point measurement setup and include the contact resistances in the calculation. Subtracting the contact resistances δR_c of the 2 probes from the total resistance R_t we can find the new SQUID loop resistance as:

$$R'_{SQUID} = R_t - 2\delta R_c \tag{3.3}$$

This also means that there is a new current through the SQUID loop which is now related to the total resistance and thus equation 3.1 transforms to the following form:

$$R_t = \frac{V_s}{I'_s} \tag{3.4}$$

Similarly, a new relationship for the output voltage can be found and equation 3.2 is transformed in the same way:

$$V'_{out} = -\frac{R_f}{R_t} V_s \tag{3.5}$$

After rewriting this equation it can be shown that the contact resistances just result in a constant offset on the measured R'_{SQUID} (assuming the contact resistances themselves stay constant). To account for the contact resistances the voltage drop over the SQUID loop is measured using the second pair of probe needles connected to the high-impedance differential amplifier V_p. In the new setup a resistor is put parallel to the SQUID loop, the resistance R_p is chosen to be 10 MΩ. It is again assumed that the second pair of probes also have a contact resistance of R_c per probe. Given this, the fact that $R_p \gg R_t$, equation 3.4 and 3.5 the following equation approximates R'_{SQUID}:

$$R'_{SQUID} \approx \frac{V_p}{I'_s} = \frac{V_p}{V_s} R_t = -\frac{V_p}{V'_{out}} R_f \tag{3.6}$$

Again, only R'_{SQUID} is unknown in this equation, and it can be calculated by measuring V_p and V'_{out}.

DIFFERENCE BETWEEN 2 & 4-POINT MEASUREMENTS

To quantify the difference between the 2 and 4-point conductance measurements the results can be compared. In figure 3.12 a histogram is shown where the frequency of distinct ranges of difference in conductance is depicted. From this it is clear that most frequently the difference lays between 0.46 and 0.91 µS. Besides that, there is a distribution ranging from 0 to a max value of 14.15 µS (there was one instance of a difference of 39.64 µS which is not shown as it lays far from the majority of the data points). Seemingly the distribution is not symmetric and thus cannot be coming from a normally distributed variable. The tail on the right side makes the distribution look similar to that of for example a Poisson distribution.

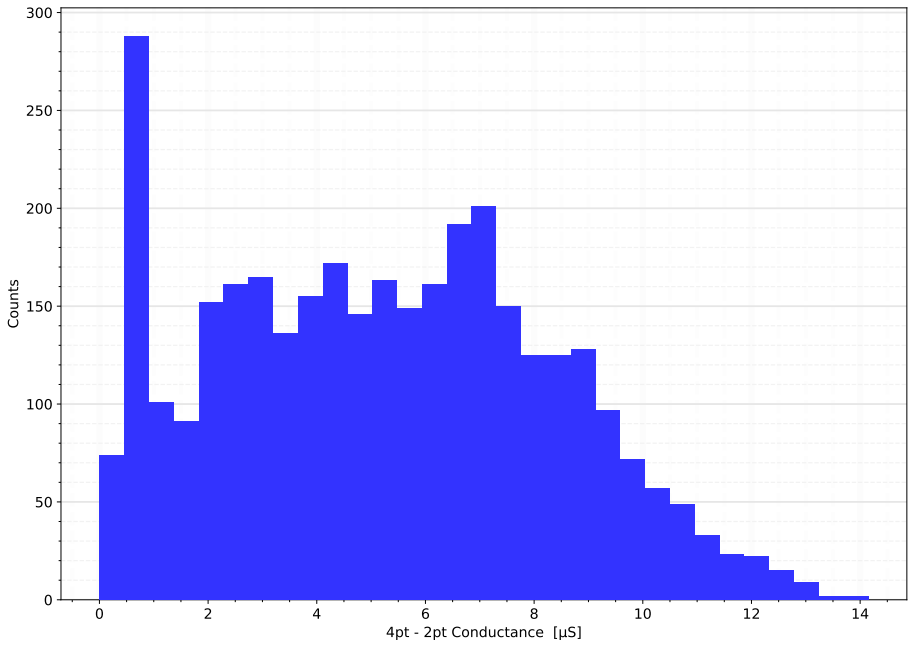


Figure 3.12: A histogram showing the distribution in the difference between the measured conductances for a 4pt measurement vs a 2pt measurement.

3.4. THERMAL ANNEALING PROCEDURES

After having deposited the junctions and measuring them the sample is ready for the annealing procedure. In this project two forms of annealing have been investigated, what is referred to here as simulated airbridge annealing and rapid thermal annealing. These are discussed in the following two sections.

3.4.1. SIMULATED AIRBRIDGE ANNEALING

During the fabrication of a superconducting quantum processor there is a step in which airbridges are fabricated. These airbridges are a necessary component in scalable quantum processors. First of, they suppress spurious modes of coplanar waveguide resonators. Secondly, it forms a connection between the ground planes which are interrupted by coplanar waveguide resonators. This step involves spinning resist and heating the die on the hotplate for which the setup can be seen in figure 3.3. First PMGI SF15 resist is spun at 2500 rpm. After spinning the resist is baked at 185°C for 5 minutes to remove the carrier solvent. After this the hotplate temperature is set to 200°C. The sample is baked for another 5 minutes, thereafter it is cooled using the N_2 gun. Finally, the resist is removed by dipping the sample in hot NMP at 88°C. After this it is cleaned using IPA.

3.4.2. RAPID THERMAL ANNEALING RECIPES

The machine used for rapid thermal processing can be seen in figure 3.13. Samples can be loaded manually into the process chamber, where they sit on top of a quartz wafer located on a special isolation tray. The system has 13 tungsten halogen lamps above and below the sample [34]. These lamps can heat up the system about 100°C per second, meaning that the set temperature for the experiments is reached in 2 to 4 seconds. During the heat cycle there is a flow of nitrogen gas that cools the system so that a consistent temperature can be reached.

(a) The system when closed, picture from [31].

(b) A picture showing how samples are loaded.

Figure 3.13: The setup used showing the Solaris 100 Rapid Thermal Processor system.

In the figures 3.14 to 3.19 the graphs of the RTA processes are shown. The x-axis shows the time axis in seconds. The y-axis shows the temperature in °C (white), flow in SCCM*10 (blue) and power level in %/10 (green). All recipes follow the same order of steps, there are 6 steps: purge, ramp up, hold, ramp down, purge and finish.

The first purging step is used to get rid of any contaminants in the process chamber. During 300 seconds the system is flushed with pure nitrogen gas. After this the system is ready for ramp up, power goes to the halogen lamps and the annealing chamber is quickly heated to a set temperature. Often there is some overshooting, in the recipes where the setpoint is 400°C this was very minor. However, in the 200 and 300°C this occurred more often and was a bit of a problem. An example of this overshooting can be seen in figure 3.15. What made it more difficult was that changing the parameters of the recipe steps (REM/Intensity, P value, I value, D value) did not always help. What

made it even more troublesome was that each run of a recipe could look different. One time it could overshoot by a lot and running the same recipe another time might only show a minor amount of overshooting. After the ramp up the temperature is held for 120 seconds after which there is a slow ramp down. After the finishing step the temperature can still be relatively high, above 80°C, it is better to wait for the sample to cool down till it reaches room temperature. This way the system stays in the controlled environment all the way till it is completely cooled off.

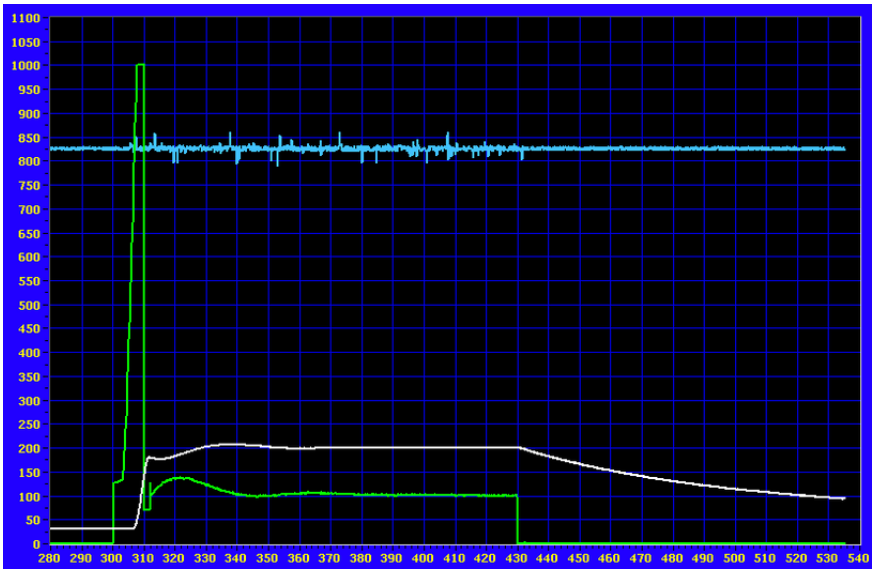


Figure 3.14: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 200°C anneal using N_2.

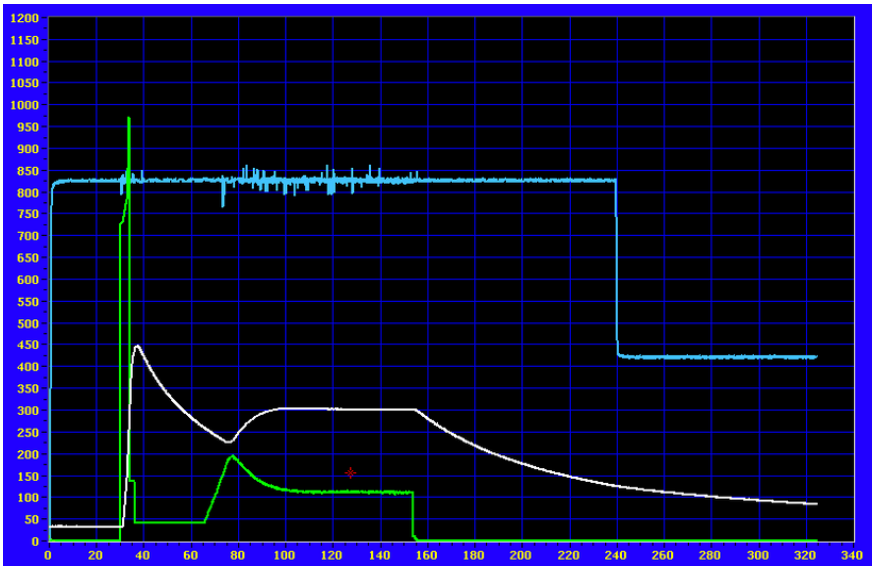


Figure 3.15: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 300°C anneal using N_2. Notice the initial spike here around $t \approx 40$ s, it shows that the temperatures overshot the setpoint of 300°C by a lot. After this the temperature drops down to below 250° and as can be seen the power is supplied too late, eventually a stable 300° plateau is reached.

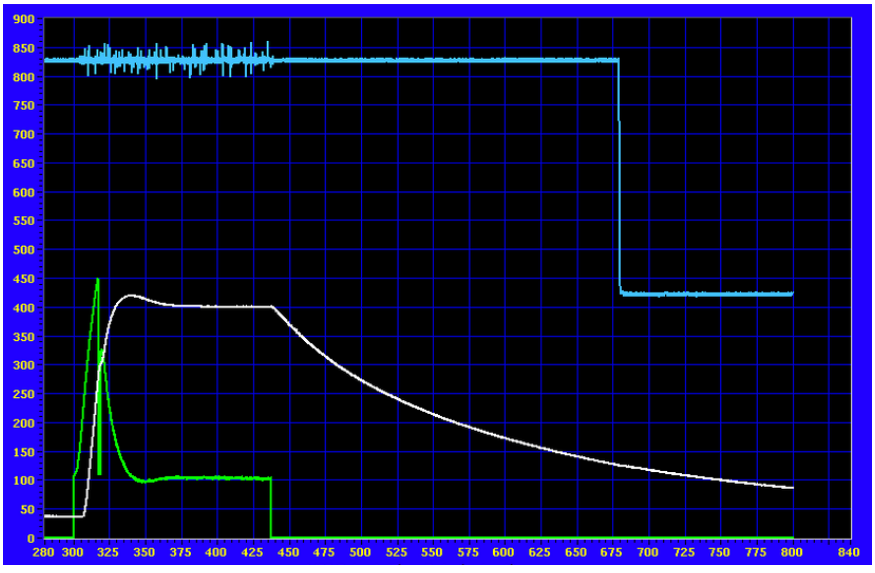


Figure 3.16: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 400°C anneal using N_2. In this recipe the setpoint is also overshot as can be seen at $t \approx 340$ s.

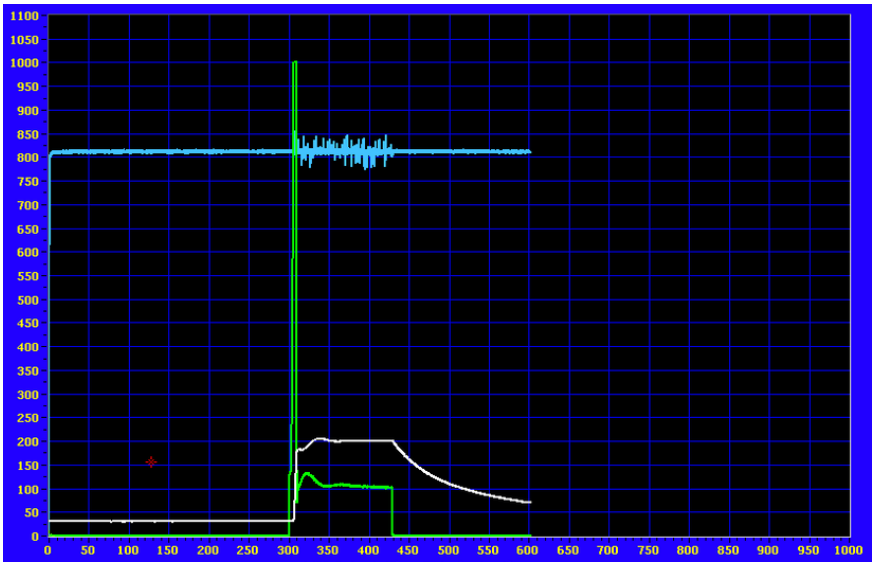


Figure 3.17: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 200°C anneal using forming gas (90% N_2 / 10% H_2).

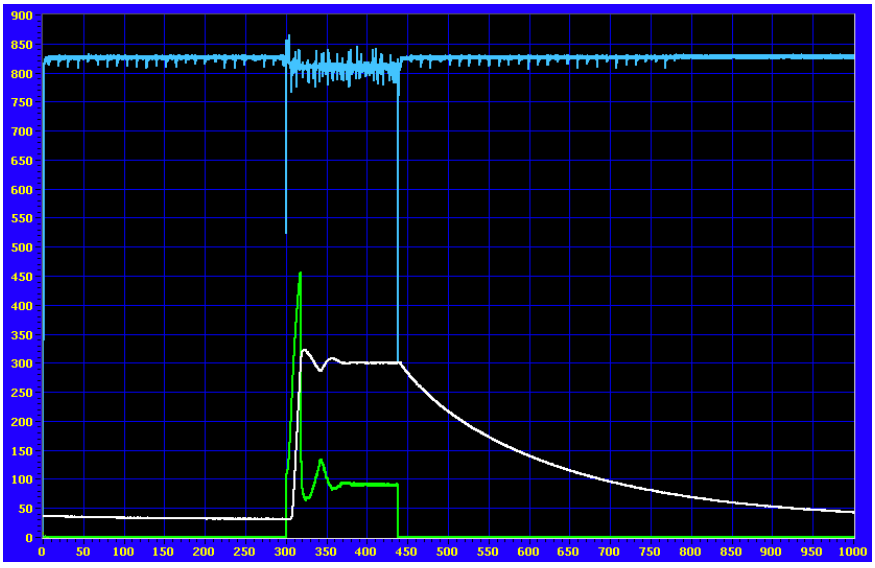


Figure 3.18: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 300°C anneal using forming gas (90% N_2 / 10% H_2). From $t \approx 310$ s to $t \approx 360$ s there is some overshooting, and the system overreacts making it take a bit longer to reach a stable 300°.

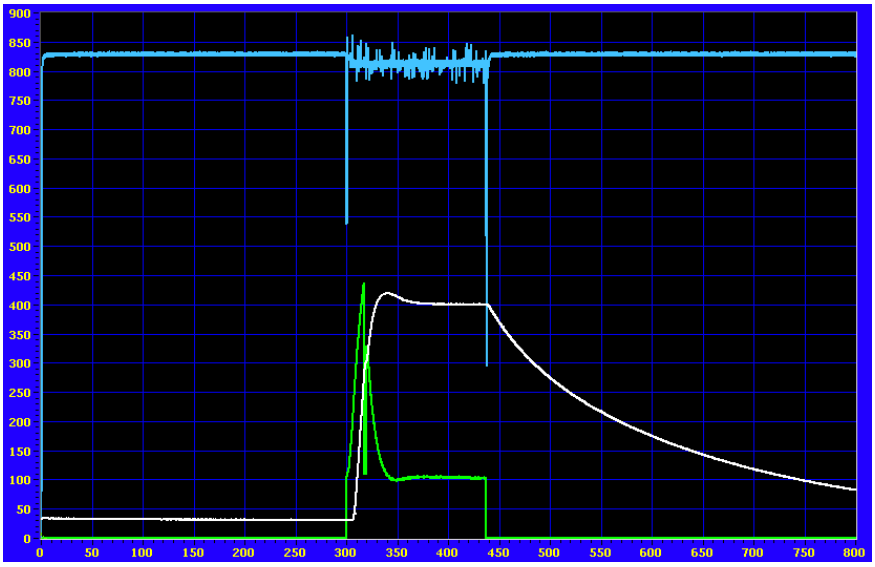


Figure 3.19: Graph showing the control temperature, total flow, and power input over time in the colours white, blue and green respectively. The process shown here was a typical 400°C anneal using forming gas (90% N_2 / 10% H_2).

4

Results & Discussion

The processes used to fabricate a die containing SQUID loops with Dolan or Manhattan type junctions for transmon qubits is described in detail in chapter 3. The layout for the dies can be seen in figure 3.1. The results for these devices are presented and analysed in this chapter.

4.1. General Data Analysis Procedure

The conductances in each square of 16 junctions are similar to those for the qubit that would be in that position on a Surface-17 device and are in a range of approximately 60 to 300 µS. To test how annealing at high temperatures (200 to 400°C) affects the conductances various experiments have been carried out. In general, the conductances of samples are measured before and after a thermal annealing procedure so that the effect of these processes can be compared. From this the change in the conductances per area can be calculated. All data shown in this chapter are filtered, initially all data points with conductances below 20 and above 500 µS are removed, as these indicate open and shorted junctions, respectively.

Besides removing data from the open and shorted junction pairs, it is also possible for a single junction to be malfunctioning. This can be due to it being either entirely or partially open. Where partially open would mean that there is still a connection but with a defect, for example there is some material missing, this would also results in a higher resistance. Similarly, a single junction could be completely shorted or have a defect which lowers the resistance. Taking these kinds of deficient irregularities into account, it necessitates an additional filtering method which is done by plotting a linear fit to the measured conductances as a function of the designed junction area. Outliers which are below 0.7 times the fit or above 1/0.7 times the fit are removed. This step is then done a second time using the newly obtained fit for the leftover dataset. In the end a dataset without extreme outliers is left.

CONDUCTANCE VS JJ AREA

The conductances measured after deposition G_{Dep} of the SQUID loops on sample N. x 3e^4 are shown in figure 4.1. Every sample has a specific label, the first letter refers to the technique that was used to form the base, in this case ALD. The second letter refers to the type of JJs on the die, in this case the x refers to the Manhattan style junctions (sometimes also referred to as cross-type). The third set of symbols indicates where the die was positioned on the wafer it is diced from. In this case the 3$^{\text{rd}}$ die on the edge, and the 4 means that it is the 4$^{\text{th}}$ time this sample was used in an experiment. In between experiments the sample has been recycled, meaning that the top layers have been removed and keeping only the base layer intact.

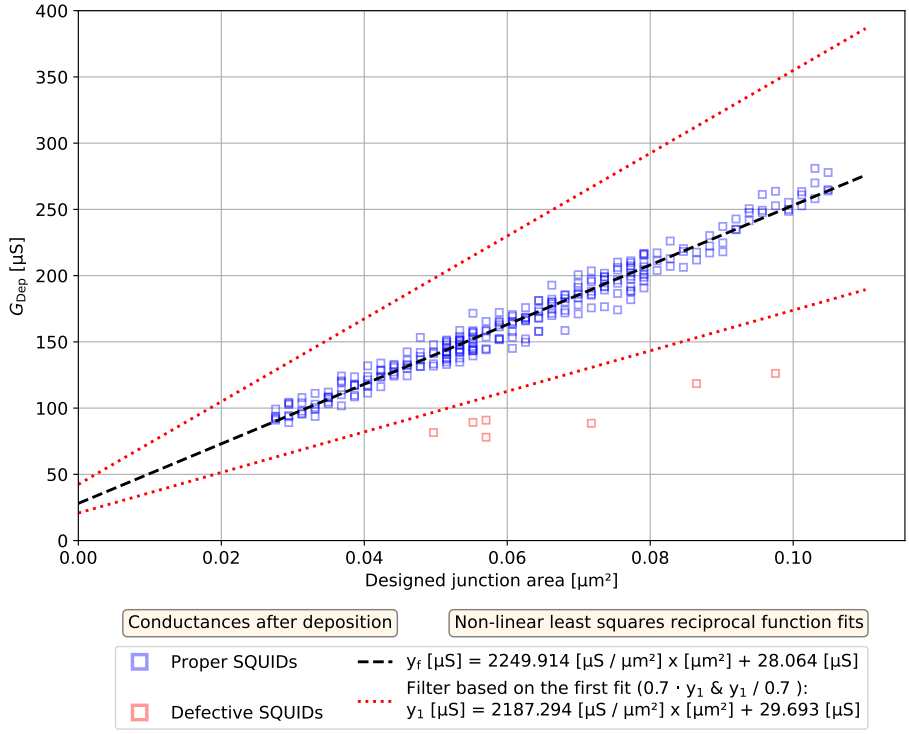


Figure 4.1: A plot showing the linear dependence between designed junction area and conductance G_{Dep} of the SQUIDs measured after deposition. The □ symbols indicate that the junctions are of Manhattan type. The blue colour shows data from proper working SQUIDs, the red colour indicates a defective SQUID. The dashed black line shows the fit line through the data of the proper SQUIDs, it is obtained from a linear regression routine from the `Python` package called `scipy`. The red dotted lines indicate the outer limits of what data passes the filter. The functions of both the first fit line y1 and the final fit line y_f are also given, showing that for y_f the slope is a bit steeper.

As can be seen in the plot most data lays in between the red dotted lines indicating the outer limit of data that would pass through the filter. What is not visible here is that before applying the filter already 7 data points got removed as the conductances were above 500 µS. In this specific dataset another 7 points are removed as they fall below the

lower filtering line. These correspond to junction pairs where one junction is open and the conductances are roughly half of what a proper SQUID should have.

The remaining data is neatly packed along a straight line, showing that as the designed junction overlap area is increased the conductance also increases proportionally. This is also as expected in accordance with a continuum form of Ohm's Law [35]. Note however that opposed to Ohm's law, when extrapolating to an infinitesimally small area a non-zero conductance still remains. This is due to the fact that only one parameter is changed, the width of the top electrode, to result in a change in designed junction area. There is an extra contribution to the conductance coming from the sidewalls, the size of the sidewalls is determined from the height of the bottom electrode × the width of the top electrode. Besides the overlap area of the top and bottom electrode the sidewalls also constitute connecting surfaces where current can flow.

CONDUCTANCE PER UNIT AREA VS JJ AREA

It is clear that a SQUID with a bigger designed junction area will also have a higher conductance. However, this result does not give much information on the condition of the tunnel barrier itself. It is important to be able to compare SQUIDs with different sizes in a fairer way. This can be done by calculating the conductance per unit area G/A. The data from sample N. x 3e[4] has been plotted in this way in figure 4.2.

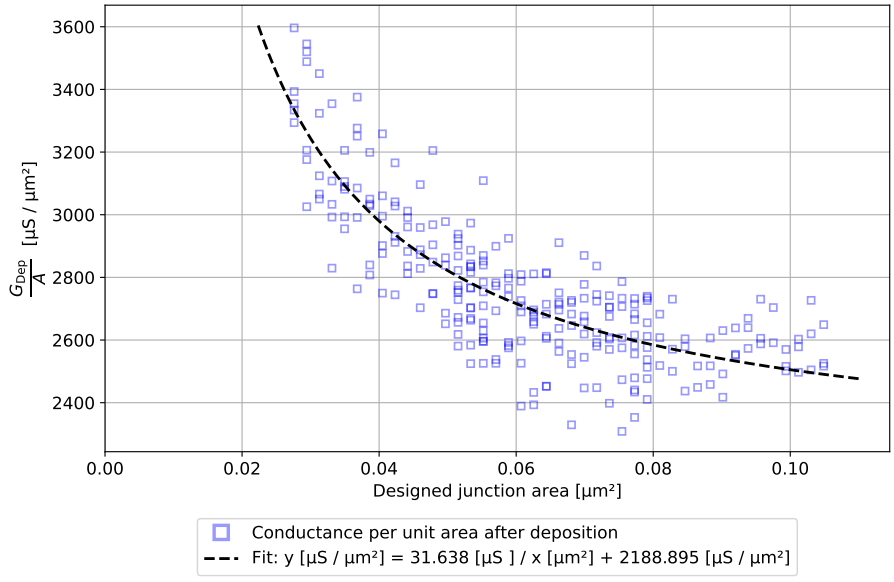


Figure 4.2: A plot showing the reciprocal dependence between designed junction area and conductance per unit area G_{Dep}/A. The black dashed fit line is obtained from doing a curve fitting routine from the `Python` package called `scipy`. This applies ordinary least squares linear regression to find an optimized line through the data.

For a normal resistive circuit component this should form a horizontal line, as the conductance increases the area also increases at the same rate and at 0 area the conduc-

tance would be 0. However, in this case because of the non-zero offset an inverse relation is found. For large junction areas the fit has an asymptote which tends towards a constant value of approximately 2189 µS µm^{-2}. Later, when comparing different datasets with each other it is convenient to compare these numbers. It allows to make a more general comparison between the conductive capabilities of the tunnel barriers from different datasets.

However, within one dataset the G/A values for individual data points are still greatly influenced by this reciprocal effect. Resulting in the smallest junctions having G/A values of about 1000 to 1400 µS µm^{-2} higher.

4.2. Role of Capping Oxidation

The results shown in the previous section come from a not-capped Manhattan style sample. Where the absence (or presence) of capping refers to the exclusion (or inclusion) of a final capping oxidation step as indicated in section 3.1.6. Both the tunnel barrier and the capping layers consist of the same material AlO_x.

4 cases - Dolan/Manhattan and capped/not-capped after deposition

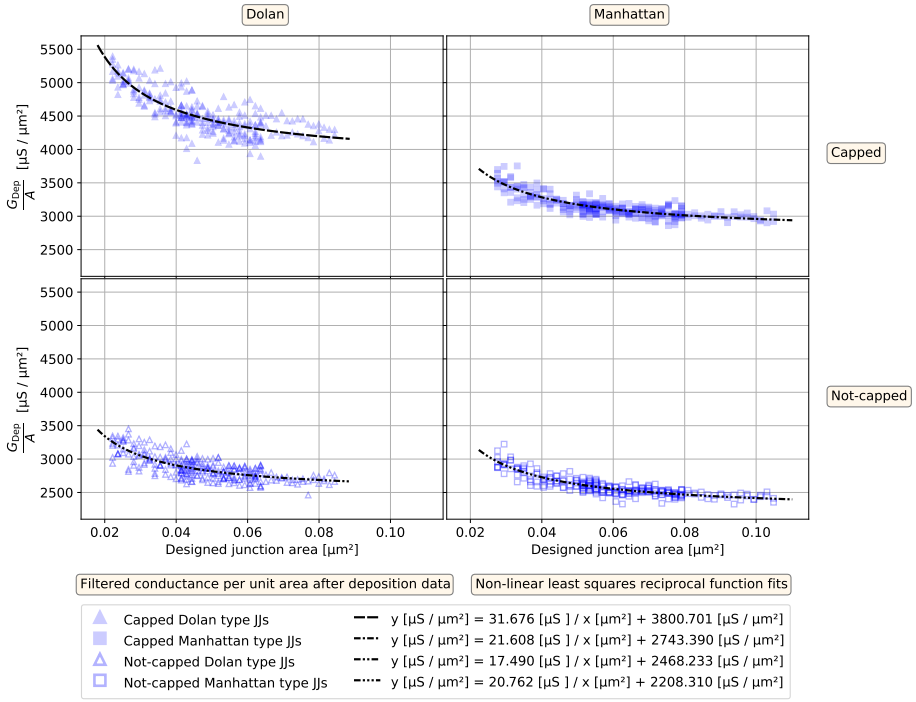


Figure 4.3: Plots showing the reciprocal dependence between designed junction area and conductance per unit area after deposition G_{Dep}/A for 4 cases with Dolan/Manhattan (△/□) and capped/not-capped (filled/unfilled symbol). The functions corresponding to the black dashed and dash dotted fit lines are also given in the legend.

When studying the conductive capabilities of the tunnel barrier and how they change due to annealing it is important to also include the role of the capping layer. Therefore, both samples with and without capping oxide are investigated. In addition, the annealing characteristics of junctions of both the Dolan and Manhattan types are examined. The results for 4 unique datasets are compared in figure 4.3. When looking at these plots it shows that the not-capped datasets have significantly lower conductances per unit area. Suggesting that the capping oxidation either improves the overall conductance or that without capping oxidation the conductances would be diminished to a lower level between deposition and measuring. The data for this figure comes from the following samples (following the order of the legend): F. i 1c, F. x 4e, F. i 4c and F. x 1e.

4.3. DEPENDENCE ON ANNEALING PARAMETERS

So far, all results shown came from data taken directly after deposition. In this section the change in conductance per unit area due to an annealing process is investigated. There are several parameters related to the annealing process that constitute what the overall change will look like. The ones investigated here are heating method, annealing temperature and # of heating rounds.

4 CASES - DOLAN/MANHATTAN AND CAPPED/NOT-CAPPED AFTER AB ANNEALING

The first method that was used to anneal the samples was the simulated airbridge annealing process as described in subsection 3.4.1. The samples are heated by putting them on a hotplate at 200°C. The resulting changes in the conductances per unit area can be seen in figure 4.4. The $\Delta G/A$ values are calculated using the G_{Dep} coming from the same samples as before shown in figure 4.3 (F. i 1c, F. x 4e, F. i 4c and F. x 1e).

Both of the not-capped datasets show a general increase in G/A around 300 to $500\,\mu\text{S}\mu\text{m}^{-2}$. While the capped Manhattan style junctions show almost no change in G/A. The results for the capped Dolan style junctions are totally different. The G/A has decreased by about $1000\,\mu\text{S}\mu\text{m}^{-2}$. Showing the aging effect that annealing can have on junctions under certain circumstances. When looking at G_{Dep}/A for these junctions as shown in figure 4.3, notice that these were already at a high level. Even though there is this aging effect, the conductances per unit area after the AB annealing step G_{AB}/A are still at a high level compared to the other datasets.

The first term in the fit for the capped Dolan style junctions is also the only one here being negative. This is visible in the data sloping down as the designed junction area is decreased. This can be understood in the following way, if one were to look at just the linear conductances plots the G_{Dep} has a higher offset than G_{AB}. Then when the difference between these two is taken the resulting offset will be negative. In the end the division by the area is done and the result is this negative reciprocal relation. From this it can be said that SQUIDs with smaller JJs are annealed more per unit area, but because of their small size the total amount of annealing is still bigger in the SQUIDs with larger designed junction areas.

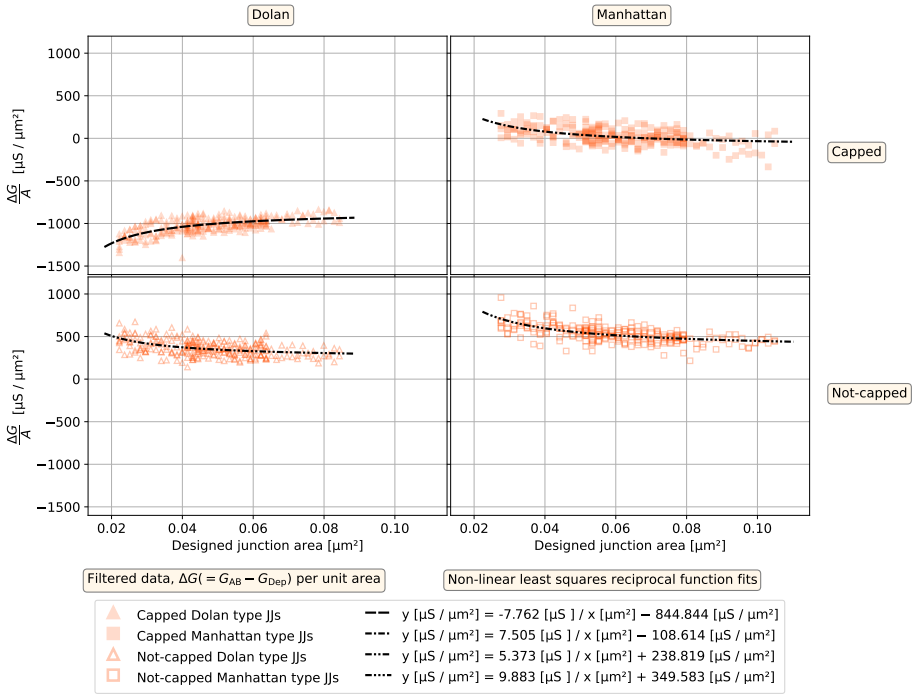


Figure 4.4: Plots showing the reciprocal dependence between designed junction area and change in conductance per unit area $\Delta G/A$ due to AB annealing for 4 cases with Dolan/Manhattan (△/□) and capped/not-capped (filled/unfilled symbol). The functions corresponding to the black dashed and dash dotted fit lines are also given in the legend.

4 CASES - DOLAN/MANHATTAN AND CAPPED/NOT-CAPPED AFTER RTA TREATMENT

The next method that was used to anneal the samples was the rapid thermal annealing (RTA) process as described in subsection 3.4.2. The samples are heated by loading them into a process chamber where either pure nitrogen gas or forming gas is heated using halogen lamps to a setpoint of 200, 300 or 400°C.

The resulting changes in the conductances per unit area for samples heated with either 200 or 300°C nitrogen gas for 2 minutes can be seen in figure 4.5. The $\Delta G/A$ values are calculated from the samples with the following labels (following the order of the legend): N. i 1e, N. i 2e, N. x 4e, N. x 3e, N. i 3e, N. i 4e, N. x 1e, and N. x 2e.

In all 4 cases the $\Delta G/A$ values for the samples heated at the lower temperature of 200°C are above those heated at 300°C. In this case all data shows a decrease in G/A except for the Manhattan samples annealed at 200°C. For the capped JJs some show a slight increase, but overal the change is small. For the not-capped JJs a slight increase around $150\,\mu S\mu m^{-2}$ can be seen.

In general, the difference between the two fit lines seems to be biggest for the not-capped datasets. For Dolan type JJs there is a difference of about $500\,\mu S\mu m^{-2}$, and for Manhattan it is about $950\,\mu S\mu m^{-2}$. This suggests that perhaps the presence of the capping oxide layer suppresses the effect which could tune the conductances to increase.

The absence of the capping oxide layer for the plots in the bottom row then allows the tunnel barrier to anneal differently depending on the set temperature. Even showing an increase on the bottom right plot when the temperature is set to 200°C.

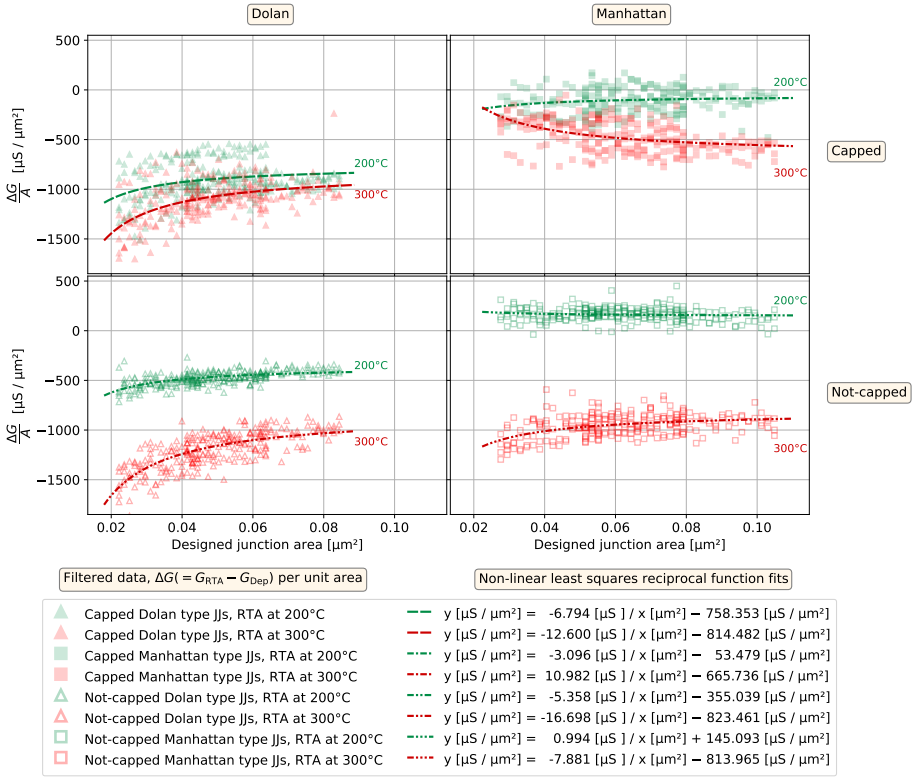


Figure 4.5: Plots showing the reciprocal dependence between designed junction area and change in conductance per unit area $\Delta G/A$ due to RTA at either 200/300°C (green/red) for 4 cases with Dolan/Manhattan (△/□) and capped/not-capped (filled/unfilled symbol). The functions corresponding to the green/red dashed and dash dotted fit lines are also given in the legend.

So far, the most success in tuning up the conductances has been had with not-capped Manhattan type junctions. For both the AB and RTA annealing at 200°C a slight increase in the conductances was measured. It is for this reason that most of the research effort after this have been focussed on similar experiments.

NOT-CAPPED MANHATTAN JJS

Besides annealing in nitrogen gas, the RTA system also has the availability to fill the processing chamber with forming gas, a mixture of nitrogen and hydrogen gasses (90% N_2/ 10% H_2). Forming gas is also used in the industry to drive out moisture and oxygen on photographic films and sometimes as a reducing agent for high-temperature soldering to suppress oxidation of the joint [36, 37]. Both the oxygen and moisture content are expected to play a role in aging and anti-aging of the junctions.

In figure 4.6 a plot can be seen showing the $\Delta G/A$ values as function of designed junction area for the data from 3 samples (N. x 1e, N.x $3e^2$ and N. x $3e^4$). These samples contain not-capped Manhattan JJs and are annealed at a temperature of 200°C using either nitrogen or forming gas.

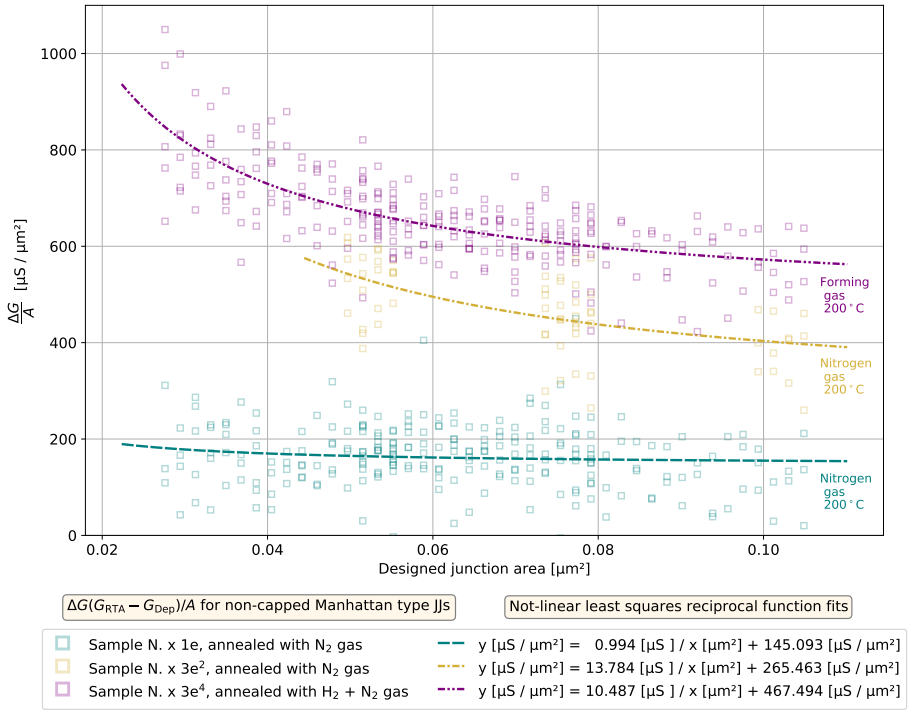


Figure 4.6: A plot showing the reciprocal dependence between designed junction area and the change $\Delta G/A$ for 3 datasets of not-capped Manhattan type JJs. The functions corresponding to the teal, yellow and purple dashed and dash dotted fit lines are also given in the legend. The corresponding sample names, as well as the gas used for annealing, are shown on the left column. For sample N.x $3e^2$ less data was gathered as this was part of the consecutive RTA steps study for which there was less time available to gather data during each step.

It is clear from the plot that the sample treated with forming gas was annealed more. The presence of H_2 molecules, instead of solely N_2, could possibly have aided in an additional increase of the conductances . For large junctions, an increase in G/A of about $467\,\mu S\mu m^{-2}$, for the smaller junctions' values of $800\,\mu S\mu m^{-2}$ and higher are reached. This is the highest degree of up tuning that is reported in this study.

One possible problem with forming gas is that hydrogen-based tunnelling defects in alumina form so called two-level systems (TLS) [38]. These form a decoherence channel for the qubit meaning that the qubit states are less long-lived. A short paragraph on decoherence can be found at the end of appendix A. It is likely that the use of forming gas would also introduce extra TLS making it detrimental to use when fabricating quantum processors.

CONSECUTIVE RTA STEPS OF 2 MINUTES

So far, the experiments reported would always involve an RTA step at which the sample is held at a high temperature for 2 minutes. As can be seen in figure 2.10a (from another study) after the first round of annealing in forming gas at 200°C a certain level was reached from which there was no big deviations in the resistances when doing subsequent rounds. Based on that the expectation was that one round of heating would be enough to reach a maximum amount of anti-aging. Of course, it is useful to check this again for our experiments. Two samples (top plot N. x $3e^2$, bottom plot N. x $4e^2$) with not-capped Manhattan JJs have been tested by annealing them multiple times using nitrogen gas, the results can be seen in figure 4.7.

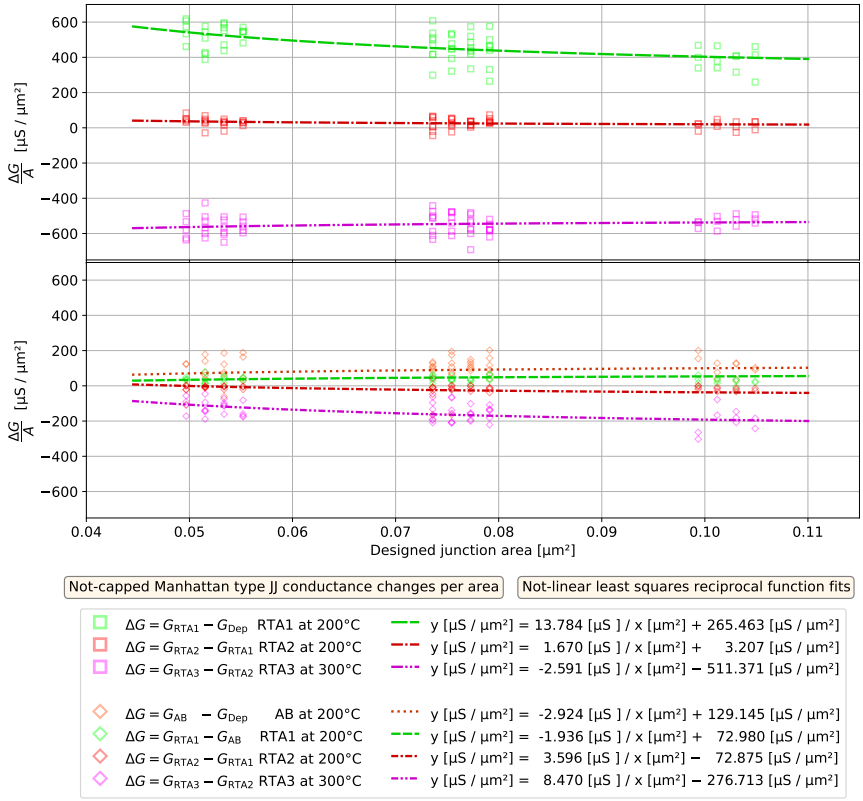


Figure 4.7: Plots showing the reciprocal dependence between designed junction area and the change $\Delta G/A$ for 2 samples with not-capped Manhattan type JJs when doing 3 rounds of RTA, for the sample shown in the bottom plot prior to the first RTA an AB anneal is done. The functions corresponding to the green, red and magenta dashed and dash dotted fit lines are also given in the legend, they correspond to the change after the first, second and third round of RTA respectively. The AB anneal is shown using an orange dotted line. The corresponding sample names, as well as the gas used for annealing, are shown on the left column. For sample N.x $3e^2$ less data was gathered as this was part of the consecutive RTA steps study for which there was less time available to gather data during each step.

For one of the samples there was an additional round of AB anneal between the deposition and the first round of RTA. Previously, this resulted in an increase of G/A of roughly $350\,\mu S\mu m^{-2}$ as can be seen in figure 4.4. However, here the increase is only $130\,\mu S\mu m^{-2}$. After that both samples have been annealed using nitrogen at 200°C twice. At this time, it was noticed that the second round had little effect on the conductances of both samples as can be seen by the red dash dotted lines being near 0. The sample where no AB anneal step was done also has a bigger increase in G/A, namely $265\,\mu S\mu m^{-2}$ for large junctions. This is higher than the combined effect of the AB anneal and first annealing step for the sample shown on the bottom plot.

After these two rounds of annealing, it was decided to anneal at a higher temperature of 300°C to see how that would affect the G/A. For both samples, a decrease in G/A is observed. Where the plot on the top shows a decrease of roughly $511\,\mu S\mu m^{-2}$. Bringing the conductances down to a level lower than was started with after deposition. For the second sample this is also the case, but the effect is weaker. From these experiments it also seems that 1 round of 2 minutes RTA at 200°C is sufficient for the tunnel barrier annealing to be either surfeited or nearly reaching the maximum effect that is sought after.

TABLE SUMMARIZING EXPERIMENTAL RESULTS

To give an overview of the findings for all relevant annealing experiments the results are summarized in table 4.1.

Table 4.1: Summary of measured devices, showing the change in conductance per unit area in $\mu S \mu m^{-2}$ due to different annealing steps. These values are determined from the asymptotic behaviour for large junctions.

Sample	Base material	JJ type	Capping	$\frac{G_{AB} - G_{Dep}}{A}$	RTA	$\frac{G_{RTA} - G_{Dep}}{A}$
F. i 1c[a]	Sput. NbTiN	Dolan	Yes	-845[b]	400 °C	-2070
F. i 4c[c]	Sput. NbTiN	Dolan	No	+239	400 °C	-956
F. x 4e	Sput. NbTiN	Manhattan	Yes	-109	400 °C	-1606
F. x 1e	Sput. NbTiN	Manhattan	No	+350[b]	400 °C	-1100[b]
N. i 1e	ALD TiN	Dolan	Yes	-	200 °C	-758
N. i 2e	ALD TiN	Dolan	Yes	-	300 °C	-814
N. i 3e	ALD TiN	Dolan	No	-	200 °C	-355
N. i 4e	ALD TiN	Dolan	No	-	300 °C	-823
N. x 1e	ALD TiN	Manhattan	No	-	200 °C	+145
N. x 2e	ALD TiN	Manhattan	No	-	300 °C[d]	-814
N. x 3e	ALD TiN	Manhattan	Yes	-	300 °C[d]	-666
N. x 4c[e]	ALD TiN	Manhattan	Yes	-	-	-114[b]
step 2					200 °C	+377[b]
N. x 3e[2]	ALD TiN	Manhattan	No	-	200 °C	+265[b]
step 2					200 °C	+269[b]
step 3					300 °C	-243[b]
N. x 4e[2]	ALD TiN	Manhattan	No	+129[b]	200 °C	+202[b]
step 2					200 °C	+129[b]
step 3					300 °C	-147[b]
N. x 3e[3]	ALD TiN	Manhattan	No	-	300 °C[f]	-320
N. x 3e[4]	ALD TiN	Manhattan	No	-	200 °C[f]	+467
N. x 4e[3]	ALD TiN	Manhattan	No	-	400 °C[f]	-933
N. x 4e[4]	ALD TiN	Manhattan	Yes	-	200 °C[f]	+70

[a] The deposition and simulated AB were spaced by 5 days.
[b] This result was obtained using 2 point conductance measurements.
[c] The simulated AB and RTA were spaced by 6 days.
[d] The RTA was unstable and reached 450 °C at the start.
[e] This sample was stored in a nitrogen environment for a week before annealing.
[f] During this experiment forming gas was used.

The results of this table can be inferred as follows:

1. It is observed that the capping oxidation plays an important role in the directionality of the junction aging. In the absence of this layer a net increase in the conductances is observed if the annealing temperature is maintained at 200 °C. There is an exception for the device with identifier N. i 3e where the conductances decreased

post RTA at 200 °C.

2. Conversely in the presence of the capping oxidation layer the conductances decrease irrespective of the type of annealing or temperature. The samples with identifier F. x 4e and N. x $4e^4$, are two exceptions, there the conductances stayed relatively at the same level.
3. Experiments with RTA at 300 or 400°C with or without capping oxidation showed a decrease in conductances. When the temperature was maintained at 400°C a larger reduction in the conductances was observed indicating the aging process is proportional to temperature that higher temperatures lead to more aging.
4. In general, there seems to be a difference in aging due to annealing for Dolan bridge versus Manhattan type junctions. It was observed that the Manhattan type junctions anti-aged under the previously described environmental conditions while this was not observed for Dolan bridge type junctions.

The table shows that in most cases the simulated air bridge (AB) step increases the conductances of the junctions. Only for one device this is not the case, and that result is disputable as the sample was stored for 5 days in between the deposition and simulated AB. In that time the sample was stored in a box under weak vacuum, intermittently other samples were being taken out introducing contaminants into the box. It is likely that during this time the sample may have aged resulting in a decreased conductance. It is also unclear what happens during the simulated AB if there are contaminants at the surface of the sample.

In several Manhattan devices rapid thermal annealing (RTA) at 200 °C shows anti-aging, the conductances are increased. The effect seems to be present in only not-capped samples, as well as the sample which was stored in a nitrogen environment for a week. This could be an indication that extraneous atoms/molecules are responsible for the change in conductance after RTA treatment. However, it is still unclear what the dynamics are and why the effect has not been measured for not-capped Dolan bridge junctions.

YIELD AFTER DEPOSITION

Some devices show a conductance which is more than 30% removed from what is expected at a specific designed junction area according to the fit lines. These correspond to SQUID devices where one of the JJs is functioning properly, but the other JJ is either open or shorted. For this reason, these datapoints are removed and a new fit is obtained. With this new fit the data is filtered once more, obtaining a final filtered dataset and fit. Figure 4.8 shows the amount of SQUIDs with specific defects (filtered, opens, shorts) directly after deposition.

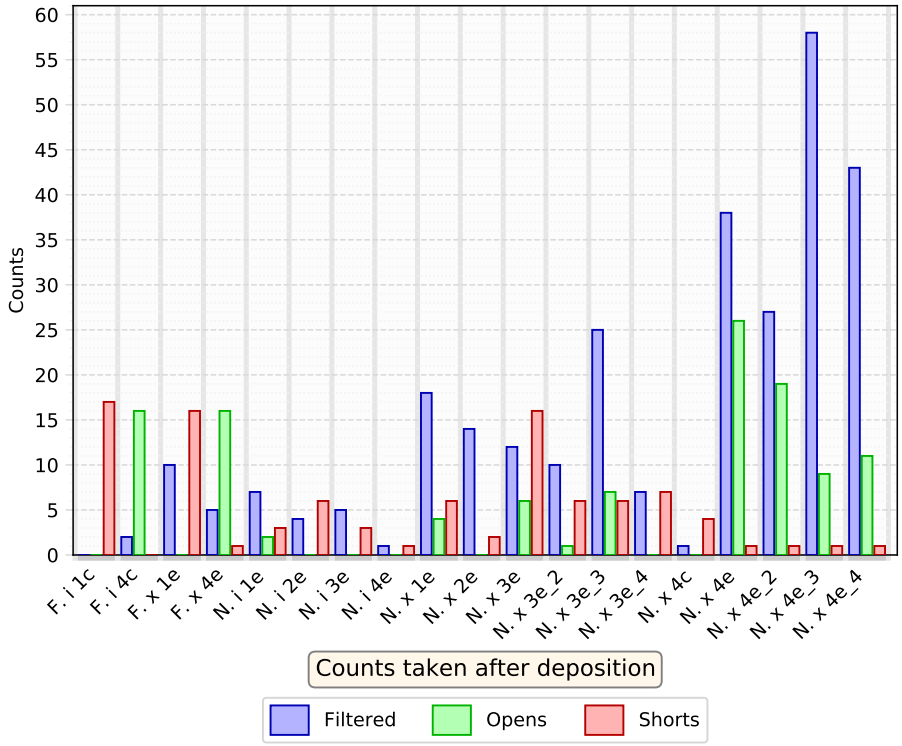


Figure 4.8: A bar plot showing the frequency of SQUIDs having fabrication flaws and failures. For reference the samples labelled with an F have 256 SQUIDs on them, the ones labelled with a N have 272 SQUIDs.

YIELD AFTER RTA

It is interesting to know if the RTA treatment would impact the yield of devices. To check this the amount of SQUIDs with specific defects (filtered, opens, shorts) after an RTA treatment is shown in figure 4.9. Notice that counts are similar to those seen in figure 4.8 meaning that the RTA treatment does not introduce a substantial amount of new flaws and failures in the SQUIDs.

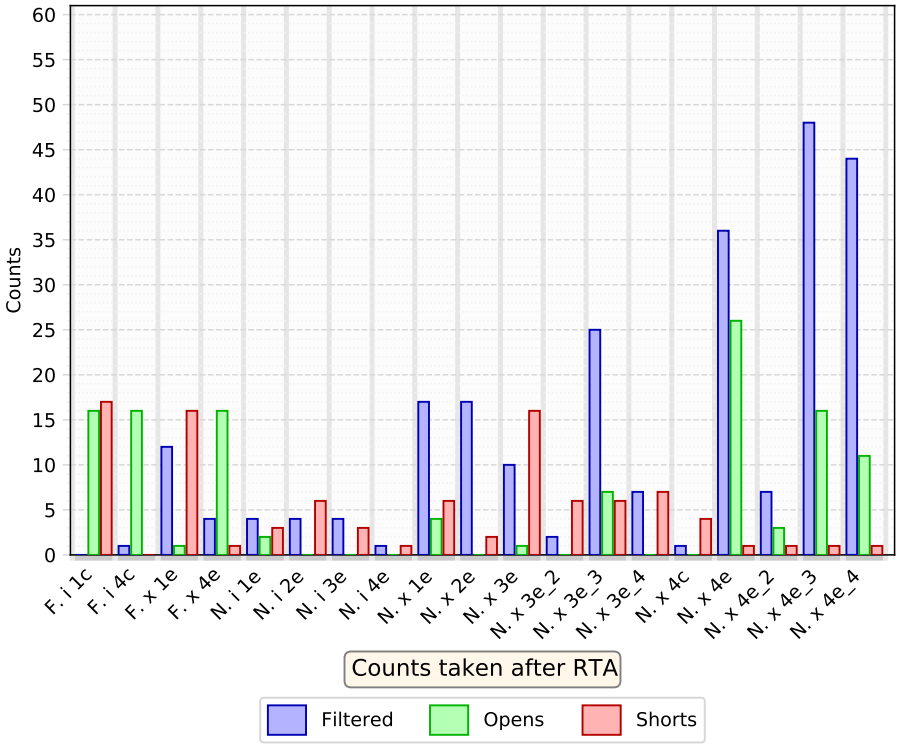


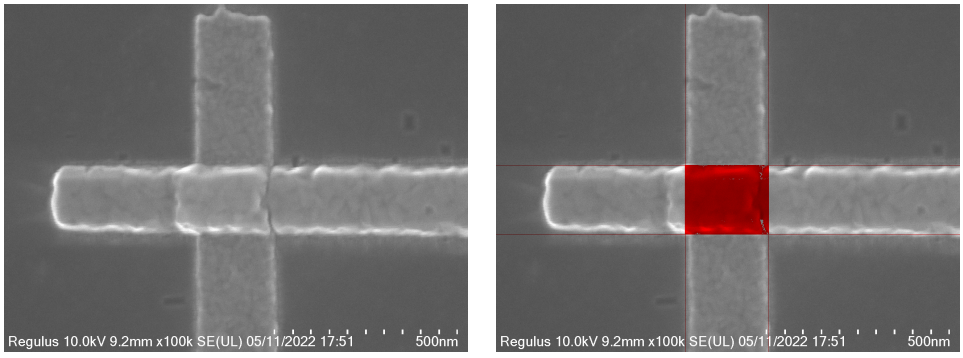
Figure 4.9: A bar plot showing the frequency of SQUIDs having flaws and failures after submitting them to the RTA treatment. For reference the samples labelled with an F have 256 SQUIDs on them, the ones labelled with a N have 272 SQUIDs.

4.4. ACCURACY OF DESIGNED JOSEPHSON JUNCTION AREA

In this report, each time a variable is plotted against the junction area, it is done so only in relation to the designed junction area. However, due to technical constraints and possible fabrication deformities the actual junction overlap area can differ. To gain insight into the accuracy of the designed Josephson junction area compared to the actual overlap area SEM pictures of die N. x 3e^4 have been taken. In total 24 pictures have been taken of the JJs from 12 SQUID loops. These Manhattan junctions have bottom electrodes with a designed width of 160 nm, the designed widths of the top electrodes vary in a range from 60 to 228 nm.

Figure 4.10a shows a 100× zoomed in picture of a Manhattan type Josephson junction. Using the `Pyclq` software package the image has been analysed. The software makes use of image recognition techniques to locate the electrodes and uses this to determine the overlap area of the JJ. A more detailed description of `Pyclq` can be found in the following thesis "`Pyclq`: Image analysis suite for fabrication and metrology of superconducting quantum processors" [29].

Figure 4.10b shows the resulting image after processing with `Pyclq`, this image shows the JJ overlap area shaded in red. The generated image can be used to quickly verify that the area the code calculates correctly corresponds to the true overlap area.



(a) The raw image taken by the SEM.

(b) The computed electrode overlap area is shaded red.

Figure 4.10: Pictures showing a 100× zoomed in image of Junction D5 a2 R (D5 refers to the middle 4 × 4 array, a2 refers to the SQUID in row 2 and column 2, R refers to the junction on the right side of the SQUID loop) from sample N. x 3e^4. The image was taken with a scanning electron microscope (SEM).

COMPUTED JOSEPHSON JUNCTION AREA

The computed JJ area for the SQUID loops and their error is plotted vs the designed JJ area in figure 4.11. The error bars indicate one standard deviation of uncertainty as determined by `Pyclq`, this is based on the uncertainty with which the location of the electrode edges is resolved. In almost all cases the computed area is slightly higher than the designed area. This is because of the electrodes having higher widths than designed, which could be due to limitations in the fabricated pattern on which the electrodes are deposited. The layout on the die after patterning with the EBPG and developing that

pattern is surmised to systematically be bigger than designed. Especially for the smaller parts in the layout. This could be due to the way the designed pattern is handled and how it is exposed using a beam with a finite spot size. This can also explain why this offset is more pronounced in the figure for the smaller overlap areas.

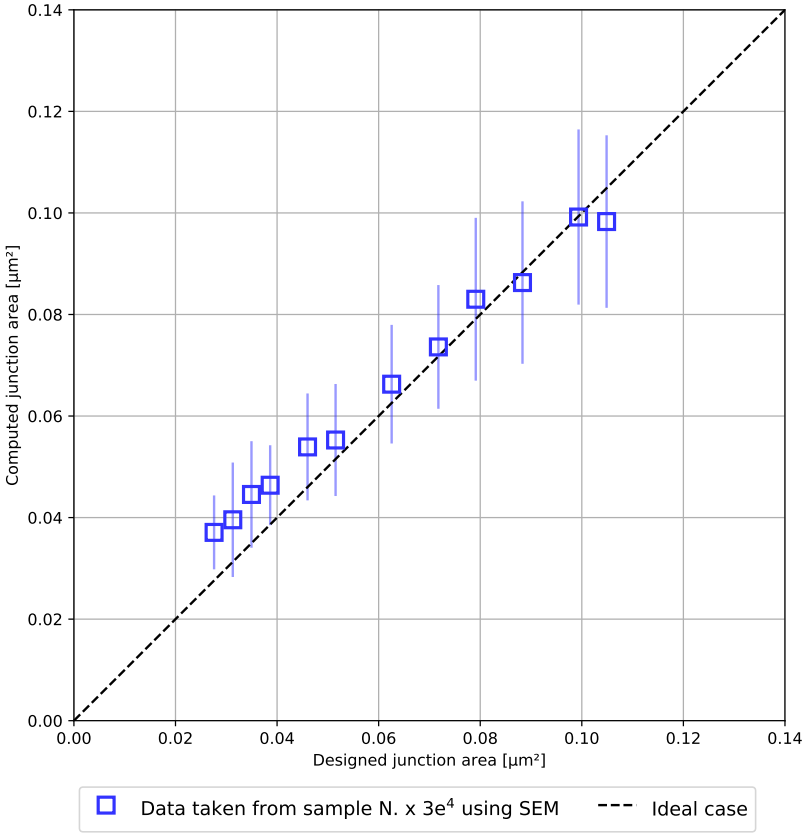


Figure 4.11: A plot showing the computed versus designed junction area. The data was taken from sample N. x $3e^4$ directly after finishing the RTA experiments on the die. Note that for both the designed and computed junction area the junction sidewalls are also included in the value thus the line for the ideal case goes through the origin.

4.5. EFFECT OF AMBIENT ENVIRONMENT ON JOSEPHSON JUNCTION ANNEALING

Besides the conductances changing due to an annealing process, the conductances of the JJs will also slowly degrade over time due to the interaction with the environment. To understand the effect of aging on JJs as described in this report two samples have been stored in an ambient environment to observe the decrease in the conductances.

TEMPORAL CHANGES TO CONDUCTANCES, JUNCTION AGING

Figure 4.12 shows that after 7 days there is already a decrease of roughly $110\,\mu S\mu m^{-2}$ in G/A. When looking at junctions which have been stored for even longer, namely 45 days, the G/A values show a decrease of about $640\,\mu S\mu m^{-2}$. This is a considerable amount and comparable to the effect of annealing at high temperatures. It is thought that the origin of the decrease in conductance between these two different effects is the same. Which is why annealing at high temperatures is described as speeding up the natural aging process that occurs in an ambient environment.

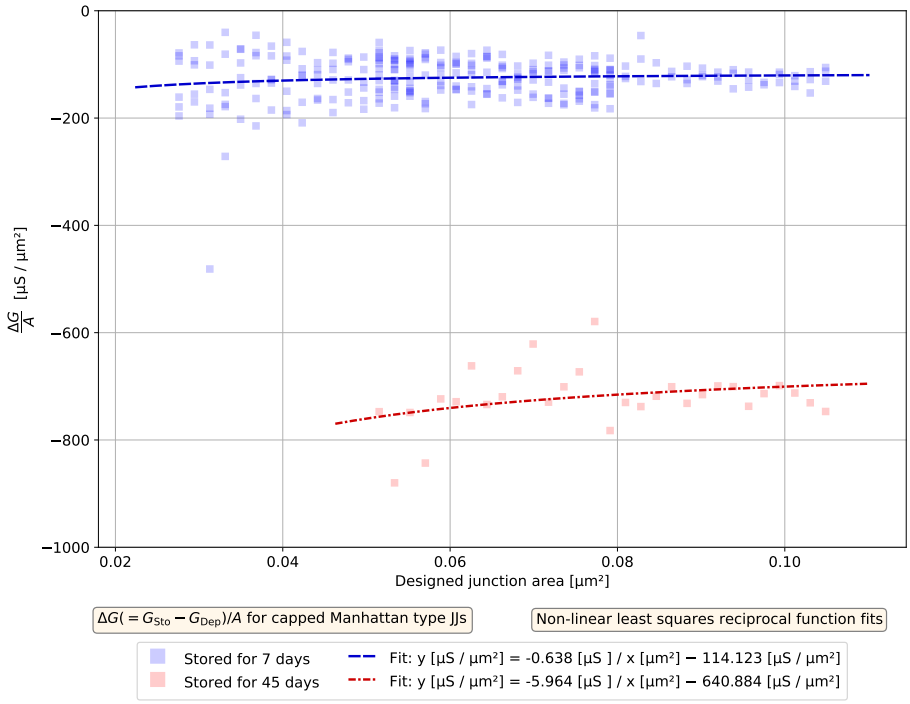


Figure 4.12: Plots showing the reciprocal dependence between designed junction area and change in conductance per unit area $\Delta G/A$ for 2 samples with capped Manhattan junctions which have been stored for a period. The functions corresponding to the blue/red dashed and dash dotted fit lines are also given in the legend.

REVERSING THE TEMPORAL CHANGES TO CONDUCTANCES, JUNCTION ANTI-AGING

Figure 4.13 shows what happens to the conductances after treating the stored samples with nitrogen gas at 200 and 300°C. In both cases there is a large increase in the conductances, roughly 380 and 720 $\mu S \mu m^{-2}$ for the samples stored 7 and 45 days, respectively. There is also a large spread in the datapoints showing the volatility of the anti-aging effect. This means that it would be more difficult to develop a well-controlled method to anti age junctions a specific amount.

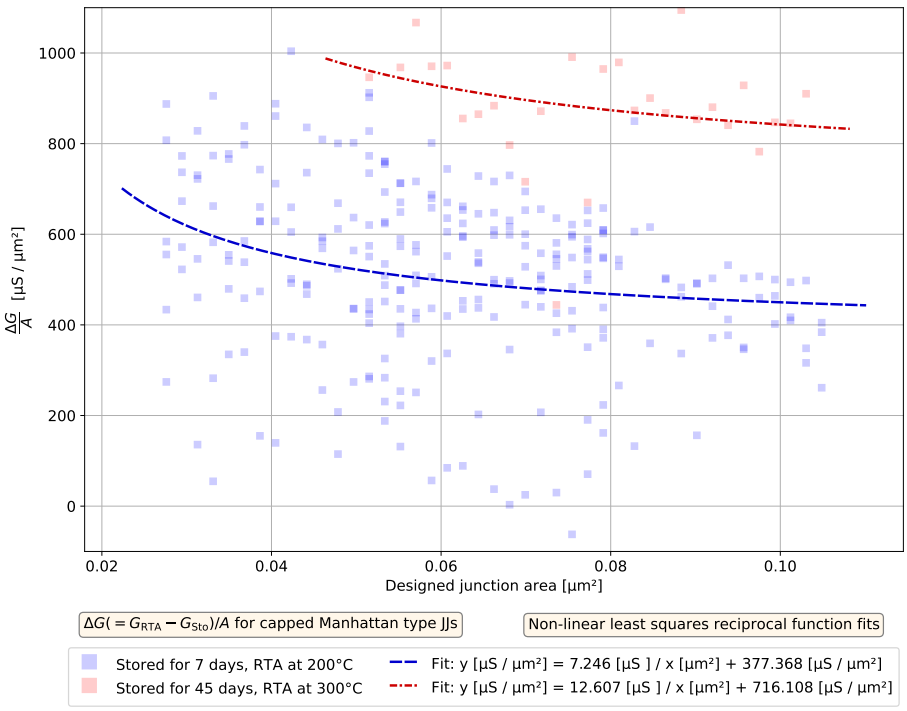


Figure 4.13: Plots showing the reciprocal dependence between designed junction area and change in conductance per unit area $\Delta G/A$ for 2 samples with capped Manhattan junctions which have been annealed after the storage period. The longer the devices are stored the more they age and thus also the anti-aging effect in conductance is bigger.

Interestingly enough if we compare the new conductance values after anti-aging with the conductances directly after deposition it is found that these are even higher than the original conductances after deposition, this is shown in figure 4.14

In this case it is clear that the RTA at 200°C still outperforms the RTA at 300°C in the ability to increase the G/A values. Some of the junctions even reached a change of approximately 800 $\mu S \mu m^{-2}$ which is similar to the highest increases in G/A that were observed for the RTA experiments with sample N. x $3e^4$.

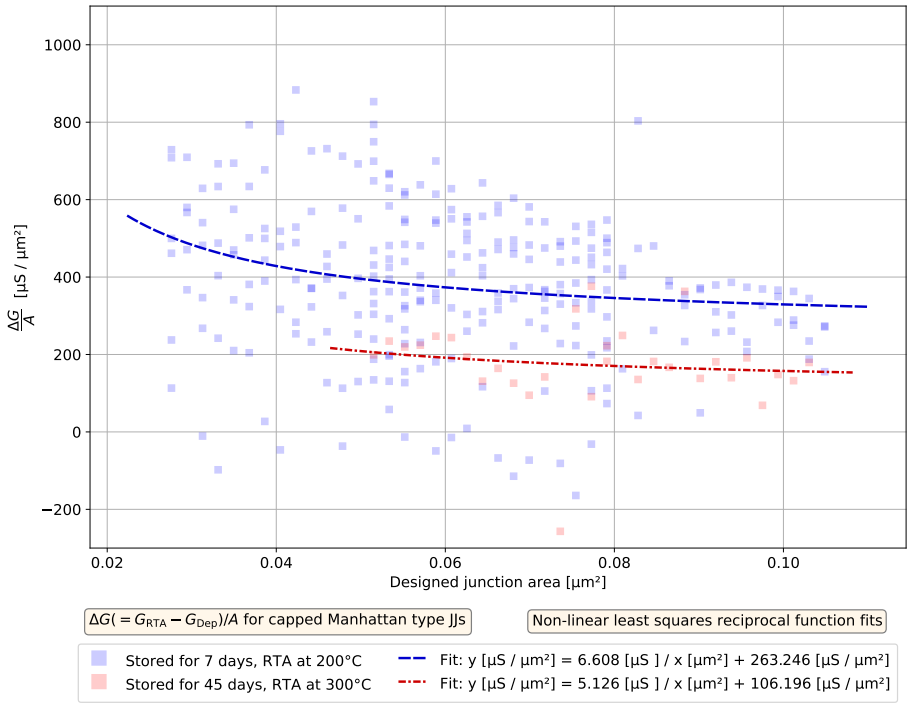


Figure 4.14: Plots showing the reciprocal dependence between designed junction area and change in conductance per unit area $\Delta G/A$ for 2 samples with capped Manhattan junctions which have been annealed after the storage period. The devices reach new conductance values which are higher than the values which are measured directly after the deposition.

THE IMPORTANCE OF RECORDING DATE OF EXPERIMENT STEPS

In the plots above it has been shown that the G/A values of junctions stored in an ambient environment decrease over time. This in turn affects the sample's response to an annealing treatment. When samples that are still relatively 'fresh' (aged less than a week) are annealed using either nitrogen or forming gas at 300°C no increase in G/A was observed. However, extensive aging of a month and a half shows that this consistent response to annealing changes. The amount of aging that samples endure depends on the kind of environment used for storing as well as the duration. Because of this, it is important to document the date of deposition and annealing, unfortunately this isn't disclosed in some of the literature [7, 8, 10, 11]. This makes it more difficult to interpret and compare their results. To provide some insight in the aging that may have occurred for samples in the experiments done during this project the date of events are recorded in a logbook in appendix B.

4.6. DIE-TO-DIE DEPOSITION STATISTICS

In this section the statistical data regarding conductances for the deposited samples are analysed.

NORMALIZED HEATMAPS

To determine if the conductance values are dependent on the region the JJ is located on the sample, a statistical analysis on sets of data from samples with the same JJ type has been done. The result of this analysis can be seen in the heatmaps shown in figure 4.15.

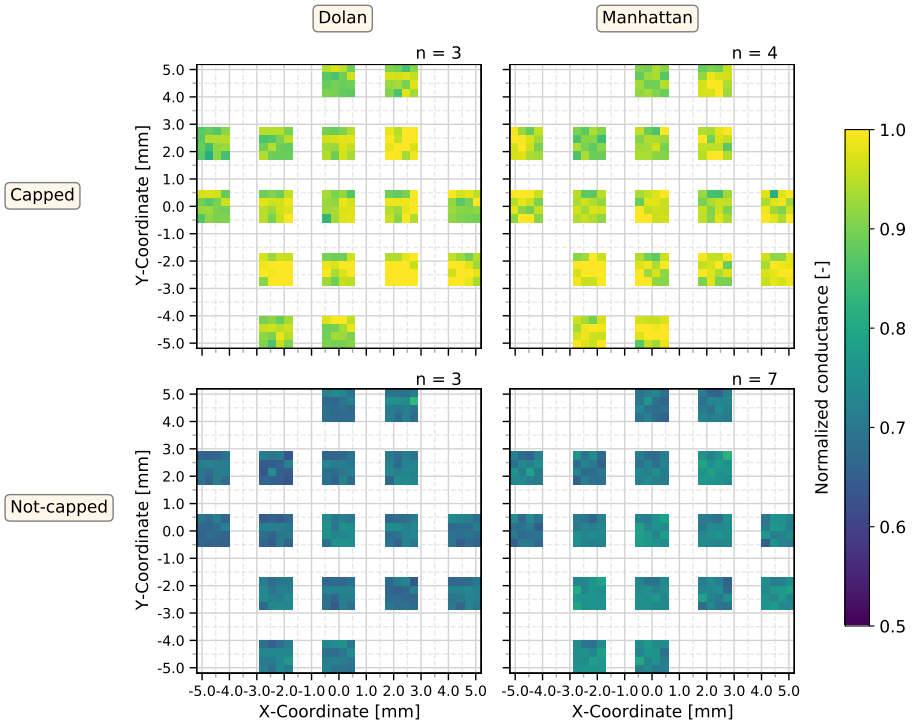


Figure 4.15: Heatmap showing the normalized conductances for 4 cases with Dolan/Manhattan and capped/not-capped. The normalized average conductance values are relatively uniform over the sample. It is also clear that capped junctions generally have higher conductances than their not-capped counterparts. The values are calculated in the following way: first the average conductances are calculated for junctions of the same type (Dolan/Manhattan), capping and location. These mean values are calculated for each case separately, where the n values indicate how many samples are included in the calculation. After this max normalization is applied to these averages. Per area the maximum averaged conductance values are selected from the two sets of averages for the device type (capped and not-capped), all JJs of the same area are then divided by this maximum.

The normalized average conductance values are relatively uniform over the entire sample region. This means that within die level the conductance values do not depend much on the location on the die. There might still be variations in the conductance values when one would look at the location of the JJ on the wafer. There the difference

between being at the centre or edge is a lot bigger. For size reference, the dies are diced from the wafer using a 4×4 grid. It is also clear from the figure that capped junctions generally have higher conductances than their not-capped counterparts. Which at first sounds counterintuitive as the oxygen in the capping layer is expected to be related to a higher resistance. It is the oxygen that is used to form the tunnel barrier. One explanation could be that the capping layer fills up areas were normally there would be no material. When looking at the design of the junctions as shown in the models in figures 2.5 and 2.6 or in the SEM images in figures 3.8 and 3.9 when covering the top electrode with an additional layer of material a larger interface connecting the two electrodes could be formed. For not-capped dies there are parts where there is just empty space which for the capped dies could now be occupied with AlO_x instead.

REPRODUCIBILITY

To show the variation in between the datasets used to create figure 4.15 the average G/A values and their standard deviation for each sample are shown in figure 4.16.

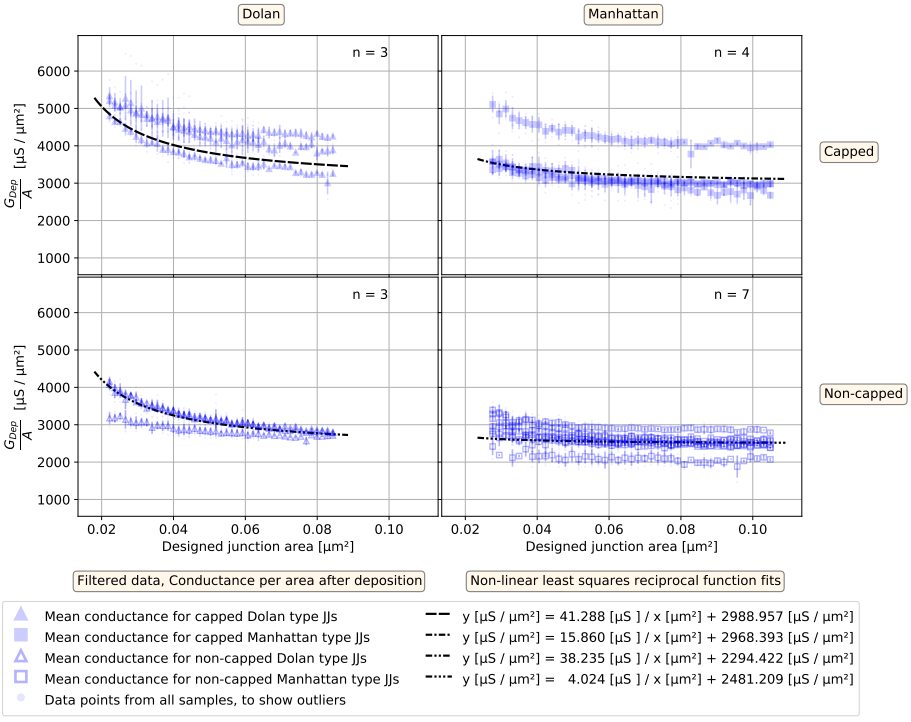


Figure 4.16: Plots showing the variation in the conductances per unit area G/A after deposition for 4 cases with Dolan/Manhattan (△/□) and capped/not-capped (filled/unfilled symbol). This shows how reproducible and controlled the deposition technique and recipes are. The functions corresponding to the black dashed and dash dotted fit lines are also given in the legend, they show the non-linear least squares reciprocal function fits to the combined datasets.

It is again observed that the G/A values and thus the conductances for the capped

JJs are higher than the not-capped counterparts. It also shows that for some of the cases there is a range of about $1000\,\mu S\mu m^{-2}$ between the lowest and highest average G/A at a specific designed junction area.

From the earlier results, it is clear that the amount a junction can be annealed and consequently tuned depends on the starting conductance. JJs with a larger area and thus higher starting G, can see a bigger change in G. So, samples with in general higher G/A values are also expected to accordingly see a larger $\Delta G/A$. This means that the variation in G/A as seen in the figure is expected to play a role in the variation in $\Delta G/A$ when annealing the JJs.

ALD VS SPUTTERED

In this project both sputtered NbTiN and ALD TiN have been used. Most samples that are investigated had a base layer which was deposited using the ALD technique. To determine whether the technique of forming the base layer significantly affects the results the G/A values after deposition of two samples are compared in figure 4.17. Both samples contain capped Manhattan type JJs coming from the same diced region of the wafer (indicated with the 4e label).

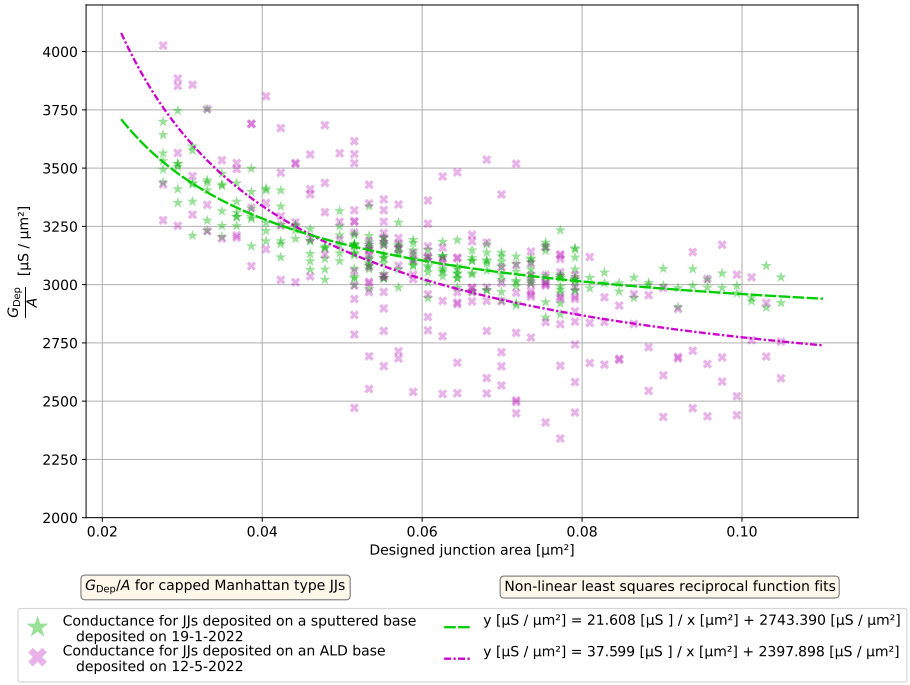


Figure 4.17: A plot showing the reciprocal dependence between designed junction area and G/A for 2 datasets of capped Manhattan type JJs. The green stars and dashed fit line correspond to a dataset (F. x 4e) of which the base layer was sputtered. The magenta crosses and dash dotted fit line correspond to the dataset (N. x 4e) for which the ALD technique was used. The samples show very similar conductances.

In figure 3.7 from the thesis "Wafer scale fabrication of Josephson junctions" [1] a heatmap of the normalized conductances of Manhattan JJs as a function of the position on a wafer with a sputtered NbTiN base layer is shown. The normalization is performed with regard to the mean values. The deposition of the JJs is done separately for each die and shows a larger variation in the conductances when comparing dies, compared to if they would have been deposited on the entire wafer at once. As can be seen in the image the dies in the positions 2c (2nd column centre row) and 1e (1st column edge row) are missing the test array in the middle due to a design mistake. Two new samples have been fabricated and analysed by N. Muthusubramanian and the heatmap for these is shown in figure 4.18.

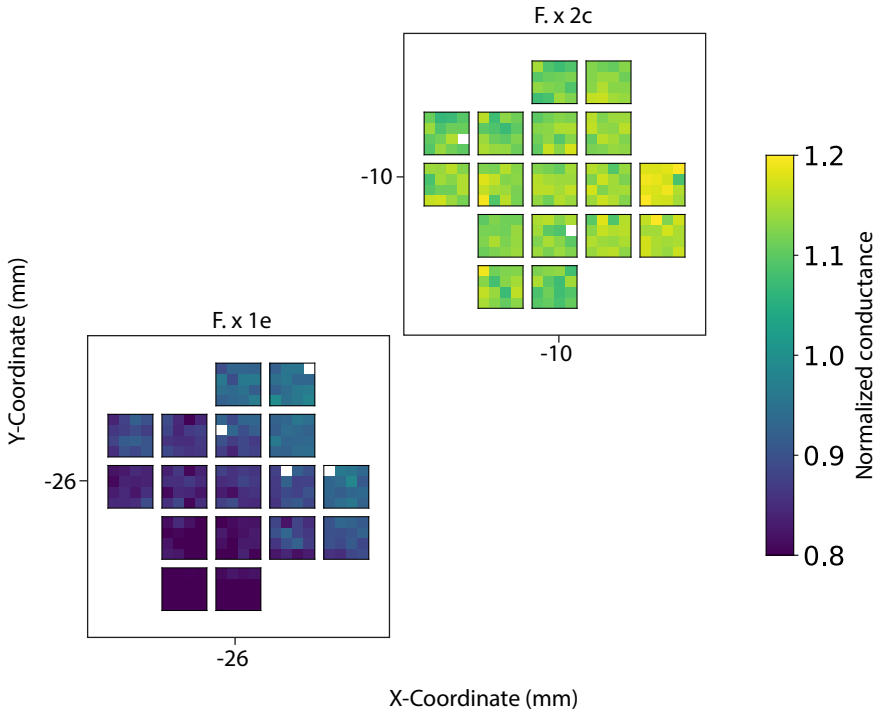


Figure 4.18: Heatmap showing the normalized conductance values for two dies with a sputtered NbTiN base layer. The junctions are Manhattan type and have been capped with oxide. The spatial coordinates of the dies on the wafer are also shown. Note that the label F. x 1e used here is of a similar die but a separate batch than the one reported on in this thesis, figure from [39]

This shows that there is a radial dependence in the conductances from centre to edge for wafers which have a sputtered NbTiN base layer. The effect has been found to be reproducible and has been attributed to contact resistance. This effect has not been observed for samples which have an ALD TiN base layer.

RECYCLING

Wafers with a sputtered/ALD base layer were prepared at the start of the project, later on in the project samples were recycled to reuse them for new experiments. To recycle them the dies were put in MF321 for 3 minutes after which they are washed with water. After that the dies would be in step 2 of the fabrication process flow as shown in figure 3.2. To determine if there is any degradation in the performance of the sample the G/A values after 3 depositions with one sample are shown in figure 4.19. The spread in datapoints looks rather similar and there is only a difference of at most approximately $400\,\mu S\mu m^{-2}$. One thing that is surprising is that on the third deposition the slope is approximately

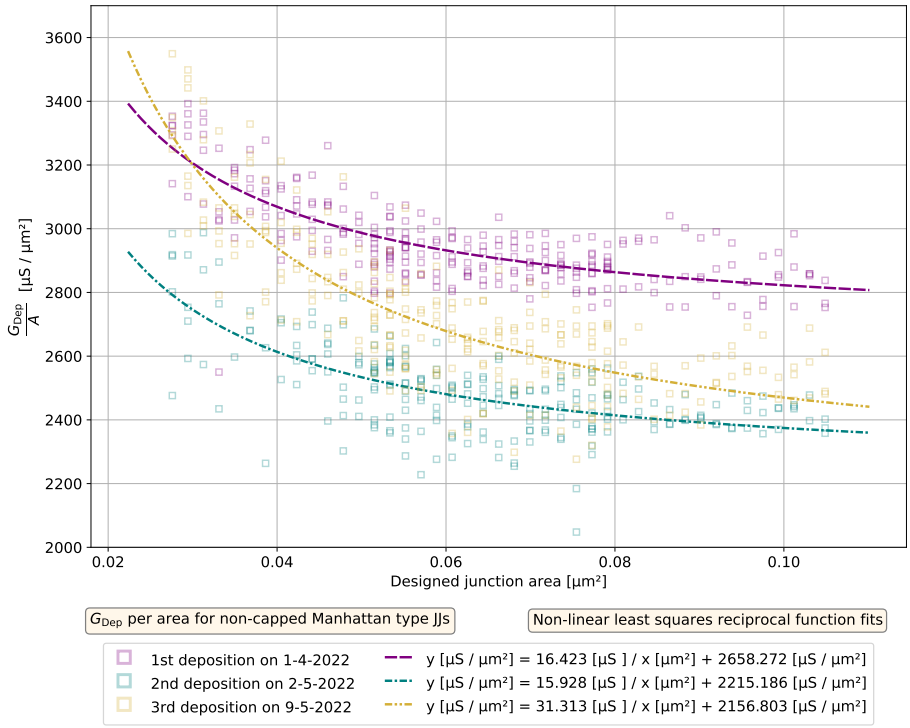


Figure 4.19: A plot showing the reciprocal dependence between designed junction area and G/A for 3 datasets of the same sample (N. x $3e^{2/3/4}$). The purple, teal and yellow squares show the data from the 1^{st}, 2^{nd} and 3^{rd} deposition. The dashed and dash dotted fit lines and their functions in the legend are also shown. The different depositions show very similar conductances.

twice as big. Showing a larger deviation from the normally expected Ohmic law where the conductances scale linearly with the junction overlap area. If this is due to recycling or just some random variation is unclear.

5

CONCLUSIONS

The objective of this thesis was to find a way to tune the resistance of Josephson junctions in both directions using rapid thermal annealing (RTA). To achieve this, RTA experiments with varying parameters were performed. The conductances of the junctions was followed throughout the processes. In this way an attempt was made to perform a systematic characterization of room temperature resistances of Josephson junctions before and after being subjected to different annealing processes. The annealing of junctions was carried out either by heating the sample up to 200°C on a hotplate which simulates the fabrication process used for air bridge deposition. While the other annealing process is using the rapid thermal annealer in an inert atmosphere of nitrogen or in forming gas performed between a temperature range of 200 to 400°C. The parameter varied during the fabrication of both variants of Josephson junctions, namely Dolan and Manhattan style, was the addition of a terminal oxidation step also referred to as 'capping oxidation.' From the simulated air bridge annealing experiment, it was observed that the capping oxidation plays a role in determining the directionality of the junction aging. In the absence of the capping oxidation layer both Dolan and Manhattan style junctions show an increase in conductance post the simulated air bridge annealing step.

In other samples the conductances were also seen to increase after RTA at 200°C using either nitrogen or forming gas. This was the case for uncapped Manhattan devices, the highest increase of roughly $450\,\mu S\mu m^{-2}$ for large junctions was obtained using an RTA with forming gas. In another capped Manhattan device, which was stored for a week in N_2 gas and subsequently annealed using RTA at 200 °C the conductances also increased. This could be an indication that extraneous atoms/molecules may diffuse through the AlO_x layer, these contaminants may be expelled from the tunnel barrier leading to a higher conductance. However, it is still unclear what the dynamics are and why the anti-aging effect has not been measured for uncapped Dolan bridge junctions, although those have not been studied to the same degree.

Annealing at higher temperatures such as 300 and 400°C only brought the junction conductances down. Indicating that this kind of annealing could speed up the aging process that would occur naturally. Where there is also a difference between annealing at

these two temperatures showing that the higher the temperature the bigger the decrease in conductances.

Consecutive annealing processes at the same temperature point showed that the conductances initially increased after the first annealing step but thereafter only minor fluctuations in the conductances were observed. In each round of annealing the sample was quickly heated in several seconds and then kept at that temperature for 2 minutes after which it was cooled for 3 to 6 more minutes. It was observed that the change in conductances of junctions was already saturated after the first round of annealing.

5.1. OUTLOOK

Based on this research some questions have been answered but there are more experiments that could be done to get a better undestanding. The following 3 experiment types give examples of research directions as possible continuation of what has been done during this project:

1. **Laser annealing experiments with forming gas:** It is clear from the current dataset that a useful extent of controllable anti-aging has not yet been obtained for junctions subjected to RTA post simulated AB annealing. It would be useful to investigate whether laser annealing in an inert gas could consistently result in junction anti-aging provided the junction deposition step is the terminal fabrication process.
2. **RTA experiments at 300°C:** Some of the experiments with RTA at 300°C showed large fluctuations in the ramping temperatures. Therefore, it would be interesting to repeat these experiments to get a statistically more reliable conclusion.
3. **More RTA experiments for Dolan bridge type junctions:** With more datasets a more complete picture could be obtained.

After having made these observations during this research it instigates further pondering of how junctions could be annealed to change the conductances in both directions. Here signs of bi-directional tuning of Josephson junctions using RTA have been seen. It is currently unclear how RTA and laser annealing differ in how they exactly reshape the tunnel barrier region. Laser annealing has the benefit that junctions can be individually addressed, whereas during RTA the whole sample is affected simultaneously. Perhaps it is also possible to increase the conductances of Josephson junctions using laser annealing by changing the parameters such as power, duration and the environment the samples are annealed in. That could then conceivably turn out to be an especially useful tool in the mission to build better quantum processors.

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A

QUANTUM BITS

The quantum bit or qubit in quantum computation is analogous to the bit of classical computation. Classical bits can only be in one of two possible states, either 0 or 1. Similarly the qubit can also be in states which look like the classical states, either $|0\rangle$ or $|1\rangle$. These are also called the computational basis states. Unlike the bit for the qubit, we can form linear combinations of states which are also called superpositions:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \tag{A.1}$$

The numbers α and β are complex numbers. Quantum mechanics does not allow us to examine the superposition and obtain $|\psi\rangle$. When a measurement is being made one of the computational basis states is obtained. Either $|0\rangle$ with a probability $|\alpha|^2$ or $|1\rangle$ with a probability $|\beta|^2$. It makes sense that these probabilities sum to 1 or mathematically: $|\alpha|^2 + |\beta|^2 = 1$. It is useful to think of the qubit state as a unit vector in a two-dimensional complex vector space. It is also common to shift towards a geometric representation. To do so we will rewrite equation A.1:

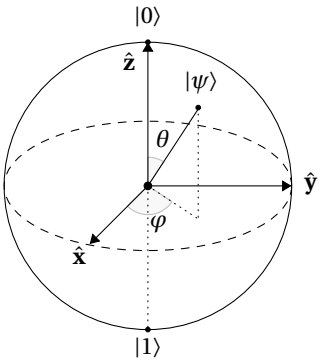

Figure A.1: Bloch sphere.

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi}\sin\left(\frac{\theta}{2}\right)|1\rangle \tag{A.2}$$

where θ and φ are real numbers. You could include an additional factor $e^{i\gamma}$ in both terms, but it is often ignored as it is just an overall rotation in the two-dimensional complex vector space. The numbers θ and φ describe a point on the Bloch sphere as shown in figure A.1.

To establish a physical qubit, we require some quantum system which has at least two states available to us. If the energy spacing between the energy levels of these states is distinguishable specific state transitions can be more easily driven.

A

A.1. WELL CHARACTERIZED QUBITS

To answer the question 'What makes a good Quantum Processor?' it is common practice to use the DiVincenzo criteria as described in *The Physical Implementation of Quantum Computation* [40]. Specifically, the first criterion: "A scalable physical system with well characterized qubits" aids in treating the design requirements for a good quantum processor. It is required that the qubits are "well characterized" meaning that its physical parameters should be accurately known, this includes the Hamiltonian of the qubit and the energy eigenstates. In the sections before the charging energy and Josephson energy were briefly examined as well as ways to change them and effectively change the qubit energy levels. This ties in with the project goals as discussed in section 1. To engineer a good quantum processor, it is important to fabricate qubits which meet the design criteria. One of the parameters that is discussed often is the qubit frequency. This refers to the operation frequency that is used to drive the qubit into a superposition state. The strong coupling to microwave photons is achieved using circuit quantum electrodynamics (cQED). The necessary frequency depends on the energy difference between the ground and first-excited state. The qubits are controlled using coplanar waveguide transmission lines which essentially deliver quanta of light to the system. The Planck relation $E = h\nu$ expresses the energy of a photon in its frequency ν and shows that they are proportional. The qubit frequency depends on the junction resistance which itself depends on the geometry of the junction. The overlapping area of the junction electrodes can be changed to adjust the junction resistance to a desired range. Any variance in the size of the overlap area will result in a shift in qubit frequency.

A.2. DECOHERENCE

Another criterion that DiVincenzo gives "Long relevant decoherence times, much longer than the gate operation time" shines light on another important aspect which complicates the realization of good quantum processors. Decoherence is due to the qubit quantum mechanically entangling with the environment [41]. There are different mechanisms responsible for decoherence. The main metrics that are measured are the relaxation and dephasing times T_1 and T_2 respectively. For a single qubit state, the decoherence can be characterized with a density matrix transformation model [12]:

$$\begin{bmatrix} a & b \\ b^* & 1-a \end{bmatrix} \rightarrow \begin{bmatrix} (a-a_0)\,e^{-t/T_1} + a_0 & be^{-t/T_2} \\ b^*\,e^{-t/T_2} & (a_0-a)\,e^{-t/T_1} + 1 - a_0 \end{bmatrix} \tag{A.3}$$

the a_0 parameter characterizes the thermal equilibrium state. Any defects in the environment around the qubit can cause the qubit to decohere more rapidly, this will then be visible in a decrease of the T_1 and T_2 times.

A.2.1. DEPHASING

There are different mechanisms responsible for dephasing. The two characteristic times that are often measured are the Ramsey dephasing time and the Echo dephasing time, respectively T_2^* and T_2^{echo} [42].

B

LOGBOOK

Table B.1: A logbook showing the dates of events. The last column shows how many probes have been used for the conductance measurements.

Sample	Deposited	AB anneal	RTA	# Probes
F. i 1c	18-11-2021	23-11-2021	23-11-2021	2
F. i 4c	10-12-2021	10-12-2021	16-12-2021	4
F. x 4e	19-01-2022	19-01-2022	20-01-2022	4
F. x 1e	21-01-2022	21-01-2022	21-01-2022	2
N. i 1e	04-01-2022	-	07-01-2022	4
N. i 2e	07-01-2022	-	07-01-2022	4
N. i 3e	17-02-2022	-	18-02-2022	4
N. i 4e	17-02-2022	-	18-02-2022	4
N. x 1e	15-02-2022	-	17-02-2022	4
N. x 2e	15-02-2022	-	17-02-2022	4
N. x 3e	08-01-2022	-	08-01-2022	4
N. x 4c	22-03-2022	-	-	2
step 2	29-03-2022[a]	-	29-03-2022	2
N. x $3e^2$	01-04-2022	-	01-04-2022	2
step 2	-	-	01-04-2022	2
step 3	-	-	01-04-2022	2
N. x $4e^2$	01-04-2022	01-04-2022	01-04-2022	2
step 2	-	-	01-04-2022	2
step 3	-	-	01-04-2022	2
N. x $3e^3$	02-05-2022	-	04-05-2022	4
N. x $3e^4$	09-05-2022	-	10-05-2022	4
N. x $4e^3$	02-05-2022	-	04-05-2022	4
N. x $4e^4$	12-05-2022	-	12-05-2022	4

[a] End of storage period, sample is measured a 2^{nd} time.