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Hou, Fengze

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Fan-Out SiC MOSFET Power Module in an Organic Substrate

Fan-Out SiC MOSFET Power Module in an Organic Substrate

Proefschrift

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Fengze Hou

Master of Science in Mechatronic Engineering,
Guilin University of Electronic Technology, Guilin, China
geboren te Shanxi, China.

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Promotor: Prof. dr. G.Q. Zhang
Promotor: Prof. dr. J.A. Ferreira

Composition of the doctoral comittee:

Rector Magnificus,	Chairman
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To My Family

Fengze Hou

CONTENTS

NOMENCLATURE

A_{GD}	Gate-drain overlap area
α_A	CTE of material A
α_B	CTE of material B
σ_T	Thermally-induced stress
C_{DS}	Drain-source capacitance
C_{GD}	Gate-drain capacitance (Miller capacitance)
C_{GDJ}	Nonlinear depletion capacitance
C_{GS}	Gate-source capacitance
C_{ISS}	Input capacitance
C_{OSS}	Output capacitance
C_{OX}	Gate oxide capacitance
C_{RSS}	Reverse capacitance
d	Thickness of material
E	Dielectric breakdown strength
E_A	Young's modulus of material A
E_B	Young's modulus of material B
ε_{sic}	Buck electron mobility of SiC
I_D	Drain current
I_G	Gate current
M	Fitting parameter
n	Rotational speed of compressor
N_D	Doping concentration
P	Pressure
q	Heat flux
q_e	Electron charge
R_{drift}	Drift layer resistance
R_{on}	On-resistance
ΔT	Temperature difference of two points along the heat path
T_s	Saturation temperature
t_{GDJ}	Depletion thickness between gate and drain
t_{OX}	Gate oxide thickness
μ_A	Poisson's ratio of material A
U_{PT}	Voltage of the pressure transducer
U_{VR}	Voltage of the variable resistor
V_{bi}	Built-in potential between the P-body and the N-drift junction
V_{BD}	Dielectric breakdown voltage
V_{BR}	Breakdown voltage of SiC MOSFET
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage

V_T	Gate-drain overlap depletion threshold
w	Drain-source un-depleted drift width
w_B	Thickness of N- drift layer
w_{DSJ}	Drain-source depletion width

Abbreviations

ABF	Ajinomoto build-up film
Ag	Silver
Al	Aluminum
Al_2O_3	Alumina
AlN	Aluminum nitride
BGA	Ball grid array
BT	Bismaleimide triazine
CCL	Copper clad laminate
Cr	Chromium
CTE	Coefficient of thermal expansion
Cu	Copper
DBC	Direct bonded copper
DPT	Double pulse test
DSC	Differential scanning calorimetry
DUT	Device under test
ECP	Embedded component packaging
EMC	Epoxy molding compound
FPC	Flexible printed circuit
GaN	Gallium nitride
GWP	Global warming potential
HEMT	High-electron-mobility transistor
HP	High-pressure
HS-MOS	High-side SiC MOSFET
IGBT	Insulated-gate bipolar transistor
JFET	Junction gate field-effect transistor
LP	Low-pressure
LS-MOS	Low-side SiC MOSFET
LTCC	Low temperature co-fired ceramic
MHS	Microchannel heat sink
Mo	Molybdenum
MOSFET	Metal-oxide semiconductor field-effect transistor
Ni	Nickel
NP	Nanoparticle
PCB	Printed circuit board
PCoB	Power chip on bus
PCoC	Power chip-on-chip
PCoI	Power chip-on-inductor
PID	Photoimageable dielectric
PMMA	Polymethyl methacrylate
POL	Power overlay

ppm	parts per million
PVD	Physical vapor deposition
Qg	Gate charge
RCC	Resin-coated copper
RDL	Redistribution layer
rpm	Revolutions per minute
Si	Silicon
SiC	Silicon carbide
Si_3N_4	Silicon nitride
SiPLIT	Siemens planar interconnect technology
Sn	Tin
TBF	Temporary bond film
TC	Thermocouple
TCIL	Thermally conductive electrically insulated layer
Tg	Glass transition temperature
TGA	Thermal gravimetric analyzer
Ti	Titanium
TIM	Thermal interface material
TLP	Transient liquid phase
TMA	Thermal mechanical analyzer
TO	Transistor outline
T-PM	Transfer molded power module
TTC	Thermal test chip
TTV	Thermal test vehicle
UV	Ultraviolet
VCRS	Vapor compression refrigerant system
VDMOS	Vertical diffused MOSFET
WBG	Wide bandgap

Summary

Global warming has caused irreversible damage to the earth. Energy-saving not only can reduce the depletion of energy sources but also prevent global warming. Nowadays, 40% of worldwide energy is consumed as electrical energy, so a high-efficient electrical energy conversion is urgently required. The power module plays a critical role in electrical energy conversion. So far, silicon (Si) power devices have still been widely used in the power module. However, they are approaching the theoretical performance limits, which drastically reduces the power module's conversion efficiency. Instead, silicon carbide (SiC) power devices have a great application perspective due to their wider energy bandgap, lower intrinsic carrier concentration, and higher critical electrical field.

However, these superior characteristics cannot be exploited via current mainstream packaging technologies and materials. SiC devices cannot be used merely as a direct drop-in replacement of Si devices.

The current mainstream packaging technology for SiC devices is mainly wire-bonding interconnection combined with a direct-bonded copper substrate. However, the wire-bonds do not allow for double-sided cooling and add parasitic inductance, which affects the heat-dissipation efficiency and switching performance of SiC devices. The high parasitic inductance (> 10 nH) can induce voltage overshoots and electromagnetic interference issues when SiC devices are switching at fast speeds. The packaging materials used in the Si-based power module, e.g., die-attach and encapsulant, generally cannot withstand the high temperature and large-temperature cycle, limiting the application of SiC devices in the high temperature. Therefore, to fully explore the potential of SiC devices, it is essential to incorporate advanced packaging with device development.

With the ever-increasing power output and packaging density, SiC devices also face severe cooling challenges, although they can withstand higher temperatures. Their sizes are much smaller than similarly rated Si devices, leading to the high heat flux of SiC devices that could reach up to 1 kW/cm^2. So, the high-efficient cooling schemes need to be developed to cope with the increasing heat flux.

In this dissertation, firstly, primary packaging schemes for Si power modules, which are the foundation of packaging methods of SiC ones, were reviewed. After that, attempts on packaging techniques for SiC power modules were thoroughly overviewed.

Secondly, SiC metal-oxide-semiconductor field-effect transistor (MOSFET) and organic substrate materials were selected and characterized. I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed via a custom fixture. The experimental results showed that SiC MOSFET had output characteristics of non-saturation, existed two distinct points in the curve of Miller capacitance versus drain-source voltage, and displayed a non-flat Miller platform. All of these are different from Si devices. After that, thermal stability, dielectric breakdown, thermo-mechanical performance, and cure kinetics of the organic substrate materials were characterized. The experimental results indicated that the substrate materials could withstand the high temperature of 300 °C and the high voltage of 46.9 kV.

The glass transition temperature was as high as over 260 °C, and the coefficient of thermal expansion was matching with SiC. Both one-hour curing at 280 °C and two-hour curing at 210 °C could ensure the full cure of the BT prepreg.

Thirdly, a novel fan-out panel-level packaging technology was proposed for a phase-leg SiC MOSFET power module. The high- and low-side SiC MOSFETs were embedded in an organic substrate, interconnected by double-sided redistribution layers (RDLs) and through vias, finally protected by double-sided soldermasks. Compared with current embedded packaging technologies for Si and GaN devices, the proposed packaging structure has several unique merits, such as structure symmetry and double-sided cooling. The electrical, thermal, and thermal-mechanical simulations were conducted to evaluate and optimize the fan-out packaging performance. After that, a detailed fan-out panel-level packaging process for the phase-leg SiC MOSFET power module was introduced. Three essential packaging processes, including exposure and development of photo imageable dielectric, panel-level physical vapor deposition (PVD), and double-sided RDL interconnection, could replace conventional laser drilling, chip/wafer-level PVD, and wire-bonding, respectively.

Fourthly, the static and dynamic characterizations of the fan-out SiC MOSFET power module were conducted. The effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed. It is found that the output characteristics of non-saturation of SiC MOSFET were more evident after packaging, and higher drive voltage was required to entirely turn on SiC MOSFET due to the extension of the non-flat Miller plateau. The double pulse test was used to evaluate and compare the switching characteristics of SiC MOSFET in the fan-out phase-leg power module and TO-247 discrete package. The results showed that the fan-out package had smaller voltage overshoot and current oscillation at turn-off and lower voltage oscillation and current overshoot at turn-on than TO-247 package.

Fifthly, a microchannel thermal management with two-phase flow boiling using refrigerant R1234yf is presented. Both single- and multi-chip silicon thermal test vehicles (TTVs) based on substrate embedded technology were fabricated and attached to a microchannel heat sink (MHS) with two-phase cooling. A vapor compression refrigerant system was implemented to realize and control the phase-change of R1234yf. The system includes two identical aluminum MHSs connected in series, a gas flowmeter, a miniature compressor, a condenser, and a throttling device. The experimental results showed that the thermal management system could dissipate a heat flux of 526 W/cm^2 while maintaining the junction temperature below 120 °C. For SiC MOSFET with a higher junction temperature of 175 °C, the system can be expected to dissipate a heat flux as high as 750 W/cm^2. The effects of the rotational speed of the compressor, the opening of the throttling device, TTV layout, and a downstream heater on the system's cooling performance were analyzed in detail. The study showed that the opening of the throttling device had a significant effect on cooling performance. For the multi-module system, the chip at the upstream location had the best cooling performance. The downstream TTV on MHS2 could function as a super-heating device instead of a heat-dissipating device, making the junction temperature of upstream TTV at a low value.

Lastly, the main conclusions and contributions are summarized, and several recommendations for future work are discussed.

SAMENVATTING

De opwarming van de aarde heeft onomkeerbare schade veroorzaakt op aarde. Energie besparing kan niet alleen het opraken van energie grondstoffen verminderen, maar ook de opwarming van de aarde. Vandaag de dag wordt 40% van de energie in de wereld geconsumeerd als elektriciteit, dus een hoge elektrische energie conversie efficiëntie is dringend nodig. De vermogensmodule speelt een kritieke rol in deze energieconversie. Tot nu toe zijn silicium (Si) vermogensapparaten veel gebruikt in de vermogensmodule. Helaas bereiken zij inmiddels hun theoretische limieten, wat hun conversie efficiëntie drastisch vermindert. In plaats daarvan bieden siliciumcarbide (SiC) vermogensapparaten een beter perspectief door hun grotere verboden zone, lagere intrinsieke ladingdrager concentraties en een hoger kritisch elektrisch veld. Echter, deze superieure eigenschappen kunnen niet worden uitgebuit met de huidige mainstream behuizingstechnologie en materialen. SiC apparaten kunnen niet zomaar als directe vervanger van Si apparaten worden ingezet.

De huidige mainstream behuizingstechnologie voor SiC apparaten is voornamelijk draad verbinding gecombineerd met een direct gehecht koperen substraat. Echter, draad verbindingen laten geen tweezijdige koeling toe en voegen parasitaire zelfinductie toe, wat de warmte dissipatie en schakel prestaties aantast. De hoge parasitische zelfinductie (>10nH) kan leiden tot voltage overschrijdingen en elektromagnetische interferentie problemen als SiC apparaten schakelen op hoge snelheden. De materialen die gebruikt worden in Si vermogensmodules, zoals de chip bevestigings- en inkapselingsmaterialen, kunnen in het algemeen hoge temperaturen en temperatuur cycli niet aan, wat de toepassing van SiC apparaten limiteert bij hoge temperaturen. Het is daarom essentieel om geavanceerde behuizing in de ontwikkeling te verwerken om het volledige potentiaal van SiC apparaten te benutten.

Door het toenemende vermogen en pakkingsdichtheid krijgen SiC apparaten ook ernstige koeling uitdagingen, ook al kunnen ze hogere temperaturen aan. Ze zijn kleiner dan Si apparaten, wat leidt tot een hoge warmte flux in SiC apparaten tot 1 kW/cm^2. Uiterst efficiënte koeling moet worden ontwikkeld om deze groeiende warmte flux aan te kunnen.

Dit proefschrift geeft eerst een overzicht van de voornaamste verpakkingsmethodes voor Si vermogensmodules, die ook de bouwstenen vormen voor SiC verpakkingsmethodes. Daarna volgt een overzicht voor verpakkingstechnieken voor SiC vermogensmodule.

Ten tweede zijn de SiC MOSFET en organische substraat materialen geselecteerd en gekarakteriseerd. I-V, C-V en gate eigenschappen van de SiC MOSFET zijn geanalyseerd met een op maat gemaakte armatuur. De experimenten laten zien dat de SiC MOSFET uitvoer niet gesatureerd was, dat er twee punten waren op de Miller capaciteit versus drain-source voltage grafiek en dat er een niet vlak Miller platform was. Allemaal anders dan in Si apparaten. Daarna zijn de thermische stabiliteit, diëlektrische doorslag en thermomechanische prestaties van de organische substraat materialen en de uithardingskinetiek van BT voorgeïmpregneerde vezels gekarakteriseerd. De experimenten aten zien dat de substraat materialen een temperatuur van 300 °C en een hoog voltage van 46.9 kV aankunnen. De glas transitie temperatuur was 260 °C en de thermische expansie coëfficiënt kwam

overeen met die van SiC. Zowel een uur uitharding op 280 °C en twee uur op 210 °C gaf volledige uitharding van de BT voorgeïmpregneerde vezels.

Als derde wordt een nieuw uitwaaierend paneel niveau verpakkingstechnologie voorgesteld voor de fase aansluiting voor een SiC MOSFET vermogensmodule. De hoge en lage kant SiC MOSFETs zijn ingekapseld in een organisch substraat, verbonden met dubbelzijdige verdelingslagen (RDLs), door vias en tenslotte beschermd met dubbelzijdige soldeer maskers. Vergeleken met huidige ingebedde verpakkingen in organische substrates voor Si en GaN apparaten, heeft de voorgestelde verpakkingsstructuur meerdere voordelen, zoals symmetrie en dubbelzijdige koeling. Elektrische, thermische en thermo mechanische simulaties zijn gedaan om de prestaties de evalueren en te optimaliseren. Daarna wordt een gedetailleerd verpakkingsproces voor de fase aansluiting van de SiC MOSFET vermogensmodule geïntroduceerd. Drie essentiële verpakkingsprocessen, waaronder blootstelling en ontwikkeling van fotogevoelig diëlektricum, paneel brede fysische damp depositie (PVD) en dubbelzijdige RDL interconnectie, kunnen respectievelijk laser boring, chip/wafer niveau PVD en draad verbinding vervangen.

Ten vierde zijn de statische en dynamische karakterisaties uitgevoerd van de uitwaaierende SiC MOSFET vermogensmodules. De effecten van de uitwaaierende verpakking op de I-V, C-V en gate lading eigenschappen van de SiC MOSFET zijn geanalyseerd. Het bleek dat de uitvoer eigenschappen van de niet-saturatie van de SiC MOSFET evidenter was na verpakking en dat een hoger aansturingsvoltage nodig was om de SiC MOSFET volledig aan te zetten door de extensie van het niet vlakke Miller plateau. De dubbele puls test was gedaan om de schakel eigenschappen van de SiC MOSFET in de uitwaaierende fase connectie vermogensmodule en de TO-247 verpakking. De resultaten laten zien dat de uitwaaierende verpakking een kleiner voltage overschrijding en stroom oscillaties had bij uitschakeling en lagere voltage oscillaties en dat het lagere stroom overschrijding had bij inschakeling dan de TO-247 verpakking.

Ten vijfde wordt er een mikrokanaal thermisch management systeem gepresenteerd met twee-fase kook stroming met R1234yf koelmiddel. Zowel de enkel- als de multichip silicium thermische test vehikels (TTVs) gebaseerd op ingebedde substraat technologie zijn gefabriceerd en gehecht aan een mikrokanaal warmteput (MHS) met twee-fase koeling. Een dampcompressie koelsysteem was geïmplementeerd om de fasetransitie van R1234yf te realiseren en te controleren. Het systeem bevat twee identieke aluminium MHSs in series verbonden, een gas stroom meter, een miniatuur compressor, een condensator en een regelaar. De resultaten laten zien dat het thermisch management systeem een warmte flux van 526 W/cm^2 aankan en de junctie temperatuur onder de 120 °C houdt. Voor de SiC MOSFET met een junctie temperatuur van 175 °C kan het systeem een warmte flux afvoeren tot 750 W/cm^2. De effecten van de rotatiesnelheid van de compressor, de opening van de regelaar, de TTV layout en een verwarmer stroomafwaarts op de koelprestaties van het systeem zijn nauwgezet geanalyseerd. Het onderzoek toont aan dat de opening van de regelaar een significant effect had op de koeling. In het multi-module systeem had de meest stroomopwaartse chip de beste koeling. De stroomafwaartse TTV op de MHS2 kon zich gedragen als een oververhittingsapparaat in plaats van een warmte afvoer apparaat, wat de junctie temperatuur van de stroomopwaartse TTV laag maakte.

Ten slotte worden de conclusies en contributies samengevat en worden verscheidene aanbevelingen gemaakt voor toekomstig werk.

1

INTRODUCTION

SiC MOSFET is a promising wide-bandgap semiconductor device in the applications of high operating temperature, high blocking voltage, and high switching frequency due to excellent material properties. However, the superior characteristics of SiC MOSFET cannot be exploited via current mainstream packaging technologies and materials. They cannot be used merely as a direct drop-in replacement of Si devices. To fully explore the potential of SiC MOSFET, it is essential to incorporate advanced packaging with device development. With the ever-increasing power output and packaging density, SiC MOSFET also faces severe cooling challenges, although they can withstand higher temperatures. Their sizes are much smaller than similarly rated Si devices, leading to the high heat flux of SiC MOSFET that could reach up to 1 kW/cm^2. So, the high-efficient cooling schemes need to be developed to cope with the increasing heat flux.

Parts of this chapter have been published in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 7, no. 10, pp. 1721-1728, Oct. 2017 [1].

1

1.1. Background

Recently, global warming has caused irreversible damage to the earth. Energy-saving not only can reduce the depletion of energy sources but also prevent global warming. Nowadays, 40% of worldwide energy is consumed as electrical energy [2], so a high-efficient electrical energy conversion is urgently required. The power module plays a critical role in electrical energy conversion. So far, silicon (Si) power devices have still been widely used in the power module. However, they are approaching theoretical physical limits [3]. The practical operating temperature of Si insulated gated bipolar transistor (IGBT) is lower than 175 °C, and the maximum block voltage is lower than 6.5 kV [4]-[5]. Thanks to the bipolar current conduction mechanism, the switching speed of IGBT is lower, leading to a higher switching loss, which affects the energy conversion efficiency, and limiting the high-switching frequencies. Now, wide bandgap (WBG) power devices have gained attention.

1.2. Potential of SiC power devices

As a potential WBG semiconductor material, silicon carbide (SiC) has several superior characteristics, as shown in Figure 1.1 [2]. Owing to the wider energy bandgap of 4H-SiC compared with Si, its intrinsic carrier concentration is smaller, which enables SiC devices to operate at higher temperatures (> 200 °C). The 10× critical electric field makes ultra-high voltage (> 10 kV) power devices achievable. The ideal specific conduction resistance enables SiC devices to be smaller, leading to lower parasitic capacitance and higher switching speed. The high switching speed allows for high switching-frequency operation (> 100 kHz) with less switching loss, resulting in a significant reduction of the size, weight, and cost of passive components [5]-[9].

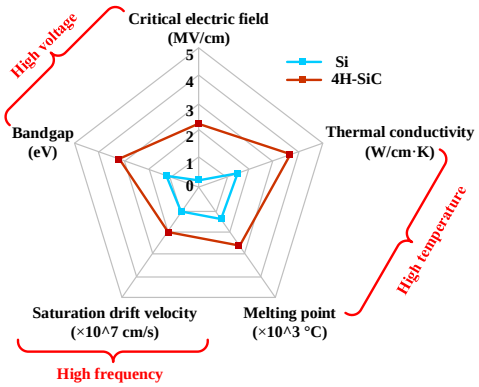

Figure 1.1: Material properties comparison between Si and 4H-SiC [2].

Figure 1.2 shows the possible application fields that SiC devices can displace Si ones in power modules. They can be used in IT and consumer, automotive, and industry. For the super-high power applications, only SiC power devices can be used [10].

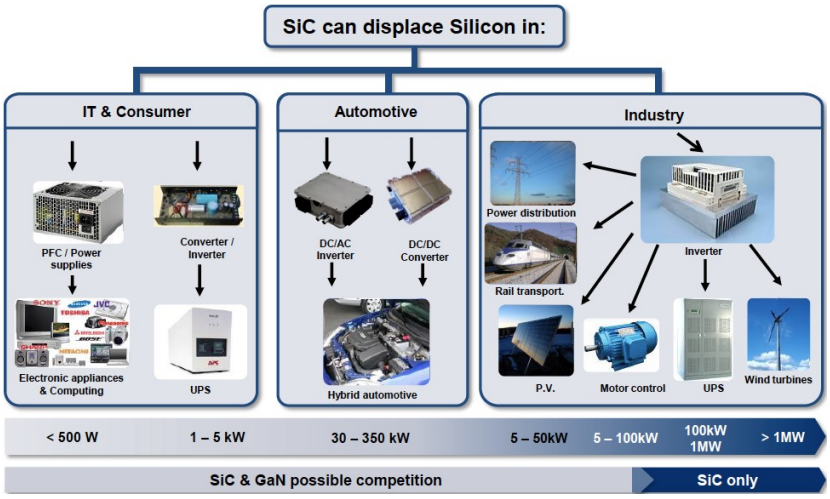

Figure 1.2: Possible applications of SiC power module in Si power electronics [10].

1.3. SiC MOSFET

Figure 1.3 illustrates the application range of Si and SiC power devices [11]-[14]. The blue dashed line is the theoretical performance limitation of Si devices. Si devices are mainly used in the low and medium voltage ranges, SiC metal-oxide-semiconductor field-effect transistor (MOSFET) possesses advantages in the applications of medium-high voltage and high frequency. So far, there have no been available SiC IGBT on the market. It will be used in the higher voltage and temperature ranges.

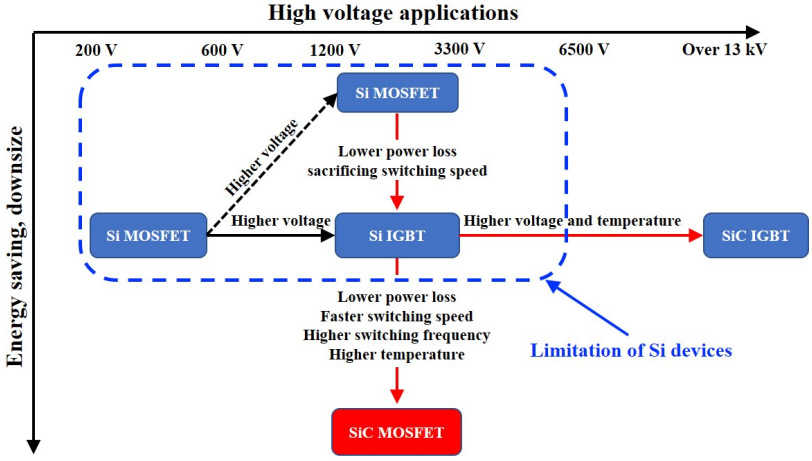

Figure 1.3: Application range of Si and SiC power devices

SiC MOSFET has much lower output capacitance and gate charge, and they can switch

at much higher *dv/dt* and *di/dt*. Switching speed comparison between SiC MOSFET and Si IGBT with the same power rating was performed in Ref. [15]. The devices from Cree's SiC MOSFET (C2M0080120D) and Infineon's third-generation Si IGBT (IKW15N120H3) were selected. The quantitative *dv/dt* and *di/dt* of the two devices are shown in Table 1.1. As seen in the table, SiC MOSFET can be switched much faster than Si IGBT.

Table 1.1: Switching speed evaluation of SiC MOSFET and IGBT [15]

Feature	Turn-on		Turn-off	
	SiC MOSFET	IGBT	SiC MOSFET	IGBT
dv/dt (kV/µs)	40	16	27	8
di/dt (kA/µs)	1.1	0.5	0.3	0.06

Due to the unipolar structure, the switching loss of SiC MOSFET is relatively low when the switching speed is faster, enabling its promising application in the high frequency. Meanwhile, the switching loss of SiC MOSFET has little variation over temperature. In comparison, Si IGBT with a bipolar structure has higher switching loss, which increases significantly in the high operating temperature as well [12]-[14]. The conduction loss of SiC MOSFET is also lower because of its higher doping concentration in the drift region. The smaller depletion width reduces the on-state resistance of SiC MOSFET, resulting in less conduction loss. Therefore, SiC MOSFET possesses definite advantages in the medium-high voltage applications over Si counterparts.

1.4. CONVENTIONAL PACKAGING TECHNOLOGY

CONVENTIONAL aluminum (Al) wire-bonding interconnection combined with direct-bonded copper (DBC) substrate has still been one of the most preferred packaging technologies for the SiC power module. DBC substrate has a copper-ceramic-copper (Cu-ceramic-Cu) laminated structure, with the top layer patterned to form an electrical circuit, the bottom layer attached to a baseplate, and the ceramic used as an electrically isolating layer [16]. A variety of ceramic materials can be selected, such as alumina (Al_2O_3), aluminum nitride (AlN), and silicon nitride (Si_3N_4). Al_2O_3 is the most economical choice but has the lowest thermal conductivity and average mechanical strength. AlN has a higher thermal conductivity than $Al_2O_3$and a better coefficient of thermal expansion (CTE) match with 4H-SiC. Si_3N_4 is a better choice in terms of much higher thermal cycling reliability, but its disadvantage is higher cost and slightly lower thermal conductivity.

Figure 1.4 illustrates the schematic of conventional packaging technology for the SiC MOSFET power module. As seen in this figure, a SiC chip is soldered to a DBC substrate and afterward wire-bonded to establish the chip top connection. The DBC is then soldered to a baseplate, and load terminals and control connectors are soldered to the DBC substrate. The entire assembly is finally enclosed in an encapsulant to protect the internal structures of the SiC MOSFET power module. The conventional packaging technology provides electrical interconnects (via Al wire-bonds and upper Cu tracks of the DBC substrate), electrical insulation (using the DBC substrate), device protection (by encapsulant), and thermal management (through the bottom side). The conventional package structure is used in the vast majority of the power modules that are currently manufactured. [17].

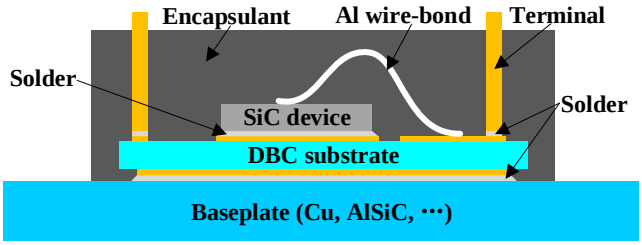

Figure 1.4: Conventional packaging technology for SiC MOSFET power module

1.5. PROBLEMS OF THE CONVENTIONAL PACKAGING

THE conventional packaging technology, however, limits the performance of the SiC MOSFET. Figure 1.5 shows the main problems of the conventional packaging for the SiC MOSFET power module.

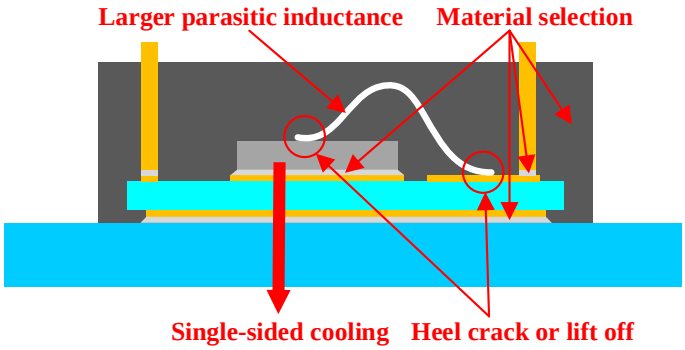

Figure 1.5: Problems of the conventional packaging

- Wire-bonding interconnection has long commutation paths so that the parasitic inductances could exceed 10 nH. High *di/dt* at turn-off transient would easily lead to significant voltage overshoot, increasing switching loss of SiC MOSFET, causing electromagnetic interferences, false-triggering, limiting switching frequency, and affecting switching waveforms [17]-[19]. Figure 1.6 illustrates the voltage overshoot caused by parasitic inductance. To avoid excessive overshoot, much smaller parasitic inductance L_S is required for fully utilizing the fast switching characteristics of SiC MOSFET [20]-[22].

- Limited by available packaging materials, junction temperatures of SiC power modules are subjected to 175 °C, even though SiC devices are, in theory, capable of op-

erating at high temperature up to 600 °C [23]-[24]. Most of the packaging materials adopted in the wire-bonded power module, such as Sn-based solder and encapsulant, cannot withstand high temperature over 200 °C, which limits the application of the power module in the high-temperature environment [25]. High-lead solder, which contains over 85% lead, is currently excluded from the Restriction of Hazardous Substances (RoHS) directive [26]. The high-temperature solders, such as Au80Sn20, Au88Ge12, Zn-12Al, etc., require higher melting points and suitable thermomechanical properties.

- Furthermore, wire-bonds do not allow for double-sided cooling [27]. Most of the heat generated by SiC MOSFET is dissipated through its bottom side, which affects the thermal performance of the power module. Moreover, as power loss increases with switching frequency, a cooling system that could remove heat from both sides of the die in a power module would be much more efficient for the high power operation of a power module [17].

- As for thermo-mechanical reliability, wire-bonds lift-off and solder joints fatigue are the main failure mechanisms of the conventional packaging due to the CTE mismatch between the Al and the SiC, the SiC and the DBC, and the DBC and the baseplate. The solder joints degradation increases the thermal resistance of the SiC power module and raises the temperature, thus accelerating the lift-off of wire-bonds. The reliability of wire-bonds is closely related to the lifetime of the SiC power module. When the wire-bonds break down, the power module will fail [25]-[28].

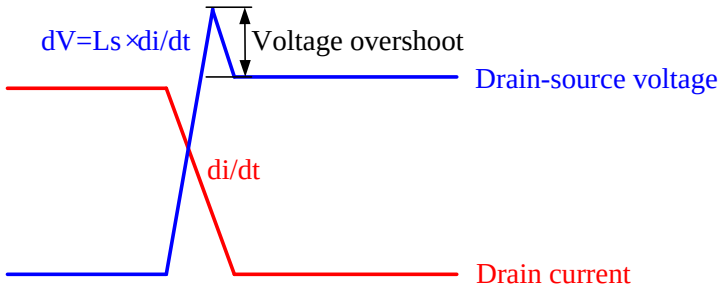

Figure 1.6: Illustration of voltage overshoot caused by parasitic inductance

Therefore, to fully explore the potential of SiC MOSFET, it is essential to incorporate advanced packaging technologies with device development.

1.6. Advanced packaging technology

Several advanced packaging technologies for the SiC power module, e.g., embedded packaging, press-pack, planar packaging, 3D packaging, and hybrid packaging techniques, have been developed in recent years [29]-[42].

The fan-out packaging is regarded as one of the latest and most potential microelectronic packaging technologies because it possesses lower cost, thinner profile, and better electrical and thermal performance [1], [43]-[44]. Figure 1.7 shows the schematic diagram of a typical fan-out packaging. It is composed of die, epoxy molding compound (EMC), dielectric, redistribution layer (RDL), ball grid array (BGA), etc. Compared with the conventional flip-chip BGA, the fan-out technology eliminates many process steps, e.g., substrate, wafer bumping, flip-chip reflow, flux cleaning, underfill, and so on [45].

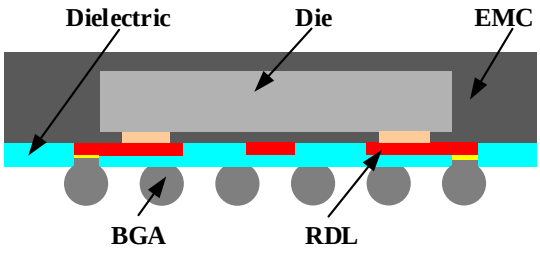

Figure 1.7: Schematic diagram of a fan-out packaging

Wafer- and panel-level fan-out packaging technologies are currently conducted [46]-[48]. Organic substrate embedded packaging is one of the panel-level fan-out technologies. Due to its evident advantages, it is considered as one of the promising applicable packaging technologies for the SiC MOSFET power module. In this dissertation, a novel fan-out SiC MOSFET power module in an organic substrate will be investigated.

1.7. CHALLENGES OF THE ADVANCED PACKAGING

COMPARED with Si counterparts, SiC MOSFET possesses definite advantages in the applications of high operating temperature, high blocking voltage, and high switching frequency. However, these superior performances cannot be fully exploited via current mainstream packaging technologies. SiC MOSFET cannot be used merely as a direct drop-in replacement of Si counterparts in the power module[49]-[51]. To develop the fan-out SiC MOSFET power module, we will face the following four challenges: 1) material selection; 2) packaging technology; 3) performance characterization; 4) and heat dissipation.

1.7.1. MATERIAL SELECTION

The organic substrate is becoming attractive for power electronics as it offers the following advantages: 1) low manufacturing cost for mass production; 2) lightweight; 3) easy high-density integration [52]-[53].

However, most organic substrate materials cannot withstand temperature over 200 °C. Their thermal conductivities are as low as 0.35 W/m·K.

With the same breakdown voltage, commercial SiC MOSFET has smaller chip area and thinner thickness compared to Si counterparts, so the organic substrate in a SiC power module needs to sustain higher electric field strength than that in a Si power module [13].

For organic embedding materials, e.g., FR4 prepreg (glass fiber reinforced uncured epoxy resin), resin-coated copper (RCC), and Ajinomoto build-up film (ABF), are often used [54]-[57]. Munding *et al.* [55] selected FR4 prepreg and RCC as embedding material, respectively, and evaluated thermo-mechanical reliability of the two lead-frame based laminate chip embedded packages through temperature cycle and high-temperature storage experiments. A high glass transition temperature (Tg) FR4 prepreg was found to be more suitable for the embedding package.

Besides, SiC power modules are often used in a harsh environment. Under high ambient temperature and operational temperature, CTE mismatch of different materials within the power modules could induce excessive warpage, stress, and strain, leading to SiC die crack, and interface delamination.

Therefore, the organic substrate should satisfy the following requirements: 1) high-temperature stability; 2) high dielectric strength; 3) high Tg; 4) CTE matching with SiC.

1.7.2. Packaging technology

In recent years, several organic embedded packaging technologies have been developed for the power diode [54], IGBT power module [56]-[57], and GaN devices [58]-[60]. Leadframe-based laminate chip technology is one of the significant representatives [55]-[57]. The bottom sides of power devices are soldered or sintered onto a Cu lead-frame, the resulting assembly is then fully embedded in the prepreg. Electrical interconnections of a power device are realized through laser drilling, electroless plating, Cu plating, and some other processes. However, the structure of the lead-frame based chip embedding package is asymmetrical in the thickness direction, which could easily cause significant stress and strain in the package due to the CTE mismatch between the chip and the Cu lead-frame in a harsh environment. A balanced package structure can relieve stress and strain. Besides, the heat generated from a power device is mainly dissipated into the ambient through a Cu lead-frame, which limits the thermal performance of a power module.

At present, most commercial SiC MOSFETs are designed for Al wire-bonding interconnection. The front-side source and gate metallization of these devices are Al, which cannot be directly used in the fan-out panel-level packaging process. Additional metallization layers on the front-side source and gate pads are required. In Ref. [61], 5 μm thick Cu was added to the MOSFET pads at the wafer level. For SiC MOSFET, however, the cost and risk of pad re-metallization at the wafer-level are high. Kearney *et al.* [56] modified the original metallization layers on the emitter, gate of IGBT chip by sputtering Cr/Cu (5 nm/8 μm) layers, while the dielectric region on the top surface of the IGBT chip was protected with a shadow mask. However, the size of SiC MOSFET is relatively small compared to IGBT, and it is challenging to realize the re-metallization of pads at such a small chip. Besides, SiC MOSFET is a vertical power device, with the gate and source on the front-side and drain on the backside, chip-level physical vapor deposition easily contaminates one side when sputtering the other side. Therefore, the exploration of a new re-metallization technique for the fan-out SiC MOSFET packaging in an organic substrate is essential.

SiC MOSFETs that had the additional metallization layers were then embedded in an organic substrate, followed by blind vias that were usually formed by laser drilling and Cu plating, thus realized the electrical interconnection between the dies and the outer layers [55]-[62]. However, if the laser energy is not properly controlled, the terminal metallization pads could be damaged by laser drilling. The technique is not suitable for devices with very thin pads. Thicker pads are needed. Besides, the drilling process is complex, and the cost is relatively high. A new alternative interconnection technique between the power devices and the outer layers needs to be developed.

1.7.3. PERFORMANCE CHARACTERIZATION

After packaging, the static and dynamic characteristics of the SiC MOSFET power module need to be measured to verify the performance improvement.

On the one hand, a static performance characterization instrument of SiC MOSFETs generally equips with several fixtures for wafer- and package-level measurements, mainly for bare-die and standard discrete devices. The discrete devices mainly include TO-247 and TO-220 packages. Single bare dies and novel packaging structures cannot be directly measured. Although some vendors could provide the performance information of SiC MOSFET bare dies, they provide the general information, and we cannot obtain the data at the specific application condition. To accurately analyze the effect of the fan-out packaging on the performance of bare dies, it is essential to develop the same kind of custom fixture so that we can conduct measurements under the same experimental condition.

On the other hand, it is challenging to accurately compare the dynamic characteristics of the two types of packages. One belongs to the surface mount device, and the other is the TO-247 package. In order to ensure the equality of comparison, the distance and width of the power loop and driver loop of the two packages should be nearly the same, respectively.

1.7.4. HEAT DISSIPATION

The heat flux of the next generation Si IGBT used in pure and hybrid electric vehicles applications would be as high as 500 W/cm^2, more than three times in comparison with the current level of 100-150 W/cm^2 [63]-[65]. As form factor of SiC MOSFET tends to be smaller, its heat flux could reach up to 1 kW/cm^2 in comparison with Si IGBT with the same voltage blocking capability, even higher heat flux is anticipated [66]-[68].

Such high heat fluxes cannot be addressed by using conventional cooling solutions such as vapor chamber [69]-[70], and single-phase liquid cooling [71]-[74]. Vapor chamber in combination with forced convection could dissipate heat flux no more than 100 W/cm^2 [75], while single-phase liquid cooling could reach 350 W/cm^2[76]-[79]. Recently, immersion pool boiling and liquid metal cooling schemes have been reported for high heat flux electronics [75], [80]-[82]. The immersion pool boiling, which requires dielectric fluid to be in contact with the ICs directly, is usually limited by the critical heat flux of dielectric fluid and thus insufficient cooling capacity. The liquid metal has much better thermophysical properties using eutectic alloys of different materials such as gallium, indium, and tin [82], but it may not be compatible with the metal piping and fittings. The cost of liquid metal is also much higher in comparison with other coolants [83].

1

Two-phase flow boiling regimes have received extensive attention in power electronics applications in recent years. Taking advantage of the latent heat vaporization of liquid refrigerant during its boiling process, it can provide higher heat transfer coefficients, lower flow rates, more uniform surface temperatures, and lower pumping power than single-phase cooling scheme [63], [84]-[86]. However, the refrigerant boiling requires a wise control of the pressure and temperature of the refrigerant in the evaporator, so that the isothermal heat absorption can be achieved during the flow boiling process.

1.8. THE LAYOUT OF THIS DISSERTATION

BASED above four challenges, with the motivation of developing new packaging technology and thermal management scheme for SiC MOSFET power module, the dissertation is divided into seven chapters. The dissertation layout is shown in Figure 1.8.

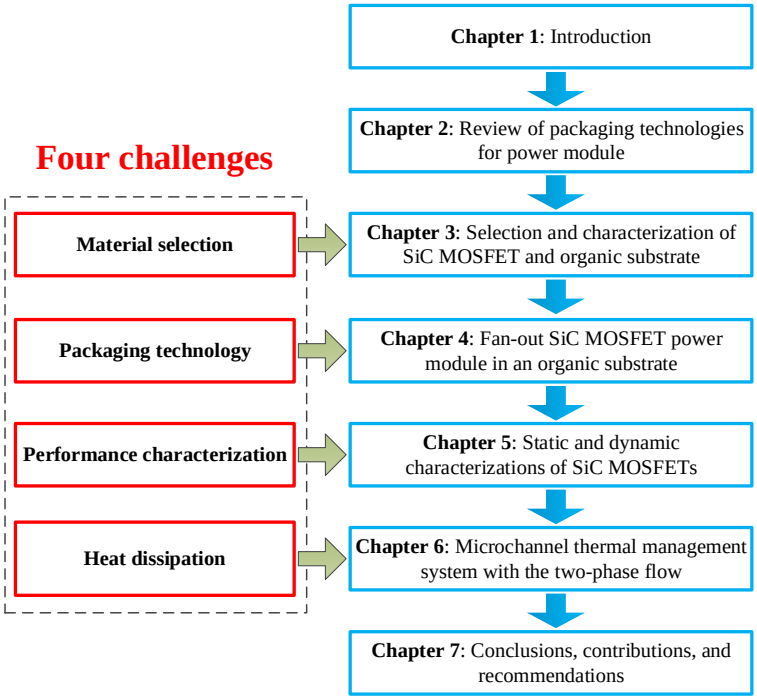

Figure 1.8: Dissertation layout

- In chapter 2, primary packaging schemes for Si power modules, which are the foundation of packaging methods of SiC ones, were first reviewed. Then, attempts on packaging techniques for SiC power modules are thoroughly overviewed. Lastly, a summary of the state-of-the-art packaging technologies for SiC power modules was performed.

- In Chapter 3, SiC MOSFET and organic substrate materials were selected. I-V, C-V, and gate charge characteristics of SiC MOSFET were first analyzed via a custom fixture. Then, thermal stability, dielectric breakdown, and thermo-mechanical performance of the organic substrate materials and cure kinetics of BT prepreg were characterized.

- In Chapter 4, a novel fan-out SiC MOSFET power module in an organic substrate was proposed. The electrical, thermal, and thermal-mechanical simulations were conducted to evaluate and optimize the fan-out packaging performance. A detailed fan-out panel-level packaging process for the phase-leg SiC MOSFET power module was introduced, and three key packaging processes were highlighted.

- In Chapter 5, the static and dynamic characteristics of the fan-out SiC MOSFET power module were studied. First of all, the effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed. Then, the switching performance of the fan-out phase-leg SiC MOSFET was evaluated via double pulse tests. A phase-leg that is composed of two TO-247 discrete packages was used as a benchmark.

- In Chapter 6, a microchannel thermal management system with the two-phase flow is presented for the fan-out SiC MOSFET power module. Due to no available SiC-based thermal test chips on the market, Si-based thermal test vehicles (TTVs) were developed to evaluate the cooling performance of the proposed thermal management system. Environment-friendly refrigerant R1234yf with low boiling points was selected to fill the system. The system mainly consisted of two identical Al microchannel heat sinks (MHSs), a compressor, a condenser, a throttling device, and several accessory measurement components. The cooling performance of the system with one single-chip TTV was first analyzed. For SiC devices with a higher junction temperature of 175 °C, the system's heat dissipation capacity was evaluated. Then, the effects of the rotational speed of the compressor, the opening of the throttling device, TTV layout on MHS, and a downstream heater on the system's cooling performance were analyzed in detail. Lastly, the potential of the cooling performance enhancement was also discussed.

- Chapter 7 concluded the dissertation, summarized the contributions, and discussed the recommendation derived from the results of this dissertation for future research.

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2

Review of packaging technologies for power module

Al wire-bonding interconnection combined with direct-bonded copper substrate has been the most preferred packaging structure for power modules. However, the superior characteristics of SiC power devices cannot be exploited via this packaging structure. In this chapter, primary packaging schemes for Si power modules, which are the foundation of packaging methods of SiC ones, were first reviewed. Then, attempts on packaging techniques for SiC power modules were thoroughly overviewed. Lastly, a summary of the state-of-the-art packaging technologies for SiC power modules was performed.

Parts of this chapter have been published in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 223-238, 2020 [1].

2.1. Packaging techniques for the Si power module

Packaging techniques of the Si power module, which are the foundation of packaging methods of SiC ones, were first reviewed. Various packaging schemes for the Si power module have been developed, such as planar packaging, press-pack, embedded packaging, 3D packaging, and hybrid packaging.

2.1.1. Planar packaging

- Siemens planar interconnect technology

Siemens introduced a novel packaging technique for power modules based on a **pl**anar **i**nterconnect **t**echnology (SiPLIT), as shown in Figure 2.1. The SiPLIT featured thick copper (Cu) interconnects on a high-reliable insulating film for top contacts of power chip. Due to the conductor structure and contact technology, both on-resistance and parasitic inductances of the power module were lower than state-of-the-art aluminum (Al) wire-bonded interconnection. Also, the large area contacting improved power cycling capability and surge current robustness significantly. Through electrical and thermal characterization, up to 50% reduction in parasitic inductances of the interconnects, and a remarkable 20% decrease in thermal resistance were achieved [2].

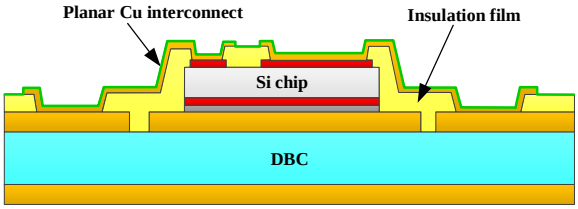


Figure 2.1: Cross-section of the power module with planar interconnects [2].

- Cu clip bonding technology

The concept of Cu clip bonding technology is illustrated in Figure 2.2. A flat Cu clip replaced Al wire-bonds. Due to high electrical and thermal conductivity, the Cu clip could not only improve the switching characteristics of the power module but also provide an additional heat conduction path from the top surface of the die [3]-[4]. Compared with the conventional wire-bonded counterpart, up to 23% reduction in junction-to-case thermal resistance for one individual die and an 18% decrease for parallel operation of two dies were observed in the single-sided cooling tests. While in the double-sided cooling experiments, an additional average 18% thermal improvement was achieved due to the addition of a top fan-cooled heatsink mounted onto the Cu clip [4].

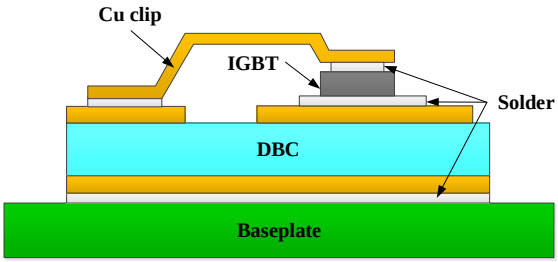


Figure 2.2: Structure diagram of Cu clip bonding package [4].

- Multilayer planar interconnection package

Liang *et al*. [5] proposed a multilayer planar interconnection package structure for a 200 A/1200 V IGBT phase-leg power module, as shown in Figure 2.3. The IGBT and diode dies were sandwiched between two symmetric substrates, providing planar electrical interconnections and insulation. Two mini coolers were directly bonded to the outer surface of the two substrates, allowing for double-side integrated cooling. The upper and lower switch pairs in the phase-leg were oriented in a face-up/face-down configuration. The bonding areas between dies and substrates, as well as substrates and coolers, were designed to use identical materials and were formed in one heating process. Compared with the wire-bonded power module, total inductance and resistance of the planar-bonded power module decreased by 62% and 90.6%, respectively. Besides, the voltage overshoot reduced by 54%, and the total power loss of the planar bond package was less than 10% of that of the wire-bonded package. The double-sided cooling of the planar module reduced the specified thermal resistance to 0.33 °C·cm^2/W, which was 38% lower than that of the wire-bonded power module.

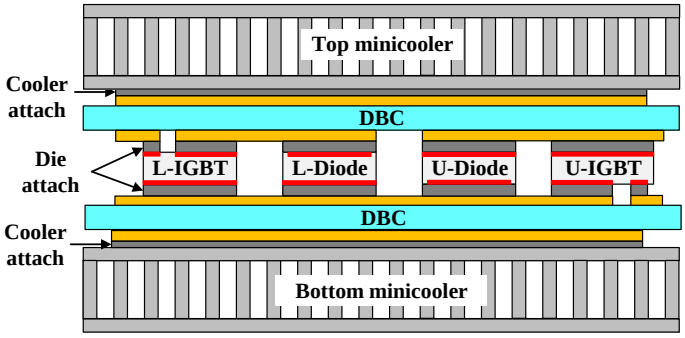


Figure 2.3: Multilayer planar interconnection package structure [5].

- Transfer molded power module package

Mitsubishi reported a simple, compact, robust, and high-performance transfer molded power module (T-PM) with direct lead bonding (DLB) technology, as illustrated in Figure 2.4. Cu lead was directly bonded on the emitter and cathode electrodes by lead-free solder, and Al conventional wire was bonded on the gate electrode. To improve the thermal performance of the T-PM, a high thermally conductive electrically insulating layer (TCIL) was applied to the module. Compared with the conventional wire-bonded power module, the T-PM showed 43% and 50% reduction in parasitic inductance and parasitic resistance, respectively [6].

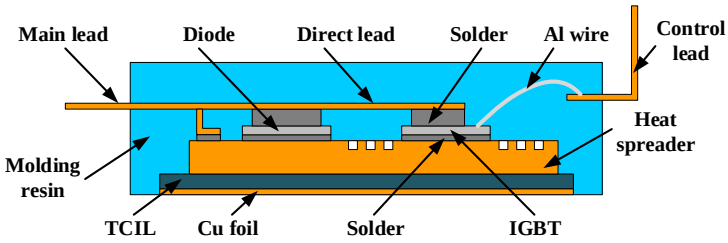


Figure 2.4: Structure diagram of DLB package [6].

- Spacer-based sandwich structure

Figure 2.5 shows the schematic of a spacer-based sandwich structure for an IGBT power module. Cu spacers with different thicknesses were used to accommodate height differences between IGBT and diode in the power module [7]-[8]. A SAC305 solder sheet was selected as a die-attach material. Additional metallization layers [titanium/nickel/silver (Ti/Ni/Ag)] (60/500/800 nm) were sputtered on the front-side source and gate pads to increase the wettability of the solder [7]. Compared with the conventional IGBT power module, 55.1% and 13.2% reductions in parasitic inductance and resistance, and a 47.5% decrease in thermal resistance were achieved.

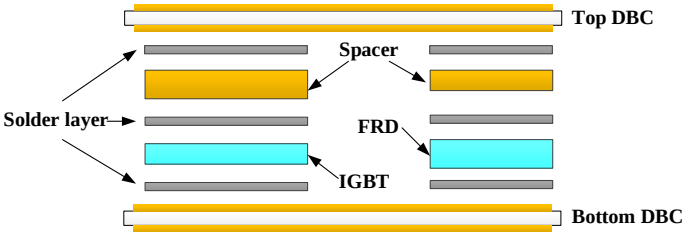


Figure 2.5: Schematic of a spacer-based sandwich structure [7].

2.1.2. PRESS-PACK PACKAGING

Press-pack is a packaging approach that uses pressure contact instead of wire bonding and soldering in conventional power modules. Press-pack packaging schemes have been developed for high-voltage and high-current applications. Figure 2.6 displays the internal construction of a rigid press-pack IGBT power module from Westcode [9]-[10]. This package employs a hermetically sealed ceramic housing, with connections to the chips made by physical contact pressure via external clamping between rigid electrodes and strain buffers. Molybdenum (Mo) plates are usually used to ease the stress of the package induced in the operating condition.

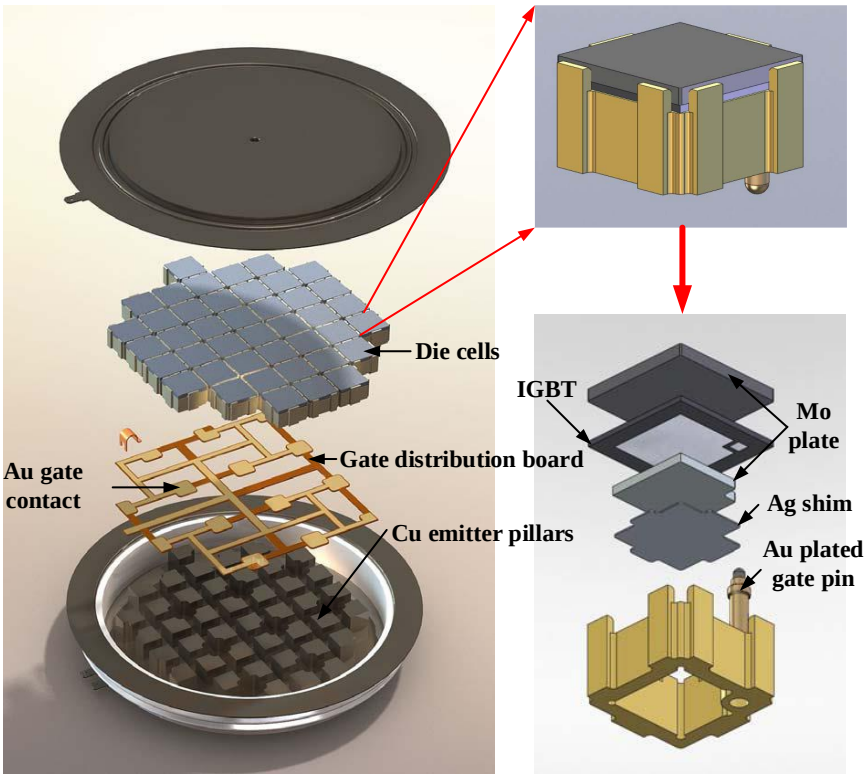
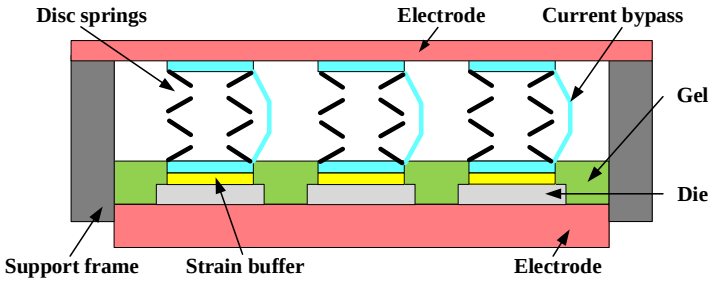
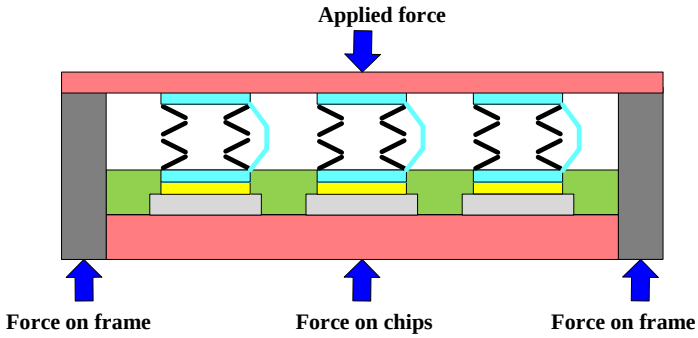


Figure 2.6: Internal construction of a rigid press-pack IGBT from Westcode [10].

Figure 2.7 shows the construction of a compliant press-pack power module. This kind of power module currently available, such as those manufactured by ABB, employs non-hermetic plastic housing, the actual contact pressure made to the individual chip surfaces is controlled locally by disc spring assemblies inside the package [11].



(a) Before compression



(b) After compression

Figure 2.7: Construction of a compliant press-pack IGBT [11].

2.1.3. EMBEDDING PACKAGING

To minimize the packaging size and increase the integration density of the power module, ceramic- and PCB-based embedding packaging schemes have been developed.

- Ceramic-embedded power module

Figure 2.8 shows the schematic of a ceramic-embedded power module [12]. Multiple power chips, such as IGBT, MOSFET, and diode, could be embedded in a ceramic frame and covered by a dielectric layer with via holes on the Al pads of the chips. Then, metallization multilayers were deposited on the whole surface, which formed contacts with the Al pads on the chips through via holes in the interlayer. Conventional sputtering was employed to add thin-film Ti and Cu layers. Electroplating was used to form thicker Cu deposition. Finally, the metallization layer was patterned to form both power and control circuits as well as their I/O terminals. Compared with the conventional wire-bonded package, a 75% reduction in parasitic inductance and a 44% improvement in thermal dissipation performance were achieved.

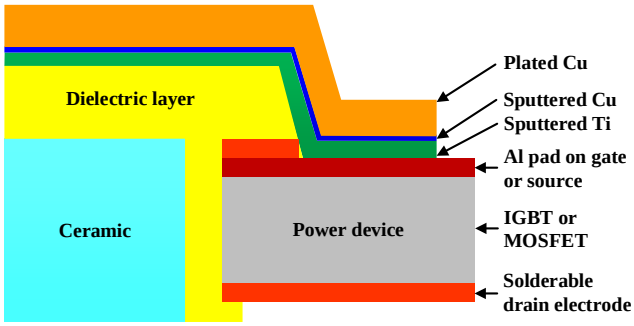


Figure 2.8: Structure schematic of a ceramic-embedded power module [12].

- PCB-embedded power module

Printed circuit board (PCB) embedded package, also called "Chip in Polymer" technology, was first introduced by Fraunhofer IZM and TU Berlin [13]. The ultra-thin semiconductor chips were embedded into the build-up layers of PCB together with integrated passive components. The electrical interconnection between the chip and the outer-layer footprints were realized by laser-drilled and metalized micro-vias [13]-[15]. The detailed packaging process is shown in Figure 2.9 [15].

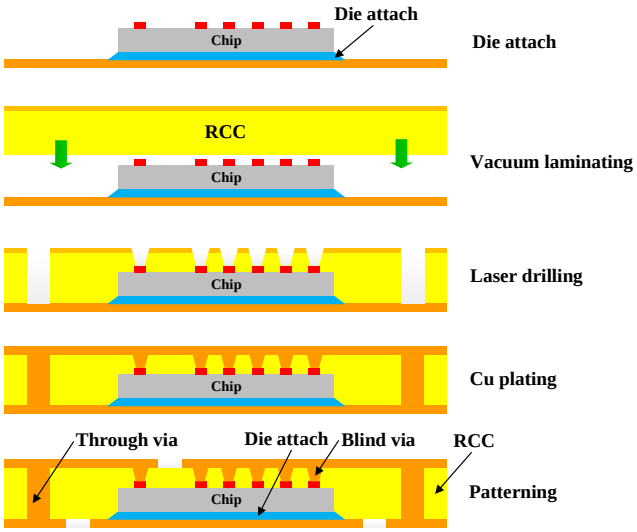


Figure 2.9: Process flow of PCB-embedded package developed by Fraunhofer IZM and TU Berlin [15].

In 2013, Fraunhofer IZM and TU Berlin developed a PCB-embedded packaging scheme for Si IGBT power module [16]. To be compatible with laser drilling and Cu plating, a thin electroless Ni/palladium layer was added on the top surfaces of IGBTs and diodes. Figure 2.10 shows the process flow. First of all, a base substrate was fabricated by laminating two layers of thick Cu and one layer of thermally conductive prepreg. The top Cu layer was structured and selectively metalized by immersion Ag. Then, Ag sinter paste was printed to Ag areas and IGBTs and diodes were placed and sintered to the substrate at 200 °C with a relatively low pressure of 2 MPa. Thirdly, IGBTs and diodes were embedded into a prepreg layer with 105 µm Cu foil through vacuum lamination. Vias to chip pads and thick Cu were drilled by laser. Finally, the vias were filled with Cu by electroplating, and the Cu was structured by etching [16].

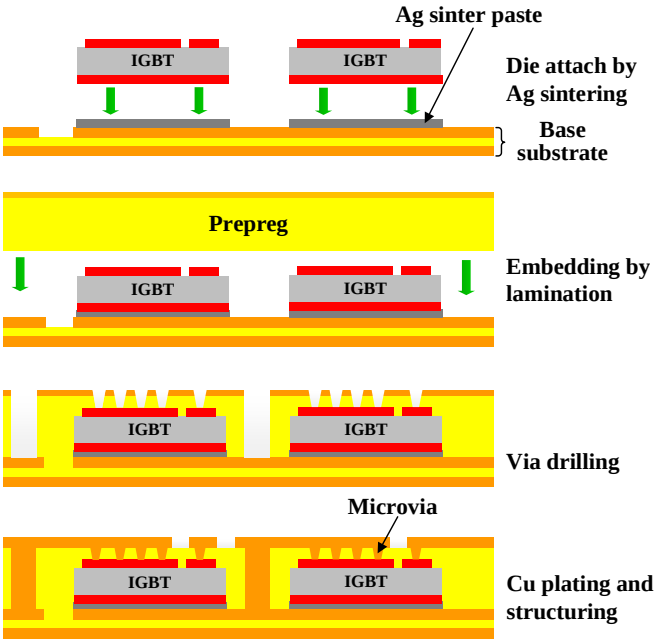


Figure 2.10: Process flow of PCB-embedded IGBT developed by Fraunhofer IZM and TU Berlin [16].

The PCB embedded packaging technology combines standard PCB processing with the addition of high-accuracy component placement and handling. There are two primary packaging processes for embedding chips using the chip-first approach: die face-up and face-down, as shown in Figure 2.11 [17]. Both packaging processes mainly include die-attach, lamination, via drilling, and Cu plating and structure. Die attach material used in the face-down process is non-conductive adhesive. For face-up technology, die-attach materials can be non-conductive adhesive, solder, Cu/Ag nanoparticle paste, and transient liquid phase bonding materials. The face-up technology is more suitable for high power-density vertical dies, such as power MOSFET, IGBT, and power diode.

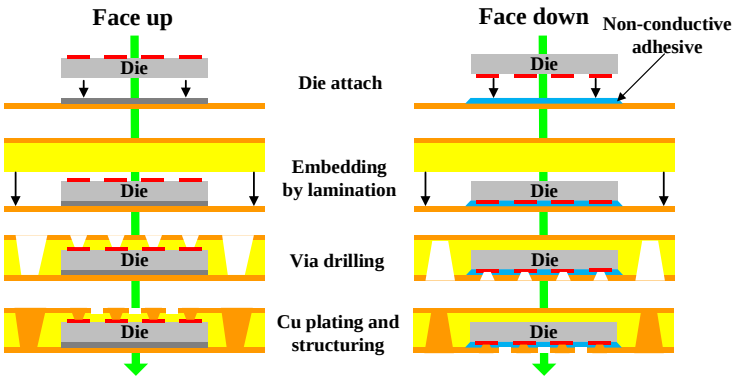


Figure 2.11: PCB embedding process flows: face up (left) and face down (right) [17].

Pascal *et al*. [18] proposed an innovative PCB-embedded manufacturing process, as shown in Figure 2.12. They used a piece of Ni foam to create a pressed contact between the top side of a power diode and the rest of the circuit. The average pore diameter of the nickel foam was about 350 μm, and there were 57~63 pores per inch. The detailed packaging process flow is shown as follows: First of all, the diode's bottom side was soldered onto a bottom PCB. Then, a piece of nickel foam, four layers of prepregs, and a top PCB were positioned above the bottom PCB, as shown in Figure 2.12(b). Thirdly, the stack was laminated through high-temperature and high-pressure processes, and the epoxy resin polymerized and flooded the foam. Compared with other PCB integration techniques, the proposed process is simple and cost-effective.

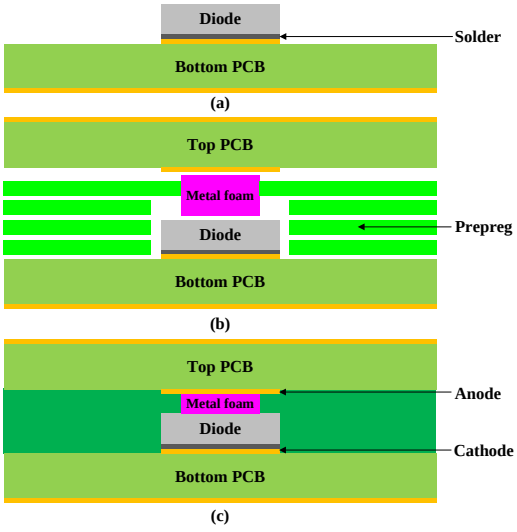


Figure 2.12: Steps of packaging process using metal foam [18].

Munding *et al.* [19] reported a new lead-frame based laminate chip embedding technology. Figure 2.13 illustrates the packaging process flow. For power dies with vertical current flow, diffusion solder was adopted as a die-attach, while for gate driver, insulating glue was used. They presented a study on the laminate material choice and found that prepreg material with highly filled glass fibers and high glass transition temperature was more robust than resin-coated copper material. They proposed a novel approach to avoid lamination voids, validated lamination process simulation based on the Monte-Carlo method, and could predict process stability for a specific set of parameters and parameter variations. Finally, they systematically analyzed the physics mechanism of laser-induced chip metallization damage and defined countermeasures to avoid such damage.

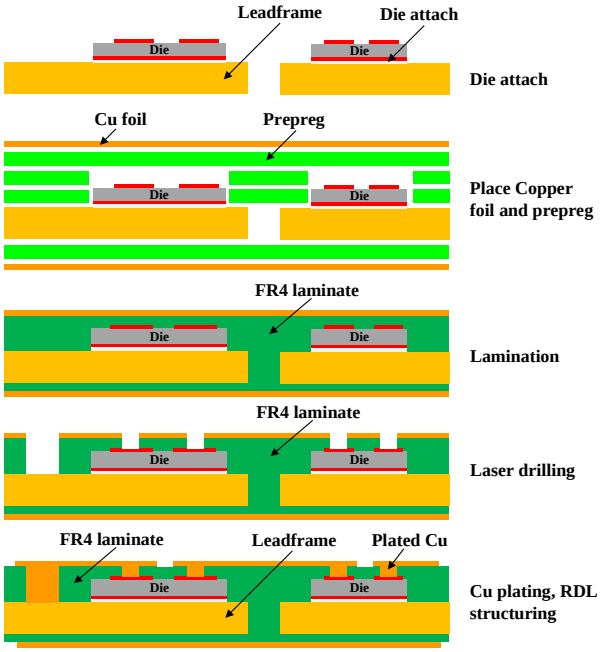


Figure 2.13: Process flow of lead-frame based laminate chip technology [19].

Kearney *et al.* [20] developed a 1200 V PCB-embedded three-phase IGBT inverter module, as displayed in Figure 2.14. The Al metallization layers of the emitter, gate, and anode contact were first modified by sputtering chromium (Cr)/Cu (5 nm/8 μm) layers, while a portion of the individual chip was protected with a shadow mask. Then, six pairs of IGBT and diodes were sintered into a Cu lead-frame with pre-machined cavities. Cu vias from outer Cu traces to chip pads were formed by laser drilling and plating. Comparing the switching performance, thermal resistance, breakdown insulation, partial discharge, and long-term reliability with Semikron MiniSKiiP 23AC126V1, which used a traditional direct bonded copper (DBC) sandwich structure, the PCB-embedded module improved thermal management, reliability, and insulation.

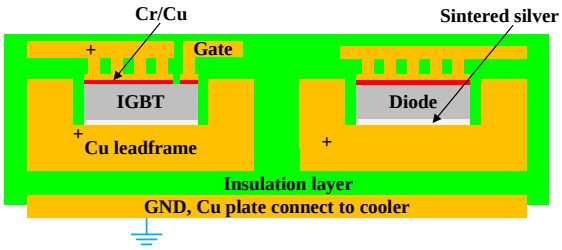


Figure 2.14: PCB-embedded three-phase inverter module [20]

AT&S developed a panel-level PCB-embedded packaging technology for a GaN lateral device, known as embedded component packaging (ECP^{TM}). Figure 2.15 [21] shows the packaging process flow of ECP^{TM}. A die was attached to a layer of dielectric on a Cu foil. The die was then covered and laminated by four layers of prepregs and one layer of Cu foil. The micro-vias were used as electrical interconnections and thermal conduction between the chip and Cu layers on the top- and bottom-surface [22]-[23].

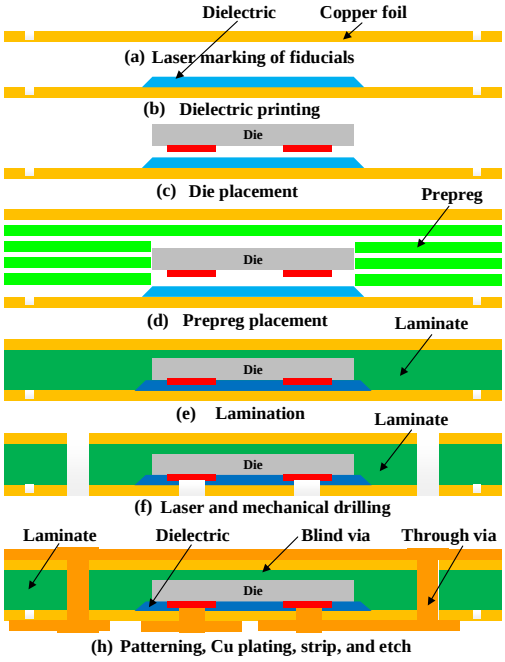


Figure 2.15: ECP^{TM} process flow [21].

Chang *et al*. [24] presented an IGBT power module by chip embedding technology. The packaging process flow is shown in Figure 2.16. Because the size and thickness of IGBT and diode are different, a half-etched Cu lead frame was designed and fabricated. The IGBTs were attached to the lead-frame by SAC305 solder paste, whereas the thicker diodes were sintered onto the half-etched Cu lead frame. Then, an Ajinomoto Build-up Film (ABF) lamination process was conducted to form a built-up dielectric layer on the Cu lead frame. Next, the blind vias and circuits were formed on the built-up dielectric layer by an ultraviolet laser and were metalized with a sputtered seed layer and electroplating. To form a circuit pattern, an additional 1 μm thick Sn layer was subsequently plated as a patterning mask, and a laser skiving process was conducted to remove the Sn above the Cu layer. Consequently, the etching of Cu, Sn, and Ti processes was performed to remove the metal on the dielectric layer, thus forming the required circuit pattern. Finally, a layer of soldermask was printed to prevent electric shock on the surface layer.

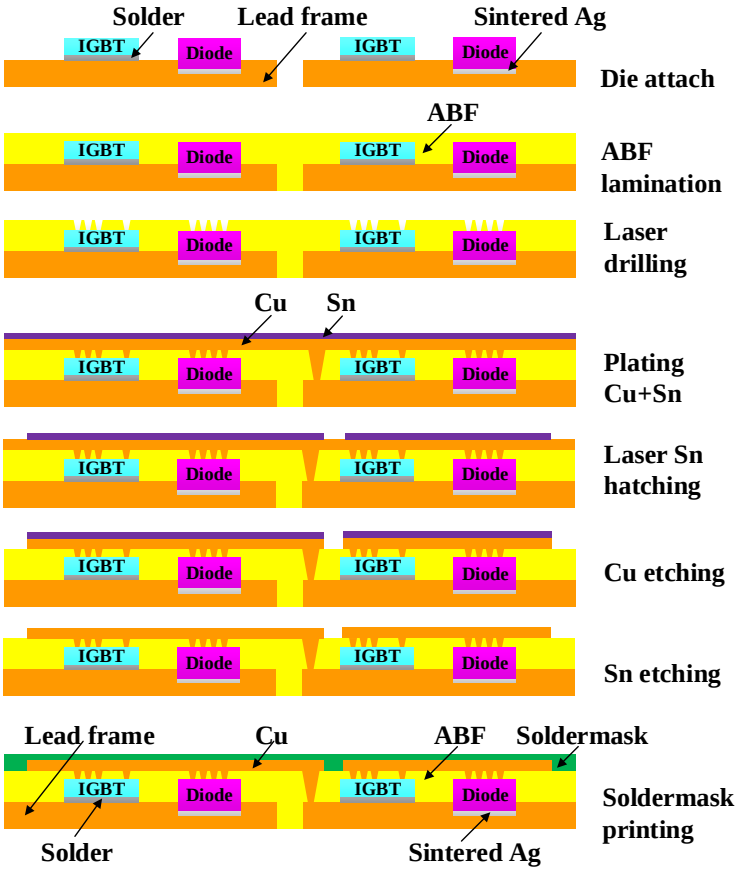
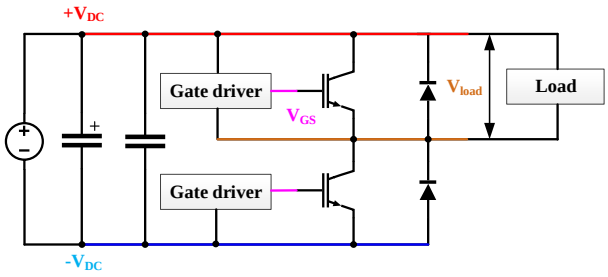


Figure 2.16: Process flow of an IGBT power module by chip embedding technology [24].

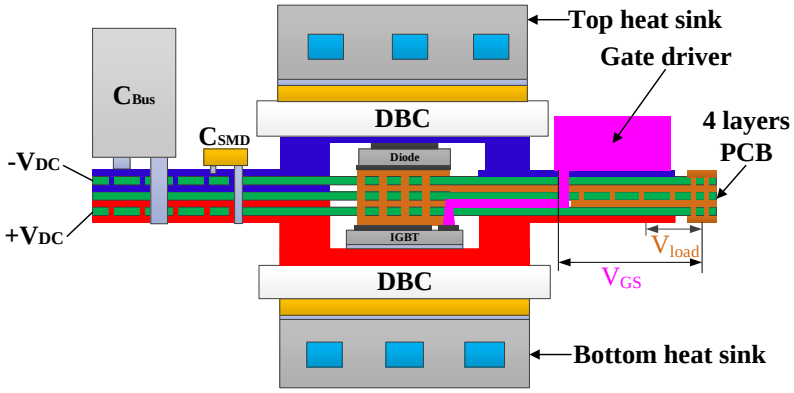
2.1.4. 3D PACKAGING

- Power chip-on-chip package

To reduce parasitic inductances, Marchesini *et al.* [25] presented a power chip-on-chip (PCoC) packaging technology for IGBT power module. Figure 2.17(a) and (b) shows the electrical circuit and structure diagram of the PCoC package. The electrical interconnection of the switching cell was realized through two DBC substrates and a 4-layer PCB. DC link and decoupling capacitors were integrated directly on the PCB. The experimental results showed that the parasitic inductance of the PCoC module was drastically reduced compared with planar ones, especially when internal decoupling capacitors were integrated into the assembly.



(a) Electrical circuit



(b) Structure diagram

Figure 2.17: PCoC package [25].

- Power chip-on-inductor package

In our previous work [26], a power chip-on-inductor (PCoI) packaging technique with double-sided cooling was presented. Figure 2.18 shows the structure diagram of the PCoI

package. A fan-out panel-level PCB-embedded packaging technique for power MOSFETs and low temperature co-fired ceramic (LTCC) inductor in a synchronous converter was proposed. The power MOSFETs and the LTCC inductor were embedded in the top and bottom PCB, respectively. The stacking of the top PCB and the bottom PCB was implemented to form a 3D integrated power supply module. The MOSFETs, gate driver, and passive components were interconnected by the redistribution layer (RDL) and PCB vias. According to thermal simulation results, PCB vias improved the thermal performance of the 3D module with a cap heat spreader, which could effectively dissipate the heat of the PCB-embedded 3D power supply module.

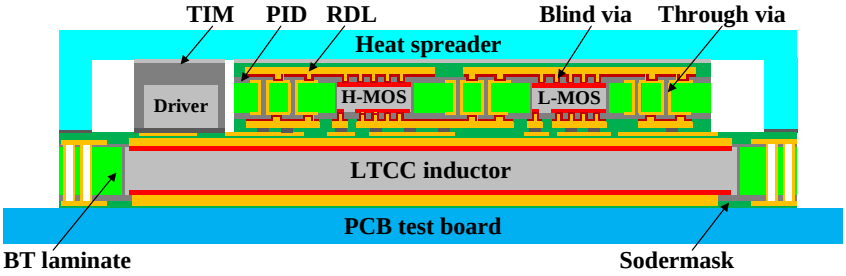


Figure 2.18: Structure diagram of PCoI package [26].

- Solderless leadframe assisted wafer-level packaging

In Ref. [27], a wafer-level packaging technique for the power module was presented. Figure 2.19 shows the schematic of the assembly with two Si wafers covered with a Cu layer and the patterned and perforated Cu lead-frame. A metallic lead-frame was bonded between two wafers of semiconductor devices. A solderless, thermo-compression bonding realized the 3D assembly of the power devices and the metallic lead frame.

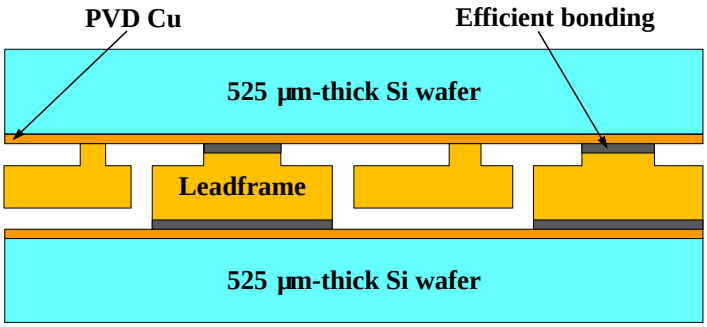


Figure 2.19: Schematics of the assembly with two Si wafers covered with Cu layer and Cu lead frame [27].

- Micro-post-based sandwich structure

The micro-post-based sandwich structure is one of the 3D interconnection configurations with double-sided cooling capability. Figure 2.20 shows the schematic of Cu micro-post interconnection for the power module. The Cu micro-posts were electroplated on the topside of the die. The die with its micro-posts was then attached to a top DBC substrate using a Cu/Sn transient liquid phase (TLP) technique. An assembly of the backside of the die to a bottom DBC substrate was processed concurrently using the same TLP technique [28]. In the bonding technique, a layer 0.5 μm Sn was deposited on the top of micro-posts, which was used as solder between posts and Cu of DBC substrate. Another bonding solution, Cu-Cu bonding, does not need any additional materials between micro-posts and Cu of DBC substrate [29].

The micro-post-based sandwich structure allows for double-sided cooling. The Cu posts provide spacing between the die and the top substrate. They are also useful to accommodate height differences between dies in a multichip power module. Different types of dies (such as IGBT and diode), which are commonly used in a single module, do not always have the same thickness. The Cu micro-posts can compensate for thickness differences between the dies [30].

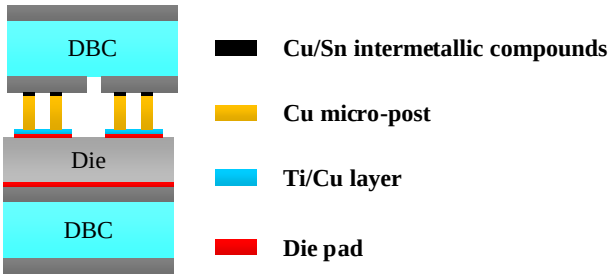


Figure 2.20: Schematic of Cu micro-post interconnection for power module [28].

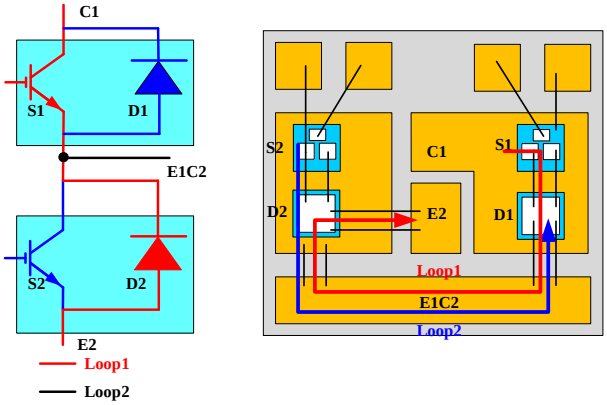
2.1.5. HYBRID PACKAGING

Since high-power devices are usually metalized by Al on their top pads to be suitable for Al bonding wires, almost all wire-bondless packaging technologies require that the top electrode pads of power devices be re-metalized. However, for hybrid packaging, the re-metallization is not a necessary process, and wire bonding techniques are still suitable.

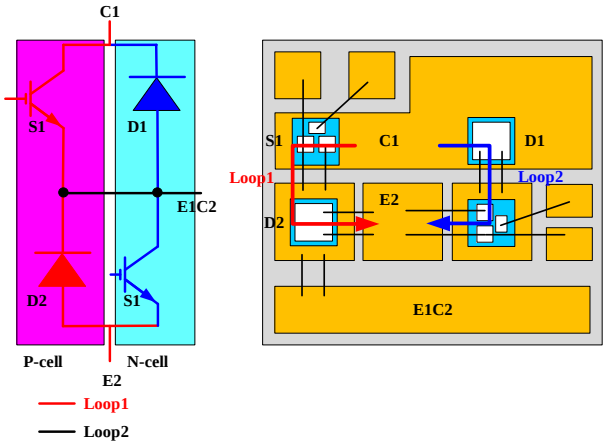
- Switching cells-based package

In Ref. [31], a switching cell-based phase-leg IGBT power module was proposed. Figure 2.21(a) and (b) shows the conventional and switching-based power modules, respectively. Compared with the conventional power module, two devices in the commutation

loop of the switching cell-based module were placed on the same side. Thus the physical length of the commutation loop was reduced. The parasitic inductance reduction of the layout design was in the range of 5~10 nH.



(a) Conventional module



(b) P-cell and N-cell-based module.

Figure 2.21: Switching cell-based IGBT phage-leg package layout [31].

Several packaging techniques for the Si power module have been developed. Table 2.1 presents a summary of features of different packaging schemes for the Si power module. The interconnection, e.g., Cu clip, Cu lead, RDL, could replace conventional wire-bonding. Cu spacers, etched lead-frame, and micro-posts could compensate for the thickness differences of different types of power dies.

Table 2.1: Summary of features of different packaging schemes for the Si power module

Packaging scheme	**Features**
SiPLIT [2]	1) Thick Cu interconnects on a high-reliable insulating film; 2) 50% parasitic inductances reduction; 3) 20% thermal resistance decrease.
Cu clip [3]-[4]	1) Cu clip replaces wire-bonds; 2) Up to 23% reduction in junction-to-case thermal resistance for one individual die.
Multilayer planar interconnection [5]	1) Double-sided cooling and structure symmetry; 2) Switch pairs in the phase-leg are oriented in face-up/face-down configuration; 3) Total inductance is 12.08 nH; 4) Specified thermal resistance is 0.33 °C·cm^2/W.
T-PM [6]	1) Cu lead is directly bonded on the emitter and cathode electrodes by Pb-free solder; 2) TCIL is applied to the module.
Spacer-based sandwich [7]-[8]	1) Double-sided cooling; 2) Cu spacers with different thickness are used to accommodate height differences; 3) 55.1% and 13.2% reduction in parasitic inductance and resistance and 47.5% decrease in thermal resistance are achieved.
Press-pack [9]-[11]	1) Pressure contact replaces wire-bonding and soldering; 2) High-voltage and high-current application.
Ceramic embedded package [12]	1) Multiple power dies are embedded in a ceramic substrate; 2) 75% reduction in parasitic inductance and 44% improvement thermal dissipation performance are achieved.
PCB-embedded package [13]-[23]	1) Small form factor; 2) Lightweight; 3) Simple packaging process.
PCoC package [25]	1) 3D integration through DBC and PCB; 2) DC link and decoupling capacitors are integrated on the PCB.
PCoI package [26]	1) The power MOSFET and LTCC inductor were embedded in a different PCB and stacked together; 2) Double-sided cooling.
Wafer-level package [27]	Power devices and lead-frame are bonded by a solderless, thermocompression process.
Micro-post-based sandwich [28]	1) Double-sided cooling; 2) Micro-posts on the top of power dies can be performed at wafer level; 3) Micro-posts can compensate for thickness differences between the dies.
Switching cells-based package [31]	Reduction in the physical length of commutation loop. The parasitic inductance reduction of the layout design was 5~10 nH.

2.2. Packaging schemes for SiC power module

To reduce the parasitic inductances of the SiC power module, some attempts on packaging techniques for SiC power modules, e.g., planar packaging, press-pack, 3D packaging, and hybrid packaging techniques, have been performed. In this section, recent developments of these technologies were thoroughly overviewed.

2.2.1. Planar packaging

- Miniaturized double-sided cooling

Woo *et al.* [32] developed a miniaturized double-sided cooling packaging for SiC high-power inverter module using new materials to withstand high temperatures over 220 °C, as shown Figure 2.22. The flip-chip bonding for source and gate interconnections was developed, and Bi-Ag solder paste was adopted. Its solidus temperature is around 260 °C, and the liquidus temperature is about 360 °C, which has much high thermal stability than conventional lead-free solder. An electroless nickel immersion gold process on the Al bonding pads on the MOSFET surface was performed to increase the wettability of solder paste. For drain interconnection, Cu clips were attached using Ag sintering materials. The power module's thermal dissipation performance was found to be enhanced by twice as much as the conventional single-sided cooling type power module through thermal modeling and characterization.

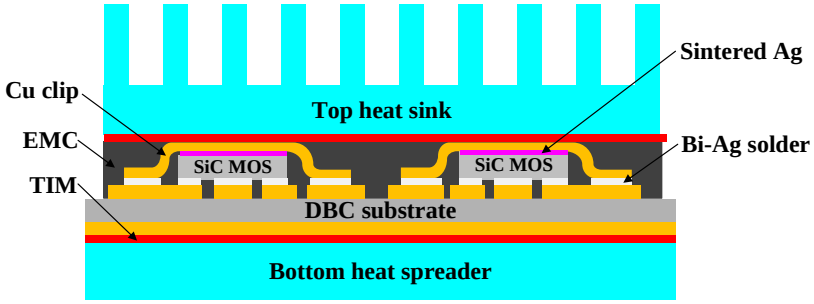


Figure 2.22: Double-sided cooling packaging for SiC high-power inverter module [32].

- Power overlay interconnect packaging

General Electric developed a power overlay (POL) interconnect technology for SiC MOSFET packaging. The drains of SiC MOSFETs were soldered on the DBC substrate, the sources and gates were interconnected by a flexible substrate, as shown in Figure 2.23. When drain-source voltage was 540 V and the drain current was 300 A, and the voltage rise time was 11.2 ns, the voltage overshoot was below 28% [33].

In 2018, they presented a power overlay kiloWatt (POL-kW) for the SiC power module. Figure 2.24 shows the schematic of a typical POL-kW module structure. Cu vias were used as interconnects between dies (Al pads) and routings on the polyimide film surface.

The adhesive layer was used to attach dies to the polyimide film. Cu vias were formed by laser drilling and subsequently filled by electroplating. DBC substrate (Ni/Au finish) was soldered to the die backside metallization (Ag finish). An underfill was applied for electrical isolation and mechanical strengthening. Compared with the conventional wire-bonded package, the utilization of polyimide-based Cu via interconnections resulted in much reduced parasitic inductance, contributing to significantly lower switching loss and less voltage overshoot [34].

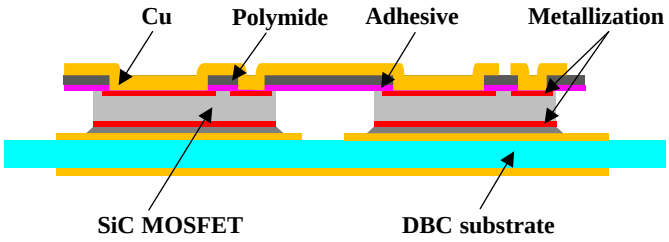


Figure 2.23: Schematic of POL interconnect package for SiC MOSFETs [33].

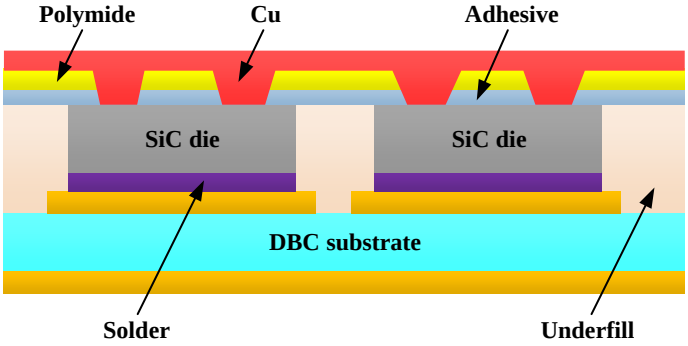


Figure 2.24: Schematic of a typical POL-kW module structure [34].

- LTCC-based double-sided cooling module

Zhang *et al.* [35] proposed a LTCC-based SiC power module with double-sided cooling, as shown in Figure 2.25. An LTCC substrate was used as a dielectric and chip carrier. Ag nanoparticle (NP) paste was used to attach power devices to the top and bottom DBC substrates. The top and bottom sides of DBC were plated with Ag. Subsequent layers of Cr/Ni/Ag were deposited on top of the anode of the diode, the source, and gate of the MOSFET through a lift-off process. A high-temperature dielectric material was used to fill

the gaps between the LTCC substrate carrier and the power devices to protect the power devices from electrical breakdown during operation. Simulation results showed that, compared with the wire-bonded module, the thermal resistance and parasitic inductances of the LTCC-based double-sided cooling module decreased by 59% and 54~85%, respectively.

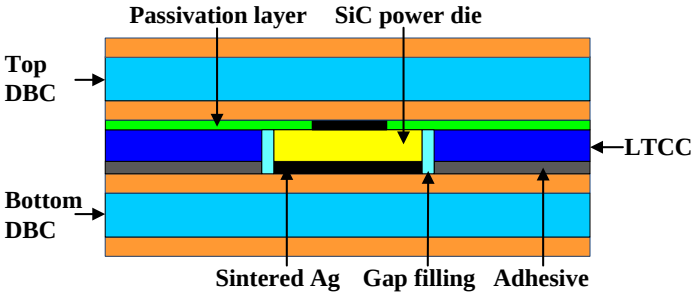


Figure 2.25: Schematic of LTCC-based double-sided cooling module [35].

- 6-in-1 power module

In Ref. [36], a magnetic cancellation effect was used to reduce the parasitic inductance. Figure 2.26 shows the schematic of a 6-in-1 SiC power module with double-sided cooling. Heat spreader was utilized as magnetic cancellation. Laminated busbar had an insulation film between the positive and negative terminal, in which current paths were in opposite directions. Current paths between chips were also configured to be opposite directions. Parasitic inductance of 7.5 nH was obtained.

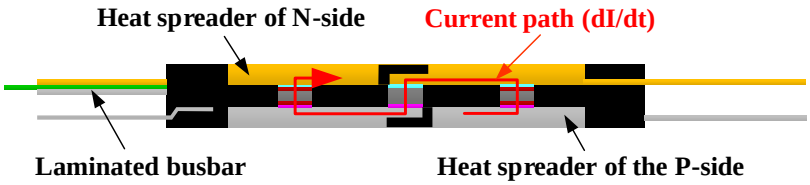


Figure 2.26: Current path and structure view of a 6-in-1 power module [36].

- Power chip on bus module

In Ref. [37], a double-sided air-cooled power chip on bus (PCoB) power module was proposed. Figure 2.27 shows the structure view of the PCoB power module. Thick finned Cu acts as both heatsink and busbar. SiC dies are electrically attached to two busbar-like

power substrates directly. Mo spacers are used as CTE buffer between the die and the bottom substrate for reducing thermo-mechanical stress caused by CTE mismatch. Through extensive multi-physics simulation and experimental verification, 0.5 °C/W thermal resistance, and 8 nH power loop parasitic inductance were achieved.

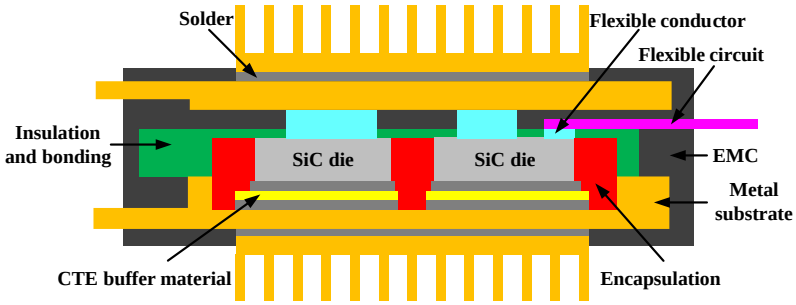


Figure 2.27: Structure view of PCoB power module [37].

2.2.2. PRESS-PACK PACKAGING

Zhu *et al.* [38] proposed a press-pack packaging solution for SiC MOSFETs, as shown in Figure 2.28. A pressure contact solution for SiC MOSFETs was developed using miniature and flexible press pins called "fuzz buttons" in a low-profile LTCC interposer. To minimize the parasitic loop inductance being introduced by heat sinks, ultrathin microchannel heatsinks were designed based on LTCC technology. A phase-leg stack prototype with two press-packs and three heatsinks was developed. According to simulation results, the internal parasitic inductances of the press-pack were less than 550 pH, the commutation loop inductance was 4.3 nH at 100 kHz, the junction-to-heatsink thermal resistance was about 0.2 K/W, and the heatsink-to-coolant thermal resistance was about 0.8 K/W.

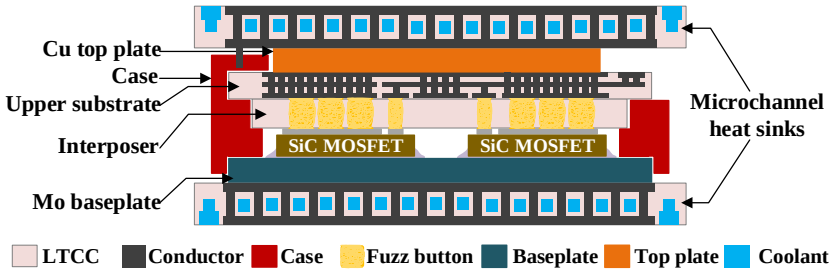


Figure 2.28: A press-pack packaging solution for SiC MOSFETs [38].

2.2.3. 3D PACKAGING

- Chip scale, flip-chip capable package

S. Seal *et al.* [39]-[40] developed a chip-scale wire-bondless packaging technology for a SiC Schottky diode that led to lower parasitics, higher reliability, lower costs, and lower losses. The approach used a flip-chip solder ball array to make connections to the anode. A Cu connector was used to make contact with the bottom cathode, thus reconfiguring the bare die into a chip-scale, flip-chip capable device [39]-[41]. Compared with the conventional wire-bonded package, a 24% reduction in on-state resistance was observed in the wire-bondless package.

In 2018, they presented a 3D wire-bondless switching cell using SiC power devices, as shown in Figure 2.29. In order to obtain a solderable finish, a very thin zinc seed layer was deposited on the top Al pads, followed by the electroless plating of a thick Ni layer. Double-pulse tests showed that over 3 times was decreased in the parasitic inductance of the 3D switching cell compared with the conventional wire-bonded module [42].

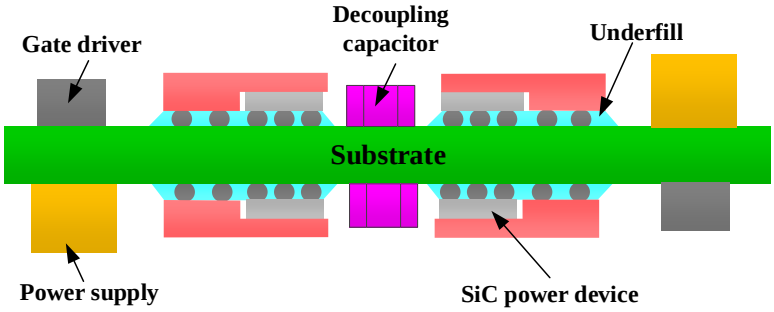


Figure 2.29: A diagram of a 3D wire-bondless switching cells [42].

- Cu pin connection technology

Fuji Electric developed a Cu pin connection technology for the SiC power module, as illustrated in Figure 2.30. Conventional Al wire-bonds, solder joints, and silicone gel encapsulating structures were replaced with Cu pin connections, Ag sintering joints, and epoxy resin molding structures, respectively. To further reduce thermal resistance, a much thicker Cu block was bonded to the silicon nitride (Si_3N_4) ceramic substrate. Compared with the conventional alumina ceramic structure, the Cu pin structure enabled a 50% reduction in the overall structure's thermal resistance. Compared with the conventional Si-based wire-bonded package, the power loss reduction with SiC devices was 57~87% using the Cu pin structure [43]-[44].

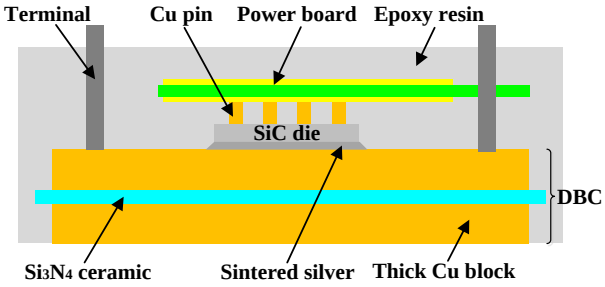


Figure 2.30: Package structure schematic of SiC power module with Cu pin [43]-[44].

- SKiN interconnect technology

SKiN comprises sintering of SiC dies to a DBC substrate, a top side sintering of the power dies to a flexible printed circuit (FPC), and sintering of the substrate to a pin-fin heat sink [45], as shown in Figure 2.31. Now the SKiN has been used in a 1200 V/400 A phase-leg SiC power module. The phase-leg module with 8×50 A SiC MOSFET chips in parallel had a total commutation parasitic inductance of less than 1.4 nH [46].

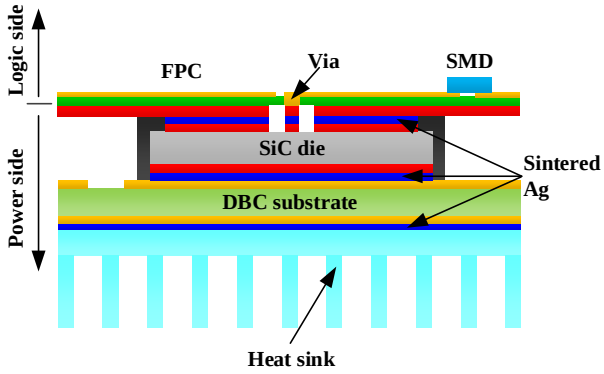


Figure 2.31: SKiN double-side sintering package [45].

2.2.4. HYBRID PACKAGING

- DBC and PCB hybrid structure

In Ref. [47], a DBC and PCB hybrid structure for the SiC power module was developed, as shown in Figure 2.32. A multilayer PCB with grooves was attached to the DBC substrate. SiC devices were fit in the grooves and attached to the DBC substrate. Bonding wires were then used to connect the top electrodes of the device to the top Cu trace on the PCB.

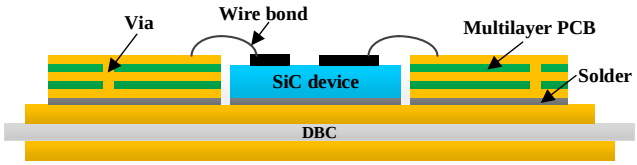


Figure 2.32: Cross-sectional view of DBC and PCB hybrid structure [47].

- DBC and FPC hybrid structure

In Ref. [48], a 1200 V/120 A SiC phase-leg power module based on DBC and FPC hybrid structure was proposed. Figure 2.33 shows the DBC and FPC hybrid structure and the commutation loop associated with MOSFET (Q1) and diode (D2). Since the opposite currents flowed through the thin FPC board, the cancellation of the magnetic coupling effect was strong. The parasitic inductance of the power module could be significantly minimized to only 0.79 nH by using the thin FPC and proper layout design. Compared with the commercial module, the voltage overshoot of the hybrid structure module was decreased by about 50%, and switching energies were only one-third of the commercial module under the same decoupling capacitors and driving conditions.

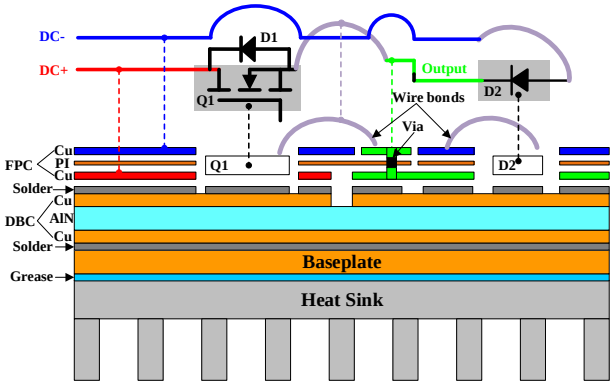


Figure 2.33: The DBC and FPC hybrid structure [48].

Table 2.2 summarized the features of different packaging schemes for SiC power modules. The clip-bond, flexible substrate, Cu connector, and Cu pin replaced conventional wire-bonding interconnect to reduce the parasitic inductance. Magnetic cancellation of the commutation loop could also reduce parasitic inductance. LTCC was used as an interposer. Ag NP sintering is a potential die-attach technology for the SiC power module.

Table 2.2: Summary of different packaging schemes for SiC power modules

Packaging scheme	**Features**
Miniaturized double-sided cooling [32]	1) Double-sided cooling with flip-chip and clip bonding; 2) Withstand high temperature over 220 °C; 3) 50% thermal resistance reduction is achieved compared with the conventional single-sided cooling type.
POL [33]-[34]	A flexible substrate replaces wire-bonds.
LTCC based double-sided cooling [35]	1) Double-sided cooling; 2) Double-sided Ag NP sintering; 3) LTCC-interposer is used as dielectric and chip carrier; 4) 59% thermal resistance reduction is realized; 5) 54~85% parasitic inductance reduction is observed.
6-in-1 [36]	1) Double-sided cooling; 2) Magnetic cancellation effect is used; 3) 70% voltage overshoot reduction is obtained.
PCoB [37]	1) Double-sided air-cooling; 2) Mo spacers are used as CTE buffer between die and bottom substrate for reducing stress; 3) 0.5 °C/W thermal resistance and 8 nH power loop parasitic inductance are achieved.
Press-pack package [38]	1) Double-sided cooling based on LTCC microchannel; 2) A miniature and flexible "fuzz buttons" in a low-profile LTCC interposer is used; 3) Commutation loop inductance is 4.3 nH at 100 kHz; 4) The junction-to-heatsink thermal resistance is about 0.2 K/W, and the heatsink to coolant thermal resistance is about 0.8 K/W.
Chip scale, flip-chip package [39]-[42]	1) Flip-chip solder ball array is used to make connections to the anode; 2) A Cu connector is used to contact the cathode; 3) 24% on-resistance reduction is observed.
Cu pin connection [43]-[44]	1) Cu pin replaces wire-bonds; 2) Si_3N_4 based DBC substrate is used; 3) 50% overall thermal resistance reduction is obtained compared to Al_2O_3 ceramic structure; 4) 57~87% power loss reduction is realized compared to Si-based wire-bonded package.
SKiN [45]-[46]	1) Sintering between FPC and SiC chip, SiC chip and DBC, DBC and heat sink; 2) Commutation parasitic inductance is less than 1.4 nH.
DBC and PCB hybrid structure [47]	1) Much more complicated routing can be achieved; 2) Ultra-low loop inductances can be realized.
DBC and FPC hybrid structure [48]	1) Cancellation of magnetic coupling effect is strong; 2) Parasitic inductance can be significantly minimized to only 0.79 nH by using thin FPC and proper layout design; 3) Compared with the commercial module, the voltage overshoot is decreased by about 50%; 4) 1/3 switching energies of the commercial module under the same decoupling capacitors and driving conditions.

2.3. SUMMARY

IN this chapter, to comprehensively investigate the packaging techniques for power modules, before the review of packaging techniques for SiC power modules, a survey of packaging schemes for Si-based power modules, which are representative and widely used power devices, was first performed. These packaging schemes are the foundation of the packaging schemes for SiC power modules. Then, several packaging schemes for SiC power modules were thoroughly overviewed. Although some similar packaging schemes for Si-based power modules have also been explored, requirements of parasitic inductance and heat dissipation for SiC power modules are demanding.

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3

SELECTION AND CHARACTERIZATION OF SiC MOSFET AND ORGANIC SUBSTRATE

In this chapter, SiC MOSFET (CPM2-1200-0080B) from CREE and organic substrate materials, including BT laminate (HL832NSF) and BT prepreg (GHPL-830NSF), from Mitsubishi Gas Chemical, were selected. I-V, C-V, and gate charge characteristics of the SiC MOSFET were first studied via a custom fixture. The experimental results showed that the SiC MOSFET had output characteristics of non-saturation, existed two distinct points in the curve of Miller capacitance versus drain-source voltage, and displayed a non-flat Miller platform. All of these are different from Si devices. Then, the thermal stability, dielectric breakdown, thermo-mechanical performance, and cure kinetics of the organic substrate materials were characterized. The experimental results indicated that the substrate materials could withstand the high temperature of 300 °C and the high voltage of 46.9 kV. The glass transition temperature was as high as over 260 °C, and the coefficient of thermal expansion was matching with SiC material. Both one-hour curing at 280 °C and two-hour at 210 °C could ensure the full cure of the BT prepreg.

Parts of this chapter have been published in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 6, pp. 1054-1061, 2019 [1].

3.1. Selection and characterization of SiC MOSFET

A SiC MOSFET is comprised of more than 10,000 small parallel-connected N-Channel enhancement mode MOSFET unit cells. Figure 3.1 illustrates the schematic of half SiC vertical diffused MOSFET (VDMOS) unit cell [2]-[3]. The SiC MOSFET device is fabricated by beginning with an N- drift layer grown on a heavy doped N+ substrate. To attain a high breakdown voltage, the drift layer is lightly doped. The breakdown voltage V_{BR} of SiC MOSFET is influenced by the doping concentration N_D of N- drift layer and the thickness w_B of N- drift layer, which can be expressed as [4]-[6].

$$N_D = \left(\frac{4.45\times10^{13}}{1.25V_{BR}}\right)^{3/4} \tag{3.1}$$

$$w_B = \sqrt{\frac{2\varepsilon_{sic}V_{BR}}{q_e N_D}} \tag{3.2}$$

where ε_{sic} is the buck electron mobility of SiC, and q_e is the electron charge.

The on-resistance R_{on} of SiC MOSFET consists of source contact, channel, junction gate field-effect transistor (JFET), spreading, drift layer, substrate, and backside drain resistances. For low-middle voltage SiC MOSFET, i.e., 900 and 1200 V ratings, the channel resistance is the dominant resistive component. However, as the voltage rating increases, the doping concentration of the drift layer decreases, and thickness increases, so drift layer resistance R_{drift} increases and becomes the dominant resistive component [7]. R_{drift} is given by Ref. [6] as expressed by

$$R_{drift} = \frac{w}{\varepsilon_{sic} q A_{GD} N_D} \tag{3.3}$$

$$w = w_B - w_{DSJ} \tag{3.4}$$

where A_{GD} is the gate-drain overlap area, w is the drain-source un-depleted drift width, and w_{DSJ} is the drain-source depletion width. According to Eq. (3.1) ~ (3.2), the breakdown voltage would be higher if increasing the drift layer and decreasing the doping level. On the contrary, according to Eq. (3.3) ~ (3.4), the drift layer resistance would be lower if decreasing the layer and increasing the doping level. Thus, a trade-off exists between breakdown voltage and drift layer resistance.

The high critical electric field of 4H-SiC (10 times greater than Si) allows SiC MOSFET with thinner (1/10 that of silicon devices) and more highly doped (10 times higher than silicon devices) drift layer. The combination of 1/10 of the drift layer thickness with the 10 times higher doping concentration can yield a lower on-resistance. It is typically a minimum of 10 times lower than for Si devices of the same blocking voltage [3], [8].

The drift layer is sandwiched between N+ substrate and p- body, creating a vertical body diode, as shown in Figure 3.1. The body diode is a PiN diode and is in anti-parallel with the SiC MOSFET channel. The foremost characteristic of the PiN diode is in the turn-off transient, where reverse recovery can be observed as a result of minority carrier extraction from the drift layer [8]-[9]. Body diode in the SiC MOSFET is utilized to replace external freewheeling diode in this work.

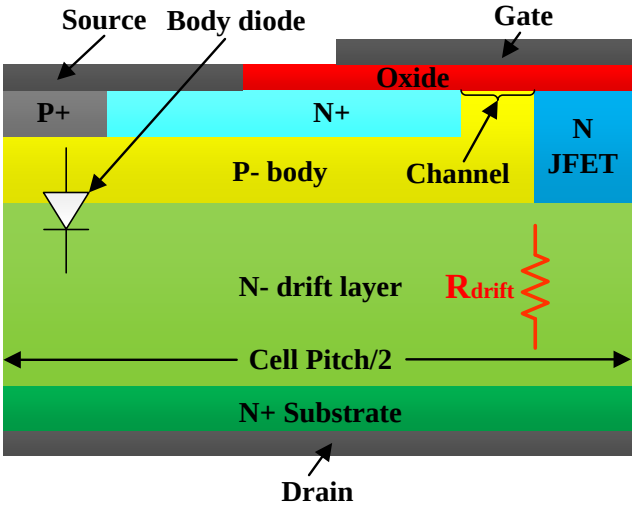


Figure 3.1: Schematic of half SiC VDMOS unit cell [2].

Figure 3.2 and 3.3 show the half unit cell with equivalent parasitic capacitances and equivalent circuit model of the SiC MOSFET, respectively. A real SiC power MOSFET is composed of an ideal MOSFET that can be described as a voltage-controlled current source, three internal parasitic capacitances, and an anti-parallel body diode. The internal parasitic capacitances of SiC MOSFET include gate-source capacitance (C_{GS}), drain-source capacitance (C_{DS}), and gate-drain capacitance (Miller capacitance, C_{GD}), which are related to its input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitances as [2], [10]-[11]:

$$C_{GS} = C_{ISS} - C_{GD} \tag{3.5}$$

$$C_{DS} = C_{OSS} - C_{GD} \tag{3.6}$$

$$C_{GD} = C_{RSS}. \tag{3.7}$$

C_{GS} consists of a constant overlap oxide capacitance between the gate and the source and a constant capacitance between the gate and the source metallization, which are in parallel. C_{DS} is the bias-dependent depletion capacitance of P-body/N-drift junction and is given by

$$C_{DS} = C_{DS0}\left(\frac{V_{bi}}{V_{bi} + V_{DS}}\right)^{M} \tag{3.8}$$

where C_{DS0} is a constant, V_{bi} is the built-in potential between the P-body and the N-drift junction, V_{DS} is the drain-source voltage, and M is a fitting parameter. C_{GD} is the most

important and complicated parasitic capacitance in SiC MOSFET, it provides a feedback loop between the output and the input of MOSFET. As shown in Figure 3.3, it is composed of a constant gate oxide capacitance C_{OX} and a nonlinear depletion capacitance C_{GDJ}. They can be expressed as Eq. (3.9) and Eq. (3.10), respectively [10].

$$C_{OX} = \frac{A_{GD}\varepsilon_{sic}}{t_{OX}} \tag{3.9}$$

$$C_{GDJ} = \frac{A_{GD}\varepsilon_{sic}}{t_{GDJ}} \tag{3.10}$$

$$t_{GDJ} = \sqrt{\frac{2\varepsilon_{sic}(V_{DS}+V_T)}{q_e N_D}} \tag{3.11}$$

where t_{OX} is the gate oxide thickness, t_{GDJ} is the depletion thickness between gate and drain, N_D is the doping concentration, and V_T is the gate-drain overlap depletion threshold.

When V_{DS} is less than $V_{GS}-V_T$, C_{GD} is equal to the gate oxide capacitance C_{OX}. While for V_{DS} greater than $V_{GS}-V_T$, C_{GD} is equal to the series combination of C_{OX} and C_{GDJ}. It can be given by

$$C_{GD} = \begin{cases} C_{OX} & V_{DS} \le U_{VR} < V_{GS}-V_T \\ C_{OX}C_{GDJ}/(C_{OX}+C_{GDJ}) & V_{DS} > V_{GS}-V_T. \end{cases} \tag{3.12}$$

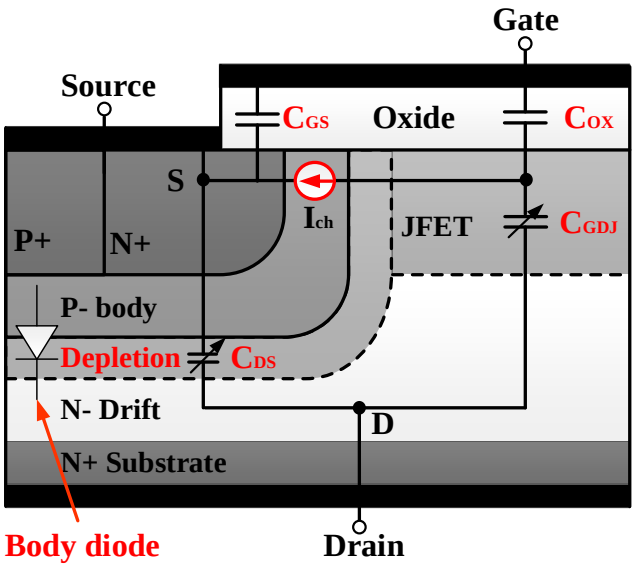


Figure 3.2: Half SiC MOSFET unit cell with equivalent parasitic capacitances.

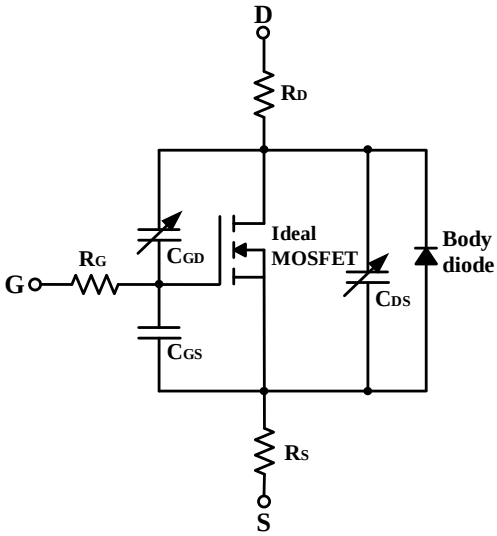
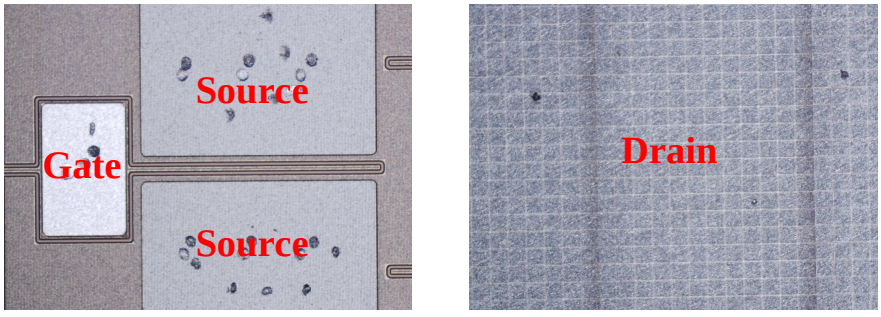


Figure 3.3: Equivalent circuit model of a SiC MOSFET.

3.1.1. Selection of SiC MOSFET

The SiC MOSFET (CPM2-1200-0080B) from CREE is selected. The drain-source breakdown voltage is 1200 V, the continuous current at 25 °C is 36 A, the specific on-resistance is 80 mΩ, and the size is 3.10×3.36×0.186 mm^3. The front-side and backside of the bare die are shown in Figure 3.4(a) and (b), respectively. The backside drain metallization is Ni (0.8 μm) and Ag (0.6 μm) and front-side source and gate metallization are Al with 4 μm thickness.



(a) Front-side (b) Bottom side

Figure 3.4: Local photos of CPM2-1200-0080B.

3.1.2. Experimental approach

Static characteristics of SiC MOSFET bare die were measured using Power Device Analyzer (Keysight B1505A), which equipped with several fixtures for wafer- and package-level measurements, mainly for wafer-level bare-die and standard discrete devices. Single bare dies and novel packaging structures can not be directly measured. In this chapter, to analyze the static characteristics of the SiC MOSFET at any operational condition, a new custom fixture for static characterization of CPM2-1200-0080B was developed, as shown in Figure 3.5. The bare die was flipped and positioned in a small cavity and covered by a cover plate so that electrical interconnection between the bare die and the external circuitry could be realized via probes on the cavity and cover plate. The current limiting was set to 20 A, in case the excessive current damaged the devices or probes.

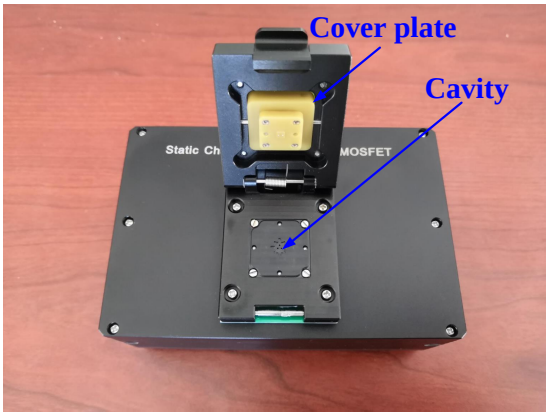


Figure 3.5: Custom fixture for static characterization of SiC MOSFET.

3.1.3. Experimental results

(1) I-V characterization

Figure 3.6 shows the test circuit for I-V characteristics of SiC MOSFET bare die. The gate and drain of SiC MOSFET were connected to its source through two voltage sources. The drain-source voltage V_{DS} was swept from 0 to 4 V under the gate-source voltage V_{GS} from 10 to 20 V in steps of 2 V.

Figure 3.7 shows the I-V characteristics of SiC MOSFET. There was no evident boundary between the linear region and the saturation region of SiC MOSFET. As V_{DS} increased, I_D did not have the trend of saturation. As V_{GS} increased, the non-saturation characteristics of SiC MOSFET became more evident, and the I-V characteristics of SiC MOSFET got closer and closer, which indicated that SiC MOSFET was changing from ON- to fully-ON state.

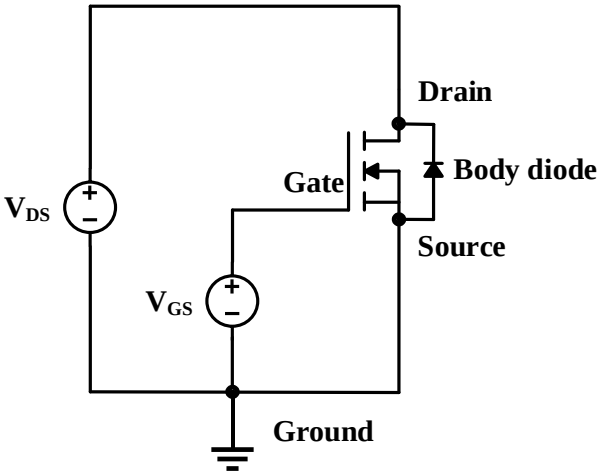


Figure 3.6: Test circuit for I-V characteristics of SiC MOSFET.

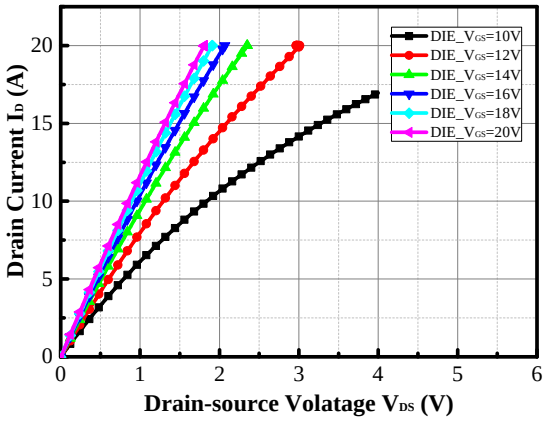


Figure 3.7: I-V characteristics of SiC MOSFET.

(2) C-V characterization

Figure 3.8 shows the test circuit for C-V characteristics of SiC MOSFET. The gate was short-connected to its source. The drain was connected to its source through one DC voltage source. The drain-source voltage V_{DS} was swept from 0 to 200 V. Three AC small signals were adopted to test the input, output, and output capacitances, respectively. The frequency is 100 kHz.

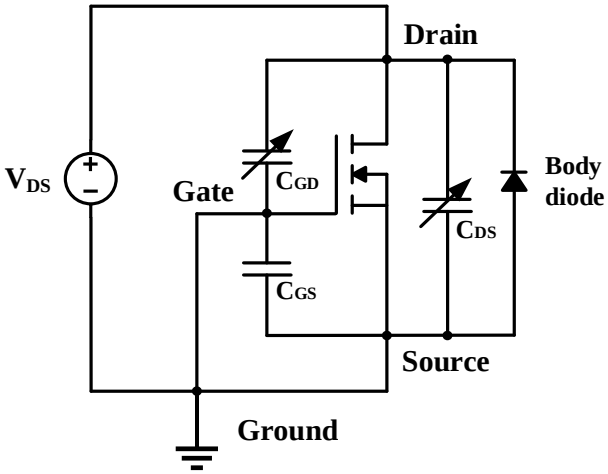


Figure 3.8: Test circuit for C-V characteristics of SiC MOSFET.

Figure 3.9 shows the input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitances of the SiC MOSFET. C_{RSS} had two distinct inflection points when V_{DS} was below about 12 V, which was different from the Si devices.

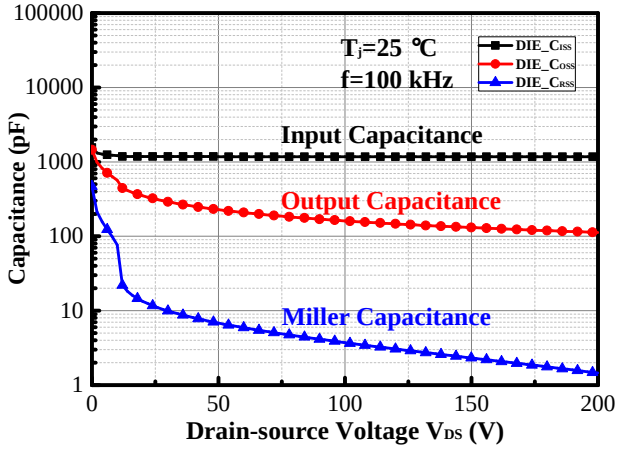


Figure 3.9: Input, output, and reverse capacitances of SiC MOSFET.

As V_{DS} increases, the depletion layer will expand into the JFET, N- drift, and N+ substrate [10], as shown in Figure 3.10. According to Eq. (3.10), C_{GDJ} drops gradually. How-

ever, because N_D at different regions are different, the expansion rates of the depletion layer at the three regions are different, and thus decay rates of C_{GDJ} are also different.

When V_{DS} is lower, the depletion layer expands to the JFET region, as shown in Figure 3.10(a). The decay rate of C_{GDJ} is slower as a result of the high N_D. When the depletion layer expands to the N- drift layer, as illustrated in Figure 3.10(b), the decay rate of C_{GDJ} is faster due to the low N_D. The voltage at which the depletion layer expands to the interface between the JFET region and the drift layer is called as JFET pinch-off voltage or transition voltage due to the different doping concentrations of the two regions. When the depletion layer expands to the N+ substrate, as depicted in Figure 3.10(c), C_{GD} slowly decreases with V_{DS}. At OFF-state, the depletion layer is the thickest, and the C_{GDJ} is the smallest and far less than C_{OX}, and the Miller capacitance C_{GD} is equal to C_{GDJ}.

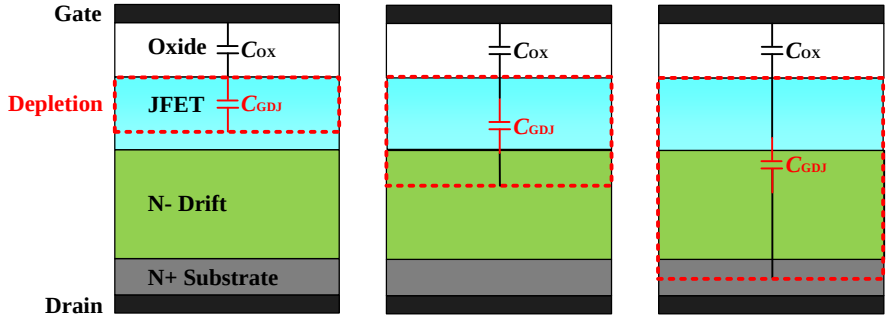


Figure 3.10: Expansion region of depletion layer: (a) JFET; (b) N- drift layer; (c) N+ substrate.

(2) Gate charge characterization

Compared with Si counterparts, SiC MOSFET has much lower output capacitance and gate charge, and they can be switched at much higher *dv/dt* and *di/dt*. High switching speed enables low switching loss and high switching frequency, which can improve the power density and efficiency of power module [12].

Gate charge (Qg) is the total amount of charge to turn on/off a power device. It is one of the critical parameters of MOSFETs and IGBTs [13], and especially crucial for high-frequency WBG devices, such as SiC MOSFET and GaN high-electron-mobility transistor. It can be used to assess the switching performance, e.g., the gate driving loss, the switching time, and the Miller capacitance.

The test circuits with a constant current source, or a resistive load, or an inductive load are often seen in a datasheet to measure Qg. These conventional measurement methods require power suppliers that can simultaneously deliver high-voltage and high-current. The test cost and operational risk are relatively high. Furthermore, when high-voltage and high-current are applied to the device under test (DUT) simultaneously, the power dissipation is enormous [13]. In this work, a high-voltage / low-current measurement and a high-current / low-voltage measurement were performed in turn. Figure 3.11(a) and (b) shows the test

circuits. Different from the former, the high-current measurement circuit is a phase-leg configuration. High-side is a constant current load. A TO-247 discrete device of Si IGBT with the same power rating, which could provide the constant current when it reached to the saturated state, was used in this experiment.

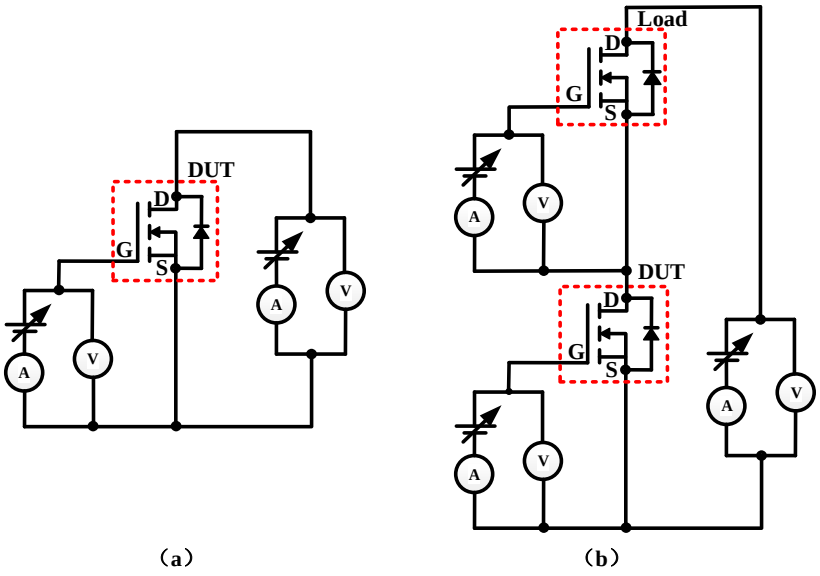


Figure 3.11: Test circuits for gate charge: (a) High-voltage measurement; (b) High-current measurement.

The high-voltage measurement was performed at the OFF-state, while the high-current measurement was conducted from the initial OFF-state to fully ON-state. The two Qg curves were then merged to form a total Qg curve.

Figure 3.12 shows the Qg of SiC MOSFET under the drain-source voltage of 600 V. As shown in the figure, the Qg curve consists of three segments with different slopes. In the first segment, C_{ISS} was charged by gate current I_G from OFF-state, because C_{GS} is much larger than C_{GD}, Qg in the segment is named as Q_{GS}. V_{GS} in the segment was increased linearly until I_D of SiC MOSFET reached the load current of 20 A. Different from IGBT, I_D of SiC MOSFET in the saturation region increases with V_{DS} due to the short-channel effect and modest transconductance [14]-[15]. In the second segment, SiC MOSFET was changing from On- to fully ON-state. Because I_G flew into C_{RSS} and I_D didn't saturate, V_{GS} still increased, which was different with Si device, Qg in the segment is called as Q_{GD}. In the last segment, the SiC MOSFET was fully turned on.

As indicated in the figure, under the same drain-source voltage of 600 V, I_D of DUT increased quickly with V_{GS}. Once I_D reached the load current, it would stop increasing and keep the value, and V_{DS} began to decrease. With the decline of V_{DS}, V_{GS} still increased due to the unsaturation of I_D. Therefore, from ON- to fully ON-state, the Miller plateau of SiC MOSFET was non-flat.

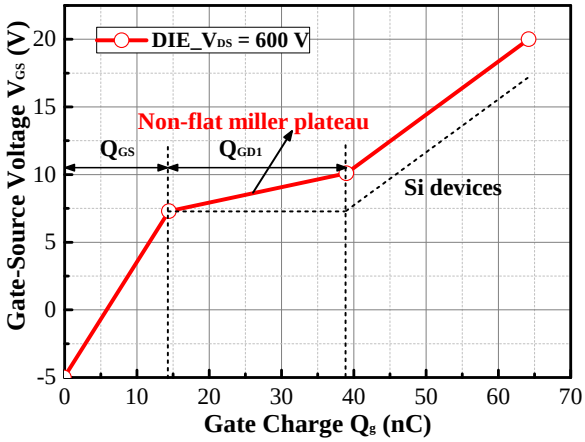


Figure 3.12: Gate charge of SiC MOSFET under the drain-source voltage of 600 V.

3.2. SELECTION AND CHARACTERIZATION OF ORGANIC SUBSTRATE

3.2.1. SELECTION OF ORGANIC SUBSTRATE MATERIALS

(1) Selection criteria

- High-temperature stability

SiC MOSFET can operate at high temperatures over 200 °C. Accordingly, the selective organic substrate materials should withstand the high temperatures over 200 °C to fulfill the high-temperature advantage of SiC MOSFET.

- High dielectric breakdown strength

SiC MOSFETs of 1.2 kV are positioned in the chip windows of BT (bismaleimide triazine) core with the almost identical thickness, so the BT core must withstand the voltage over 1.2 kV to keep the laminated substrate from being broken down. BT core of specific thickness can be formed by laminating BT laminate, prepreg, and Cu foil under high-temperature and high-pressure conditions. The dielectric breakdown strength E is defined as:

$$E = \frac{V_{\mathrm{BD}}}{d} \tag{3.13}$$

where V_{BD} is the dielectric breakdown voltage, and d is the thickness of material.

Figure 3.13 shows the electric field distribution of the laminated substrate when the drain-source voltage of high-side SiC MOSFET is 1.2 kV. The maximum electric field strength is 8.56×10^5 V/m. And accordingly, the dielectric breakdown strength of the laminated substrate must be much higher than 8.56×10^5 V/m.

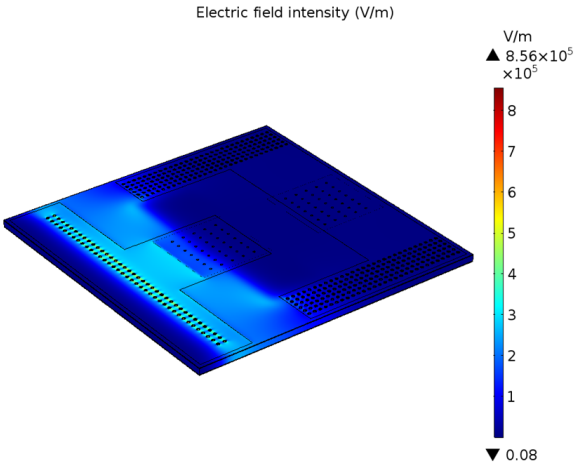


Figure 3.13: Electric field distribution of laminated substrate.

- High glass transition temperature (Tg)

As viscoelastic materials, thermo-mechanical properties of the organic substrate materials will change significantly below and above Tg, storage modulus decreases dramatically, and CTE increases evidently. Therefore, choosing materials with high Tg can improve thermo-mechanical reliability of the package.

- CTE matching with SiC

Material CTE mismatch within the SiC power module could induce excessive stress when subjected to temperature change and constraint, leading to package failure. The thermally-induced stress at the interface of two materials can be described by Eq. (3.14).

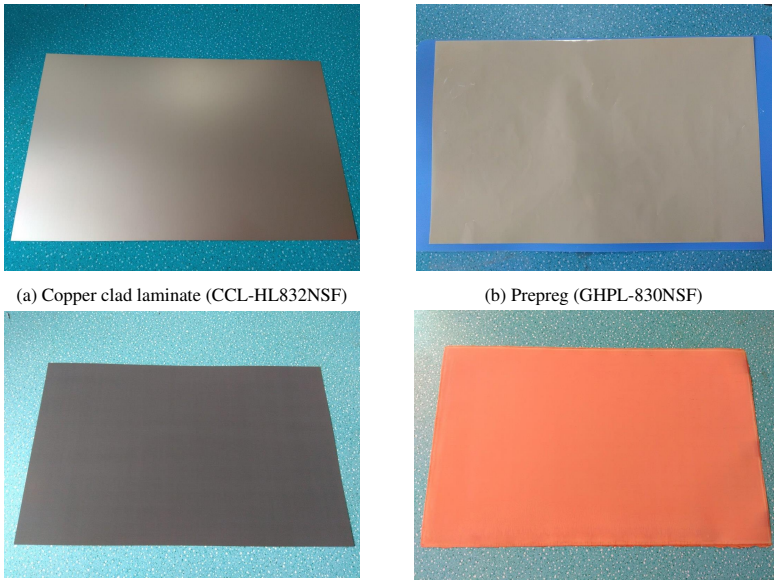
$$\sigma_T = \int_{T1}^{T2} \frac{\alpha_A(T) - \alpha_B(T)}{[\frac{1}{E_A} + \frac{1}{E_B}](1-\mu_A)} dT \tag{3.14}$$

where α_A, α_B, E_A, E_B are the CTE and Young's modulus of materials A and B. μ_A is the Poisson's ratio of material A. If α_A (T)- α_B (T) is approximately zero, there will induce a tiny stress.

(2) Material selection

The organic substrate materials adopted in the SiC power module packaging process are copper clad laminate (CCL-HL832NSF) and prepreg (GHPL-830NSF) from Mitsubishi Gas Chemical. CCL-HL832NSF is a double-sided copper-clad BT laminate (E-glass fiber-reinforced BT resin), as shown in Figure 3.14(a). Figure 3.14(b) is a sheet of BT prepreg (E-glass fiber-reinforced uncured BT resin). To analyze and compare the properties of the laminate and the prepreg comprehensively, double-sided copper of CCL is etched, as shown

in Figure 3.14(c). Cured prepreg, with the same thickness as BT laminate, consists of two layers of BT prepregs through high-temperature and high-pressure laminating process, as illustrated in Figure 3.14(d). BT laminate is commonly used as a substrate core material in microelectronic packaging [16]. In this work, SiC MOSFETs were placed in the chip windows of a BT core with almost the same size as them. The BT core could be laminated by BT laminate, BT prepreg, and Cu foil through high-temperature and high-pressure laminating process.



(a) Copper clad laminate (CCL-HL832NSF)

(b) Prepreg (GHPL-830NSF)

(c) Laminate

(d) Cured prepreg

Figure 3.14: Organic substrate materials.

3.2.2. EXPERIMENTAL APPROACH

Firstly, dynamic and isothermal thermal gravimetric experiments were performed using TGA (Thermal Gravimetric Analyzer) under the nitrogen atmosphere to investigate the thermal stability of the organic substrate materials.

Secondly, the thermo-mechanical performance of the organic substrate materials was analyzed and compared using the film/fiber tensile clamp in TMA (Thermal Mechanical Analyzer) under the nitrogen atmosphere. Tg and CTE of the organic substrate materials were analyzed.

Thirdly, the breakdown voltage of the BT laminate was characterized through a withstanding voltage tester. Weibull statistical distribution was adopted to analyze the dielectric breakdown strength. The breakdown voltage of the laminated substrate was evaluated to ensure that it could withstand the maximum drain-source voltage of SiC MOSFET.

Lastly, dynamic and isothermal cure kinetics experiments of BT prepreg were conducted using DSC (Differential Scanning Calorimetry) under the nitrogen atmosphere. The

effects of ramp rate, curing temperature, and curing time on the degree of cure of the BT prepreg were analyzed to provide guidelines for high-temperature and high-pressure laminating process.

3.2.3. Experimental results

(1) Thermal stability

TGA is used to measure weight gain or loss of the material as a function of time, temperature, and environmental factors. Most of the changes in the properties can be traced back to the loss of weight [17]. In this experiment, first of all, thermal stabilities of BT laminate and cured prepreg were compared at a ramp rate of 10 °C/min. Then, both dynamic and isothermal TGA experiments were performed to investigate the BT laminate's thermal stability. Dynamic TGA is used to determine the degradation temperature, while isothermal TGA is to determine the decomposition temperature [17].

- Thermal stability comparison between the BT laminate and the cured prepreg

Figure 3.15 compares the thermal stability between the BT laminate and the cured prepreg. It can be seen that the two materials showed similar weight loss rate from room temperature to 400 °C. The two materials were very stable below 300 °C. The weight-loss rates of the two materials began to increase as the temperature continued to rise. When temperature scaled from 400 to 600 °C, weight loss rates of two materials started to deviate from each other. Therefore, the organic substrate materials were considered as stable when the temperature was below 300 °C.

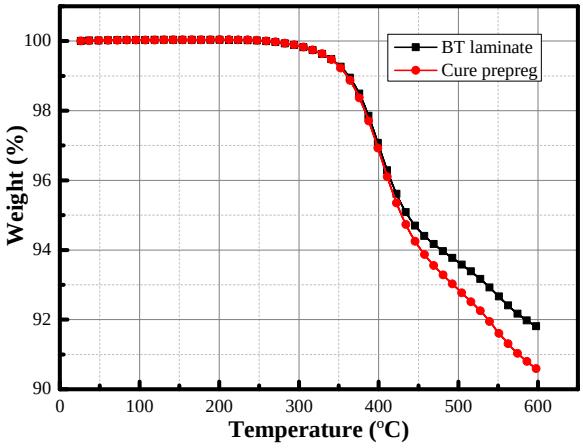


Figure 3.15: Comparison of high-temperature stability between the BT laminate and the cured prepreg.

- Dynamic thermal gravimetric analysis of BT laminate

Dynamic TGA was performed by heating the BT laminate until 800 °C through different ramp rates of 5, 15, and 30 °C/min, as depicted in Figure 3.16. The extrapolated onset temperature that denotes the degradation temperature at which the weight loss begins can be calculated. Onset temperature is a reproducible temperature calculation, specified to be used by ASTM and ISO [18]. The onset temperature of the laminate rose as ramp rate increased. When the ramp rate increased to 30 °C/min, the onset temperature of the laminate reached up to 381 °C. Therefore, increasing the ramp rate could decrease the degradation of the material.

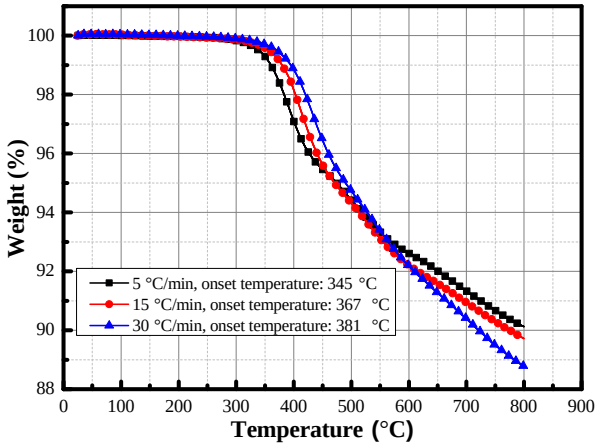


Figure 3.16: Dynamic thermal gravimetric analysis of the laminate material.

- Isothermal thermal gravimetric analysis of BT laminate

The BT laminate was first heated up to an isothermal temperature from room temperature at a high ramp rate of 100 °C/min to avoid any dissipation of heat during heating and then executed at 300, 350, 400, 450, and 500 °C for one hour, respectively.

Figure 3.17 shows weight losses of the laminate under different isothermal TGA experiments. The weight loss mainly occurred in the temperature rising process and the initial phase of the isothermal process. As holding time went on, little weight loss occurred, so only one-hour isothermal holding time was adopted. When the laminate material was subjected to the temperature of 300 °C for one hour, a slight weight loss was observed, which could be attributed to the outgassing of solvents. However, when the temperature ramped up to 350 °C and isothermally heated for one hour, decomposition of the laminate material became evident, and about 2% of the weight was lost. Therefore, the laminate was thermally stable under the high temperature of 300 °C. The organic substrate materials were suitable for SiC power module in high-temperature applications over 200 °C.

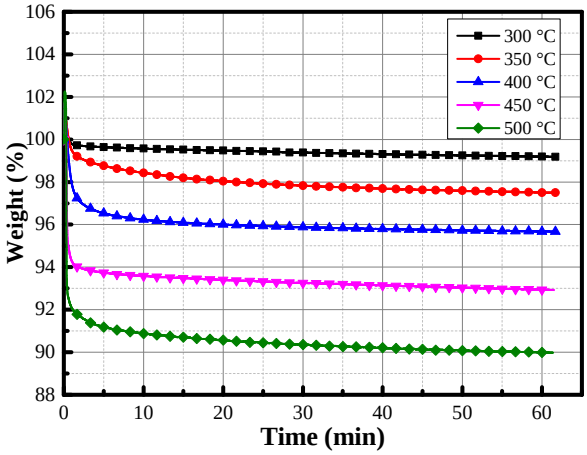


Figure 3.17: Isothermal thermal gravimetric analysis of the laminate material.

(2) Dielectric breakdown strength of the BT laminate

In this section, BT laminate's breakdown voltage was characterized by a withstanding voltage tester, whose highest voltage is 20 kV. To be able to observe the broken down phenomenon, a BT laminate of 60 μm was selected. A series of voltage breakdown experiments were performed. Weibull statistical distribution was adopted to analyze the breakdown behavior of the BT laminate. The cumulative distribution function for two-parameter Weibull distribution is expressed as:

$$P(\mathrm{E}) = 1 - \exp[1 - (\frac{E}{\mathrm{E_0}})^{\beta}] \tag{3.15}$$

where $P(\mathrm{E})$ is the cumulative probability, E_0 is the scale parameter representing the value of E corresponding to a cumulative probability of 63.2%, and β is the shape parameter which is the slope of the straight line of Weibull plot [19].

This equation can be rewritten as follows:

$$\log(\ln \frac{1}{1-P}) = \beta \log \mathrm{E} - \beta \log \mathrm{E_0}. \tag{3.16}$$

Assume that:

$$x = \log E \tag{3.17}$$

$$y = \log(\ln \frac{1}{1-P}). \tag{3.18}$$

Then, y is a linear function of x, can be expressed as:

$$y = \beta x - \beta \log E_0. \tag{3.19}$$

Figure 3.18 shows the Weibull plot of dielectric strength of BT laminate. From the figure, it can be seen that the fit linear function is

$$y = 5.37x - 12.9. \tag{3.20}$$

From Eq. (3.19), it can be calculated that the dielectric strength of the BT laminate is about 252 kV/mm. For the BT core of 186 μm, its breakdown voltage can reach as high as about 46.9 kV, which is much higher than drain-source voltage of 1.2 kV. And therefore, the BT core can withstand the high voltage of 46.9 kV.

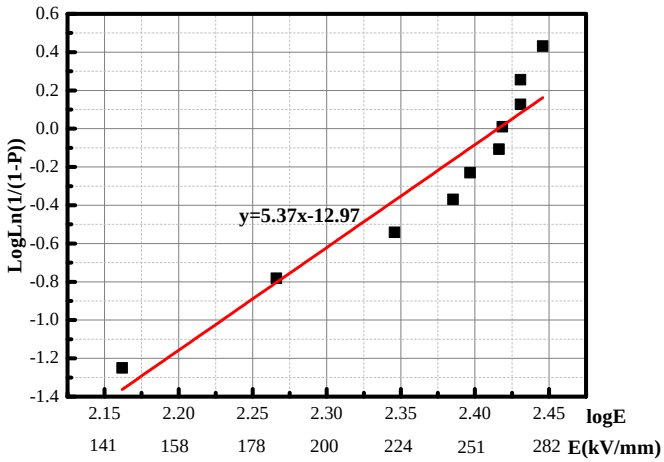


Figure 3.18: Weibull plot of dielectric strength of the BT laminate.

(3) Thermo-mechanical performance

CTE and Tg of the organic substrate materials are two crucial factors that can determine materials' thermo-mechanical performance. In the extreme environment, CTE mismatch between the organic substrate materials and the SiC dies could lead to package failure, e.g., die crack and interface delamination. CTE of the organic substrate materials changes significantly below and above Tg. In this section, Tg and CTE of the BT laminate and cured prepreg were first analyzed. They were heated separately from 25 to 330 °C at a ramp rate of 5 °C/min. The effect of the ramp rate on the in-plane CTE of the cured prepreg was then investigated. The ramp rate was increased from 5 to 25 °C/min.

- Thermo-mechanical comparison between the BT laminate and the cured prepreg

Figure 3.19 compares the Tg and in-plane CTE between cured prepreg and BT laminate. As can be concluded from the result, the two materials had a similar thermo-mechanical performance. Tg of the two materials was about 262~265 °C, which was much higher than those of other organic substrate materials. A common one, such as FR4 prepreg, Tg is usually around 150 °C. In-plane CTEs of the two materials above Tg were lower than those below Tg. When the temperature was below Tg, in-plane CTEs of the two materials were about 5~7 ppm/°C. When the temperature was above Tg, in-plane CTEs of the two materials were about 3 ppm/°C. Because the cured prepreg was made of two layers of BT prepregs through high-temperature and high-pressure laminating process and contains two layers of glass fibers, while BT laminate had only one layer of glass fiber, CTE of the cured prepreg was slightly bigger than that of the laminate. Thus, the organic substrate materials had Tg as high as over 260 °C, and CTE as low as 5.3 ppm/°C.

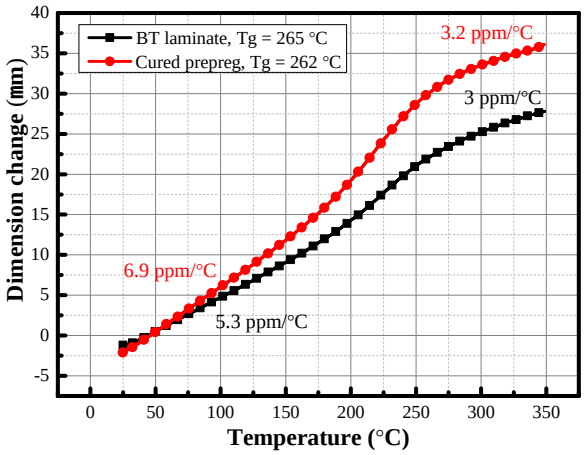


Figure 3.19: Comparison of Tg and in-plane CTE between cured prepreg and BT laminate.

- Effect of ramp rate on the thermo-mechanical performance of the cured prepreg

Figure 3.20 depicts the effect of ramp rate on the thermo-mechanical performance of the cured prepreg. As the ramp rate increased, Tg of the cured prepreg rose, while CTE of the cured prepreg decreased. When ramp rate increased to 25 °C/min, Tg of the cured prepreg reached 273 °C, while CTE below Tg decreased to 5.5 ppm/ °C, which was approaching CTEs of BT laminate and 4H-SiC. Therefore, from the thermo-mechanical performance point of view, the BT laminate and BT prepreg were ideal packaging materials for the SiC power module.

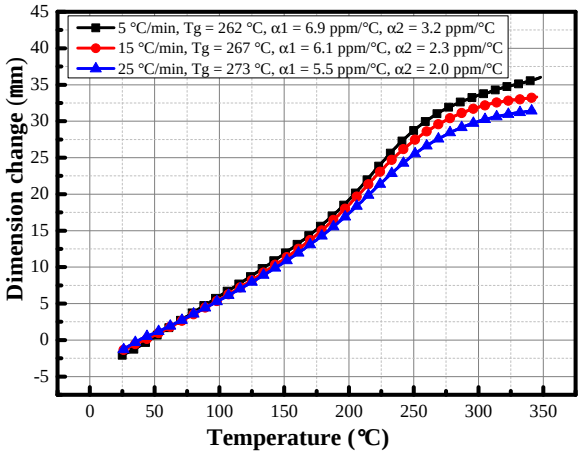


Figure 3.20: Effect of ramp rate on the in-plane CTE and Tg of the cured prepreg.

(4) Cure kinetics of BT prepreg

Both dynamic and isothermal DSC experiments were performed to reveal BT prepreg's degree of cure to provide one guideline for BT core high-temperature and high-pressure laminating process. Effects of ramp rate, curing temperature, and curing time on the degree of cure of the BT prepreg were analyzed, respectively, and an optimal curing schedule of the prepreg was suggested.

DSC measures the quantitative difference of temperature and heat flow as a function of time and temperature between the target and reference materials when heat evolves from the chemical reaction within the target material. As a guideline, the upper temperature limit of the DSC experiment should not exceed a temperature of 2% weight loss due to decomposition. Based on the above analysis results through TGA, when the heating rate was 5 °C/min, the temperature of 2% weight loss was about 383 °C. In this section, the upper temperature of the dynamic DSC experiment was set to be 330 °C.

- Effect of ramp rate on the degree of cure of BT prepreg

Curing or cross-linking of a BT prepreg is an exothermic reaction, while the melting of a BT resin is an endothermic reaction. Twice dynamic DSC experiments from room temperature to 330 °C were performed to study the effect of ramp rate on the degree of cure of BT prepreg. Figure 3.21 shows the first dynamic DSC scan of the prepreg at the ramp rates of 5, 10, and 20 °C/min. There was an endothermic peak and an exothermic peak when BT prepreg was heating at a ramp rate. There was an endothermic peak at about 50 °C, indicating BT resin inside the prepreg began to melt. When the temperature rose to about 150 °C, heat flow began to increase, revealing that the prepreg started curing. As

the temperature continued to rise, an exothermic peak appeared, at which point the released heat in the cross-link reaction of prepreg was the most. The exotherm's magnitude increased as the ramp rate increased from 5 to 20 °C/min. The peak temperature shifted to a higher temperature range with an increase of ramp rate.

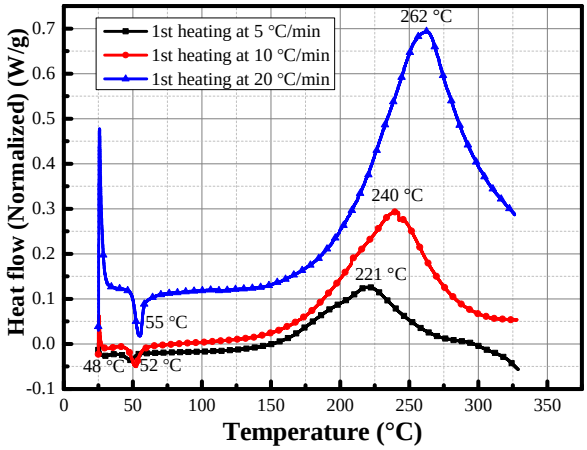


Figure 3.21: First dynamic DSC scan of the prepreg at different ramp rates.

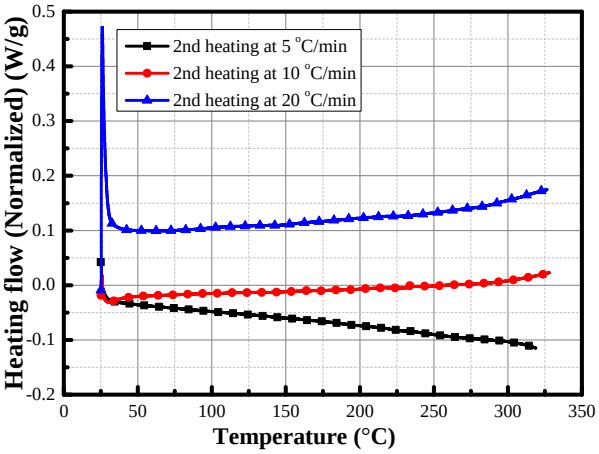


Figure 3.22: Second dynamic DSC scan of the prepreg at different ramp rates.

The second dynamic DSC scans were performed at the same ramp rate as the first scanned to examine the degree of cure of the prepreg, as illustrated in Figure 3.22. When

the ramp rate was 5 °C/min, exothermic did not exist, indicating that the prepreg was fully cured after the first dynamic DSC scan at the heating rate of 5 °C/min. However, when the ramp rate increased to above 10 °C/min, there was still exothermic, suggesting that the cross-linking reaction of the prepreg was ongoing as the temperature rose. Therefore, lowering the ramp rate could improve the degree of cure of the prepreg.

- Effect of the curing temperature on the degree of cure of the BT prepreg

The prepreg was first heated up to an isothermal curing temperature from room temperature at a high heating rate of 100 °C/min to avoid any dissipation of heat during the heating process, and then isothermally heating for one hour through DSC. Then, the prepreg was cooled down from the isothermal temperature to 25 °C with the same high cooling rate of 100 °C/min to prevent any dissipation of heat during the cooling process, and then dynamic heating experiments at a heating rate of 10 °C/min from room temperature to 330 °C were conducted to verify the degree of cure of the prepreg.

Figure 3.23 displays the dynamic DSC scans of the prepreg that have been isothermally for one hour at the curing temperature of 200, 220, 240, 260, and 280 °C. As expected, residual heat released by the cross-linking reaction of prepreg decreased with increasing curing temperature. When curing temperature ramped up to 280 °C, after isothermally heating one hour, there was neither exothermic peak nor endothermic peak, and the prepreg was fully cured. Therefore, when curing time remained constant, increasing isothermally curing temperature could improve the BT prepreg's degree of cure. When curing time was one hour, a curing temperature of 280 °C could ensure the full cure of the BT prepreg.

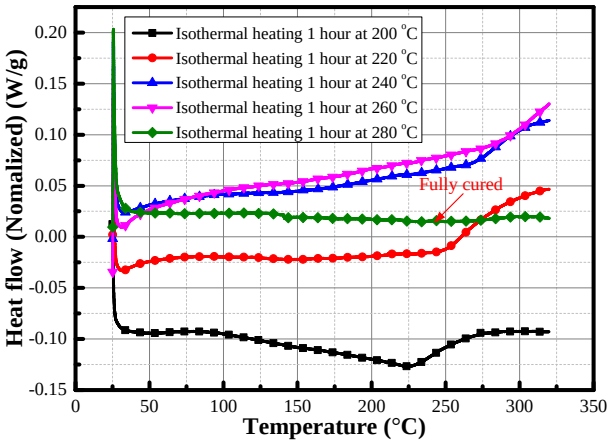


Figure 3.23: Effect of the curing temperature on degree of the cure of the BT prepreg.

- Effects of the curing time on the degree of cure of the BT prepreg

The DSC cell was heated up to 210 °C at 100 °C/min and then isothermally kept the temperature for various time intervals ranging from 30 minutes to two hours. Following this scan, the DSC cell was immediately cooled down to 25 °C at the same ramp rate and then heated up to 330 °C at 10 °C/min to verify the degree of cure of the prepreg.

Figure 3.24 illustrates the dynamic DSC scans of the prepreg that have been isothermally for various curing time at 210 °C. When curing time was below 90 minutes under the curing temperature of 210 °C, there still existed residual cure. After ramping up to about 230 °C, as the temperature continued to rise, uncured prepreg would be fully cured. However, when heating two hours, there was neither exothermic nor endothermic peak, and the prepreg was entirely cured. Therefore, when the curing temperature remained constant, increasing curing time could improve the BT prepreg's degree of cure. When curing temperature was 210 °C, the curing time of two hours could ensure the full cure of the BT prepreg.

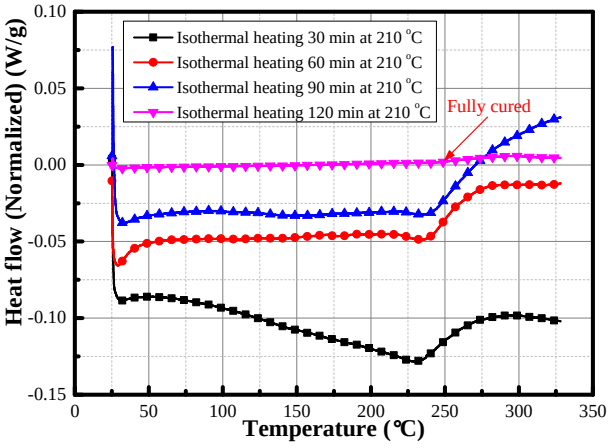


Figure 3.24: Effect of the curing time on the degree of cure of the BT prepreg.

3.3. Summary

In this chapter, SiC MOSFET and organic substrate materials were selected. I-V, C-V, and gate charge characteristics of the SiC MOSFET were first analyzed via a custom fixture. The results showed that compared with Si devices, SiC MOSFET had output characteristics of non-saturation, existed two distinct points in the curve of Miller capacitance versus drain-source voltage, and showed a non-flat Miller platform. Then, thermal stability, dielectric breakdown, and thermo-mechanical performance of the organic substrate materials and cure kinetics of BT prepreg were characterized. The results indicated that the substrate materials could withstand the high temperature of 300 °C and the high voltage of 46.9 kV. Tg was as high as over 260 °C, and CTE was matching with SiC. Both one-hour curing at 280 °C and two-hour at 210 °C could ensure the full cure of the BT prepreg.

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4

FAN-OUT SIC MOSFET POWER MODULE IN AN ORGANIC SUBSTRATE

In this chapter, a novel fan-out panel-level packaging technology was proposed for a phase-leg SiC MOSFET power module. The high- and low-side SiC MOSFETs were embedded in an organic substrate, interconnected by double-sided redistribution layers (RDLs) and through vias, finally protected by double-sided soldermasks. Compared with current embedded packaging for Si and GaN devices, the proposed packaging structure has unique merits, such as structure symmetry and double-sided cooling. Then, the electrical, thermal, and thermal-mechanical simulations were conducted to evaluate and optimize the fan-out packaging performance. Lastly, a detailed fan-out panel-level packaging process for the phase-leg SiC MOSFET power module was introduced. Three essential packaging processes, including exposure and development of photo imageable dielectric, panel-level physical vapor deposition (PVD), and double-sided RDL interconnection, could replace conventional laser drilling, chip/wafer-level PVD, and wire-bonding, respectively.

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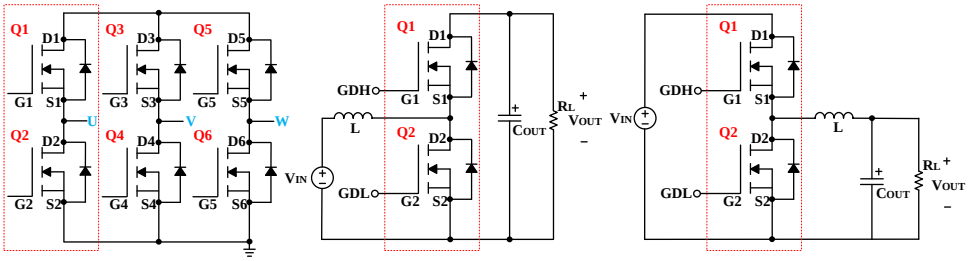
4.1. Phase-leg SiC MOSFET power module

A phase-leg is a building block for various converters and inverters in power electronic systems, as shown in Figure 4.1. It is a one-leg in a 3-phase inverter and can replace the transistor and diode in boost and buck converters. In this work, a phase-leg SiC MOSFET power module was designed, simulated, and packaged.

Figure 4.2 shows the circuit diagram of the phase-leg SiC MOSFET power module. The phase-leg power module consists of a high-side SiC MOSFET (HS-MOS) and a low-side SiC MOSFET (LS-MOS). Body diode in the SiC MOSFET can be utilized to replace the external freewheeling diode. Compared with Si counterparts, SiC MOSFET has a shorter lifetime of minority carriers so that not a sizeable reverse recovery current is estimated, which enables the body diode of SiC MOSFET to be a brilliant diode with almost no reverse recovery charge and forward recovery voltage [2].



(a) 3-phase inverter **(b)** Boost converter **(c)** Buck converter

Figure 4.1: Application of a phase-leg (inside red dashed line) in the inverter and converter.

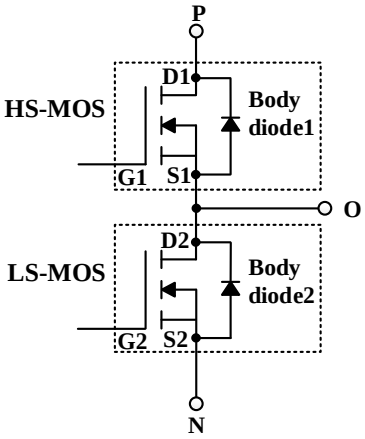


Figure 4.2: Circuit diagram of the phase-leg SiC MOSFET power module.

4.2. FAN-OUT SIC MOSFET POWER MODULE PACKAGING

4.2.1. PACKAGING STRUCTURE DESIGN

Figure 4.3 shows the schematic of a fan-out phase-leg SiC MOSFET power module in an organic substrate. The HS-MOS and LS-MOS in the phase-leg are positioned in the chip windows of BT core with the same thickness and covered by top- and bottom-layer photo imageable dielectrics (PIDs). Both through holes in the BT core and gaps between SiC MOSFETs and BT core are filled with PID. Both the front-side source and gate pads and bottom-side drain pads are extended beyond (fan-out) the chip edges through blind vias and RDLs. The electrical interconnections between HS-MOS and LS-MOS, chip and lead, are realized by blind vias, through holes, and inner and outer RDLs. Finally, the assembly is protected by top- and bottom-layer soldermasks. Table 4.1 lists the size of each component in the fan-out packaging.

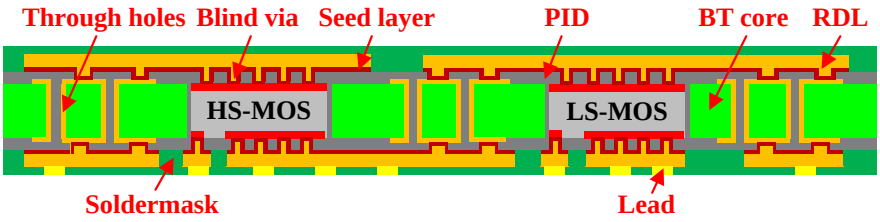
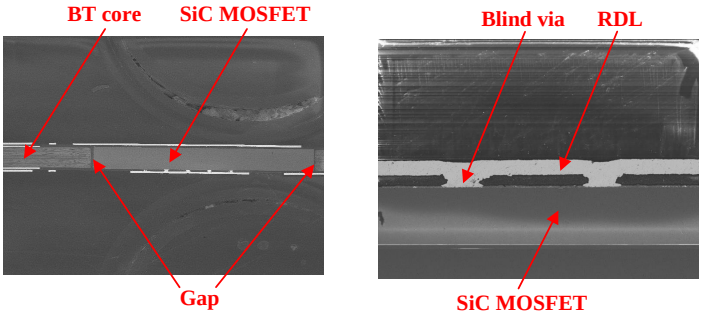


Figure 4.3: Schematic of a fan-out SiC MOSFET power module in an organic substrate.

Table 4.1: Geometry size of each component in the fan-out packaging

Component	Size (mm)
SiC MOSFET	3.36×3.10×0.186
Soldermask	15×15×0.04
PID	15×15×0.04
Chip pitch	6
BT core	15×15×0.186
Through hole	Diameter = 0.15, Pitch = 0.4
Blind via	Diameter = 0.1, Pitch = 0.2
RDL thickness	0.025

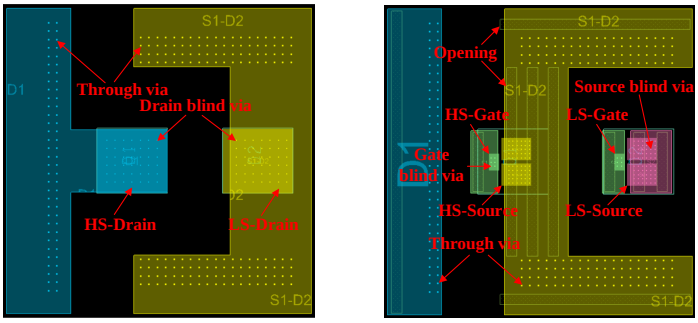
Figure 4.4(a) and (b) shows the cross-sections of the fan-out SiC MOSFET power module. Compared with the conventional wire-bonded packaging, the interconnection length within the fan-out packaging are greatly shortened, the parasitic inductances thus become lower. Compared with current embedded packaging technologies for Si and gallium nitride (GaN) devices, the proposed packaging structure has several unique merits, such as structure symmetry and double-sided cooling.



(a) HS-MOS region (b) Local zoom-in

Figure 4.4: Different cross-sections of the fan-out SiC MOSFET power module.

Figure 4.5(a) and (b) displays the front-side and backside of the fan-out packaging layout of the phase-leg SiC MOSFET power module. The package size is 15×15×0.36 mm^3. To withstand the voltage of 1.2 kV, the calculated safe distance between power terminals is 3 mm, as shown in the black regions of the figures. The Cu coverages of the front-side and backside RDLs are about 63% and 57%, respectively, so the package will take on a "smile" shape when cooling down from stress-free high temperature due to different Cu coverages.

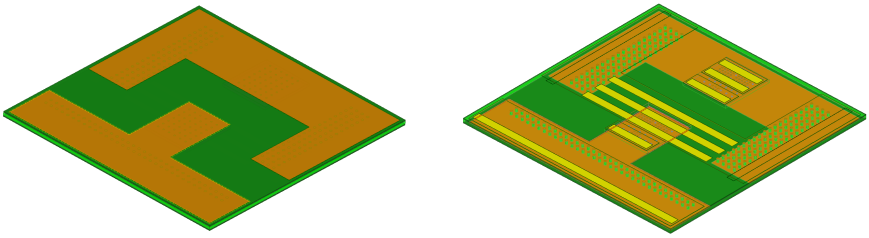


(a) Front-side (b) Backside

Figure 4.5: Packaging layout of the fan-out SiC MOSFET power module.

4.2.2. PARASITIC INDUCTANCES EXTRACTION

The voltage overshoot of SiC MOSFET is sensitive to parasitic inductances. In this work, ANSYS Q3D Extractor was used to extract the parasitic inductances of the fan-out SiC MOSFET power module. Figure 4.6(a) and (b) shows the parasitic inductance extraction model of the fan-out SiC MOSFET power module. Figure 4.7 illustrates the parasitic inductance definitions of the fan-out packaging. Table 4.2 lists the definitions, sources, and sinks of the package parasitic inductances.



(a) Front-side (b) Backside

Figure 4.6: Parasitic inductance extraction model of the fan-out SiC MOSFET power module.

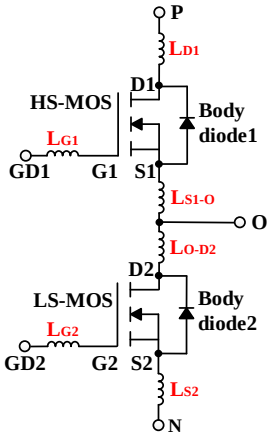


Figure 4.7: Parasitic inductance definitions of the fan-out packaging.

Table 4.2: Definitions, sources, and sinks of the parasitic inductances

Inductance	Definition	Source	Sink
L_{D1}	HS-MOS drain inductance	Interfaces between blind vias and HS-MOS drain	P terminal
L_{G1}	HS-MOS gate inductance	Interfaces between blind vias and HS-MOS gate	GD1 terminal
L_{S1-O}	HS-MOS source inductance	Interfaces between blind vias and HS-MOS source	O terminal
L_{O-D2}	LS-MOS drain inductance	Interfaces between blind vias and LS-MOS drain	O terminal
L_{G2}	LS-MOS gate inductance	Interfaces between blind vias and LS-MOS gate	GD2 terminal
L_{S2}	LS-MOS source inductance	Interfaces between blind vias and LS-MOS source	N terminal

Figure 4.8(a)~(f) shows the parasitic inductances of the fan-out SiC MOSFET power module dependent on switching frequency. The sweep frequency range was 20 kHz ~ 1 MHz. As shown in the figure, the parasitic inductances of the package decreased with the frequency, which was due to the skin and proximity effect. From 20 to 200 kHz, the parasitic inductances dropped significantly. The parasitic inductances decreased slowly and leveled off when increasing the frequency from 200 kHz to 1 MHz.

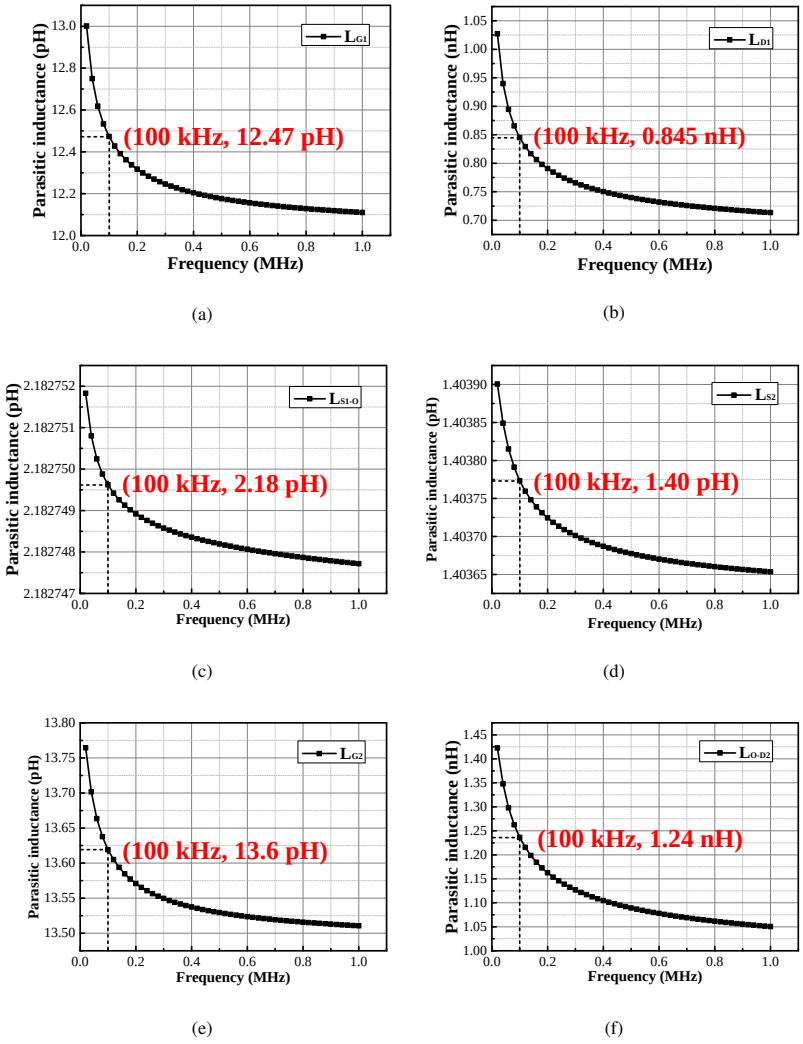


Figure 4.8: Parasitic inductances of the fan-out SiC MOSFET module dependent on switching frequency.

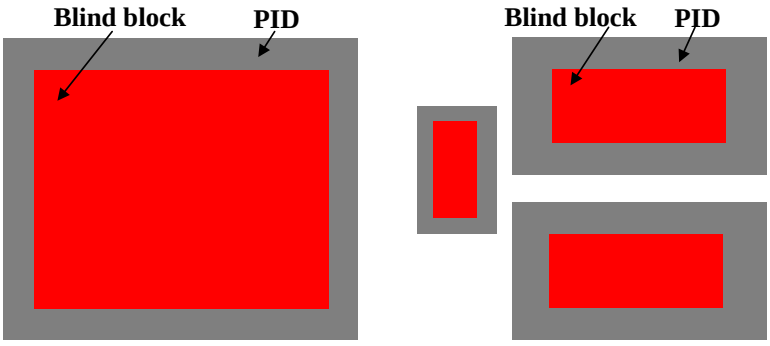
From Figure 4.3, it can be seen that the drains of HS- and LS-MOS are connected to the package terminals by blind vias, front-side RDLs, through holes, and backside RDLs, while the sources and gates are connected to the package terminals through blind vias and backside RDLs, so the drain inductances are much higher than the source and gate inductances. As shown in Figure 4.8, the HS-MOS drain inductance L_{D1} is about 0.845 nH at 100 kHz, and LS-MOS drain inductance $L_{O–D2}$ is about 1.24 nH at 100 kHz, which is the largest. Other parasitic inductances within the fan-out packaging are lower than 15 pH. Compared with wire-bonded packages, in which parasitic inductances exceed 10 nH, Therefore, the parasitic inductances of the fan-out packaging decreased by at least 87.6%.

4.2.3. THERMAL MODELING ANALYSIS

The thermal conductivities of packaging materials are relatively low. Furthermore, heat flux of SiC MOSFET is higher than that of Si counterparts with the same voltage rating due to the smaller size and the higher switching frequency, a more efficient heat dissipation design from the package's point of view should be first considered. The heat dissipation capability of the single-sided cooling design is limited. A packaging design that could remove the heat through double-side will be much more efficient.

As shown in Figure 4.3, SiC MOSFETs are communicated with outer interconnection layers through blind vias in the PID film. The blind vias are filled with Cu through sputtering and plating. Because the diameter of the blind via is only 100 μm, Cu coverage above the pads of SiC MOSFETs is relatively low, which is only about 3.2%. Theoretically, increasing the Cu coverage above the die pads can improve the heat dissipation of the fan-out SiC MOSFET power module. However, if only increasing the amount or the diameter of blind vias, the increase of Cu coverage above chip pads is limited.

In this section, an interconnection structure called a "blind block" was proposed to increase the Cu coverage above the SiC MOSFET pads, thus improving the heat dissipation capability of the fan-out SiC MOSFET power module. The blind block could be formed by PID exposure and development, panel-level PVD, and RDL interconnection techniques. Figure 4.9(a) and (b) shows the structure diagrams of the blind block above the SiC MOSFET pads.



(a) Drain (b) Gate and source

Figure 4.9: Structure diagram of the blind block above the SiC MOSFET pads.

Figure 4.10 shows a compact thermal resistance network model of the fan-out SiC MOSFET power module. The model includes junction-to-case thermal resistance (θ_{JC}) and junction-to-board thermal resistance (θ_{JB}) of the fan-out packaging, which were analyzed through ANSYS ICEPAK. Table 4.3 compares the thermal resistances of the blind via and blind block structures. From the table, it can be calculated that the thermal resistance of the proposed structure reduced by about 26%.

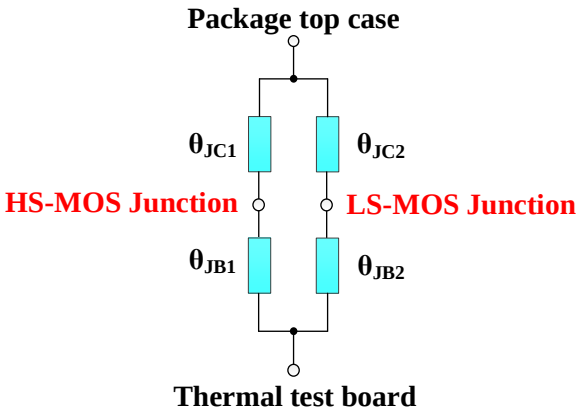


Figure 4.10: Compact thermal resistance network model of the fan-out SiC MOSFET power module.

Table 4.3: Comparison of thermal resistance between the blind via and the blind block structure

Structure above pads	θ_{JC1} (K/W)	θ_{JC2} (K/W)	θ_{JB1} (K/W)	θ_{JB2} (K/W)
Blind via	0.502	0.522	0.262	0.558
Blind block	0.386	0.386	0.256	0.455

4.2.4. THERMO-MECHANICAL VIRTUAL PROTOTYPING

Before the packaging process, the thermo-mechanical simulation was carried out using ANSYS Mechanical APDL to provide a guideline. The effect of the Cu coverage above the chip pads on von Mises stress was optimized.

Table 4.4 lists the thermo-mechanical properties of the packaging materials. SiC was considered as isotropic and elastic. RDL and PCB vias were assumed as elastoplastic. The material properties of PID and soldermask were taken from the vendors' datasheets. Figure 4.11 shows the storage modulus, loss modulus, and tan delta of the BT laminate dependent on temperature. As shown in the figure, the Tg of the laminate was up to 275 °C, which was much higher than most other organic substrate materials.

Table 4.4: Thermo-mechanical properties of the packaging materials

Component	Material	Tg (°C)	E (GPa)	CTE (ppm/°C)	υ
SiC MOSFET	4H-SiC	--	400	5.1	0.14
BT core	832NSF	275	See Figure 4.11	α1=5.3; α2=3	0.18
PID	PVI-3 HR100S	160~165	3.5	α1=45; α2=120	0.3
RDL	Cu	--	129	17.3	0.34
PCB via	Cu	--	129	17.3	0.34
Soldermask	--	--	8	29	0.4

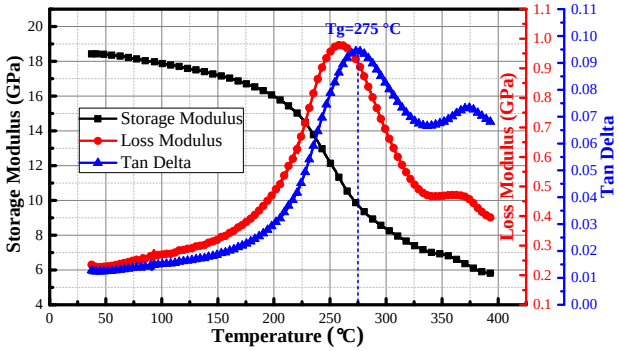
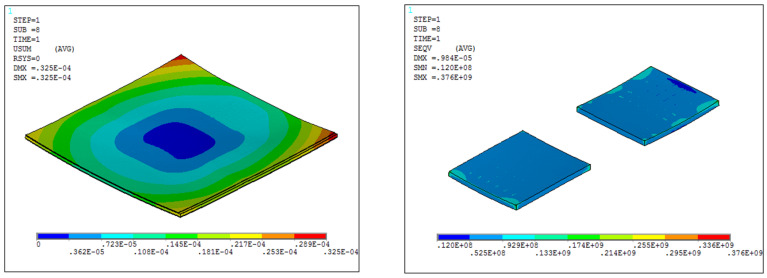


Figure 4.11: Storage modulus, loss modulus, and tan delta of the BT laminate dependent on temperature.

When conducting the thermo-mechanical simulation of the fan-out packaging, the initial reference temperature of the finite element model was set to be the baking temperature of 175 °C, the final room temperature was 25 °C, and the bottom center point of the model was fixed. Besides, the perfect adhesion was assumed between all material interfaces, and the manufacturing tolerances of dimensions were not considered [3]-[5].

Figure 4.12(a) shows the warpage of the fan-out SiC MOSFET module package after high-temperature baking. The package takes on an approximately isotropic "smile face" shape due to the asymmetrical chip layout, which is consistent with the previous analysis. The maximum warpage is about 32.5 μm, which is lower than 0.5% of the package diagonal length. Figure 4.12(b) illustrates the von Mises stress distribution of SiC MOSFETs. The figure shows that the maximum von Mises stress is 376 MPa, which occurs at the corner of the SiC MOSFET, and is far lower than the yield stress of 4H-SiC.



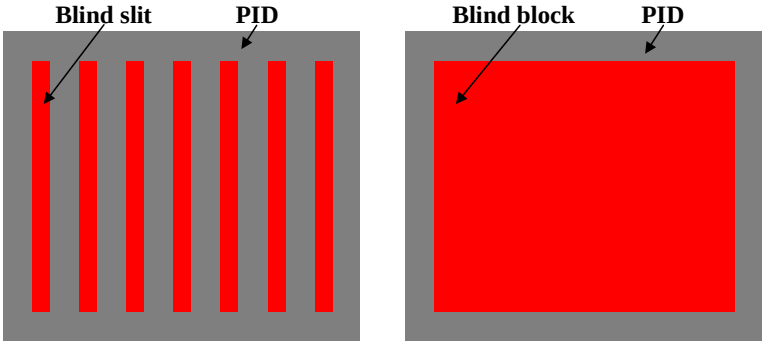
(a) Warpage of the fan-out packaging

(b) von Mises stress distribution of SiC MOSFETs

Figure 4.12: Thermo-mechancial simulation results.

From Table 4.4, it can be seen that the CTE of PID is relatively high compared to SiC and Cu. CTE mismatch between the SiC MOSFET and the PID film could lead to higher stress. In this work, the effects of the blind slit and blind block structures on von Mises

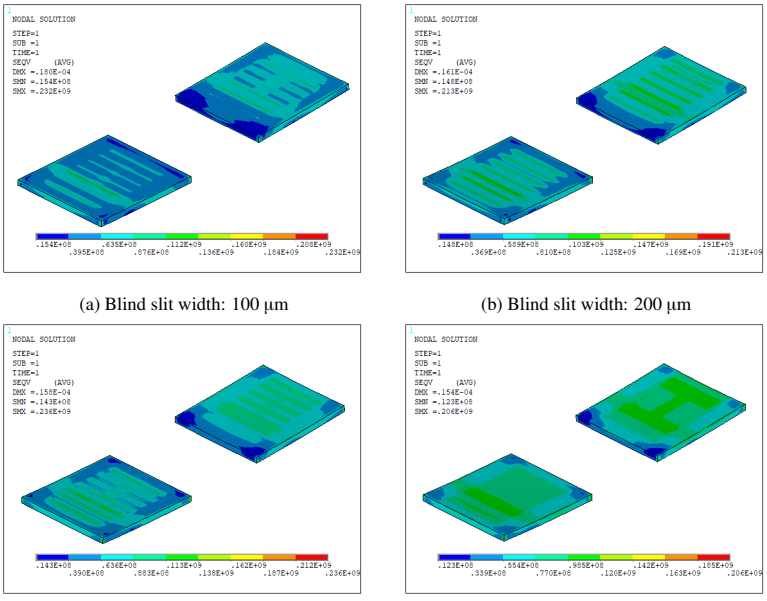
stress of SiC MOSFET were analyzed and compared. Figure 4.13(a) and (b) shows the structure diagrams of the blind slit and block above the drain, respectively.



(a) Blind slit (b) Blind block

Figure 4.13: Structure diagram above the MOSFET drain.

Figure 4.14(a)~(d) shows the von Mises stress distributions of the HS-MOS and LS-MOS in different structures. Compared with the blind via structure, the proposed blind block structures relieved the von Mises stress of SiC MOSFETs, and von Mises stress of the SiC MOSFETs decreased by about 45.2%.



(a) Blind slit width: 100 μm (b) Blind slit width: 200 μm

(c) Blind slit width: 300 μm (d) Blind block

Figure 4.14: von Mises stress of the HS-MOS and LS-MOS in different structures.

4.3. Fan-out packaging process in an organic substrate

Currently, commercial SiC MOSFETs are designed for front-side Al wire-bonding interconnection. Hence, metallization layers of front-side pads on these devices are Al, which is not compatible with the fan-out packaging process in an organic substrate. Thanks to the high reactivity, Al pads of SiC MOSFET could be damaged in the Cu plating process if they are not modified. Therefore, an additional metallization layer that can protect the Al pads in the plating and other processes should be added. In Ref. [6], 5 μm thick Cu was added to the MOSFET pads at the wafer level. For SiC power MOSFET, however, the cost and risk of pad re-metallization at the wafer level are high. Kearney *et al.* [7] modified the original metallization layers on the emitter and gate of IGBT chip by sputtering Cr/Cu (5 nm/8 μm) layers, while the dielectric region on the top surface of the IGBT chip was protected with a shadow mask. However, the size of SiC MOSFET is relatively small compared to IGBT, and it is challenging to realize the re-metallization of pads at such a small chip. Besides, SiC MOSFET is a vertical power device, with the gate and source on the front-side and drain on the backside, chip-level PVD easily contaminates one side when sputtering the other side. Therefore, the exploration of a new re-metallization technique for the fan-out SiC MOSFET packaging in an organic substrate is essential.

SiC MOSFETs that had the additional metallization layers were then embedded in an organic substrate, followed by blind vias that were usually formed by laser drilling and Cu plating, thus realized the electrical interconnection between the dies and the outer layers [6]-[9]. However, if the laser energy is not properly controlled, the terminal metallization pads could be damaged by laser drilling. The technique is not suitable for devices with very thin pads. Thicker pads are needed. Besides, the drilling process is complex, and the cost is relatively high. Therefore, a new alternative interconnection technique between the power devices and the outer layers needs to be developed.

4.3.1. Overall packaging process

In this work, a novel 114×114 mm^2 panel-level fan-out packaging technology for the phase-leg SiC MOSFET power module was developed. Figure 4.15 detailed the packaging process flow of the fan-out SiC MOSFET power module in an organic substrate.

First of all, a BT core of 0.18 mm, which was slightly thinner than SiC MOSFET, was laminated using one layer of BT laminate of 0.1 mm, two layers of BT prepreg of 0.04 mm, and two layers of Cu foil under the high-temperature and high-pressure condition. Figure 4.16 shows the lay-up for the lamination of BT core. Through holes in the core were drilled by a mechanical drilling system, internal RDLs on the core were built, and chip windows of 3.15×3.41 mm^2 in the BT core were drilled by a laser drilling system, which was bigger 50 μm than SiC MOSFET.

Furthermore, the core was attached to one layer of PID film and placed on one heating plate of 60 °C. The SiC MOSFETs were picked and placed in the chip windows of the core and covered by the other layer of PID film. There were gaps of about 25 μm between the SiC MOSFETs and the core. The gaps and through vias would be filled with PID when performing a vacuum laminating process under the temperature of 90 °C.

Next, some vital processes, including PID exposure and development technique, panel-level PVD technique, and double-sided RDL interconnection technique, were developed.

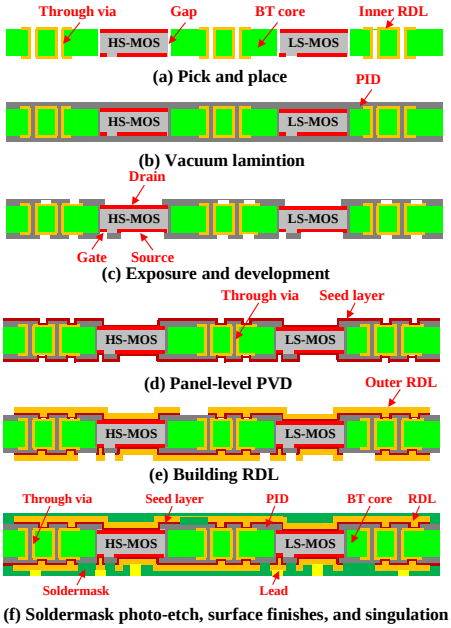


Figure 4.15: Process flow of the fan-out panel-level SiC MOSFET power module.

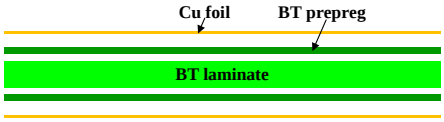


Figure 4.16: The lay-up for lamination of BT core.

4.3.2. PID exposure and development technique

In this work, SiC MOSFET dies were picked and placed in the chip windows of the core of 0.18 mm. The top and bottom surfaces of the core were covered by PID films and laminated in a vacuum laminator. Due to the flowability of PID during high-temperature processing, it flew into gaps between SiC MOSFETs and core, and through holes in the core. Chip pads and inner interconnection layers covered by PID films were then opened through the exposure and development process, as shown in Figure 4.17. Figure 4.18(a) and (b) show the terminal pads of SiC MOSFET after exposure, development, and cure. The PID film is a transparent material, so it is challenging to distinguish whether the die pads and inner RDLs are opened or not after development, leading to interconnection failure. If exposure and development condition is not well controlled, SiC MOSFETs and inner interconnection layers could not be open. Therefore, the core should not be thicker than the die, and the process conditions should be well controlled.

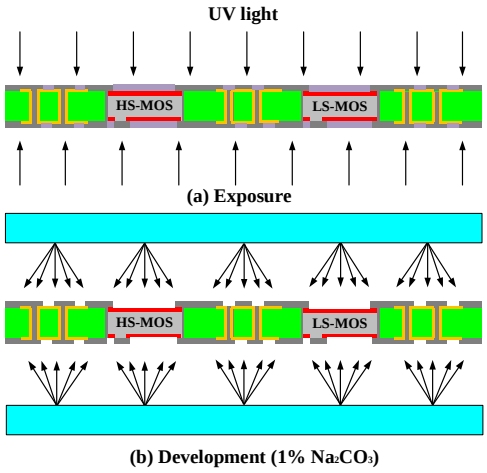
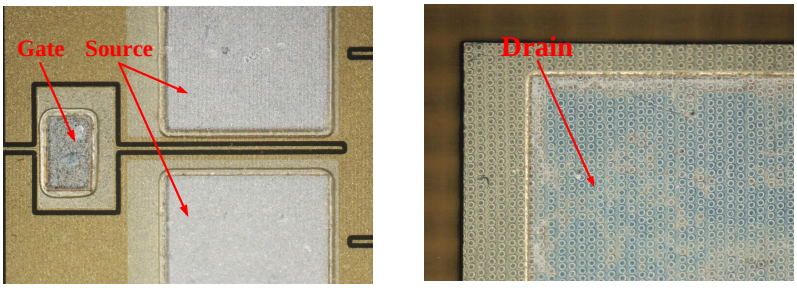


Figure 4.17: Process of PID exposure and development.

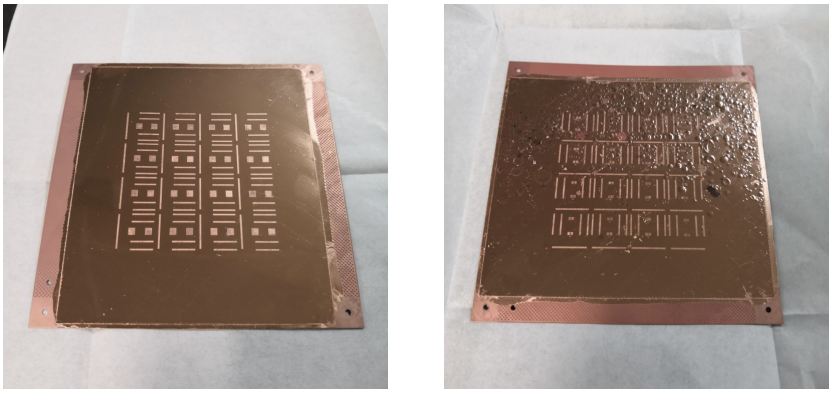


(a) Source and gate (b) Drain

Figure 4.18: Terminal pads of SiC MOSFET after exposure, development, and cure.

4.3.3. PANEL-LEVEL PVD TECHNIQUE

In this work, after PID exposure, development, and cure, the panel-level PVD process was carried out to sputter two-layer of seed layers on the top and bottom surfaces of the substrate. A thin layer of Ti (50 nm) is deposited on the surfaces to improve the adhesive force between the PID film and the final metal layer, followed by a layer of thick Cu (500 nm). Thus the Al metallization of front-side gate and source contacts and Ag metallization of backside drain contact were modified. Figure 4.19(a) illustrates one successful sputtering. Compared with the chip-level PVD, any chip pads can be re-metalized via the panel-level PVD. If the sputtering condition is not well controlled, some Cu bubbles could be induced on the organic substrate during the sputtering process, as shown in Figure 4.19(b). It is due to high-power sputtering and high-concentration air in the sputtering chamber. Therefore, a panel-level PVD process should be performed in a low-power and ultra-low vacuum environment.

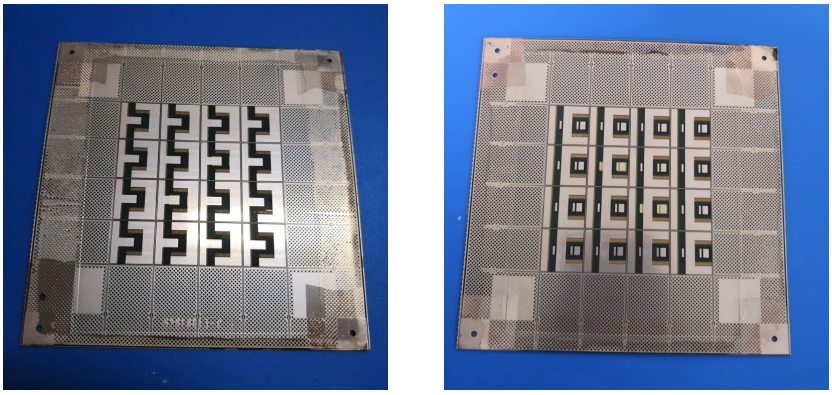


(a) Successful sputtering (b) Failed sputtering

Figure 4.19: Seed layers on the substrate surface.

4.3.4. Double-sided RDL interconnection technique

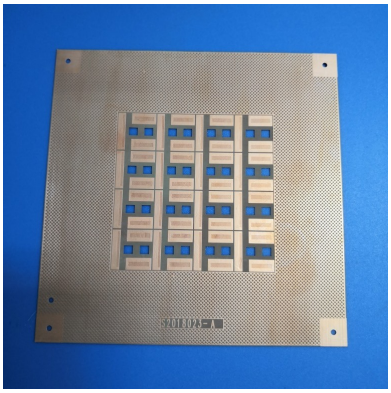
After the PVD process, the fan-out package's front-side and backside RDL layers were built by dry-film exposing and developing, and Cu plating. Cu and Ti on the non-conductive areas were removed through the flash etch process and hydrofluoric acid solution. Figure 4.20(a) and (b) shows the front-side and backside RDLs of the panel-level fan-out package, respectively. The double-sided RDLs replaced wire-bonds, and interconnection structure related to the DBC substrate, the physical length of the commutation loop was shortened. Thus parasitic inductances of the fan-out package were reduced.



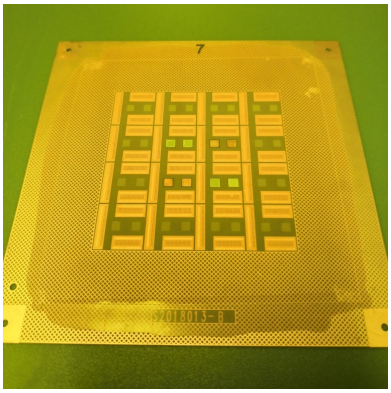
(a) Front-side (b) Backside

Figure 4.20: Double-sided RDLs of the panel-level fan-out package.

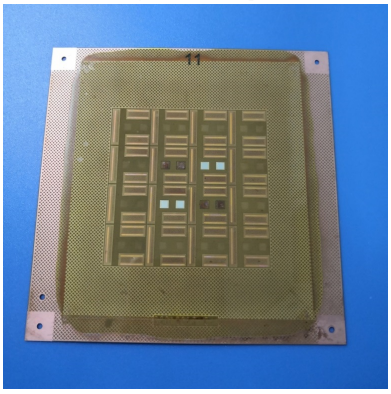
Figure 4.21(a)~(f) shows the main fan-out packaging process for a phase-leg SiC MOSFET power module. Table 4.5 compares this work and other current embedded technologies from ABB, Infineon, Fraunhofer IZM, etc.



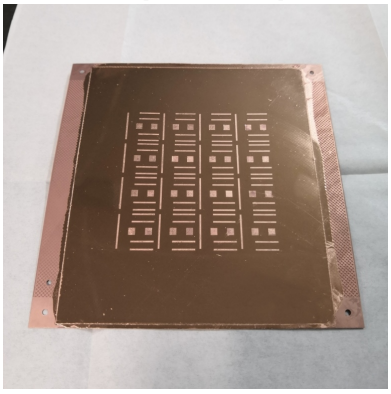
(a) Drilling holes and chip windows



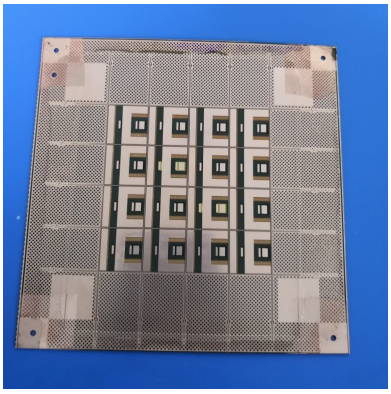
(b) PID exposure and development



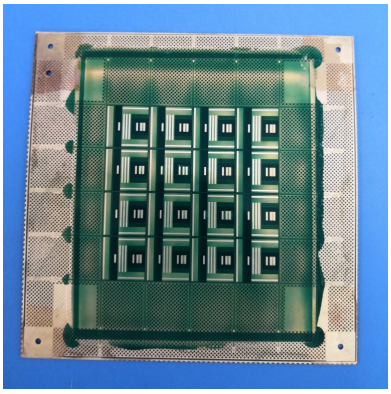
(c) PID curing



(d) Panel-level PVD



(e) Building RDLs



(f) Soldermask photo etch and surface finishes

Figure 4.21: Primary fan-out packaging process for a phase-leg SiC MOSFET power module.

Table 4.5: Comparison between this work and others

Technology	Power die	Substrate	Laminating material	Die re-metallization	Feature
This work	SiC MOSFET	BT core	PID	Ti/Cu (50/500 nm)	1) PID exposure and development; 2) Panel-level PVD; 3) Double-sided RDL interconnection; 4) Structure symmetry; 5) Double-sided cooling.
ABB [7]	IGBT and diode	Cu lead-frame	FR4 prepreg	Cr/Cu (5 nm/8 μm)	1) Dies were sintered into a Cu lead-frame with pre-machined cavities; 2) Interconnection by laser drilling and plating.
Infineon [10]	MOSFET	Cu lead-frame	FR4 prepreg		1) The lay-up for lamination contains two outer Cu foils, unstructured prepreg, and structured prepreg layers with openings at the chip positions and openings for epoxy resin flow control; 2) Laser drilled down to the lead-frame surfaces and chip landing pads.
IZM [11]	IGBT and diode	Base substrate	Prepreg	Ni/Pd	1) The base substrate was fabricated by laminating thick Cu and a thermally conductive prepreg layer; 2) Dies were sintered to the substrate at 200 °C with a pressure of 2 MPa.
AT&S [12]	GaN HEMT	Cu foil	Prepreg		1) Die face-down process; 2) Die was attached to a Cu foil via a layer of dielectric; 3) UV laser drilling.
ITRI [13]	IGBT and Diode	Cu lead-frame	ABF	Ti/Cu (100/300 nm)	1) IGBTs were attached to the lead-frame by SAC305 solder, whereas thicker diodes were sintered onto the half-etched Cu lead frame; 2) Sn layer was plated as a RDL patterning mask.
CNAM [14]	Diode	PCB	FR4 prepreg	Ni foam	A piece of Ni foam was used create a pressed contact between the top side of a PCB-embedded power die and the rest of the circuit.

4.4. SUMMARY

In this chapter, a novel fan-out panel-level packaging technology is proposed for a phase-leg SiC MOSFET power module. The high- and low-side SiC MOSFETs were embedded in an organic substrate, interconnected by double-sided RDLs and through vias, finally protected by double-sided soldermasks. Compared with current embedded packaging for Si and GaN devices, the proposed packaging structure has unique merits, such as structure symmetry and double-sided cooling. Then, the electrical, thermal, and thermal-mechanical simulations were conducted to evaluate and optimize the fan-out packaging performance. Lastly, a detailed 114×114 mm^2 fan-out panel-level packaging process for the phase-leg SiC MOSFET power module was introduced. Three essential packaging processes, including PID exposure and development, panel-level PVD, and double-sided RDL interconnection, could replace conventional laser drilling, chip/wafer-level PVD, and wire-bonding, respectively.

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5

Static and dynamic characterizations of SiC MOSFETs

In this chapter, the static and dynamic characteristics of the fan-out SiC MOSFET power module were studied. First of all, the effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed via two custom fixtures. The experimental results showed that the I-V non-saturation feature of SiC MOSFET was more evident after packaging, and higher drive voltage was required to turn-on SiC MOSFET fully due to the extension of the non-flat Miller plateau. Then, the switching performance of the fan-out phase-leg SiC MOSFET was evaluated via double pulse tests. A phase-leg that is composed of two TO-247 discrete packages was used as a benchmark. The experimental results showed that the fan-out packaging had smaller voltage overshoot and current oscillation at turn-off and smaller voltage oscillation and current overshoot at turn-on than TO-247 package.

Parts of this chapter have been published in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 367-380, 2020 [1].

5.1. Experimental sample

Figure 5.1 shows the size comparison among the phase-leg SiC MOSFET module, a 5 cent euro coin, and a TO-247 single-chip discrete device from CREE. From the figure, it can be seen that the phase-leg SiC MOSFET module is smaller than 5 cent euro coin and much smaller than the TO-247 discrete device, which is a standard single-chip packaging form and has long terminals. Figure 5.2 shows the phase-leg SiC MOSFET power module circuit with equivalent parasitic elements. The leads of the package sample are corresponding to the terminals of the phase-leg SiC MOSFET power module.

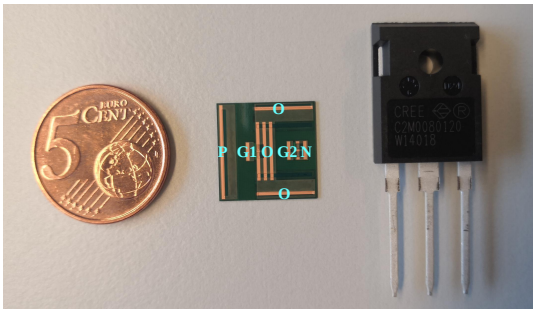


Figure 5.1: Size comparison among the phase-leg SiC MOSFET module, a 5 cent euro coin, and a TO-247 single-chip discrete device from CREE.

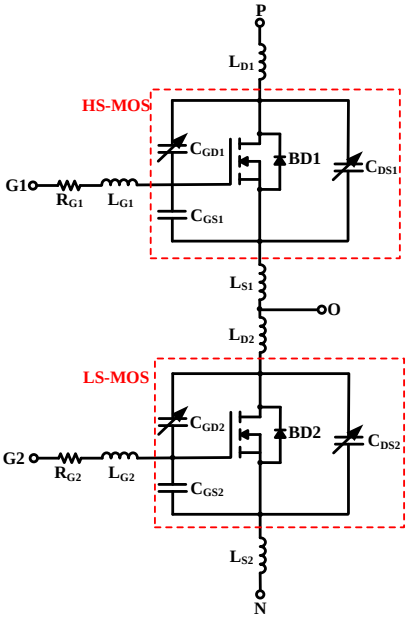


Figure 5.2: A phase-leg SiC MOSFET power module circuit with equivalent parasitic elements.

5.2. STATIC CHARACTERIZATION

5.2.1. EXPERIMENTAL APPROACH

In this chapter, a new custom fixture for static characterization of the fan-out SiC MOSFET power module package was developed, as shown in Figure 5.3. The static characteristics of HS-MOS in the SiC MOSFET power module were measured using Power Device Analyzer (Keysight B1505A). The effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were investigated.

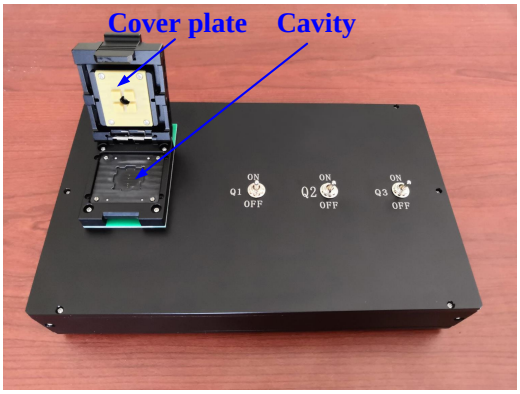


Figure 5.3: Custom fixture for static characterization of the fan-out SiC MOSFET power module.

The fan-out SiC MOSFET power module was flipped and placed in the fixture cavity with probes corresponding to the module leads, then capped by a cover plate. The probes could realize the electrical interconnection between the module and the external circuit. The current limiting in the experiments was set to 20 A, in case the excessive current damaged the module and probes.

5.2.2. EXPERIMENTAL RESULTS

(1) I-V characterization

Figure 5.4 shows the test circuit for I-V characteristics of the fan-out SiC MOSFET power module. The gate and drain of HS-MOS were connected to its source through two voltage sources. The drain-source voltage V_{DS} was swept from 0 to 4 V at the gate-source voltage V_{GS} from 10 to 20 V in steps of 2 V.

Figure 5.5 shows the effect of the fan-out packaging on I-V characteristics of SiC MOSFET. It can be observed that the SiC MOSFET's I-V non-saturation characteristics were more evident after packaging. The drain current I_D of the fan-out packaging was increased under the same V_{GS} and V_{DS} compared to the SiC MOSFET bare die. Therefore, for the fan-out packaging, to get the same output current under the same V_{DS}, higher drive voltage is needed due to the existence of parasitic resistance induced by packaging.

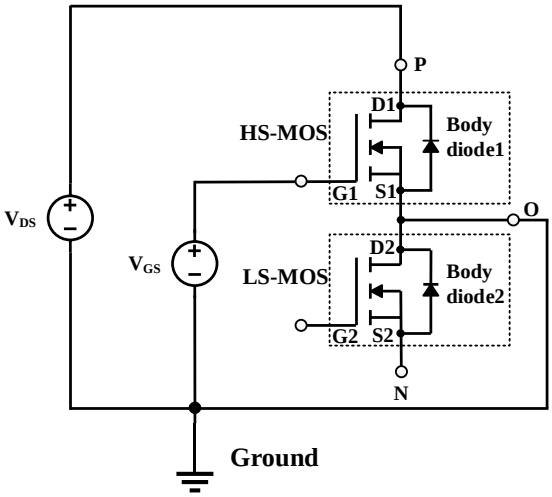


Figure 5.4: Test circuit for I-V characteristics of the fan-out SiC MOSFET power module.

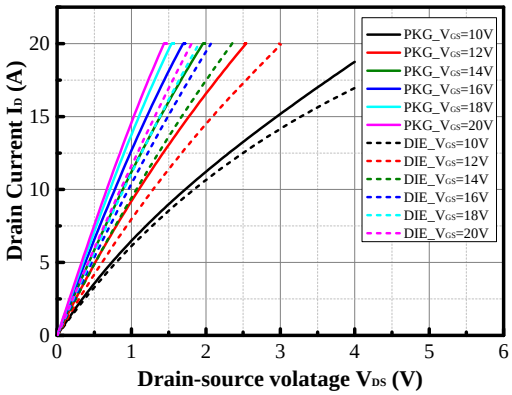


Figure 5.5: Effect of the fan-out packaging on I-V characteristics of SiC MOSFET.

(2) C-V characterization

Figure 5.6 shows the test circuit for C-V characteristics of the fan-out SiC MOSFET power module. The gate of HS-MOS was short-connected to its source. The drain of HS-MOS was connected to its source through one voltage source. The drain-source voltage V_{DS} was swept from 0 to 200 V. Three AC small signals were adopted to test the input, output, and output capacitances, respectively. The frequency is 100 kHz.

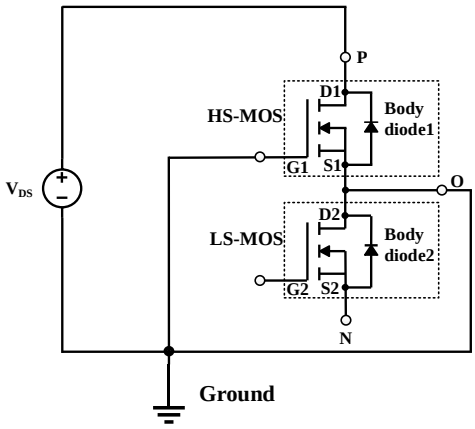


Figure 5.6: Test circuit for C-V characteristics of the fan-out SiC MOSFET power module.

Figure 5.7 shows the effects of the fan-out packaging on input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitances of SiC MOSFET. As seen in the figure, the fan-out packaging had a great impact on reverse capacitance (Miller capacitance) of SiC MOSFET, a certain effect on output capacitance, and little influence on input capacitance. Due to the package-induced parasitic capacitance, the Miller capacitance of SiC MOSFET within the module became larger than that of bare die. As drain-source voltage V_{GS} increased, the difference of Miller capacitance between the package and the bare die increased. According to Eq. (3.5) ~ (3.6), both the gate-source capacitance C_{GS} and the drain-source capacitance C_{DS} of the fan-out SiC MOSFET power module were decreased.

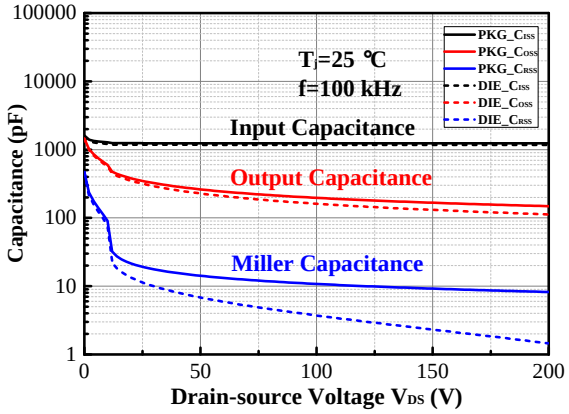


Figure 5.7: Effect of the fan-out packaging on input, output, and reverse capacitances of SiC MOSFET.

(3) Gate charge characterization

Figure 5.8 shows the effect of the fan-out packaging on gate charge of SiC MOSFET. As found in the figure, Q_{GS} was almost the same before and after packaging. In the first stage (I), C_{ISS} that was almost not affected by the fan-out packaging was being charged by the gate current I_G from OFF- to On-state of SiC MOSFET, C_{GS} is much larger than C_{GD}, so Q_{GS} was almost the same in the first stage. In the second stage (II+III), Miller capacitance of the fan-out SiC MOSFET power module was increased, so the non-flat Miller plateau of the fan-out packaging extended compared to SiC MOSFET bare die, Q_{GD} and V_{GS} increased by 10 nC and 1.1 V, respectively. The extension of Miller plateau indicated higher drive voltage was required to make the fan-out SiC MOSFET power module turn-on from ON- to fully ON-state.

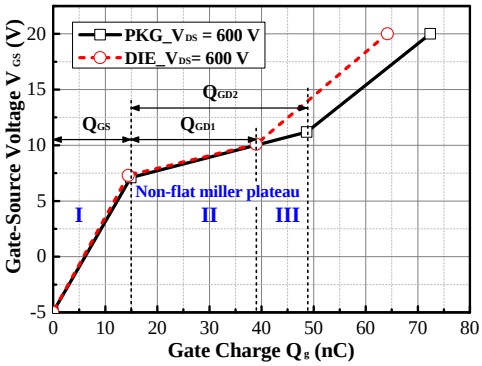


Figure 5.8: Effect of the fan-out packaging on gate charge of SiC MOSFET.

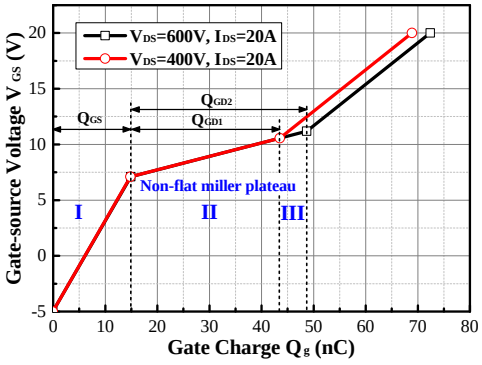


Figure 5.9: Effect of the drain-source voltage on gate charge of SiC MOSFET.

For the fan-out SiC MOSFET power module, the effect of the drain-source voltage V_{DS} on Qg was also investigated, as shown in Figure 5.9. It is found that as drain-source voltage V_{DS} increased, the non-flat Miller plateau extended, which meant higher drive voltage was needed to make fan-out SiC MOSFET power module fully ON-state as V_{DS} increased.

5.3. Dynamic characterization

5.3.1. Experimental approach

Double pulse test (DPT) is widely used for evaluating the switching characteristics of power devices, e.g., MOSFET and IGBT [1]-[3]. It is an inductive load DPT setup and primarily consists of a DC power supply, a load inductor, a DC capacitor, and a gate driver.

In this work, DPT was used to evaluate and compare the switching characteristics of SiC MOSFET in the fan-out phase-leg power module and the conventional TO-247 discrete device. Two TO-247 discrete devices (C2M0080120D) from CREE were selected to form a phase-leg. Figure 5.10 shows the equivalent circuit schematic of DPT. DC bus voltage was set to 600 V. The gate of HS-MOS was connected to its source, and its body-diode was used for the reverse recovery. The LS-MOS was controlled by a double pulse gate signal, as shown in the figure. The time of the first and second pulse was 1 µs and 0.3 µs, respectively. The duration between the two pulses was 5 µs.

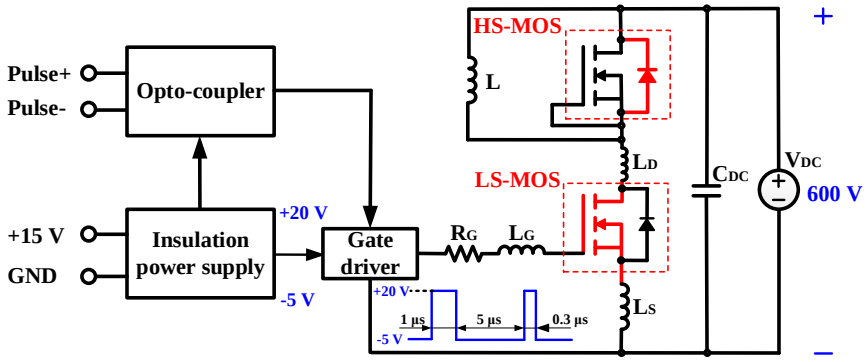


Figure 5.10: DPT equivalent circuit.

Figure 5.11(a) and (b) display DPT boards of the fan-out phase-leg power module and the two TO-247 discrete devices, respectively. Because the fan-out packaging is a surface mount device, it is challenging to test real switching waveforms of the package. In this experiment, switching waveforms of test points on the DPT boards of the fan-out packaging and the TO-247 discrete device were measured and compared. Test points on the DPT boards were designed as close as possible to the leads of the fan-out packaging and TO-247 discrete device, as shown in Figure 5.11(a) and (b), respectively. In order to ensure equal comparison, both the distances of the power and driver loop of the two packages on the DPT boards were nearly identical.

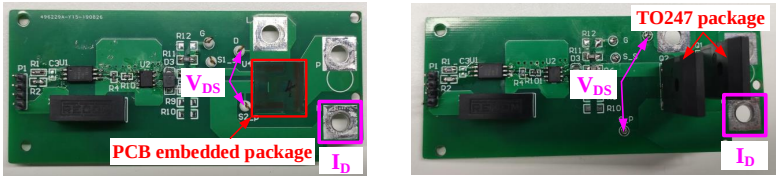
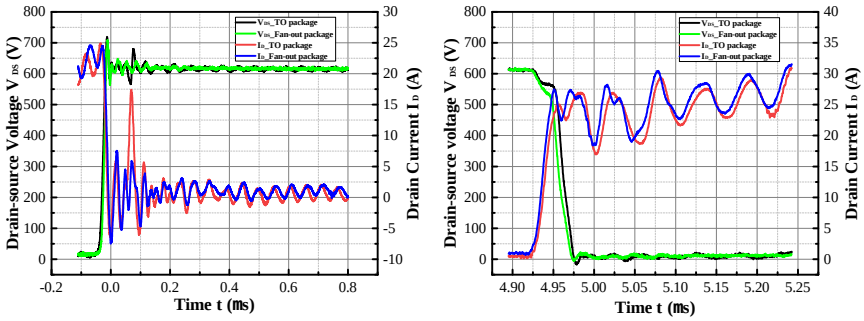


Figure 5.11: DPT boards of (a) fan-out packaging and (b) two TO-247 discrete devices.

5.3.2. EXPERIMENTAL RESULTS

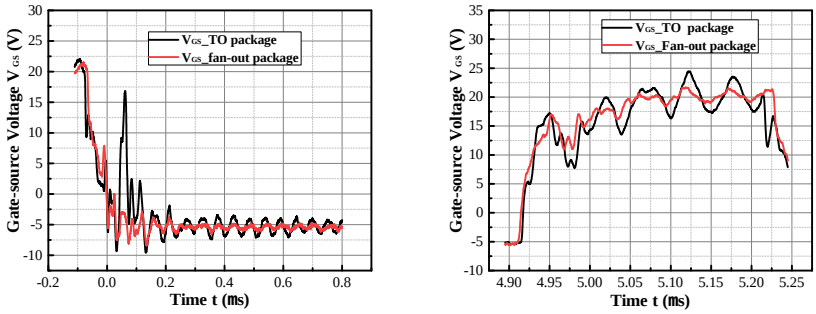
Figures 5.12 and 5.13 compare the switching characteristics and the driver signal waveforms between the fan-out packaging and the TO-247 discrete device. As can be seen from Figure 5.12(a) and (b), the fan-out packaging had smaller voltage overshoot and current oscillation at turn-off and smaller voltage oscillation and current overshoot at turn-on than TO-247 discrete device. The results indicated that the fan-out packaging had smaller parasitic inductances and capacitances than the TO-247 discrete device, making SiC MOSFET more suitable for high voltage and high-frequency applications.

As can be seen from Figure 5.13(c) and (d), the driver signals of the fan-out power module had significantly smaller oscillation than the TO discrete package. Because the power and driver loops were connected through source terminal of LS-MOS, larger parasitic inductances of the power loop connected to the TO-247 discrete device would affect the driver loop, leading to the larger oscillation of the drive signal. When the oscillation amplitude exceeded the threshold voltage of SiC MOSFET, it could falsely turn on the device, affecting the regular operation of the circuit. The fan-out packaging module proposed in this paper had smaller parasitic inductances, which could reduce the oscillation of the driver signal and avoid false turn-on in high-frequency applications.



(a) Turn-off (b) Turn-on

Figure 5.12: Comparison of switching characteristics between the fan-out packaging and TO-247 discrete device



(a) Driver signal transition from high-to-low voltage (b) Driver signal transition from low-to-high voltage

Figure 5.13: Comparison of driver waveforms between the fan-out packaging and TO-247 discrete device

5.4. SUMMARY

IN this chapter, the static and dynamic characteristics of the fan-out SiC MOSFET power module were studied. First of all, the effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed via custom fixtures. The experimental results showed that SiC MOSFET's I-V non-saturation characteristics were more evident after packaging, and higher driver voltage was required to fully turn-on SiC MOSFET due to the extension of the non-flat Miller plateau. Then, the switching performance of the fan-out phase-leg SiC MOSFET was evaluated via double pulse tests. A phase-leg that is composed of two TO-247 discrete packages was used as a benchmark. The experimental results showed that the fan-out packaging had smaller voltage overshoot and current oscillation at turn-off transient, and smaller voltage oscillation and current overshoot at turn-on transient than TO-247 package.

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6

Microchannel thermal management system with the two-phase flow

In this chapter, a microchannel thermal management with two-phase flow boiling using refrigerant R1234yf is presented. Both single- and multi-chip silicon thermal test vehicles (TTVs) were fabricated and attached to a microchannel heat sink (MHS) with two-phase flow. A vapor compression refrigerant system (VCRS) was implemented to realize and control the phase-change of R1234yf. The system includes two identical aluminum (Al) MHSs connected in series, a gas flowmeter, a miniature compressor, a condenser, a throttling device, and several accessory measurement components. The experimental results showed that the thermal management system could dissipate a heat flux of 526 W/cm^2 while maintaining the junction temperature below 120 °C. For SiC MOSFET with a junction temperature of 175 °C, the thermal management system was expected to dissipate a heat flux as high as 750 W/cm^2. The effects of the rotational speed of the compressor, the opening of the throttling device, TTV layout on MHS, and a downstream heater on the system's cooling performance were analyzed in detail. The study showed that the opening of the throttling device had a significant effect on cooling performance. For the multi-module system, the chip at the upstream location displayed the best cooling performance. The downstream TTV on MHS2 could function as a super-heating device instead of a heat-dissipating device, making the junction temperature of upstream TTV at a low value.

Parts of this chapter have been published in IEEE Transactions on Power Electronics, 2020 [1] and Applied Thermal Engineering, vol. 163, 114338, 2019. [2].

6.1. Design of thermal management

6.1.1. Two-phase cooling for the fan-out SiC MOSFET

Figure 6.1 shows the schematic of the fan-out SiC MOSFET power module assembled on an MHS with two-phase flow. An environment-friendly refrigerant R1234yf was adopted. Its boiling point at 1.01 bar is -29.5 °C. A high thermal conductivity thermal interface material (TIM) was applied between the SiC MOSFET power module and the MHS to reduce the contact resistance. The maximum heat generated by SiC MOSFETs could be absorbed by taking full advantage of the latent heat of liquid R1234yf while vaporizing in the MHS.

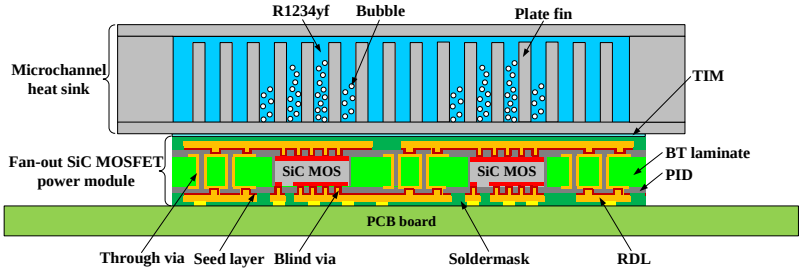
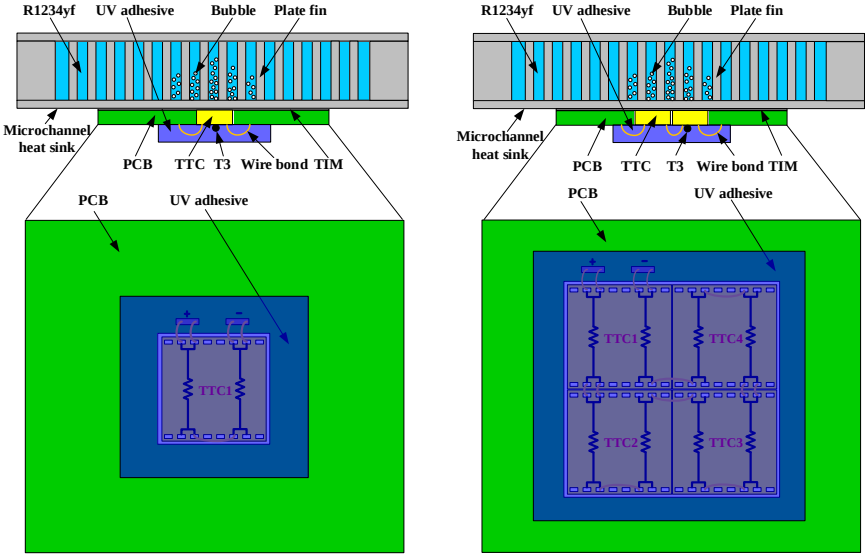


Figure 6.1: Schematic of the fan-out SiC MOSFET power module assembled on an MHS with flow boiling



(a) TTV1 (b) TTV2

Figure 6.2: Test schematics of TTVs assembled on the MHS.

The fan-out SiC MOSFET power module is a phase-leg unit. It is challenging to acquire accurate heat flux when it is operating. TTVs that their heat flux could be accurately adjusted were used to evaluate the cooling performance of the MHS with two-phase flow boiling. Figure 6.2 shows the test schematics of single- and multi-chip TTVs assembled on the MHS. The TTCs were attach to the MHS through a layer of TIM.

6.1.2. TTVs

Currently, SiC-based TTC is not available on the market, Si TTC from Thermal Engineering Associates Inc. was selected to simulate the SiC MOSFETs. The size of a single TTC was 2.5×2.5×0.625 mm^3, which had two resistors in the same layer and four diodes in the other layer. The two resistors covered more than 85% of the chip area. The electrical resistance of each resistor was 7.6 Ω ± 10%.

Two TTVs, namely TTV1 and TTV2, were designed and fabricated. Figure 6.3 shows the packaging and assembling process flow of single-chip TTV1 on the MHS. A TTC was picked and placed in chip windows of an organic substrate with the almost same thickness, and temporarily bonded onto a carrier through a layer of temporary bond film (TBF). The two resistors on the TTC were connected in series and bonded to two substrate pads close to the chip windows through gold wires. The total electrical resistance of the TTV1 reached about 15.2 Ω. A thermocouple (TC) was directly attached to the top surface of TTC so that its junction temperature could be precisely monitored in real-time when it was operating. The TTC and TC were then encapsulated by ultraviolet (UV) adhesive to protect from damage. After that, the TTV1 was debonded from the carrier.

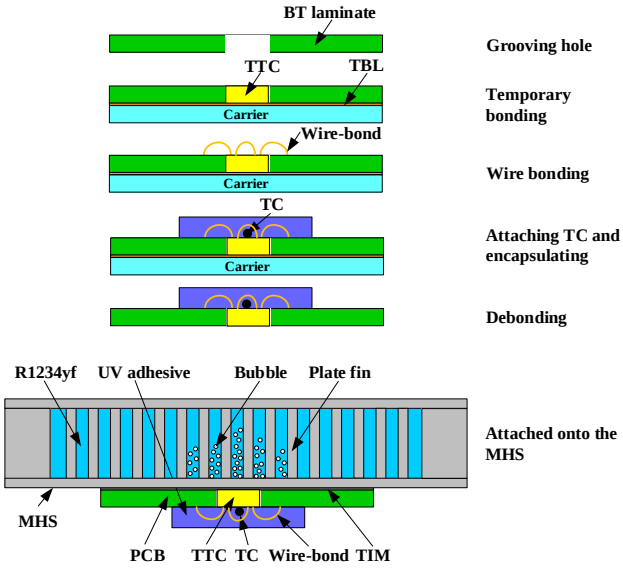
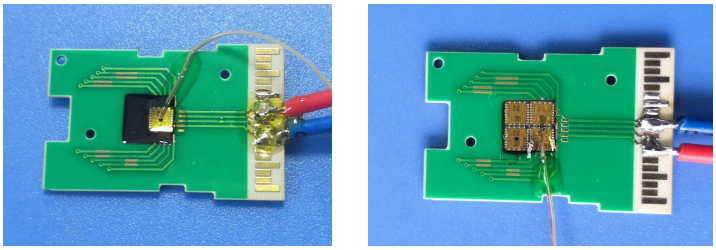


Figure 6.3: Packaging and assembling process flow of TTV1 on the MHS

The TTC in the TTV1 was then directly attached to the bottom center of MHS through a layer of TIM with high thermal conductivity, as shown in Figure 6.2(a) and (b). The TIM (TC-5888) from Dow Corning was used. It combined advantages of high thermal conductivity (5.2 W/m·K) and thin bond line thickness of approximately 20 μm, which yielded a low specific thermal resistance of 0.05 °C·cm^2/W.

For TTV2 with multi-chips, it integrated four TTCs in a 2×2 array without extra spacing. The eight resistors in the four TTCs were connected in series and then bonded to two substrate pads close to the chip windows through gold wires. The chip area and electrical resistance of TTV2 were four times of TTV1, amounting to 0.25 cm^2, and 60.8 Ω, respectively. Figure 6.4(a) and (b) shows the TTV1 and TTV2 samples, respectively.



(a) TTV1 (b) TTV2

Figure 6.4: TTV samples

6.1.3. VCRS

In this study, a VCRS was implemented to realize and control the phase-change of R1234yf. Figure 6.5 and Figure 6.6 illustrate the experimental measurement platform and schematic diagram of the designed VCRS. The system mainly consists of two identical Al MHSs connected in series, a miniature compressor, a condenser, a throttling device, and several accessory measurement components. All the components were connected through Cu tubes and fittings.

In the VCRS, the compressor was to increase the pressure of the refrigerant, while the throttling device played a reverse role. The system was divided into a high-pressure (HP) region and a low-pressure (LP) region by the two components. The two MHSs, gas flowmeter, and LP transducer were in the LP region, and the condenser and HP transducer lay in the HP region.

The temperatures at the connection tubes of the LP region could reduce to -10~-20 °C when the system was operating. In order to decrease the effect of heat loss on the cooling performance of the system due to the vast temperature difference between the connection tubes and the ambient, the connection tubes in the LP region were protected with rubber foam tubes, as shown in Figure 6.5.

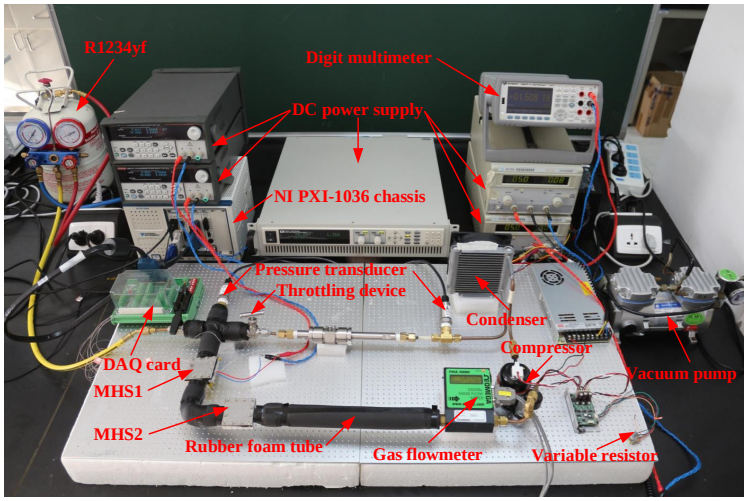


Figure 6.5: Experimental measurement platform of VCRS

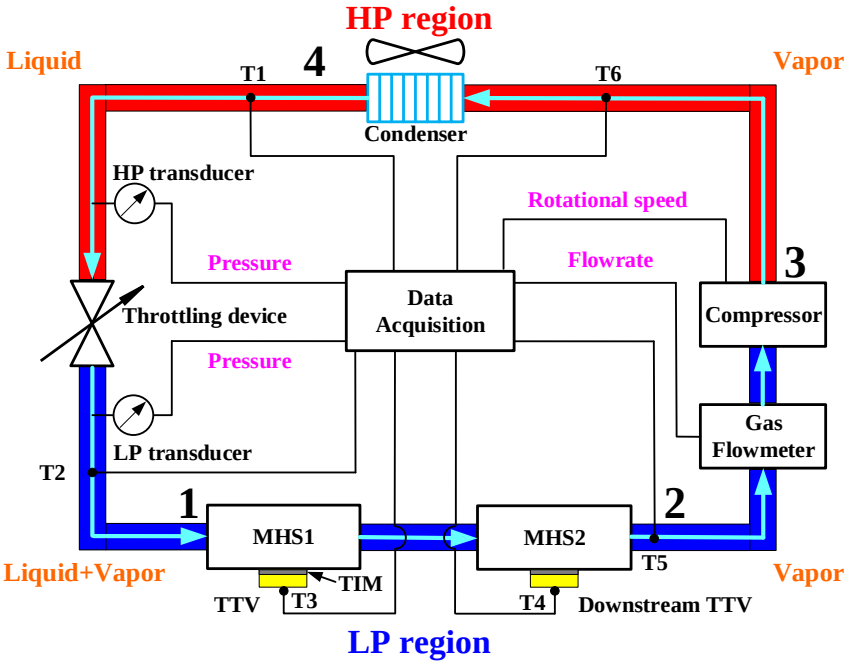


Figure 6.6: Schematic diagram of VCRS

6.1.4. MHS COMPONENT

In this work, two identical Al MHSs were designed and fabricated, whose thermal resistance was about 0.04 °C/W. The MHS is a highly compact and lightweight Al component. Its detailed size is shown in Table 6.1. A single MHS, denoted as MHS1, was studied in Section 6.2.1-6.2.4, whereas two MHSs, denoted as MHS1 and MHS2, were analyzed in Section 6.2.5.

Table 6.1: The size of MHS

Part	Size (mm)
MHS	50×50×9
Base plate	50×50×1
Cover plate	50×50×1
Chamber	30×30×7
Plate fin	20×0.5×6
Channel spacing	0.5
Inner diameter of tube	5.35
Outer diameter of tube	6.35

Figure 6.7 shows the interior structure of MHS. Initially, to observe the refrigerant's vaporization phenomena, the MHS was sealed by a visible polymethyl methacrylate (PMMA) plate using a plastic sealing ring and glue. Unluckily, when the heat flux of the TTC increased to about 200 W/cm^2, the PMMA plate was fractured by vapor flow beating. For safety, the chamber was sealed by an Al plate through-bolt connection and glue sealing to withstand higher vapor pressure.

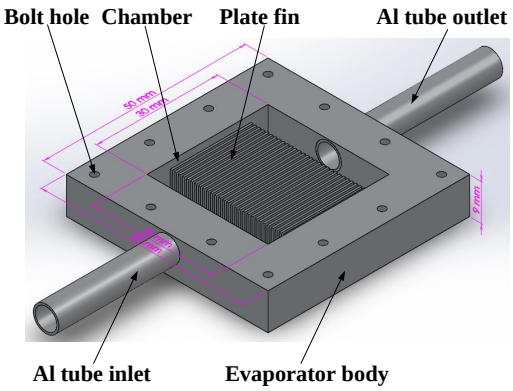


Figure 6.7: Interior structure of MHS

The MHS has one inlet and one outlet Al tubes, which could connect to the standard Cu tubes with straight connectors, and then connect to the system. TTV needs to attach the bottom of MHS to realize a better cooling effect.

6.1.5. Other components

(1) Compressor

A miniature rotary compressor (14-24-000X) from Aspen was used in the system. As far as we know, it is the smallest and lightest compressor available on the market. Its suction volume was 1.4 cm^3, and the maximum rotational speed was up to 6500 rpm, which can be adjusted by a variable resistor. The pressure and flow rate of refrigerant thus could be adjusted through the variable resistor. Compared with the pump, the compressor cannot only move the fluid but also increase the potential energy of fluid by compressing it in a closed system, thus controlling the phase-change of refrigerant.

(2) Throttling device

The throttling device played a dual role in regulating its pressure drop and flow rate and preventing large pressure drop oscillations across the test module. The pressure in the LP region could reduce to very low by decreasing the opening of the throttling device so that the refrigerant in the MHS could absorb a large amount of heat due to easy vaporation. When liquid refrigerant began to dry off, more refrigerants could enter the MHS by adjusting the opening of the throttling device, and new phase-change would continue to occur and absorb much more heat.

(3) Condenser

The condenser is an opposite component of MHS. When refrigerant passed through it, heat absorbed in the MHS and compressor could dissipate into the ambient. An Al mini-channel heat exchanger was adopted as the condenser, which was fabricated based on a mini-end milling process. A fan was applied onto the condenser to improve the convective heat transfer coefficient.

(4) Measurement components

To accurately evaluate the cooling performance of the thermal management system, several accessory measurement components were connected to the system.

Six high precision Type K TCs (T1-T6) from OMEGA were adopted to monitor the ***temperatures*** at different locations of the system. Figure 6.6 shows one of the attached locations. The positive and negative leads of the six TCs were connected to a high-resolution data acquisition device from National Instruments. The real-time temperatures could be read via LabVIEW. All TCs signals were calibrated before testing, and the reference temperature was set to 20 °C.

Two voltage output pressure transducers (PX309-200 G5V) from OMEGA were selected to detect the ***pressure*** of the HP region and LP region, respectively. The pressure range was 0~14 bar, and the driver voltage/current was 5 V/0.1 A. The pressure changes in the evaporators were negligible compared to those in the throttling device and miniature compressor [3], so the two pressure transducers could provide the important data needed to

assess the system performance. The pressures could be displayed in real-time in the form of voltages by a digit multimeter from KEYSIGHT. Figure 6.8 displays the calibration curve of the pressure transducer. It is found that the pressure P is almost proportional to the voltage U_{PT}. The correlation can be fitted as follows.

$$P = 2.32 \times U_{PT} + 0.565. \tag{6.1}$$

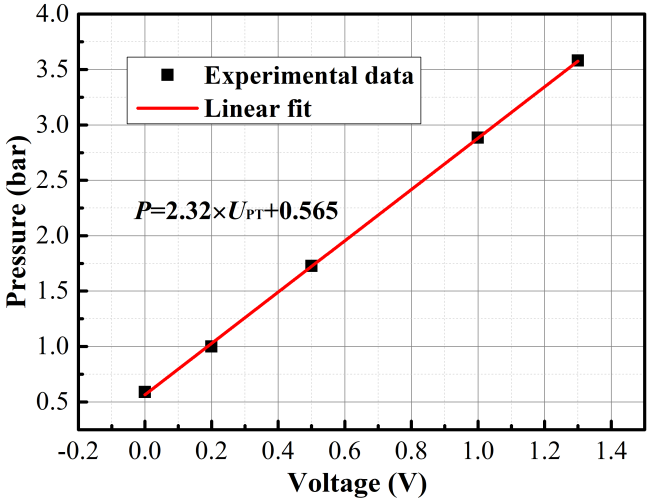


Figure 6.8: Calibration curve of the pressure versus the voltage output for the pressure transducer

The digit multimeter could indirectly acquire the ***rotational speed*** of the compressor. The voltage of the variable resistor U_{VR} could be read when the compressor was operating. The rotational speed of compressor n (rpm) then can be calculated as Eq. (6.2):

$$n = \begin{cases} 0 & (4.3\text{V} \le U_{VR} < 5\text{V}) \\ 7078.93 - 1157.89 U_{VR} & (0.5\text{V} \le U_{VR} < 0.3\text{V}) \\ 6500 & (U_{VR} < 0.5\text{V}). \end{cases} \tag{6.2}$$

The gas flowmeter (FMA-4312) from OMEGA was used to monitor the ***flowrate*** of vapor refrigerant, which could be directly read in the electronic display. The driver voltage/current was 5 V/0.09 A, and the flowrate range was 0~10 L/min.

The ***temperatures*** at different positions, the ***pressures*** of HP and LP regions, the ***flowrate*** of vapor refrigerant, and the ***rotational speed*** of compressor could be recorded in real-time. The system would have a better cooling performance only if these parameters were properly controlled.

6.1.6. Thermodynamic analysis of R1234yf refrigerant

R1234yf from Honeywell was selected as the refrigerant and filled into the system. Figure 6.9 shows the variation of vapor pressure with the saturation temperature of R1234yf. The fit function is expressed as Eq. (6.3).

$$P = \exp(1.14119 + 0.03326T_s - 9.33109 \times 10^{-5} T_s^2 \tag{6.3}$$

where T_s is the saturation temperature of R1234yf, and P is the corresponding pressure. As seen in the figure, the pressure of the refrigerant rises nearly quadratically with the saturation temperature. Under the same temperature, reducing the pressure can make the refrigerant change from liquid to vapor, and thus absorb a large amount of heat. Likewise, increasing the pressure can make the refrigerant change from vapor to liquid, and thus release much heat.

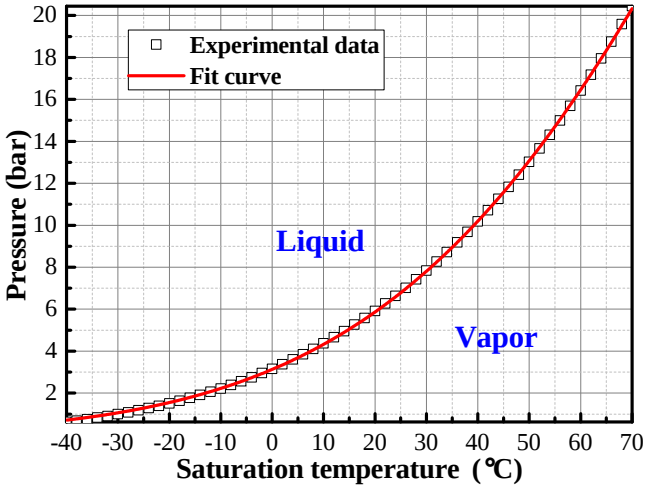


Figure 6.9: Variation of pressure with the saturation temperature of R1234yf

Figure 6.10 shows a representative experimental working cycle of R1234yf in the system. An ideal pressure-enthalpy diagram of R1234yf was dotted in the figure, which was divided into the subcooled liquid, the liquid/vapor mixture, and the superheated vapor regions by a saturated liquid curve and a saturated vapor curve. The points 1~4 in the figure correspond to the system locations 1, 2, 3, and 4, as shown in Figure 6.6.

As shown in Figure 6.10, most of the heat generated by the TTV is absorbed by the liquid/vapor mixtures of R1234yf due to the liquid refrigerant's vaporization in the process 1-2. The bubble grows and departs at a high frequency, forming bubbly flow and then slug flow in the microchannels between the plate fins of the MHS. After heating, the liquid/vapor mixtures entirely change to the superheated vapor. Then, the superheated vapor enters a

gas flowmeter. Thirdly, the superheated vapor goes to a compressor and is compressed to higher pressure vapor, resulting in a higher temperature in the process 2-3. Fourthly, the compressed vapor R1234yf flows into a condenser, the superheated vapor changes to the subcooled liquid. The heat accumulated in the previous processes (1-3) is released to the ambient air due to the latent heat of condensation of vapor refrigerant in the process 3-4. Lastly, the subcooled liquid refrigerant returns into the MHS1 through a throttling device, the subcooled liquid refrigerant changes into the liquid/vapor mixtures again, and the pressure drops drastically to a low level (process 4-1).

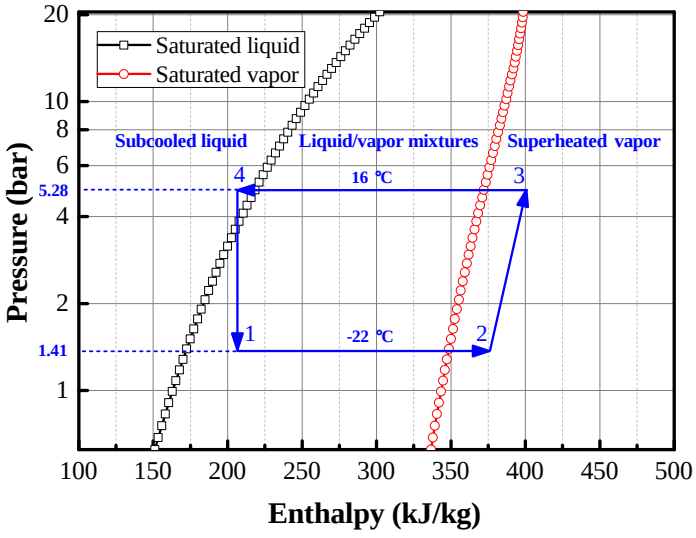


Figure 6.10: Representative experimental working cycle of R1234yf in the system

6.2. RESULTS AND DISCUSSION

6.2.1. COOLING PERFORMANCE EVALUATION WITH TTV1

In this section, the cooling performance of the microchannel thermal management system was evaluated using TTV1. The measured electrical resistance of the TTV1 was 13.76 Ω through a digit multimeter. A 200 V / 60 A DC power supply was adopted to drive the TTV1. The heat fluxes rising from 55 to 526 W/cm^2 were tested by increasing the current from 0.5 to 1.51 A.

Figure 6.11 displays the junction temperature of TTV1 and the pressure of the LP region dependent on the heat flux of TTV1. As seen in the figure, the junction temperature of TTV1 increased almost linearly with the heat flux of TTV1. When the heat flux of TTV1 increased from 55 to 124 W/cm^2 (seen from inset), the junction temperature of TTV1 rose from 8 to 24.3 °C, which was below the ambient temperature of 25 °C. As shown in the

figure, the pressure of the LP region remained about 1.8 bar. Combining Eq. (6.3) with Figure 6.9, the saturation temperature of R1234yf at 1.8 bar was estimated to be -16 °C, so the junction temperature of TTV1 could be lower than the ambient temperature of 25 °C when the heat flux of TTV1 reached 124 W/cm^2. When the heat flux of TTV1 increased to 526 W/cm^2, the junction temperature of TTV1 approached to 119 °C, which was near the allowed highest junction temperature 125 °C. For SiC devices with a higher junction temperature, e.g., 175 °C [4], the heat dissipation of the system could go up to 750 W/cm^2 based on the same level of thermal resistance. Therefore, the thermal management system could dissipate a heat flux of 526 W/cm^2 while maintaining the junction temperature of TTV1 below 120 °C.

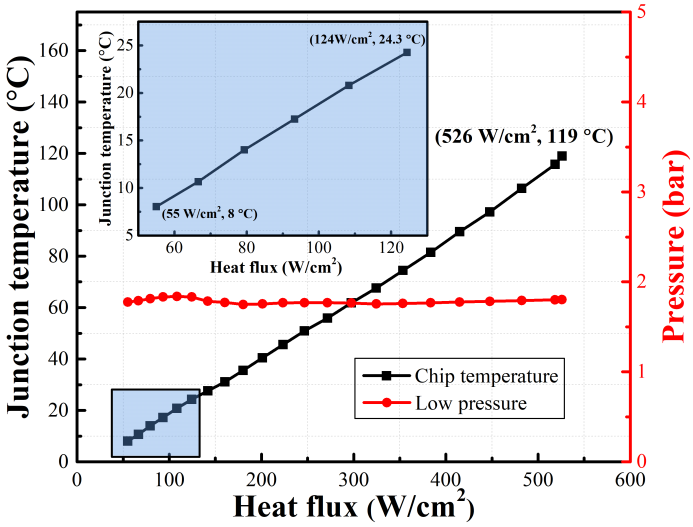


Figure 6.11: The junction temperature of TTV1 and the pressure of LP region dependent on the heat flux of TTV1

6.2.2. Effect of the rotational speed of the compressor

In this section, the effect of the rotational speed of the compressor on the cooling performance was analyzed under the same heat flux of TTV1. The rotational speed of the compressor was changed by adjusting the voltage of a variable resistor connected to the compressor controller. According to Eq. (6.3), when the voltage of the variable resistor decreased from 3.6 to 3.2 V, the speed increased from 2911 to 3374 r/min.

Figure 6.12 illustrates the junction temperature of TTV1 dependent on the rotational speed of compressor under the heat flux of 229 W/cm^2. From the figure, it can be seen that the junction temperature first decreased and then increased with the rotational speed of the compressor. When the rotational speed of compressor reached 3258 r/min, the junction temperature of TTV1 went down to 47.1 °C, which was lowered by 4.4 °C compared with the rotational speed of 2911 r/min. During the system operation, the phase-change heat transfer of R1234yf depended on its flowrate and system pressure drop, which changed

with the compressor's rotational speed. Either too high or too slow flowrate would adversely affect the cooling performance of the MHS. In the following investigations, the rotational speed of the compressor was fixed to be 3258 r/min.

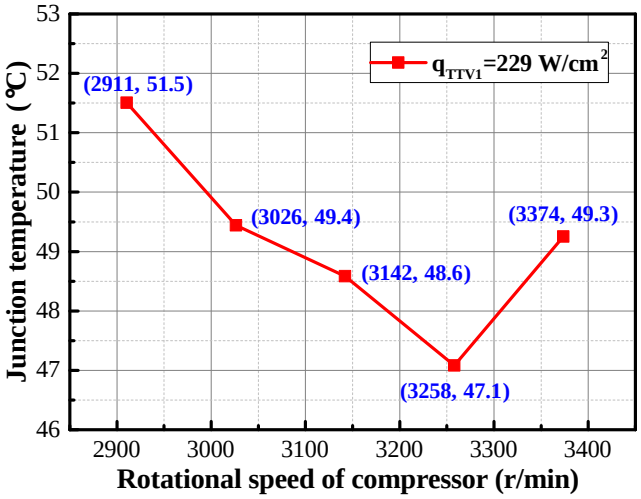


Figure 6.12: Junction temperature of TTV1 dependent on rotational speed of compressor

6.2.3. Effect of the opening of the throttling device

In this section, both the effects of changing the opening of the throttling device at the beginning and the testing process on cooling performance were analyzed, respectively.

For changing the opening at the beginning, by applying current swings from 0.5 to 1.4 A, TTV1's heat flux increased from 55 to 449 W/cm^2. Figure 6.13 shows the pressure drops across the throttling device and junction temperatures dependent on heat flux of TTV1 under small and large openings of throttling device. The pressure drop across the throttling device was affected by its opening. The pressure drops were about 4 and 3.1 bar under the small and large opening, respectively, and a smaller opening led to a higher pressure drop. In other words, the opening of the throttling device can be quantitatively represented by its pressure drop.

As shown in Figure 6.13, when TTV1's heat flux increased from 55 to 353 W/cm^2, the junction temperature under the pressure drop of 4 bar was lower than that under the pressure drop of 3.1 bar. However, when continuing to increase TTV1's heat flux, the junction temperature of the TTV1 under the pressure drop of 4 bar surpassed that under the pressure drop of 3.1 bar. Because only a small portion of refrigerants flew into the MHS1 under the pressure drop of 4 bar, complete phase-change of the fluid refrigerant could occur, the system showed better cooling performance at lower heat fluxes but deteriorated at higher heat fluxes. This phenomenon could be due to the lower flowrate in the MHS1, which could

make the refrigerant approach the dry-out limit at higher heat fluxes. Therefore, increasing the throttle device's opening could increase the flowrate and reduce the junction temperature at higher heat fluxes, thus improving the cooling performance of the system.

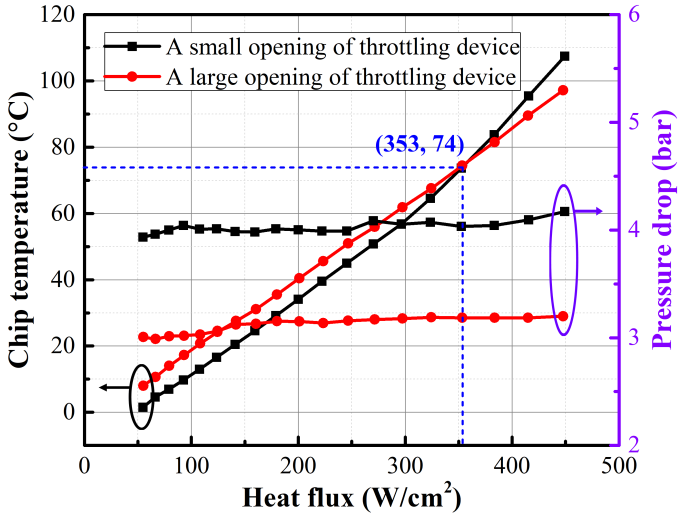


Figure 6.13: Pressure drops across the throttling device and junction temperature dependent on heat flux of TTV1 under different openings of throttling device

For changing the throttling device's opening at the testing process, by applying current from 0.8 to 1 A and then from 1 to 1.1 A, the TTV2's heat flux increased from 152 to 244 W/cm^2, and then from 242 to 297 W/cm^2, respectively. Figure 6.14 shows the effect of the throttling device's opening on the junction temperature of the TTV2, the pressure drop across the throttling device. When TTV2's heat flux increased from 152 to 244 W/cm^2, junction temperature rose from 59.5 to 107 °C, and pressure drop almost kept 2.92 bar. The refrigerant was approaching to the dry-our regime due to the lower flowrate. At this moment, the opening of the throttling device was increased to observe its effect on cooling performance. The junction temperature, pressure drop significantly dropped, which decreased from 107 °C, 2.92 bar to 92 °C, 2.67 bar, respectively. More R1234yf flew into the MHS1, and new phase-change occurred, so the system's cooling performance improved. Therefore, when the refrigerant is approaching the day-out regime, the junction temperature can be reduced by increasing the opening of the throttling device at high heat flux, which allows more refrigerant to MHS and thus improves the cooling performance of the system without reaching the dry-out regime.

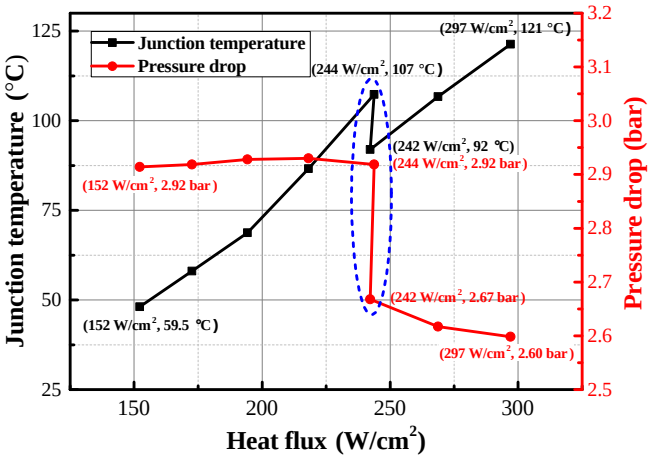


Figure 6.14: Effect of opening of throttling device on junction temperature of TTV2 and pressure drop across the throttling device

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6.2.4. Effect of TTV layout on MHS

In this section, the junction temperature distributions of two groups of TTV2 layouts on MHS1 were studied.

In the first layout, two TTV2s were arranged at the upstream and downstream of the centerline of MHS1, and their heat fluxes increased from 59 to 202 W/cm^2. Figure 6.15 shows the junction temperatures of the two TTV2s. As shown in the figure, when the TTV2's heat flux reached 202 W/cm^2, the junction temperature of TTV2 at the upstream was 11 °C lower than at the downstream. The all fresh cold refrigerant was first heated at the upstream, a part was fully vaporized. The other part was preheated to vaporize to some degree due to the heat spreading effect, unfavorably affecting the cooling performance at the downstream.

In the second layout, two TTV2s were arranged at the lateral middle stream, symmetrically to the centerline of the MHS1, and the heat fluxes increased from 59 to 136 W/cm^2. Figure 6.16 illustrates the junction temperatures of the two TTV2s, which were nearly the same. The junction temperature difference at the two lateral positions was only 3.3 °C, even at the heat flux of 136 W/cm^2. However, compared with the case arranged at the upstream and downstream, the heat dissipation capacity of the system with TTVs arranged at the lateral middle stream was significantly reduced, which was attributed to the reduced flow distribution at the lateral channels instead of centerline channels. Therefore, for a single heater, it is preferred to attach the heater close to the inlet of MHS. For two heaters with the same heat flux, it is suggested to allocate the heaters at the two lateral positions. For multi-heater with different heat fluxes, it is recommended to put the heaters at the centerline in the order of decreasing heat fluxes, with the highest one allocated at the upstream.

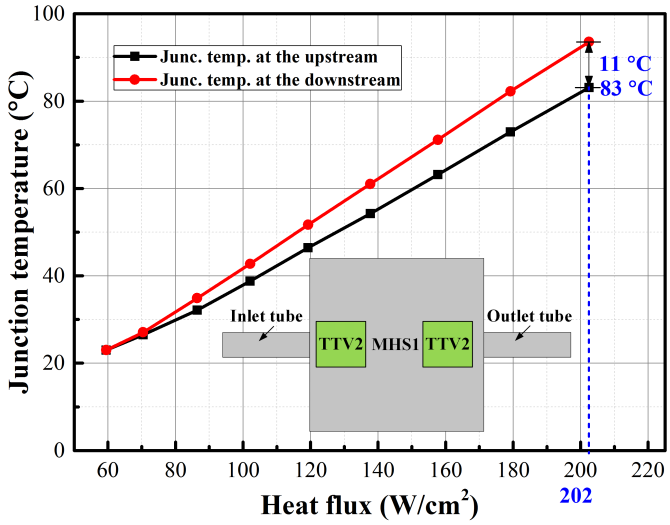

Figure 6.15: Junction temperatures of two TTV2s arranged at Positions A and B of MHS1

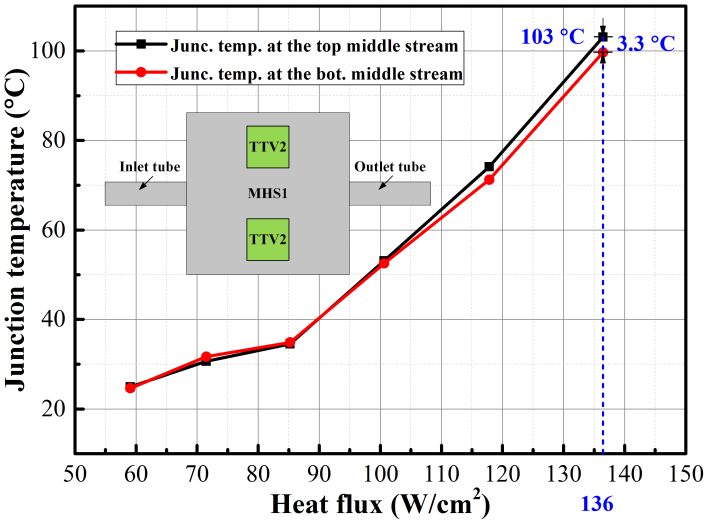

Figure 6.16: Junction temperatures of two TTV2s arranged at Positions C and D of MHS1

6.2.5. EFFECT OF A DOWNSTREAM HEATER

In this section, both MHS1 and MHS2 were used. The effect of a downstream TTV1 on the MHS2 on the pressure drop across the throttling device was first studied. Then, its effect

on the junction temperature of upstream TTV1 on the MHS1 was studied. The downstream TTV1 could be viewed as either a regular heat-dissipating device or a super-heating device. The liquid R1234yf was expected to vaporize more completely in MHS2 upon absorbing heat from the downstream TTV1, thus increasing the enthalpy change of R1234yf before flowing into the condenser.

In the experiment, two 72 V / 1.2 A DC power supplies were used to drive the two TTV1s, respectively. By applying the current from 0.5 to 1.15 A, the heat flux of the TTV1 increased from 55 to 297 W/cm^2.

Figure 6.17 shows the pressure drops across the throttling device dependent on the heat flux of upstream TTV1 when a downstream heater TTV1 is used as a heat-dissipating device and a super-heating one, respectively. As seen from the figure, the pressure drop across the throttling device in the system with a downstream super-heating TTV1 was higher than that with a downstream heat-dissipating one. The pressure difference increased slightly with the heat flux of the upstream TTV1. As discussed in Section 6.2.3, a smaller opening of the throttling device led to a higher pressure drop. Therefore, the downstream heater could be a heat-dissipating device or super-heating device, determined by the pressure drop across the throttling device.

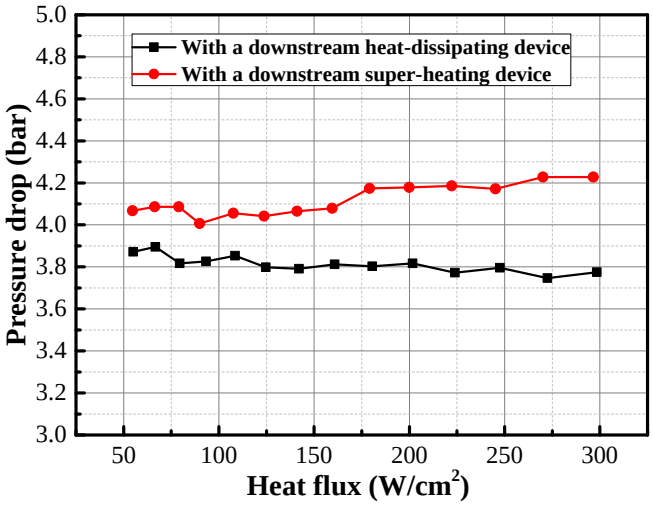

Figure 6.17: Effect of a downstream heater on pressure drop

Figure 6.18 shows the effect of a downstream heater on the junction temperatures of TTV1s. Compared with the upstream TTV1 followed by a regular heat-dissipating TTV1, the junction temperature of the upstream TTV1 followed by a super-heating TTV1 dropped by 8 °C when their heat fluxes increased to 297 W/cm^2. Nonetheless, the junction temperature of the super-heating TTV1 increased evidently, which increased to 92 °C. Because a few refrigerants flew into the MHSs under the higher pressure drop across the throttling device, the liquid R1234yf was vaporized more completely in MHS2 upon absorbing heat

from the downstream TTV1, thus increasing the enthalpy change of R1234yf. Therefore, the upstream TTV1 followed by a super-heating TTV1 showed a lower junction temperature than that followed by a heat-dissipating TTV1. The refrigerant in the MHS2 was preheated to vaporize, unfavorably leading to higher junction temperatures of super-heating TTV1 than heat-dissipating TTV1's junction temperatures. The junction temperatures of the heat-dissipating and upstream TTV1s were close but higher than junction temperature of upstream TTV1 followed by a super-heating TTV1. Because enough refrigerant flew into the MHSs under the lower pressure drop across the throttling device, the phase-change rate was almost the same in the two MHSs. Therefore, the downstream heater on MHS2 could function as a super-heating device while making the junction temperature of the upstream heater at a lower value.

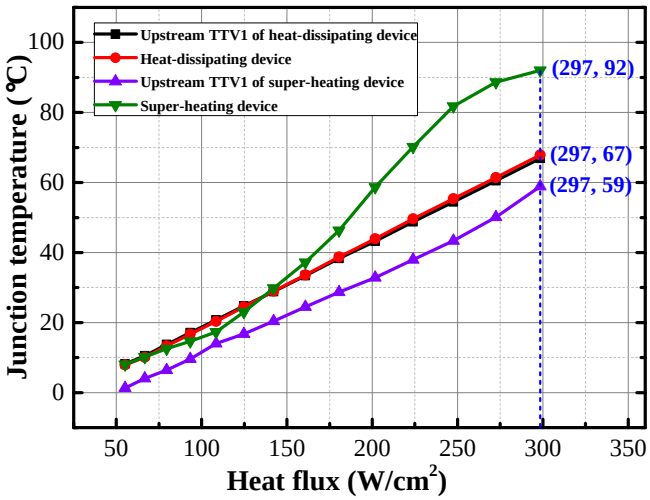

Figure 6.18: Effect of a downstream heater on junction temperature

6.2.6. Discussion on cooling performance enhancement

In this study, various effect factors were studied to improve the thermal management system's cooling performance. However, there is still some room to improve.

- A super-heating device can also be called a sacrificed device, which can improve the cooling performance of the system.
- In this experiment, it is found that the filling amount of R1234yf affected the cooling performance of the system. Either over-filled or under-filled refrigerants would cause deterioration in cooling performance. A more detailed study on the filling amount needs to be conducted.

- Compared with an air-cooled condenser, a liquid-cooled condenser could improve the heat transfer capability from the system to the ambient. A liquid-cooled condenser could be used in the future to achieve much better cooling performance.

- In this experiment, a throttling device with a wide range of openings was used. However, only in the last turn, could the adjustment of the opening affect the cooling performance. In the future study, a programmable controlled valve will be used to achieve precise control of the pressure difference. The maximum operating pressure of the thermal expansion valve should be slightly larger than the highest pressure of the system.

- MHS interior structures and its inlet and outlet will be optimized via computational fluid dynamics simulation. The effect of the mass flow rate of refrigerant on the cooling performance of the system will be studied.

- Single-sided MHS with two-phase flow boiling has been proved to be an effective cooling solution for high heat-flux TTV. If double-sided cooling is adopted, much more heat can be absorbed.

With the improvement mentioned above techniques, the cooling performance of the system could be further improved to address the more demanding heat dissipation level, and overcome even higher heat flux level of 1000 W/cm^2 for the SiC MOSFET power modules.

6.3. SUMMARY

IN this paper, we developed a microchannel thermal management system with the two-phase flow. Single/multiple Si-based TTCs were packaged in the chip window of an organic substrate with the same thickness. Thus, the TTCs in the TTVs could be directly attached to an MHS through a layer of TIM. To quickly realize the phase-change and make full use of the latent heat of vaporization, a low boiling-point R1234yf refrigerant with environmental friendliness was selected to fill the system. The system mainly consisted of two identical Al MHSs, a compressor, a condenser, a throttling device, and several accessory measurement components. The cooling performance of the system with one single-chip TTV1 was first analyzed. The experimental results showed that the microchannel thermal management system could dissipate up to 526 W/cm^2 while maintaining the junction temperature of TTV1 below 120 °C. For SiC devices with a junction temperature, e.g., 175 °C, the current system is predicted to dissipate the heat flux as high as about 750 W/cm^2. Then, the effects of the rotational speed of the compressor, the opening of the throttling device, TTV layout on MHS1, and a downstream heater on MHS2 on the cooling performance of the system were analyzed sequentially. The study showed that the opening of the throttling device had a significant effect on cooling performance. For the multi-module system, the chip at the upstream had the best cooling performance. On the other hand, the downstream TTV on MHS2 could function as a super-heating device instead of a heat-dissipating device, making the junction temperature of upstream TTV at a low value.

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7

Conclusions, contributions, and recommendations

In this chapter, first of all, the main conclusions are drawn. Then, primary contributions are summarized. Lastly, several recommendations for future work are discussed.

7.1. Conclusions

In this dissertation, there are four major developments based on the challenges proposed in Chapter 1.

For **material selection**, SiC MOSFET (CPM2-1200-0080B) from CREE and organic substrate materials, including BT laminate (HL832NSF) and BT prepreg (GHPL-830NSF) from Mitsubishi Gas Chemical, were selected. I-V, C-V, and gate charge characteristics of the SiC MOSFET were first analyzed via a custom fixture. The results showed that compared with Si devices, SiC MOSFET had output characteristics of non-saturation, existed two distinct points in the curve of Miller capacitance versus drain-source voltage, and displayed a non-flat Miller platform. Then, thermal stability, dielectric breakdown, thermo-mechanical performance, and cure kinetics of the organic substrate materials were characterized. The results indicated that the organic substrate materials could withstand the high temperature of 300 °C and the high voltage of 46.9 kV. The glass transition temperature was as high as over 260 °C, and the coefficient of thermal expansion was matching with SiC. Both one-hour curing at 280 °C and two-hour curing at 210 °C could ensure the full cure of the BT prepreg.

For **packaging technology**, a novel fan-out panel-level packaging technology was proposed for a phase-leg SiC MOSFET power module. The high- and low-side SiC MOSFETs were embedded in an organic substrate, interconnected by double-sided redistribution layers (RDLs) and through vias, finally protected by double-sided soldermasks. Compared with current embedded packaging technologies for Si and GaN devices, the proposed packaging structure has unique merits, such as structure symmetry and double-sided cooling. Then, the electrical, thermal, and thermal-mechanical simulations were conducted to evaluate and optimize the fan-out packaging performance. Lastly, a detailed fan-out panel-level packaging process for the phase-leg SiC MOSFET power module was introduced. Three essential packaging processes, including exposure and development of photo imageable dielectric, panel-level physical vapor deposition (PVD), and double-sided RDL interconnection, could replace conventional laser drilling, chip/wafer-level PVD, and wire-bonding, respectively.

For **performance characterization**, the static and dynamic characteristics of the fan-out SiC MOSFET power module were studied. First of all, the effects of the fan-out packaging on I-V, C-V, and gate charge characteristics of SiC MOSFET were analyzed via two custom fixtures. The experimental results showed that the SiC MOSFET's I-V non-saturation characteristics were more evident after packaging, and higher drive voltage was required to fully turn-on SiC MOSFET due to the extension of the non-flat Miller plateau. Then, the switching performance of the fan-out phase-leg SiC MOSFET was evaluated via double pulse tests. A phase-leg that is composed of two TO-247 discrete packages was used as a benchmark. The experimental results showed that the fan-out packaging had smaller voltage overshoot and current oscillation at turn-off transient, and smaller voltage oscillation and current overshoot at turn-on transient than TO-247 package.

For **heat dissipation**, a microchannel thermal management system with the two-phase flow is presented. Single/multiple Si-based TTCs were packaged in the chip window of an organic substrate with the same thickness. Thus, the thermal test chips in the thermal test vehicles (TTVs) could be directly attached to a microchannel heat sink (MHS) through

a layer of thermal interface material. To quickly realize the phase-change and make full use of the latent heat of vaporization, a low boiling-point R1234yf refrigerant with environmental friendliness was selected to fill the system. The system mainly consisted of two identical Al MHSs, a miniature compressor, a condenser, a throttling device, and temperature, pressure, and accessory measurement components. The cooling performance of the system with one single-chip TTV1 was first analyzed. The experimental results showed the microchannel thermal management system could dissipate up to 526 W/cm^2 while maintaining the junction temperature of TTV1 below 120 °C. For SiC devices with a junction temperature, e.g., 175 °C, the current system is predicted to dissipate the heat flux as high as about 750 W/cm^2. Then, the effects of the rotational speed of the compressor, the opening of the throttling device, TTV layout on MHS1, and a downstream heater on MHS2 on the cooling performance of the system were analyzed sequentially. The study showed the opening of the throttling device had a significant effect on cooling performance. For the multi-module system, the chip at the upstream had the best cooling performance. On the other hand, the downstream TTV on MHS2 could function as a super-heating device instead of a heat-dissipating device, making the junction temperature of upstream TTV at a low value.

7.2. CONTRIBUTIONS

In this dissertation, major contributions include as follows.

- Wire-bondless and hybrid packaging schemes for Si and SiC power modules were reviewed.
- Electro-thermo-mechanical properties of the organic substrate materials were thoroughly characterized to support the packaging process development of the fan-out SiC MOSFET power module in an organic substrate.
- A novel fan-out phase-leg SiC MOSFET power module in an organic substrate was developed. Three new packaging processes, including PID exposure and development, panel-level PVD, and double-sided RDL, were proposed to replace the conventional laser drilling, PVD, and wire-bonding technologies. Laser-induced damage could be avoided. The die metallization before packaging is not necessary, and any devices can be deposited via panel-level PVD.
- Two custom fixtures for static characterization of SiC MOSFET bare die and the fan-out packaging were developed. I-V, C-V, gate charge, and other characteristics could be measured according to specific applications. The effect of the fan-out packaging on the performance of SiC MOSFET could be accurately characterized.
- Double pulse test was used to evaluate and compare the switching characteristics of SiC MOSFET in the fan-out phase-leg power module and the standard TO-247 discrete device.
- A novel microchannel thermal management system with the two-phase flow for power electronics over 500 W/cm^2 heat dissipation was developed, which paved the way for the research of thermal management of SiC MOSFET power module.

7.3. Recommendations

Although significant contributions have been made in the Ph.D. project, there is still many work to do in the future. Some recommendations are as follows.

- **Optimizatin:** To improve the thermal and thermo-mechanical performance of the fan-out SiC MOSFET power module, the packaging structure optimization and packaging process will be further conducted.

- **Reliability:** Reliability test, including thermal and power cycling, high-temperature storage, and highly accelerated stress test, failure analysis, and fast lifetime prediction of the fan-out SiC MOSFET power module, will be performed.

- **Thermal management:** Single-sided Al-based MHS with the two-phase flow has been proved to be an effective cooling solution for high heat-flux electronics. The double-sided two-phase flow cooling will be able to absorb much more heat. Internal structure optimization of the MHS, precise control of the system, and Si-based microchannel heat sink with the two-phase flow will be studied. Besides, a trade-off analysis between packaging design and cooling costs will be considered from the perspective of applications. A passive cooling solution could satisfy the cooling requirement of SiC high-temperature packaging, thus decrease the module's size and weight and reduce the cooling costs. All above mentioned is to solve the heat dissipation of electronic devices. The heat is finally dissipated to the ambient, which is a waste of energy. On the contrary, the Si-based thermoelectric generator (TEG) can recycle waste heat into electrical power. As an emerging energy-saving and emission-reduction technology, the TEG has spread application prospects.

- **Application:** Demonstration and practical applications of the phase-leg SiC MOSFET power module based on the fan-out packaging technology will be conducted. As a basic unit, it can be used in the converter and inverter power systems. The switching characteristics of SiC MOSFETs in the package will be evaluated in the real power electronic system.

- **Technology transfer:** This packaging technology can be applied to GaN, RF, and other WBG/ultra-WBG devices. The high-frequency properties of these devices can be fully exploited. The package has the features of low parasitics, miniaturization, and lightweight.

- **SiP^2:** With the ever-increasing need for more compact power electronic systems, a system in power package (SiP^2) based on the fan-out organic substrate packaging technology will be one of the developing trends in the middle-power module. The embedding power chips offer the possibility to place gate drivers and passive components on the top layer of the substrate. They can also be embedded in the PCB together with power devices. A shorter conduction loop results in a smaller parasitic resistance that reduces the conduction losses. A smaller parasitic inductance helps to maintain a smaller voltage overshoot and reduce the switching loss.

- **3D SiP^2:** A 3D SiP^2 based on the organic and DBC substrates will be developed to make full use of the features of SiC MOSFET in the high-temperature, high-voltage, high-frequency, and high-power applications. The next-generation power module for operating above 250 °C/6.5 kV will be investigated. The bonding technologies, e.g., Cu/Ag nanoparticle sintering, transient liquid phase, will be used in the chip-to-DBC and DBC-to-heatsink to reduce the contact thermal resistance. The thermal resistance of bonding layers will be analyzed.

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List of publications

Journal papers

1. **F. Hou**, H. Zhang, D. Huang, J. Fan, F. Liu, T. Lin, L. Cao, X.J. Fan, J.A. Ferreira, and G.Q. Zhang, "Microchannel Thermal Management System with Two-Phase Flow for Power Electronics over 500 W/cm^2 Heat Dissipation," *IEEE Transactions on Power Electronics*, 2020.

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