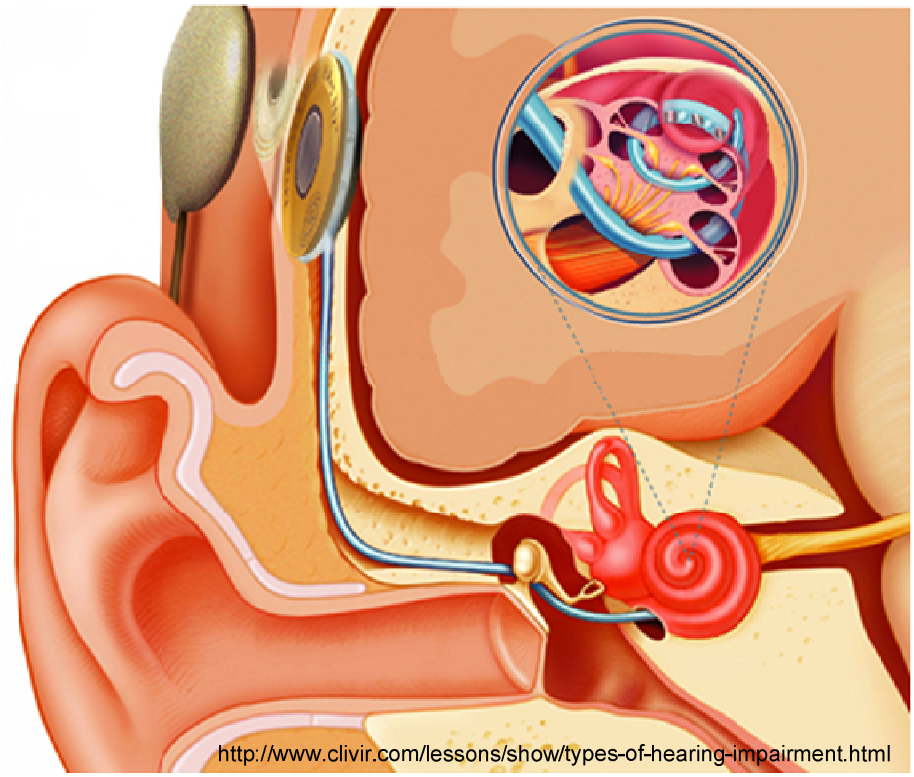
A FRONT-END FOR SENSING THE STIMULATION AND RESPONSE OF AUDITORY NERVE CELLS

by

C.J. Bes



TU Delft Delft University of Technology

Challenge the future

“So many of our dreams at first seems impossible, then they seem improbable, and then, when we summon the will, they soon become inevitable.”
Christopher Reeve

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A FRONT-END FOR SENSING THE STIMULATION AND RESPONSE OF AUDITORY NERVE CELLS

by

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A thesis submitted to the Department of Microelectronics,
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Abstract

This thesis describes the design of a new readout system for cochlear implants.

At the moment, about 30 million people worldwide are suffering from hearing loss. Most people are helped with a simple hearing aid that just amplifies sounds coming to the ear. However, if the hearing loss is too severe, these aids will not help. More than 100.000 people worldwide need a more complex device in order to let them hear again. A cochlear implant is such a device and is partially implanted inside the human body.

Today's implants are not able to let people hear sounds as people hear them with normal hearing. The main cause can be found in the stimulation accuracy of the auditory nerve fibres. To improve this accuracy, research should be performed in order to improve stimulation algorithms, increase the amount of electrodes and focus the stimulation field of the electrodes.

Researchers now reached the limitations of existing neural response readout systems needed for reading out the evoked compound action potential for their research. These limitations urge the need for a new neural response readout system having a dynamic range of 126dB, that is small, power efficient, has noise levels under 10µV and can handle input signals exceeding the supply voltage. The readout system will be able to read out 256 electrodes and is implemented in a MEMS cochlear implant.

Existing techniques do not offer solutions to meet the above specifications. An overall readout system design is proposed based on compensation containing an input system, multiplexer, compensation circuit, amplifier and an analog to digital converter (ADC). Because the overall readout system is too big to design in one thesis, only the input system is handled.

Existing techniques do not offer solutions to handle input signals above supply voltage being compact, power efficient, have high dynamic range and have a low noise contribution. A new technique based on additive instantaneous companding in order to record the evoked compound action potentials from the stimulated auditory nerve is proposed.

Three alternative circuit implementations are proposed, two voltage domain implementations and a charge domain implementation. The proposed input systems are designed to be implemented in AMIS I3T25 (high voltage) CMOS technology. The charge domain circuit implementation is very promising only using 70 components, having a bandwidth of 10kHz, and a noise level of 1.1pV. It is capable to readout input signals which are bigger than the supply voltage while the signal information is preserved. For checking the correct working of the circuit, a signal reconstruction is performed. In addition, this charge domain implementation is never reported before in literature.

Acknowledgement

In this thesis, the result of my research on improving neural response readout circuitry is presented. It started with an extensive search through many papers, books and articles. It took a lot of effort to turn this into a system design and, finally, into a circuit design. Hopefully, this research will be useful in developing improved hearing aids and thereby improving the quality of life of patients in the near future.

During my thesis work I have been supervised by Wouter Serdijn. I would like to thank him for all his effort he has done in guiding me through my thesis work, the nice meetings and his support.

The cooperation with the Leiden University Medical Center provided me with a complete view on the medical aspects essential for this thesis. I would like to thank Johan Frijns and Jeroen Briaire for guiding me through these medical aspects and the opportunity to attend a surgery in which a cochlear implant is placed in a patient.

My daily work was done at the 18th floor of the EWI building led by John Long. Here, I had a very good working environment and a very nice team of people who helped me to solve the problems I faced during my thesis. I would like to thank all these people for all their support.

As a biomedical group, the students in this group were not just fellow students. The group was unique. It was a very close group and the people were supporting each other closely. I would like to thank those people for being part of this group.

During my study in Delft Marion de Vlieger, the secretary of the 18th floor, was always there to make a small talk or help me with finding my way through the administrative papers. I would like to thank her for all her help and support.

Finally, I would like to thank my father Kees, mother Zilla and my four brothers Dick, David, Daan and Bart for their support and help during this thesis.

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Chapter 1: The human hearing system

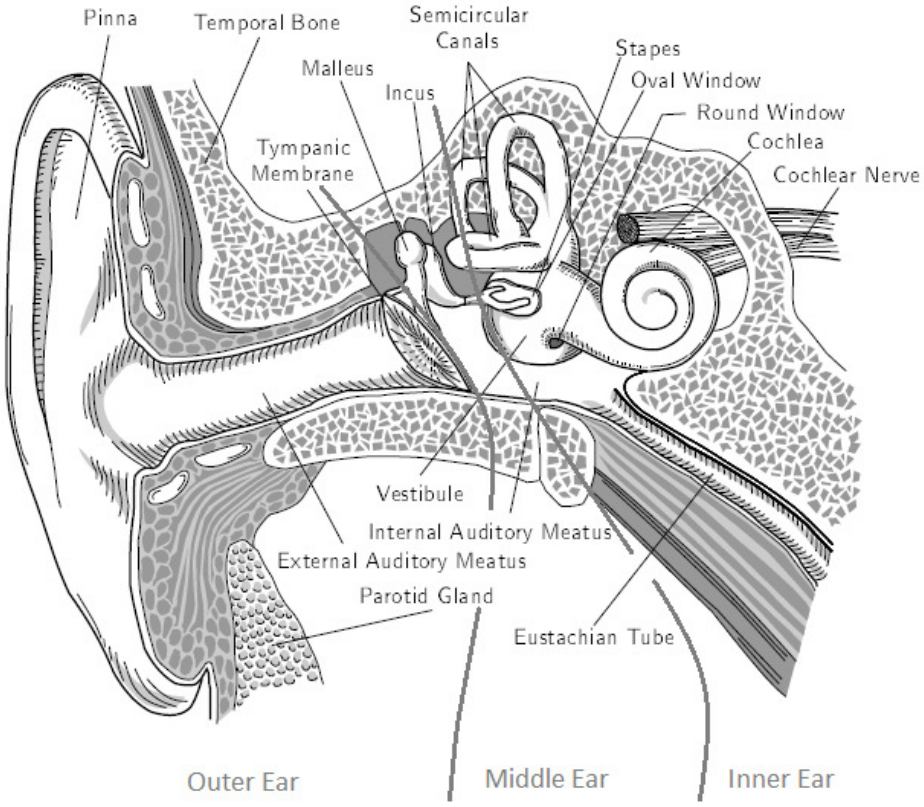

Figure 1.1: Anatomy of the ear [1]

While explaining the working of the ear, the path of the acoustic sound will be followed. Figure 1.1 shows the ear in which three sections can be distinguished: the outer ear, middle ear and inner ear. The outer ear consists of the pinna. It is visible for people and is the entrance to the ear. Going further to the inside of the ear we arrive at the external auditory meatus. Here, the acoustic sound is guided to the tympanic membrane or also called the ear drum. The ear drum is actually a thin membrane. The membrane will start to vibrate at the rhythm of the sound. After the ear drum the middle ear, consisting of a network of three bones, is reached. The first bone is the malleus or hammer. After the hammer, there is the incus or also called the anvil. The last bone is the stapes or also called the stirrup. Together they work as a lever in order to amplify the vibrations of the eardrum. In combination the bones double or triple the force of the vibrations at the eardrum. The muscles of the middle ear modify the performance of this lever system as an amplifying unit. They act as safety devices to protect the ear against excessively large vibrations from very loud sounds - a sort of automatic gain control. The inner ear consists of the cochlea, cochlear nerve and semicircular canals. The entrance into the cochlea is called the oval window, consisting of a membrane covering an opening in the bony case of the cochlea. In the cochlea, the vibrations will travel through the cochlear channels, which are filled with fluid. Mechanical vibrations are transformed to electric action potentials by the organ of Corti located in the cochlea. The action potentials are transported trough the auditory nerves to the brain [2]. To get a better understanding of the conversion of mechanical vibrations to action potentials, next section will tell more about the cochlea and its subparts.

1.1. The cochlea

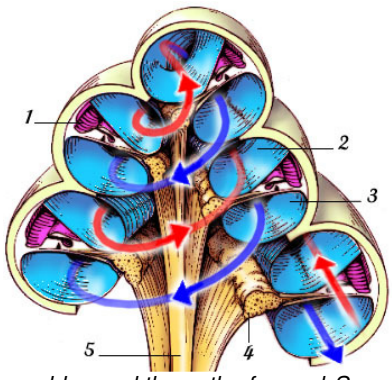

Figure 1.2: Cross section of the cochlea and the path of sound, Source: S. Blatrix, R. Pujol INSERM-Montpellier

The cochlea is an organ looking like the house of a snail. Inside there are two ducts which are filled with fluid. The entrance for sound of the cochlea is called the oval window and is located at the beginning of the cochlea. The sound waves will travel through the cochlea as illustrated by the arrows in figure 1.2. The red arrow indicating the direction of the mechanical vibrations is coming from the oval window and will go all the way up to the top of the cochlea. There, it turns into the blue arrow indicating the direction of the mechanical vibrations which travel back down in the cochlea ending at the round window. The middle part of the cochlear duct (1) contains endolymph fluid. The cochlear duct, in which the sound goes to the upper side of it (2) is called the scala vestibuli. The way down to the round window (3) is the scala tympani. The scala vestibuli and scala tympani contain perylymph. At point (4), the spiral ganglion is located. Finally, the auditory nerves are located at (5). The auditory nerves go through the middle part of the cochlear duct to the brain. Zooming in to a single turn of the cochlea, the drawing depicted in figure 1.3 is obtained. Here, again the cochlear duct can be distinguished. This duct is isolated from the scala vestibuli by the Reissner's membrane and from the scala tympani by the basilar membrane. Inside the cochlear duct, the organ of Corti is present. The organ of Corti is covered by the tectorial membrane which is floating in the endolymph. From the organ of Corti, the nerve fibres go into the spiral ganglion through the bony shelf [3].

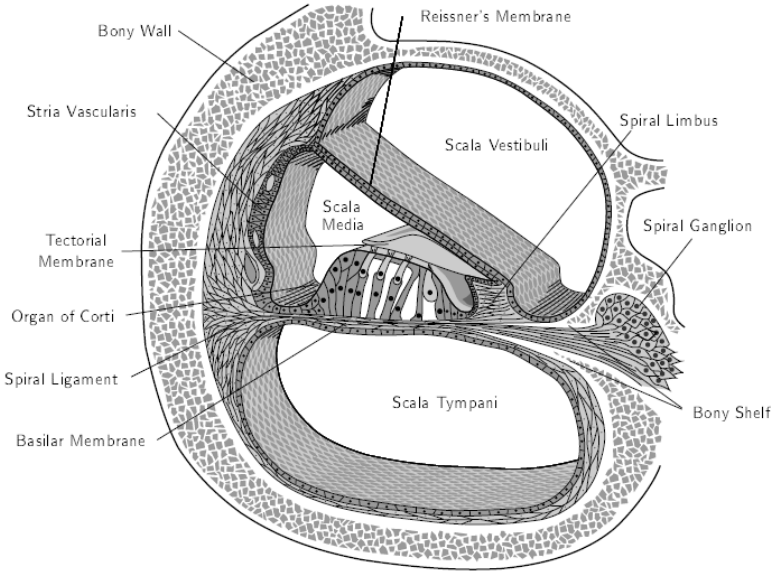

Figure 1.3: Cross section of a single turn of the cochlea [1]

1.1.1. The organ of Corti

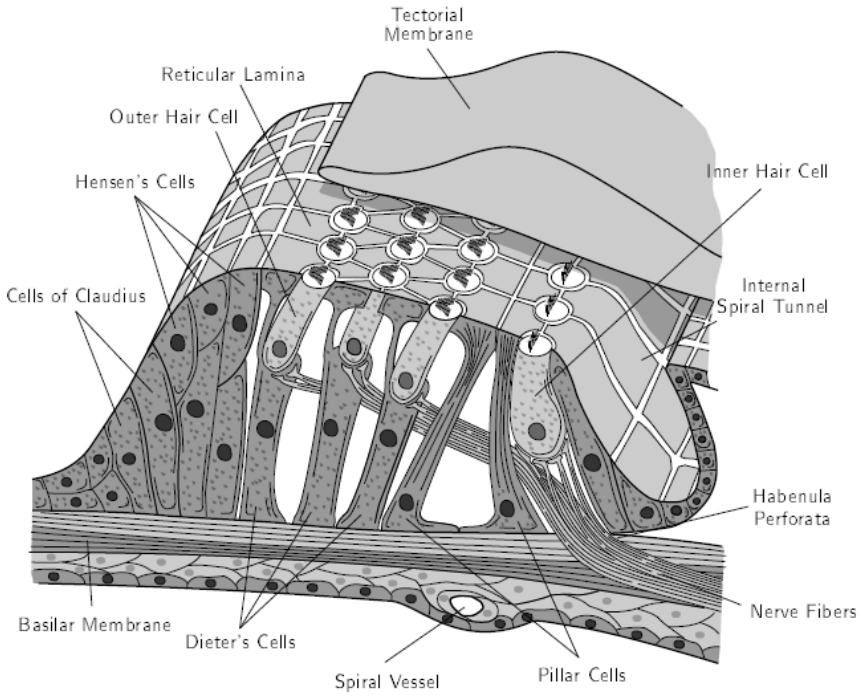

Figure 1.4: The organ of corti [1]

The organ of Corti is the actual sensing element which converts the vibrations due to sound to the neural pulses. The organ of Corti is depicted in figure 1.4. Inside the organ of Corti, two types of hair cells can be distinguished; the inner hair cell and the outer hair cell. The tectorial membrane covers the organ of Corti. It actually covers the hair cells embedding the tips of the tallest outer hair cell called stereocillia. Due to pressure at the Reissener and Basilar membrane, the tectorial membrane is moved. The tectorial membrane moves over the hairs of the hair cell which is connected to the auditory nerve [3].

1.1.2. Conversion of mechanical force to electricity

Figures 1.5 and 1.6 show the hair cells located inside the organ of Corti. The hairs located on the hair cells are called stereocilla (2). Due to the movement of the stereocilla, action potentials are generated and passed to the auditory nerves (4) and (5) for the Inner Hair Cell (IHC) and to (6) and (7) for the Outer Hair Cell (OHC).

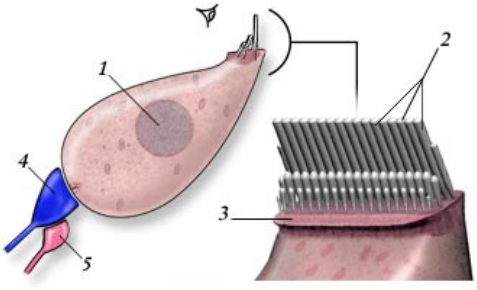

Figure 1.5: Inner Hair Cell (IHC). Source: S. Blatrix, R. Pujol, INSERM-Montpellier

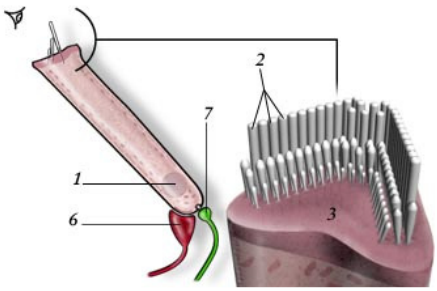

Figure 1.6: Outer Hair Cell (OHC). Source: S. Blatrix, R. Pujol, INSERM-Montpellier

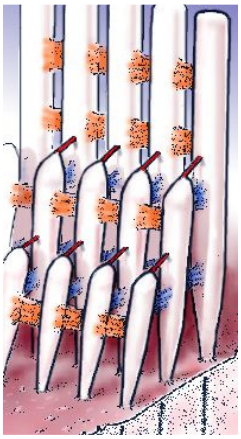

Figure 1.7: Stereocilla with the connections between them. Source: S. Blatrix, R. Pujol, INSERM-Montpellier

The stereocilla are connected to each other by very small connections as is depicted in Figure 1.7. The conversion of mechanical force to an electrical pulse takes place by the exchange of ions. If the hairs are moved, ions will move through the stereocilla into the hair cell. The cell will depolarize producing a stimulus to the auditory nerves. When the moving of the stereocilla is finished, the hair cell will restore to its initial situation.

1.2. Hearing problems

In the previous sections, normal functioning of the auditory system is described. Sometimes, it occurs that one part of the ear is malfunctioning, damaged or not present. This problem can be classified into three categories [4]:

- Conductive hearing loss
- Sensorineural hearing loss
- Mixed hearing loss

Conductive hearing loss

Conductive hearing loss occurs when sound is not conducted efficiently through the outer ear canal to the eardrum and subsequently to the tiny bones, or ossicles, of the middle ear. Conductive hearing loss usually involves a reduction in sound level, or the ability to hear faint sounds. This could be corrected or solved with a hearing aid, which only amplifies the sounds. If this does not suffice, a cochlear implant can be considered. Conductive hearing loss is the most common form of hearing loss.

Sensorineural hearing loss

Sensorineural hearing loss occurs when there is damage to the inner ear (cochlea) or to the nerve pathways from the inner ear (retro cochlear) to the brain. Sensorineural hearing loss cannot be corrected medically or surgically. It is a permanent loss.

Mixed hearing loss

Sometimes conductive hearing loss occurs in combination with sensorineural hearing loss. In other words, there may be damage in the outer- or middle ear and in the inner ear (cochlea) or auditory nerve. When this occurs, the hearing loss is referred to as mixed hearing loss.

1.3. Hearing aids

To repair the hearing loss mentioned in previous section, a hearing aid can be used. There are two general groups of hearing aids:

- Conventional hearing aids (sound amplifier)
- Cochlear implanted hearing aids

This thesis will handle the cochlear implanted hearing aid, so the conventional hearing aid will not be discussed in more detail.

1.3.1. Cochlear implanted hearing aids

A cochlear implant is based on the principle of electrically stimulating the auditory nerves. It basically takes over the stimulating function of the hair cells. The auditory hair cells still present in the cochlea will be bypassed. Figure 1.8 shows a cochlear implant as is used today. A schematic of the subparts of a cochlear implant is depicted in Figure 1.10. Most implants work according to the same principle. The implant can be divided into separate system blocks:

- Microphone pre-amplifier / audio front-end
- AGC
- Channels
    - Band Pass Filter
    - Envelope detector
    - A-to-D converter
- Shift register
- RF-link
- Electrode

Figure 1.8: Cochlear implant. Source: Advanced Bionics; http://www.advancedbionics.com /CMS/Products/Harmony-System.aspx

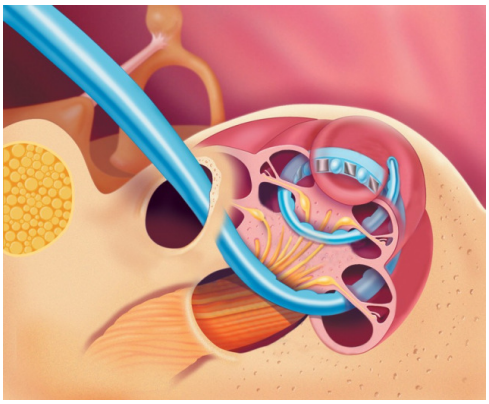

Figure 1.9: Electrode. Source: http://www.lumc.nl/ meer_cochleaire_implan tatie.html/Care_System/ Cochlear_Implant/

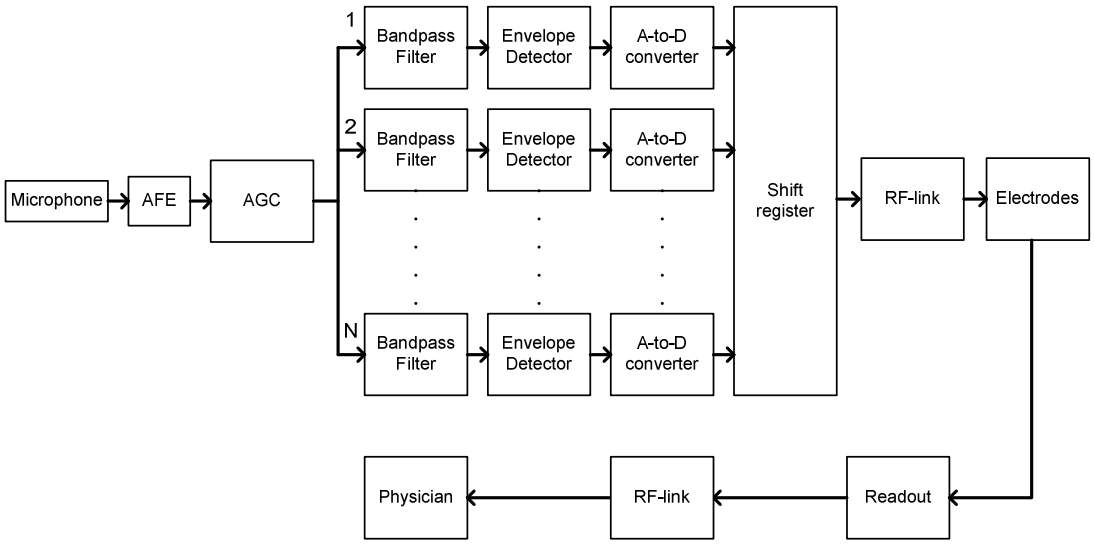

Figure 1.10: Overall architecture of an analog cochlear implant.

Microphone pre amplifier / audio front end

The microphone preamplifier will sense acoustic signals and convert these signals into the electrical domain. The microphone membrane has the same functioning as the ear drum. There are several ways to implement a microphone [5] [6]. The audio front end (AFE) amplifies and conditions the signals coming from the microphone.

AGC

An Automatic Gain Control (AGC) is needed in cochlear implants in order to protect the ears from overload just like the malleus, incus and stapes do. When the incoming signal is too large, it will damage the hearing even further. An AGC is a device that can adapt its gain to the incoming signal. It takes care of guaranteeing a constant output signal level over a certain input range [6] [7].

Speech processing

A speech processor consists of a certain amount of channels. Each channel represents a certain position in the cochlea and thereby a certain frequency. After the automatic gain control, the signal will be guided through those channels. In these channels the signal will be processed into a signal which is suitable for the electrodes. In order to do so, each channel consists of:

- Band Pass Filter
- Envelope detector
- A-to-D converter

Band Pass Filter

The band pass filter selects the proper frequency for the channel. The electrode belonging to the channel will only stimulate the cochlear part according to the signal strength at that frequency [8].

Envelope detector

In order to get a good signal power estimation, for each channel an envelope detector is added. Mostly it will consist of a transconducting rectifier, followed by a current-mode peak

detector. Together this will take care of determining the amplitude of the signal [6]. This signal is fed to the A-to-D converter.

A-to-D converter

The A-to-D converter converts analog signals into digital signals in order to prepare it for sending with the RF-link to the implanted part. A human is able to distinguish 8-50 electrode stimulation steps per electrode [6] [9]. 50 steps can be achieved with a 5-bit A-to-D converter. The A-to-D converter will convert the signal of the envelope detector to a corresponding digital level.

This is done in every channel in the cochlear implant. All channels will go to a shift register.

Shift register

The shift register will scan all channels and convert the parallel input to a serial output. The signal is now prepared to be transported to the implanted part of the cochlear implant. The output of the shift register is coupled to the RF-link.

RF-link

To transfer signals to the implanted part of the cochlear implant and back, an RF-link is used. The speech processor applies the multiplexed signal to the RF transmitter. The multiplexed signal is send through the skin to the implanted RF receiver. It is located at the skull behind the ear underneath the skin. Then, the signal is de-multiplexed and by a current source applied to the electrodes which are located in the cochlea. Readout signals are transferred from the implanted part to the external part.

Electrode

Figure 1.9 shows how the electrodes are placed in the cochlea. The array of electrodes consists of a small appendix which fits the form of the cochlea. Mostly, the appendix will consist of 16 to 24 electrodes. Each of them is placed at a certain position and may cover a range of frequencies due to the physiognomy of the cochlea. By applying an electrical current via an electrode, the cochlear implant directly stimulates a group of nerves and thus creates the ability to hear a certain frequency. Not all the electrodes are placed in the cochlea. Generally, we can find one or two extra-cochlear electrodes.

Readout

The readout enables physicians to record the neural responses coming from the cochlea. From the electrode, the neural response signal goes to the readout circuitry. Here, the signal is conditioned and prepared for sending back by the RF-link.

Now-a-days not only cochlear implants, having a part outside the body and a part inside the body are available, also implants which are completely implanted inside the body are available. The microphone is then placed in the external ear channel.

1.3.2. Recording neural responses

A neural response is initiated by a stimulus coming from the cochlear implant. After the stimulus, the neural response becomes visible and can be recorded by the readout system. Modern cochlear implants have a neural recording system on board. This recording system is used for two purposes:

- Fitting of the implant
- Serving scientific research

Fitting of the implant

Fitting the cochlear implant to the patient gives the patient the best possible hearing condition/situation. Neural responses are measured and the amplitude of the neural response is determined. From this and subjective data (spoken feedback of the patient himself), the optimal stimulation currents are determined.

Scientific research

Neural response data is used for gaining a better understanding of the human cochlea. Although a lot of research is performed on this topic already, there is still not a complete understanding of the working of the cochlea. Results are used for developing better stimulation methods and the further development of the hardware of cochlear implants.

1.4. Limitations of current implants

At the moment, cochlear implants are becoming more and more sophisticated devices. The size is reduced and power consumption is brought down significantly. Besides these achievements, there are still a lot of issues to be solved. As the cochlear implant evolves, physicians get better results which give them new insights in cochlear stimulation [10]. These new insights demand new improvements for cochlear implants. Stem cell therapy is developing which makes it possible to grow auditory nerves closer to the implant in the future [11]. This enables the usage of more electrodes. Medical doctors like to have an implant equipped with 256 electrodes. This can not be achieved with techniques used in modern implants. The biggest issue is the amount of wires which will be needed in order to connect all 256 electrodes. The resulting wire bundle will be too thick to fit inside the cochlea. In order to be able to increase the amount of electrodes, a solution has to be found for this problem.

Another issue which should be overcome is the improvement of measurement results enabling audiologists to obtain more accurate information. Current implants give very poor measurement results due to electrical noise and Electro Magnetic Interference (EMI). Todays implants limit the development of new stimulation algorithms and prevent more detailed research. Many averaging cycles must be performed in order to get reasonable data. If stimulation of the nerves becomes too low, neural responses can not be read out; not enough nerve fibres will fire. The neural response will drown in the noise. Neural responses can already occur during stimulation of tissue [12]. During stimulation the readout amplifier is saturated, which means that during stimulation the input of the amplifier becomes too big. The amplifier output will start clipping until the input signal becomes small again. During this clipping, no neural response can be read out.

During measurement, the RF-link is turned off in order to reduce EMI at the electrodes. Moreover, it is not possible to adjust settings. Medical doctors like to be able to adjust these settings during measuring and monitor neural responses in real-time. In order to achieve this, the RF-link has to be on. State of the art implants used today do not have this possibility.

The patient must always carry an external battery with him for powering the implant. This is due to the high power consumption which is still needed in cochlear implants. At the moment, the first fully implantable cochlear implants are presented on the market. These implants are able to function for about 2 or 3 days on one battery charge before recharging is required. If a battery is

able to be recharged up to 1000 times, an average lifetime can be achieved of approximately 7 years. Medical doctors like to have an implant which is able to use one single rechargeable battery over a period of at least 10 years. This implies that the power consumption of implants have to be brought down drastically.

1.5. Thesis organization

This thesis will handle the development of a new readout system applicable in a cochlear implant using a large amount of electrodes (256). The readout system not only will readout the neural response, but will also multiplex the signals resulting in a reduction of the amount of wires needed.

Chapter 2, handles two subjects. First of all, tissue modelling is discussed. An electrical circuit representation of tissue will be found with its component values. Then, the characterisation of signals is performed. They can be subdivided into three groups. Finally, measurement algorithms will be discussed.

Chapter 3 will discuss several front end systems. First, existing systems and their shortcomings are discussed. A readout system in today's cochlear implants is explained, followed by an experimental setup developed at the Leiden University Medical Centre. Then, a new system design is proposed and system level simulations are performed using the Cadence design suite. The system consists of several blocks. At the input an compressor block is present. Because the development of the complete system will take too much time to fit into this thesis, only the input compressor based on the newly developed principle of additive companding will be implemented. This is the most difficult and challenging part of the readout system.

Chapter 4 discusses the general implementation of the input compressor. Section 4.1 discusses existing solutions for the input circuitry like resistive dividers, switched capacitor techniques, multiplicative companding, folding ADC and ΣΔ ADC's. Then, a new technique called additive companding is proposed. A system design for the additive companding technique is made and system level simulations are performed using cadence.

In Chapter 5, the input compressor system is implemented as a switched circuit in the voltage domain. First, an ideal circuit design is proposed, followed by the implementation in the AMIS I3T25 CMOS technology. Then, simulation results will be discussed. Finally, limitations of the circuit will be discussed.

Chapter 6 discusses an alternative implementation of the input compressor system in the voltage domain by using parallel capacitances. Charge distribution between the capacitances have to solve the limitations of the circuit described in chapter 5. A circuit implementation of this concept in the AMIS I3T25 technology is discussed. Simulation results will be discussed. Finally, limitations of the circuit will be discussed.

In chapter 7, a charge domain implementation of the additive companding technique is discussed. A circuit concept will be given followed by the implementation in the AMIS I3T25 CMOS technology. Simulations are performed and discussed.

Chapter 8 discusses a comparison between the three implementations of additive companding in this thesis. Recommendations will be given about how to continue with the work including the implementation of all system blocks of the system discussed in Chapter 3.

Chapter 2: Tissue modeling and signals characterization

In this chapter, the electrode and tissue behavior as a electric source is investigated. First, the modeling of tissue will be discussed starting with the bioelectricity mechanism of nerve cells, working towards an electrical model of tissue and the electrode-tissue interface used for stimulating the auditory nerve. Then, signals generated by the tissue going to the electrodes will be discussed and identified.

2.1. Tissue modeling

Tissue is basically built-up by several types of cells. Modeling of tissue is very important in order to predict the electrical behavior of tissue. Tissue has special characteristics which will be discussed in the next paragraphs.

2.1.1. The nerve cell

General

The nerve cell is a type of tissue which can generate an electric potential. The nerve cell consists of some basic parts as can be seen in figure 2.1.

- The nucleus, in which the DNA material of the cell is kept
- The cell body, being the main part of the cell
- Dendrites, which can be seen as the input or sensors of the cell. They sense the potentials of other cells. Neural cells can have up to hundreds of dendrites.
- The axon is the transport line of the cell. Electric potentials are carried from the cell body to the end of the cell. At the end, we find the axon terminals, which transfer their signal to the next nerve cell.
- The axon is covered with myelin sheath. This sheath enables neural responses to travel at high speeds through the nerves. Without this material, it takes way too long for a signal to arrive. At some points, the axon is uncovered. These parts are the nodes of Ranvier. Here, the cell is able to exchange Na and K ions with its surroundings.

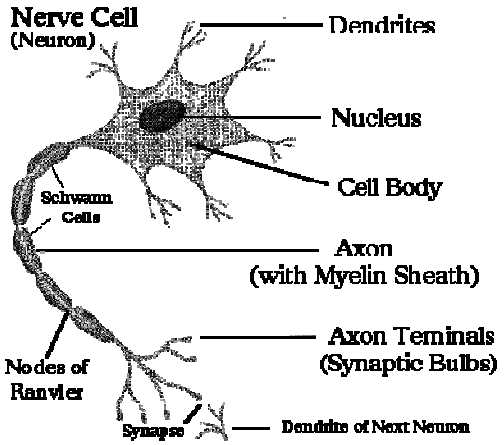

Figure 2.1: The nerve cell. Source: www.naturalhealthschool.com/img/nervecell.gif

The nerve cell is able to conduct electric pulses by moving ions through its axons. The ions are the charge carriers in the nerve cell.

In order to activate a nerve cell, the membrane voltage of the cell has to be raised to a particular threshold voltage. The cell will be activated and an impulse signal will start to travel through the axon towards other cells. During rest, a resting potential is present in the nerve cell, the so-called Nernst Potential. At this potential, the cell is in equilibrium and no current is flowing [13].

Kinetics of Electron exchange

The Nernst potential works according to the kinetics of an electron exchange. Suppose that an electrode material can supply and can take electrons during chemical reaction in an electrolytic solution. A material can act as a cathode or as an anode. These cathode and anode have particular electron transfer rate constants, k_a and k_c. The current densities will become

$$I_c = -nFk_c c_c \tag{2.1}$$

for the cathode and

$$I_a = nFk_a c_a \tag{2.2}$$

for the anode. Where n is the valence of molecules, F is the Faraday constant and c_c and c_a are the concentration constants of molecules at the cathode and the anode, respectively. At equilibrium, it does not mean that the sum of both currents I_c and I_a is 0. The exchange of both currents will be equal to each other. This equilibrium can be represented according to Equation 2.3.

$$I_a + electrons \underset{k_c}{\overset{k_a}{<=>}} I_c + electrons \tag{2.3}$$

The value of k is not constant but depends approximately exponentially on the Nernst potential.

The Nernst potential is reached under an equilibrium of the current densities. The potential can be denoted by E and is represented by Equation 2.4:

$$E = E_0 - \frac{RT}{nF} ln \frac{c_c}{c_a} = E_0 - \frac{kT}{ne} ln \frac{c_c}{c_a} \tag{2.4}$$

Where E_0 is a characteristic parameter from the “nature” of the electrode-electrolytic interface, R is the universal gas constant, T is the temperature in kelvin, n is the number of moles of electrons, F is the faraday constant, k the Boltzmann’s constant and e the charge constant. Every ion has its own Nernst potential [14].

Membrane model

At equilibrium, inside the nerve cell there is a surplus of sodium (Na^+) -ions. At the outside of the nerve cell, there is a surplus of potassium (K^+) -ions. When a stimulus is given to the cell, the cell pores will open and K^+ -ions will flow into the cell and Na^+ -ions will flow out of the cell. This movement of ions is due to diffusion and osmosis.

In the membrane model depicted in figure 2.2, three channels can be distinguished. These are caused by the so called sodium (Na^+) flux, a potassium (K^+) flux and a chlorine (Cl^-) flux. In which flux stands for the flow of ions through the membrane. Each channel has its own ion conductance G_{Na}, G_K and G_L respectively. These conductances depend on the membrane voltage.

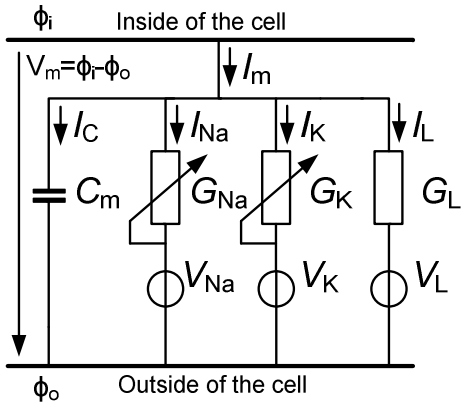

Figure 2.2: Model of a cell membrane

Every channel has its own built-in potential V_{Na}, V_K and V_L respectively. Mostly, the concentration of chlorine in the cell is very low. Therefore, the contribution of chlorine to the total flux, consisting of the summation of sodium flux, potassium flux and chlorine flux, is small. For this reason, the chlorine conductance can be approximated with a constant value.

Hodgkin and Katz [15] found that the permeability of the neural biomembrane at rest for potassium can be 25 times larger than for sodium giving the relation $P_K : P_{Na}=1 : 0.04$. Because of this property, the potassium ions will move much faster to the inside of the nerve cell, than the sodium ions will move out. This causes the membrane potential to rise until the concentration of the potassium ions at the in- and outside of the nerve cell reaches equilibrium. The sodium ions are not finished diffusing. The membrane potential will drop again until the sodium ions also reach equilibrium. The action potential is now finished. In this situation, the nerve cell will not be able to generate a new potential. The sodium and potassium ions are present at the inside and outside of the nerve cell. To prepare the nerve cell for a new action potential, the Na-K-pump is present. This pump transports potassium ions to the outside of the cell and sodium ions to the inside of the cell. This is an active process and thus uses energy.

The membrane voltage is represented by Equation 2.5 which is the Equation of Goldman [16].

$$V_m = \frac{kT}{e} \ln \frac{P_K c_{e,K} + P_{Na} c_{e,Na} + P_{Cl} c_{i,Cl}}{P_K c_{i,K} + P_{Na} c_{e,Na} + P_{Cl} c_{e,Cl}} \tag{2.5}$$

In which *P* is the permeability of the membrane, *c* the concentration of molecules, *k* the Boltzmann's constant, *T* the temperature in kelvin and e represents the charge. The subscripted *e* is used for efflux, *i* for influx, *K* for representing potassium, *Na* for sodium and *Cl* for representing chlorine.

When combining the findings of Hodgkin and Katz and the Equation of Goldman, it can be said that the potassium channel is dominant to the other channels giving Equation 2.6.

$$V_m \approx \frac{kT}{e} \ln \frac{c_{e,K}}{c_{i,K}} \tag{2.6}$$

During generation of the stimulus and recovery of the nerve cell to its initial state, the nerve cell becomes refractory which means that it is insensitive for new stimulus pulses during this refractory period which typically lasts for approximately 0.5ms. After that, a stimulus pulse will generate a new neural potential [16].

2.1.2. Electrode-Tissue interface modelling

General

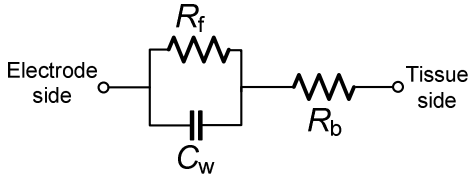

Figure 2.3: Model for the electrode-tissue interface

During modeling of the electrode-tissue interface as a circuit it has to be taken into account that the charge carriers in tissue are ions and the charge carriers in metal are electrons. The difference in type of charge carriers can be modeled as a capacitive element. However, this is not enough. Also the resistance of the electrode and tissue plays a role, giving a resistive element. At first glance, the capacitive element can be modeled as a double layered capacitor and the resistive element as a resistor. These two elements can be seen as a series network. However, the electrode-electrolyte interface is a bit more complicated. The reason for this are electrochemical reactions taking place at the electrode-tissue interface. These processes have to be modeled with an extra resistor in parallel to the double-layer capacitor. Figure 2.3, depicts this network in which capacitor C_w is the double-layer capacitor. Resistor R_f represents the electrochemical interface resistor and resistor R_b the resistive component of the electrode and tissue interface. The double-layer capacitance appears to be phase independent and can be replaced by a constant phase angle impedance (Z_{cpa}) and is represented by Equation 2.7:

$$Z_{cpa} = \frac{1}{(j\omega C_w)^{\beta}} \text{ with } 0 \le \beta \le 1. \qquad (2.7)$$

In which Z_{cpa} is the impedance of the tissue, ω the angular frequency, C_w the double-layer capacitor and β the phase. For β=0.5, the capacitance is also called Warburg capacitance (C_w). Warburg was the first person who found this component. For β=0.5 the phase angle is 45˚. Resistor R_f is a faradic constant and can also be represented by Equation 2.8:

$$R_f = \frac{RT \ln \frac{J}{J_0}}{(1-\alpha)nF} \frac{1}{J} = \frac{\eta}{I_0} \qquad (2.8)$$

Where I_0 is the exchange current, η the voltage deviation from the equilibrium voltage, R the universal gas constant, T the absolute temperature in Kelvin, F the Faraday constant, J the current density, J_0 the equilibrium current density, α the transfer coefficient and n the number of electrons per molecule oxidized or reduced [17][32].

Modeling of tissue in the cochlea

For modeling cochlear tissue, one element is added to the electrode-tissue interface model. The modified schematic is depicted in figure 2.4.

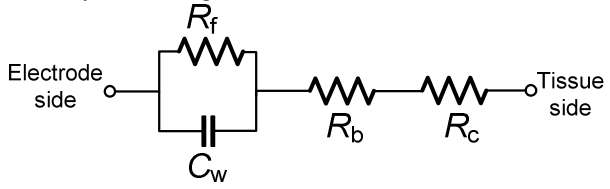

Figure 2.4: Electrical representation of the tissue-electrode interface in the cochlea

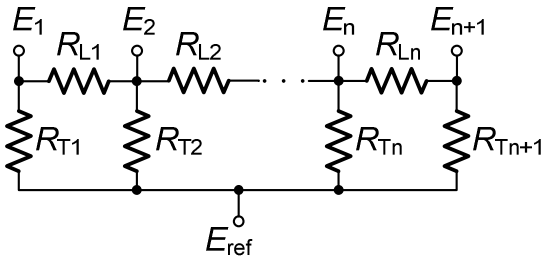

Figure 2.5: Resistor network of cochlear tissue

Resistor R_C is the equivalent input resistance of the cochlear tissue network. This resistance represents a network of longitudinal and transversal tissue resistances between the electrodes in the cochlea. Figure 2.5 shows a resistor network of electrodes placed next to each other. Electrodes E_1 to E_{n+1} represent the stimulation electrodes. Electrode E_{ref} represents the reference electrode. Longitudinal resistors R_{L1} to R_{Ln} represent the current flow along or parallel to the scala tympani. Transversal resistors R_{T1} to R_{Tn+1} represent the current leaving the scala tympani to return to the reference electrode via the lateral and modular bony structures.

Because the cochlea is spiraling, the model has to be expanded with current paths between the nonadjacent contacts. In practice, current path values of non-adjacent electrodes are very small compared to the current paths to the adjacent electrodes. For this reason, the current paths between non-adjacent electrodes will be neglected giving the complete model as depicted in Figure 2.6. Above the dashed line, the electrode-tissue interface is modeled. The part below the dotted line represents the tissue impedance network and the reference or grounding electrode [17].

The reference electrode has a large surface area decreasing the contact resistance to a minimum and increasing the capacitive coupling to very high values compared to the much smaller intracochlear electrode contacts. For this reason, the reference electrode impedance can be neglected and thus omitted.

The tissue impedance can be written according to Equation 2.9.

$$Z = R_c + R_b + \left(C_w // R_f\right) \tag{2.9}$$

In which Z is the total tissue impedance, R_c the equivalent input resistance of the cochlear tissue network composed of R_L and R_T, resistor R_b the resistive component of the electrode tissue interface, C_w the double layered capacitance and R_f the faradic resistance.

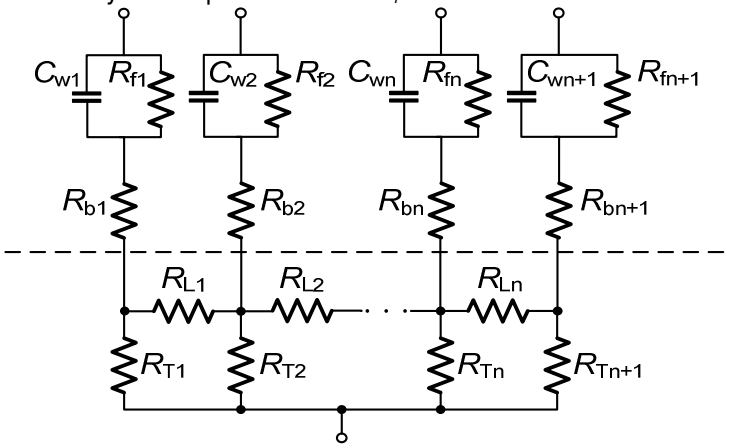

Figure 2.6: Network of the cochlear tissue, and electrode-tissue interface

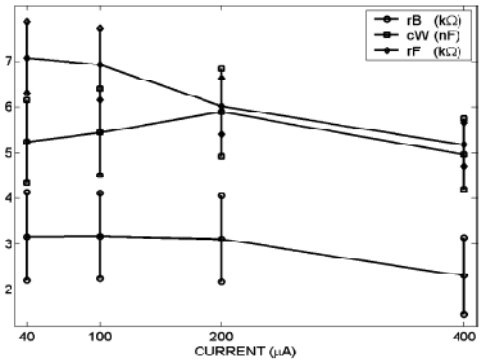

Figure 2.7: component values vs. stimulation current [17].

Rewriting Equation 2.9 gives 2.10:

$$Z(t) = R_c + R_b + R_f \cdot \left(1 - e^{\frac{-t}{C_W \cdot R_f}}\right) \tag{2.10}$$

In which t stands for time. All other parameters used are the same as used in Equation 2.9.

Values for the electrode-tissue model

For determining the electrode-tissue model component values, a range of values will be found. Several measurements have been performed to determine the component values. It appears that tissue impedance is dependent on the stimulation current. Figure 2.7 shows a graph with values of the tissue components at several currents. Every tissue component has its own graph.

Besides the component value variation due to the current, there is also a component value variation due to frequency. Model values can be averaged around the stimulation frequency of interest. Figure 2.8 shows the electrode-tissue impedance obtained by stimulating with a sine wave of 1kHz. Every electrode-tissue interface acts differently due to its specific local electrochemical circumstances in the cochlea. Measurement results in this section are obtained using an electrode having 16 contacts. Another way to determine the electrode-tissue impedance is to use a pulse shaped stimulus. Since stimulus signals in cochlear implants are pulse shaped, this more complies with reality.

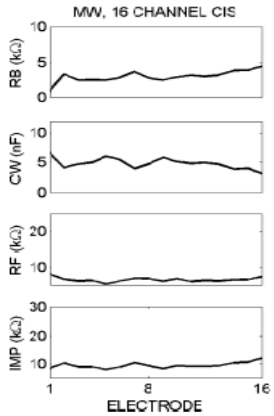

Figure 2.8: Channel number vs. component value at 1kHz [17].

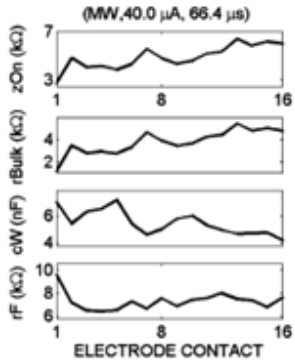

Figure 2.9: Electrode model component values per stimulation site stimulated with pulses with 66.4μs pulse width [17].

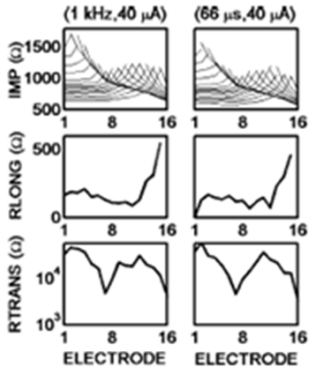

Figure 2.10: Impedances of the internal resistances due to several signals [17].

Tissue will likely be stimulated with a biphasic square wave. An example of tissue stimulated with a biphasic square wave is depicted in Figure 2.9. A pulse having a current of 40µA and a width of 66.4µs is applied. The impedance of the individual electrodes clearly differ from each other.

Comparing Figures 2.8 and 2.9, the measured component values differ from each other. Apparently the cochlear tissue impedance, composed of transversal and longitudinal resistors, is also dependent on the stimulus. The longitudinal and transversal resistance values are measured and depicted in Figure 2.10. The resistances measured with the same frequency and stimulation current as in Figure 2.8 can be seen in the first column. The second column contains results of resistances measured at the same stimulation pulse as used in Figure 2.9. The first row represents the total impedance of the tissue. The second row represents the longitudinal resistance and the third row is the transversal resistance. Comparing the two columns, some difference can be seen in the curves confirming non-linearity of tissue [17].

Calculated values of the electrode impedance are compared with measured values. Figure 2.11 shows results for 16 electrodes. Every electrode has its own graph consisting of a measured value (green line), a calculated value (blue line) and the difference between those two values (red line).

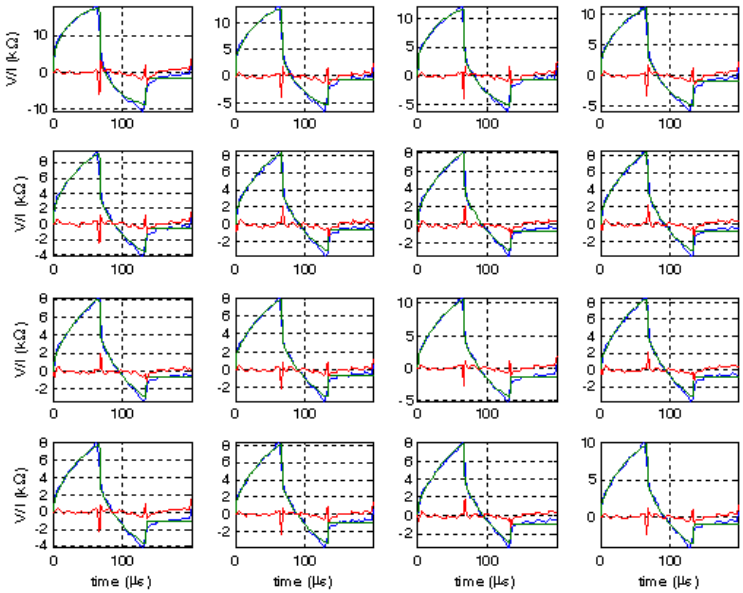

Figure 2.11: Calculated and measured impedance due to stimulus of electrode and the difference between those two [18].

Every stimulation site has its own impedance. The impedance varies with the biphasic signal which is applied at the electrode. The theoretical model approaches reality pretty well. Biggest deviations occur where the slope of the stimulus is the biggest [18].

The tissue is modeled and impedance values are determined. Next section handles the identification of signals coming from the tissue and measurement algorithms for measuring these signals.

2.2. Signal identification and measurement algorithms

Neural responses can reveal a lot of information about the functioning of the ear. Reading out this information is crucial in developing new stimulation algorithms and working towards a closed loop operation of cochlear implants. To design a proper readout system, signals at the input of the system should be identified.

2.2.1. Signal identification

Signals appearing at the input of the readout system in an implant are composed of several components. To be able to find the correct information, a distinction should be made between those components. The signal coming at the input of the readout has three different origins. These are:

- Stimulus
- Artifact
- Neural response

A typical readout curve is depicted in Figure 2.12.

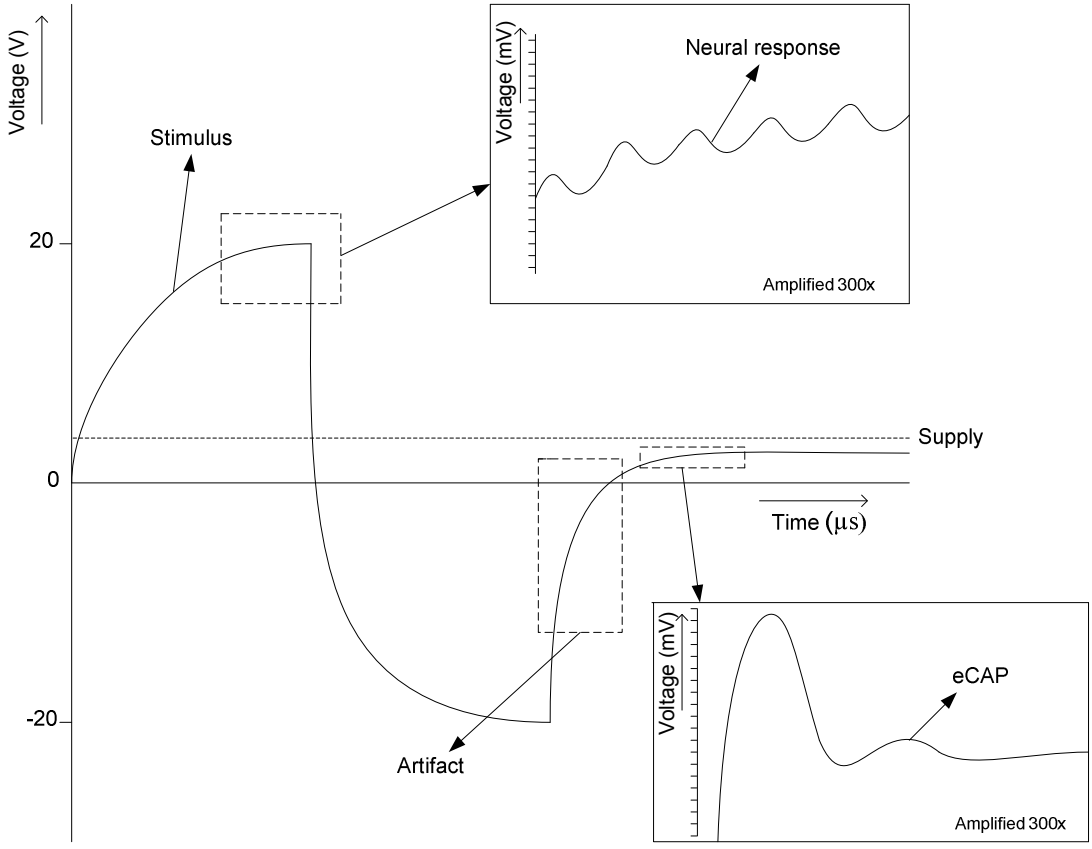

Figure 2.12: Neural response curve

Stimulus

The stimulus is a signal which can be measured in the whole cochlea. The position of readout electrode has only a slight influence in reducing this signal. The stimulation happens at relatively high energies so it will always appear in the readout of the electrode. The stimulus signal is depicted in Figure 2.12 as the big wave reaching 20 volts. In current implants, stimulus signals can reach 6 volt at maximum stimulation currents of 1200µA.

In new implants the stimulus will reach 20V due to reduced electrode area, and thus a higher electrode-tissue impedance. The stimulation power can be determined very accurately, so a prediction of this signal can be made very well.

Artifact

The artifact is a phenomenon which occurs as result of stimulation of nerve cells. It is a residual charge which is present at the electrode after giving a stimulus. This charge will flow away, but causes a major measuring error. The artifact is visible at the end of the stimulus in Figure 2.12, the bipolar stimulus precedes the artifact. As soon as the bipolar stimulus ends, the artifact starts to play a role. This charge is very difficult to predict exactly because of non-linearity of the tissue. Only a coarse estimation can be done. This has to be taken into account during the system design.

Neural response

The neural response occurs during and after stimulus and artifact. Figure 2.12 contains the neural response. Neural responses are electrochemical reactions of nerve fibers due to application of a stimulus. Neural responses are in the order of 10µV to 1mV. To be able to capture these small signals by a simple A-to-D converter, an amplifier will be needed which amplifies the signal 300-1000 times.

Evoked Compound Action Potential (eCAP)

The eCAP is the signal coming from the electrodes containing the stimulus, artifact and neural response. The eCAPs measured with todays implants can be seen in Figure 2.12. Only a small part of the complete response can be captured due to the limited dynamic range of the neural response amplifier used today. Medical doctors like to increase this dynamic range without losing signal information in order to better understand the human cochlea. The eCAPs used today are used by medical doctors for analysis. The amplitude and time of the positive and negative peaks of the neural responses are of main interest.

2.2.2. Measuring eCAPs

To obtain neural responses without stimulus and artifact, some algorithms are developed. These are:

- Electrical subtraction
- Alternating stimulus polarity
- Forward masking technique (MP3)

Electrical subtraction

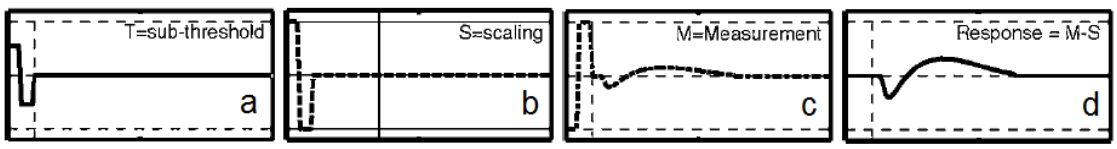

Figure 2.13: Electrical subtraction method signals [10]

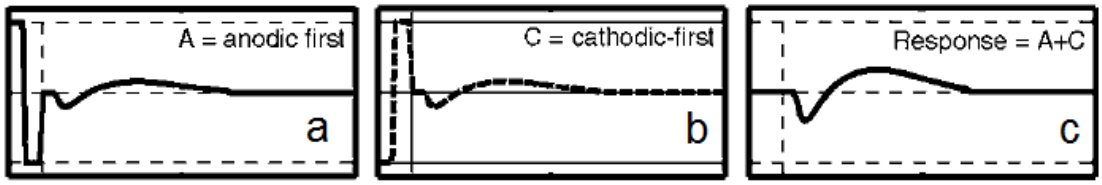

Figure 2.14: Alternating polarity method signals [10]

Figure 2.13.a shows a stimulus which is created beneath the threshold voltage (T) of the nerve enabling measurement of the stimulus and artifact at the electrode without a neural response. Figure 2.13.b shows the measured signal scaled (S) to the full-scale stimulus signal level. Then, the full-scale stimulus signal is applied and measured (M). The resulting signal is depicted in Figure 2.13.c. The scaled stimulus will be subtracted from the full-scale measured stimulus (M-S) leaving only the neural response as shown in Figure 2.13.d [10].

Because of the scaling of the stimulus beneath threshold (T), the noise of this signal is also amplified introducing an error in the neural response signal. Moreover, it is very difficult to obtain a signal which is completely neural response free. By amplifying the signal, it is assumed all components are linear, which is not the case since the electrode-tissue model is non-linear. This can give a major error.

Alternating polarity

Alternating polarity follows the principle of equal neural responses for both polarities. First, an anodic stimulation (A) is performed as showed in Figure 2.14.a. Then, a cathodic stimulation (C) is performed as showed in Figure 2.14.b. When both recordings are added (A+C) as showed in Figure 2.14.c, the stimulus and artifact of both recordings cancel each other and the two added neural responses remain [10].

In practice, the neural responses obtained by the anodic and cathodic stimulations are different, so actually two different signals are measured. This implies that the remaining signal left after averaging is something else than only the neural response.

Forward masking technique (MP3)

The forward masking method makes use of the refractory property of the nerve. A stimulus is applied to the tissue, called mask (M). The stimulus and resulting neural response are measured and the resulting graph is shown in Figure 2.15.a. A second, delayed stimulus is applied called probe (P). This stimulus with its neural response is measured and the resulting graph is shown in Figure 2.15.b. After this, two stimuli, a mask and a probe (MP) are given in which the probe is applied within the refractory period. These stimuli and the neural response is measured and the resulting graph is depicted in Figure 2.15.c. During the refractory period of the nerve, no neural response can be given. By subtracting Graphs 2.15.a and 2.15.b from graph 2.15.c (M+P-MP), the neural response remains. The resulting graph is depicted in Figure 2.15.d [10].

Not only one nerve but a complete nerve population is stimulated in the cochlea. After the mask stimulation of Graph 2.15.c some nerves can be charged, but not enough to reach the threshold for firing. This threshold can be reached with the probe stimulation, resulting in a neural response. The neural response in Graph 2.15.d can deviate because of the pre-charged nerves firing during the probe measurement.

Suppression of unwanted signals

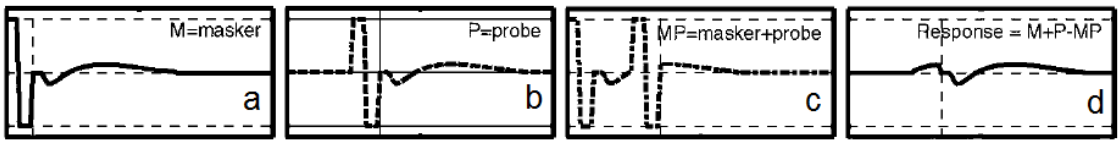

Figure 2.15: Forward masking method signals [10]

To suppress electrical noise, EMI and action potentials originating from different parts of the human body, many averaging cycles are performed. In practice, up to 512 readout cycles are performed and averaged.

To solve the issues found in this chapter, a new readout front end should be designed. Next chapter will discuss a new readout system based on compensation.

Chapter 3: System design

In this chapter, the readout system design of the cochlear implant is discussed. First, existing systems and their drawbacks will be discussed. Then, several system designs will be suggested for the new implant. These will be discussed and a choice will be made.

3.1. Existing systems

Two systems can be distinguished in measuring neural responses from the cochlea. The first one is used in implants today for fitting to the patient. The second one is an experimental system. This system has been tested on animals, but is never developed into a complete product. These two systems are discussed separately.

3.1.1. Readout system in today's implants

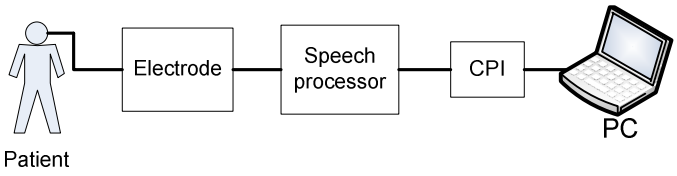

Figure 3.1: Block-system diagram of the front-end for advanced bionics implants [37]

Readout systems in today's cochlear implants are used by physicians for monitoring neural responses originating from the patients cochlea. It helps the physician to adjust the stimulus level of the implant to comfortable levels for the patient. Besides that, also scientific data is acquired. For transferring the neural response data, a connection with the audiologist's computer can be established.

The readout system of the neural response is depicted as block system diagram in figure 3.1. The left block in the figure is called patient, representing the cochlear tissue of the patient which will receive stimulus signals and give neural responses. The next block is the electrode, representing the electrode array placed in the patient's cochlea, applying stimuli to the tissue and receiving neural responses. Then, a speech processor block is added. The speech processor runs its own operating system. It has a special interface for programming the implant and acquires the measured neural responses from the electrode. To convert the speech processor interface to a computer interface (e.g. RS232), a Computer Programming Interface (CPI) is added. The computer runs special software from the manufacturer.

The neural response readout circuitry is located at the electrode array. A system block diagram is depicted in figure 3.2. Several system blocks can be distinguished and will be discussed following the signal path. The neural response induces a certain signal at the electrodes. From the electrodes, the signal goes through a wire and DC blocking capacitor to the implanted main board.

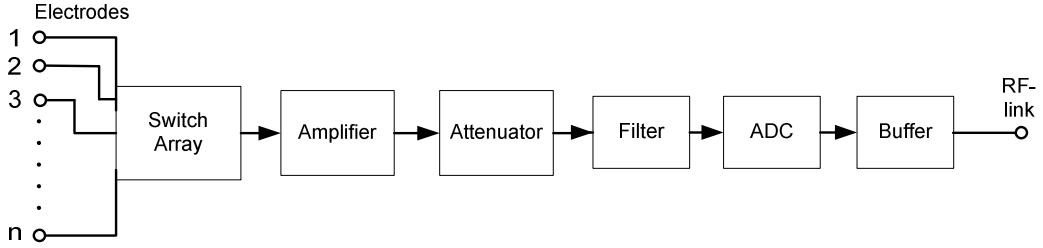

Figure 3.2: System block diagram of the front-end of the implant

At the main board, the wires coming from the electrodes are connected to a switch array. An electrode can be selected and passed to the amplifier. To obtain an optimal output signal from the amplifier, several fixed gains can be selected in the range 1-1000 times. The maximum output swing of the amplifier is 7,4 volts. At high gains needed for amplifying neural responses the amplifier will clip during stimulus.

To adapt the output signal of the amplifier (amplified neural response) to the dynamic range of the ADC, an attenuator is added. This attenuator will attenuate the amplified signal, when needed, down to values suitable for the ADC, which has an input range of -2.5 to 2.5 volts. A filter limits the bandwidth of the signal coming from the attenuator to reject noise and Electro Magnetic Interference (EMI).

After the filter, the signal is converted to the digital domain by an ADC. The ADC has a resolution of 9 bits, which is not sufficient for accurate data acquisition.

The digital signal coming from the ADC is put into a data buffer and is transferred over the RF link at a maximum transfer rate of 90.000 pulses per second to the speech processor. During measuring, the RF link is turned off in order to prevent interference between the RF link and electrodes. The field of the RF link is picked up by the electrodes and causes distortion of the measurement.

To avoid distortion caused by the RF link, a large capacitor is charged through the RF link and commands for stimulating are loaded into the memory of the implant. Then, the RF link is turned off and the implant applies its stimulus algorithm. The neural response is measured and stored in a data buffer. After measurement, the RF link is established again and the measured data is transferred to the speech processor. During measurement, it is not possible to change settings in the implant.

Today's cochlear implants still suffer from noise generated in the analog circuitry. Besides neural responses, the electrodes and wires also pick up EMI signals. EMI and noise levels have to be brought down in order to obtain correct measurement data.

3.1.2. Front-end developed at the Leiden University Medical Centre

At the Leiden University Medical Centre (LUMC), an amplifier is developed to measure neural responses of an animal cochlea. It is based on the cancellation of stimulus artifacts enabling the acquiring of data during this artifact and not only after. This amplifier is built with conventional components on a printed circuit board having dimensions of approx 10x20cm. The amplifier suffers from noise, EMI and big component tolerances. It is a differential amplifier based on the driven right-leg principle which consists of a signal path back to the body of the animal to reduce the measured noise generated by the animal's body.

A system block diagram of the complete measurement system is depicted in figure 3.3. A computer with software called "Winmeasure" is used for controlling a device called SPES and readout an ADC. The SPES is actually a Digital to Analog converter and can generate voltages at its output to control a current source.

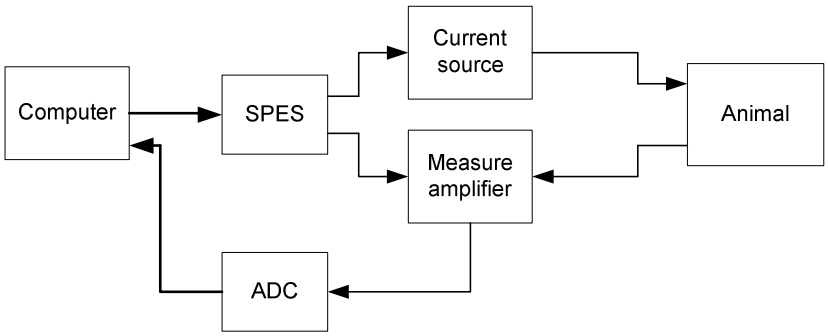

Figure 3.3: System block diagram of the setup used for animal testing with the measure amplifier.

The current source is battery operated and has an optical insulator on board to isolate the signal coming from the computer and the signal going to the animal's body. It creates a current as function of the input voltage at its output. The current is applied to the electrode positioned in the animal's cochlea. The measure amplifier measures the neural response of the cochlear nerve fibers.

To filter away the stimulus artifact, the SPES gives a trigger pulse to a special circuit in the amplifier which (almost) eliminates the artifact. The output signal of the measure amplifier is digitized by an Analog to Digital converter and captured by the computer. The software program Winmeasure depicts the measured signals at the screen and saves the data. This data can easily be imported into matlab for signal processing.

The measurement amplifier is a special developed amplifier which makes it possible to measure signals almost directly after application of the stimulus. Figure 3.4 depicts the system block diagram of the amplifier. The input of the amplifier is represented by the *+*, - and V_{gnd} terminals. Electrodes used for animal testing can be attached to those terminals. The trigger signal coming from the computer is applied to the trigger input.

The trigger pulse is applied to two RC-networks with a variable resistor for generating a logarithmic pulse. One network is used for positive stimulation, one network is used for negative stimulation. Because of electrode-tissue interface non-linearity, the network has to be tuned for each individual electrode. An amplifier with adjustable gain is connected to the output of each RC-network for amplifying the generated logarithmic signals. The output of the amplifiers is added to the input signal to cancel the artifact.

The remaining neural response is fed to a limiting amplifier for suppressing spikes in the neural response exceeding the dynamic output range of the amplifier. This is done by a non-linear adjustable feedback network which automatically adjusts due to the signal. Because of its non-linearity, the feedback network is a potential source of noise. The amplifier is equipped with some filtering elements to suppress noise.

The next stage is a clamped amplifier with adjustable gain. The gain is set by a control line. Also this amplifier has a non-linear feedback loop enabling the amplifier to recover from saturation very fast.

For safety of the animal, an optically isolated amplifier is added. The output of this amplifier is connected to a 12-bit A-to-D converter. The measurement amplifier is completely battery operated.

Although first measurement results with this amplifier were promising, it is never been further developed and converted to an amplifier suitable for use in an implant. A lot of adjustments by hand (or software) have to be made before the artifact is cancelled completely. This amplifier is able to eliminate the artifact, but not the stimulus.

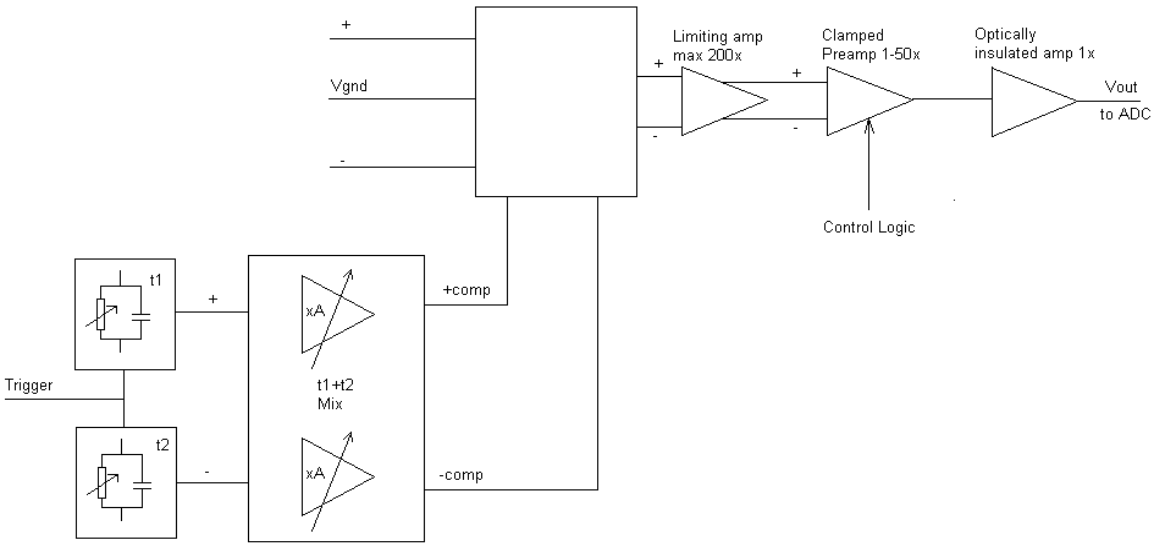

Figure 3.4: Block-system diagram of the amplifier developed at the LUMC used for cancelling stimulus artifact during measurements [10]

At the output of the amplifier, a noise of $2{,}5mV/\sqrt{Hz}$ is measured. The gain is set to 1000 times, so an equivalent input noise of 2,5 µV present at the input.

The challenge is to be able to get the complete neural response including stimulus and artifact. All methods discussed until now are not able to measure during stimulation of the auditory nerve. The measuring systems all have clipping amplifiers preventing the system to obtain correct measurement data during stimulus.

3.1.3. Readout system specifications

During stimulus and artifact, already neural responses occur. State of the art implants used today are not able to readout this data because the amplifiers used are clipping during stimulus and artifact. Physicians don't know what these responses look like and because of this, they like to be able to read out the complete eCAP. Physicians also would like to stimulate at very low currents [12]. Neural responses resulting from these low current stimulations cannot be determined because they drown in noise and signals caused by Electro Magnetic Interference (EMI).

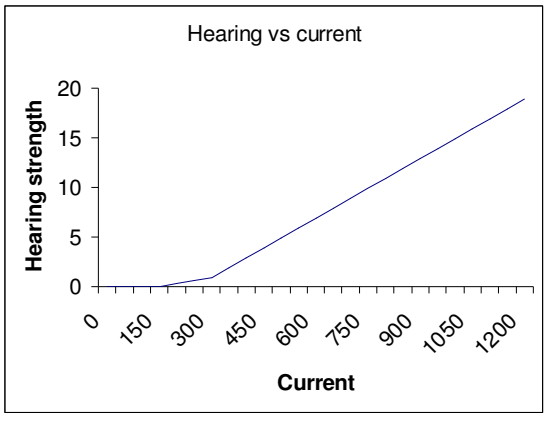

Figure 3.5: Hearing strength versus current

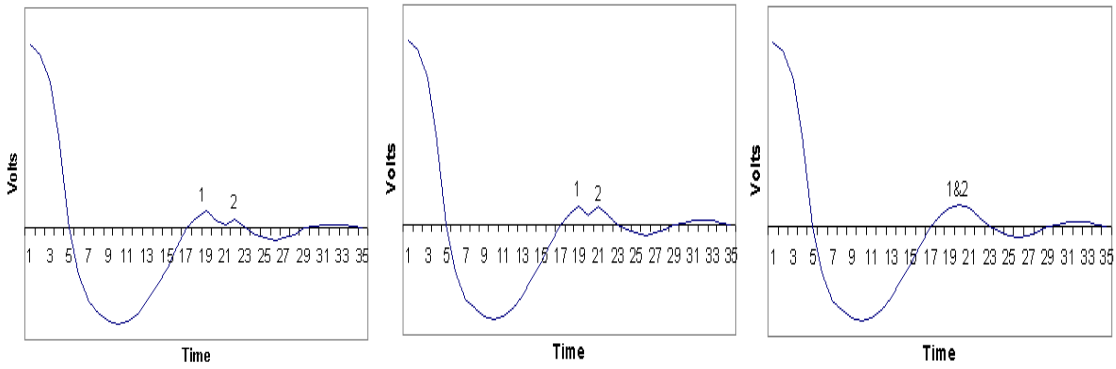

Figure 3.6: Example of neural responses at three different stimulation currents

Another issue is that it is not possible to read out multiple electrodes at the same time. The readout amplifier used in today's implants consists of only a single channel. Physicians would like to have a multichannel monitoring system in which they can adjust parameters in real-time during measuring, urging the RF-link to be active during measurements. To realize such a system, a higher data transfer rate of the RF-link is needed than available in current implants.

The new readout system will be designed as an integrated circuit. Supply voltages will be limited to the maximum allowed voltage of the used CMOS technology. The impedance of the electrodes ranges from 565Ω to 30kΩ. In present electrodes, for every stimulation site a decoupling capacitor is used to prevent residual charge at the cochlea. In the new implant, this capacitor will be replaced by a charge cancellation system.

Sampling should happen at a minimum speed of twice the bandwidth (Nyquist criterion) per channel. Neural responses can be found in a frequency range of 100Hz to 10kHz, giving a bandwidth of 9.9kHz.

Physicians would like to stimulate the cochlear nerves at very low currents. At these low currents, the patient cannot hear yet, but has the feeling the implant is already stimulating. Neural responses resulting from these stimuli are too small to measure with existing implants. A graph depicting hearing strength versus current is shown in Figure 3.5. Between 150µA en 300µA, some single nerve fibers of the patient starts to fire. This is the area where the patient cannot hear, but already has the feeling that the nerves are stimulated.

Physicians have the idea that the neural response as we know it is composed of a lot of nerve fiber responses [12]. It is possible that every nerve fiber has its own characteristic resulting in constantly different graphs. An example of possible neural responses is depicted in Figure 3.6. In the left graph, a response is depicted of two nerve fibers. The nerve fibers are indicated with the numbers 1 and 2. Nerve fiber one has a bigger response than nerve fiber two. In the middle graph, the neural response of the two nerve fibers is depicted again having a higher stimulus current applied. Nerves 1 and 2 both have equal amplitudes. In the right graph, the stimulus current is raised again. The separate responses are fallen together, so it seems that only one nerve is activated. Stimulus currents will be applied at a minimum pulse width of 20µs and a maximum of 50µs.

Noise

Researchers like to have a lower "noise" in their measurements. The interpretation of the phenomenon "noise" is different for physicians than for engineers. Physicians like to see a smooth curve of the neural response.

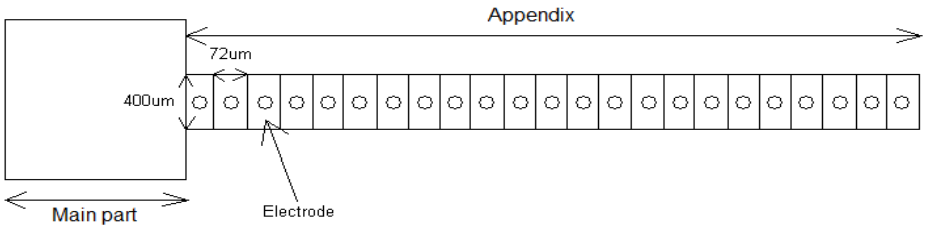

Figure 3.7: Cochlear implant with electrodes and dimensions of the electrodes

All the other signals they see is considered to be noise, e.g. internal noise of electrical circuitry, action potentials of the body like heart pulses and muscle potentials, 50Hz from the mains voltage, interference of the implants RF-link, gsm pulses, radio waves and so on.

Space available on chip

To determine the space budget for the readout circuitry, an estimation of the separate electrode areas placed in the cochlea can be made. The appendix will be inserted into the cochlea until a depth of ±18.6 mm. The 256 electrodes have to be placed in this area. This implies that every electrode site can have a maximum length of:

$$\frac{18.6mm}{256\ electrodes} = 72.66\mu m \tag{3.1}$$

To fit into the cochlea, a maximum width of approximately 400µm can be used. This depends on how deep the electrode is placed in the cochlea. At the beginning of the cochlea, the implant can be wider than at the end of the cochlea. For simplicity, an average width is used. The implant with appendix is depicted in Figure 3.7. The total chip area available per electrode is very small. A small capacitor (e.g. 10pF) already consumes more chip area than available. Care have to be taken in choosing the position and topology of the electronic circuit. A part can be located at the electrodes and another part can be placed at the main part of the implant.

The appendix will be able to bend. Electronics located at the appendix should be immune for mechanical stress. In order to bend the appendix to the shape of the cochlea, a special bending mechanism will be developed at TU Delft and placed at the appendix.

Dynamic range

Neural responses can reach levels down to 10 µV, while the stimulus can reach levels up to 20V. This implies that a dynamic range of 126dB is needed according to Equation 3.2.

$$DR = 20 \cdot log_{10}\left(\frac{20V}{10\mu V}\right) = 126dB \tag{3.2}$$

Which results in a minimum amount of 21 bits needed for proper analog to digital conversion according to Equation 3.3.

$$Amount\ of\ bits: 2^x = \frac{20V}{10\mu V} \rightarrow x = 21 \tag{3.3}$$

The system specifications are determined so the system design can now commence. This will be discussed in the next section.

3.2. The readout system design

The readout system can be divided into several parts. Each part has to comply with certain specifications. All the parts of the front-end system will be discussed separately and a topology for the front-end will be chosen.

3.2.1. Front-end subparts

Several possibilities have to be investigated in order to design a system topology solving the problems of today's implants mentioned in paragraph 3.1. The readout can be divided in the following subparts:

- Link through skin
- Buffering
- Analog-to-digital converter
- Amplifier
- Multiplexing

All these subparts will be discussed separately and several techniques will be considered. Filtering of the incoming signals should be performed. This can be done anywhere in the system and is for simplicity not discussed in this thesis.

Link through skin

A wired link or an RF-link can be used. A wired link has the benefit of easy transfer of supply and signals. An external battery will feed the implanted part easily through a wire. Transmission speeds of data can be made high and almost no energy loss will occur. Electrically, it is a very attractive solution. Physiologically, a wire through skin will cause inflammation of the surrounding tissue and even rejection of the implant by the human body can occur. This makes the wired link unsuitable for the transfer of signals and power through the skin.

An RF-link transfers data and power through the skin wirelessly. The RF-link should be able to transfer supply and signals to the implant and back. Several chips are available on the market having much higher transfer speeds than used in today's implants. This can imply the next-generation implants will be able to reach much higher transfer rates as well.

Firstly, there is the Zarlink ZL70101. This chip is specially designed for implanted medical devices (IMDs) and has a maximum raw data transfer rate of 800kbps. It consumes 5mA at full power and needs a supply of 2.2V. It has a much higher data rate than available in todays implants.

Secondly, the Nordic nRF24LE1 is available. This chip is able to transfer a maximum of 2Mbps raw data and consumes 11mA at full power and needs a supply of 2V. This chip is not tested for application in IMDs, but can potentially work.

Both chips operate in special RF-bands reserved for medical and industrial applications. High data transfer rates creates the opportunity to transfer more accurate measurement data and/or multichannel measurement data. These chips are not able to transfer power through the RF-link for powering the implant.

Keeping these chips in mind, it can be said that it must be possible to create an RF-link with a raw data rate of at least 2Mbps through skin for a cochlear implant [19][20].

For powering the implant, inductive coupling can be used. It consists of two flat coils. One is placed under the skin of the patient. One is placed on top of the skin of the patient. Together, they act as transformer able to transfer power to the implanted part of the cochlear implant. By varying the coil impedance, a limited data transfer can be performed [33].

Buffering

Measured data will be converted for transfer through skin by the RF-link. It can happen that signals become corrupted on their way through the skin via the RF-link due to loss in the wireless channel. An internal buffer will be needed to be able to send the data again. Memory coupled to a microcontroller can be used as a buffer. A microcontroller with memory will already be present in the implant for translating stimulus codes coming from the speech processor into stimuli applied at the electrode.

Analog-to-Digital Converter

Several ADC principles are available, each having their own benefits [21]. In the readout system, power efficiency, chip area consumption and resolution play a big role. The sampling rate is less critical because it is relatively low. The topology of a Successive Approximation ADC is the most power efficient converter and is available with resolutions up to 16 bit. Sampling speeds are high enough for application in the implant. The power consumption can be made very low making this topology a good candidate for application in the implant. The Successive Approximation ADC also consumes the smallest space. The major drawback is the limited resolution.

A Sigma-Delta converter can typically convert up to 24 bits and thereby has a higher resolution than the successive approximation ADC. Power consumption is quite high compared to other ADC architectures [34]. High voltage components, causing a high chip area consumption, will be needed for dealing with the high input signals. A choice should be made between those two topologies.

Power and resolution are very important specifications, so a compromise should be found. The Successive approximation is very attractive because of its low power consumption, the Sigma-Delta because of its high resolution. Power consumption cannot be repaired in other stages of the readout system making the successive approximation architecture more suitable for application in the readout system.

A prediction of the power consumption can be made. The most energy efficient ADC which is developed and tested until now has a Figure of Merit (FoM) of 4.4fJ/conversion step [22]. It uses a chip area of approximately 280 µm x 110µm in 65nm technology. The figure of merit can be calculated with the Equation:

$$FoM = \frac{P}{2^{ENOB}.F_s} \tag{3.4}$$

In which p is the power consumption, F_s the sampling frequency and ENOB the Effective Number Of Bits. To determine the power consumption, the Equation is rewritten to:

$$P = FoM \cdot 2^{ENOB} \cdot F_s \tag{3.5}$$

Because the first bits are lost due to noise and non-linearity (INL, DNL), the 10-bits ADC has an ENOB of 8 [22]. A 10-bit successive approximation ADC developed by R. Lotfi [35] has an ENOB of 9.2. The ENOB for a 16 bits ADC is therefore chosen to be 14. Using a FoM of 4.4fJ/conversion for a 16-bit converter which can convert data from 4 electrodes simultaneously with a sample rate of 56kS/s each gives:

$$P = 4.4fJ \cdot 2^{14} \cdot (56kS/s \cdot 4) = 16{,}1\mu W \tag{3.6}$$

The limited resolution can be solved by the following techniques.

1. *Input scaling*: The ADC will have a limited input range and when the input range is exceeded, the signal is attenuated. A major drawback is that the resolution of the neural responses during stimulation will become too poor.
2. *Supply voltages scaling*: This technique shifts the supply voltage with the input signal. An ADC is used with a limited input range. As soon as the input signal exceeds the input signal range of the ADC the complete ADC including supply voltage, is offsetted resulting into a shift of the ADC input signal range. Because only one ADC is used, the power consumption will remain almost the same. The chip area hardly increases. A major drawback is that only one electrode can be read out. If two electrodes are read out simultaneously, this can give problems because the signal levels coming from the electrodes can differ from each other requiring a large input signal range. Moreover, interfacing of the ADC to the microcontroller will be complicated.
3. *Internal ADC reference shifting*: The internal reference of the ADC can be shifted with the stimulus and artifact. As a consequence, the ADC will only measure neural responses and not the stimulus and artifact. This can give the desired resolution for the neural response signal. The reference will be shifted at estimated stimulus and artifact values. Power supply limitations will give a problem since the reference has to be shifted higher than the supply voltage. Moreover, high voltage components will be needed.

All techniques discussed have their own limitations making them not suitable for application into a cochlear implant. The resolution problem cannot be solved in the ADC itself, so it have to be solved at a different subsection.

Amplifier

To adapt the dynamic range of the readout system to the ADC input signal range, an amplifier can be used. The amplifier has to amplify the neural response signal to a higher voltage without clipping. Several solutions are possible for this problem. These can be divided in two principles. The first one is adjusting the dynamic range. The other principle is compensation.

Adjusting the dynamic range

Several amplifier techniques are available to enlarge the dynamic range of the readout system.

1. *Logarithmic amplifiers*: The logarithmic amplifier is shown in Figure 3.8. A logarithmic amplifier will have a big amplification factor for small signals and a small amplification factor for large signals. Because of this property, the logarithmic amplifier will not clip. A diode takes care of the logarithmic behavior of the amplifier. Because of the diode in the feedback network, noise becomes proportional to the square root of the input signal. This makes it more difficult to reconstruct the signal accurately later. In the design, low distortion, low noise and low EMI are of primary importance. This makes the logarithmic amplifier unsuitable for application in the implant.

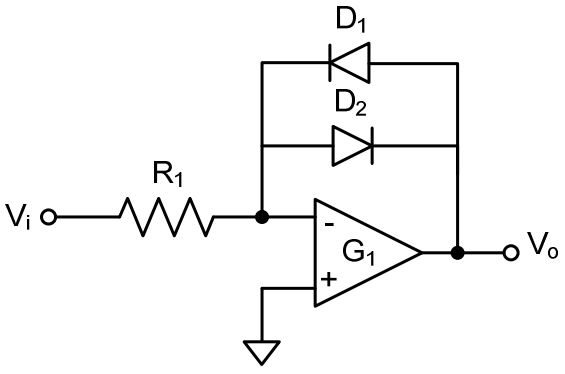

Figure 3.8: Principle of logarithmic amplifier

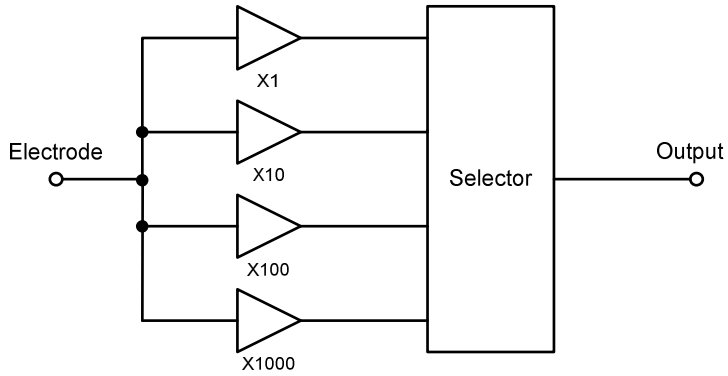

Figure 3.9: Principle schematic of parallel amplifiers

2. *Parallel amplifiers*: Another approach is to choose a topology with several amplifiers in parallel. Every amplifier has its own gain and can be selected by a multiplexer. The amplifiers should have a fast recovery time from saturation. A principle schematic is depicted in Figure 3.9. This topology gives a linear amplifier. A big disadvantage is a high power and space consumption. The previous discussed topologies only use one amplifier. A minimum of 2 amplifiers will be needed. But it is very probably that more amplifiers are needed. Power consumption can be reduced by switching off the amplifiers which are not used. To prevent transients at the output due to the settling of amplifiers when switched on, the amplifiers should be turned on slightly earlier than selecting it. Because multiple amplifiers are needed, the chip area consumption will be relatively big. Moreover, during stimulus, the gain is low giving problems in reading out the neural response properly. This is a major drawback for this system.
3. *Automatic gain controlled amplifier*: A dynamic technique for adjusting the output to a certain level. If the input signal level becomes too high, the amplifier will bring its gain down preventing the amplifier to clip. It will always try to get an optimum output level. In case of the implant, the output of the difference amplifier should also be measured to be able to recalculate the original signal. The expander can be realized in the digital domain. During stimulus, the gain is low giving problems in reading out the neural response properly. This is a major drawback for this system.

Compensation

Compensation can be achieved by eliminating signals which are of no interest or reducing signals which are too large. A method to do this is subtraction of signals at the input. For creating the subtraction signal, only an approximation of the input signal can be used. If this approximation can be made well enough, the stimulus and artifact signal can be eliminated sufficiently in order not to saturate the amplifier. Because the generated signal used for elimination of the stimulus and artifact is known well, the measured signal can be restored digitally. Because the signal is reduced to almost only the neural response, the resolution of the ADC can be lower. Compensation is therefore preferred above adjusting the dynamic range.

Multiplexing

Recent implants have one wire coming from every electrode to the microcontroller. If the amount of electrodes is increased to 256, the same amount of wires will be needed making the implant very bulky and, consequently, it won't fit in the cochlea. Multiplexing can reduce the amount of wires significantly. Several multiplexing methods are available and can be subdivided into three domains; time domain, frequency domain and digital domain.

1. *Time domain:* Time domain multiplexing consists of multiple lines to transport data from and to the electrode and its proper function.

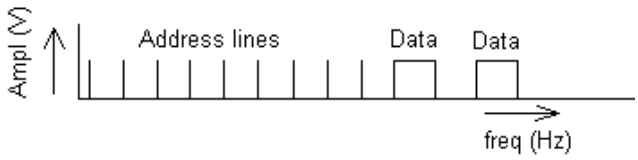

Figure 3.10: Addressing and data at one single wire

If multiple data packets should be transported simultaneously, the number of lines will rise. The amount of lines can increase exceeding the available space in the cochlea. Today's implants can handle a maximum of 16 to 24 lines, which is also the maximum amount of wires fitting into the cochlea. This topology will potentially give a too bulky system not fitting in the cochlea.

Time domain multiplexing suffers from noise and EMI, making this technique not a favorable option. However, if stimulation and readout electronics are located at the electrode, no long wires are necessary solving the space, noise and EMI issues. Time domain multiplexing can help reducing size and power consumption of the electronic circuitry located at the electrode significantly.

2. *Frequency domain:* Transporting data from and to electrodes and its proper function can be achieved by giving every type of data its own frequency enabling the use of only one single line. Figure 3.10 shows the addressing of electrodes and the transport of data on one wire in the frequency domain. The data bandwidth coming from the electrode should be limited before it is put in its frequency band for preventing the data to cover the whole frequency spectrum and distort other data. Frequency domain multiplexing will not suffer from EMI and noise can be kept low. Electronics located at the electrode for conversion to the frequency domain will consume a lot of space making this topology not suitable for application in the implant.

3. *Code domain:* When multiplexing in the code domain, signals will not suffer from EMI or noise. The amount of lines and power consumption can be kept very low. Biggest problem is the conversion from the analog to the digital domain at the electrode. The converter will not fit on one electrode.

4. *Combination of domains:* The noise and EMI levels will become too high if only time domain multiplexing is used. For multiplexing in digital domain the ADC will be too big to fit on one electrode. If first a time domain multiplex is performed on a limited amount of electrodes, there will be enough space for one ADC enabling digital multiplexing. This method seems to be the most suitable for application in the implant.

3.2.2. System topology choice

The system can be designed in several ways depending on the criteria the system has to comply with. Two subparts can already be given their fixed place. Figure 3.11 depicts the two subparts, which are the Microprocessor and the RF-Link. They will be located at the main part of the chip, not on the appendix (Fig 3.7). The electrodes are all positioned next to each other, enabling the division of them in clusters. At these clusters, an ADC can be placed. The ADC of M. van Elzakker [22], which is designed in 65nm technology, will consume approximately the area of 4 electrodes in 350nm technology.

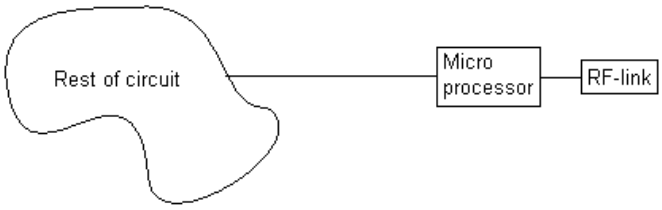

Figure 3.11: System-diagram of the new implant

One cluster of electrodes will consist of 8 or 16 electrodes depending on the space required for the readout circuitry. Every electrode will get its own current source for stimulation of tissue enabling the random choice electrodes for stimulation and readout. The current source transistors should be able to handle currents of 1200µA, requiring high voltage transistors consuming much more space than a normal transistor. A space consumption estimation using a cluster of 8 electrodes is depicted in figure 3.12. The black rectangles represent the electrode areas, the big red rectangle the ADC and the small red rectangles the PMOS and NMOS power transistors for the current sources.

To be able to read out every electrode by the ADC, an analog multiplexer will be needed. After digitizing the signal by the ADC, it will be offered to a microcontroller through a digital multiplexer. For addressing the current sources used for stimulation, a de-multiplexing circuit can be used. How to design the stimulation part falls outside the scope of this thesis. Figure 3.13 shows a high level system block diagram of the readout and stimulation circuitry.

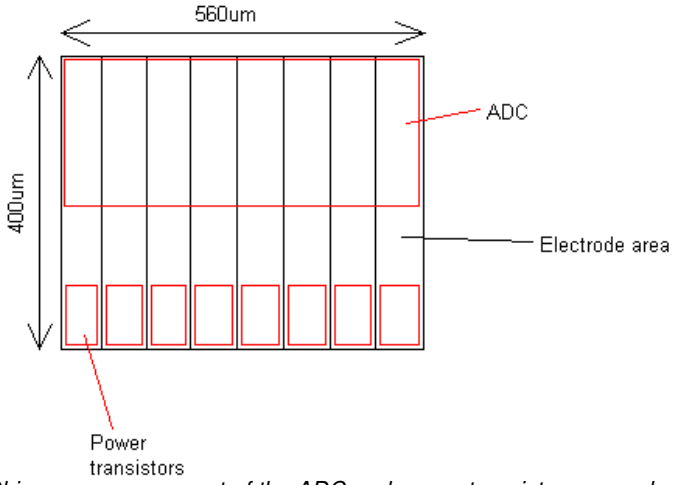

Figure 3.12: Chip area arrangement of the ADC and power transistors spread over 8 electrodes

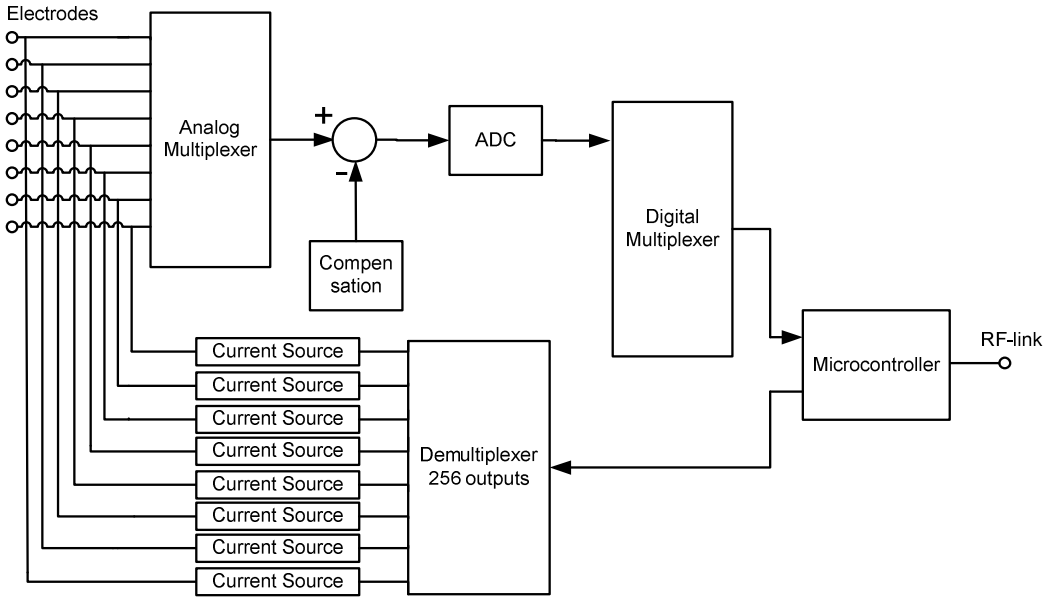

Figure 3.13: High level system-block diagram of the cochlear implant readout and stimulation circuit

The terminals at the left are representing the electrodes. Signals coming from the electrodes are applied to a multiplexer which is able to switch higher voltages than its own supply. The multiplexed signals will be compensated by a compensation circuit located after the multiplexer. By placing the compensation after the multiplexer, space and power is saved in comparison to placing a compensation after every electrode. After compensation, the signal is digitized by the ADC and multiplexed by the digital multiplexer. The digitized signal is applied to the microcontroller and subsequently to the RF-link. The path for stimulation is also depicted in the figure. From the RF-link, the signal for stimulation goes into the microcontroller. This microcontroller sends the stimulation signal through a multiplexer to the proper electrode via a current source.

A high level system design is performed. The readout path will now be discussed in more detail. Figure 3.14 shows a detailed system block diagram of the readout path. The electrodes are depicted at the left, followed by the multiplexer. Physicians like to be able to verify the entrance of the signals in the readout without doing compensation. Therefore, after the multiplexer an attenuator is added enabling the readout of the stimulus without applying compensation algorithm. The attenuator will only be used in this specific case, else it is bypassed by a switch. A compensation circuit will subtract a predefined signal from the signal coming from the multiplexer. The remaining signal will be amplified to use the complete input range of the ADC. The signal used for compensation is generated by a DAC.

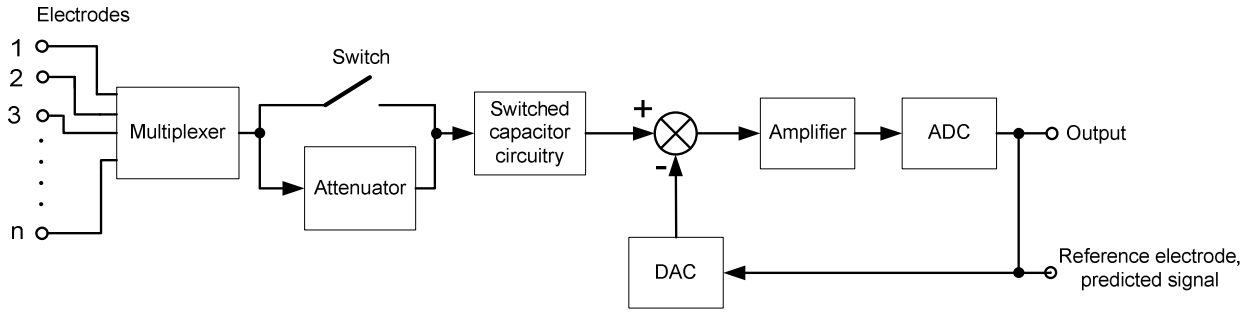

Figure 3.14: Detailed system-block diagram of the readout circuit of the cochlear implant

Specifications per system block

Before every block is discussed, there are some issues that are important for all the system blocks. All system blocks should be very compact and have an ultra low power consumption.

Multiplexer

At the input, signals will appear exceeding the supply voltage. To deal with these signals, the supply voltage have to be increased or the signals have to be attenuated. The circuitry should be compact and the signal to noise ratio should be extremely high, at least 126dB. A smart circuit technique should be found to deal with this.

Attenuator

The attenuator will normally be bypassed by the switch and will not contribute to the circuit specifications. When the attenuator is used, it is done for measuring the stimulus. The smallest signals which have to be measured depend on the resolution of the ADC. If for example a 10 bit ADC is used having an input range of 1V, the smallest signal which can be measured will be approx 1mV (1/1024). This part will not be a very critical one in the overall design.

Switched capacitor circuitry

To move to the charge domain, a switch in combination with a capacitor is added for sampling. The switch introduces charge injection which should stay under 10µV. It should be able to handle voltages above supply. The noise contribution should be extremely low. Together with the multiplexer the switch will be a critical part in the design.

Amplifier

After subtraction of the predicted signal from the sampled signal, the signal can be amplified to improve resolution of the measured signal. The amplifier should be able to amplify an input signal of 10µV to at least 10mV resulting in an amplification factor of 1000 times. The input referred noise should remain under this 10µV.This will be a critical part of the design.

ADC

A 10-bit ADC will have an input range of 1V. The ENOB of the design of [22] is 8. This gives $2^8 = 256$. Every step represents $\frac{1}{256} = 3.9mV$. Taking a minimum of ½ LSB, the ADC should get a minimum input voltage of 7,8mV. This can be achieved by using an amplifier having an amplification factor of 1000 times.

DAC

By subtraction of a predicted signal from the sampled signal, the initial resolution requirement of 21-bits can be brought down significantly. The DAC should have a high accuracy and produce extremely low noise to prevent distortion of the remaining signal which has to be amplified and converted by the ADC. If the ADC of [22] is used with an amplifier having sufficient gain, the resolution of the DAC should be 13 bits. This is higher than the ADC itself. The DAC will therefore be as well as the switch and multiplexer a critical part in the design.

In the system diagram shown in Figure 3.14, high voltage components have to be used from the input until the amplifier, including the DAC. These components will occupy too much space on the chip. A maximum of approximately 6 high voltage components can be used in the available area. The input signal should be brought down to values lower than the supply voltage as soon as possible without the loss of information in the signal.

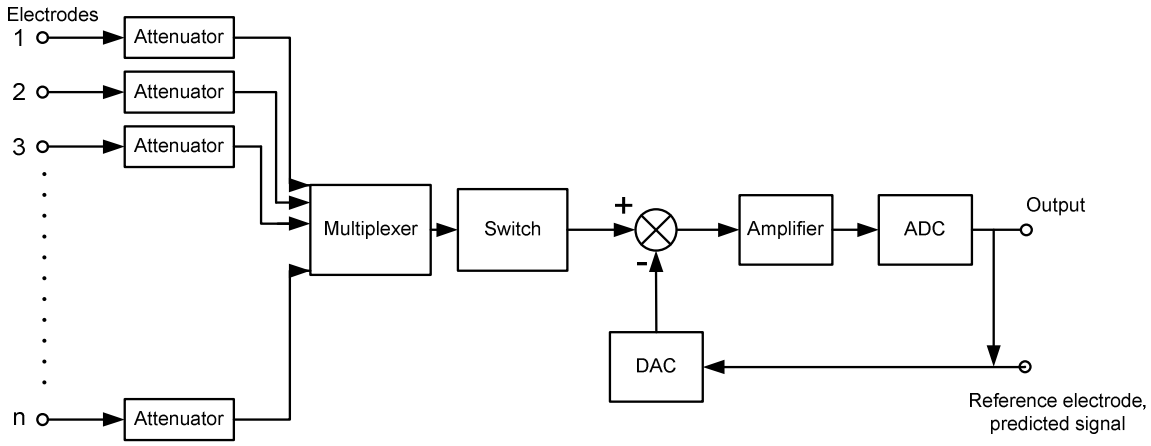

Figure 3.15: Modified system-block diagram of the readout circuit of the cochlear implant

The attenuator is therefore moved to the input of the system, before the multiplexer and will be constantly used. Figure 3.15 shows the modified system block diagram.

Noise

Digital and analog circuitry will be placed very close to each other. A very familiar problem is the injection of digital noise into the analog circuitry causing distortion of the input signal. An estimation of the amount of digital noise is therefore desired. In [23], it can be found that switching noise injected into the bulk is the biggest source of digital noise. Because an accurate noise estimation taking into account all noise sources can only performed after the complete circuit design, a coarse noise estimation is performed in this section only handling the noise injected into the bulk. Other sources of digital noise such as coupling through power lines and capacitive coupling between components are omitted.

For simulating noise injection into the bulk, a simulation of a circuit consisting of three inverters is performed. The circuit is depicted in figure 3.16. Because in digital circuitry transistors can be kept small, the transistors used in the circuit all have the smallest possible length and width. Input voltage V_{in} is represented by a square wave having an amplitude of 3V and a rise time of 100ns. The current injection into the bulk I_m of the last inverter is measured and is about 100nA. For estimating a complete digital circuit, an amount of 1000 transistors switching simultaneously is chosen, giving a current of 100µA.

The resistance of silicon can be calculated by:

$$R = \frac{L}{Q \cdot x_j \cdot W} \tag{3.7}$$

Where L is 1.86cm representing the length of the electrode, W is 400µm representing the width of the electrode, x_j is 700µm representing the junction thickness (in this case the thickness of the silicon wafer) and Q is 20Ω/cm representing the conductivity [24]. Filling in these values into Equation 3.7 results in Equation 3.8:

$$R = \frac{1.86cm}{20\Omega/cm \cdot 0.07cm \cdot 0.04cm} = 33.2\Omega \tag{3.8}$$

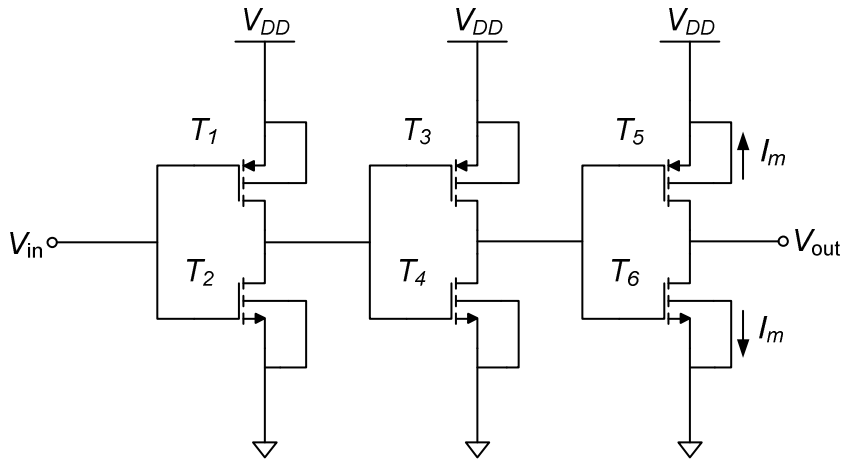

Figure 3.16: Inverter schematic with 3 inverters

The voltage drop created in the silicon will be:

$$100\mu A \cdot 33.2\Omega = 3.32mV \tag{3.9}$$

The estimation is based on the worst case situation and when all transistors switch at the same time. Normally, the transistors will not all switch at the same time. Nonetheless, the digital noise will have large values.

Some precautions should be made:

1. The digital part can be held in a stable state during sampling. This will reduce the amount of digital noise significantly.
2. The digital noise can be estimated by counting the amount of switching actions occurring over a certain amount of time and subtracting them later from the signal digitally.
3. Working with separated bulks and guard rings is desirable.

System validation

The system is built in Cadence using ideal components from the AMIS library and is depicted in Figure 3.17. Voltages V_{in1} to V_{in8} represent the voltages coming from the electrodes. Data measured during a first run at 8 electrode contacts in a patient is offered at these inputs. Attenuators A_1 to A_8 are realized by voltage controlled voltage sources having a gain of 0.05. Switches S_1 to S_8 represent the multiplexer. Every switch is closed for 1µs in a total period of 40µs. Switch S_1 does not have any delay. Every subsequent switch has a delay of 5 µs.

The switches used as multiplexer also act as a part of the sample and hold system for conversion to the charge domain. The sampled signal is stored in capacitor C_1 which is shorted by S_9 between every sample. In this simulation, the DAC is represented by inverted multiplexed predicted signals of input voltages V_{in1} to V_{in8}. The predicted signals used are actually a second run of the data measured at the 8 electrode contacts of a patient. To convert these signals to the charge domain, components C_2, S_{10} and S_{11} are added. The signal coming from the DAC is sampled in the same way as the signals coming from the attenuators.

By closing switches S_{12} and S_{13}, the charges stored in C_1, C_2 and C_3 are averaged resulting in a residual charge, which is the difference between the predicted signal and the patients signal. If C_1=C_2=C_3, the average voltage V_x is represented by Equation 3.10.

$$V_x = \frac{V_{C_1}+V_{C_2}+V_{C_3}}{C_1+C_2+C_3} \tag{3.10}$$

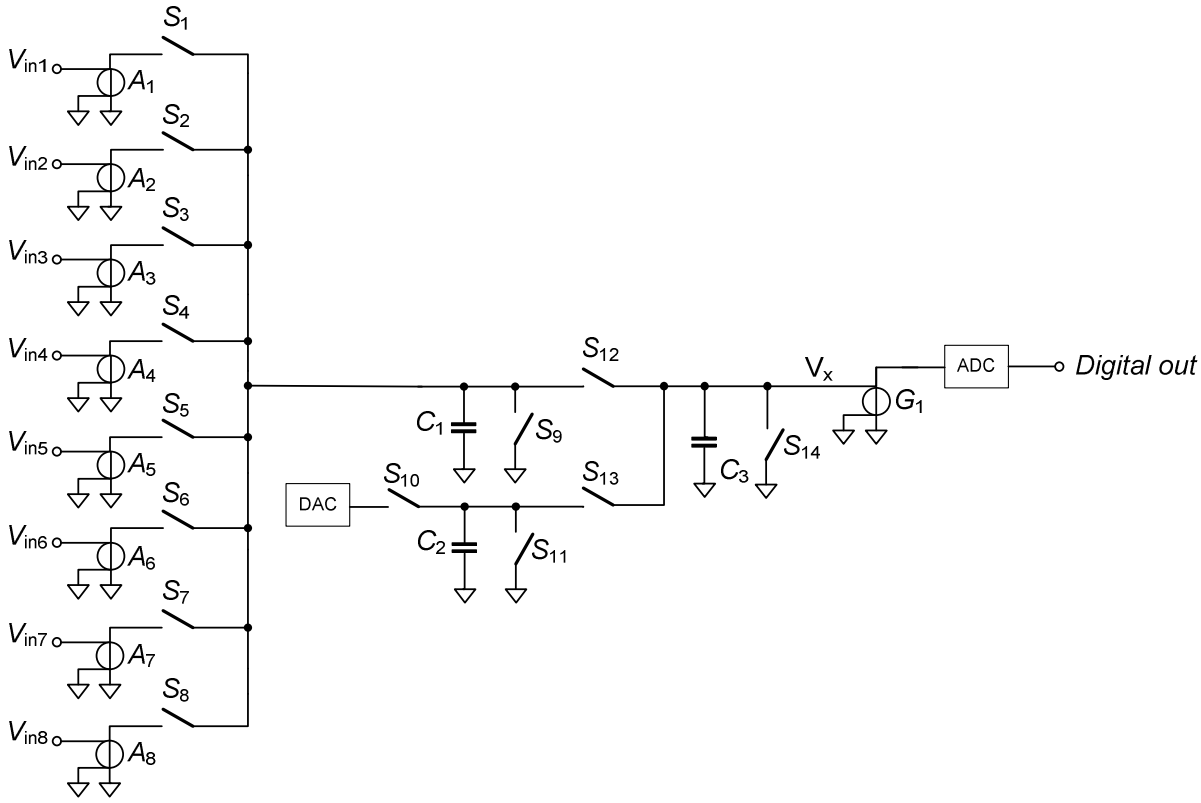

Figure 3.17: High level cadence schematic of the proposed system

This residual charge is stored in C_3 and amplified by amplifier G_1 to levels suitable for the *ADC*. Switch S_{14} blanks capacitor C_3 in order to prepare it for the next sample.

Figure 3.18.a shows the output of amplifier G_1, consisting of the 8 multiplexed input signals each having a predicted signal subtracted and amplified 100.000 times.

Figure 3.18.b shows a zoom in on the output signal consisting of the separate multiplexed inputs in which the first peak is the signal coming from electrode 1, the second peak from electrode 2, the third peak from electrode 3 and so on until all 8 electrodes are sampled. Then it starts again at electrode 1, which is the ninth peak. This signal can be applied to the ADC converting the signal to the digital domain.

If a single peak is evaluated, it can be seen that the peak rises very rapidly followed by a part rising slower, in Figure 3.18.b indicated with *vertical part* and *sloped part* respectively. During the vertical part, capacitor C_3 is charged through closed switches S_{12} and S_{13}. During the sloped part, the capacitor is charged through the parasitic resistance of open switches S_1 to S_8 and S_{10}, until the closed switches are opened. This problem can be solved by enlarging the open switch parasitic resistance.

It can be said that the system works properly. Ideally, the system can reach very high dynamic ranges. This mainly depends on the quality of the predicted signal. Noise contribution of the components, charge injection and distortion is not taken into account. The non-ideal system will therefore have lower specifications than this ideal system. To make the output of the system visible, the ideal system uses an amplifier having a gain of 100.000 times. In reality, this will be 100 times less enabling the non-ideal system specifications to be lower than the ideal system.

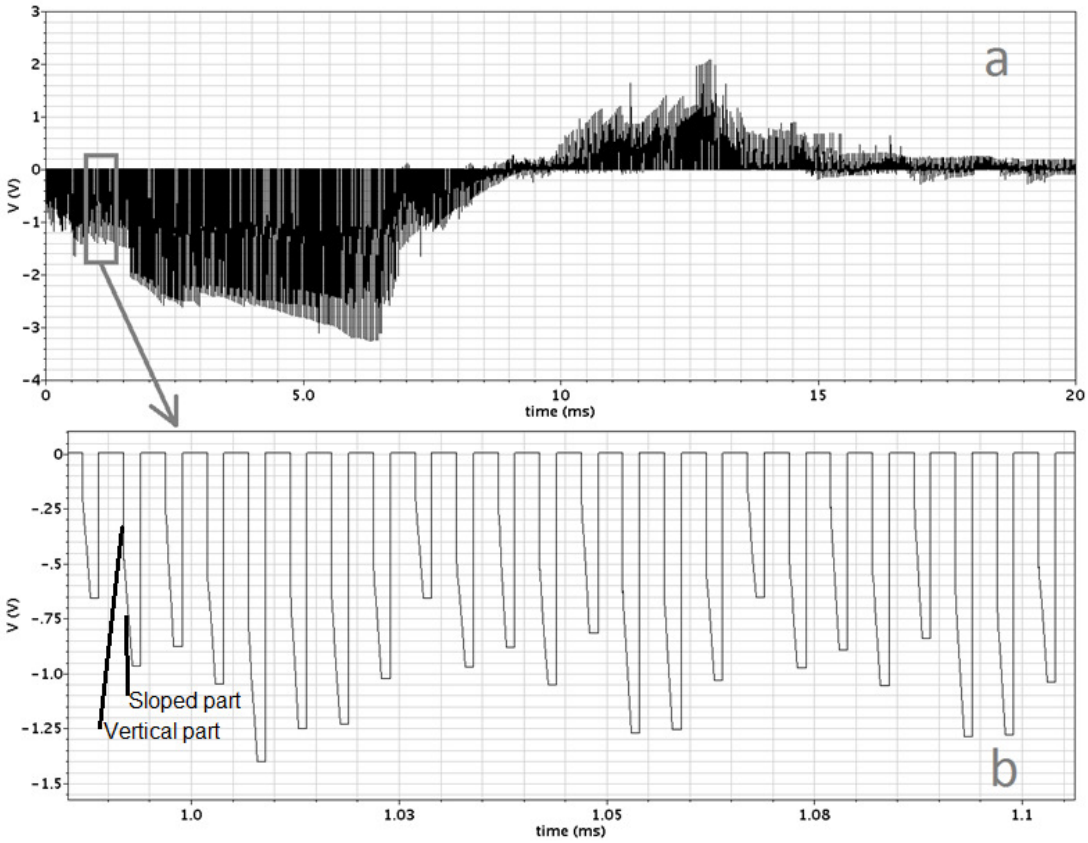

Figure 3.18: Output of amplifier G_1

The next chapter will handle the design considerations of the attenuator system block. The design of the attenuator system block will be very time consuming in order to let it comply with all the specifications mentioned earlier in terms of noise, dynamic range, input signals above supply level, space consumption and power consumption. Because of this reason, this thesis will only handle the design of the input attenuator. The rest of the system has to be developed further in a future project.

Chapter 4: Input stage design considerations

In this chapter, the design of an attenuator, which plays a big role in the neural readout system is described.

4.1. Input attenuator system concepts

To read out the complete evoked compound action potential, several techniques can be considered. They will be discussed in the next subsections.

4.1.1. Resistive divider

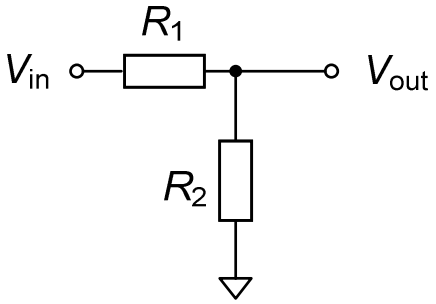

Figure 4.1: Resistive dividing network

A resistive divider is the simplest option. Figure 4.1 shows the resistive divider consisting of two resistors in series going from the input to ground. The node between the two resistors and the ground is taken as the output terminal. The output voltage can be measured at the V_{out} node. Because the resistive divider is a passive circuit, no extra power will be consumed. Using resistors as attenuator has certain drawbacks.

- A resistor is a space consuming element and will not fit on the electrode.
- The resistors introduce noise according Equation 4.1.

$$V_n = 4 \cdot K \cdot T \cdot R \tag{4.1}$$

  The input impedance has to be high to prevent loading of the electrode causing a high noise contribution.
- By attenuating the input signal by 20, the smallest voltage will not be 10µV, but 0.5 µV. Noise and accuracy specifications for the circuitry following the attenuator become higher causing the power consumption to rise.

4.1.2. Conventional switched capacitor

A switched capacitor circuit can be used. No attenuator will be present, but the input voltage is switched and directly stored into a capacitor.

The input transistors which will be used should be able to handle voltages up to 20 volt. Special high voltage transistors will be needed in order to do so causing space consumption to rise dramatically. To switch the transistor, supply voltages exceeding the supply voltage are required. They should be higher than the input voltage plus threshold voltage of the transistor.

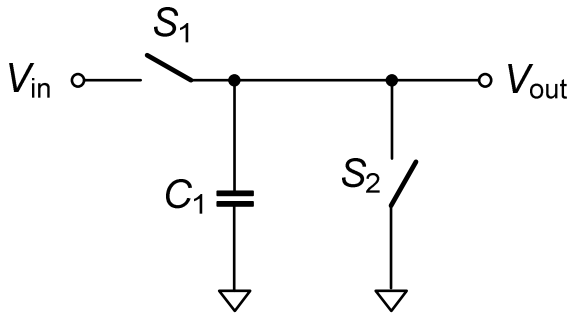

Figure 4.2: Conventional switched capacitor circuit

Figure 4.2 shows a switched capacitor circuit in which switch S_1 represent the input switch, capacitor C_1 is the capacitor for charge storage and switch S_2 the switch for shorting the charge stored in capacitor C_1.

To switch high voltage transistors, a floating voltage source, also called bootstrapping, can be used. Figure 4.3 shows the bootstrapping principle. It consists of a capacitor C_1 which can be charged by the normal supply by closing switches S_1 and S_2. When the capacitor is charged, switches S_1 and S_2 are opened and switches S_3 and S_4 are closed for applying the voltage of the capacitor to the gate of the high voltage transistor T_1 by terminal V_G and to the source of the high voltage transistor T_1 by V_S. The capacitor voltage is put on top of the input voltage V_{in} causing the high voltage transistor to switch. An important drawback for this method is the usage of high voltage transistors for the switches which increasing the chip area consumption. To save space, the capacitor can be replaced by the parasitic capacitance of a transistor. This transistor has to be put into a high voltage well which will cause the size of the transistor to rise. Hence, the system becomes too big.

The same holds for a system with a locally generated high voltage. A charge pump will be needed. These devices are very lossy causing an increase in power consumption. Besides that, charge pumps make use of several capacitors making the system too big for placing at the electrode.

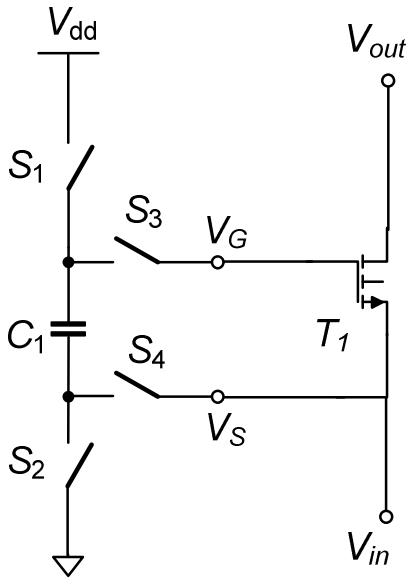

Figure 4.3: Bootstrapping

4.1.3. Multiplicative companding

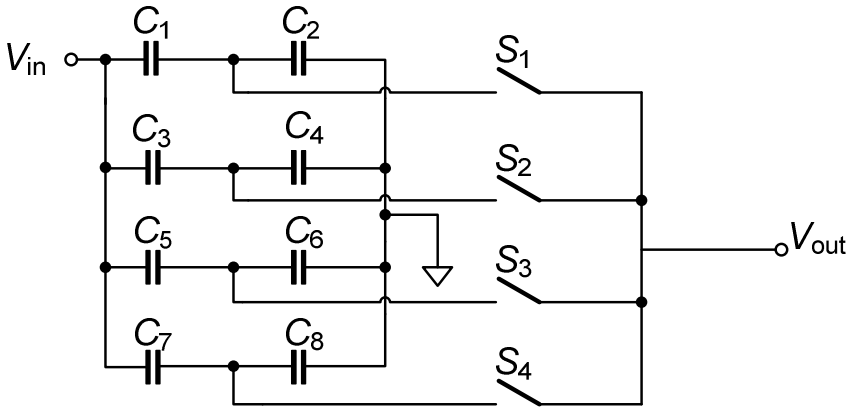

Figure 4.4: Multiplicative companding principle

Multiplicative companding is a technique for compressing the input signal to reasonable voltage levels which can be handled by circuitry operating in the low voltage domain while an optimal attenuation is achieved. The input signal is applied to several capacitive dividers shown in Figure 4.4. Dividing factors of capacitors C_1 and C_2, C_3 and C_4, C_5 and C_6, C_7 and C_8 are ½, ¼, $1/8$, $1/16$, respectively. Switching moments of S_1 to S_4 depend on the amplitude of input voltage V_{in}. If the signal is small, S_1 will close, if the signal is large, S_4 will close.

Output curves are depicted in Figure 4.5. The input signal used is a half sine wave, which is the dashed line. The output signal is represented by the solid line. When the input signal is small, the lowest attenuation factor is used. At point 1, the signal becomes too large and a bigger attenuation factor is used. At point 2 again the signal becomes too large and a bigger attenuation is used. When the signal becomes too low, a smaller attenuation factor is chosen, which is at point 3. This sequence repeats until the lowest attenuation factor is reached again, which is at point 4.

The signal to noise ratio decreases as the compression of the signal becomes higher. At high compression, it will be more difficult to read out the neural response. After digitization of the signal, the signal will be expanded to the original signal. A high dynamic range can be achieved and overloading of subsequent circuitry is prevented [25]. Just as the resistive divider, also multiplicative companding will not meet the noise requirements. The capacitors used have to be high voltage types, because the voltage over the capacitive dividers and capacitors itself will rise above the supply voltage. The switches which will be used should be high voltage transistors too. This makes the circuit very bulky.

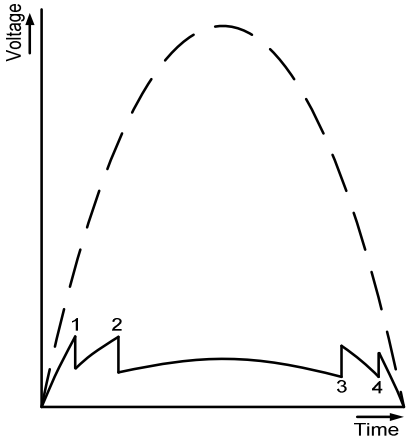

Figure 4.5: Output voltage of the multiplicative companding circuit

4.1.4. Folding ADC

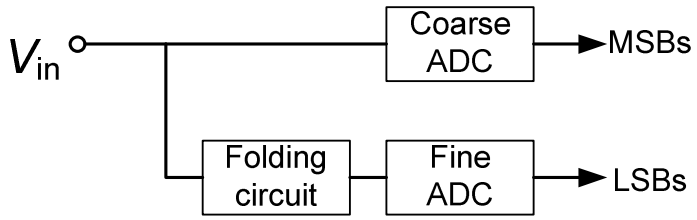

Figure 4.6: System block schematic of a folding ADC

A folding ADC consists of two ADCs; a coarse and a fine ADC. It is a technique to reduce the amount of comparators needed in ADCs. The coarse ADC is used for determining a coarse signal value resulting in the most significant bits (MSBs). The fine ADC is used for precise determination of the signal value resulting in the least significant bits (LSBs). The fine ADC is preceded by a preprocessing circuit for folding the signal. This circuit consists of several folding cells. The principle is depicted in Figure 4.6. The folding circuit folds the signal and thereby keeps its output voltage low.

Figure 4.7 depicts a plot consisting of the input and output signal. If the input signal is directly offered at the input of an ADC, the normal ADC input curve is obtained. If the signal is folded, the folded ADC input curve is obtained. The coarse ADC can be realized by giving a trigger for every folding action [26]. The high voltage input signal is attenuated to a low voltage signal for the ADC. Each folding cell consists of high voltage components in order to handle the high input voltage levels using a large amount of chip area compared to their low voltage equivalents.

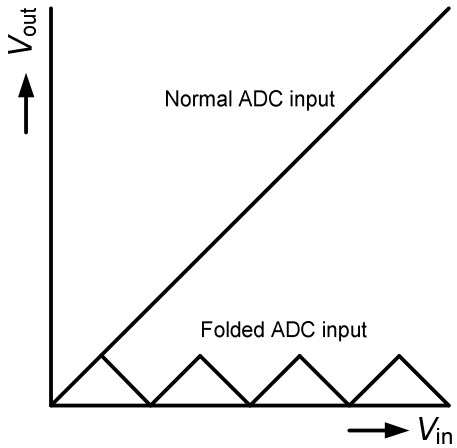

Figure 4.7: ADC input voltages with and without folding

4.1.5. ΣΔ ADC

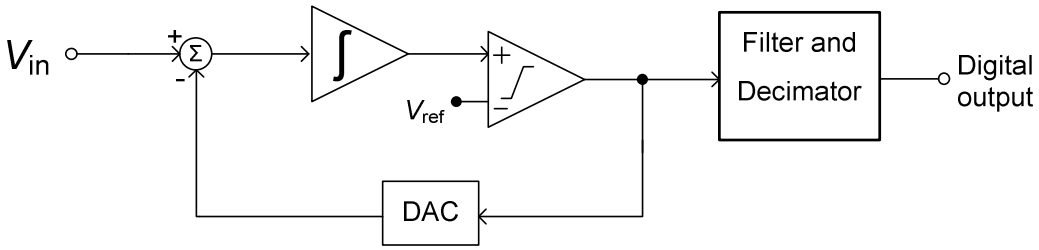

Figure 4.8: System block diagram of a ΣΔ converter

A sigma-delta ADC basically consists of one comparator, integrator and a DAC. The integrator integrates the incoming signal and after that, the signal is compared with a reference signal. The output of the comparator is send to the DAC and to a filtering and decimator block. The output signal of the DAC is added to the input signal. This sequence is repeated until the value of the input is determined. The filtering and decimator block makes the signal suitable for processing in a digital circuit. Figure 4.8. depicts the block system diagram. The converter can typically convert up to 24 bits. High dynamic ranges in combination with low noise levels can be achieved. The power consumption is quite high compared to other ADC architectures [27]. Just as in the previous case, high voltage components will be needed causing a high chip area consumption.

All principles discussed are having drawbacks making them unsuitable for application as input stage. A new technique called additive instantaneous companding will be proposed in the next section solving these issues.

4.2. Additive Instantaneous Companding design

To read out the evoked compound action potential completely, a new technique is developed. This section describes the design and implementation of this topology in detail of system and ideal circuit concept levels.

4.2.1. System design

A system-block diagram is depicted in Figure 4.9. Input voltage V_{in} represents the signal coming from the electrode. The signal is applied to a gain stage representing a capacitive division factor created by capacitors.

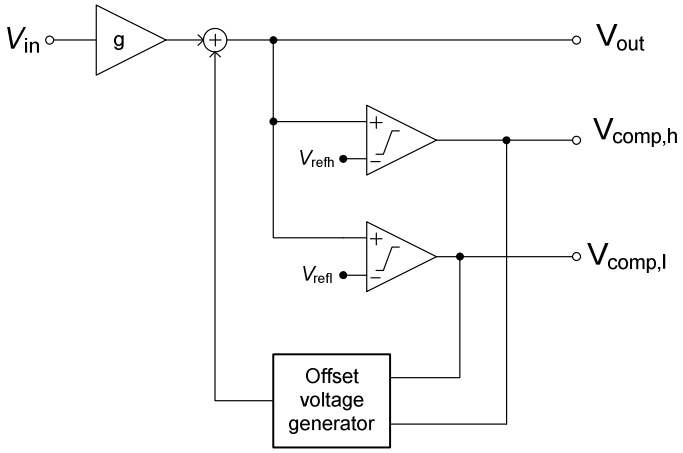

Figure 4.9: system-block diagram of the input attenuator

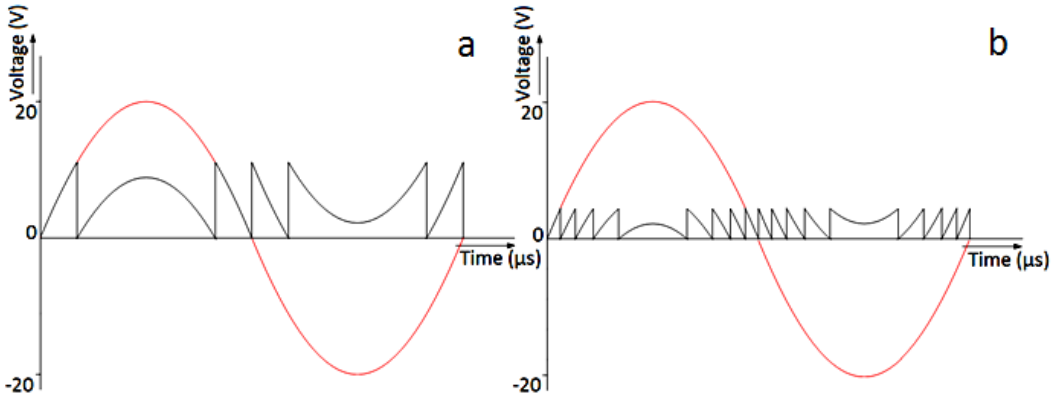

Figure 4.10: Two plots of the input and output signal at different reference levels

A control loop will be needed in order to short the capacitor at the right voltage. After the gain stage, an addition block is present. This block adds offsets generated by an offset generator to the output signal.

The offset generator creates a positive or negative offset depending on its input pulse. To measure if the output signal level is within boundaries, two comparators are added. One having a high reference voltage and one with a low reference voltage. If the high reference voltage is exceeded by a higher output voltage, the comparator will become high and thereby enabling the offset generator to give a negative offset. If the low reference voltage is exceeded by a lower output voltage, the comparator will become high and thereby enabling the offset generator to give a positive offset.

Figure 4.10 depicts two plots of the input signal and the output signal. The input signal is a sine wave having an amplitude of 20 volt. The output signal consist of the input sine wave with added offsets. Plot (b) has a lower reference level than plot (a) resulting in more offsetting steps. Every time a comparator output is high, this output will also be used for reconstructing the original signal digitally. Digital reconstruction of the signal is only possible if the exact value of the offset voltage is known. By defining exact switching and reference voltages, this is possible. It is the first step in the analog to digital conversion. The concept can be compared with a folding ADC. The difference between a folding ADC and the technique used here is that a folding ADC inverts the slope of the signal as soon as it gets too large. This concept offsets the voltage with a certain value.

To obtain a proper accuracy, the overshoot of the signal should remain below 10µV. This will be a critical point in the design of this system.

Figure 4.11 depicts a capacitive divider. Capacitive dividers do not introduce noise and consists of only two components. A capacitive divider is actually a division of charges over the two capacitances. One of the capacitors can be shorted, causing the charge present in this capacitor to be removed, which results in a voltage of 0 volt over the shorted capacitor. The charge in the other capacitor will remain the same. Taking an attenuation approaching 1 for the capacitive attenuator, in combination with shorting the capacitor, output voltages can be kept low.

The input V_{in} can have an offset at the start of the measurement due to residual charges in the capacitances. To prevent this, a shorting circuit is required. By shorting the capacitors, the system is calibrated. Shorting of the residual charges will be performed by charge balancing circuitry used in the stimulator [28].

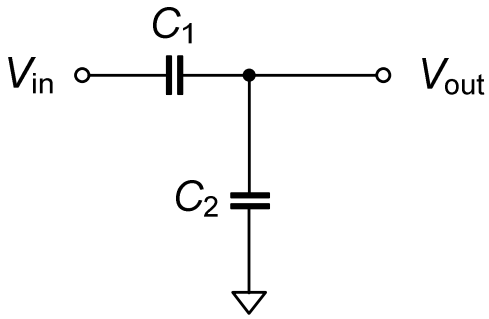

Figure 4.11: Capacitive divider

For referencing the floating output node V_{out} between the two capacitors C_1 and C_2, this node will be shorted to V_L or V_H.

The circuit basically *compresses* the signal by *adding* or *subtracting* a certain offset as soon as a threshold is reached. The signal will be *expanded* in the digital domain just as the multiplicative companding. This new technique will be called *"Additive Instantaneous Companding"*. Next section will tell more about the system design of additive companding.

4.2.2. Ideal circuit design

The switched capacitor circuit depicted in figure 4.12 is proposed. It consists of only two capacitors, two switches and two sources; a high voltage capacitor C_1 and a low voltage capacitor C_2, a switch S_1 to offset to a low voltage source V_L and a switch S_2 to offset to a high voltage source V_H. Voltage V_{in} represents the input voltage coming from the electrode. As soon as the signal V_{out} over the low voltage capacitor C_2 becomes too large, it is offsetted to a low reference source V_L by closing switch S_1. Low reference source V_L can be a voltage, current or charge source. The high voltage capacitor is charged to V_{in}. The signal over the low voltage capacitor can rise again as the input rises. For negative slopes of the signal, the same can be done, but now the capacitor is offsetted to a high reference source V_H by closing switch S_2. High reference source V_L can be a voltage, current or charge source.

The amount of offsets can be count and used to reconstruct the signal digitally. Capacitances can be kept very small to save space. No high voltage transistors are needed. The circuit can be built up consisting of only low voltage components and one high voltage capacitor. The circuit is power efficient, will have low noise contribution and will not consume a lot of space. This circuit is able to handle high dynamic input ranges. It makes the circuit suitable for application in the readout circuitry of the cochlear implant.

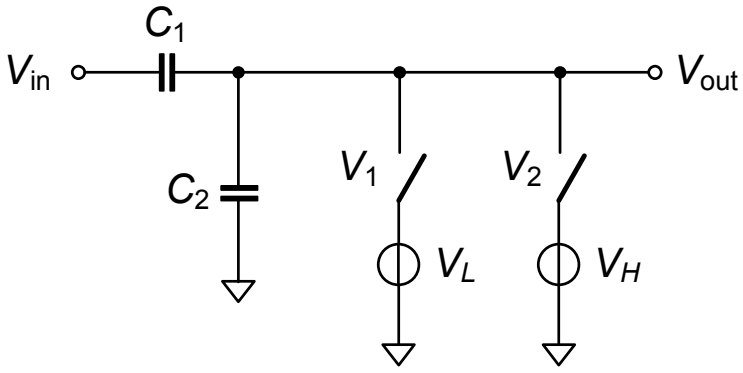

Figure 4.12: Schematic of the blanking capacitor concept

Chapter 5: Implementation switched offsetting in voltage domain

This chapter discusses the practical voltage domain design issues of the proposed circuit. First, the ideal circuit design is discussed, followed by the implementation into CMOS. Simulation results will be discussed and, finally, control loop issues will be discussed.

5.1. Ideal circuit design

The system block diagram is designed, but it is not yet verified. In this section, the system diagram will be converted to an ideal voltage domain circuit diagram. Figure 4.12 shows a voltage domain circuit diagram in which voltage V_{in} represents the input voltage coming from the electrode. Gain stage *g* depicted in Figure 4.9 is formed by the connection of two capacitors C_1 and C_2 giving Equation 5.1. Their series impedance is assumed to be much smaller than the source (tissue) impedance.

$$\mathrm{g} = \frac{C_1}{C_1 + C_2} \tag{5.1}$$

The ratio of them can be chosen such that the gain will be almost 1. The offset voltage generator can be realized by two simple switches S_1, S_2 and two voltage sources, V_H and V_L for a high and low reference voltage, respectively. The voltages are chosen to be different from V_{refh} and V_{refl} of the control loop of Figure 4.9 to prevent oscillation. Switch S_1 together with V_L represent the offset voltage generator to reset to a lower voltage across C_2. Switch S_2 together with V_H represent the offset voltage generator to reset to a higher voltage across C_2. The circuit can be represented by Equation 5.2 in which *floor* stands for rounding down to integers. For example 0.8 becomes 0 and 5.2 becomes 5.0.

$$V_{out} = \mathrm{g} \cdot \left[V_{in} - (V_{TH1} - V_L) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_{TH1} - V_L} \right) + (V_H - V_{TH2}) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_H - V_{TH2}} \right) \right] \tag{5.2}$$

Accuracy of the system is crucial for the correct operation of the circuit.

The switches are controlled by the control loop depicted in Figure 5.1. Every switch has its own control loop. The control loop used for switch S_1 will have a high reference voltage. As soon as the input signal V_{in} reaches V_{ref}, the *comparator* output V_S will become high. This will activate the *single shot* giving a pulse of 20ns to switch S_1. This switch will close, discharging capacitor C_2 to the low reference voltage V_L. The control loop for switch S_2 will have a low reference voltage. As soon as the input signal V_{in} drops to V_{ref}, the *comparator* output V_S will become high. This will activate the *single shot* giving a pulse of 20ns to switch S_1. This switch will close, charging capacitor C_2 to the high reference voltage V_H.

The ideal comparator used in Cadence is actually just a voltage controlled voltage source with a gain of 100.000 times, having no delay time and no offset. The pulse width of the single shot is chosen to be 20ns for closing the switch long enough for offsetting the signal properly. The low reference voltage V_L is chosen at 90mV and the high reference voltage V_H is chosen at 990mV.

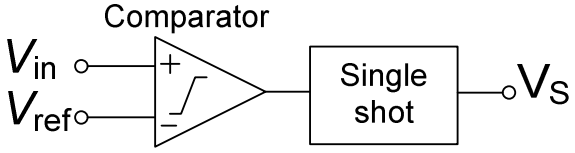

Figure 5.1: Control loop

For determining the required switching speed, the overshoot of the input signal should be kept within boundaries and the rise time of the stimulator should be known. Because the stimulator is not designed yet, an estimation is made, based on the circuit of M. van Dongen [28], who has done his thesis on neurostimulator circuits. His circuit is able to raise a voltage from 0 to 8 volt in 50µs. If an interval of 1 volt for every offset in the readout is taken, 8 switching steps are required in order to follow the generated signal. This implies that every offsetting step should be performed in less than 6.25µs. Within this time, it should also be possible for the ADC to make a sample. Therefore every offsetting step has to be performed in approximately 3µs.

Figure 5.3 depicts the output signal of the ideal circuit in Cadence having a sine wave with a frequency of 25kHz and an amplitude of 20 volt at the input. The output signal V_{out} goes up until the 1 volt reference. Switch S_1 is closed and an offset voltage over capacitor C_2 of 90mV is created. After that, the voltage can rise again and the sequence starts from the beginning. When the slope of the signal changes from positive to negative, the signal will decrease. The signal will reach 80mV, switch S_2 is closed and an offset voltage over capacitor C_2 of 990mV is created. After that, the voltage can drop again and the sequence starts from the beginning.

When a strong zoom in is performed, an overshoot of the signal of several tens of µV's is measured. This overshoot is caused by the delay of the control loop. Rise and fall times of the control loop can be made smaller; the overshoot of the signal becomes less and can be brought down to several hundreds of nV's. Ideally, the overshoot goes to zero.

The new input system level design output has a similar shaped output signal as the circuit described in [31], published in may 2010 at ISCAS2010. It consists of a neural response amplifier as input stage, followed by a delta generator switching as soon as certain thresholds are exceeded. This principle can be compared with the voltage domain implementation described in this thesis. Its application is however completely different. In this thesis, it is used for lowering the high voltage signal level appearing at the input with help of capacitors. The topology in [31] is used as a power efficient technique for the analog to digital conversion of low voltage (in the mV range) neural responses with help of a neural response amplifier.

The next step in the design can be taken; the implementation of the switched capacitor attenuator with non-ideal components in a technology which best suits for cochlear implants.

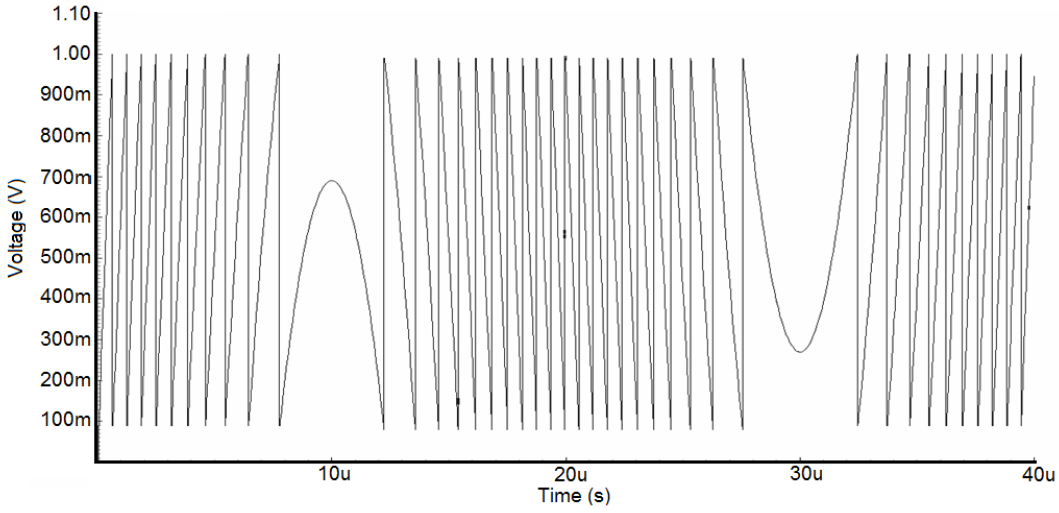

Figure 5.3: Output of the switched capacitor attenuator.

5.2. Practical design issues

This section will handle the implementation of the circuit discussed in previous section in a practical circuit using CMOS technology.

5.2.1. Technology

In order to make a good choice of the technology which will be used, an inventory of available technologies is made to provide the most suitable features:

- IBM
- Austria Micro Systems (AMS)
- IHP
- LFoundary
- TSMC
- UMC
- DIMES
- AMIS

A very important issue in choosing a technology is the ease of producing a prototype. Fabrication of the chip should be cheap and quick. In Delft, an in house technology from DIMES is available. This technology is not available within industry making it only suitable for experimental projects. Mass production will not be possible with this technology. Besides DIMES, an institution exist called Europractice. This company collects designs and put them on one wafer for fabricating. The production costs are shared over the amount of collected designs. This makes Europractice very cheap. Europractice is able to produce wafers in several technologies. The technology used for the circuit designed in this thesis should be able to handle high input voltages. In order to get an as large as possible freedom of design, a large set of high voltage components should be available. This makes the AMIS technology the most suitable for the circuit described here. The AMIS I3T25 technology has a very large number of well documented and tested high- and low voltage devices. The high voltage devices can handle voltages up to 25 volts. Besides that, the TU Delft has the design kit for the AMIS technology already in house. Because of these reasons, in this thesis the AMIS I3T25 technology will be used.

5.2.2. Non-ideal circuit

The ideal components can be replaced by non-ideal components chosen from the library of the AMIS technology.

Capacitors

The ideal high voltage capacitance can be replaced by a bar shaped metal to metal high voltage capacitor (mmchb) from the AMIS library. This capacitor has the highest capacitance per unit area. Capacitance can be calculated by Equation 5.3:

$$C = Length \cdot (C_{0\_p} + N_f \cdot C_{1\_p}) \tag{5.3}$$

In which

C_{0_p}=-9.94e-11

C_{1_p}=3.3e-10

If a capacitance of 1pFis desired, the parameters can be filled in the Equation obtaining a number of fingers N_f of 40 and a *Length* of 80.

The ideal low voltage capacitor is replaced by a metal-isolator-metal capacitor (mimc) from the AMIS library. Also this capacitor has the highest capacitance per unit area and can be calculated by Equation 5.4:

$$C = C_a \cdot Area + C_p \cdot Perimeter \tag{5.4}$$

In which C_a=1.5fF/µm^2 and C_p=0.34e-6fF/µm. If a capacitance of 600fF is desired, the parameters can be filled in the Equation obtaining a perimeter of 80µm and an area of 400µm^2. By filling in these parameters in the mimc model, length and width of the capacitance are automatically depicted. The length will be 20µm and the width will be 20µm.

Using these capacitor values, the attenuator will have a gain of 0.6. This parameter can be changed by changing the ratio of the capacitances.

Transistors

The ideal switches can be replaced by transistors. For offsetting to V_H, an NMOS transistor is used. The NMOS transistor selected from the AMIS library, is the enm transistor. For obtaining sufficient switching speed, an on-resistance R_{on} should be small resulting in a large width and parasitic capacitances should be small resulting in a small width. An optimum is found at 10 µm. In the small width regions (0.35 to 10µm) the width has a substantial effect on the switching speed. Above 10µm, the on-resistance R_{on} does not significantly change. Because of the limited space and power available, the transistor width is chosen to be 10um. The length is determined in the same way. The smaller the length, the faster the switching. In the region above 1um, the speed of the transistor will quickly decrease. Because of chip area, power limitations and switching speed, the length is chosen at 0.35µm.

For offsetting to V_L, a PMOS transistor is used. The length and width of the PMOS transistor is determined in the same way as for the NMOS transistor. The width and length for the PMOS transistor are the same as for the NMOS transistor. A width of 10 and a length of 0.35µm is chosen.

Figure 5.4 depicts the circuit with non-ideal components. Transistor T_1 offsets capacitor C_2 to reference voltage V_L and transistor T_2 offsets capacitor C_2 to reference voltage V_H. The control loop is kept ideal for now as shown in Figure 4.4. Switching sources V_{S1} and V_{S2} are representing the outputs of the control loop.

The circuit is simulated having a sine wave with an amplitude of 20V and a frequency of 25kHz as input voltage V_{in}. This input signal is kept the same throughout this whole chapter. Output voltage V_{out} is depicted in Figure 5.5. In order not to suffer from signals originating from parasitics, reference voltage V_L is raised to 100mV.

The offsetted output signal V_{out}, depicted in Figure 5.5.a, is amplified 0.6 times by the capacitive attenuator.

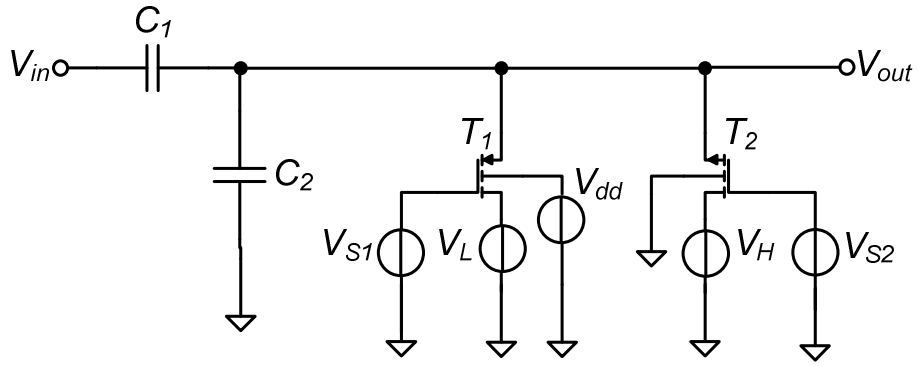

Figure 5.4: The blanked capacitor circuit with non-ideal components

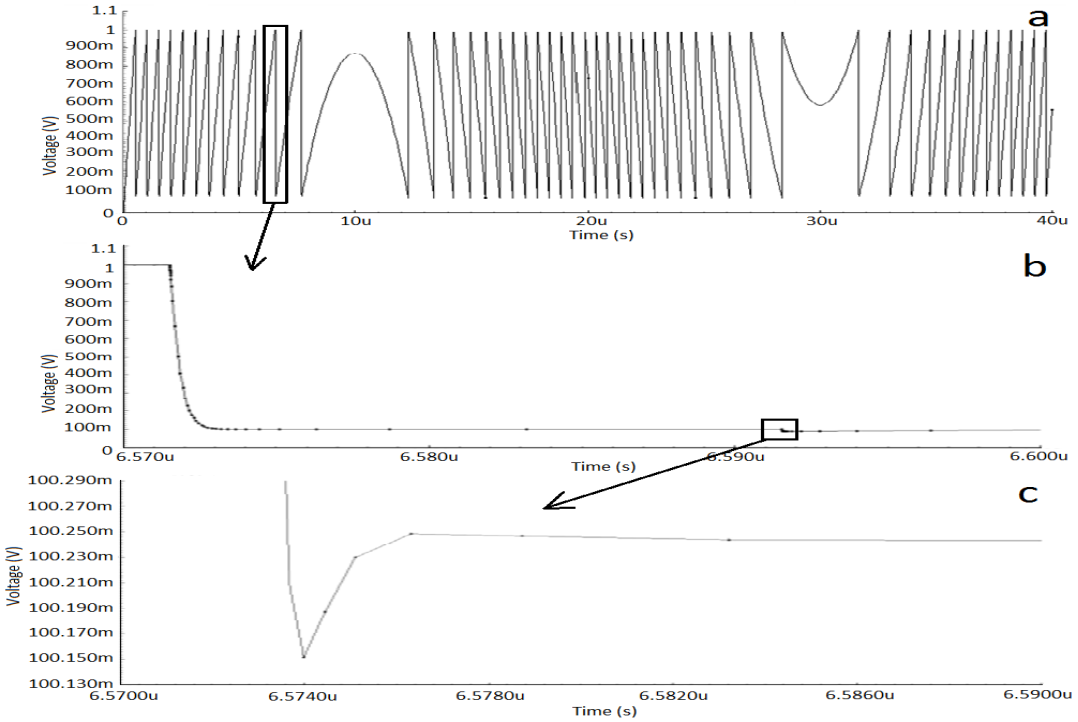

Figure 5.5: Transient output practical switched capacitor circuit

A zoom in on the offsetting of the signal is depicted in Figure 5.5.b. It can be seen that the slope of the signal changes as the signal is approaching the reference voltage of 100mV. At 6.592µs, the switch is opened again and a small step takes place.

Zooming in on this step, the graph depicted in Figure 5.5.c is obtained. The signal does not exactly reach 100mV, but floats approximately 250µV above 100mV giving an inaccuracy of the signal which is way too big. This deviation is caused by the R_{DS} of the transistor. At the beginning of the offsetting, V_{DS} is relative big. This also gives a large drain current I_D. When V_{DS} becomes smaller and, ideally, goes to 0, I_D also goes to 0 according to Equation 5.5 [36].

$$I_D = \frac{\mu_0 \cdot C_{ox} \cdot W}{L}\left[(V_{GS} - V_T) \cdot V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{5.5}$$

In which I_D is the drain current, L the transistor length, μ_0 the surface mobility of the channel, C_{ox} the gate oxide capacitance per unit area, W the transistor width, V_{GS} the gate-source voltage, V_T the threshold voltage and V_{DS} the drain-source voltage. To calculate R_{DS}, Equation 5.6 can be used [36].

$$r_{DS} = \frac{1}{\partial i_D / \partial v_{DS}} = \frac{L}{\mu_0 \cdot C_{ox} \cdot W \cdot (V_{GS} - V_T - V_{DS})} \tag{5.6}$$

In which R_{DS} is the drain to source resistance. From the Equation, it can be seen that if V_{DS} becomes small, R_{DS} will become bigger. To prevent R_{DS} to become too big, an extra reference can be added to the control loop for every switch. One reference $V_{ref,close}$ is used for closing the switch, one reference $V_{ref,open}$ is used for opening the switch and is reached before V_H or V_L is reached. The single shot is replaced by a flipflop.

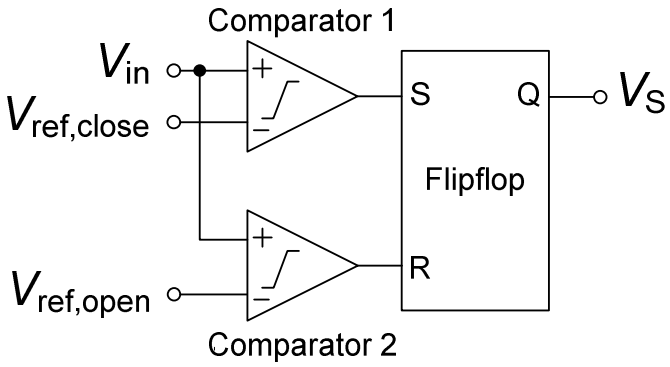

Figure 5.6: Modified control circuit

The adjusted control loop is depicted in Figure 5.6. As soon as the input signal exceeds $V_{ref,close}$, *comparator 1* becomes high, setting the *flipflop* and switching the transistor on. The *flipflop* holds the transistor on until it is reset by *comparator 2* which will become high as the input signal drops below $V_{ref,open}$. The control loop can switch fast enough making the circuit very accurate. Simulation results are depicted in Figure 5.7.

Figure 5.7.a shows a transient simulation of the circuit with modified control loop. Threshold levels are changed to 2.1 volt and 1.2 volt for offsetting to a lower voltage and 1.18 volt and 2.09 volt for offsetting to a higher voltage for creating better on/off switching characteristics of the transistors. Figure 5.7.b zooms in to the end of the offsetting. The signal reaches threshold $V_{ref,open}$ which is at 1.2V. The switch is opened and an offset is introduced due to charge injection caused by the switching. Section 5.2.3 will go into more detail about this.

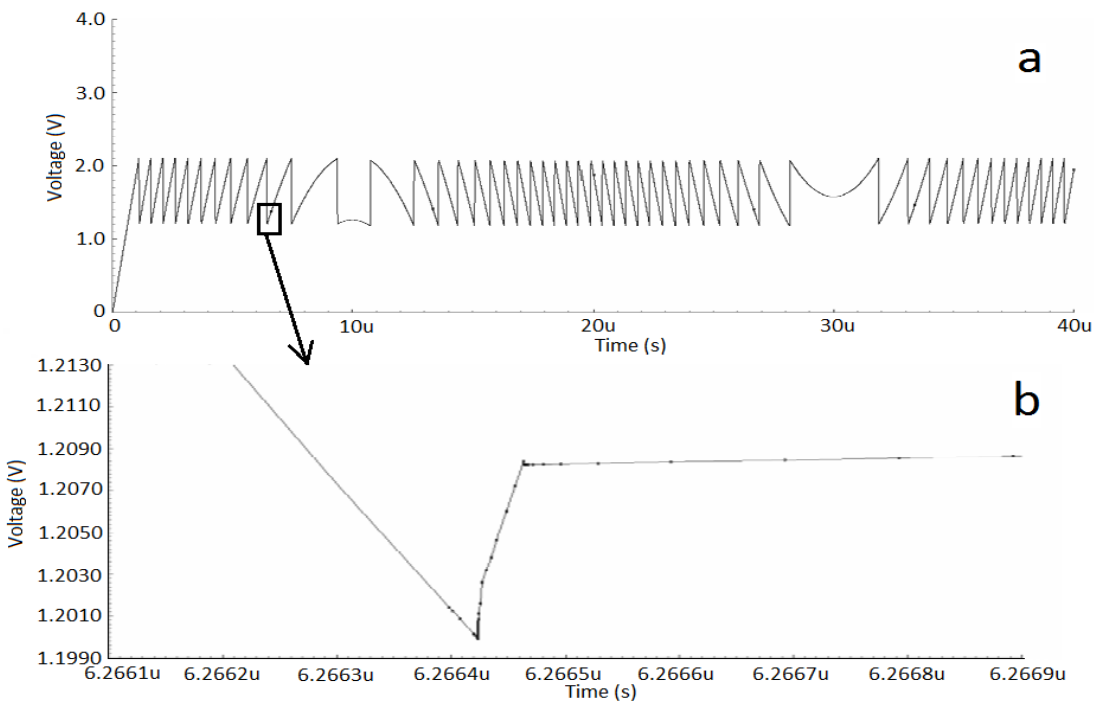

Figure 5.7: Simulation of the circuit with modified control loop

5.2.3. Charge injection

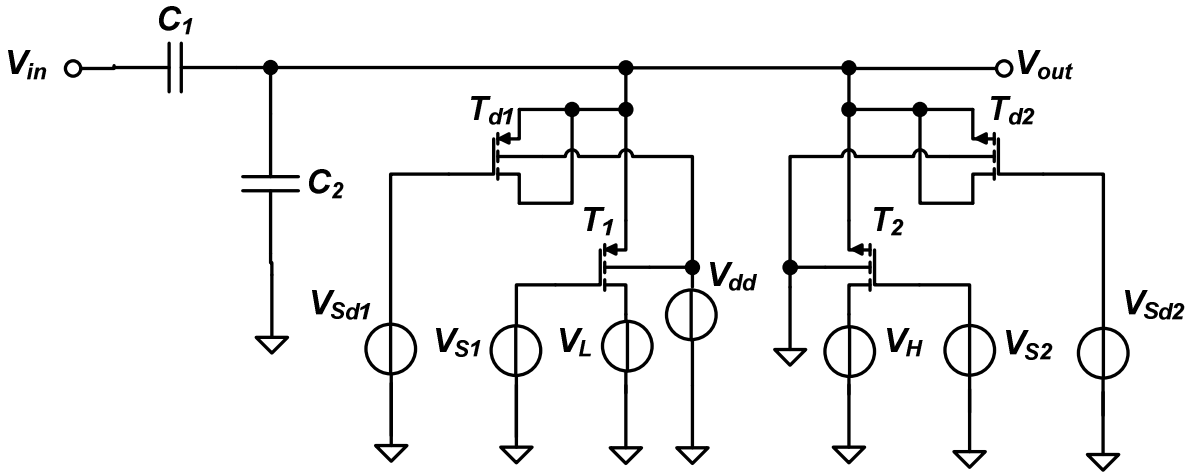

Figure 5.8: Circuit with dummy transistors

Because of the high accuracy needed in this circuit, charge injection plays a big role in the success of the design. As discussed in Section 5.2.2, charge injection can introduce deviations of several millivolts, where only 10µV is allowed. A reduction can be made by adding dummy switches having an opposite switching voltage of transistors T_1 and T_2. They will introduce a charge injection which is the opposite of the charge injection introduced by transistors T_1 and T_2 and thereby cancel the charge injection. The circuit with dummy transistors is depicted in Figure 5.8.

Figure 5.8 is basically the same as Figure 5.4. The difference is the added dummy transistors T_{d1} and T_{d2} and switching sources V_{Sd1} and V_{Sd2} which represent the inverted output of the control loop for steering transistors T_{d1} and $T_{d2.}$

Charge injection occurs because transistors have parasitic capacitances from gate to source and from gate to drain. The gate to drain capacitance of transistors T_1 and T_2 depicted in Figure 5.8 is not important because it is not connected to the signal side of the transistor. A dummy transistor is connected to the signal at its source and at the drain causing their parasitic capacitance to be twice the parasitic capacitance of transistors T_1 and T_2. Figure 5.9 depicts a dummy transistor T_d with its parasitic capacitances C_{GD} and C_{GS}.

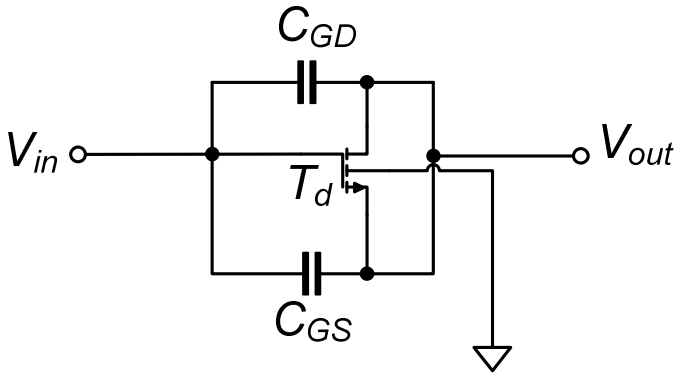

Figure 5.9: dummy transistor with parasitic capacitance

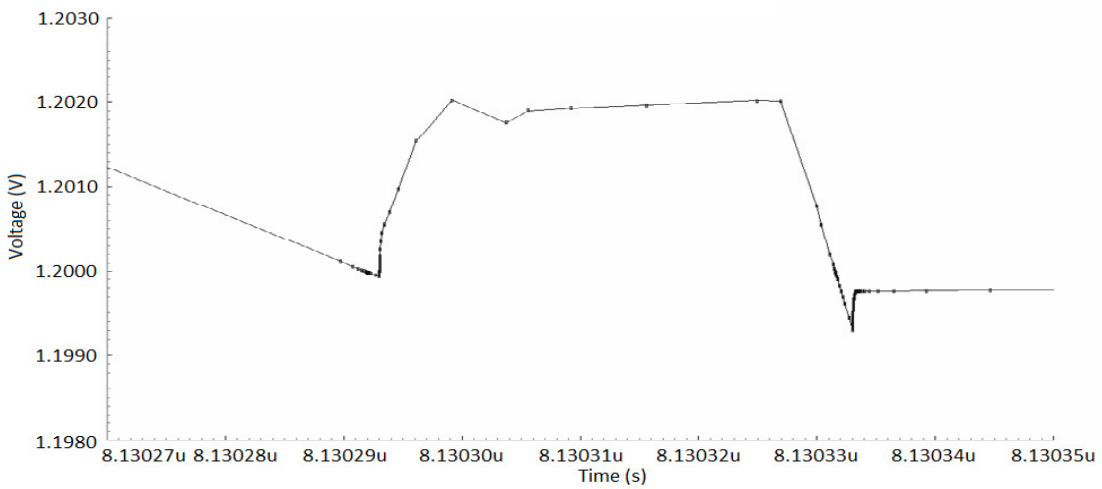

Figure 5.10: Charge injection cancellation at the end of the blanking

Input voltage V_{in} represents the inverse switching voltage coming from the control loop. Output voltage V_{out} represents the charge injection signal coming from the dummy transistor T_d. The dummy transistors are chosen at half the width and the same length as the switching transistors T_1 and T_2 obtaining approximately the same parasitic capacitance for the dummy as for transistors T_1 and T_2.

The schematic depicted in Figure 5.8 is simulated and a zoom in on the end of an offsetting step at the output signal is depicted in Figure 5.10. Output voltage V_{out} comes down to the reference voltage of 1.2 Volt. Then, charge is injected by switching transistor T_1 giving a deviation of approximately 2mV. Then, dummy transistor T_{d1} injects its opposite charge cancelling the charge injected by transistor T_1. The signal now only has some small deviation in the order of tens of microvolts due to mismatch of the transistors. A refinement of the circuit is needed in order to be able to meet the specifications which are discussed in Section 5.2.4.

5.2.4. Refinement of the circuit

Two problems give the need of an extra design step. These are:

- Charge injection, as explained in the previous section.
- Control loop delay, the offsetting does not stop exactly at the right output voltage level because of delay of the control loop. Although no signal information is lost, the offsetting is not accurate enough.

A solution to these issues is to take two offsetting steps instead of one. The offsetting can be divided in two parts:

- Coarse offsetting
- Fine offsetting

Both parts are discussed separately.

Coarse offsetting

Coarse offsetting is the circuit as it is designed already. The output signal can be offsetted to a reference voltage level, but still there is an offset caused by a residual of the charge injection and the overshoot caused by the control loop which is not fast enough. The course offsetting consists of the same components as in Figure 5.8. Coarse offsetting should happen before fine offsetting.

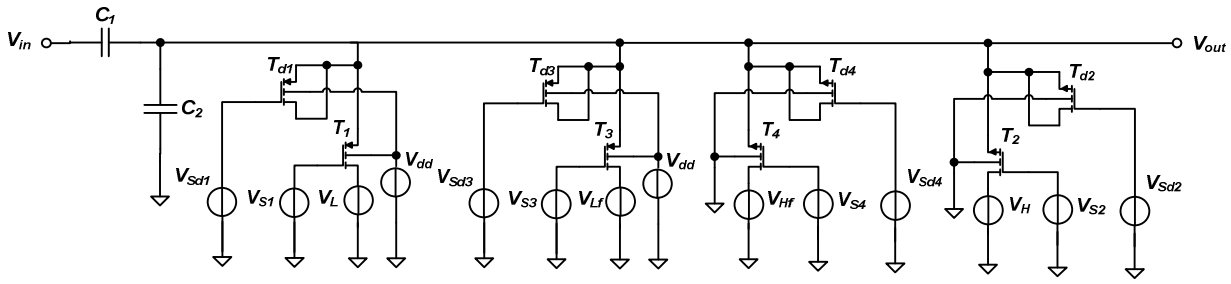

Figure 5.11: Switching circuit with coarse and fine offsetting

Fine offsetting

To get rid of the remaining charge injection and overshoot which could not be suppressed by the coarse offsetting circuit, a fine offsetting circuit is added. The fine offsetting is based on an extra transistor T_3 with dummy transistor T_{d3} for offsetting to reference voltage V_{Lf} and an extra transistor T_4 with dummy transistor T_{d4} for offsetting to reference voltage V_{Hf}. Those transistors are optimized for offsetting only very small voltages and to add a minimum of charge injection. To switch the extra transistors, the control loop needs to be extended with output V_{S3} and V_{Sd3} for offsetting to reference voltage V_{Lf} and output V_{S4} and V_{Sd4} for offsetting to V_{Hf}. The modified circuit containing course and fine blanking is depicted in Figure 5.11.

The fine offsetting transistors T_3 and T_4 have a length of 0.35 and a width of 1 which is 10 times smaller than the course offsetting transistors. Dummy transistors will also be 10 times smaller giving a length of 0.35 and a width of 0.5. Because of the small sizes of the transistor, offsetting to V_{Lf} or V_{Hf} by a comparator only is sufficient. Voltage deviation due to R_{DS} are less than 1µV, so specifications are met.

The extended control loop needed for controlling the fine offsetting transistors is depicted in Figure 5.12. The control loop consist of a part already depicted in Figure 5.6 for the course offsetting and a new part for fine offsetting. A *single shot* is present for closing switch S_1 enabling the fine offsetting control loop. The fine offsetting control loop will only be enabled when also the course offsetting starts. When the fine offsetting is enabled, *comparator 2* will directly control the fine offsetting transistor. The signal is inverted by *inverter 2* for controlling the dummy transistor.

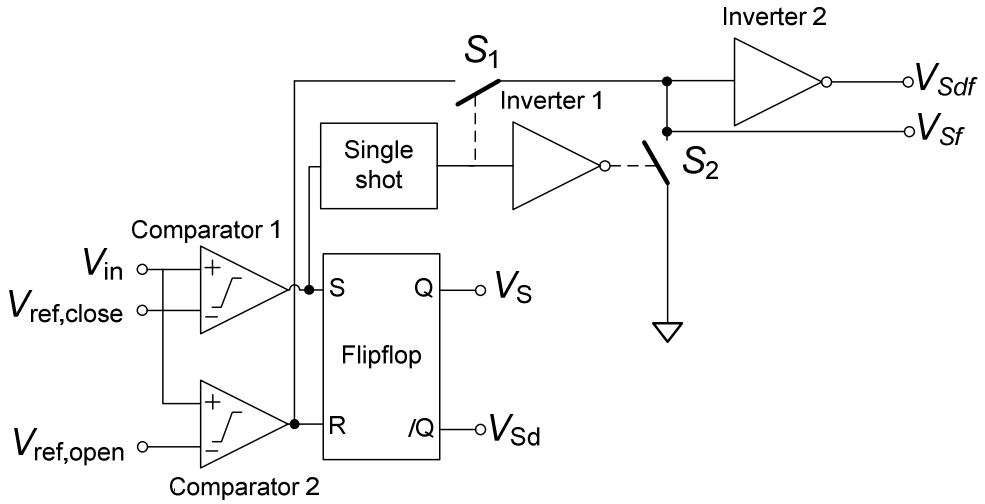

Figure 5.12: Control loop with course and fine offsetting ability

Inverter 1 resets the output signal by activating switch S_2. Two of these control loops are used. One for offsetting to a low reference voltage V_L and one for offsetting to a high reference voltage V_H. An accuracy better than 1µV is reached.

5.2.5. Component noise behaviour

To determine the noise behavior of the switching circuit, a noise simulation is done. The noise level should be beneath 10µV. Four states can be distinguished, presented in Table 5.1:

State	T_1	T_2
1	on	on
2 (offsetting)	on	off
3 (offsetting)	off	on
4 (resting)	off	off

Table 5.1: switching states

State 1 will not occur because then a short-circuit is created between V_H and V_L. The ADC will only sample during state 4. For obtaining an optimal noise behavior, all parameters of the circuit should be investigated separately. This is done by sweeping the component parameters for every state.

Figure 5.13 shows the noise level versus transistor width of the four states of a PMOS transistor. It can be said that the bigger the width, the lower the noise. Below 10µm, the noise rises very fast. The PMOS and NMOS transistors give the same result. The noise generated by T_1 and T_2 at a width of 10µm, is during and after offsetting below 10µV. The noise generated at a width of 1µm, chosen for T_3 and T_4, is also below 10µV during and after offsetting.

The same simulation is performed for the noise level versus the length. The PMOS transistor adds a minimum amount of noise between 0.35 µm and 1 µm. A length of 0.35 µm is sufficient for meeting the noise specification. For the NMOS, the minimum noise contribution is at 1µm, which will be used in the circuit.

The optimal noise behavior of the capacitors is achieved by choosing the capacitance as big as possible. Noise contribution of capacitors is much lower than transistors and low capacitances will not cause the noise level to exceed the noise specification. Capacitance values of the high voltage and low voltage capacitor do not have to be changed.

By changing the values for reference sources V_H, V_{Hf}, V_L and V_{Lf}, the noise behavior of the components can be tuned even more. Figure 5.14.a shows the noise contribution of PMOS transistors T_1 and T_3 due to the variation of voltage source V_L. At 0.9V, the noise contribution of PMOS transistors T_1 and T_3 at State 2 becomes smaller than the noise level of State 3.

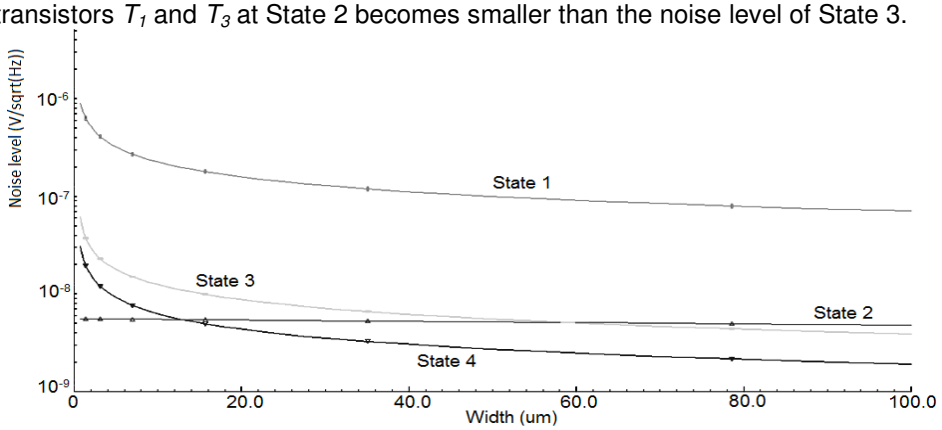

Figure 5.13: Transistor width variation for 4 different states

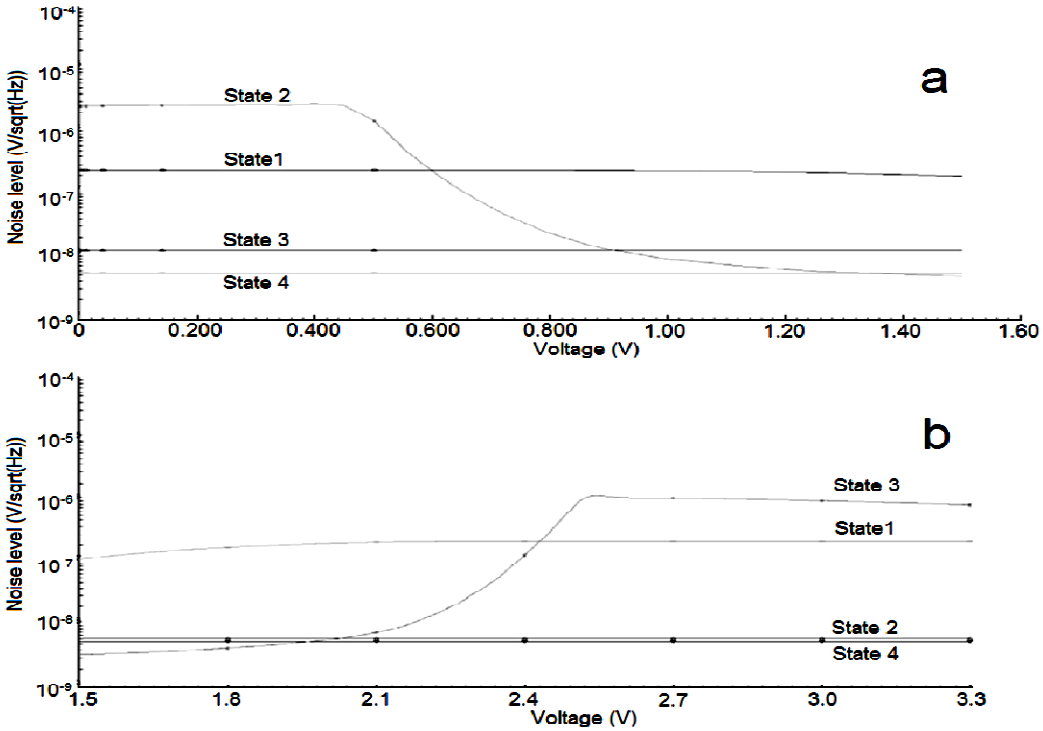

Figure 5.14: Voltage source variation

Figure 5.14.b shows the noise contribution of NMOS transistors T_2 and T_4 due to the variation of voltage source V_H. At 2V, the noise contribution of the NMOS transistors T_2 and T_4 at State 3 becomes smaller than the noise level of State 2. Values of reference sources V_H, V_{Hf}, V_L and V_{Lf} do not have to be changed. All components are now tuned for noise behavior. Next section will discuss about the total noise generated by the circuit.

5.2.6. Circuit noise behavior

A noise simulation of the complete, optimized circuit is performed. The complete noise contribution is again represented by the states discussed in the previous section. Figure 5.15 depicts the simulation results. During switching (States 2 and 3), the noise remains below 10µV. In rest (State 4), the noise is even lower. Three kinds of noise can be distinguished.

- 1/f noise
- Capacitor dielectric generated noise
- Channel conductance noise

1/f noise

The input referred low frequency noise region is dominated by 1/f noise and is represented by Equation 5.7.

$$\overline{V_n^{\,2}} = \frac{K}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f} \qquad (5.7)$$

In which K is a process dependant constant, C_{ox} is the gate oxide capacitance per unit area of the device, W is the width, L is the length and the 1/f factor the 1/f –noise frequency dependency. For the simulation, all parameters are fixed except W and L. By increasing W and/or L, the noise level will be lowered [29].

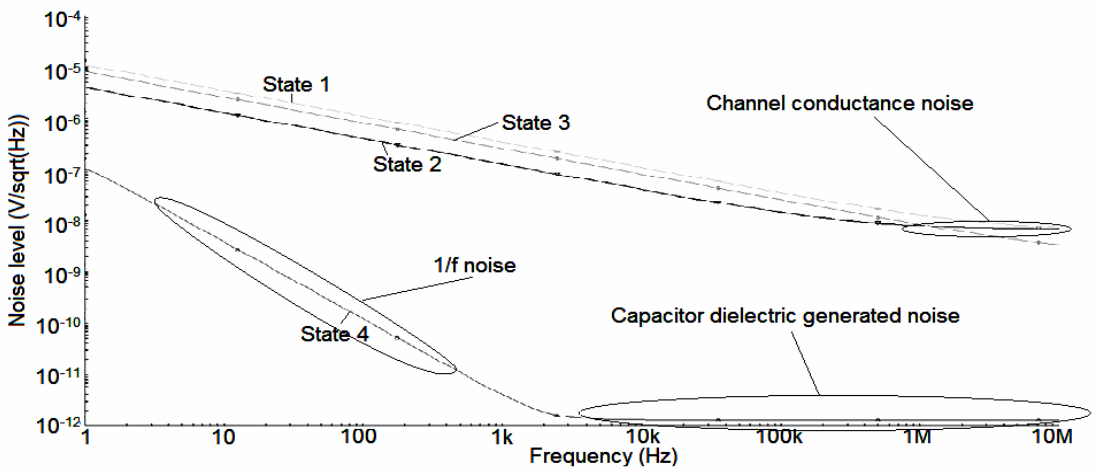

Figure 5.15: Noise simulation of the complete circuit

Capacitor dielectric generated noise

The high frequency region of State 4 is dominated by noise generated by the capacitor dielectric. It is fundamental noise which cannot be lowered as long as the capacitance is not changed.

Channel conductance noise

The input referred channel conductance noise can be seen at high frequencies in State 2 and is determined by the drain current I_d. Channel conductance noise is represented by Equation 5.8.

$$\overline{V_n{}^2} = \frac{4 \cdot k \cdot T}{g_m} \tag{5.8}$$

In which g_m is represented by Equation 5.9.

$$g_m = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \tag{5.9}$$

Merging Equations 5.8 and 5.9 together, Equation 5.10 is obtained

$$\overline{V_n{}^2} = \frac{4 \cdot k \cdot T}{\mu_n \cdot C_{ox} \cdot \frac{W}{L} (V_{GS} - V_{TH})} \tag{5.10}$$

In which k is the Boltzmann constant, T the absolute temperature, μ_n the mobility of charge carriers, C_{ox} the gate oxide capacitance per unit area, W the width of the device, L the length of the device, V_{GS} the gate source voltage and V_{TH} the threshold voltage. The only parameters which are not constants are W and L. The noise voltage V_n can be made smaller by enlarging L or decreasing W [36].

5.2.7. Replacing low voltage capacitor by parasitic capacitance of transistors

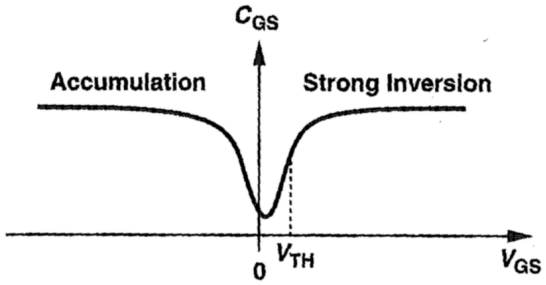

Figure 5.16: Parasitic capacitance versus voltage of a transistor [29]

To reduce chip area consumption, the low voltage capacitor can be replaced by the parasitic capacitances of the switching transistors. Those parasitic capacitances, however, have a voltage dependency according to Figure 5.16. Since the minimum gate-source voltage V_{GS} will be at 1.2V, the parasitic capacitors are in the relatively flat region making them, in combination with a calibration, suitable for application as low voltage capacitor.

5.3. Simulation results

For checking the validity of the designed circuit with ideal control loop, the output signal is expanded to its original signal in matlab. Temperature variations and the influence of and process corners of the designed circuit are investigated. Circuit calibration for improving accuracy is discussed.

5.3.1. Output signal and expanding simulation

Every time an offset is present in the output signal coming from the circuit, a reverse offset can be applied. Figure 5.17 shows a schematic for expanding the offsetted output signal V_{out}. The offsetted output signal is applied to the input of the expanding circuit as $V_{offsetted,in}$. The signal is compared with reference voltage V_{refh} for a positive offset compensation and with reference voltage V_{refl} for a negative offset compensation. When one of these values is exceeded, a pulse will be applied to a counter increasing its output value. The counter output is applied to an amplifier for creating the proper offset voltage. The offset voltage is added to the input signal and thereby expanding the signal. When the expanded signal crosses 0, both counters are reset for preventing the counters to run out of their output range.

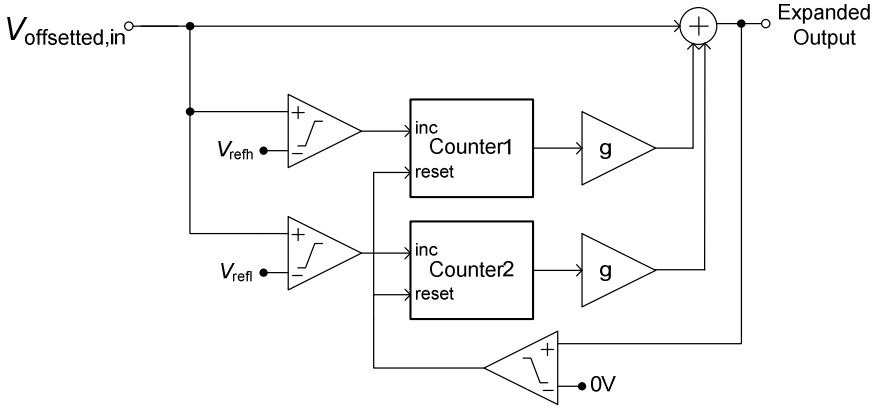

Figure 5.17: Simulink schematic for expanding the offsetted signal

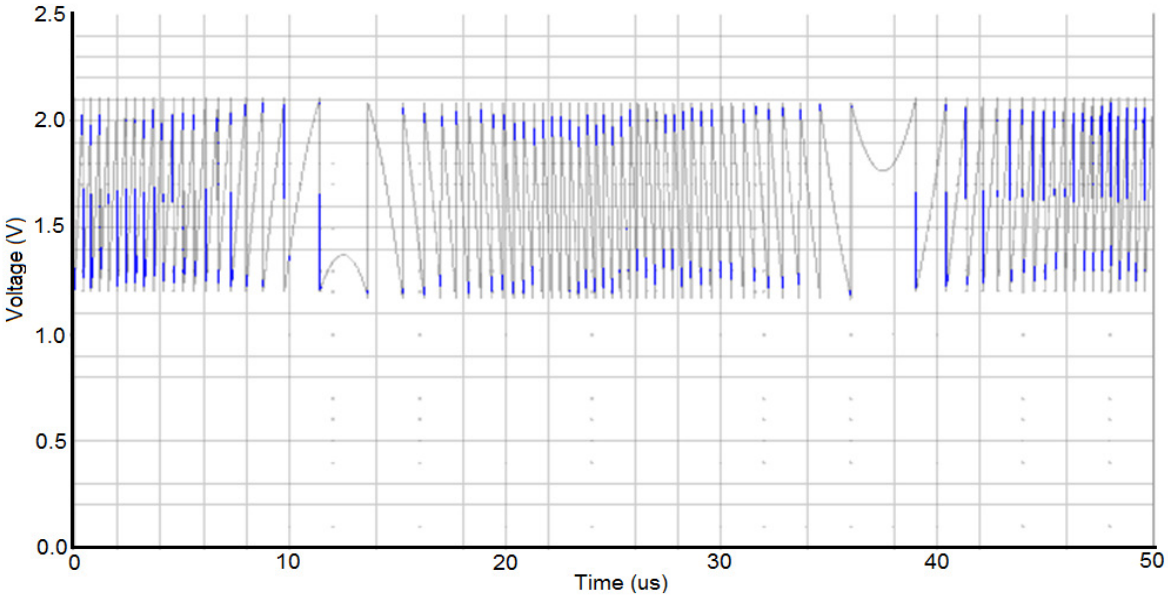

Figure 5.18: Offsetted input signal of the expander

Figure 5.18 depicts the input signal $V_{offsetted,in}$ of the expander coming from the offsetting circuit. The original input signal of the offsetting circuit is a sine wave having a frequency of 20 kHz and an amplitude of 20V. Figure 5.19 depicts the expanded signal coming from the expander. The expanded signal is a sine wave of 20kHz with spikes on top caused by the offsetting. The amplitude of the spikes is the same as the offsetting step. The spikes are very easy to remove by filtering.

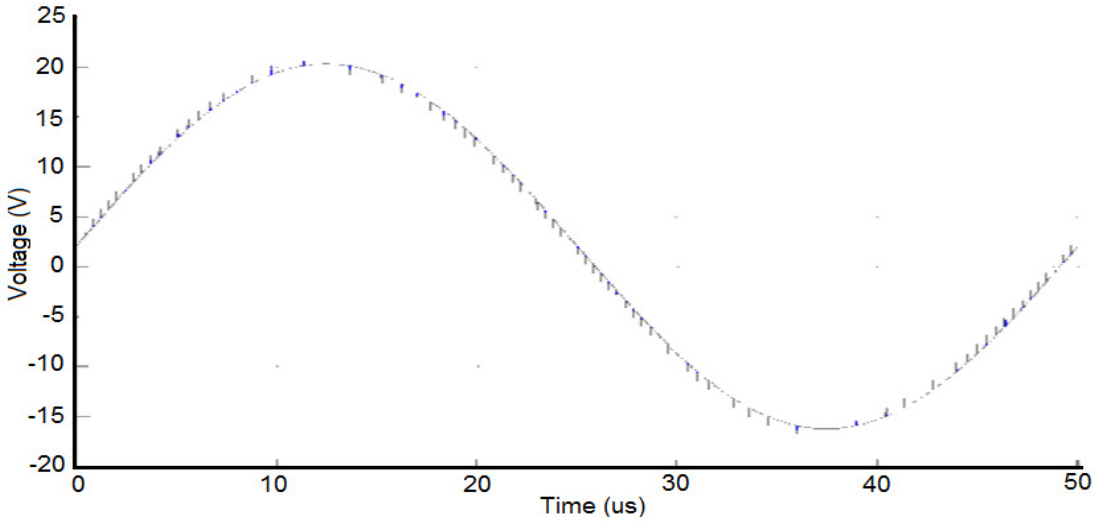

Figure 5.19: Output signal of the expander

5.3.2. Temperature simulation & process corners

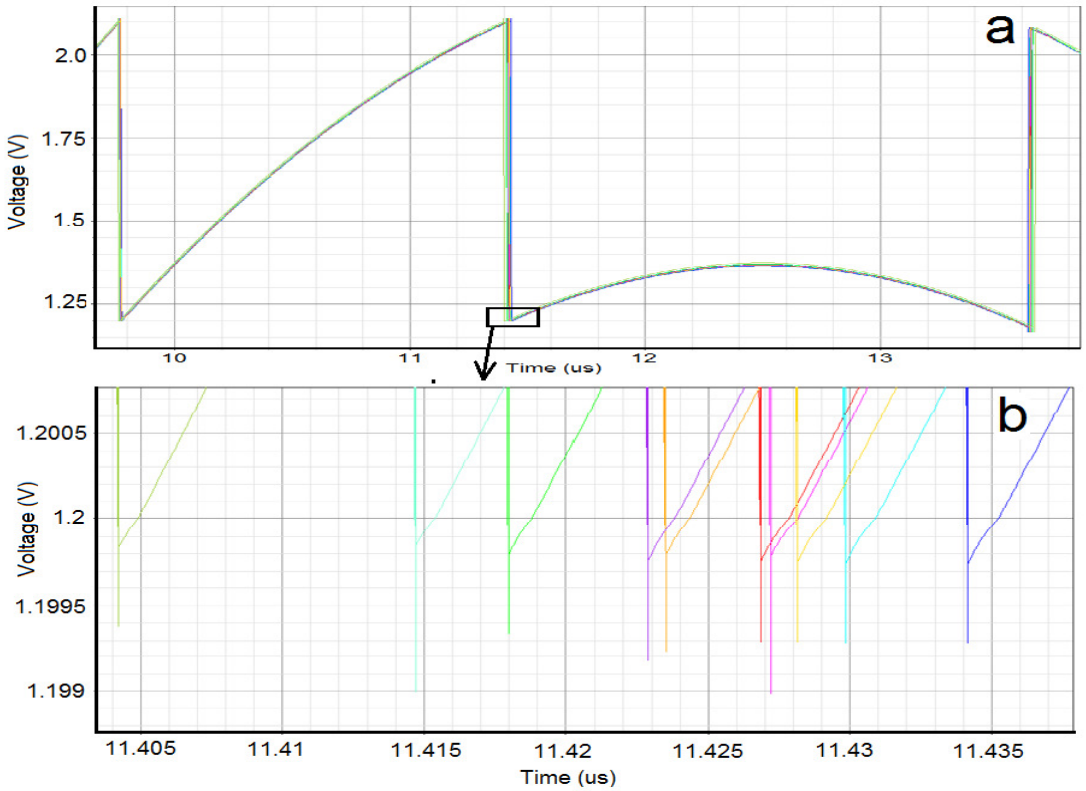

Figure 5.20: Temperature simulation of the offsetting circuit

For investigating the robustness of the circuit, a simple temperature simulation is performed consisting of ten sweeps around 37˚C (body temperature). Figure 5.20.a shows the output signals of the circuit as a result of a temperature sweep. Steps of 1˚C are taken for the different traces.

Figure 5.20.b shows a zoom in on the signal. The traces are shifted in time due to deviation of the gain factor of the attenuator consisting of a low voltage and a high voltage capacitor. The switching points and overshoot are still very accurate and do not deviate significantly, even if zoomed in more. Because the implant is placed in the body, temperature variations will be reduced to a minimum. Ideally, it will be constant. A calibration can be done to determine the gain error if necessary.

During fabrication of the chip, process variations will play a big role in the accuracy of the circuit. Figure 5.21 shows process corner simulation plots in which every trace represents a corner of the process variation. Those are:

- Pmos and nmos at maximum power
- Pmos at maximum power and nmos at minimum power
- Nmos at maximum power and pmos at minimum power
- Pmos and nmos at minimum power
- Capacitance at minimum power
- Capacitance at maximum power

Again, the gain factor varies. However, the switching points and overshoot remain very accurate. A calibration of the circuit can be performed to determine the gain error. Next section will describe more about calibration of the circuit.

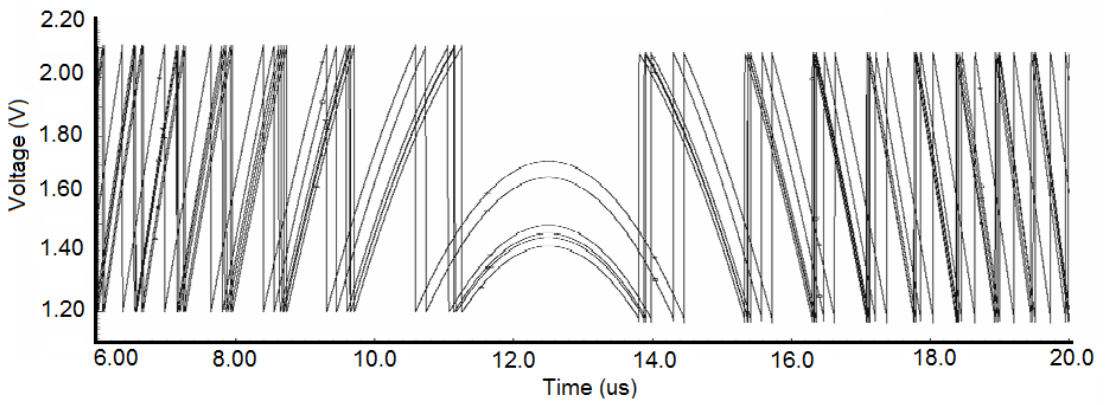

Figure 5.26: Process corner simulation

5.3.3. Calibration

The gain factor is determined by the capacitive divider. This divider consists of a high voltage capacitor and a low voltage capacitor. Because these capacitors have different tolerances, the gain factor of the circuit can vary by 7.2% from the typical value giving accuracy problems. If an input signal of 20 volt is applied at the input, a variation of approximately 1 volt is present at the output of the capacitive divider. By performing a calibration, the deviation from the typical value can be determined and used through the measurement.

Offsetting accuracy deviates as function of the input frequency. To obtain accurate information, a calibration should be performed. To assure no neural responses are present during calibration, it should be performed beneath the nerve threshold. The best way to calibrate is to use a series of triangle shaped stimulus pulses. If these pulses are well defined by the stimulator, the signal readout by the circuit can be compared with the well defined triangle pulse. Switching peaks can be filtered out digitally. Noise can be shifted out of the information band by the use of an oversampling ADC.

Ideal voltage sources should be able to deliver a constant and robust voltage level, even during offsetting. In order to do so, the source should be able to deliver sufficient current and have a low impedance.

Implementing the ideal control loop into CMOS, switching speeds are not reached. This causes errors which cannot be fixed by calibration. It is therefore necessary to design the circuit in a different way. Next chapter will handle a circuit using parallel capacitors to solve the switching speed problem.

5.4. Control loop issues

To have a properly working control loop, all components will have to be very fast and give constant output values. The ideal control loop is composed of the following components:

- Switches
- Flipflops
- Inverters
- Single shot generator
- Comparators

Accuracy of the control loop is crucial for the correct operation of the circuit. Offset voltages generated by the actual offsetting should not exceed 10µV. This implies that at the threshold

voltage the switch has to be closed immediately to prevent overshoot. In addition, the switch has to be opened fast enough in order to prevent loss of the signal as, during offsetting, the voltage across C_2 cannot follow the input signal. The control action will always undergo a certain delay and have a certain spread in exact switching time. In Equation 5.2, the inaccuracy can be found by giving a small deviation to V_{TH1} and V_{TH2}. Moreover, the accuracy depends on the input signal frequency. The higher the input signal frequency, the bigger the inaccuracy will be.

To determine the minimum control loop speed, an estimation can be made. First, the most steepest slope of a sine wave having a frequency of 25kHz and an amplitude of 20V is determined by differentiating the sine wave at the point it crosses 0. This is represented by Equation 5.11:

$$\sin(180°)\frac{d}{dt} = \cos\ 180° = -1 \tag{5.11}$$

The speed of the signal is represented by Equation 5.12:

$$\frac{\text{Amplitude}}{\text{Period time}} \cdot \cos 180° = \frac{20\text{V}}{40 \cdot 10^{-6}} \cdot -1 = -500 \cdot 10^{3}\text{V/s} \tag{5.12}$$

The maximum switching time for achieving an accuracy of 10µV is represented by Equation 5.13:

$$\frac{\text{Maximum inaccuracy}}{\text{Signal speed}} = \frac{10 \cdot 10^{-6}\text{V}}{|-500 \cdot 10^{3}\text{V/s}|} = 20 \cdot 10^{-12}\text{s} \tag{5.13}$$

In order to have sufficient accuracy, the switching time should not exceed 20ps. In most technologies, this will not be possible in a low power fashion. Next section will handle simulation results.

Chapter 6: Implementation parallel capacitor offsetting in voltage domain

As concluded in Section 5.4, the designed circuit with switches cannot be fully implemented in CMOS. The capacitive divider stays very attractive to use because of the low amount of high voltage devices. In this chapter, offsetting by parallel capacitances is investigated and a circuit implementation will be discussed.

6.1. Charge injection by parallel capacitors

To solve the control loop speed problem, a charge domain solution can be used. The concept is based on a capacitive divider and will be discussed in next subsection. Then, an ideal circuit concept will be proposed.

6.1.1. Concept

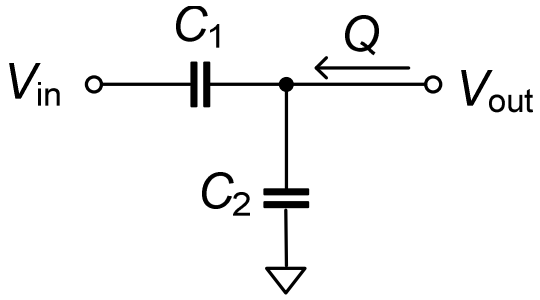

Figure 6.1: Charge blanking

For offsetting in the charge domain, no accurate defined threshold voltages and switching speeds will be needed. If a threshold is reached, a predefined amount of charge is subtracted. If the amount of charge is not subtracted at the exact time, it does not matter because the offset step always remains the same.

Figure 6.1. shows the circuit input with a capacitive divider consisting of a high voltage capacitance C_1 and low voltage capacitance C_2. The gain factor is determined by Equation 5.1. By injecting a well known amount of charge Q in the low voltage capacitance C_2, the output voltage V_{out} can be calculated back to the input voltage V_{in}. The charge injection can be achieved by adding a parallel capacitance having a well defined amount of charge stored. As explained in Section 5.1, charge injection into the tissue will be very small.

6.1.2. Ideal circuit design

Charge can be defined by storing it in a capacitor. After storage, the charge can be applied to the capacitive divider. Polarity of the charge should be taken into account before applying it to the resistive divider. Figure 6.2 shows an implementation of the parallel capacitor offsetting circuit.

Input voltage V_{in} is applied to capacitor C_1. Capacitances C_1 and C_3 together represent the gain block g of Figure 4.9. Capacitor C_2 represents the parallel capacitor for injecting a negative charge into C_2. Negative voltage source $V_{ref,n}$ charges capacitor C_2 to the proper charge. Capacitor C_2 is charged by closing switches S_1 and S_5. The charge in capacitor C_3 is offsetted by closing switches S_2 and S_6. The charge stored in C_2 can now be divided over C_2 and C_3. The output of the circuit is located in between C_1 and C_3. For injecting a positive charge, the same holds. Capacitor C_4 is charged by closing switches S_4 and S_8.

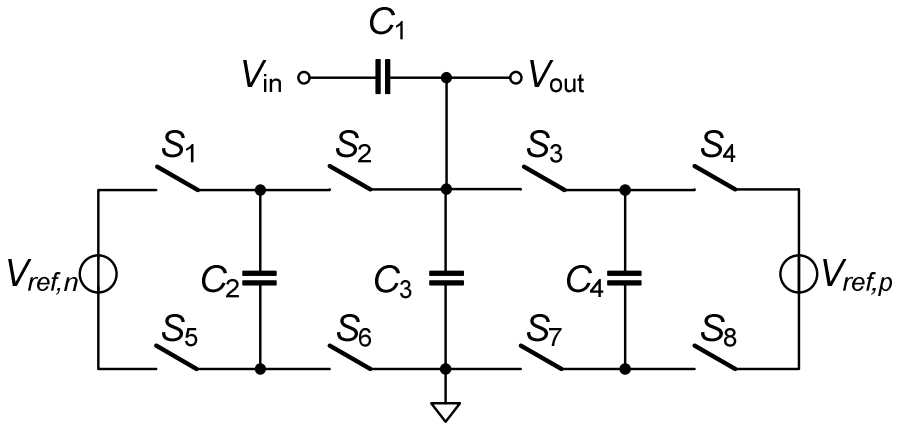

Figure 6.2: Ideal circuit for charge subtraction

The charge stored in capacitor C_3 is offsetted by closing switches S_3 and S_7. The charge stored in C_4 can now flow into C_3. Because the input signal V_{in} is not known, it is not possible to use only one capacitor for applying a positive and negative charge. Both capacitors should be charged and ready to apply their charge to C_3. The circuit can be represented by Equation 6.1 in which *floor* again stands for rounding down to integers.

$$Q_{out} = V_{in} \cdot \mathrm{g} \cdot C_3 \cdot \left[floor\left(\frac{V_{in} \cdot \mathrm{g} - \mathrm{floor}\left(\frac{V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,h}}}\right)}{V_{in} \cdot \mathrm{g}} \right) + floor\left(\frac{V_{in} \cdot \mathrm{g} - \mathrm{floor}\left(\frac{\mathrm{V_{ref,l}} - V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,l}}}\right)}{V_{in} \cdot \mathrm{g}} \right) - 1 \right] + \left(V_{in} \cdot \mathrm{g} \cdot C_3 + \mathrm{V_{ref,n}} \cdot C_2\right) \cdot floor\left(\frac{V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,h}}}\right) + \left(V_{in} \cdot \mathrm{g} \cdot C_3 + \mathrm{V_{ref,p}} \cdot C_4\right) \cdot floor\left(\frac{\mathrm{V_{ref,l}} - V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,l}}}\right) \quad (6.1)$$

This Equation can be simplified to Equation 6.2:

$$Q_{out} = V_{in} \cdot \mathrm{g} \cdot C_3 + \mathrm{V_{ref,n}} \cdot C_2 \cdot floor\left(\frac{V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,h}}}\right) + \mathrm{V_{ref,p}} \cdot C_4 \cdot floor\left(\frac{\mathrm{V_{ref,l}} - V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,l}}}\right) \quad (6.2)$$

The switches are controlled by a control loop. It actually consists of two almost identical parts, one part having a high reference $V_{ref,h}$ for controlling switches S_1, S_2, S_5 and S_6 and one part having a low reference $V_{ref,l}$ for controlling S_3, S_4, S_7 and S_8. The control loop will be discussed in Section 6.4.

6.2. Practical circuit design

This section handles the implementation and verification of the ideal circuit into CMOS. A topology for the switches will be chosen and implemented. Several simulations are performed.

6.2.1. Switch topology

As discussed at Section 5.2, implementing the ideal capacitive divider by non-ideal capacitors will not cause problems. The same capacitors and capacitor values will be used as in 5.2. Capacitors C_2 and C_4 from Figure 6.2 will have the same value as C_3 from Figure 6.2. The ideal switches can be implemented in two ways:

- Single transistor
- Transmission gate

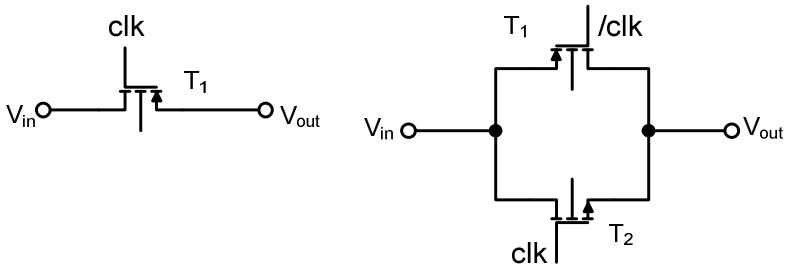

Figure 6.3: a: single transistor *b: Transmission gate*

Single transistor

Figure 6.3.a shows a single transistor used as switch. A single switch will introduce charge injection. In order to cancel this, dummy transistors can be used. One dummy is needed for every side causing the chip area consumption to rise. The single transistor is limited by its threshold voltage V_{th}. The gate-source voltage V_{gs} should be higher than the threshold voltage V_{th}. Below this threshold voltage, the transistor will not conduct. In the circuit design, this can be taken into account by obtaining an input voltage V_{in} varying between 1 and 2 volt, which is above V_{th} or by using bootstrapped switches.

The noise generated by the transistor consists of a relative small 1/f noise part and a relatively high thermal noise part. The frequency region of interest is in the area where 1/f noise is dominant.

Transmission gate

Figure 6.3.b shows a transmission gate. It consists of two complementary transistors which will be matched. Because they are complementary, it will not be possible to cancel charge injection as well as in the case of the single transistor with dummy transistors. To obtain a good cancellation for the complementary switches, the ratio for the width of the NMOS and PMOS transistors should be 3 to 1 respectively. This ratio is related to the ratio of the mobilities in NMOS, μ_n, and PMOS, μ_p.

Chip area consumption of the transmission gate will be less compared to a single transistor with dummy transistors. Transmission gates in contrary to a single transistor are able to switch over the full supply voltage range because they do not suffer from threshold voltages. When the NMOS is under threshold, the PMOS is above threshold and vice versa. The transmission gate enables rail to rail signal swing.

The 1/f noise of a transmission gate is higher than that of a single transistor. For obtaining the same conduction, transmission gates can have smaller transistor lengths and widths in comparison with the single transistor. The 1/f noise of the transmission gate will decrease. Still, the 1/f noise behavior of a single transistor is better than the 1/f noise behavior of a transmission gate. The thermal noise of the transmission gate is better than the single transistor. In the frequency region of interest, 1/f noise is dominant.

Taking all these things in account, in this case the single transistor as component for the switch is favored. It has better noise behavior and has a better charge injection cancellation.

6.3.2. Replacing ideal switches by transistors

Two types of transistors are available; an NMOS and a PMOS transistor. The circuit with transistors is depicted in Figure 6.4. Switches S_1 to S_8 are replaced by transistors T_1 to T_8, respectively.

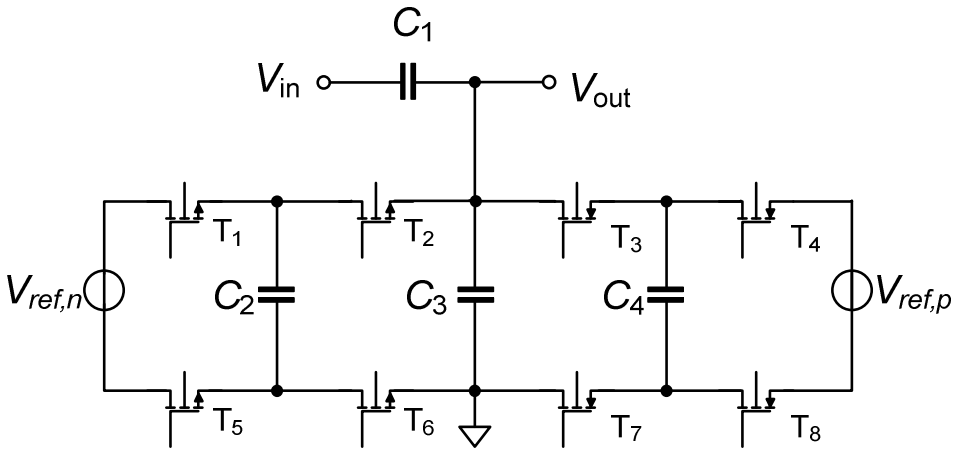

Figure 6.4: Practical circuit for charge offsetting

For offsetting to low voltages, NMOS transistors are used having a length of 0.35µm and a width of 10µm. For offsetting to high voltages, PMOS transistors are used having a length of 0.35µm and a width of 10µm. Reference source $V_{ref,n}$ is chosen to be 0V, or ground.

Reference source $V_{ref,p}$ is chosen to be 3.3V, or supply. Figure 6.5 shows the modified practical implementation of charge offsetting. Because $V_{ref,n}$ will be ground, the source can be replaced by a direct connection to ground. Switches T_5, T_6, T_7 and T_8 can also be connected to ground and thus can be omitted.

To reduce charge injection, dummy transistors T_{d1}, T_{d2}, T_{d3} and T_{d4} will be added. Transistor T_{d1} takes care of charge injected by T_1 and T_2. Transistor T_{d2} takes care of charge injected by T_2. Transistor T_{d3} takes care of charge injected by T_3. Transistor T_{d4} takes care for the charge injected by T_3 and T_4. At the source of T_4, no dummy transistor is needed because this terminal is connected to supply. At the drain of T_1, no dummy transistor is needed because this terminal is connected to ground.

NMOS and PMOS transistors can both be used in the circuit. The difference between them is the conduction. If the conduction is higher, the noise becomes lower. This makes the NMOS more suitable for offsetting to the low reference voltage and the PMOS to the high reference voltage. Next section handles a transient simulation of the circuit.

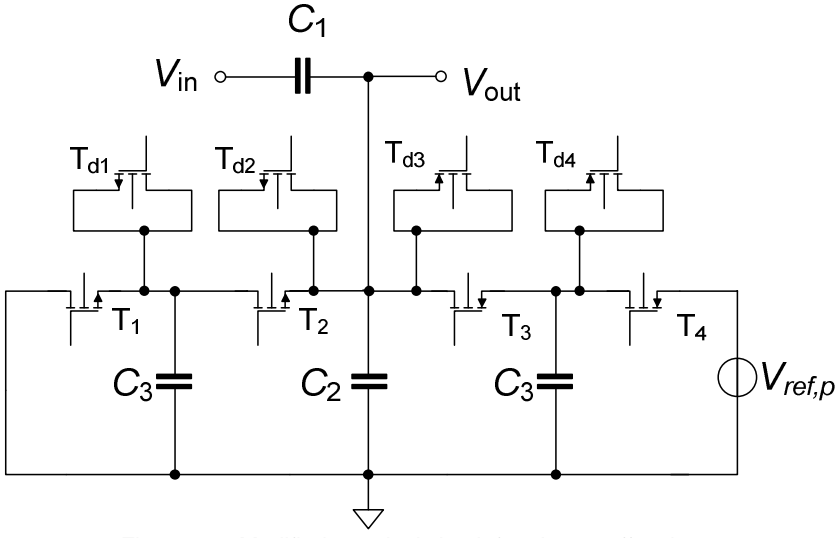

Figure 6.5: Modified practical circuit for charge offsetting

6.3.3. Transient simulation

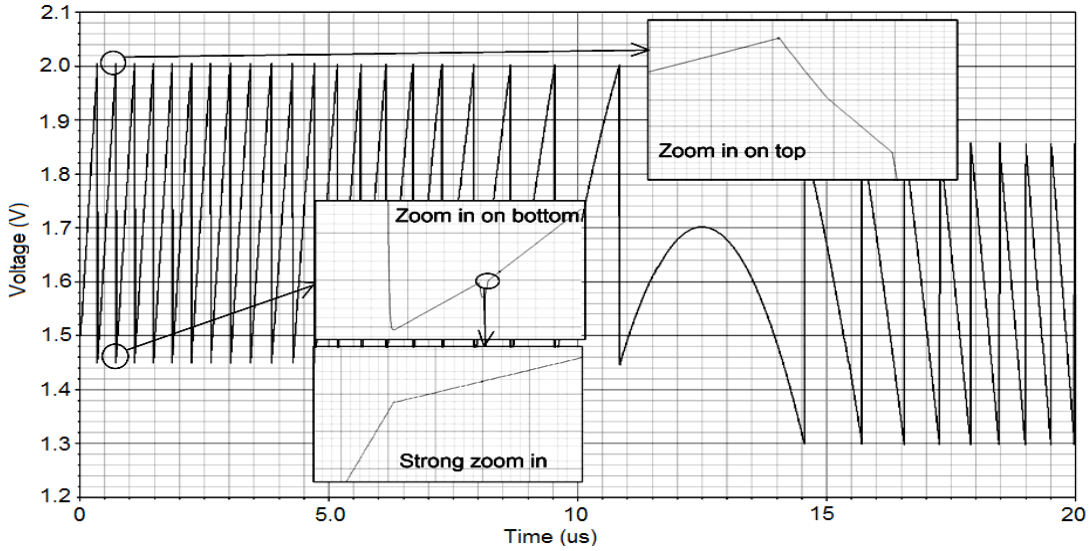

Figure 6.6: Plot of a transient analysis

To check if the charge offsetting circuit works properly, a transient simulation of the circuit having an ideal control loop is performed. This control loop is discussed in more detail in Section 6.4. A sine wave having a frequency of 25kHz and an amplitude of 20V is used as input voltage V_{in}. The offsetted output signal V_{out} is shown in figure 6.6.

Zooming in on the top of the signal, it can be seen that some charge injection occurs. Zooming in on the bottom, this also happens. The peak which can be distinguished is charge injected by the switch, followed by the opposite charge injected by the dummy switch. Zooming in more, the point can be distinguished where the circuit returns to its initial state. The voltage drop due to blanking is 0,541931 V. Comparing multiple offsets with each other, the voltage drops have a deviation in the order of several 100nVs.

6.3.4. Noise

To investigate the noise behavior, a noise simulation can be performed. Noise is determined in 3 different states showed in Table 6.1.

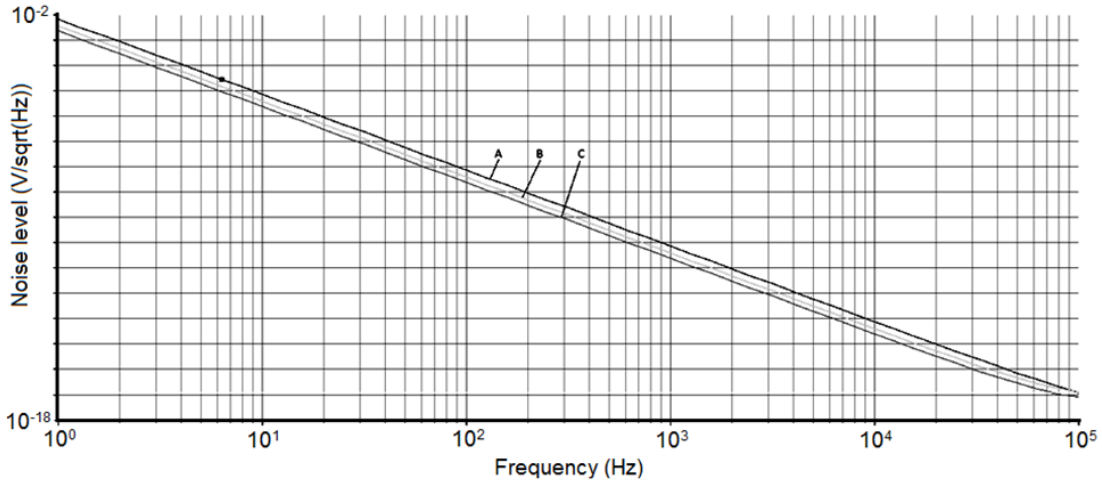

Figure 6.7: Noise behavior in three different states

State	C_2	C_4
A	Offsetting	Charging
B	Charging	Charging
C	Charging	Offsetting

Table 6.1: Capacitor states

The noise behavior is optimized by adjusting the length and width of the transistors. A trade off is made between the size of the transistor and the noise contribution. Final results are depicted in Figure 6.7.

The highest noise level occurs in state A. The noise depicted can be characterized as 1/f noise. The bandwidth of interest for neural responses is from 100Hz to 10kHz. Integrating the noise over the bandwidth gives a noise signal level of 600µV which is not within the specifications. The noise level is 60 times too high.

6.3.5. Temperature simulation

To determine the temperature dependency of the circuit, a temperature simulation is performed. For now, a simple and quick simulation consisting of only a few runs is performed. Extensive testing will be performed if the complete circuit including control loop is designed and works properly.

Results of the temperature simulation are depicted in Figure 6.8. One offsetting step is depicted. At the top of the signal, which is just before offsetting, a zoom in is made. At the zoom in, it can be seen that the signals do not reach the threshold of the comparator at the same time. This is due to deviation of the gain factor. If the time difference of the signals just before the top voltage is measured, it can be compared to the end of the offsetting later. At the end of the offsetting, a zoom in is performed in two steps. In the first step, a bump can be seen in the signal. This is due to charge injection and the cancellation which are not timed exactly at the same time. A stronger zoom in is performed, the signals are visible separately again.

Taking the time difference caused by the gain error measured at the top and measuring the voltages using this time difference at the end of the offsetting, the voltage deviation of the signals is below 1µV. The offsetting can be defined very accurately. The gain error can be corrected by calibration. Giving the ideal comparators of the control loop a delay, thereby making them more realistic, also gives accurate results.

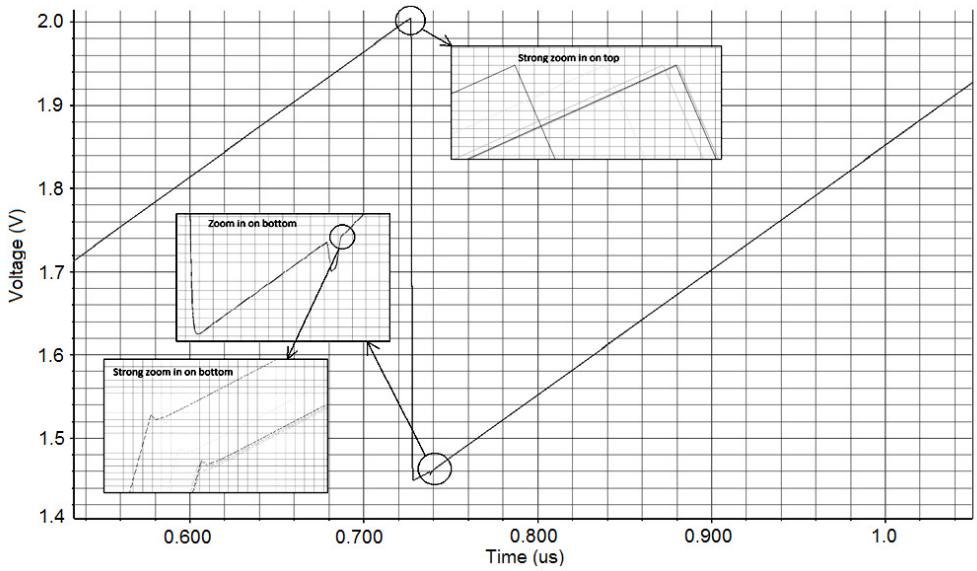

Figure 6.8: Temperature simulation plot of the offsetted signal

6.4. Control loop design

This paragraph handles the control loop design. The design of the control loop can be subdivided into two parts: the ideal control loop design and the implementation of this ideal control loop to a non-ideal control loop. First, the design of the ideal control loop will be discussed.

6.4.1. Design of the ideal control loop

The ideal control loop can be subdivided into two almost identical parts. The difference is in the controlling of NMOS or PMOS transistors and in the reference voltage for the comparator.

The control loop for generating negative offsets by closing the NMOS transistor is depicted in Figure 6.9. This loop is able to control 2 switching transistors and 2 dummy transistors, resulting in 4 outputs. The output voltage V_{out} coming from the circuit (Fig 6.5) is applied to the control loop as V_{in} of the comparator in order to compare it with a reference voltage of 2 volt. If the input signal V_{in} becomes higher than the reference, the output of the comparator becomes high.

Two single shots are activated. *Single shot 1* has a pulse width of 10ns and a delay of 2ns. Single shot 2 has a pulse width of 14ns and a delay of 0ns. Two non-overlapping clocks are created preventing short circuit during switching of transistors T_1 and T_2 (Fig. 6.5). The output of *single shot 1* is directly applied to transistor T_2 by terminal V_{T2}. This output is also inverted by *inverter 2* for application to dummy transistor T_{d2} by terminal V_{Td2}. *Inverter 1* inverts the output of *single shot 2* and is applied to transistor T_1 by terminal V_{T1}. The outputs of *single shot 1* and *inverter 1* are applied to an *OR*-port. After the *OR*-port, the signal needs to be inverted to control transistor T_{d1} properly. Transistor T_{d2} is controlled by terminal V_{Td1}. Figure 6.10 depicts the signals generated by the control loop.

The control loop for generating positive offsets by closing the PMOS transistors is very similar to the control loop for controlling NMOS transistors. All outputs have to be inverted. The inverted output V_{T2} will control transistor T_3, inverted output V_{Td2} will control dummy transistor T_{d3}, inverted output V_{T1} will control transistor T_4, and inverted output V_{Td1} will control transistor T_{d4}. The reference voltage will be at 1.3V.

Figure 6.11 depict the signals coming from the PMOS transistor control loop. Transient simulation results achieved with this control loop are already discussed in paragraph 6.3.3. Noise simulation results are already discussed at paragraph 6.3.4. Results of a temperature simulation is already discussed in Section 6.3.5. The ideal control loop can be implemented into CMOS.

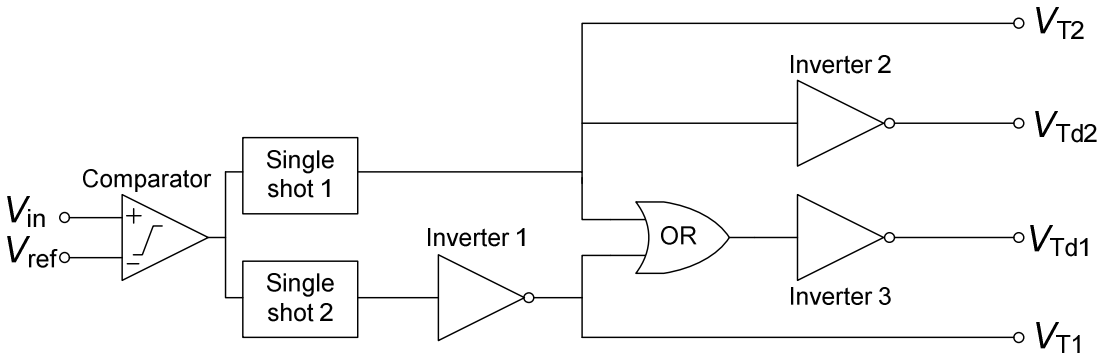

Figure 6.9: Control loop for subtracting charge

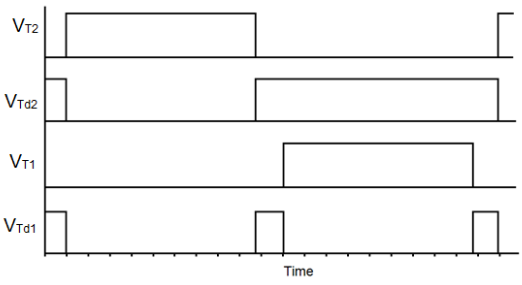

Figure 6.10: Control signals applied to NMOS transistors transistors

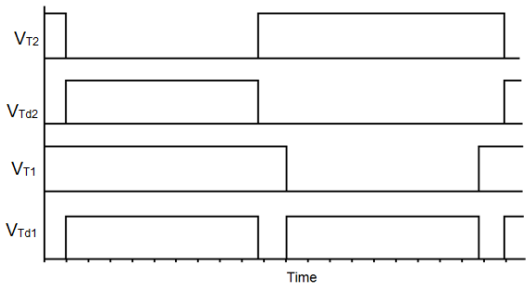

Figure 6.11: Control signals applied to NMOS transistors

6.4.2. Practical control loop

The implemented control loop slightly differs from the ideal one. The NMOS control loop is discussed. The modified charge offsetting control loop is depicted in Figure 6.12. The output coming from the circuit is applied to the control loop as V_{in} of the comparator in order to compare it with a reference voltage of 2 volt. If the signal becomes higher, the output of the comparator becomes high. This output is applied to a clocked *D-flipflop*. The flipflop switches at the rising edge of the signal and is used to create a single shot function. For creating the second single shot function, a second *D-flipflop* is put into cascade with the first *D-flipflop*. The outputs of the flipflops are shifted in time. To create a non-overlapping functionality, some additional components are needed. The outputs of both *D-flipflops* are connected to an *AND*-port and a *NOR*-port. The *AND*-port creates the *single shot 1* of Figure 6.9, the *NOR*-port the *single shot 2* of Figure 6.9. The *AND*-port is directly coupled to transistor T_2 by V_{T2}. The inverted output is connected to dummy transistor T_{d2} by V_{Td2}. The *NOR*-port is directly connected to transistor T_1 by V_{T1}. The *NOR*-port and *AND*-port are both connected to an *OR*-port and, subsequently, to *inverter 2* to create the switching signal V_{Td1} for dummy transistor T_{d1}.

The control loop for controlling PMOS transistors is very similar to the loop that has just been discussed. However, some small adjustments have to be made. All outputs have to be inverted. The inverted output V_{T2} will control transistor T_3, inverted output V_{Td2} will control dummy transistor T_{d3}, inverted output V_{T1} will control transistor T_4, and inverted output V_{Td1} will control transistor T_4. The reference voltage will now be at 1.3V. The practical logic blocks are already present in the library of the AMIS I3T25 technology. An investigation has to be performed to check if it is possible to implement the control loop and whether it will be functional.

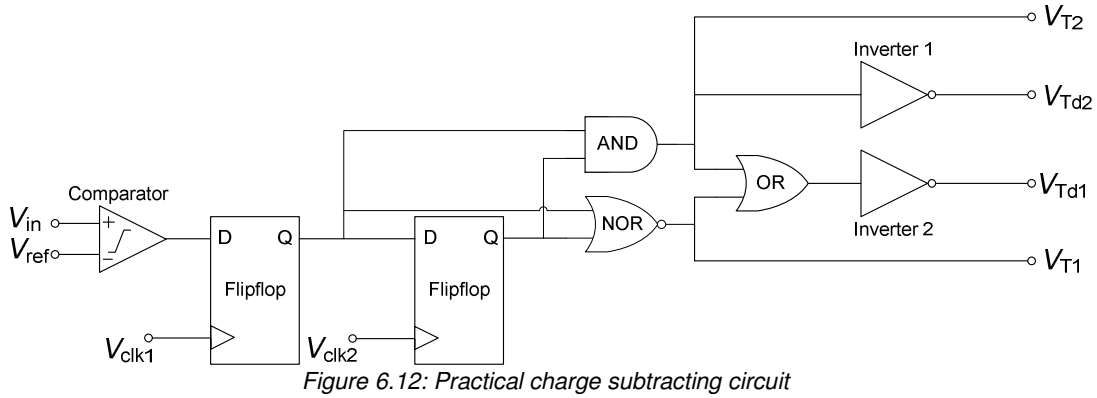

Figure 6.12: Practical charge subtracting circuit

6.4.3 Transient simulation

A transient simulation is performed in order to check the correct operation of the circuit with control loop. A saw tooth wave having an amplitude of 20 volt and a frequency of 25kHz is used as offsetting circuit input signal. Figure 6.13 shows the output signal of the offsetting circuit having a non-ideal control loop, which can be described as an offsetted saw tooth wave.

Zooming in on the top of the signal, only charge injection generated by the transistor switch can be seen. Charge injection caused by the dummy transistor cannot be seen because it happens during offsetting.

Zooming in at the bottom, a bump can be distinguished. This bump is caused by charge injected by the transistor switch followed by the injection of a charge having opposite polarity in order to cancel the charge injected by the switch.

Zooming in more, the part of the signal can be seen where the dummy transistor finishes charge injection. Comparing multiple offsetting steps with each other, only a small voltage variation can be distinguished. This variation is under 1µV, which is within the specifications.

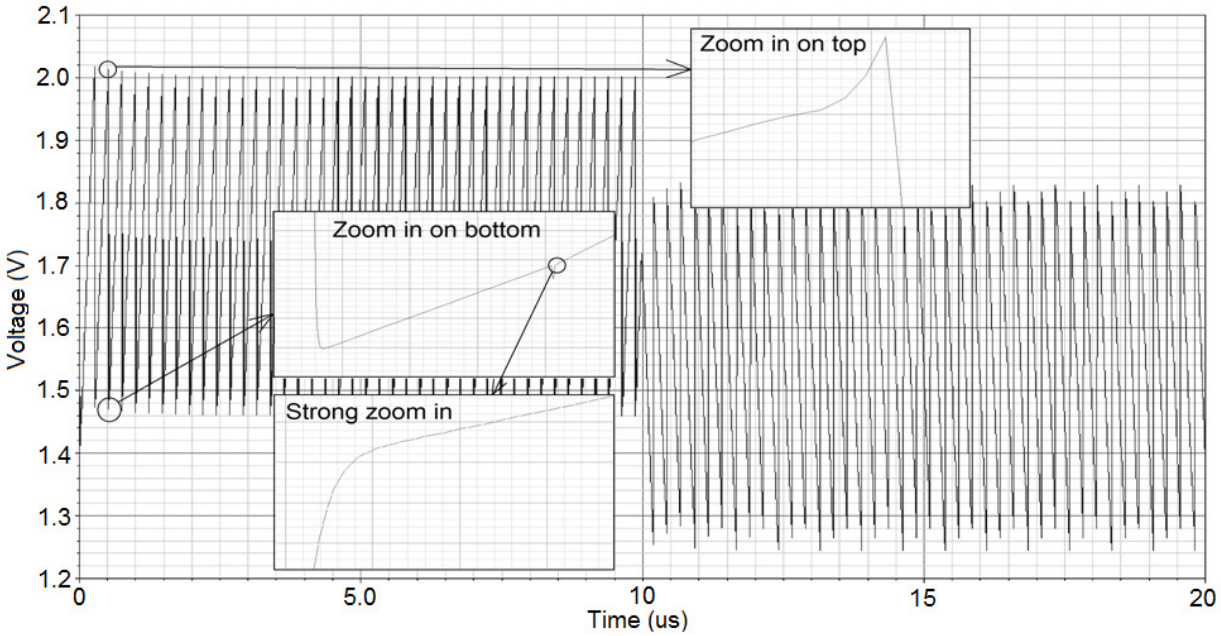

Figure 6.13: Results of a transient simulation of the practical circuit

6.4.4. Noise

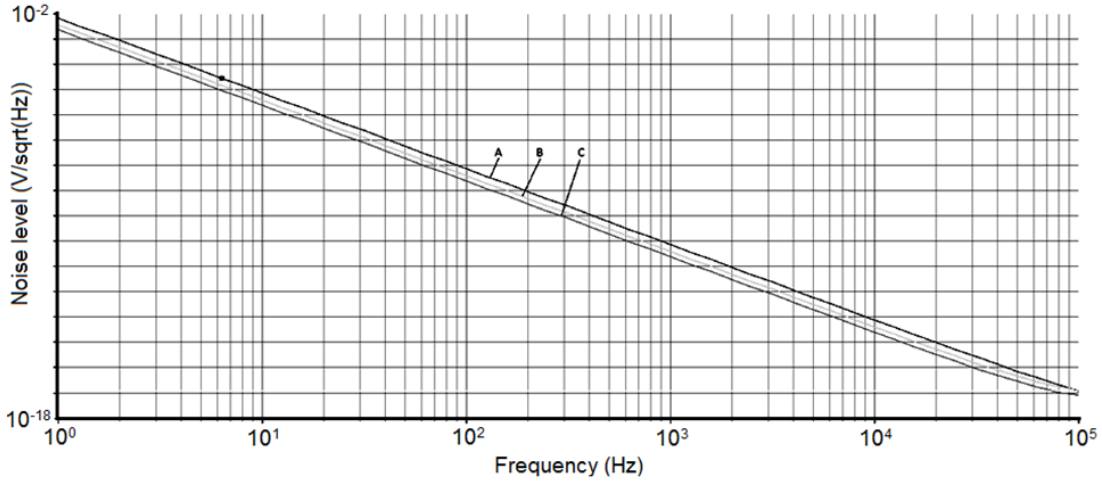

Figure 6.14: Noise analysis of the implemented circuit with implemented control loop

To investigate the noise behavior of the circuit, a noise simulation can be performed. Noise is determined in 3 different states as explained in section 6.3.4. Results are depicted in figure 6.14. The highest noise level occurs in state A. The generated noise can be characterized as 1/f noise. The bandwidth of interest for neural responses is from 100Hz to 10kHz. The noise is integrated over the bandwidth resulting in a noise level of 600µV which is not within specifications. Comparing the noise behavior of the circuit with ideal control loop with the noise behavior of the circuit with the non-ideal control loop, no difference can be distinguished. This is because only two comparator inputs are present having a high input impedance and thus almost adding no noise to the signal path.

6.4.5. Temperature simulation

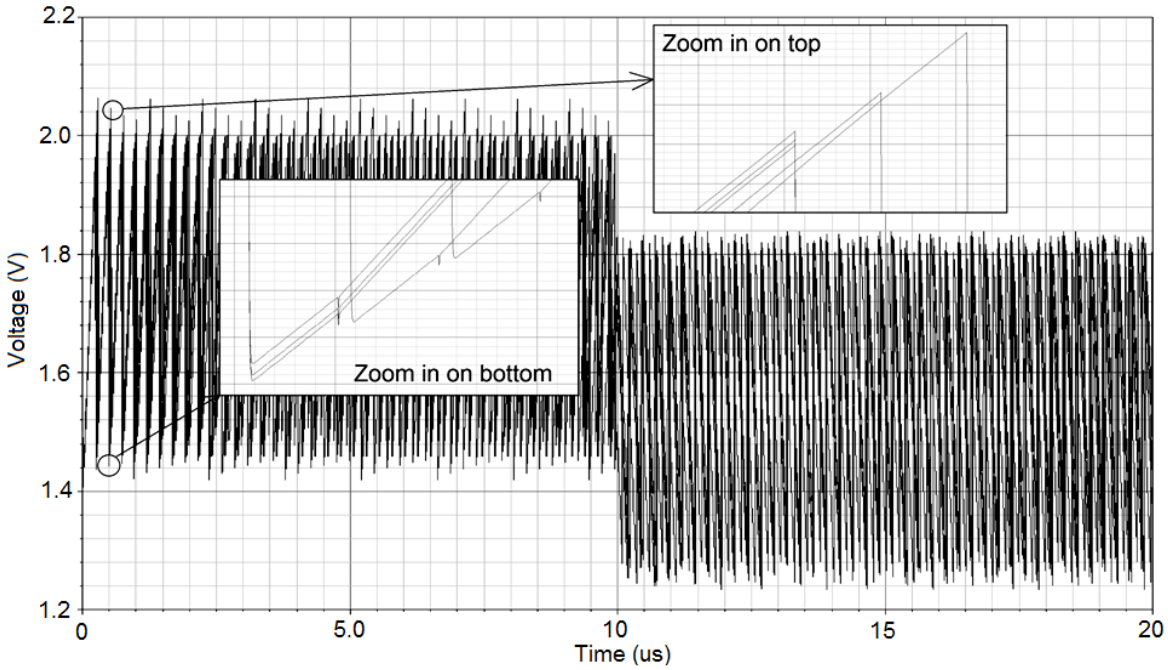

Figure 6.15: Temperature simulation results

To determine the circuit behavior due to temperature variations, a parametric temperature simulation at 37ºC is performed. To obtain a simple estimation, only 5 runs are performed. The same input signal is used as in Section 6.5.4. Figure 6.15. shows the simulation results. Every wave represents the output of the circuit at a different temperature.

A zoom in on the top of the signal shows a gain error. Besides that, the signal level at the point the transistors start switching varies. This is caused by variations in speed of the comparator and by control loop delays due to the clock signal.

A zoom in on the bottom of the signal shows again a gain error. The end of the offsetting is shifted in time by the variation of the speed of the comparator and by delays due to the clock signal. The bump which can be seen is caused by charge injection of the switching transistor and its dummy transistor.

If a comparison of the offset voltages of the different signals is performed, a big variation of ±150µV between the offset voltage of the different signals is present. The maximum variation allowed is 10µV. These variations will not only occur due to temperature, but also due to the switching speed of the control loop which varies and has a limited switching speed. In order to have sufficient accuracy, the switching time of the control loop should not exceed 20ps. In most technologies, this will not be possible in a low power fashion. Next section will handle this problem and a solution will be suggested.

6.5. Results

In this chapter, a parallel capacitor offsetting method is proposed. A system design is made, followed by the implementation as an ideal circuit. The ideal circuit is finally converted to an implementation in the AMIS I3T25 CMOS technology. Some simulations are performed on the implemented circuit and control loop.

Firstly, a transient analysis is performed, The offsetted output is plotted and analyzed. Results did not show any problems. All specifications are met.

Secondly, a noise analysis, is performed giving three states. In all states the noise exceeds the noise specification by a factor 60(!).

Thirdly, during offsetting the capacitance of the capacitive divider changes due to a parallel capacitor placed at the low voltage transistor for offsetting. If the control loop is fast enough, this is not a problem. The charge injected in the capacitive divider will always be the same and the division of charge between the capacitances will always be the same. Unfortunately, the comparator and the rest of the control loop do not switch at exactly the same voltage value. Moreover, it is not fast enough for obtaining sufficient accuracy.

Every time the transistor switches at a different voltage, the charge stored in the low voltage capacitor of the capacitive divider will deviate. By putting a capacitor with a fixed charge in parallel with the low voltage capacitor of the capacitive divider, both charges will divide over the two capacitors introducing the deviation in the offset. Formula 6.1 handles the output charge. Because of the parallel capacitors, the output voltage should be considered instead of output charge resulting in Equation 6.3.

$$V_{out} = V_{in} \cdot \mathrm{g} \cdot \left[floor\left(\frac{V_{in} \cdot \mathrm{g} - \mathrm{floor}\left(\frac{V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,h}}}\right)}{V_{in} \cdot \mathrm{g}} \right) + floor\left(\frac{V_{in} \cdot \mathrm{g} - \mathrm{floor}\left(\frac{\mathrm{V_{ref,l}} - V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,l}}}\right)}{V_{in} \cdot \mathrm{g}} \right) - 1 \right] + \frac{(V_{in} \cdot \mathrm{g} \cdot C_3 + \mathrm{V_{ref,n}} \cdot C_2) \cdot floor\left(\frac{V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,h}}}\right)}{\mathrm{C_2 + C_3}} + \frac{(V_{in} \cdot \mathrm{g} \cdot C_3 + \mathrm{V_{ref,p}} \cdot C_4) \cdot floor\left(\frac{\mathrm{V_{ref,l}} - V_{in} \cdot \mathrm{g}}{\mathrm{V_{ref,l}}}\right)}{\mathrm{C_3 + C_4}} \quad (6.3)$$

The ADC used has a low sampling rate, so the voltage where the switching transistor starts offsetting cannot be determined exactly. The error of ±150µV cannot be repaired making this circuit not suitable for use in the readout.

This circuit is dependent on the accuracy of the comparator and the speed of the control loop. Actually, this is the same problem as the voltage switching circuit discussed in chapter 5. Moreover, noise levels are too big. Another solution should be found. The circuit should deal with charge only. A solution for this problem is proposed in the next chapter.

Chapter 7: Charge offsetting circuit design

In this chapter, a new concept is proposed based on offsetting in the charge domain. This concept can be realized by injecting charge through a capacitor while the injecting capacitance is not seen by the capacitive divider.

7.1. Ideal circuit design

In this section, first a charge injection concept using a capacitor without adding its capacitance is discussed. Then, an ideal circuit design for offsetting in the charge domain is found and improved. Finally, a transient simulation will be performed on a realistic circuit.

7.1.1. Injecting charge without adding a capacitance to the capacitive divider

The concept of injecting charge without adding a capacitance to the capacitive divider is based on the idea that the capacitance, in which the charge is stored, will not be seen by the capacitive divider. Figure 7.1 shows the concept circuit. The charge stored in capacitance C_2 will be transferred to the capacitive divider consisting of C_1 and C_3. The capacitive divider will be completely free to follow the input signal. When the input signal becomes too high, an accurately defined charge is injected in the capacitive divider by applying a voltage step at the input of capacitance C_2. A part of the charge will be injected into the tissue via C_1. Because the tissue-electrode interface consists of a capacitance which is much bigger than that of the capacitive divider, this will not give problems. The charge reaching the tissue will be very small. Next section proposes the principle of a floating charge amplifier.

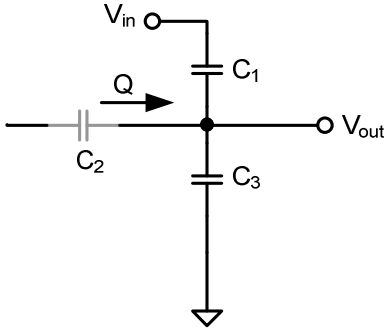

Figure 7.1: concept of charge injection in the capacitive divider

7.1.2. Floating charge amplifier

Capacitance C_2 will not influence the capacitances of resistive divider C_1 and C_3 when the potential at both sides of capacitor C_2 is equal. Since one terminal is connected to the capacitive divider, the other terminal should have the same potential. This terminal should also be able to receive a voltage step for injecting charge into the capacitive divider.

An amplifier *Amp* which floats on the output voltage and thereby keeping the terminals of capacitor C_2 at the same potential can give a solution. As soon as amplifier *Amp* creates a voltage step, a voltage drop over capacitor C_2 will be created and charge will be injected into the capacitive divider.

Figure 7.2 depicts the concept of using a floating charge amplifier. Amplifier *Amp* together with C_4 and C_5 represent a charge amplifier. Switches S_4 and S_6 are charging switches for charging C_5 with a charge coming from reference voltage source V_1. Switches S_5 and S_7 represent switches used for coupling C_5 to the charge amplifier. Amplifier *Amp* floats on the output voltage V_{out}, buffered by voltage follower V_{VCVS}. For resetting the amplifier back to its initial state, switch S_1 is used generating an inverted voltage step.

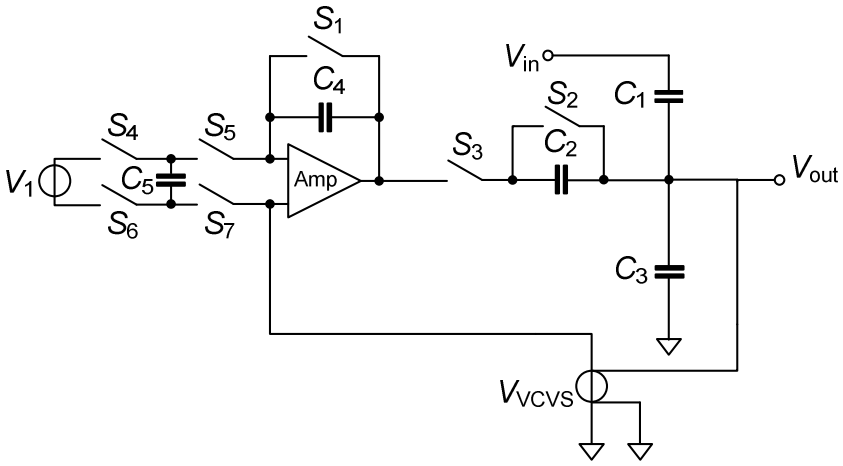

Figure 7.2: Concept of a floating charge amplifier

To prevent this voltage step to reach capacitor C_2, the charge amplifier is decoupled from capacitor C_2 by switch S_3. During resetting amplifier *Amp*, also the charge present in capacitor C_2 is blanked by switch S_2.

When simulating this circuit, no charge injection by amplifier *Amp* occurs. This is due to voltage follower V_{VCVS}, which will compensate for the charge injected by charge amplifier *Amp*. To prevent this compensation, another solution should be found.

To prevent voltage follower V_{VCVS} from correcting charge amplifier *Amp*, it can be put on a fixed potential at the moment charge amplifier *Amp* applies its voltage step. Figure 7.3 shows a modified circuit which is able to do so. Capacitor C_6 is added as reference source during the voltage step application of charge amplifier Amp. Switch S_9 will connect to the capacitor changing the input terminal of the voltage follower from the capacitive divider output to reference source C_6. Switch S_8 will open.

During the creation of a voltage step of charge amplifier *Amp*, the output voltage of voltage follower V_{VCVS} is fixed while the voltage at the capacitive divider output still varies due to its input. The time the output voltage of the voltage follower should be fixed should be very short to prevent inaccuracies due to undesired charge injection by capacitor C_2, caused by the output variation of the capacitive divider. To create high accuracy, voltage follower V_{VCVS} cannot hold the reference voltage longer than 20ps. This is not possible in the AMIS I3T25 technology. Next section proposes a circuit with a fixed charge amplifier injecting a charge with help of a capacitor into the capacitive divider.

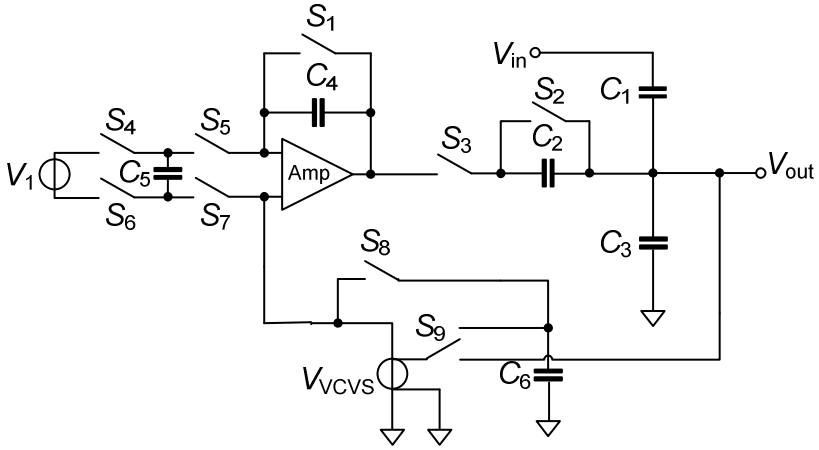

Figure 7.3: Modified floating charge amplifier concept

7.1.3. Charge amplifier with fixed reference, controlled charge injecting capacitor

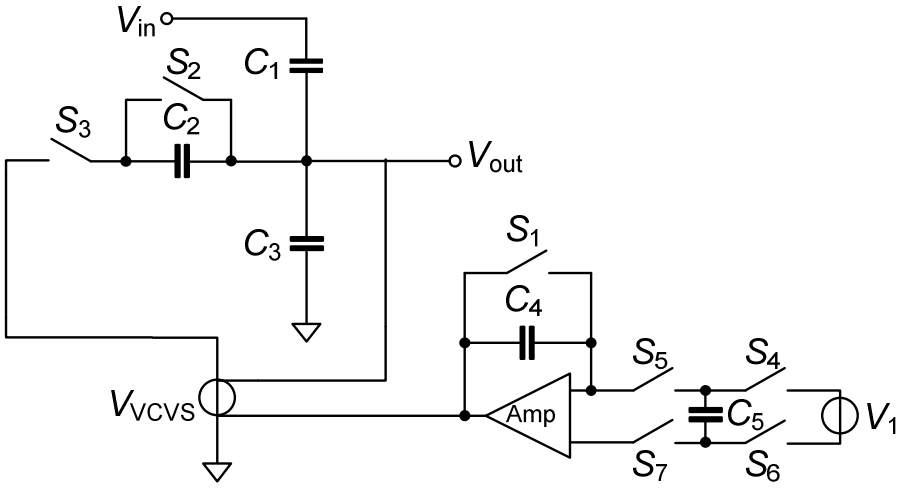

Figure 7.4: Charge injection circuit with a charge amplifier having a fixed reference

The floating charge amplifiers discussed in the previous section are not able to inject charge into a capacitive divider with high accuracy. This section proposes an alternative circuit solving this problem. Figure 7.4 shows a circuit having a differential input voltage follower. One input is connected to the capacitive divider output V_{out} and one input comes from the charge amplifier *Amp*.

The charge amplifier can create a voltage step which will be followed by the voltage follower to capacitor C_2. Capacitor C_2 converts the voltage step into a charge which is injected into the capacitive divider. For returning the charge amplifier back to its initial state, switch S_3 is opened so the inverse voltage step created by resetting the charge amplifier with switch S_1 is not passed to capacitor C_2. Capacitor C_2 will be shorted by switch S_2 for discharging.

Section 5.2.2, explains about the use of a transistor as switch for shorting capacitances. Implementing switch S_2 by a transistor will give accuracy problems due to a high R_{ds} at a low V_{ds}. Due to the high R_{ds}, capacitor C_2 depicted in Figure 7.4 cannot be blanked completely. Another solution should be found for blanking the capacitor.

7.1.4. Capacitor blanking

If the capacitor is not blanked, an opposite charge of the offsetting charge will be injected in the capacitive divider during returning to the initial state of the charge amplifier. If during blanking of the charge amplifier the capacitor is connected reversely, two charge injections with the same polarity will be applied to the capacitive divider. Both charge injections are defined accurately by the charge amplifier solving the accuracy problem.

This principle basically consists of a double charge injection. Figure 7.5 shows the double charge injection circuit which is able to reverse the capacitor polarity. The circuit is almost the same as the one depicted in Figure 7.4. Two extra switches S_8 and S_9 are added. During the capacitor blanking step, switches S_3 and S_8 are closed and switches S_2 and S_9 are open. During the return to initial state of the amplifier, switches S_2 and S_9 are closed and S_3 and S_8 are open, reversing the capacitor polarity.

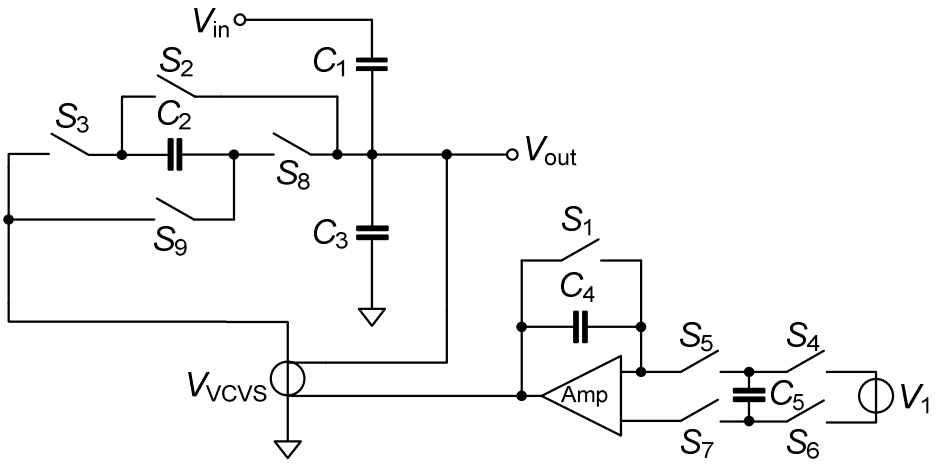

Figure 7.5: Double charge injection circuit with a fixed reference charge amplifier

A transient simulation of the circuit is performed in order to check if the circuit functions properly. Figure 7.6 shows input voltage V_{in}, which is the saw tooth curve and output voltage V_{out}, which is the offsetted saw tooth curve. For this simulation capacitance C_1 is equal to capacitance C_3. The offsetted output signal contains two voltage drops of 0.4 volt. The first one is caused by the charge injected by applying a voltage step generated by the charge amplifier to capacitor C_2. The second voltage drop is created by returning to the initial state of the amplifier and reversing the capacitor polarity.

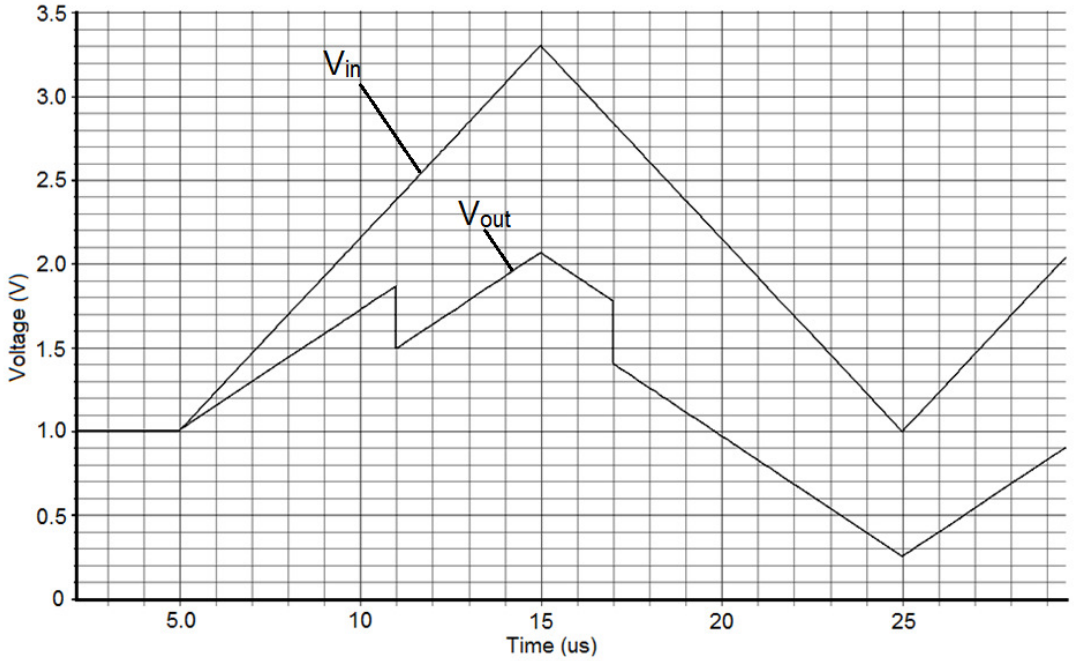

Figure 7.6: Transient simulation of double charge injection circuit with fixed reference amplifier

7.2. Practical circuit design

The ideal circuit will be implemented in several parts by CMOS components. The first implemented components are the capacitors of the capacitive divider at the input and the charge injecting capacitor. These three capacitances do not influence the simulation results. This is as expected because in section 5.2.2, the same implemented capacitive divider also did not influence the simulation results. The switches switching the charge injection capacitor will be discussed in the next section.

7.2.1. Switches

Ideal switches are replaced by NMOS transistors. The schematic is depicted in Figure 7.7. Standard values for the width (10 µm) and length (0.35µm) are used.

Input signal V_{in}, coming from the differential voltage follower V_{VCVS} (see Figure 7.5), is applied to transistor T_1 and passed to capacitor C_1. Capacitor C_1 creates a charge which will travel through T_2 to the output represented by V_{out}. When the charge amplifier returns to its initial state, T_3 and T_4 will be closed. The polarity of the capacitor is now reversed and the charge applied to the capacitive attenuator has the same polarity as the first charge. For preventing charge injection by the switching transistors, dummy transistors can be used. Dummy transistors do not completely cancel charge injection coming from the switching transistor leaving a residual charge.

Input signal V_{in} ideally varies between 0 and 3.3 volt. The clock of the transistor is also in the range of 0-3.3volt. To prevent the transistors from turning off, clock bootstrapping will be applied. By applying clock bootstrapping, charge injection caused by the switching of the switching transistors will be defined very accurately. For this reason, dummy transistors can be omitted in the circuit. The noise contribution of the switching transistors will be lower because a bigger V_{GS} is achieved. Next section will handle the clock bootstrapping concept.

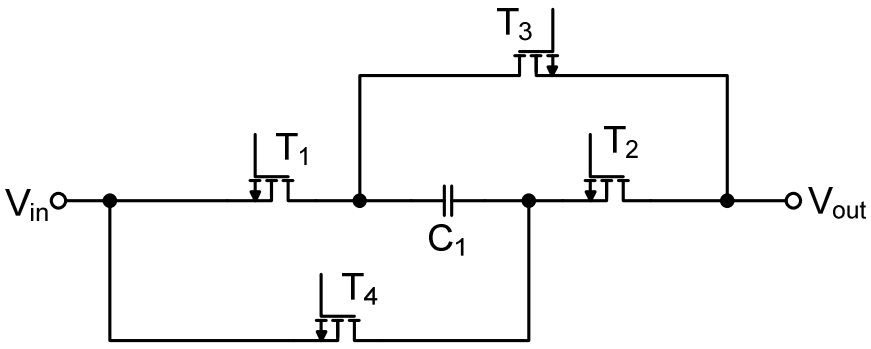

Figure 7.7: Practical implementation of capacitor reversing switches

7.2.2. Clock bootstrapping

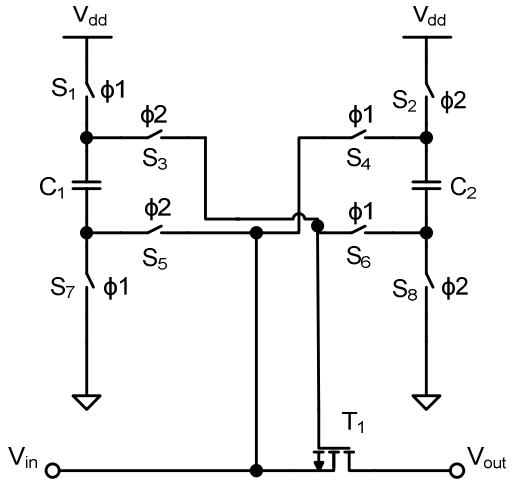

Figure 7.8: Clock bootstrapping principle

The concept of bootstrapping consist of creating a constant voltage drop between the gate and source of a transistor during on-state and creating a constant voltage drop between gate and source during off-state. This can be achieved by a applying a charged, floating capacitor between gate and source. An ideal clock bootstrapping circuit is depicted in Figure 7.8.

Eight switches can be distinguished. Four are controlled by ϕ_1 and four are controlled by ϕ_2. When ϕ_1 is high, ϕ_2 is low and vice versa. Control signals ϕ_1 and ϕ_2 are non-overlapping clocks. When ϕ_1 is high, capacitor C_1 will be charged and capacitor C_2 is connected between the gate and the source of transistor T_1. When ϕ_2 is high, capacitor C_2 will be charged and C_1 is connected between the gate and the source of transistor T_1 [30]. Transistor T_1 represents one of the transistors depicted in Figure 7.7. To control all four transistors depicted in Figure 7.7, four clock bootstrapping circuits are needed.

Implementing all components into AMIS I3T25 CMOS technology, care has to be taken in choosing the correct transistor type. Voltages above the supply level may exist over the switches. The switches will be replaced by P- or N-type transistors. The clock bootstrapping implemented in CMOS is depicted in Figure 7.9. Because the positive capacitor nodes of capacitor C_1 and C_2 can exceed the supply voltage, transistors T_1 and T_2 are PMOS transistors. Transistors T_7 and T_8 are NMOS transistors. The drain terminal will not exceed the supply or become negative. The drain of transistor T_4 will be connected to the source of switch transistor T_9.

At the node between T_4 and T_9, the voltage will not exceed supply and thus transistor T_4 can be NMOS. The drain of transistor T_6 is connected to the gate of switch transistor T_9. The voltage at the gate will be lower than at the source. For transistor T_6, an NMOS transistor can be used. The drain of transistor T_5 is connected to the source of switch transistor T_9. The drain will not exceed the supply, hence an NMOS transistor can be used. The drain of transistor T_3 is connected to the gate of T_9. The voltage at this node can exceed the supply, hence a PMOS transistor should be used. The PMOS transistors need an inverted clock signal compared to NMOS transistors. Transistors T_2 and T_3 should be connected to the inverted clock ϕ_2, indicated as $/\phi_2$. Transistor T_1 has to be connected to the inverted clock ϕ_1, indicated as $/\phi_1$. The supply voltage of the bootstrapping circuit is chosen to be 1 volt for preventing voltage drops over the wells higher than 3.3V. The bootstrapped clock voltage between gate and source of T_9 will be +1 volt (on-state) or -1 volt (off-state).

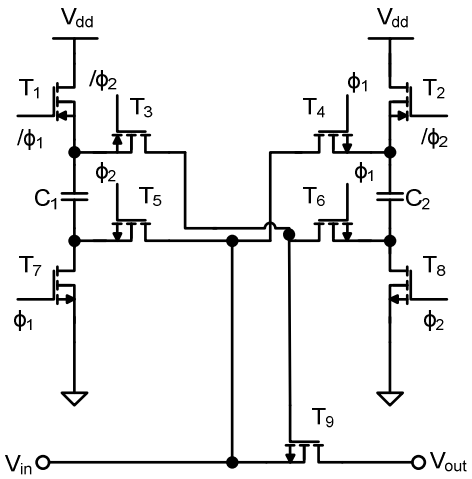

Figure 7.9: Practical clock bootstrapping circuit

The realistic switched system controlled by the non-ideal bootstrapped clock has an inaccuracy of 10µV without optimization. The switched system is accurate enough to meet specifications.

7.2.3. Three state amplifier

Charge amplifier *Amp* and voltage controlled voltage source V_{VCVS} from figure 7.5 can be combined into one amplifier acting as voltage follower for the signal coming from the capacitive divider and generate positive or negative offsets. The amplifier will have three states:

- A normal voltage follower; $V_{Out}=V_{In}$
- A voltage follower plus a well defined positive offset voltage; $V_{Out}=V_{In}+V_{off}$
- A voltage follower plus a well defined negative offset voltage; $V_{Out}=V_{In}-V_{off}$

In which V_{out} is the output voltage, V_{in} is the input voltage, V_{off} the created offset voltage.

To create an offset voltage at the output of the amplifier, a voltage drop can be created in the feedback loop of the voltage follower. This can be achieved in a compact way by putting two diodes in the feedback loop, controlled by current sources. A switch is present for normal voltage follow operation. Figure 7.10 shows the three state amplifier in which N_1 represents a nullor/opamp. The feedback network configured as voltage follower is just a short circuit from the output to the negative input of nullor N_1. For creating a positive and negative offset voltage, two diodes D_1 and D_2 are added. In normal voltage follow operation, these diodes are bypassed by switch S_1. For creating a positive offset, S_1 is opened and a current flows from I_2 through diode D_2 to I_1. For creating a negative offset, a current flows from I_1 through diode D_1 to I_2. The offset voltage is determined by the threshold voltage V_{THD1} of diodes D_1 and V_{THD2} of diode D_2. The output voltage of the amplifier is determined by the input voltage plus offset voltages.

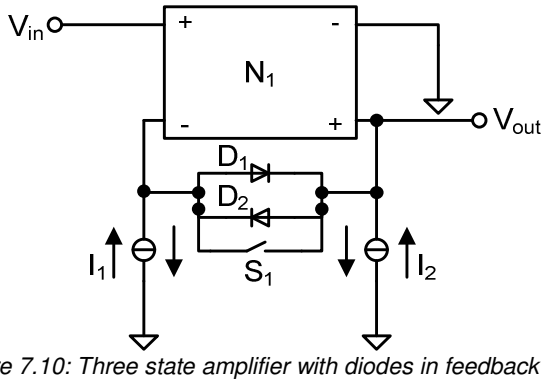

Figure 7.10: Three state amplifier with diodes in feedback loop

7.2.4. Implementation of the nullor

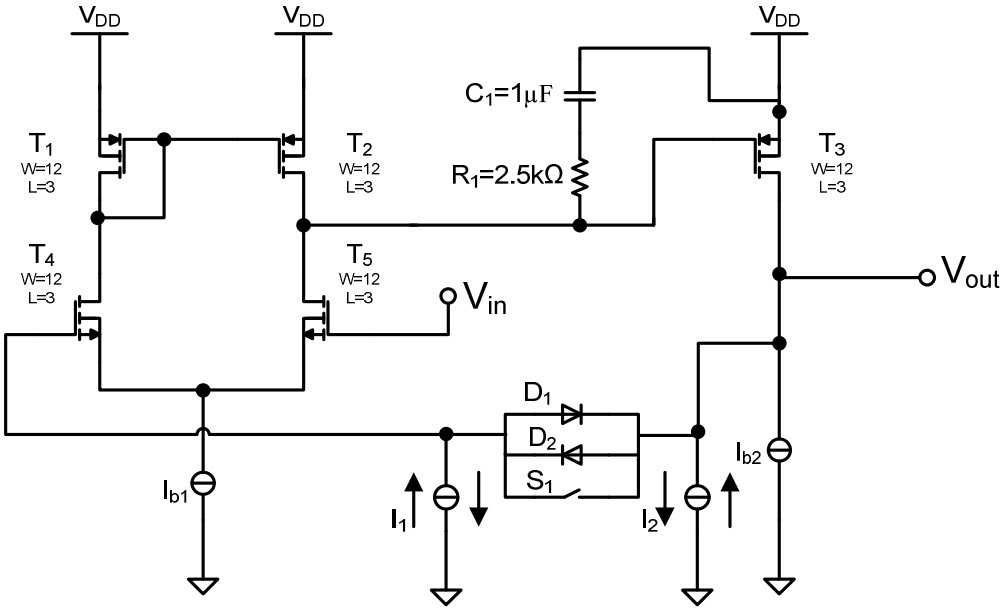

Figure 7.11: Implemented nullor including ideal biasing and feedback

Nullor N_1 should be able to follow the input signal during the voltage following state and during the offsetting states. If a stimulator generates a ramp shaped signal having an amplitude of 20 volt and a rise time of 1µs, the signal has to be switched for approximately 20 times resulting in a maximum offsetting time of 0.05µs. Within this time, the ADC should be able to take a sample of the signal. If a offsetting time of 0.01µs is taken, the remaining time is available for sampling. From this, it can be said that the amplifier should have a bandwidth of 100MHz. To reach high accuracies, a high open loop gain is needed. Therefore, a 2-stage topology is chosen. Input signals will be in the range of 0.6 to 2.7 volt. Figure 7.11 shows the implemented nullor N_1 including feedback network and ideal current sources.

The first stage consists of a differential pair. For a better output voltage range and higher gain, a second stage is added. For creating a stable amplifier, a simple resistive broadbanding frequency compensation is performed by placing R_1 and C_1 between the gate and drain of transistor T_3. Capacitor C_1 is chosen to be 1µF for simulation purposes only and will be replaced by a more practical solution later. Resistor R_1 is chosen to be 2.5kΩ and is determined by tuning.

7.2.5. Offsetting feedback loop

The offsetting feedback loop is implemented into a practical circuit composed of transistors. The circuit is depicted in Figure 7.12. Ideal diodes D_1 and D_2 are replaced by diode connected transistors T_1 and T_2. The threshold voltage of these transistors V_{THD1} and V_{THD2} determine the offset voltage created in the feedback loop. Switch S_1 is replaced by transistor T_3.

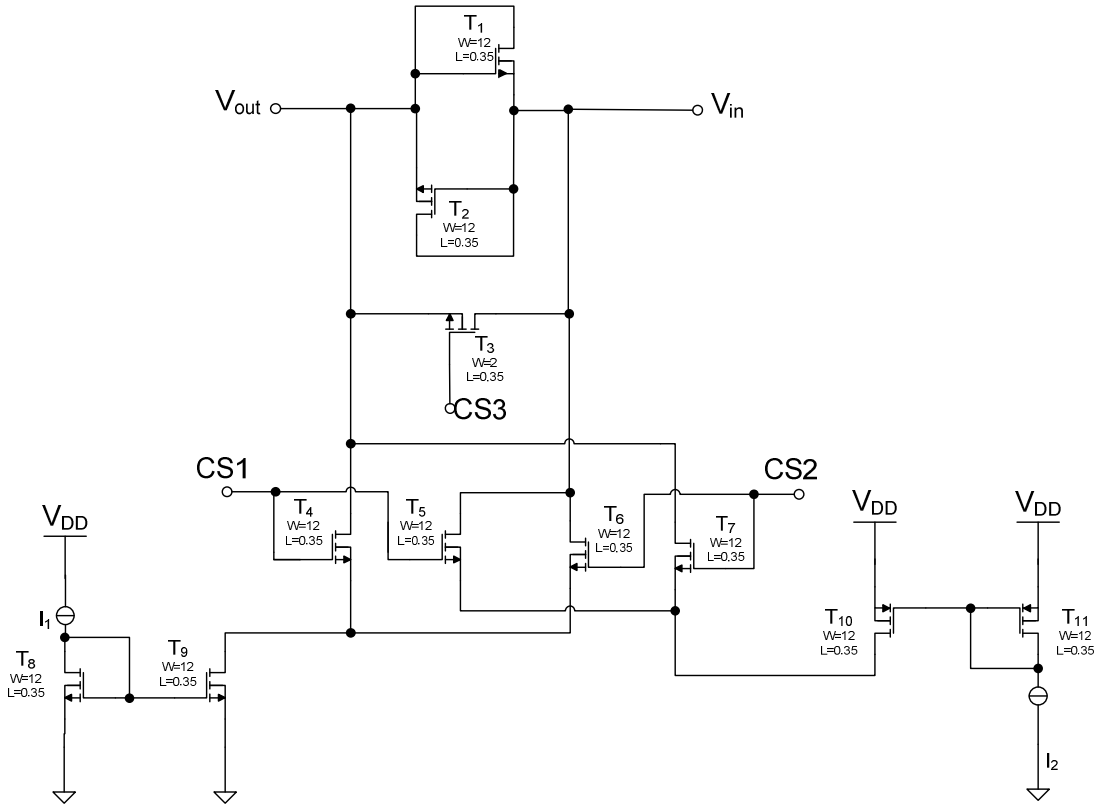

Figure 7.12: Offsetting circuitry

The reversible current sources are composed of two non-reversible current sources, I_1 and I_2, and four switches, T_4, T_5, T_6 and T_7, for reversing the current through the diode connected transistors. The fixed current sources are implemented by simple current mirrors. The current mirror delivering a positive current to the diode connected transistors is composed of transistors T_{10} and T_{11}. The current mirror delivering a negative current to the diode connected transistors is composed of transistors T_8 and T_9.

7.2.6. Frequency compensation

The ideal frequency compensation depicted in Figure 7.11 (C_1, R_1) can be implemented by practical components. If CMOS resistors and capacitors will be used, chip area consumption will rise dramatically. Alternatively, a diode connected transistor with a bias current can be used. The amplifier having CMOS frequency compensation components is depicted in Figure 7.13. Transistor T_{comp} together with current source I_{comp} represent the practical frequency compensation. Component parameters are determined by tuning. A length of 0.35µm and width of 1.7µm is used. A current I_{comp} of 104µA is used.

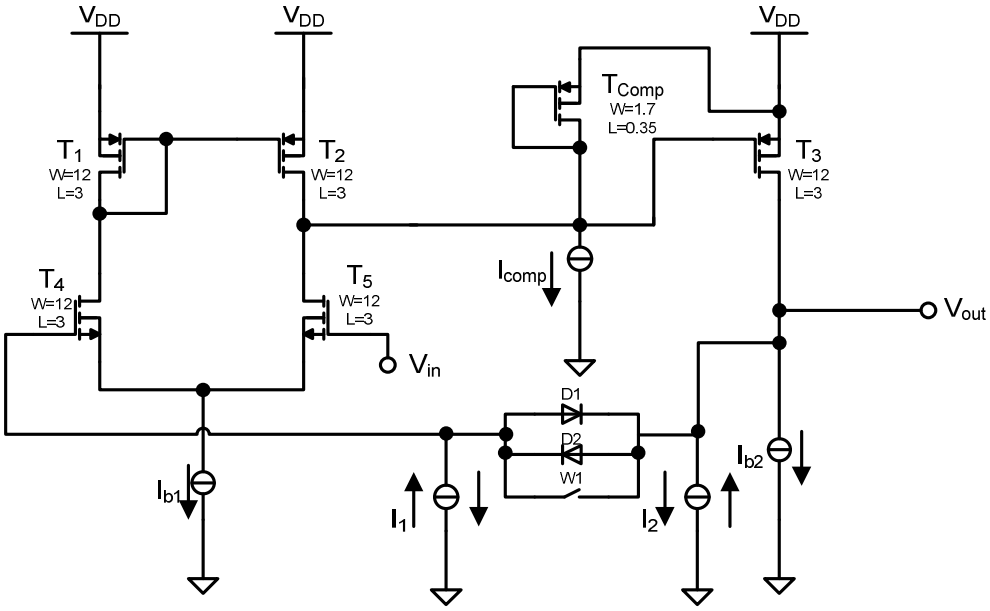

Figure 7.13: Amplifier with practical implementation of frequency compensation

7.2.7. Biasing

For biasing of the amplifier, simple current mirrors are used. The biasing as it is now is just to show that the amplifier also works with realistic current sources. The current mirror used for biasing is depicted in Figure 7.14. The current mirror is composed of two NMOS transistors T_1 and T_2.

Amplifier, frequency compensation and current sources still have to be optimized for this particular design. The circuit designed in this chapter is done to show the designed system works in CMOS and meets specifications.

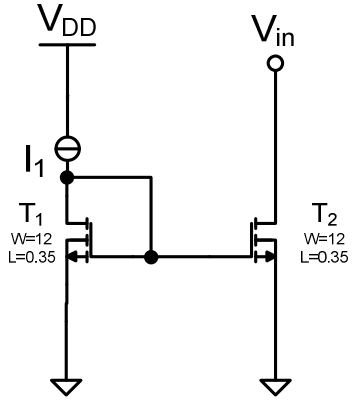

Figure 7.14: Practical current mirror for biasing

7.3. Ideal Control loop design

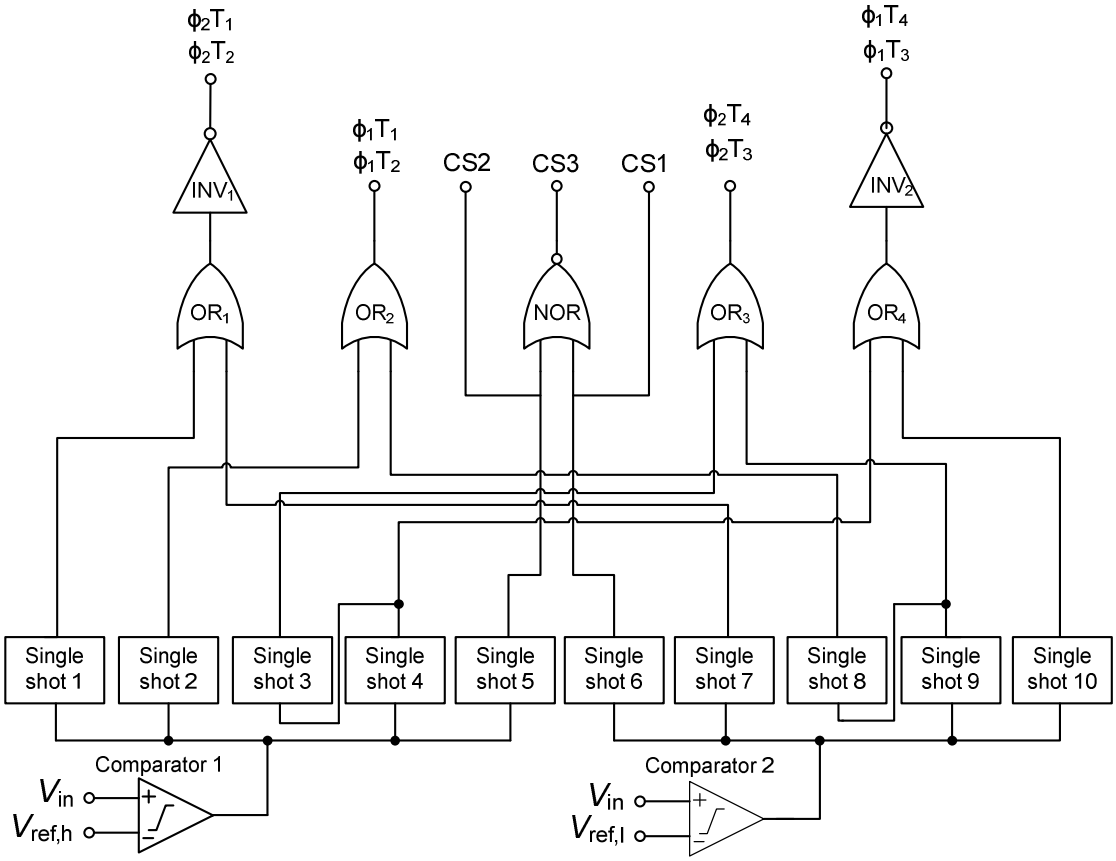

Figure 7.15: Ideal control loop

In this section, the control loop is discussed. Since the control loop is not a critical element in this design, only the ideal control loop will be discussed. A CMOS implementation of the control loop can be realized in a follow up project. Figure 7.15 shows an ideal control loop for the charge domain offsetting circuit.

The output of the charge domain offsetting circuit is applied to *comparator1* and *comparator2* as input voltage V_{in}. If the input voltage of *comparator1* exceeds the high reference, which is 1.8V, the output of *comparator1* becomes high. *Single shots 1,2,4* and *5* are activated, each having different delay times and pulse widths. *Single shot 3* is activated when the output of *single shot 4* becomes high. It also has its own delay time and pulse width. The outputs of *single shots 1,2,3* and *4* are applied to *OR*-ports. *Single shot 5* is directly connected to terminal *CS2* and to a *NOR*-port. Logic port OR_1 is connected to an inverter.

The output of the OR_1-port is connected to the NMOS transistors of the clock bootstrapping circuit (Fig. 7.9) used for transistor T_1 (Fig. 7.7), having ϕ_2 as input voltage, called $\phi_2 T_1$, and to the NMOS transistors of the clock bootstrapping circuit for transistor T_2, having ϕ_2 as input voltage, called $\phi_2 T_2$. The output of OR_2 is connected to the NMOS transistors of the clock bootstrapping circuit for transistor T_1, having ϕ_1 as input voltage, called $\phi_1 T_1$, and to the NMOS transistors of the clock bootstrapping circuit for transistor T_2, having ϕ_1 as input voltage, called $\phi_1 T_2$. For PMOS transistors, the output signals of the control loop are inverted.

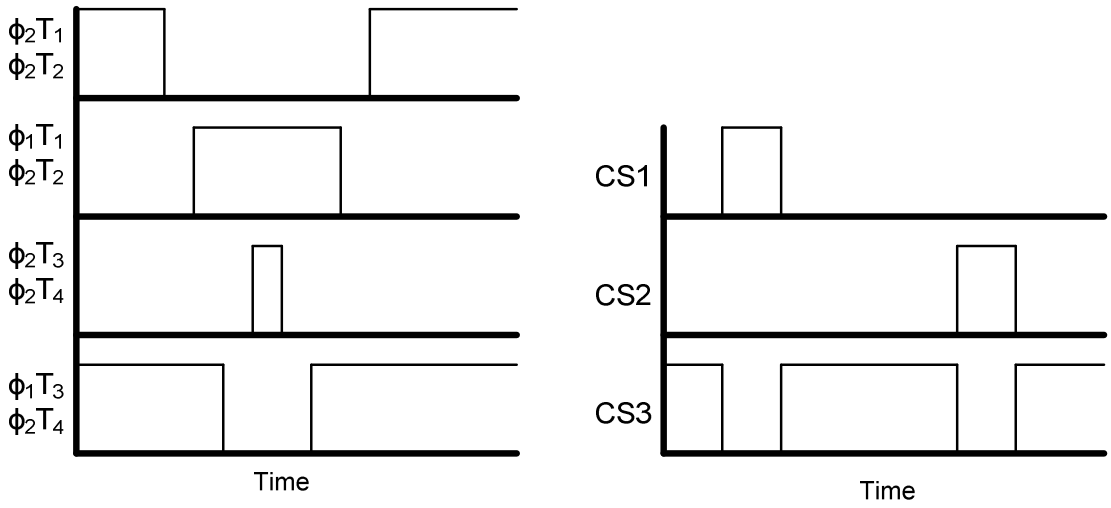

Figure 7.16: Output signals of the control loop

Figure 7.16 depicts signals coming from the control loop. Signals depicted in the plots on the left are used for controlling the clock bootstrapping circuit. Only signals for controlling NMOS transistors of the clock bootstrapping circuit are depicted. Signals for controlling PMOS transistors are the inverted control signals for the NMOS transistors. Signals depicted in the plots on the right are used for controlling the reversible current sources discussed in Section 7.2.5.

If the input voltage of *comparator2* drops under the low reference, which is 1V, the output of *comparator2* becomes high. *Single shots 6,7,9* and *10* are activated each having different delay times and pulse widths. *Single shot 8* is activated when the output of *single shot 9* becomes high. It also has its own delay time and pulse width. The outputs of *single shots 7,8,9* and *10* are applied to *OR*-ports. *Single shot 6* is directly connected to terminal *CS1* and to a *NOR*-port. The output of the *NOR*-port is connected to terminal *CS3*. The OR_4-port is connected to an inverter. Terminals *CS1*, *CS2* and *CS3* are used for controlling the offsetting circuitry (Fig.7.12).

The output of the OR_4-port is connected to the NMOS transistors of the clock bootstrapping circuit for transistor T_3, having ϕ_1 as input voltage, called $\phi_1 T_3$, and to the NMOS transistors of the clock bootstrapping circuit for transistor T_4, having ϕ_1 as input voltage, called $\phi_1 T_4$. The output of OR_3 is connected to the NMOS transistors of the clock bootstrapping circuit for transistor T_3, having ϕ_2 as input voltage, called $\phi_2 T_3$, and to the NMOS transistors of the clock bootstrapping circuit for transistor T_4, having ϕ_2 as input voltage, called $\phi_2 T_4$. For PMOS transistors, the output signals of the control loop are inverted.

For implementation into a realistic circuit, the control loop can be redesigned with a shift register saving space and power consumption.

7.4. Complete circuit overview

To get a complete overview of the circuit, all components are added together and depicted in Figure 7.17. The control loop is depicted as one block since no circuit implementation of the control loop is done. More details about the control loop can be found in Section 7.3.

The circuit is composed of 59 transistors and 11 capacitors. By replacing the capacitors used in the bootstrapping circuitry by transistors, a space reduction can be achieved. Moreover, by combining bootstrapping circuits, even more space can be saved. Further research should be performed to determine if this is possible.

Next section will handle the simulation of the complete circuit.

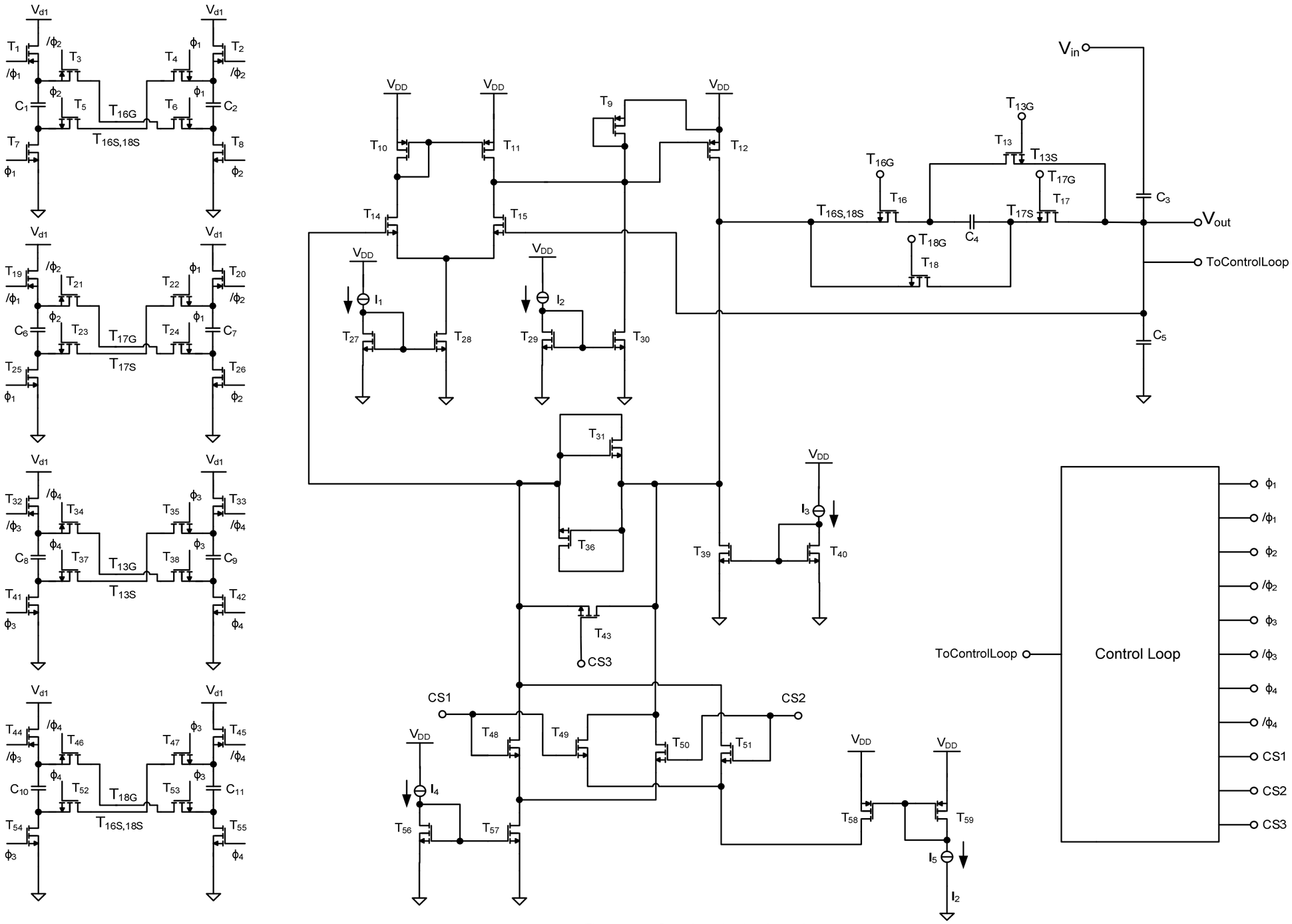

Figure 7.17: Complete circuit schematic

7.5. Simulation results

This section discusses simulation results of the complete circuit implemented in the AMIS I3T25 CMOS technology. First, a transient simulation is performed, followed by a noise simulation. Finally, a temperature simulation is performed.

7.5.1. Transient simulation

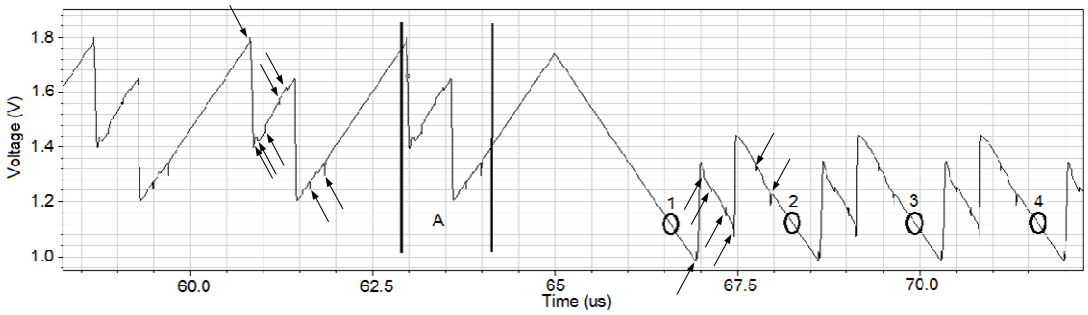

Figure 7.18: Transient simulation of the charge offsetting circuit

A transient simulation is performed on the complete circuit to check if the circuit meets specifications. A saw tooth input signal having an amplitude of 10V and a frequency of 10kHz is applied at the input. Figure 7.18 shows the output signal of the circuit. At area called A, offsetting takes place in two steps. In this part, several small bumps in the signal can be distinguished, indicated with the arrows.

These small bumps are caused by charge injection of the switching transistors for changing the charge injecting capacitor terminals and by the switches for changing the current direction in the feedback loop. At every offsetting cycle, these bumps can be seen.

For measuring the accuracy of the circuit, four time points can be measured. In the figure indicated by the numbers 1,2,3,4. All time points are measured at a voltage of 1.033000V and compared. If the system is accurate, time differences between the points should be the same. Table 7.1 shows the times belonging to the time measurement points.

Measurement point	Time (µs)
1	66.807700
2	68.487210
3	70.167077
4	71.847155

Table 7.1: Measurement point time

Difference between measurement points:	Time (µs)
(A) 1 and 2	1.679510
(B) 2 and 3	1.679867
(C) 3 and 4	1.680078

Table7.2: Difference between measurement points

Time differences between the measurement points can be calculated. Results are presented in table 7.2. The expectation is that the time differences are the same every time. This is not the case. A deviation between (A) and (B) of 257ps is found and a deviation of 211ps between (B) and (C) is found. Taking more points, again deviations in this range are found. The deviations are caused by charge injection of the switches and can be approximated by an average deviation of 234ps. The difference between the deviations is 46ps, which gives 23ps per measurement point. Shifting 23ps in the graph gives a deviation of 9µV.

Increasing the amplitude to 20V, the slope of the signal becomes steeper and the deviation will increase to 18µV, which is too big. By making the simulation steps smaller, an accuracy of 9.6µV is obtained. Because this circuit is not optimized, a major reduction of the deviation should be possible by optimization.

From the graph, it can be seen that switching takes approximately 0.25µs which is 5 times too long. By making the control loop sequence faster, this problem is solved.

The total power consumption of the circuit during operation is 1,254mW. A total current of 418µA is consumed, which is very high. Most current is consumed by the amplifier. For reducing power consumption, this amplifier should be tuned, or even replaced by another amplifier concept.

7.5.2. Noise

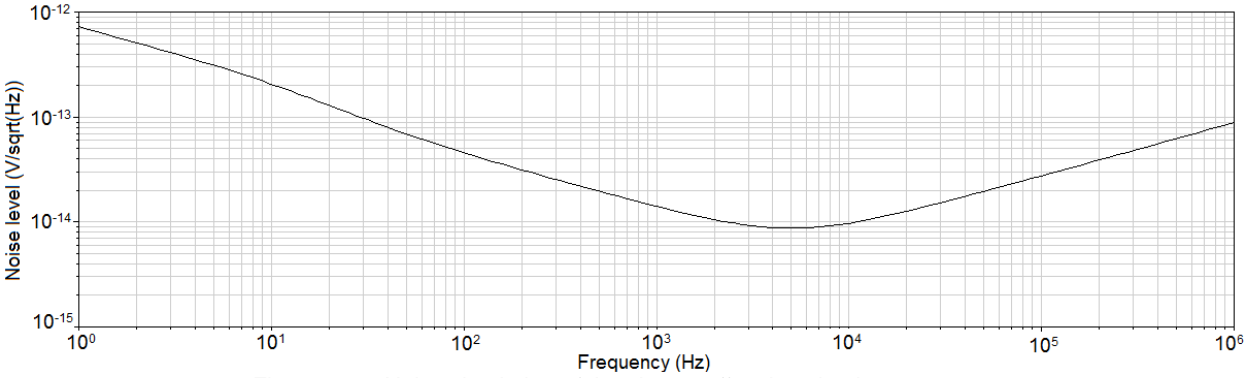

Figure 7.19: Noise simulation of the charge offsetting circuit

A noise simulation of the circuit is performed to determine the noise behavior of the circuit. Results are depicted in Figure 7.19. Integrating the noise over the bandwidth gives a total noise of $1.1 \cdot 10^{-12}$ V. This is within specifications.

7.5.3. Temperature simulation

To determine the temperature behavior of the circuit, a temperature simulation is performed. The same input signal is used for this simulation as for the transient simulation. Figure 7.20 shows the output signal at two different temperatures. A total of 500 runs is done, but for clarity, only two runs are depicted here. The difference between the two curves is clearly visible. This is due to a gain error of the capacitive divider and due to the temperature dependency of the threshold voltages of the diode connected transistors. Also, a difference in charge injection of the switch transistors can be seen. A calibration can be used to correct for the gain error. The same holds for the diode connected transistor threshold voltage. The charge injection which deviates can also be calibrated obtaining high accuracies. Calibration is possible because the implant is placed inside the human body, which keeps its temperature very stable. Temperature simulation does not reveal any obstructions for the circuit.

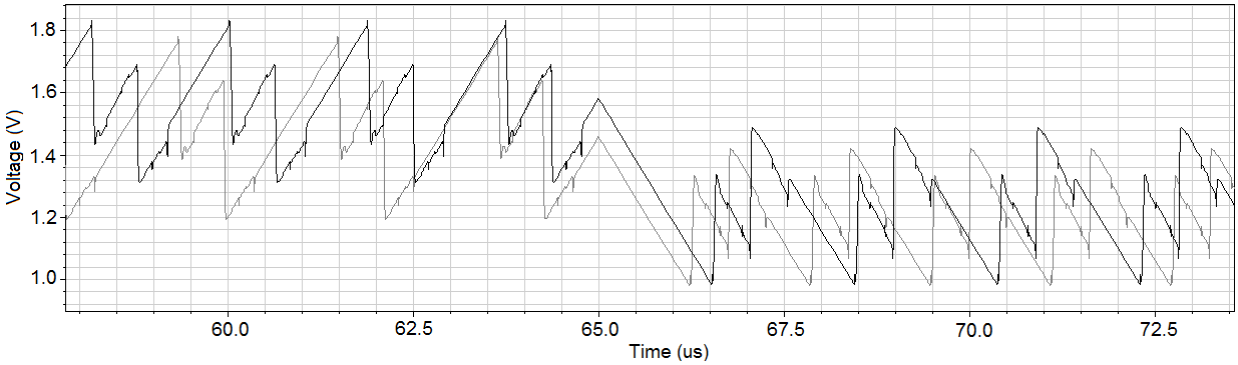

Figure 7.20: Output of a parametric temperature simulation

7.5.4. Monte Carlo Simulation

To determine the random behavior of the circuit, a Monte Carlo simulation is performed. The same input signal is used for this simulation as for the transient simulation. Figure 7.21 shows the output signal at two different simulation runs. A total of 500 runs is done, but for clarity, only two runs are depicted here. The difference between the two curves is clearly visible. This is due to a gain error of the capacitive divider. Also, a difference in charge injection of the switch transistors can be seen. A calibration can be used to correct for the gain error. The charge injection which deviates can also be calibrated obtaining high accuracies. Monte Carlo simulation does not reveal any obstructions for the circuit.

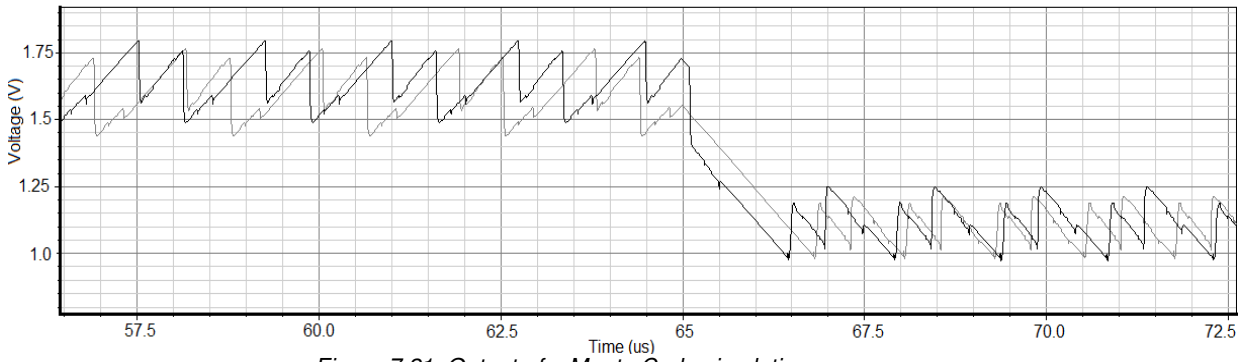

Figure 7.21: Output of a Monte Carlo simulation

7.5.5. Process Corners

To determine the behavior of the circuit due to process variations, worst case situations (corners) are simulated. A sine wave having a frequency of 10kHz and an amplitude of 10V is applied at the input of the circuit. Figure 7.22 shows the output signal at every process corner.

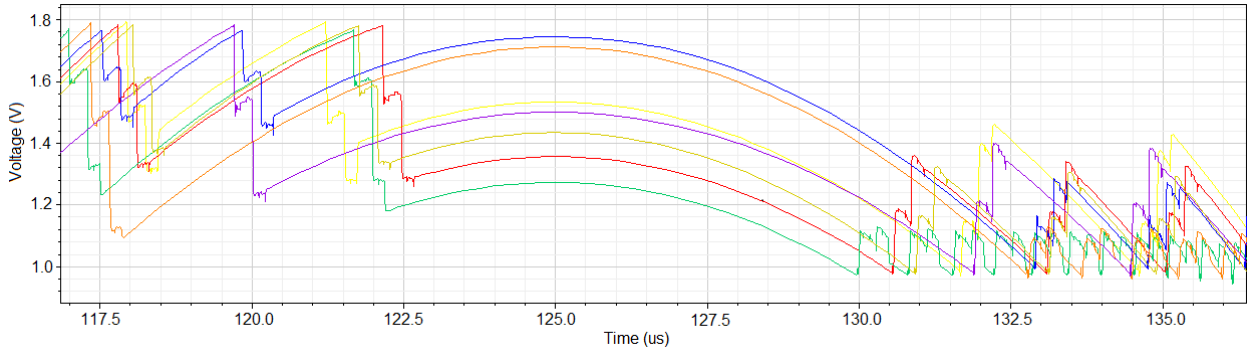

Figure 7.22: Output of a process corners simulation

Every line represents a corner according to table 7.3. in which awcs, awcp, awc1, awc0 are process corners of the transistors and min and max process corners of the capacitors. At typical, all components are at their typical value.

Line color	Corner
Yellow	Awcs
Red	Typical
Green	Awcp
Blue	Awc1
Orange	Awc0
Purple	Min
Brown-yellow	Max

Table 7.3: Process corner and line color

The output curves obtained for every process corner clearly differ from the typical output curve. This is due to a gain error of the capacitive divider. Also, a difference in charge injection of the switch transistors can be observed. A calibration can be used to correct for the gain error and charge injection deviation. Besides that, some curves show more than two voltage steps during offsetting, while two steps are expected.

Figure 7.23 shows the output curve at the awcs corner. The negative offsetting step is represented by the numbers 1, 2 and 3. At (1), the first voltage step takes place. At (2), the second voltage step takes place by reversing the charge injecting capacitor polarity as explained in Section 7.1.4. However, because the control loop switches the capacitor polarity back to initial state too fast, the capacitor is not fully discharged. At (3), the capacitor polarity is changed back to its initial state and the residual charge is applied to the capacitive divider creating a voltage step.

The positive offsetting step is represented by the numbers 4, 5 and 6. At (4), the first voltage step takes place. However, because the control loop reverses the capacitor polarity too fast, the charge injection from the capacitor into the capacitive divider is not finished yet. At (5), the second voltage step takes place by reversing the charge injecting capacitor polarity as explained in Section 7.1.4. At (6), the capacitor polarity is changed back to its initial state and the residual charge which was not applied at (4), is now applied to the capacitive divider creating a voltage step.

By reducing the control loop switching sequence speed, the third voltage step can be avoided. Another solution is to lower the switch resistances.

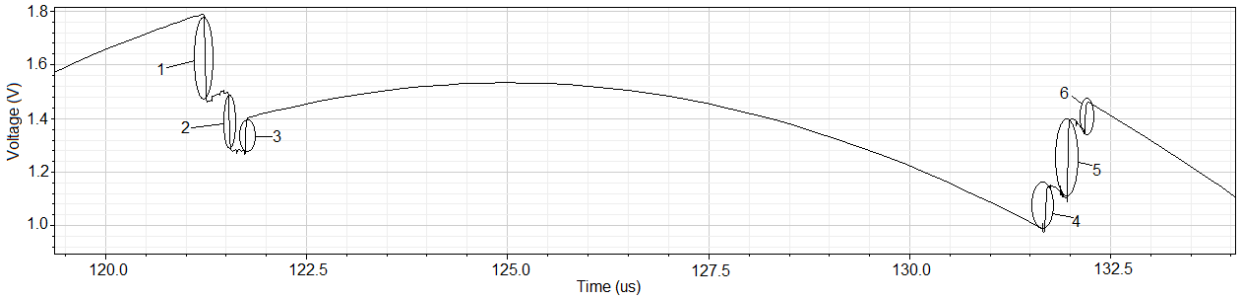

Figure 7.23: Separate output of the awcs corner simulation

7.5.6: Output signal reconstruction and linearity

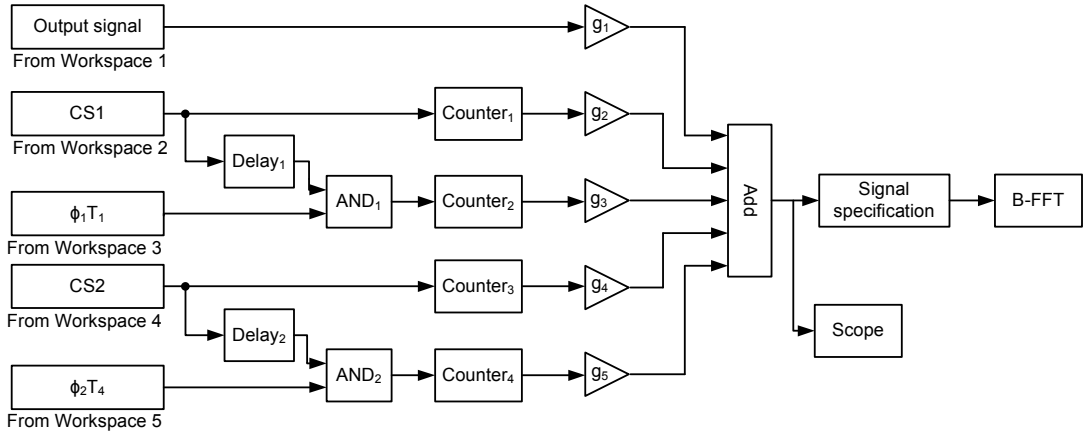

Figure 7.24: Simulink reconstruction circuit

To reconstruct the signal coming from the circuit, the output curve of the circuit simulated in Cadence is exported to Matlab. This is also done for the control loop signals *CS1*, *CS2*, $\phi_1 T_1$ and $\phi_2 T_4$. The control loop signals are used to reconstruct the output curve of the circuit back to its original. The input signal of the circuit is the same as in Section 7.5.5. Figure 7.24 shows the reconstruction schematic built in Matlab Simulink.

The blocks *From Workspace* are used to import the signals from Cadence into Simulink. Gain block g_1 corrects for the gain of the capacitive divider. Delay blocks $Delay_1$ and $Delay_2$ together with the logic blocks AND_1 and AND_2 create the signal for compensating the second voltage step of the circuit offsetting sequence. Counters $Counter_1$, $Counter_2$, $Counter_3$ and $Counter_4$ count the control loop pulses creating offsets used for compensating the offsets generated by the circuit. Gain stages g_2, g_3, g_4 and g_5 amplify the output signals of the counters to the proper offset levels. The offset values and the amplified output signal are added creating a reconstruction of the original signal. For readout the reconstructed signal, a *Scope* is present. For determining the linearity, a *B-FFT* analysis block is added. Signals coming from the *Add* block are not suitable for direct application to the *B-FFT* block. Therefore, a *Signal specification* block is added.

Figure 7.25 shows the signal appearing at the *Scope* display. The reconstructed sine wave having spikes on top is depicted. These spikes are due to the offsetting of the circuit. Zooming in, even the charge injection of the switches can be distinguished.

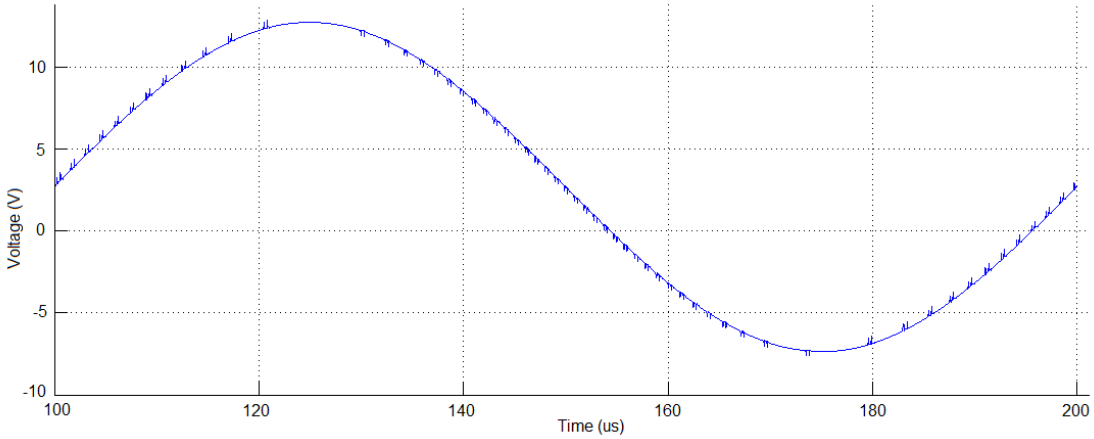

Figure 7.25: Reconstructed output signal

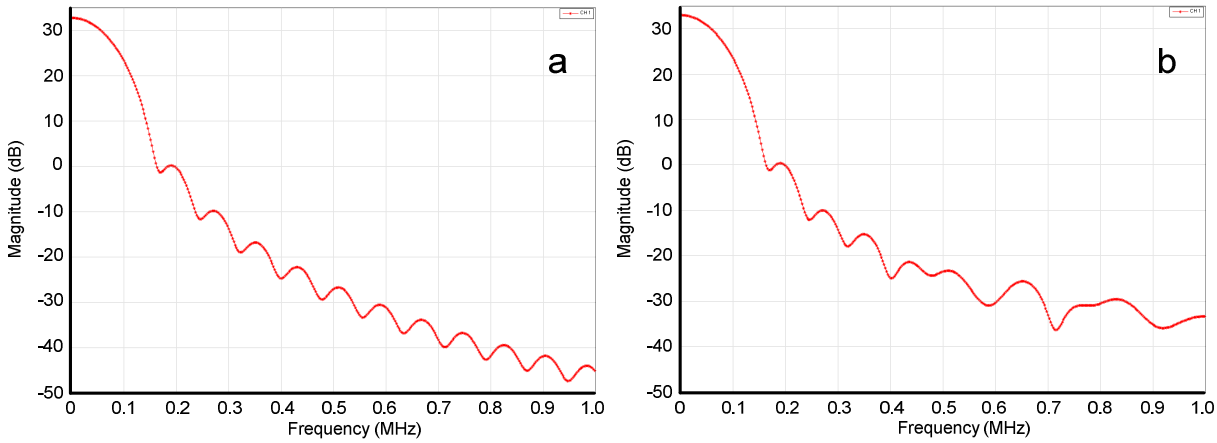

Figure 7.26: Fourier analysis output of a sine wave and of the circuit output

To determine linearity, a Fourier analysis is performed of a clean sine wave and the reconstructed sine wave coming from the circuit. Both have the same frequency, amplitude and offset. Figure 7.26 shows the results. Plot (a) shows the Fourier analysis of a clean sine wave and plot (b) shows the Fourier analysis of the reconstructed signal. Both signals are the same until approximately 400kHz. Above this frequency, major deviations are visible. This is not a problem, since the frequency of interest is much lower.

7.5.7. Results

In this chapter, a charge domain offsetting method is proposed. A system design is made, followed by the implementation as an ideal circuit. The ideal circuit is finally converted to an implementation in the AMIS I3T25 CMOS technology. Some simulations are performed on the implemented circuit.

Firstly, a transient analysis is performed, The offsetted output is plotted and analyzed. Results show the inaccuracy due to switching is too high. Tuning of this circuit should be performed to solve this problem.

Secondly, a noise analysis of the complete circuit in operation is performed. Integrating the noise over the bandwidth gives promising results.

Thirdly, a temperature sweep is performed. Results show a varying gain factor and varying charge injection. Because the circuit will be implanted in the human body, temperature will be very constant. A calibration will be sufficient to solve this problem.

Fourthly, a Monte Carlo simulation is performed. Results show a varying gain factor and varying charge injection. A calibration will be sufficient to solve this problem.

Fifthly, a process corners simulation is performed. Control loop times are too fast at certain corners. Extending these times or tuning the switches will solve this problem.

Finally, a reconstruction and linearity is performed. The reconstructed signal consists of the original sine wave with some added spikes due to offsetting. Fourier analysis of the reconstructed signal do not reveal problems.

The circuit presented in this chapter should be developed more to make it power efficient and to reduce space consumption.

Chapter 8: Results & recommendations

This chapter contains a discussion of the designed system, circuitry and the results. This chapter subsequently elaborates on the recommendations.

8.1. Results

In this thesis, several things are discussed. Firstly, a literature study is performed about the working of the human hearing system. This literature study includes the description of the ear, from the outer ear to the inner ear. This is followed by a study about the behavior of neural tissue located in the cochlea resulting in the representation of tissue as an electrical circuit.

Secondly, hearing disorders are discussed followed by the explanation of a prosthesis for partially restoring human hearing, called the cochlear implant. Signals occurring at the electrodes of a cochlear implant are identified. Shortcomings of existing cochlear implant neural response readout systems are discussed. Specifications are found for a proper cochlear implant readout system.

Thirdly, an investigation is performed on readout systems which are available. Positive and negative properties are discussed. None of the existing systems is able to meet the specifications needed for the neural response readout system.

Fourthly, a system design for new readout circuitry is proposed. The system design consists of input circuitry, followed by compensation of the measured signal by a predicted signal. Then, the remaining signal is amplified and digitized. The signal is reconstructed digitally.

Fifthly, a system design for the readout input circuitry is investigated. Existing techniques are considered but cannot meet specifications. An alternative technique called additive companding is proposed to meet the specifications. A system design for this technique is performed and implemented in an ideal circuit.

Sixthly, the ideal circuit is implemented in the voltage domain, which meets specifications having an ideal and very fast control loop. When a practical control loop is applied, specifications are not met due to control loop delays and tolerances which are too large.

Seventhly, an alternative circuit based on parallel capacitors is proposed. During design, it became clear that specifications cannot be met. This is due to the change of the division ratio of the capacitive divider during offsetting. In combination with the control loop speed and accuracy which are too low, this causes too large inaccuracies. The circuit actually has the same problem as the circuit implemented in the voltage domain.

Finally, an alternative circuit implemented in the charge domain is proposed. A circuit definition into CMOS is made. Although this implementation is not optimized yet, results with ideal control loop are promising. The control loop is not the limiting factor of the circuit as was the case in the other two circuit implementations.

8.2. Discussion

A new system level design based on compensation is proposed to deal with the limited dynamic ranges of readout circuitry in cochlear implants. This system allows the complete readout of evoked compound action potentials including stimulus and artifact at a high resolution. This enables researchers to do new research on the working of the cochlea to improve stimulation techniques and move towards a closed loop stimulation system.

The new readout system level design has some similarities with the amplifier used in [10], which is the amplifier used at the Leiden University Medical Centre. This amplifier also uses compensation. This compensation is performed in the voltage domain while the compensation

used in the system proposed in this thesis is based on charge domain compensation. Moreover, the amplifier used in [10] is only capable to cancel the artifact by a predicted artifact, while the system proposed in this thesis also compensates the stimulus by subtracting a predicted signal in the charge domain.

The readout system designed in this thesis is able to read out signals above the supply level obtaining a large DR of 126dB without the occurrence of clipping. Multiple electrodes can be readout simultaneously. However, noise behavior and power consumption is not optimized yet and offsets created due to switching of the input circuitry are still too big. The design can become very bulky, so care has to be taken to prevent this. Moreover, only a coarse input circuit is designed. The rest of the system still consists of ideal blocks which can cause problems in the design later.

8.3. Recommendations

This thesis forms a starting point for the design of a readout system for application in cochlear implants. Only a small part of the system is investigated and implemented giving the need for future work to finish this. Because this project is too big to do by a single master student a PhD position should be created for this work.

Only a coarse circuit level implementation into CMOS of the charge domain circuit is performed, Optimization of this circuitry should be performed to create a properly functioning, power efficient and compact circuit. Moreover, the control loop is still composed of ideal components and should be implemented into CMOS.

Digital noise generated in the digital part of the complete readout system can introduce major interference into the analog circuitry giving distortion of the measured signals. The vulnerability of analog circuitry to digital noise can be reduced by taking this into account during the chip layout. Guard rings should be used and a proper separation of analog and digital circuitry should be achieved. Moreover, to reduce digital noise, the digital circuit should be held into a stable non-switching state during sampling of the neural signal.

8.4. Publications

[1] C.J. Bes, C. Sawigun, W.A. Serdijn, “An Additive Instantaneously Companding Readout System for Cochlear Implants,” IEEE Biomedical Circuits and Systems conference, Cyprus, 3rd -5th November 2010 *(Accepted)*.

The publication is added as appendix.

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Appendix I: BioCAS paper

An Additive Instantaneously Companding Readout System for Cochlear Implants

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***Abstract*—This paper presents an additive instantaneous companding technique in order to record the compound action potentials from the stimulated auditory nerve. This technique is intended to be combined with an analog to digital converter to achieve the 126-dB dynamic range that covers both stimulus (up to 20V), artifact and the neural response (down to 10µV). From the readout signal, the correct operation and placement of the cochlear stimulator can be estimated and useful information for further clinical studies can be obtained. The proposed system is designed to be implemented in AMIS I3T25 (high voltage) CMOS technology. Simulation results confirm the correct operation of the circuit.**

I. INTRODUCTION

At the moment more than 100,000 people suffer from deafness. In the case of profoundly deaf, the patients cannot be helped with conventional hearing aids. Cochlear implants (CIs) can successfully restore hearing of people who are profoundly deaf. CIs nowadays are the most successful and most advanced neurostimulator available. An important tool to help fitting cochlear implants to patient specific needs is a neural readout system. Besides, this readout system is used for acquiring neural responses for scientific research to get better understanding of the human hearing and pushing forward the development of autonomous closed loop cochlear implanted devices.

Reading out the neural response after stimulation can be done by using a technique called evoked compound action potential (eCAP) [1]. Unfortunately, only a small part of the total eCAP can be captured due to the limited dynamic range of the neural amplifier used.

In this paper, a compact readout system using a technique called 'additive instantaneous companding' to handle the entire range of the evoked neural response is proposed. This technique can be realized by using compact switched-capacitor (SC) circuits. Despite being compact, i.e., having a low physical area hence low total capacitance, the noise contribution of the circuit can be kept small. Using the proposed technique, the stimulus and the artifact amplitude can be lossless compressed to fit the dynamic range of a practical electronic circuit while the neural response amplitude is preserved.

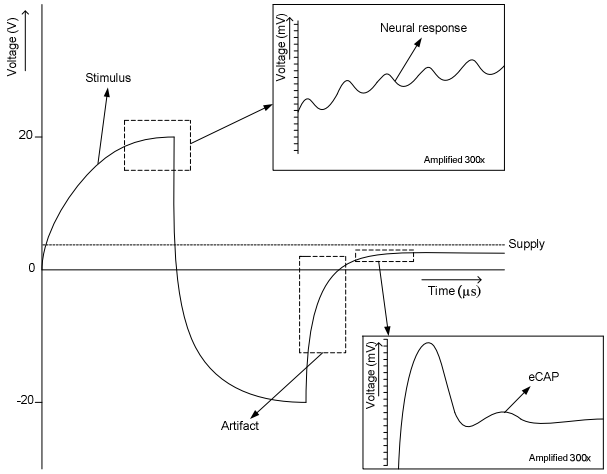

Figure 1. Signals presented at the cochlea

The remaining sections of the paper are organized as follows. In the next section, an overview of the compound action potential is described. In Sec. III, several techniques that have been investigated to read out action potentials will be discussed. The proposed technique and its circuit solutions are reported in Sec. IV. Next in Section V, the simulation results are reported. The conclusions will be drawn in the last section.

II. EVOKED ACTION POTENTIAL

Signals occurring at the cochlea excited by electrical stimulation can be divided into three categories. The first one is the stimulus generated by a stimulator; the second one the residual charge caused by the stimulus, called artifact; and the last one the neural response coming from the auditory nerves that can take place during stimulus, artifact and thereafter. Fig. 1 illustrates a typical signal occurring at the cochlea.

As can be seen from Fig. 1, the peak amplitude of the input signal can reach 20V. Neural responses can have frequencies

up to 10 kHz [2]. This implies a minimum sampling rate of 20kS/s is needed for the signal conversion. The neural response to be measured can be as small as 10µV. This implies a dynamic range of 126dB is needed. Converting this signal range into a digital code, at least 21 bits resolution is required. Using the most power efficient analog to digital converter (ADC), a successive approximation ADC, a huge area for the capacitive array and a relatively large switching energy will be needed [3].

III. EXISTING SOLUTIONS

In order to cope with the large dynamic range of the input signal, four system principles are considered.

1. *Resistive divider*: By linearly attenuating the input signal level down to the level of the supply voltage or lower. Major drawback of this method is the noise contribution of the resistors combined with the attenuation of the original signal. The neural responses will drown into the noise making this principle not suitable for this application.
2. *Multiplicative companding*: This technique
   a. compresses the dynamic range at the input, thereby decreasing the signal to noise ratio.
   b. Processes the signal in a low-voltage environment.
   c. Expands the dynamic range such that it becomes equal to that of the input signal.

   In this way, a high dynamic range can be achieved and overloading of subsequent circuitry is prevented. However, the higher the compression, the higher the noise level will be [4][5]. Just as the resistive divider, also multiplicative companding will not meet the noise requirements.
3. *Folding ADC*: A folding ADC consists of several folding cells. Each folding cell consists of high voltage components in order to handle the high input voltage levels [6]. High voltage components use a large amount of chip area compared to their low voltage equivalents which is very critical in medical implants.
4. *ΣΔ ADC*: A sigma-delta ADC can typically convert up to 24 bits. High dynamic ranges in combination with low noise levels can be achieved. However, power consumption is quite high compared to other ADC architectures. Just as in the previous case, high voltage components will be needed causing a high chip area consumption [7].

The aforementioned techniques do not provide a good solution to handle the high dynamic range signal within an electronic device that consumes a small area and low power consumption. In the next section, we propose to use the concept of additive instantaneous companding to solve the problem.

IV. PROPOSED READOUT DETECTOR

A. System

To readout the evoked action potential, an additive instantaneous companding system is proposed. Fig. 2 depicts a high level system block diagram. V_{in} represents the input signal coming from the electrode placed in the cochlea. A (small) attenuation factor g is introduced at the input. After this attenuation block, the signal is sensed by two comparators. One comparator compares the input signal with a high reference voltage, V_{refh}, and one comparator compares the signal with a low reference level, V_{refl}. When one of the reference levels is crossed, a pulse will be given to an offset generator. The positive offset will be generated when V_{refl} has been reached and when V_{refh} has been reached a negative offset will be generated. The signal coming from the offset generator is added to the attenuated signal. Then, the added signal is sampled by a sample and hold amplifier (SHA) and converted to the digital domain by an ADC. In order to keep track of the amount of positive and negative offsets generated, a shift register is added to reconstruct the input signal in the digital domain.

The output will be "reset" to a high or a low level whenever one of the voltage references is reached. Fig. 3a depicts the input and output voltages in case of a sinusoidal input signal. The output voltage follows the input voltage until reference V_{refh} is reached. Then, a negative offset is added. The signal can rise again but does not reach V_{refh} again. It goes down to V_{refl} and now a positive offset is added. This mechanism goes on throughout the whole sine wave. What actually happens is shifting the input voltage range up or down within the input dynamic range as soon as the input voltage becomes too high or too low. This can be implemented without extra noise contribution.

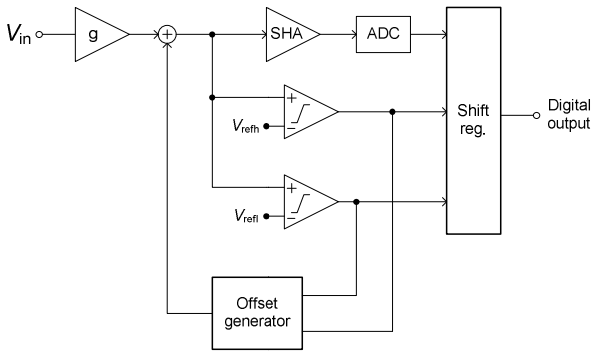

Figure 2. High level system diagram of the additive companding technique

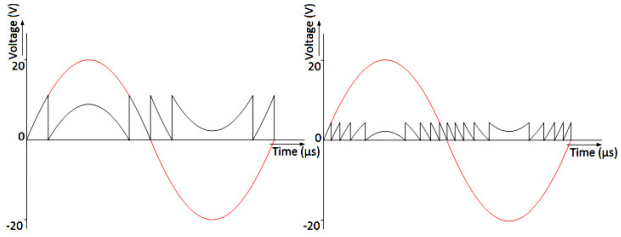

Figure 3. The input and output waveforms of the system at different reference voltages

Fig. 3b again shows the input and output signal obtained by setting a lower V_{refh} . As can be seen, this results in more switching steps.

B. Circuits

Two implementations of the system are discussed. The first one is based on offsetting in the voltage domain. The second one is based on offsetting in the charge domain.

1) Offsetting in the voltage domain

A voltage domain implementation of the system is depicted in Fig. 4. The control loop circuit that controls the switches is omitted for clarity. Gain stage g is formed by the connection of two capacitors C_1 and C_2 yielding

$$\mathrm{g} = \frac{C_1}{C_1 + C_2} \tag{1}$$

The ratio of them can be chosen such that the gain will be almost 1. The offset voltage generator can be realized by two simple switches S_1, S_2 and two voltage sources, V_H and V_L for a high and low reference voltage, respectively. The voltages are chosen to be different from V_{refh} and V_{refl} of the control loop to prevent oscillation. Capacitors C_1 and C_2 represent the attenuation stage. Switch S_1 together with V_L represent the offset voltage generator to reset to a lower voltage across C_2. Switch S_2 together with V_H represent the offset voltage generator to reset to a higher voltage across C_2. The circuit can be represented by (2) in which *floor* stands for rounding down to integers, for example so 0.8 becomes 0.

$$V_{out} = \mathrm{g} \cdot \left[V_{in} - (V_{TH1} - V_L) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_{TH1} - V_L} \right) + (V_H - V_{TH2}) \cdot \frac{1}{\mathrm{g}} \cdot floor\left(\frac{V_{in}}{V_H - V_{TH2}} \right) \right] \tag{2}$$

Accuracy of the system is crucial for the correct operation of the circuit. Offset voltages generated by the actual offsetting should not exceed 10μV. This implies that at the threshold voltage the switch has to be closed immediately to prevent overshoot. Also, the switch has to be opened fast enough in order to prevent loss of the signal as, during offsetting, the voltage across C_2 cannot follow the input signal. The control action will always undergo a certain delay and have a certain spread in exact switching time. In (2), the inaccuracy can be found by giving a small deviation to V_{TH1} and V_{TH2}. Moreover, the accuracy depends on the input signal frequency. The higher the input signal frequency, the bigger the inaccuracy will be. In order to have sufficient accuracy, the switching time should not exceed 2ps. In most technologies, this will not be possible in a low power fashion. It is therefore necessary to design the circuit in a different way.

2) Charge domain based offsetting

Offsetting can also be done by injecting a certain charge. For offsetting to lower voltages, a negative charge can be used. For offsetting to higher voltages, a positive charge can be used. The principle is depicted in Fig. 5. Attenuation stage g is identical to the voltage domain circuit described in the previous subsection. The ratio of C_1 and C_2 again can be chosen such that the gain will almost be 1.

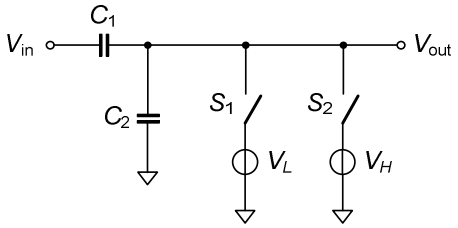

Figure 4. Voltage controlled offsetting circuit

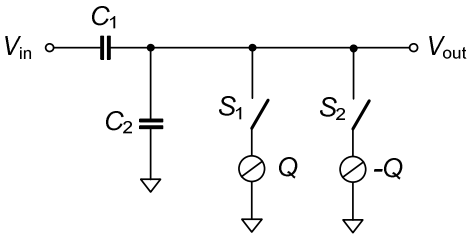

Figure 5. Charge controlled offsetting circuit

The charge injector can be realized by a charge source $-Q$ for injecting a negative charge which can be switched by switch S_1 when output voltage V_{out} reaches threshold V_{refh} and a charge source Q for injecting a positive charge which can be switched by S_2 when output voltage V_{out} reaches threshold V_{refl}. During the injection of charge Q or $-Q$, the input signal is still passed through the capacitive divider to the output. The addition or subtraction of charge does not influence the charge distribution from the input signal over C_1 and C_2 (superposition holds). A well defined charge Q or $-Q$ is added to the charge in C_2. The circuit can be seen as a dynamical system and can be represented by (3).

$$Q_{out} = V_{in} \cdot \mathrm{g} \cdot C_2 - \mathrm{Q} \cdot floor\left(\frac{-V_{in} \cdot \mathrm{g} \cdot C_2}{-\mathrm{Q}} \right) + \mathrm{Q} \cdot floor\left(\frac{-V_{in} \cdot \mathrm{g} \cdot C_2 + \mathrm{Q}}{\mathrm{Q}} \right) \tag{3}$$

In the formula, no threshold voltage is presented. This implies that the threshold levels will not give inaccuracies in addition and subtraction. Thresholds are still used in a control loop for closing switches S_1 and S_2, but the speed of the control loop and switch do not influence the accuracy of the system as was the case for the voltage-based additive companding. The accuracy is now determined by the accuracy of the charge source which can be made very accurately. The offsetting time has to be limited within 0.5 sample time. Because sampling of the subsequent sample and hold stage at the input of the ADC only occurs in between the offsetting steps and not during these steps, the added noise will ideally be zero. Because of this reason, this circuit is suitable for application in the readout of cochlear implants.

V. SIMULATION RESULTS

The charge domain based offsetting circuit is simulated using Cadence. The circuit is made using AMIS I3T25 (high voltage) CMOS technology.

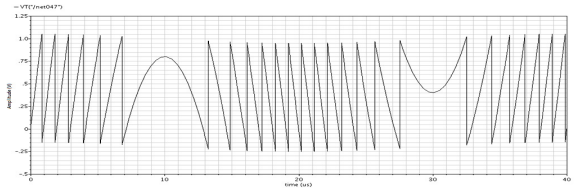

Figure 6. Compressed signal

Capacitor C_1 is realized with high voltage capacitor *mmchb* from the technology library having a finger length of 80µm and a number of fingers of 40. C_2 is realized with low voltage component *mimc* from the technology library having a width and a length of 20µm. Q and S_1 for this simulation are composed as a voltage source acting as a counter in series with a *mimc* capacitor having the same length and width as C_2. For $-Q$, the counter counts down instead of counting up. The simulation temperature is set at 37 ºC (body temperature). At the input of the circuit, a sine wave with an amplitude of 20V is applied. A gain of approximately ½ is achieved. The output of the attenuator is sensed and when a threshold of 1V is reached, the control loop will close switch S_2, thereby injecting a negative charge into C_2. When a threshold of -200mV is reached, the control loop will close S_1 injecting a positive charge into C_2. The resulting output signal (voltage) is depicted in Fig. 6. The signal is not offsetted exactly at the same voltage all the time. This is due to the different slope of the input signal and deviations in switching speed of the control loop. This does not affect the accuracy of the addition/subtraction step. The addition and subtraction steps are equal. By using a charge for offsetting, a high accuracy can be reached. Deviations of less than 1µV are reached.

A transient noise simulation is performed. The results are depicted in Fig. 7, which consists of two plots. The upper plot is the one of one period of a sine wave. The area around the peak amplitude is zoomed in and depicted in the lower plot. From this plot, the noise level is read out by the two markers. The difference is 124mV. For making the noise visible in the simulation, a magnification factor of the noise of 10.000.000 times was used (to make it visible). So, the original noise peak-peak value is 12.4nV. This is far under the 10µV which is required.

Finally, an expansion of the compressed signal is performed by adding a fixed offset to the output signal. The compressed and expanded signals are depicted in Fig. 8. The reconstructed signal looks the same as the input signal. Only one difference can be seen. The reconstructed signal is approximately ½ of the input signal, which is the same as the gain of the circuit. Gain errors can be corrected by performing a calibration.

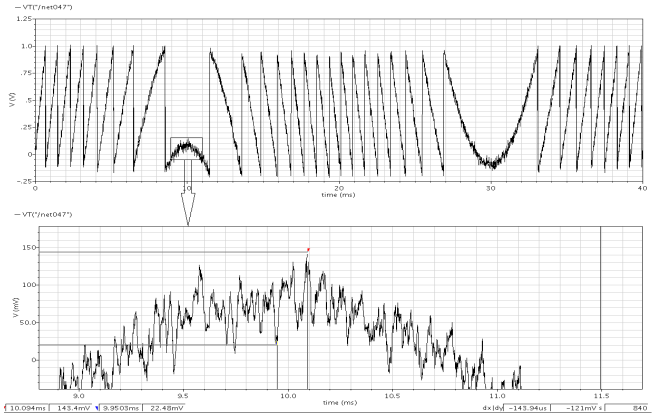

Figure 7. Noise simulation results

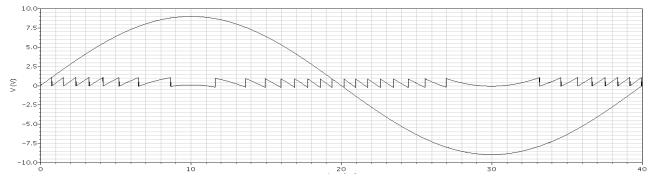

Figure 8. Reconstruction of the input signal

VI. CONCLUSION

A working circuit prototype based on additive instantaneous companding has been presented. The circuit is especially designed for application in cochlear implants read out systems. System level design and two circuit implementations have been discussed. Circuit simulations of the transient behavior, noise contribution and signal reconstruction are performed. The results verify that this method can be combined with an ADC to significantly reduce power consumption, chip area consumption and enable a very large dynamic range.

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