Features and Design Constraints for an Optimized SC Front-End Circuit for Capacitive Sensors With a Wide Dynamic Range

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***Abstract*—This paper presents optimization criteria for an integrated switched-capacitor front-end circuit for capacitive sensors with a wide dynamic range. The principle of the interface is based on the use of a relaxation oscillator. A negative-feedback circuit controls the charge-transfer speed to prevent the overload of the input amplifier for large input signals which thus enables a wide dynamic range of capacitor values. Moreover, it has been shown that the use of negative feedback can also result in much better noise performance. However, for the interface to function properly, there is a serious limitation for the value of a specific parasitic capacitance. Therefore, a method which extends the acceptable range of this parasitic capacitance is proposed. A novel method of linearity measurement which takes the influence of PCB parasitic capacitances into account, is also presented. The circuit has been designed and implemented in 0.7 μm standard CMOS technology. The supply voltage is 5 V and the measured value for the supply current is about 1.4 mA. Experimental results show that for the capacitor range of 1 pF to 300 pF, application of negative feedback yields a linearity of about 50×10^{-6} (14 bits) with a 16-bit resolution for a measurement time of 100 ms. Tests have been performed over the temperature range from $-55\,^{\circ}$C to $+125\,^{\circ}$C.**

***Index Terms*—Capacitance measurement, noise, nonlinearity, switched capacitor circuits.**

I. Introduction

CAPACITIVE sensors are used in a wide variety of physical measurement systems [1], such as liquid–level gauges, pressure meters, accelerometers, etc. In these systems a physical quantity is converted into a capacitance change. Next, the capacitance change is converted into a digital signal using a sensor interface.

Simple, low-power A/D conversion can be achieved first by converting the value of an electrical parameter (in this case the capacitance) into a period-modulated signal by using a so-called modifier, and next by using the microcontroller peripherals to digitize the time modulating signal into the digital domain [2]–[5]. The modifier can easily be implemented with relaxation oscillators. This principle has been applied in, for instance, Smartec's universal transducer interface (UTI) [6]. This interface offers four different modes for various ranges of capacitor values from 2 pF to 300 pF.

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For many applications, it would be more convenient if this range could be covered with fewer modes. Moreover, a high resolution must be obtained in a short measurement time, especially in capacitive sensors which measure mechanical parameters. In [4] it is shown that the range for larger capacitive signals is limited by possible overload from the input integrator and that this range can be extended with a switched-capacitor interface with negative feedback. The circuit described in [4] was implemented with discrete components. In this paper it will be shown that applying negative feedback can also result in a significant improvement in the noise performance. On the other hand, it will be shown that due to the occurrence of a specific parasitic capacitor, in many practical applications the circuit with negative feedback cannot work properly unless specific measures are taken. The details of this problems and its solution are presented in Section III of this paper.

The interface circuit has been developed for implementation in 0.7 μm standard CMOS technology. In order to reduce the effects of temperature changes, drift, and other nonidealities of the interface, we applied the three-signal-auto calibration technique.

II. Basic Principle of the Interface

Fig. 1 shows the basic principle of the interface with negative feedback. In this circuit, $I_{\rm b} = mI_{\rm int}$, V_1, and V_2 are block-shaped voltages with an amplitude of $V_{\rm dd}/2$. The basic idea of the circuit is similar to that of the circuit presented in [4]. However, the circuit has been modified and redesigned for implementation as a CMOS integrated circuit. Since offset effects for the integrated circuit are intolerably high, we added a special kind of chopper, following the $(+--+)$ principle described in [3]. This chopper and corresponding "de-chopper", together with the filter, act as a second-order switched-capacitor filter. Besides offset and $1/f$ noise, this filter also removes low-frequency interference which is caused by parasitic coupling of the main-supply to the sensor electrodes. Some important signals of this circuit are shown in Fig. 2.

To understand the basic principle of this circuit, we ignore the two feedback loops that are indicated with dashed lines and assume that $C_{\rm x}$ and $C_{\rm o2}$ are driven in the same way. During the time interval T_1, φ_1 starts with a transient at the HIGH state, which causes the charge $Q_1 = V_{\rm dd}C_{\rm o1}$ of $C_{\rm o1}$ to be pumped into integrator capacitor $C_{\rm int}$. Next, this charge is removed by the integration of $I_{\rm int}$. During the time interval T_1, the capacitor $C_{\rm x}$ is charged by the supply-voltage source $V_{\rm DD}$. At the beginning of time interval T_2, φ_2 changes from low to high, the drive-side of

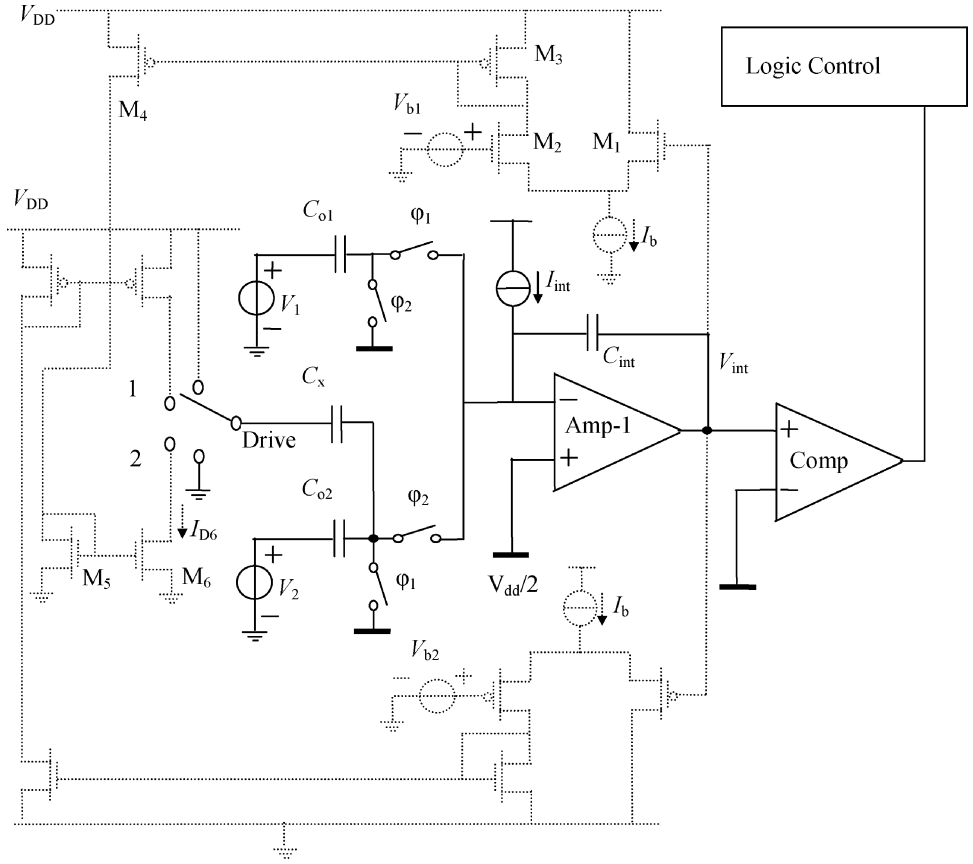

Fig. 1. Capacitive–sensor interface with negative feedback.

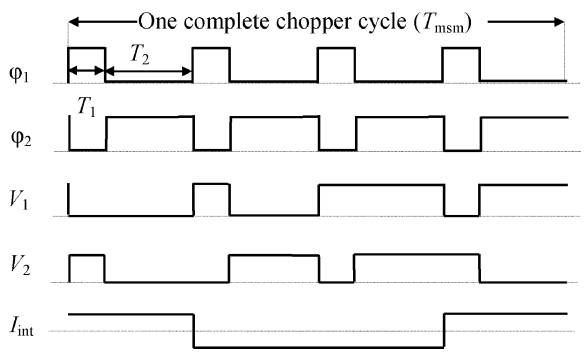

Fig. 2. Some related signals of the interface of Fig. 1.

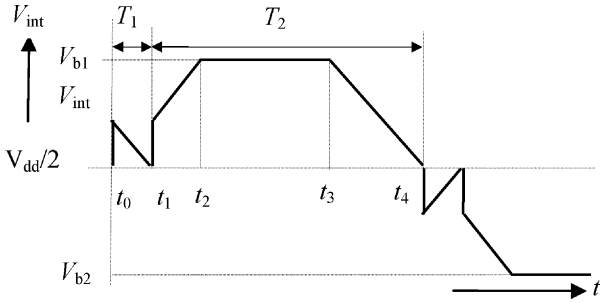

Fig. 3. Integrator output voltage $V_{\rm int}$ versus the time.

$C_{\rm x}$ is grounded, and the charge $Q_2 = V_{\rm dd}(C_{\rm o2}+C_{\rm x})$ is pumped into $C_{\rm int}$. Also, this charge is removed by the integration of $\hat{I}_{\rm int}$. Since the entire charge of $C_{\rm x}$ is pumped into $C_{\rm int}$ at once, — in the case of a large $C_{\rm x}$ — this will cause the integrator to overload. However, in the circuit in Fig. 1, negative feedback controls the charge transfer speed in such a way that the integrator output voltage always remains in between the two values $V_{\rm b1}$ and $V_{\rm b2}$. These values, which represent the input-bias voltages of the CMOS differential amplifiers, can easily be set by the designer. Fig. 3 shows the asymptotic values of the integrator output voltage $V_{\rm int}$ for the circuit in Fig. 1.

From t_0 to t_1 the circuit integrates the current $I_{\rm int}$, which removes the charge pumped by $C_{\rm o1}$. In this time interval, $C_{\rm x}$ is connected to $V_{\rm dd}$. At t_1, $C_{\rm x}$ is connected to node 2 of the selector and at the same time $C_{\rm o2}$ pumps its charge into $C_{\rm int}$. In the design, care has been taken to meet the condition $C_{\rm int}/C_{\rm o2} > V_{\rm DD}/(V_{\rm b1} - V_{\rm DD}/2)$. In this case, immediately after t_1, the voltage $V_{\rm int}$ is still less than $V_{\rm b1}$, and all bias current $I_{\rm b}$ of the differential amplifier goes to the left-hand branch so that $C_{\rm x}$ starts to be discharged by $I_{\rm b}$. Consequently, $C_{\rm int}$ is charged by $I_{\rm b} - I_{\rm int}$. At t_2, $V_{\rm int}$ equals $V_{\rm b1}$, at which point the negative feedback forces the integrator output voltage to remain constant, which occurs when the charge current through $C_{\rm int}$ is zero. In this case, the magnitude of the discharge current $I_{C\rm x}$ of $C_{\rm x}$ equals $I_{\rm int}$. At t_3, the discharging of $C_{\rm x}$ is almost completed and the drain-source voltage across $\rm M_6$ drops to almost zero. Then, the drain current of $\rm M_6$ also drops so that the charge current through $C_{\rm in}$ equals approximately $I_{\rm int}$.

It can be shown that the accuracy of the differential-amplifier bias current has no significant effect on the accuracy of the total time intervals representing the capacitive signals. When all four chopper phases are taken into account in the $+,-,-,+$ order [3], one complete chopper cycle (Fig. 2) equals

$$T_{\mathrm{msm}} = \frac{4V_{\mathrm{dd}}(C_{\mathrm{o1}} + C_{\mathrm{o2}} + C_{\mathrm{x}})}{I_{\mathrm{int}}}. \tag{1}$$

III. Conditions to be Met for Proper Operation

In order to guarantee stability of the negative-feedback loop, certain conditions should be met. For instance, if we assume that the parasitic capacitances of the sensor capacitance C_{x} (Fig. 1) are zero, then for a phase margin of 45°, it should hold that

$$\omega_{\mathrm{u}} \geq \frac{g_{\mathrm{m,D.A.}}}{C_{\mathrm{int}}} \tag{2}$$

where ω_{u} is the unity-gain bandwidth of the operational amplifier (Amp-1 in Fig. 1), and $g_{\mathrm{m,D.A.}} = I_{D6}/V_{\mathrm{int}}$ is the transconductance of feedback path via transistors M_1 to M_6. The same story is valid for the other side of the signal.

So far, the description of the negative feedback mechanism corresponds to that presented in [4]. However, in [4], both the details of the discharging C_{x} in the triode region of M_6 during the time interval $t_3 - t_4$ and the effect of any parasitic capacitance at the drive side of C_{x} have been overlooked. A good understanding of these details is of crucial importance for optimal interface design: Before C_{x} is completely discharged, transistor M_6 goes into the "triode region" and its current decreases, since it cannot follow the current through M_5. For example, Appendix A shows that during the time interval $t_3 - t_4$, C_{x} is discharged to a voltage $V_{\mathrm{ds(exp.)}}$, which is less than the so-called overdrive voltage V_{on} of M_6. For $m = I_{\mathrm{b}}/I_{\mathrm{int}} = 2$ it holds that $V_{\mathrm{ds(exp.)}} = 0.3V_{\mathrm{on}}$. In the triode region of M_6, the discharging process continues at an exponential pace. The condition for discharging C_{x} with a specified accuracy has been derived in Appendix A.

Until now, we have ignored the effects of the parasitic capacitances C_{p1} and C_{p2} of the sensor interconnects (Fig. 4). Since C_{p2} is connected to virtual ground, it does not play a first-order role. However, the parasitic capacitor C_{p1} consumes a portion of the available current needed to discharge C_{x}. As a consequence, the available current to discharge C_{x} is reduced to

$$I_{C_{\mathrm{x}},\mathrm{max}} = \frac{I_{\mathrm{b}}C_{\mathrm{x}}}{C_{\mathrm{x}} + C_{\mathrm{p1}}}. \tag{3}$$

In order to transfer the charge of the capacitor C_{x} with assured accuracy, the available current should be at least greater than I_{int}. For the earlier design presented in [4], where $m = I_{\mathrm{b}}/I_{\mathrm{int}} = 2$, with (3) this yields the condition

$$C_{\mathrm{p1}} \leq C_{\mathrm{x}}. \tag{4}$$

In most applications, this condition cannot be satisfied. However, by increasing the driving current we are able to extend the maximum tolerable value of C_{p1}. This can be done in various ways, for instance by increasing the differential-amplifier bias current, by increasing the aspect ratio of M_6 with respect to M_5, by adding a resistor in the source of M_5, or by any combination

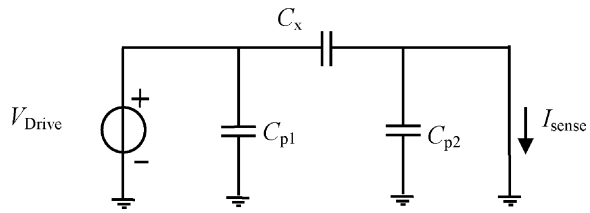

Fig. 4. Sensor capacitor with the interconnecting parasitic capacitance and the concept of the two-port measurement technique.

of these. However, the last two ways are more power-efficient, because then — only when necessary — the current has a larger value. Assuming that $I_{\mathrm{d,max}} = nI_{\mathrm{int}}$ for the maximum available driving current $I_{\mathrm{d,max}}$, the condition to be met for parasitic capacitor C_{p1} is

$$C_{\mathrm{p1}} \leq (n-1)C_{\mathrm{x}}. \tag{5}$$

For excessive values of the parameter n, the loop stability will decrease. For instance, when we need to measure a 1 pF capacitor in the presence of a 1 nF parasitic capacitor; then according to (5) it is necessary that $n \geq 1000$, which for practical reasons is too high. In our design, without increasing the amplifier bandwidth, the maximum value for n is about 40, which means that in the above-mentioned example, the maximum parasitic capacitance should be less than about 40 pF. This value can be increased at the cost of using more power by increasing the amplifier bandwidth. This example shows that care must be taken to avoid circuit malfunction. In many applications the condition of (5) can be met. In other cases, we have to use a conventional drive interface without negative feedback. In addition to (5), $(C_{\mathrm{x}} + C_{\mathrm{p1}})$ will have an upper-limit, which in our design is about 550 pF (Appendix A).

IV. Noise Performance of Interface With Negative Feedback

Based on the calculation in [7] it can be concluded that for small values of the parasitic capacitor C_{p2} (Fig. 4), the noise of the conventional interface (the interface of Fig. 1 without negative feedback) is dominated by the noise of the comparator. During each decision event, the noise voltage of the comparator causes variation in the period. The sensitivity for noise depends on the slope of the integrator output voltage V_{int} – the steeper the slope, the less the sensitivity of the period length for comparator noise. Based on this, we can derive the jitter of one measurement cycle caused by the comparator noise. The standard deviation of this jitter is

$$\sigma_{\mathrm{T_{msm}},u_{nc}} = 2\sqrt{2}\frac{u_{\mathrm{nc}}C_{\mathrm{int}}}{I_{\mathrm{int}}} \tag{6}$$

where u_{nc} is the equivalent input voltage noise of the comparator. To evaluate the effect of negative feedback on the noise performance of the interface, we assume for the conventional interface with $V_{\mathrm{dd}} = 5$ V that at the beginning of time interval T_1 [Fig. 5(a)], the voltage step in V_{int} is 0.5 V. Furthermore, we assume that at the beginning of time interval T_2, this step is 2 V for the maximum input capacitance $C_{\mathrm{x,max}}$. With these voltage steps, linearity and an acceptable dynamic range are guaranteed.

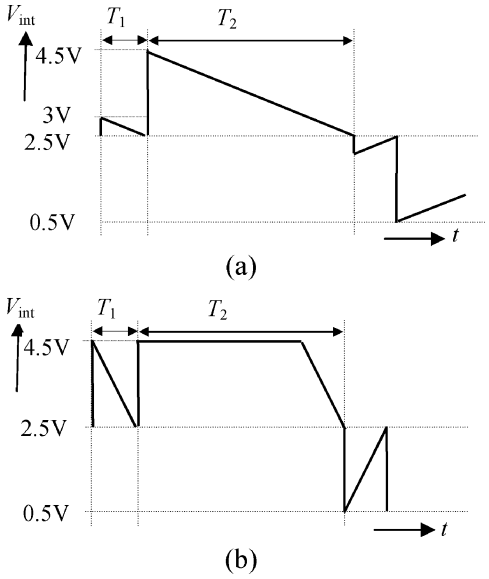

Fig. 5. Integrator output voltage: (a) without negative feedback and (b) with negative feedback when the integrator capacitor has been decreased by a factor of 4.

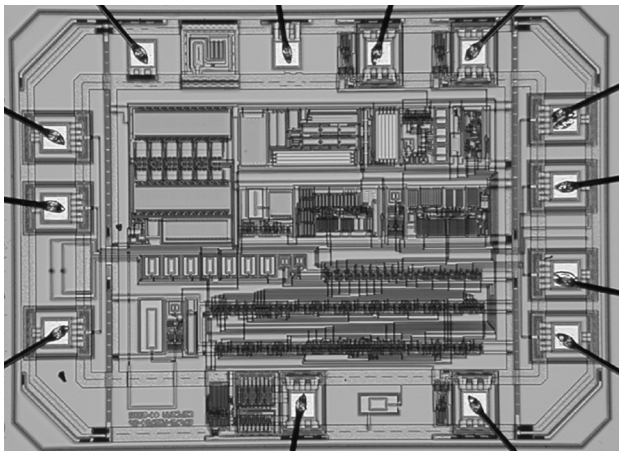

Fig. 6. Photograph of the chip, which measures 1.4 mm × 1.9 mm.

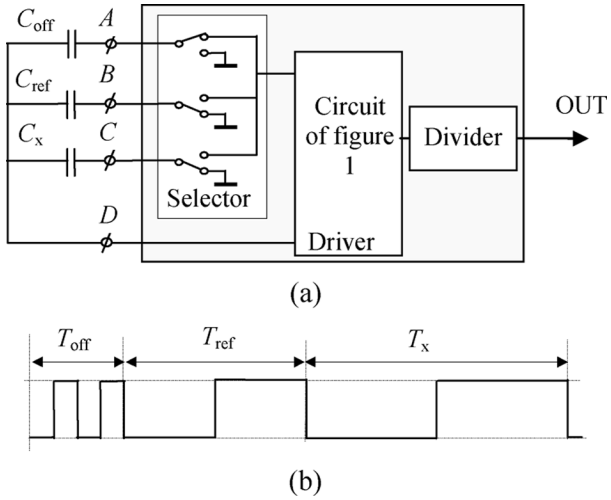

Fig. 7. (a) Block diagram of the interface system and (b) its output signal.

In the interface of Fig. 1, thanks to the negative feedback, we are able to decrease the integrator capacitor by a factor of 4, which results in the step of 2 V on $V_{\rm int}$, during both T_1 and T_2 [Fig. 5(b)]. With this simple change we are able to decrease the noise contribution of the comparator by a factor of 4. To enable the voltage swing mentioned above, it is essential that $V_{\rm b1} \geq 4.5$ V and $V_{\rm b2} \leq 0.5$ V. The accuracy of these voltages does not affect the accuracy of the interface, and the only restriction for them is that their values are within the output-swing range of the integrator amplifier. Therefore, implementation of these voltages is simple. Fig. 5(b) shows the integrator output voltage $V_{\rm int}$ for $V_{\rm b1} = 4.5$ V and $V_{\rm b2} = 0.5$ V.

V. Implementation and Measurement Results

The modified interface has been designed and implemented in 0.7 μm standard CMOS technology (Fig. 6). The supply voltage is 5 V and the measured value for the supply current is about 1.4 mA. The three-signal auto-calibration removes the main part of the effects of channel-charge injection and clock feedthrough of the chopper switches. Yet, our simulation results showed some residual switch effects. Therefore, to reduce these effects, the relevant switch sizes have been optimized. Because of the use of the three-signal auto-calibration technique [3], [5], one measurement cycle consists of three phases: one to measure the offset capacitor $C_{\rm off}$, one for the reference capacitor $C_{\rm ref}$, and a third one for the sensor capacitor $C_{\rm x}$. For identification purposes, time interval $T_{\rm off}$ is split into two short periods [3]. The data is read via a serial port (RS232) and analyzed using a Labview program.

In each measurement phase, the selected capacitor is first driven by a current and afterwards by a voltage. The non-selected capacitors are connected to ground. This is necessary to keep the systematic error at a minimum. Fig. 7(a) shows an overview of the interface system with its external capacitors. We measured the different periods of the output signal [Fig. 7(b)] with a microcontroller. The microcontroller has an internal counter with a sampling frequency of 5 MHz, which can measure each period by measuring concatenated rises in the interface output signal. When necessary, the user of the interface can reduce the quantization noise by using a microcontroller with a faster counter. In this way, the level of quantization noise can be decreased to less than that of thermal and shot noise.

In order to verify the results of the analysis of Section IV and to demonstrate the effect of negative feedback for the noise, the chip design includes the option of decreasing $C_{\rm int}$ by a factor of 4 by laser-cutting of a part of it. Capacitors $C_{\rm o1}$ and $C_{\rm o2}$ are equal and their values are selected in such a way that before laser-cutting, the step in the integrator output voltage is 0.5 V, as mentioned in Section IV. Next, after decreasing $C_{\rm int}$, this step is 2 V. Fig. 8 shows the measurement results for the measurement time of 100 ms before and after laser-cutting. It can be concluded that increasing the slope of the integrator output voltage by a factor of 4 results in 2.8 times less noise. If the noise had been caused by comparator noise only, the improvement would have been 4 times. Most probably the difference is due to the noise of the integrator amplifier (Amp-1). The achieved noise

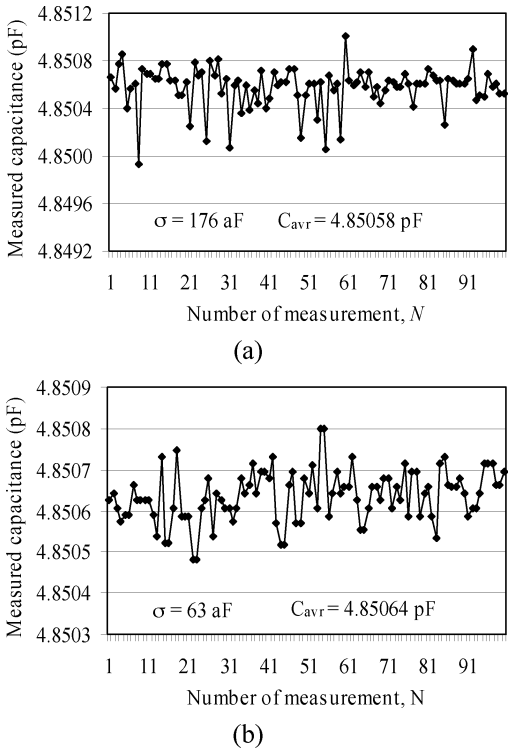

Fig. 8. Measurement results for $C_{\rm x}$ with a nominal value of 4.7 pF and a measurement time of 100 ms: (a) for an integrator capacitor $C_{\rm int} = 10$ pF, (b) for $C_{\rm int} = 2.5$ pF.

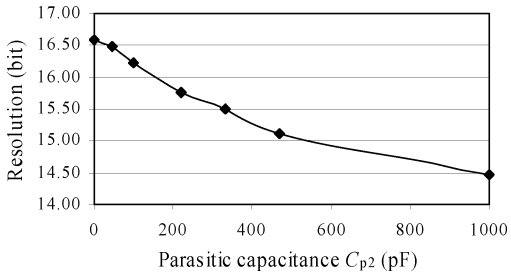

Fig. 9. Effect of parasitic capacitor, $C_{\rm p2}$ on the resolution for $C_{\rm ref} = 15$ pF, $C_{\rm x} = 10$ pF and measurement time of 100 ms.

level corresponds to a resolution of 16.2 bits, which is more than one bit better than the resolution reported in [3] for the UTI.

Fig. 9 shows the effect of the cable parasitic capacitor $C_{\rm p2}$ on the noise performance of the interface. In addition to a decrease in resolution, capacitor $C_{\rm p2}$ also causes a systematic error, which is shown in Fig. 10. As it can be seen, for a parasitic capacitance up to 470 pF, this error is less than 0.1%. However, for $C_{\rm p2} = 1$ nF, this error increases to 0.5%.

As discussed in Section III, the effect of the parasitic capacitor $C_{\rm p1}$ (Fig. 4) depends heavily on the value of capacitor $C_{\rm x}$. Care should be taken that condition (5) is met (in our design $n \cong 40$). In our measurement, we found that for $C_{\rm x} = 10$ pF, a parasitic capacitor –$C_{\rm p1}$– up to 330 pF does not cause a significant error. However, the performance of the interface is seriously degraded for a parasitic capacitance with a value higher than required, according to (5). For instance, for $C_{\rm p1} = 470$ pF, the measured result for $C_{\rm x}$ is about 5 pF instead of 10 pF, which is in agreement with the calculation presented in the Appendix A.

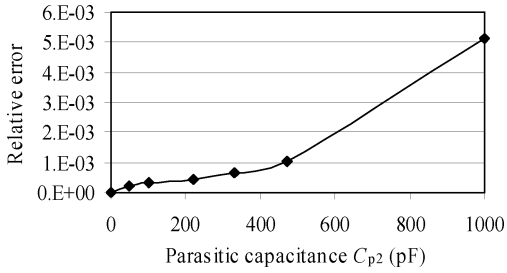

Fig. 10. Measured systematic error caused by the parasitic capacitor $C_{\rm p2}$ for $C_{\rm ref} = 15$ pF and $C_{\rm x} = 10$ pF.

The measurement of the nonlinearity is carried out carefully. In a straightforward way, one could expect that it would be possible to first measure the value of three or more reference capacitors with a (very) precise impedance analyzer and afterwards insert these reference capacitors one by one into the test set-up for testing the interface nonlinearity. In practice, this method does not work well. In the first place, the nonlinearity of the interface circuit is that small, that it is difficult to find impedance analyzers with sufficient accuracy. Moreover, when moving the reference capacitors to another position, the magnitude of the parasitic capacitances changes as well. Yet, it makes sense to measure the small linearity, because in precision application for sensor signals with a low-bandwidth, the accuracy is mainly limited by the nonlinearity. To solve this problem, in [3] a method is presented in which the nonlinearity is derived from the measurement of three stable capacitors: $C_{\rm ref1}$, $C_{\rm ref2}$ and $C_{\rm ref1} + C_{\rm ref2}$.

Then the nonlinearity is found using the equation [3]

$$\lambda = \frac{T_{C_{\rm ref1}+C_{\rm ref2}} - T_{\rm off}}{T_{C_{\rm ref1}} + T_{{\rm T}_{C_{\rm ref2}}} - 2T_{\rm off}} - 1 \tag{7}$$

where $T_{\rm Cref1}$, $T_{\rm Cref2}$, $T_{\rm Cref1+Cref2}$ and $T_{\rm off}$ are the output periods corresponding to $C_{\rm ref1}$, $C_{\rm ref2}$, $C_{\rm ref1} + C_{\rm ref2}$, and 0 pF capacitors, respectively. Assuming a linear relation of the period to the capacitance ($T_{\rm i} = AC_{\rm i} + B$), λ in (7) equals zero. However, in Appendix B it is shown that the accuracy of this method is limited by the presence of PCB parasitic capacitances. It is shown that when there is a parasitic offset capacitance which shunts the capacitor under test (CUT) and which does not depend on the presence of the DUT, this will affect the measurement.

To solve this problem, we modified the method for this work to be less sensitive for the effect of parasitic capacitances with the help of an external multiplexer. For this purpose, instead of three capacitors $C_{\rm ref1}$, $C_{\rm ref2}$ and $C_{\rm ref1} + C_{\rm ref2}$, we used four capacitors: $C_{\rm ref1}$, $C_{\rm ref2}$, $C_{\rm ref1} + C_{\rm ref3}$, and $C_{\rm ref2} + C_{\rm ref3}$, respectively. The nonlinearity λ has been calculated according to the equation

$$\lambda = \frac{T_{C_{\rm ref2}+C_{\rm ref3}} - T_{C_{\rm ref1}+C_{\rm ref3}}}{T_{C_{\rm ref2}} - T_{{\rm T}_{C_{\rm ref1}}}} - 1. \tag{8}$$

The setup should be arranged in such a way that no parasitic capacitance (parasitic capacitances of PCB) are changed during the measurement. This means that not only the wiring of the

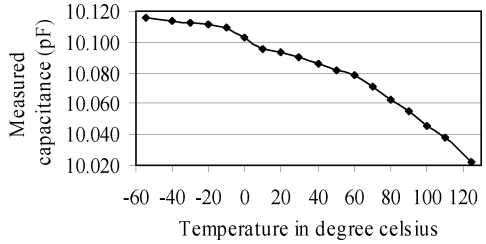

Fig. 11. Measurement results for a capacitance with nominal value of 10 pF at different temperatures.

setup, but also the position of any conductors should be invariable [8]. As shown in Appendix B, it can be proven that the presence of PCB parasitic capacitances cannot affect the linearity measurement based on (8); however, the presence of these parasitics can still spoil the absolute accuracy of our capacitance measurement. As explained in Appendix B, the solution consists of a) minimizing these parasitics by careful design, and b) making a symmetrical design, so that compensation of the effect is achieved. Moreover, using an additional calibration procedure at a system level further compensation can be achieved.

In our nonlinearity tests, we selected different combinations of $C_{\rm ref1}, C_{\rm ref2}$ and $C_{\rm ref3}$ in such a way that $C_{\rm ref1}, C_{\rm ref2}, C_{\rm ref1}+C_{\rm ref3}$, and $C_{\rm ref2}+C_{\rm ref3}$ always stayed in the range of 1 pF to 300 pF. Our experimental results show that the nonlinearity is less than 50×10^{-6} over the full range, which is five times better than that reported in [3]. Note, that because the dynamic range of the interface presented in this paper is much wider than that of the one presented in [3], a straightforward comparison of the mutual results of the different interfaces is not possible and should be evaluated using practical setups.

In addition, we measured the effect of the interface temperature on the overall measurement results. During this experiment, we kept $C_{\rm x}$ at a constant temperature. Fig. 11 shows the measured capacitor at different interface temperatures, where $C_{\rm ref}=15$ pF and $C_{\rm x}=10$ pF (nominal values), both of which are of the type NP0. The offset capacitor $C_{\rm off}$ should be 0 pF. The effect of temperature changes on the interface circuit corresponds to a capacitance change of $C_{\rm x}$ of about 80×10^{-6}, which is in the same range as the temperature coefficient of NP0 type capacitors. Therefore, it can be concluded that the measured temperature effects are mainly due to that of the reference capacitor, where the temperature varies together with the rest of the interface circuit.

VI. Conclusion

An integrated interface circuit for capacitive sensors with a wide dynamic range has been designed and presented. Negative feedback controls the discharging process of the switched capacitor at the input. In this way, overload of the applied integrator is prevented. However, to function properly, a condition for the parasitic capacitance of one of the sensor electrodes to ground must be met. It has been shown how the circuit has to be arranged to meet this condition. In addition, it has been shown that the unavoidable PCB Parasitic capacitances can cause an error in the conventional nonlinearity measurement. It has also been shown that this error can be avoided by a novel method of nonlinearity measurement. The circuit has been implemented in 0.7 μm standard CMOS technology. Measurement results show a resolution of more than 16 bits for a measurement time of about 100 ms. The nonlinearity has been found to be about 50×10^{-6} (14 bits) for the range of 1 pF to 300 pF.

Appendix A
Detailed Analysis of Charge Transfer Process

In this Appendix we will derive the voltage $V_{\rm ds(exp.)}$ of the MOSFET $\rm M_6$ at which point $C_{\rm x}$ starts to discharge exponentially. Also, we will derive the conditions that should be met in order to discharge the $C_{\rm x}$ with the required accuracy.

Let us first assume that $I_{\rm b}=mI_{\rm int}$ and $C_{\rm p1}=0$ pF. During time interval t_2 to t_3 (Fig. 3), $C_{\rm x}$ can easily be discharged to $V_{\rm on}$ by the current $I_{\rm int}$. After that, $\rm M_6$ goes to the triode region and its drain current decreases. As long as $I_{\rm d6}$ is greater than $I_{\rm d5}/{\rm m}$, the negative feedback forces the sensor discharge-current to be $I_{\rm int}$. However, after that, $C_{\rm x}$ is discharged exponentially. The drain-source voltage of $\rm M_6$ which causes this to happen can easily be derived from the equation [9]

$$\frac{\mu C_{\rm ox}W}{L}\left((V_{\rm gs}-V_{\rm T})V_{\rm ds(exp.)}-\frac{V_{\rm ds(exp.)}^2}{2}\right)=\frac{1}{m}\frac{\mu C_{\rm ox}W}{2L}(V_{\rm gs}-V_{\rm T})^2 \quad \text{(A1)}$$

where μ is the majority-carrier mobility in the channel, $C_{\rm ox}$ is the oxide capacitance for the active area, and W and L are the width and length of transistor $\rm M_6$, respectively. The result is

$$V_{\rm ds(exp.)}=\left(1-\sqrt{\left(1-\frac{1}{m}\right)}\right)V_{\rm on} \quad \text{(A2)}$$

where $V_{\rm on}=(V_{\rm gs}-V_{\rm T})$ is the so-called overdrive voltage of $\rm M_6$ for $I_{D6}=mI_{\rm int}$. For $m=2$, this results in:

$$V_{\rm ds(exp.)}=0.3V_{\rm on}. \quad \text{(A3)}$$

To find the condition that should be met in order to discharge the $C_{\rm x}$ with the required accuracy, we assume that $V_{\rm dd}=5$ V and $V_{\rm on}=0.33$ V. Moreover, we assume that $C_{\rm x}$ discharges with an accuracy of 15 bits, which corresponds to 1.5×10^{-4} V. From t_1 to t_3 (Fig. 3), $C_{\rm x}$ is discharged from 5 V to 0.1 V. Then from t_3 to t_4 it should be discharged to 1.5×10^{-4} V. To achieve this, the condition that should be met is

$$\frac{\left(V_{\rm b}-\frac{V_{\rm dd}}{2}\right)C_{\rm int}+0.3C_{\rm x}V_{\rm on}}{\widehat{I}_{\rm int}}\geq 6.5R_{\rm ds}C_{\rm x}. \quad \text{(A4)}$$

The left-hand side of this equation represents the time available to discharge the capacitor $C_{\rm x}$, which is the time interval of t_3 to t_4 in Fig. 3. The right-hand side represents the time needed to discharge the capacitor $C_{\rm x}$ from 0.1 V to 1.5×10^{-4} V.

So far it has been assumed that $C_{\rm p1}=0$ pF. If we assume that $C_{\rm p1}\neq0$ pF, and the maximal drain current of $I_{\rm d6,max}=nI_{\rm int}$ (Fig. 1), and if we take into account the current loss via the

parasitic capacitance $C_{\rm p1}$, we find for the maximum available current $I_{\rm Cx,max}$ for discharging $C_{\rm x}$ that

$$I_{C_{\rm x},\max} = \frac{nI_{\rm int}C_{\rm x}}{C_{\rm x}+C_{\rm p1}}. \tag{A5}$$

In this case, $V_{\rm ds(exp.)}$ can easily be found from (A2) by substituting $m = nC_{\rm x}/(C_{\rm x}+C_{\rm p1})$. For instance, for $C_{\rm x}/(C_{\rm x}+C_{\rm p1}) = 1/10$ and $n = 40$, we find that $V_{\rm ds(exp.)} = 0.13V_{\rm on}$. Note that $V_{\rm on}$ is the overdrive voltage of $\rm M_6$ for $I_{\rm d6} = 4I_{\rm int}$. The condition that should be met in order to discharge the $C_{\rm x}$ with the required accuracy can be calculated in a similar way as shown in (A4). For the same accuracy of 15 bits and the same $V_{\rm on}$, this yields

$$\frac{\left(V_{\rm b1}-\frac{V_{\rm dd}}{2}\right)C_{\rm int}+0.13C_{\rm x}V_{\rm on}}{\widehat{I}_{\rm int}} \geq 5.6R_{\rm ds}(C_{\rm x}+C_{\rm p1}). \tag{A6}$$

A comparison of conditions (A6) and (A4) shows that for a large parasitic capacitance $C_{\rm p1}$, we need a much smaller $R_{\rm ds}$ to achieve the same level of accuracy. For instance in our design, where $V_{\rm b1} = 4.5$ V, $V_{\rm DD} = 5$ V, $C_{\rm int} = 2.5$ pF, $V_{\rm on} \approx 0.3$ V and $R_{\rm ds} = 2.5$ kΩ, it holds that

$$(C_{\rm x}+C_{\rm p1}) \leq 550 \text{ pF}. \tag{A7}$$

Appendix B
Effect of PCB Parasitic Capacitances

In this Appendix we will explain how the PCB parasitic capacitances can affect our measurement and how their effect can be minimized.

Ideally, if there is no parasitic capacitance, we will have

$$T_{\rm off} = AC_{\rm off}+B \tag{B1}$$

$$T_{\rm ref} = AC_{\rm ref}+B \tag{B2}$$

$$T_{\rm x} = AC_{\rm x}+B \tag{B3}$$

where $T_{\rm off}$, $T_{\rm ref}$ and $T_{\rm x}$ represent the period times shown in Fig. 7(b). Then for $C_{\rm off} = 0$ pF, it holds that

$$M = \frac{T_{\rm x}-T_{\rm off}}{T_{\rm ref}-T_{\rm off}} = \frac{C_{\rm x}}{C_{\rm ref}}. \tag{B4}$$

Therefore, by measuring M and knowing the reference capacitance, $C_{\rm ref}$, the input capacitance, $C_{\rm x}$ can be calculated.

In reality there are parasitic capacitances between any pairs of conductors [8]. Fig. 12 shows these parasitic capacitances for the interface of Fig. 7(a), where $C_{\rm p-x}$, $C_{\rm p-off}$ and $C_{\rm p-ref}$ are parasitic capacitances from the excitation terminals to the sense terminal. With the existence of these parasitic capacitances, (B4) can be rewritten as

$$M = \frac{T_{\rm x}-T_{\rm off}}{T_{\rm ref}-T_{\rm off}} = \frac{C_{\rm x}+(C_{\rm p-x}-C_{\rm p-off})}{C_{\rm ref}+(C_{\rm p-ref}-C_{\rm p-off})}. \tag{B5}$$

In our case, these capacitances are in the range of tens of femtofarads. Thus, for small values of $C_{\rm x}$, the effect of the parasitic capacitances can easily spoil the accuracy. The best solution to this problem is to minimize the parasitic capacitances by maximizing the distance of pin D respective to pins A, B, and C and even to the related conductor at chip level. Since the excitation terminals, A, B, and C, are always connected to a low-impedance DC or AC voltage source, the parasitic capacitance amongst the terminals does not affect the measurement result.

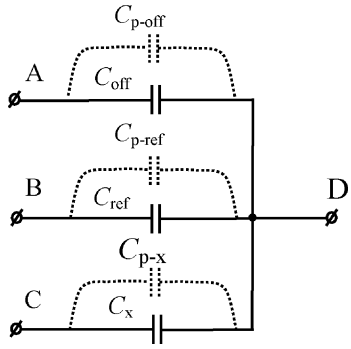

Fig. 12. Parasitic capacitance between different pins in the interface.

From (B5) it can be concluded that only the differential parasitic capacitances, $(C_{\rm p\text{-}x}-C_{\rm p\text{-}off})$ and $(C_{\rm p-ref}-C_{\rm p-off})$, affect the measurement result M. Therefore, a symmetrical design of the terminal (pin) configuration at both chip level and PCB level will considerably decrease the influence of these parasitic capacitors.

By using initial calibration of offset capacitors and assuring proper physical conditions, a higher accuracy can be obtained with two additional measurements: First we measure $T_{\rm off-0}$, $T_{\rm ref-0}$ and $T_{\rm x-0}$, which correspond to the zero capacitances for all three input capacitances, $C_{\rm off}$, $C_{\rm ref}$ and $C_{\rm x}$. Next we measure $T_{\rm x-C1}$ by applying a well-known, non-zero capacitor as $C_{\rm x}$ $(C_{\rm x} = C_1)$. The gain factor of capacitance to period converter, A, and differential parasitic capacitances can be calculated as

$$A = \frac{T_{{\rm x},C_1}-T_{\rm x,0}}{C_1} \tag{B6}$$

$$(C_{\rm p-ref}-C_{\rm p-off}) = \frac{T_{\rm ref,0}-T_{\rm off,0}}{A} \tag{B7}$$

$$(C_{\rm p-x}-C_{\rm p-off}) = \frac{T_{\rm x,0}-T_{\rm off,0}}{A}. \tag{B8}$$

Therefore by combining equations (B5) to (B8), $C_{\rm x}$ can be extracted.

These parasitic capacitances can also affect the nonlinearity measurement. Including the PCB parasitic capacitances, and yet assuming a linear relation of the period to the capacitance, λ in (7) results in:

$$\lambda = \frac{C_{\rm x}+C_{\rm ref}+C_{\rm p-x}+C_{\rm p-ref}-C_{\rm p-off}}{C_{\rm x}+C_{\rm ref}+C_{\rm p-x}+C_{\rm p-ref}-2C_{\rm p-off}}-1. \tag{B9}$$

As it can be seen, assuming that the system is linear, the nonlinearity λ as calculated in (7) will not result in zero. For instance, for $C_{\rm x} = C_{\rm ref} = 10$ pF and a fully symmetrical design, $C_{\rm p-x} = C_{\rm p-ref} = C_{\rm p-off} = 10$ fF, the nonlinearity λ amounts to 5×10^{-3}. In the same way it can be proven that the nonlinearity λ as calculated in (8) is independent of these parasitics.

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