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Piezoelectric Energy Harvesting Interface Using Self-Bias-Flip Rectifier and Switched-PEH DC–DC for MPPT

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***Abstract*— This article proposes a novel eight-phase self-bias-flip piezoelectric energy harvesting interface with charge recycling and reusing (SBFRR) and a switched-piezoelectric energy harvester (PEH) dc–dc (SPDC) converter. The proposed scheme innovatively utilizes the inherent capacitors (C_P) of four PEHs as energy sources, flying capacitors, and flipping capacitors for time-sharing reuse to achieve both a high-voltage flipping and dc–dc conversion efficiency, while avoiding the use of extra energy reservoirs. The design is fully integrated and fabricated in standard 0.18-μm CMOS. Measurement result demonstrates that the voltage flipping efficiency of up to 80% is achieved. Compared with the ideal full-bridge rectifier (FBR), the measured maximum output power improving rate (MOPIR) can be increased to 4.88×. In addition, with the four C_P serving as flying capacitors to achieve SPDC conversion for maximum power point track (MPPT), an MOPIR of >3.5× can be maintained with a PEH input voltage from 0.78 to 4.9 V.**

***Index Terms*— Energy harvesting, flipping efficiency, fully integrated, maximum output power improving rate (MOPIR), maximum power point track (MPPT), multi-input, piezoelectric, self-bias-flip, switched-piezoelectric energy harvester (PEH) dc–dc (SPDC).**

I. Introduction

WIRELESS sensor network raises the challenge of employing multiple sensor nodes for facilitating human life. The energy harvesting technique is a promising technique that attracts widespread attention. Energy sources including piezoelectric [1], [2], [3], [4], [5], thermoelectric [6], [7], [8], solar [9], [10], [11] and radio frequency (RF) [12], [13], and piezoelectric energy harvesting have been reported. Among them, piezoelectric energy harvesting is popular for the advantage of high power density and simple structure. Commonly, a piezoelectric energy harvester (PEH) adopts a cantilever structure by attaching the piezoelectric materials (such as PZT) to a cantilever beam. During vibration, a PEH transfers the mechanical power into electricity through the piezoelectric effect. When motivated by a sinusoidal force at the resonant frequency as shown in Fig. 1, a PEH can be equivalent to an ac current source in parallel with an inherent capacitor (C_P) and a resistor. The ac current source can be defined as $i_P = I_P \sin\omega_P t$, where the peak value I_P is related to the level of vibration. Here, $\omega_P = 2\pi f_P$, with f_P denoting the vibration frequency. The value of C_P is relevant to the PEH's area and can be in the order of tens of nF. To convert the ac voltage of PEH into the required dc voltage, a rectifier is necessary for ac–dc conversion. Although a full-bridge rectifier (FBR) has a simple structure with well-defined operation, it can lead to energy loss due to the periodic charging and discharging of C_P.

To increase the efficiency, the existing synchronous switch harvesting on inductor/capacitor (SSHI/C) techniques [14], [15], [16], [17], [18], [19] target to flip the charge on C_P when I_P crosses zero, as shown in Fig. 1. SSHI constructs an LC loop by an inductor and C_P to realize bias-flip at zero-crossing (ZC) of I_P. For higher flipping efficiency, a high Q inductor is necessary. Thus, the value of the inductor is usually in the range of μH–mH, inevitably occupying a large volume. Different from SSHI, SSHC flips the charge on C_P based on charge-sharing. In SSHC, large flipping capacitors with multiphase bias-flip operation are adopted to improve the voltage flipping efficiency. As both SSHI and SSHC require large passive elements, they cannot be employed in applications with strict volume constraints.

In [20], it is illustrated that multi-input piezoelectric energy harvesting is a potential trend that can significantly reduce the size of flipping capacitors or inductors. The proposed SE-SSHC technique can achieve a fully integrated design by separating PEH electrodes. However, this solution still requires ON-chip capacitors to achieve voltage flipping, resulting in a large chip area. In addition, the series PEH connection can reduce the system efficiency due to the use of excessive HV devices. In [21], [22], and [23], the use of shared inductors

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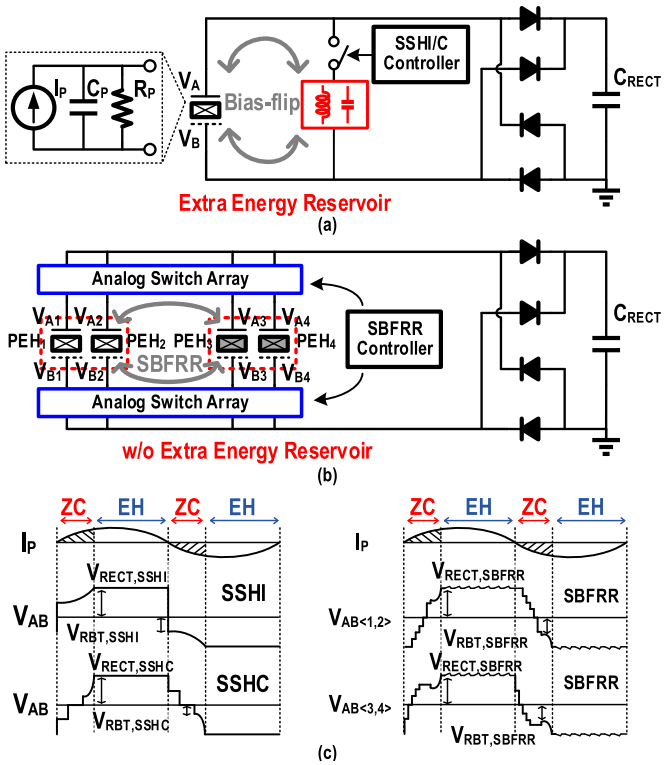

Fig. 1. Bias-flip technique: (a) SSHI/C. (b) Proposed SBFRR. (c) Corresponding current and voltage waveforms.

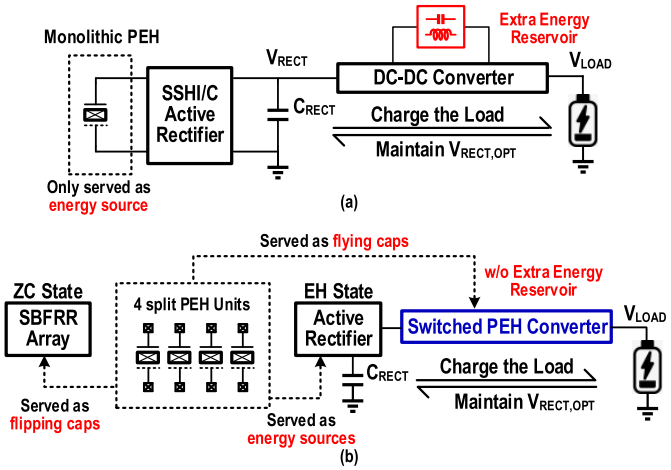

Fig. 2. (a) Conventional PEH interface based on the dc–dc converter. (b) Proposed PEH interface based on the SPDC technique.

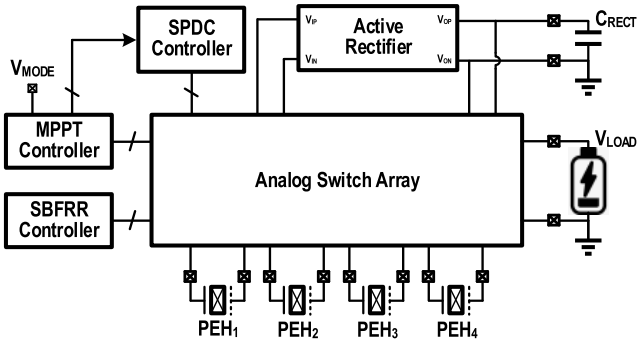

Fig. 3. Overview of the proposed interface system.

or reconfigurable PEH arrays in multi-input PEH circuits is studied, but large passive components are still inevitable. As shown in Fig. 1(b), this design innovatively uses the inherent C_P of piezoelectric harvesters as flipping capacitors. A total of four PEHs are employed to tradeoff between the number of flipping phases and circuit complexity. During the ZC state, the charge of $\text{PEH}_{<3,4>}$ are cleared to serve as flipping capacitors to flip $\text{PEH}_{<1,2>}$. Except for basic bias-flip phases, charge recycle and charge reuse phases are also added to improve the voltage-flipping efficiency. The proposed voltage flipping technique is named self-bias-flip with charge recycle and reuse (SBFRR) and will be introduced in detail later.

To achieve a high ac–dc conversion efficiency, the rectifier output voltage (V_{RECT}) must be adjusted to the optimal value $V_{\text{RECT,OPT}}$. However, $V_{\text{RECT,OPT}}$ is usually not equal to the required load voltage (V_{LOAD}). Thus, a complete interface system should include a maximum power point track (MPPT) module to maintain V_{RECT} at $V_{\text{RECT,OPT}}$ and further convert $V_{\text{RECT,OPT}}$ to the V_{LOAD}. Conventional PEH interfaces realize MPPT by configuring the voltage conversion ratio (VCR) of an inductive or capacitive dc–dc converter as shown in Fig. 2(a). To avoid using extra passives as in conventional dc–dc converters, we propose a switched PEH dc–dc converter (SPDC), which is composed of a four-PEH input array and C_{RECT} as shown in Fig. 2(b). The PEH array can be implemented by splitting one monolithic PEH into four elements, each with independent positive and negative electrodes, thus not occupying additional volume. Particularly, the four PEHs alternately serve as energy sources and flying capacitors as part of SPDC, and the VCR of the SPDC is set according to the vibration level.

The rest of the article is organized as follows. Section II aims to introduce the proposed SBFRR and SPDC and conducts the theoretical analysis with simulation verification. Section III introduces the circuit implementation. Section IV carries out the test verification of the proposed piezoelectric energy harvesting interface. Finally, Section V draws the conclusion.

II. Proposed SBFRR and SPDC Technique

Based on the proposed SBFRR and SPDC techniques, PEHs are alternately employed as energy sources, flying capacitors, and flipping capacitors for efficient energy extraction. The operation of the proposed interface is composed of three states: ZC, EH, and MPPT. During the ZC state, the interface flips the PEH voltage based on the proposed SBFRR technique. In the EH state, the harvested power is transferred to load by the proposed SPDC technique. In the MPPT state, the MPPT controller presets the configuration of the four PEHs according to the vibration level. Fig. 3 shows the proposed interface system. SBFRR and SPDC are realized by configuring the analog switch array through the MPPT controller as triggered by the external signal V_{MODE} to set the VCR. Thanks to the SBFRR and SPDC techniques, the proposed system achieves self-bias-flip and MPPT with a fully integrated design and is especially suitable for miniaturized applications.

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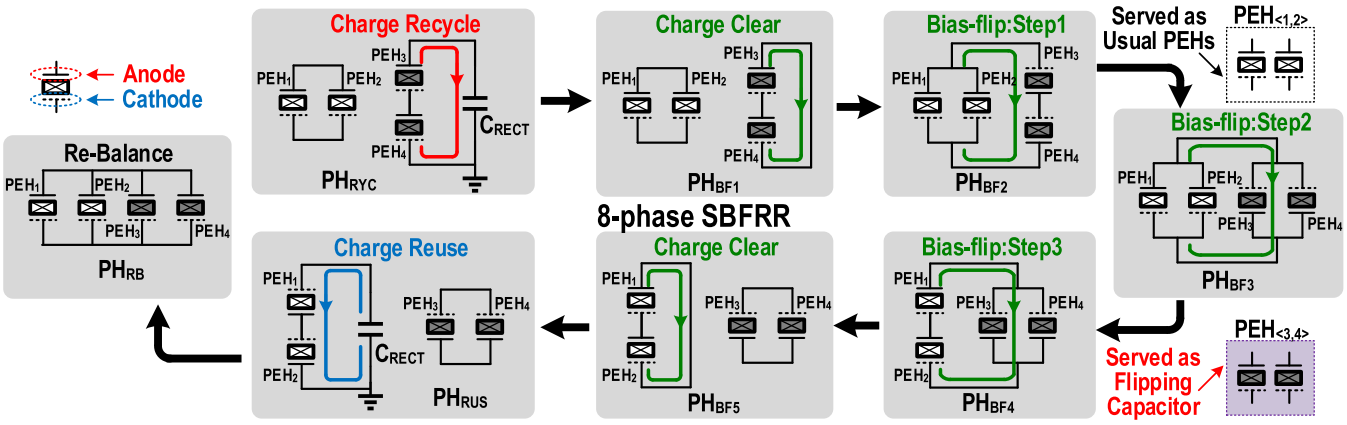

Fig. 4. Operation of the proposed SBFRR technique.

A. Proposed SBFRR Technique

Upon the zero crossing of I_P, the system enters the ZC state. The ZC state consists of the recycle phase ($\mathrm{PH_{RYC}}$), bias-flip phases ($\mathrm{PH_{BF<1,5>}}$), the reuse phase ($\mathrm{PH_{RUS}}$), and the rebalance phase ($\mathrm{PH_{RB}}$). The combinations of the four PEH inputs under each phase are shown in Fig. 4. For illustration, we assign $\mathrm{PEH_{<1,2>}}$ to serve as the conventional PEHs and configure $\mathrm{PEH_{<3,4>}}$ as flipping capacitors. Starting from $\mathrm{PH_{RYC}}$, $\mathrm{PEH_{<3,4>}}$ recycles half of the charge to C_{RECT}, followed by $\mathrm{PH_{BF1}}$ where the residual charge is completely discharged. The charge on $\mathrm{PEH_{<1,2>}}$ is gradually flipped in three steps from $\mathrm{PH_{BF2}}$ to $\mathrm{PH_{BF4}}$ to reduce the charge sharing loss and is finally cleared in $\mathrm{PH_{BF5}}$. To improve the energy extraction efficiency, the previously recovered charge at C_{RECT} is reinjected to $\mathrm{PEH_{<1,2>}}$ in $\mathrm{PH_{RUS}}$, and the PEH voltage is then equalized in $\mathrm{PH_{RB}}$. Finally, $\mathrm{PEH_{<1,4>}}$ are connected in parallel to attain the rebuilt voltage (V_{RBT}) in $\mathrm{PH_{RB}}$, where V_{RBT} is defined in (9), and the polarity of V_{RBT} is correlated with that of I_P. Thanks to the proposed SBFRR, the interface achieves a high efficiency without using any extra energy reservoir. The theoretical analysis and proof are as follows.

Assuming the inherent capacitors of $\mathrm{PEH_{<1,4>}}$ are $C_{P<1,4>}$ with $C_{P1} = C_{P2} = C_{P3} = C_{P4} = C_P$. Thus, the PEH open-circuit voltage V_P is

$$V_P = \frac{I_P}{\omega_P \cdot C_P}. \tag{1}$$

The charge generated by four PEH inputs ($Q_{0.5\mathrm{CY}}$) in half a cycle is

$$Q_{0.5CY} = 8 \cdot C_P \cdot V_P. \tag{2}$$

During $\mathrm{PH_{RYC}}$, $\mathrm{PEH_{<3,4>}}$ are configured in series to deliver power $P_{\mathrm{RECT,RYC}}$ to C_{RECT}

$$P_{\mathrm{RECT,RYC}} = C_P \cdot V_{\mathrm{RECT}}^2 \cdot f_P. \tag{3}$$

After the charge recycling is completed, the voltage across $\mathrm{PEH_{<1,2>}}$ and $\mathrm{PEH_{<3,4>}}$ are equal to

$$V_{\mathrm{PEH1,2}} = 2 \cdot V_{\mathrm{PEH3,4}} = V_{\mathrm{RECT}}. \tag{4}$$

Subsequently, $V_{\mathrm{PEH<3,4>}}$ are fully discharged during $\mathrm{PH_{BF1}}$. During $\mathrm{PH_{BF2}}$, $\mathrm{PEH_{<1,2>}}$ are in parallel, while $\mathrm{PEH_{<3,4>}}$ are in series. They are further connected in parallel to execute charge sharing, resulting in

$$V_{\mathrm{PEH1,2}} = 2 \cdot |V_{\mathrm{PEH3,4}}| = 0.8 \cdot V_{\mathrm{RECT}}. \tag{5}$$

Similarly, after $\mathrm{PH_{BF5}}$, we can have

$$V_{\mathrm{PEH1}} = V_{\mathrm{PEH2}} = 0 \tag{6a}$$

$$|V_{\mathrm{PEH3}}| = |V_{\mathrm{PEH4}}| = 0.72 \cdot V_{\mathrm{RECT}}. \tag{6b}$$

During $\mathrm{PH_{RUS}}$, $\mathrm{PEH_{<1,2>}}$ are series connected, and the recycle charge in $\mathrm{PH_{RYC}}$ is invested to $\mathrm{PEH_{<1,2>}}$. The reuse power P_{RUS} is

$$P_{\mathrm{RUS}} = C_P \cdot V_{\mathrm{RECT}}^2 \cdot f_P. \tag{7}$$

And the voltage across the $\mathrm{PEH_{<1,4>}}$ after $\mathrm{PH_{RUS}}$ are

$$V_{\mathrm{PEH1}} = V_{\mathrm{PEH2}} = 0.5 \cdot V_{\mathrm{RECT}} \tag{8a}$$

$$|V_{\mathrm{PEH3}}| = |V_{\mathrm{PEH4}}| = 0.72 \cdot V_{\mathrm{RECT}}. \tag{8b}$$

Finally, $\mathrm{PEH_{<1,4>}}$ are switched to parallel during $\mathrm{PH_{RB}}$, and the rebuilt voltage V_{RBT} is

$$|V_{\mathrm{RBT}}| = 0.61 \cdot V_{\mathrm{RECT}}. \tag{9}$$

The charge loss ($Q_{0.5\mathrm{LOST}}$) in SBFRR is

$$\begin{aligned} Q_{0.5\mathrm{LOST}} &= 4 \cdot C_P \cdot (V_{\mathrm{RECT}} - V_{\mathrm{RBT}}) \\ &= 1.56 \cdot C_P \cdot V_{\mathrm{RECT}}. \end{aligned} \tag{10}$$

The harvested power related to self-bias-flip $P_{\mathrm{RECT,SBF}}$ is

$$P_{\mathrm{RECT,SBF}} = (Q_{0.5CY} - Q_{0.5\mathrm{LOST}}) \cdot V_{\mathrm{RECT}} \cdot 2 f_P. \tag{11}$$

Thus, the output power of the rectifier P_{RECT} is

$$\begin{aligned} P_{\mathrm{RECT}} &= P_{\mathrm{RECT,SBF}} + P_{\mathrm{RECT,RYC}} - P_{\mathrm{RUS}} \\ &= [16 \cdot V_P - 3.12 \cdot V_{\mathrm{RECT}}] \cdot C_P \cdot V_{\mathrm{RECT}} \cdot f_P. \end{aligned} \tag{12}$$

By differentiating (12) with respect to V_{RECT} and equating the result to zero, the maximum output power can be attained when $V_{\mathrm{RECT}} = 2.564 \cdot V_P$

$$P_{\mathrm{RECT,MAX}} = 20.512 \cdot C_P \cdot V_P^2 \cdot f_P. \tag{13}$$

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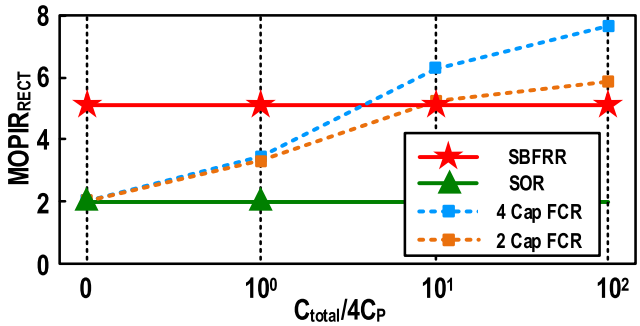

Fig. 5. Comparison on the $\mathrm{MOPIR_{RECT}}$ of FCR and the proposed SBFRR.

If $\mathrm{PEH}_{<1,4>}$ is followed by an ideal FBR, the harvested power attains the maximum value $P_{\mathrm{FBR,MAX}}$ when $V_{\mathrm{RECT}} = V_P/2$ [2]

$$P_{\mathrm{FBR,MAX}} = 4 \cdot C_P \cdot V_P^2 \cdot f_P. \tag{14}$$

The maximum output power improving rate (MOPIR) can be calculated as

$$\mathrm{MOPIR_{RECT}} = \frac{P_{\mathrm{RECT,MAX}}}{P_{\mathrm{FBR,MAX}}} = 5.128. \tag{15}$$

According to (15), the proposed SBFRR can reach a $\mathrm{MOPIR_{RECT}}$ of 5.128× without the aid of extra passive elements. Particularly, the introduction of $\mathrm{PH_{RYC}}$ and $\mathrm{PH_{RUS}}$ contributes to the significant improvement of $\mathrm{MOPIR_{RECT}}$. Otherwise, the theoretical value of $\mathrm{MOPIR_{RECT}}$ will decrease to 3.12×.

The proposed SBFRR can be expanded to a larger input array. When applying SBFRR to the eight-PEH input array, the $\mathrm{MOPIR_{RECT}}$ will increase to 7.04. Although increasing the array scale can improve the $\mathrm{MOPIR_{RECT}}$, the switch array complexity and switching loss will also increase significantly. To balance energy extraction efficiency, area overhead, and design complexity, a four-PEH input array is adopted to realize the SBFRR. Fig. 5 compares theoretical $\mathrm{MOPIR_{RECT}}$ of the switch only rectifier (SOR) [2], capacitive bias-flip technique FCR [18], and the proposed SBFRR. The line labeled "4 cap FCR/2 cap FCR" represents the total $\mathrm{MOPIR_{RECT}}$ obtained by extracting power from four independent PEHs through the FCR circuit using 4/2 additional capacitors. It can be observed that the proposed SBFRR achieves the $\mathrm{MOPIR_{RECT}}$ of 5.128 without any extra capacitor C_{total}. FCR has a much worse energy improvement effect than SBFRR when the number of capacitors and the total capacitance value are small. Although the FCR can attain the $\mathrm{MOPIR_{RECT}}$ of about 5.21 (using two capacitors) and 6.3 (using four capacitors), it will occupy much more volume due to the cost of large C_{total} ($C_{\mathrm{total}}/4C_P = 10$).

B. Proposed SPDC Technique

Fig. 6 presents the operation of the proposed SPDC at the EH state, where the four PEHs serve as flying capacitors for dc–dc conversion to extend the input power range. It is composed of three phases ($\mathrm{PH_{EH0}}$–$\mathrm{PH_{EH2}}$). During $\mathrm{PH_{EH0}}$, the four PEHs serve as energy sources and transfer charges to C_{RECT} through the active rectifier (AR), which is also responsible for ZC detection and I_P polarity determination. During $\mathrm{PH_{EH1}}$ and $\mathrm{PH_{EH2}}$, the four PEHs are used as flying capacitors and are periodically switched among series and parallel connections. During $\mathrm{PH_{EH1}}$, the PEH array and C_{RECT} together form an SPDC to deliver charge to the load, with a total of four possible VCRs through SPDC reconfiguration. Fig. 6 presents the configurations of the four PEHs at different VCRs, which are preset according to the vibration level in the MPPT state. To prevent error during ZC detection at $\mathrm{PH_{EH0}}$, the voltages on $\mathrm{PEH}_{<1,4>}$ and C_{RECT} are rebalanced in $\mathrm{PH_{EH2}}$. This can also prevent the PEH from deviating from the MPP. The proposed system typically transits between the ZC and EH states as shown in Fig. 7. Upon the triggering of the external signal V_{MODE}, the system will temporarily switch to the MPPT state, and the combination of $\mathrm{PEH}_{<1,4>}$ is configured according to the current phase. The ZC detection occurs at $\mathrm{PH_{EH0}}$. If I_P has crossed zero, the system will switch to the ZC state. Otherwise, it keeps in the EH state.

C. Simulation Results of SBFRR and SPDC Techniques

Fig. 8 shows the simulated waveform of the proposed SBFRR and SPDC techniques. The waveform of $V_{\mathrm{PEH}<1,4>}$ in the EH state and the ZC state is shown in Fig. 8(a), which indicates that the charge on $\mathrm{PEH}_{<1,4>}$ is harvested and flipped periodically. The zoomed-in view of the waveform in the ZC state is depicted in Fig. 8(b), showing the change of $V_{\mathrm{PEH}<1,4>}$ during $\mathrm{PH_{RYC}}$, $\mathrm{PH_{BF<1,5>}}$, $\mathrm{PH_{RUS}}$, and $\mathrm{PH_{RB}}$ in detail. Through the eight-phase SBFRR technique, the $V_{\mathrm{PEH}<1,4>}$ can be rebuilt at a voltage of 0.61 V_{RECT}. Notice that as the duration of the ZC state is about 80 μs, which accounts for only 1.6% of half the excitation cycle, $\mathrm{PEH}_{<3,4>}$ can be regarded as flipping capacitors during this period without sacrificing the energy harvesting efficiency.

Fig. 8(c) depicts the zoomed-in view of the waveform in the EH state. Due to the use of the three-phase SPDC technique, the voltage at both ends of the PEH is not clamped to V_{RECT} as the traditional designs, but changes periodically with the states. The detailed view of the PEH voltage ripple is shown in Fig. 8(d). During $\mathrm{PH_{EH0}}$, $V_{\mathrm{PEH}<1,4>}$ are rectified and charge C_{RECT}. As C_P is much smaller than C_{RECT}, $V_{\mathrm{PEH}<1,4>}$ increases significantly. During $\mathrm{PH_{EH1}}$, $\mathrm{PEH}_{<1,4>}$ are used as flying capacitors to power the load, leading to a decrease in $V_{\mathrm{PEH}<1,4>}$. During $\mathrm{PH_{EH2}}$, $\mathrm{PEH}_{<1,4>}$ are connected in parallel to C_{RECT} to voltage rebalancing. Notice that a hump will emerge on C_{RECT} when the interface enters the ZC state as shown in Fig. 8(c). This phenomenon is due to the charge recycle in $\mathrm{PH_{RYC}}$ and charge reuse in $\mathrm{PH_{RUS}}$. Fig. 9 shows the simulation results when the load voltage V_{LOAD} is set to 4.8 V. It can be observed that the nonideal factors have much less influence on MOPIR when vibration level is high. When VCR = 1×, the simulated MOPIR is 5×, which is close to the theoretical value. When the VCR is other than 1, the simulated MOPIRs are lower due to the offset in ZC detection and forward voltage in AR.

III. Circuit Implementation

The block diagram of the proposed system is depicted in Fig. 10. To reduce the power consumption, the system is

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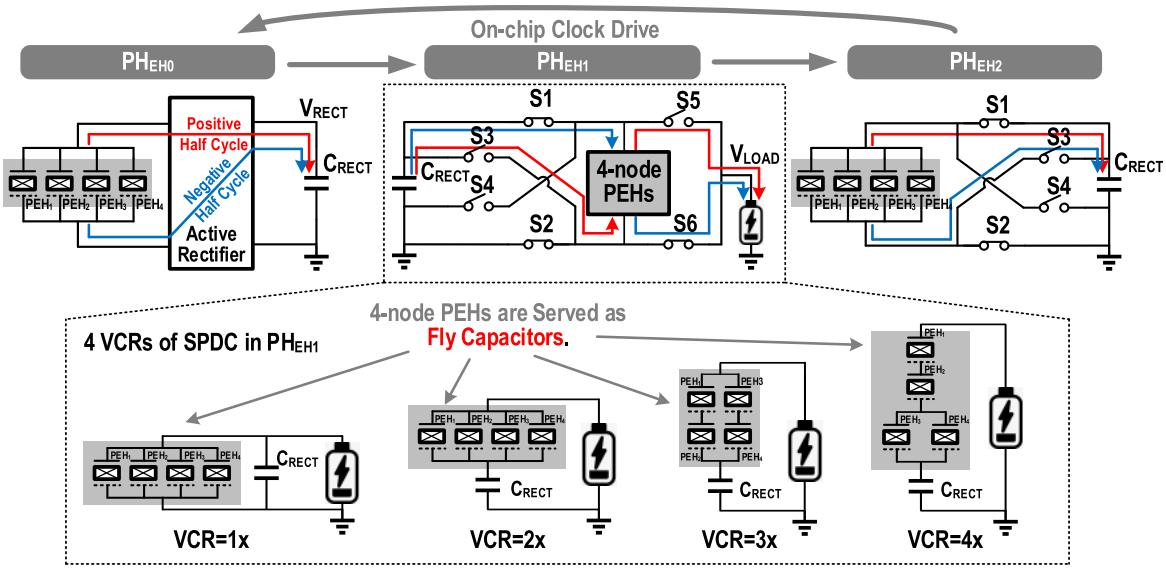

Fig. 6. Three-phase operation of the proposed SPDC technique.

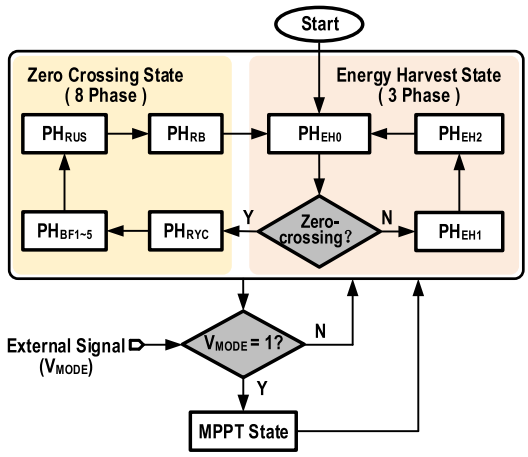

Fig. 7. State machine of the proposed interface system.

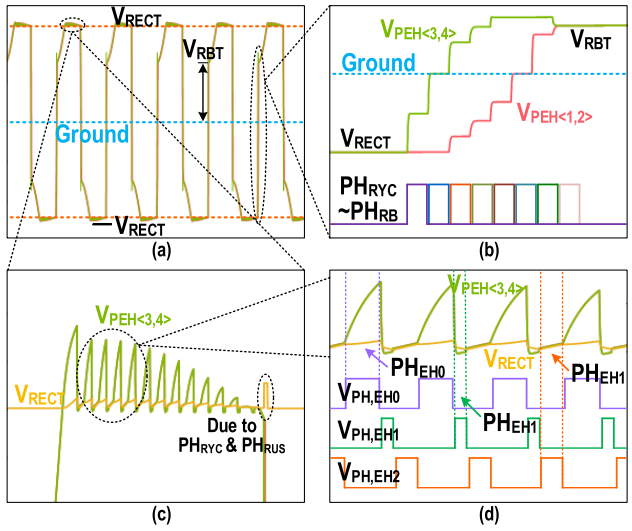

Fig. 8. Simulated waveform of the proposed system: (a) EH state. (b) ZC state. (c) $V_{PEH<3,4>}$ in EH state. (d) Detailed view of the ripple and drive clocks.

divided into two voltage domains. The controller is driven by system clock f_{OSC_SLOW} to configure the analog switch array

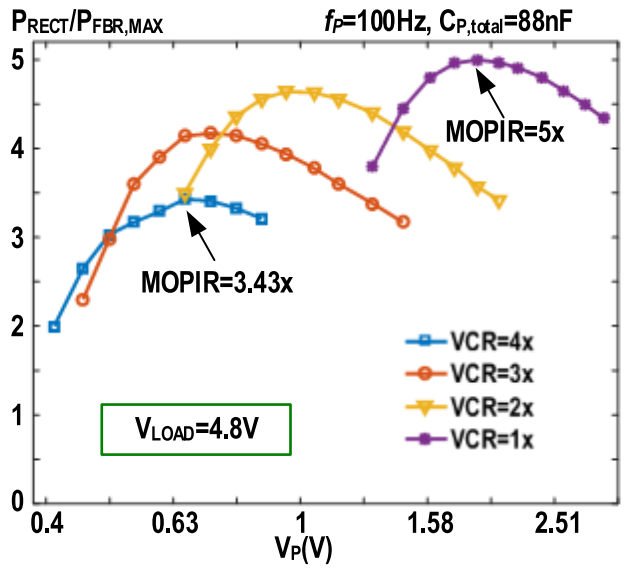

Fig. 9. Simulated $P_{RECT}/P_{FBR,MAX}$ versus V_P under different VCR.

to adjust the combination of the PEH inputs. The controller configures the analog switch array to adjust the combination of the PEH inputs. During PH_{EH0}, the AR generates $V_{CP<1,2>}$, which is sampled by f_{ZCD_SAMPLE} to output $V_{ZC<1,2>}$. $V_{ZC<1,2>}$ is the instruction signal of the ZC/EH state. When $V_{ZC<1,2>}$ maintains at a high voltage, the system operates in EH mode and enters the ZC state otherwise. The analog switch array controller generates signals $[(\vec{U}, \vec{B}, \vec{K}, \vec{D})]$ to control the analog switch array to configure PEHs as energy sources, flying capacitors, and flipping capacitors for time-sharing reuse. The external signal V_{MODE} can control whether the system switches to the MPPT state. In the MPPT mode, the MPPT controller will set the VCRs of SPDC according to V_P. Meanwhile, f_{OSC_SLOW} is adjusted to improve the output ripple under high excitation intensity, reduce switching losses, and improve the reliability of zero crossing detection under low excitation intensity.

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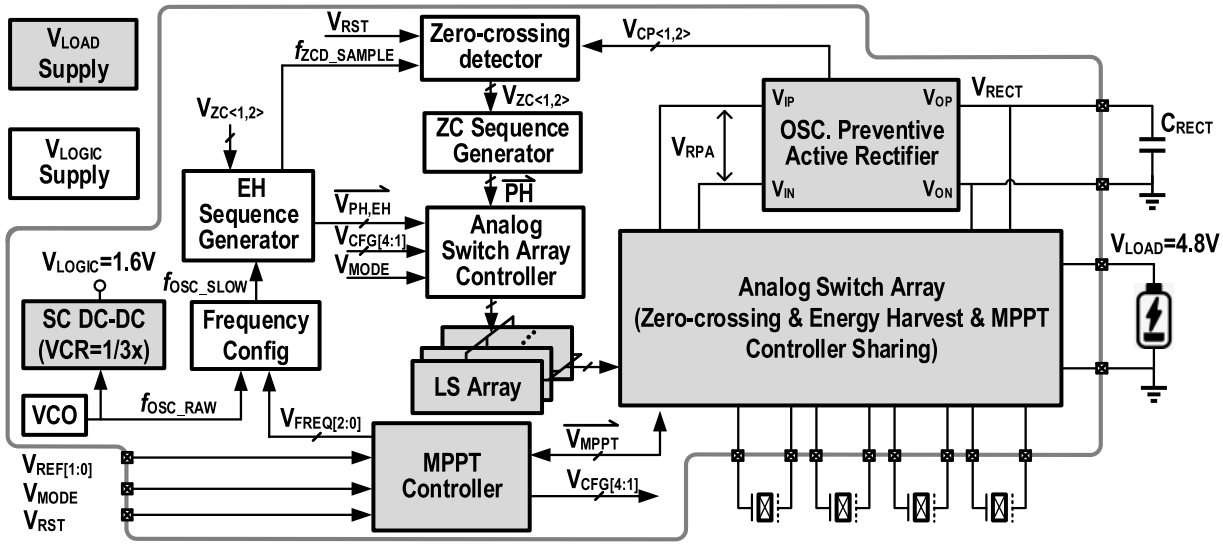

Fig. 10. Structure of the proposed interface.

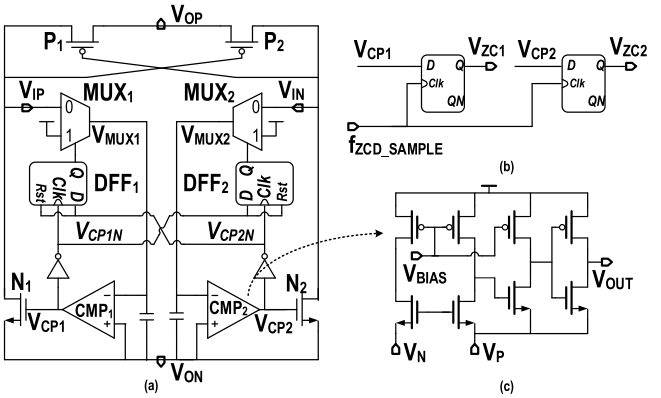

Fig. 11. Circuit implementation: (a) OSC preventive AR. (b) ZC detector. (c) Comparator in rectifier.

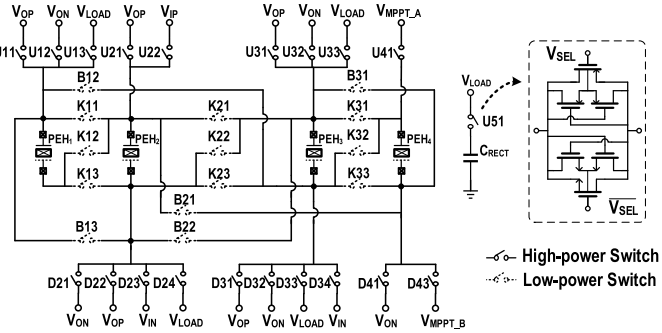

Fig. 12. Analog switch array.

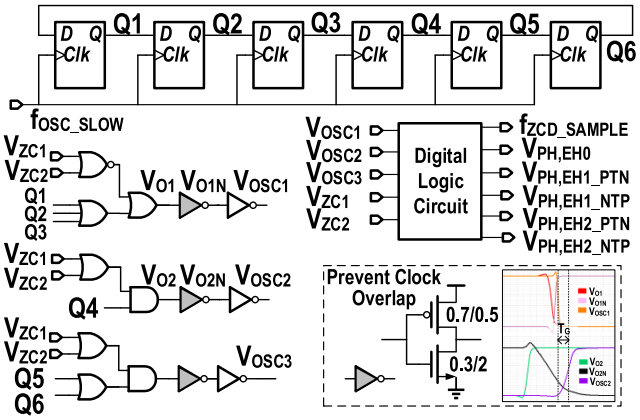

Fig. 13. EH sequence generator.

A. AR and ZC Detectors

Fig. 11(a) shows the AR implementation, which is composed of power transistors $P_{<1,2>}$ and $N_{<1,2>}$ and comparators $CMP_{<1,2>}$, with $CMP_{<1,2>}$ and $N_{<1,2>}$ serving as active diodes. One major problem of AR is that when the ZC of I_P is detected, the nonideal factors such as charge injection may induce a voltage noise at both ends of the PEH, leading to $V_{CP<1,2>}$ oscillation after being amplified by the comparator, affecting the normal operation of the system. To address this problem, MUXs are inserted in the loop to disconnect the comparators after $V_{CP<1,2>}$ changes and connect the comparators next time before ZC detection. Taking the left side of AR as an example, V_{CP1} drops down to zero to turn off N_1 when I_P crosses zero, causing V_{CP1N} to rise. This triggers DFF_1 for switching MUX_1 output to ground, thus cutting off the path that may cause oscillation at the V_{CP1} node. Meanwhile, the rising edge of V_{CP1N} resets the DFF_2 to enable MUX_2 and CMP_2. During PH_{EH0}, f_{ZCD_SAMPLE} samples $V_{CP<1,2>}$ to obtain $V_{ZC<1,2>}$, which will be utilized to instruct the EH/ZC sequence generator to produce the required configuration pulses.

B. Analog Switch Array

Fig. 12 depicts the analog switch array. There are 34 switches in the array, including 20 high-power switches and 14 low-power switches. The switches adopt the transmission gate structure, and the MOSFETs in each switch adopt active body biasing. The switch array is designed based on two considerations, to optimize the gate switching loss, the switch conduction loss, and the power density. The first consideration is to reuse switches on the same path to reduce the number of switches required in different phases. For example, switch U11 is reused during PH_{RYC} and PH_{EH1}, and switch K12 is reused during PH_{BF4}, PH_{BF5}, PH_{RUS}, and PH_{EH1}. Thanks to the switch

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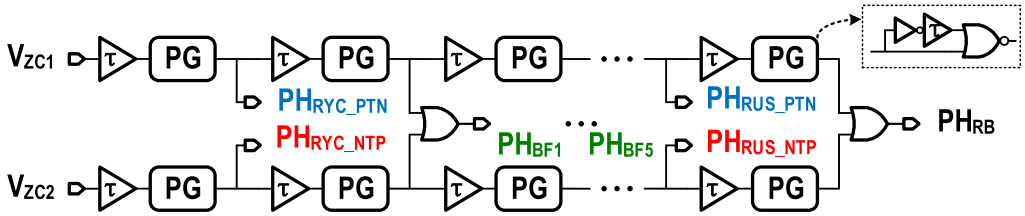

Fig. 14. ZC sequence generator.

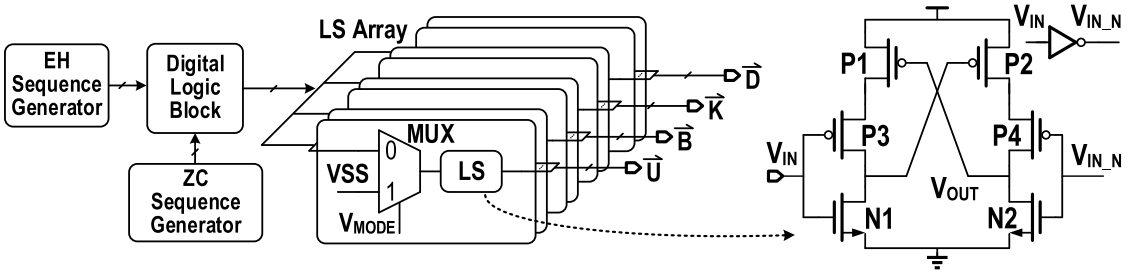

Fig. 15. Analog switch array controller.

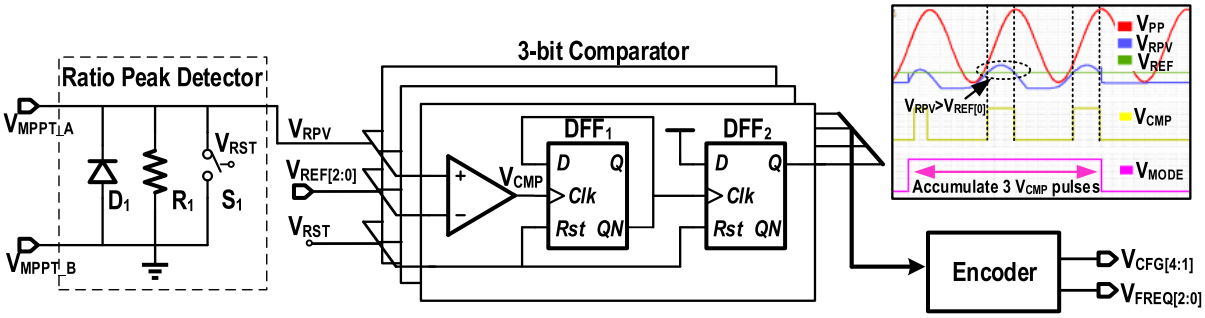

Fig. 16. MPPT controller and simulated waveform during the MPPT state.

reuse, the number of switches decreased from 110 to 34. The second consideration is that there are two switch sizes based on the conduction current. Specifically, the current at nodes near C_{RECT} and V_{LOAD} is larger than that at the other nodes. The aspect ratio of PMOS and NMOS in the high-power switches are 480/0.5 μm and 400/0.6 μm, respectively, while the size of low-power switches is half of that of the high-power switches.

C. Sequence Generator

Fig. 13 shows the EH sequence generator, which generates the control sequence to drive the SPDC switches from $\mathrm{PH_{EH0}}$ to $\mathrm{PH_{EH2}}$ during EH state. The six DFFs form a shift register to generate six pulses periodically. The logic circuit then encodes $V_{\mathrm{ZC}<1,2>}$ and $Q_{<1,6>}$ to generate the required control signals, such as $f_{\mathrm{ZCD_SAMPLE}}$, $\vec{V}_{PH,EH}$, and so on. The duration ratio of $\mathrm{PH_{EH0}}$~$\mathrm{PH_{EH2}}$ is 3:1:2, as $\mathrm{PH_{EH0}}$ and $\mathrm{PH_{EH2}}$ need more time to ensure stable sampling and voltage balancing. Notice that there is no interval between adjacent pulses $Q_{<1,6>}$, which will lead to phase overlap between $\vec{V}_{PH,EH}$ and energy loss in the EH state. To avoid phase overlap, the aspect ratio in the gray-filled inverter adopts an asymmetric design to increase the delay time of the rising edge as shown in the figure.

Fig. 14 depicts the ZC sequence generator which generates the pulses from $\mathrm{PH_{RYC}}$ to $\mathrm{PH_{RB}}$ during the ZC state. There are two paths in the generator. When the rectifier detects the ZC time, $V_{\mathrm{ZC1/2}}$ jumps to zero, indicating that the I_P crosses from positive to negative (PTN) or negative to positive (NTP), respectively. The falling edge of $V_{\mathrm{ZC1/2}}$ triggers the pulse generators (PGs) to generate the required sequence.

D. Analog Switch Array Controller

Fig. 15 shows the analog switch array controller, which decodes the output pulses of EH & ZC sequence generator to generate the control signals ($\vec{U}$, $\vec{B}$, $\vec{K}$, $and\,\vec{D}$). To save power, digital signals are processed in the low-power domain and then level-shifted using the level shifter (LS) array to control the analog switch array. When V_{MODE} is low, the system will enter the normal energy harvesting state. Otherwise, the system will enter the MPPT state. The analog switch array controller employs 39 LS cells with low power consumption as shown in Fig. 15. Simulation results show that an LS cell only consumes 0.53 pJ/cycle when the input is converted from 1.6 to 4.8 V.

E. MPPT Controller

In this system, the open-circuit voltage of the PEH is positively correlated with the excitation intensity. Therefore, it is necessary to set the optimal VCR according to V_P in the MPPT state for operating at the MPP. Fig. 16 depicts the MPPT controller, which is composed of a ratio peak detector, a 3-bit comparator, and an encoder. We explore the fractional open-circuit voltage (FVOC) method for MPPT and employ a ratioed peak detector to prevent detection error or overshoot. When the external signal V_{MODE} triggers the system into the

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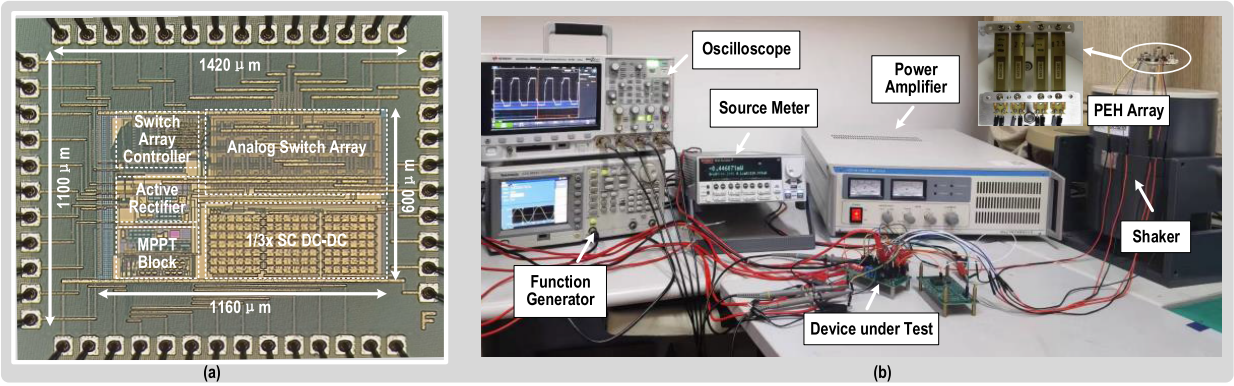

Fig. 17. (a) Chip micrograph. (b) Measurement setup.

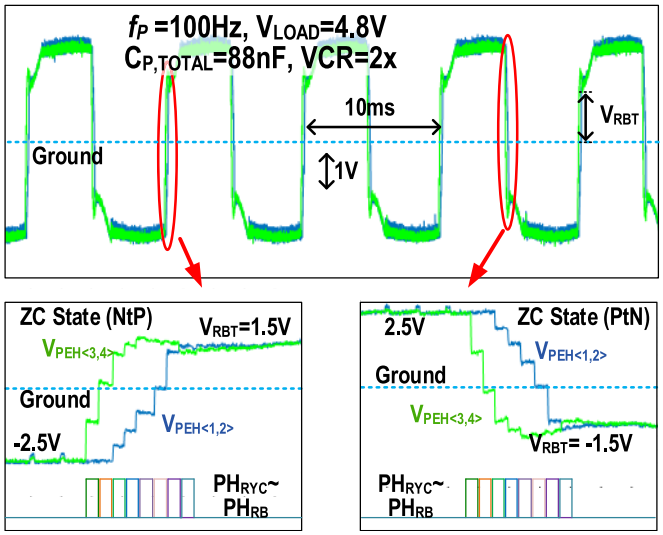

Fig. 18. Measured waveform of V_{PEH} and the zoomed-in view during the ZC state.

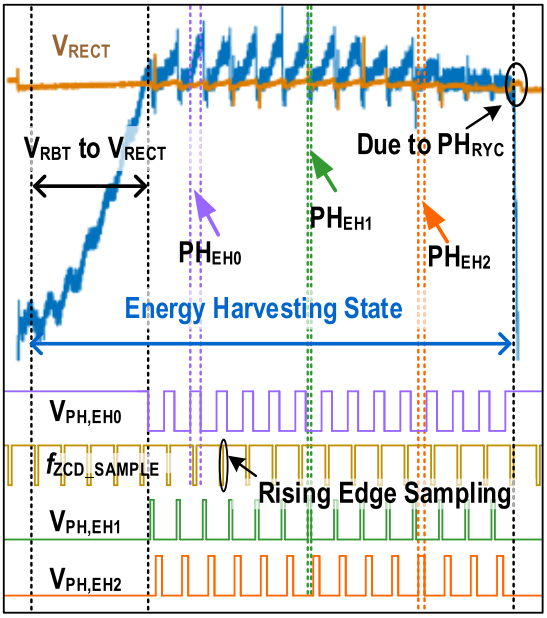

Fig. 19. Zoomed-in view of the measured V_{PEH} during the EH state.

MPPT state, the ratio peak detector and the 3-bit comparator will be reset by V_{RST} to switch $PEH_{<1,4>}$ into parallel and connect to the node V_{MPPT}. Here, D_1 is responsible for rectifying the PEH output, and R_1 is for reducing the impedance across the PEH terminals. The detected peak voltage V_{RPV} is scaled to about 0.5 V_P. The 3-bit comparator outputs are determined according to V_{RPV} for triggering DFF_1 and DFF_2, with the results further processed by the encoder to configure the VCR and f_{OSC_SLOW} to optimize the system's performance.

IV. Measurement Results

The proposed interface chip prototype is fabricated using a 0.18-μm CMOS process. The chip micrograph is shown in Fig. 17(a), occupying an active area of 0.7 mm^2.

The four PEH arrays are tightly mounted on the shaker (KDJ-50), which receives periodic vibrations from a function generator together with a power amplifier (KD5708) as shown in Fig. 17(b). PPA-1021 is adopted to implement the PEH array. To decrease the mismatch between the PEH cells, the customized clamp used to fix the array is designed with rigid materials. The measurement results indicate that the maximum voltage difference between the edge PEHs and center PEHs is 0.1 V, which is only about 3% of the open-circuit voltage. This mismatch will decrease with the reduction of the vibration level. The interface is measured at a PEH excitation frequency of 100 Hz, with V_{LOAD} set to 4.8 V by manually tuning the load current.

Fig. 18 shows the measured waveform across the PEH terminals at ZC state with VCR = 2 at an excitation frequency of 100 Hz. During the ZC state, after eight phases of SBFRR operation, the PEH voltage is flipped from −2.5 to 1.5 V. This corresponds to a voltage flipping efficiency of 80%, defined as

$$\text{Flipping efficiency} = \frac{V_{RBT} + V_{RECT}}{2 \cdot V_{RECT}}. \tag{16}$$

Fig. 19 shows the measured waveform across the PEH terminals during the EH state. $V_{PEH<1,4>}$ is charged from the rebuilt voltage (V_{RBT}), with the clock signal (f_{ZCD_SAMPLE}) triggering the sampling of $V_{CP<1,2>}$. When $V_{PEH<1,4>}$ exceeds V_{RECT}, AR is turned on, and the system starts to operate among the EH phases (PH_{EH0}–PH_{EH2}). If $V_{PEH<1,4>}$ is lower than V_{RECT}, the system will reenter the ZC state, leading to a droop at V_{RECT} as observed in Fig. 19 as induced by the charge injection in the PH_{RYC} phase. This droop will be recovered in the PH_{RUS} phase due to the connection to C_{RECT}.

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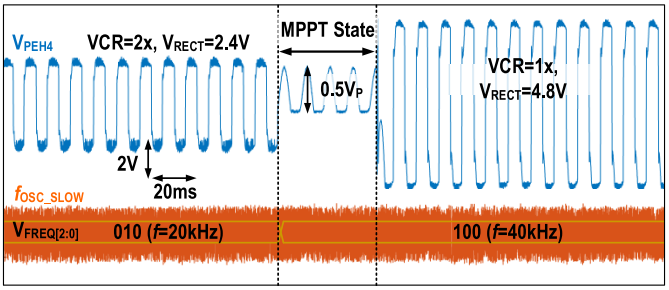

Fig. 20. Measured waveform during the MPPT state.

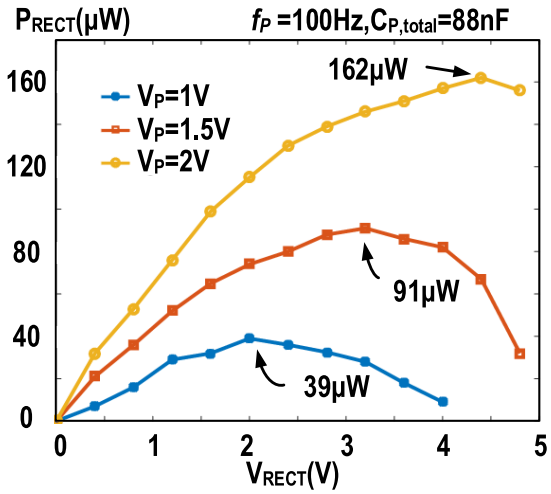

Fig. 21. Measured P_{RECT} versus V_{RECT} under different V_P.

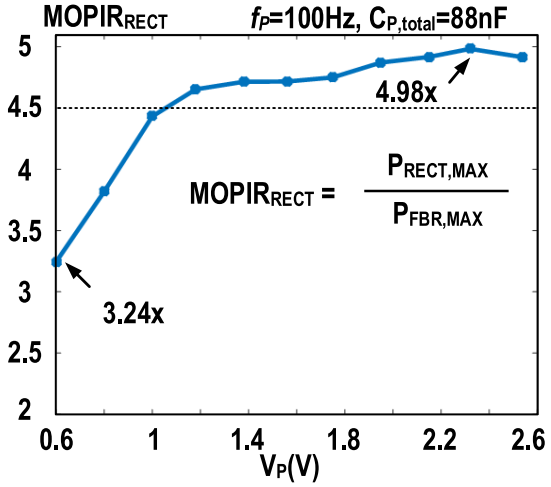

Fig. 22. Measured relationship between $\mathrm{MOPIR}_{\mathrm{RECT}}$ and V_P.

Fig. 20 depicts the waveform of V_{PEH4} in the MPPT state. Initially, the optimal VCR is 2×, and V_{RECT} is around 2.4 V. Increasing the vibration level causes the interface to deviate from the maximum power point. During the MPPT state, V_{PEH4} is rectified and decreased to about 0.5 V_P. The shrunken V_{PEH4} is then compared with the reference voltage $V_{\mathrm{REF[2:0]}}$ to update VCR. When the interface returns to the EH state, V_{RECT} rises to about 4.8 V, which verifies that the VCR is switched to 1×. The operation frequency $f_{\mathrm{OSC_SLOW}}$ automatically changes based on the input vibration level. When VCR = 1×, $f_{\mathrm{OSC_SLOW}}$ is 40 kHz; When VCR = 2×, 3×, and 4×, $f_{\mathrm{OSC_SLOW}}$ is 20 kHz.

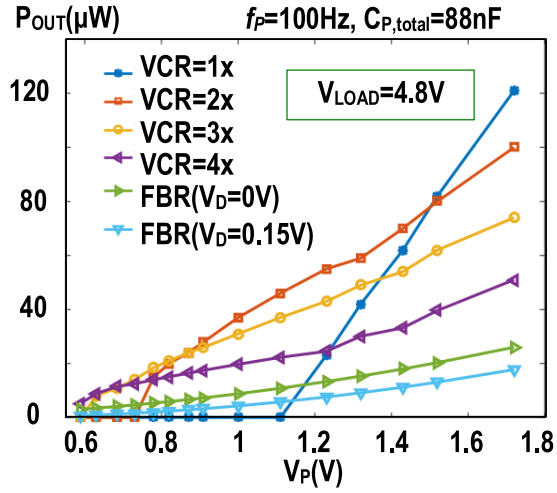

Fig. 23. Measured P_{OUT} versus V_P under different VCR.

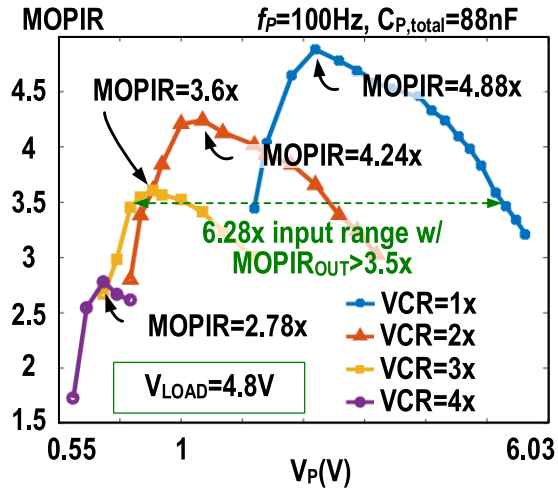

Fig. 24. Measured relationship between MOPIR and V_P under different VCR.

Fig. 21 depicts the measurement of the harvested power P_{RECT} versus V_{RECT} under three different vibration levels. When V_P equals 1.5 V, P_{RECT} attains its maximum value at $V_{\mathrm{RECT}} = 3.2$ V. It can deliver up to 162μW at $V_P = 4.4$ V. The relationship between $\mathrm{MOPIR}_{\mathrm{RECT}}$ and V_P is shown in Fig. 22. The measured $\mathrm{MOPIR}_{\mathrm{RECT}}$ can be up to 4.98× when $V_P = 2.32$ V. The MOPIR is obtained by comparing the measured maximum output power with the calculated output power for an ideal FBR (with diode drop $V_D = 0$). When $V_P > 1$ V, $\mathrm{MOPIR}_{\mathrm{RECT}}$ can maintain above 4.43×. When $V_P < 1$ V, $\mathrm{MOPIR}_{\mathrm{RECT}}$ is significantly reduced due to the nonideal zero-crossing detection and increased switching loss.

The measured P_{OUT} versus V_P under different VCR is depicted in Fig. 23. It can be observed that a low VCR is preferable when the vibration intensity is high. When $V_P = 1.72$ V, the interface can obtain 121 μW with VCR = 1×, while only output 51 μW with VCR = 4×. Fig. 24 shows MOPIR versus V_P under different VCR. When VCR = 1, the MOPIR of the system can reach 4.88×. As the VCR increases, the MOPIR reduces due to the reduction of the ZC accuracy. However, when VCR = 4, the MOPIR can still reach 2.78×, which is a 39% improvement compared to the ideal switch-only rectifier. The entire system can maintain an MOPIR of

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TABLE I
PERFORMANCE COMPARISON

	JSSC'19 [4]	JSSC'20 [19]	ISSCC'19 [24]	JSSC'19 [20]	ISSCC'22 [25]	TCAS-I'21 [26]	**This Work**
Technology	0.13μm	0.18μm	0.18μm	0.18μm	65nm	0.18μm	**0.18μm**
Technique	SSHI	SPFCR	SaS	SE-SSHC	MSVR SECE	SSHCI	**SBFRR**
Passive Energy Reservoir for Bias-flip	L=33μH	C_{TTL}=272nF	L=1mH C_{TTL}=10nF	C_{TTL}=4nF	L=22μH	L=68μH C_{TTL}=2nF	**None**
Passive Energy Reservoir for DC-DC	N/A	C_{TTL}=272nF	L=1mH C_{TTL}=10nF	N/A	L=22μH	L=68μH C_{TTL}=1.1nF	**None**
Normalized Volume (V^*_{NOR})	1.3	1.3	11.15	1.3†	1.29	2.06	**1**
Chip Size	0.53mm^2	0.2mm^2	0.47mm^2	3.9mm^2	3.11mm^2	1.23mm^2	**0.7mm^2**
P_{IN} Adaptation	N/A	SC DC-DC	SaS	N/A	SECE	Inductive DC-DC	**SPDC**
No. of Input	1	1	1	4	3	1	**4**
Piezoelectric Capacitor	22nF	22nF	8nF	1.94nF	N/A	2nF	**88nF (22nF each))**
Flipping Efficiency	0.88	0.84	N/A	0.85	N/A	0.82	**0.8**
MOPIR	3.66x	3.7x∽6.26x	3.96x	2.57x∽5.89x	3.2x	3.62x	**2.78x∽4.88x**
FoM$^+$	0.28	0.28∽0.48	0.04	0.2∽0.45	0.25	0.17	**0.28∽0.49**
VCR of DC-DC converter	N/A	1/3x, 2/3x, 1x, 2x	Continuous	N/A	Continuous	Continuous	**1x, 2x, 3x, 4x**
Operating Frequency	432Hz	200Hz	85Hz	219Hz	N/A	415Hz	**100Hz**

$^*V_{NOR}$ = System Volume / ChipVolume
$^+$FoM = MOPIR / System Volume
† Assume [19] introduce a L = 33μH for DC − DC

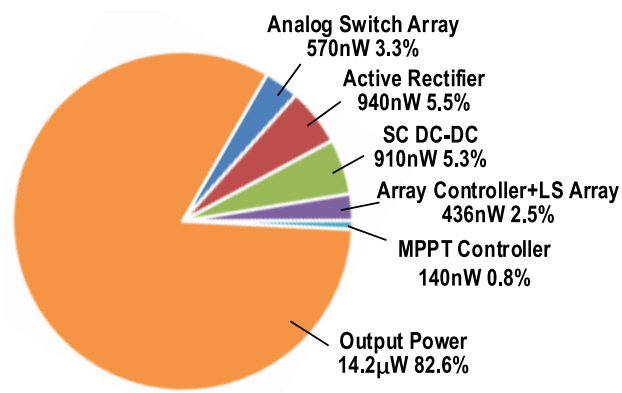

Fig. 25. Power breakdown of the proposed system at VCR = 3×.

> 3.5× when V_P is from 0.78 to 4.9 V. Fig. 25 summarizes the measured power breakdown at VCR = 3×. The proposed system achieves an efficiency of 82.6%, with 3.3%, 5.5%, 5.3%, 2.5%, and 0.8% consumed by the switch array, AR, SC dc–dc, array controller, and MPPT controller.

Table I shows the comparison of the proposed design with the state of the art. Compared to [20], this work can avoid using flipping and flying capacitors, as well as excessive HV devices, thus greatly reducing the chip area and cost. In this article, the IC chips for all the interface circuits are assumed to occupy 10 mm^3, the volume of the resistance or capacitance is assumed to occupy 0.75 mm^3/unit, and the volume of the inductance is assumed to be 100 mm^3/mH, similar to [17]. Based on these parameters, we can calculate the system volume for other works. The figure of merit (FoM) represents the performance improvement per unit volume, which is given by FoM = (MOPIR)/(system volume). Compared to other designs in the table, this work achieves the highest FoM without using any external energy reservoirs, which is imperative to applications requiring an ultracompact system volume, such as an implantable microoxygen generator (IMOG) [27] or a gastric seed [28].

V. CONCLUSION

This work proposes a novel self-bias flip PEH interface and switched-PEH dc–dc converter. The fully integrated solution together with a high FoM renders the proposed PEH interface suitable for applications requiring ultracompact system volumes such as biomedical implants or wearable devices. Particularly, the proposed technology can be combined with MEMS, greatly reducing the system volume. It utilizes the PEH inherent capacitor for self-bias-flip, which further improves the system energy efficiency through charge recycling and reusing phases. Using a total of four PEHs, this work achieves an eight-phase operation without using additional volume-consuming passive components. In addition, PEHs can serve as both energy sources and flying capacitors to achieve maximum power transmission to the load. To ensure a more stable and reliable operation, this work also improves the active diode in the ac–dc rectifier to avoid zero-crossing oscillation.

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