An ultrasound receiver channel for vagus nerve imaging

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An ultrasound receiver channel for vagus nerve imaging

by

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Abstract

The neuromodulation modality based on the focused ultrasonic stimulation (FUS) has gained its interests for being non-invasive while having unprecedented high spatial resolution and deep penetration. The commercially available image-guided FUS device for neuromodulation setups are normally bulky, by employing an 1-D array transducer element to produce the FUS and a separate ultrasonic scanning device for B-Mode imaging purpose. Aiming to design a wearable neural stimulating device for human's vagus nerve, a miniature device with 2-D array transducers is proposed to replace the conventional setup as it can statically generate FUS. The device is capable of locating the vagus nerve and non-invasively stimulating the nerve by integrating the imaging system and the neural modulation system together. In typical neuroFUS applications, an ultrasound image is obtained prior to neuromodulation, to obtain the precise coordinates of the nerve. This project presents a front-end CMOS circuit for the 2-D array ultrasound-based system for imaging the vagus nerve, as a part of the full system for the neuromodulation capabilities. The imaging signal chain enables the local digitization, allowing a robust digital beamforming and readout signal.

The front-end CMOS circuit mainly contains three functions: the low-noise amplifier (LNA), time-gain-compensation (TGC) function block and the analog-to-digital converter (ADC). The front-end received chain employs the power- and area-efficient design consideration, interfacing the 12 MHz piezoelectric signal from the PMN-PT transducer element. The mixed signal system is implemented in 0.18μm TSMC CMOS technology and operating under the 1.8 V voltage for both analog and digital supply. The analog front end (AFE) has the variable voltage gains up to 62 dB to interface the 1 V full scale range of the ADC. For ultra low power and chip area considerations, the ADC topology is a 6-bit single-ended common-voltage based successive-approximation (SAR) ADC with the typical sample rate 50 MS/s. The SAR ADC consumes 415.8 μW and achieves dynamic performances of 37 dB SNDR and 49.4 dB SFDR. The total power consumption of the signal chain is 1.3 mW and the layout chip area consumes 150 μm^2.

Keywords: ultrasound neuromodulation, 2-D array, receive digitization, low-power, low-area, SAR ADC

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1 Introduction

1.1. Background and Motivation

The vagus nerve plays a critical role in the autonomic nervous system by regulating the metabolic balance and maintain the homeostasis [15]. This regulatory function is implemented by means of using afferent and efferent nerve fibers, which implements a bidirectional pathway between the brain and several organ systems, such as the gastrointestinal tract. As the Figure.1.1 shows. It maintains the gastrointestinal homeostasis and to connect emotional and cognitive areas of the brain [16]. The vagus nerve system is strongly related to psychiatric conditions, such as the mood disorder, emotion, anxiety disorder, depression and headaches. Besides this, the vagus nerve fibers in the pathway also regulate many other organs such as heart, lungs, liver and kidneys [1].

Researches have been conducted on of the cervical region since the 1880s. It was found that crude and compression on the carotid artery near the neck region could mitigate the seizure of epilepsy [17]. The term vagus nerve stimulation (VNS) is used to represent techniques that stimulates the vagus nerve. During 1930s to 1940s, it was found that electrical VNS had the effect on the anticonvulsant effects on experimentally induced seizures in dogs [16]. In 1997, the United States Food and Drug Administration (FDA) approved an implanted VNS device to treat the epilepsy [16]. In 2005, the FDA also regulated the indication that implanted VNS techniques also helps to ameliorate depression. Many other trials and studies have reported the use of VNS to treat Alzheimer's disease, anxiety disorders, epilepsy and PTSD. However, these studies are not yet approved by the FDA. Despite these findings, there is still a lot to discover about the biological effects of VNS. Researchers have shown that VNS has potentially favorable effects on cerebrovascular, cardiovascular, metabolic and many other physiological conditions [18].

Modern VNS methods are primarily used as a replacement or complement to pharmaceutical therapies. In the case of epilepsy, it has been shown that about one-third of patients don't fully respond to pharmaceutical drugs. [19]. Thus, VNS gained its

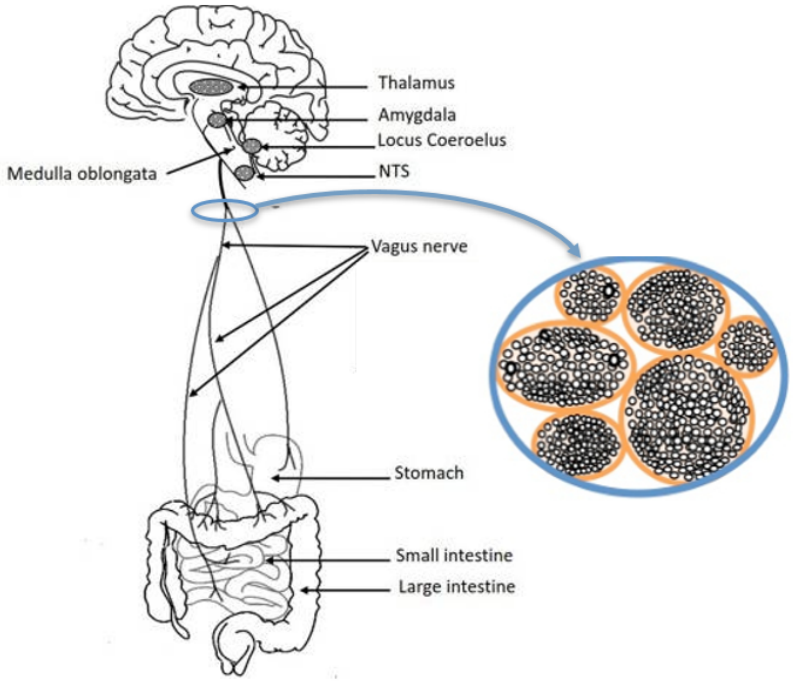


Figure 1.1: The overview of the function of the vagus nerve and its cross-section fibers [1].

interest for helping these patients. However, the implant device also brings surgery risks such as infection and pain where the implanted device locates and side effects after surgery such as Insomnia, difficulty swallowing and shortness of breath [19]. Thus, there has been several recent works on non-invasive neural interfaces for both research and clinical applications. The challenge of this field are on techniques to reach safe neuromodulation with high-spatial resolution and high depth of penetration. These two characteristics are hard to mutually obtain.

From past few years, some approaches are proposed such as the transcutaneous vagus nerve stimulation (t-VNS) [20] device to treat neurological diseases and the vagus nerve stimulation non-invasively (nVNS) [21] by delivering a proprietary signal through the skin to either the right or the left branches of the vagus nerve in the neck. Focused ultrasound stimulation (FUS) has emerged as a solution for reaching unprecedented resolution while being non-invasive. NeuroFUS techniques enable using low intensity FUS to deliver burst of ultrasound waves with high-spatial resolution without leading to tissue heating and damage. For example, the peripheral focused ultrasound neuromodulation (pFUS) could stimulate sub-organ locations containing specific targeted neurons by employing the ex vivo platform setup [22].

Another advantage of using FUS techniques is that the ultrasound imaging is also a good medical imaging technique. In typical neuroFUS research experiments for peripheral nerve stimulation, an ultrasound image is obtained prior to neuromodulation, to obtain the precise coordinates of the nerve. In this thesis project, we are targeting on designing a image-guided FUS device that the FUS could excite the vagus neuronal activity in the human's neck region. The conventional image-guided FUS setup for

experiment research normally very bulky. As the Figure.1.2 shows, in order to image the FUS-elicited physiological responses, a separated ultrasonic imaging transducer is needed. To visually observe the neuronal responses of the mouse, the static nerve is precisely and non-invasively targeted by both the ultrasound brightness (B-mode) imaging transducer and the activation induced by the FUS stimulation [2].

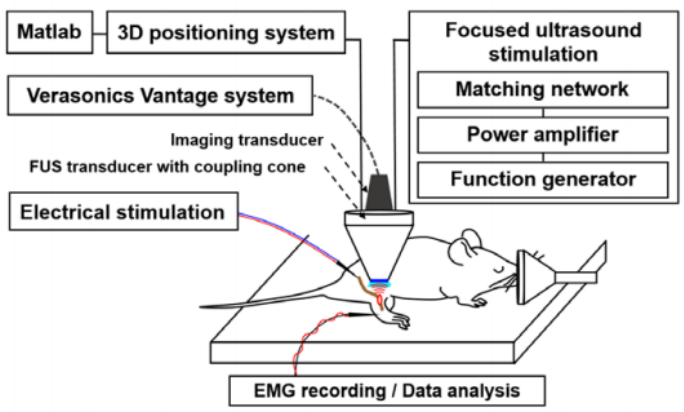
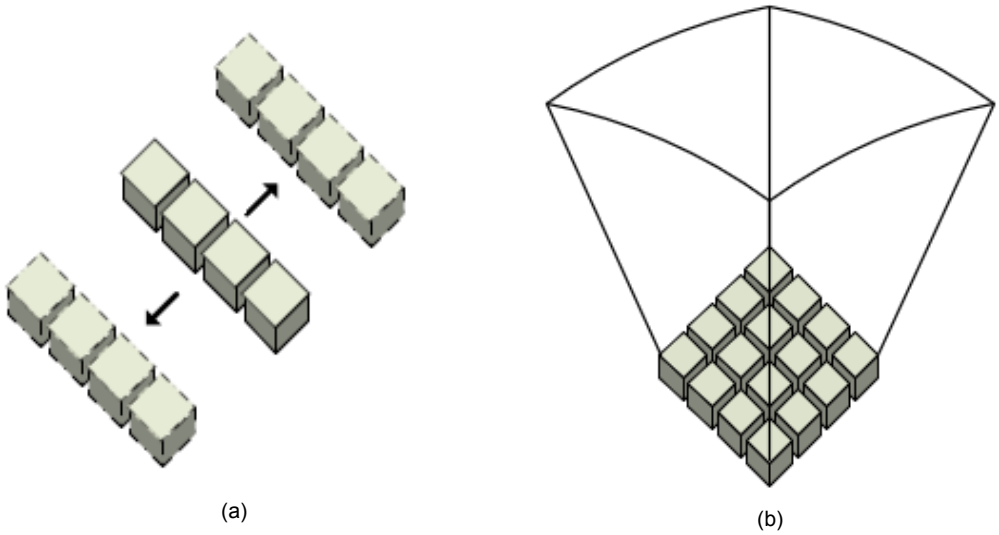


Figure 1.2: The conventional experimental setup to test the mouse's static nerve: 3-D positioning system, image-guided FUS stimulation and EMG recording [2].

The traditional imaging transducer is typically a 1-D array and the stimulation transducer is a single element focused transducer with a mechanical acoustic lens. The volumetric 3-D FUS is formed by the combined multiple cross-sectional frame line by moving the 1-D array in the elevation direction (Figure.1.3a). The limitation of the current setup is the large size, which is impossible for neuroFUS to be used as wearable device. Instead, the static 2-D array (Figure.1.3b) to enable the imaging system fully reflecting the real time visualization [23]. This is done by using the 2-D array to perform a real-time focusing, allowing for a stronger stimulating at any desired planes.



(a) (b)

Figure 1.3: (a) Moving 1-D array transducer. (b) 2-D array transducer to form the 3-D image.

Neuromodulation relies on a imaging system to reflect the stimulation response

after a focus acoustic wave is carried out. To the date, the state-of-the-art commercial miniature 2-D transducer arrays are already out in market, such as the electroCore [24], which is still a bulky system that is impractical to be used as a wearable device. This work's objective is to explore the imaging implementation of the 2-D transducer array for vagus nerve neuromodulation with the characteristics of being miniaturized to a wearable form factor, and can be powered by a small battery. This specifications require the design of a micro-scale and power efficient receiver circuit channel underneath each transducer in a 2D array. This project is focused on the ultrasound receivers, through the combination of advanced ultrasound signal receiver techniques and several existing technical innovations to provide the promising solutions for the 2-D image of the vagus neuromodulation based on the 2-D transducer elements.

1.1.1. Prior Works and Challenges

Efforts have been done in the past few years that using the 2-D piezo-material transducer with the integrated CMOS transmit beamformer. It replaced the conventional bulky ultrasound transducer that requires the manual moving. The miniature 2-D beamformer transmitter can steer the focus spot by employing the electrically phased ultrasound array. This enables to have over 100 kPa with a 5 V supply at 0.5cm focused depth even without the acoustic matching layers [25]. To design the CMOS chips underneath the monolithic integration 2-D transducer array, the size of each channel should be considerably small that the each channel should be bound to $\frac{\lambda}{2}$ (λ is the wavelength of the ultrasound wave) in both directions to avoid grating lobes.

For the image channel, one work has proposed an area-efficient signal chain that utilizes Low-noise Amplifier (LNA) and programmable gain amplifier (PGA) to readout the ultrasonic echoes [26]. Each channel can be controlled individually so that the full 2-D array transducers are controlled by column-by-column and row-by-row operations for the beamforming application. It requires massive number of channels to reach the sufficient dynamic range (DR). Another work that targets on image the transesophageal echocardiography (TEE) with advanced sub-array beamforming techniques to decrease the needed area and power of each channel [27]. It successfully demonstrated the 2-D image by electrically controlling the 2-D array with a fast frame rate.

Besides the above advanced system-level innovations, the developments on the circuit implementations have also recently seen several improvements. A variety of analog circuit topologies have been proposed that implement compact and low-power receive beamformers, such as time-interleaved switched-capacitor circuit [28] and current-reused operational amplifier [27]. Digital beamformer system is also been established, so that all the beamforming is implemented in the digital domain. With the scaling down of CMOS processes, the power consumed by the digital circuits decrease. This leads to a more power-efficient system, while also reducing the complexity at the front-end. However, this approach requires an Analog-to-Digital Converters (ADC) to digitize the received echo. Some approaches also have been established that use the time-interleaved SAR ADC [5] to save the power on the digitizer.

Targeting neuromodulation on the vagus nerve near the neck region brings more harsh design requirements, because the needed penetration depth is deep and the received ultrasound echo is predictably weak as the low reflection coefficient between soft tissue and a nerve. Additionally, for the purpose of a wearable therapeutic device, the heat dissipation budget is also limited. To minimize the overall heat dissipation, the number of transducer and power of each transducer interfacing circuit both are constrained. For the purpose of achieving small volume, the chip density becomes the another challenge as the interconnection among adjacent channels brings more electrical interference. This calls for the more robust circuit implementation, while the layout of whole chip system should be highly compact.

All above mentioned challenges demand innovations both at the system-level and at circuit-level designing. Additionally, some more advanced and even aggressive techniques are needed such as the higher transducer sensitivity and advanced imaging signal algorithm. This is an emerging field requires a comprehensive understanding in both ultrasound transducer physics and solid-state circuit design, which motivates this thesis work.

1.2. Thesis Organization

Apart from the introduction chapter, this thesis is organized as following.

The **chapter 2** introduces methods to achieve neuromodulation on human's vagus nerve. The assumptions and proposes are evaluated by simulation in Matlab environment, which in turn leads to specifications for the ultrasound receiver channel, as giving us the data for the receiver chip design.

The **chapter 3** describes the analog front-end readout circuit to interface with the ultrasound transducer in each channel of a 2-D array. The readout chain contains the LNA and Time Gain Compensation (TGC) blocks.

The **chapter 4** introduces the design of a power-efficient A/D converter with a compact layout size.

The **chapter 5** summarizes the contribution, concludes the final achievement and gives the future perspective of this project.

2

Ultrasound Imaging

This chapter introduces some basic principles of the ultrasound imaging and considerations of the system-level design. The simulation outcomes based on the Matlab environment give specifications of received ultrasonic echoes.

2.1. Fundamental of Ultrasound Imaging

An ultrasound wave is a longitudinal pressure wave with a frequency above the human auditory range (frequency above 20 kHz). When propagating in tissue, ultrasound waves are attenuated by heat conversion from the medium. Additionally, due to the irregular shape of the medium, scattering and refraction also cause energy loss. However the highest contribution for the loss factor is the reflection pattern. This occurs at any different boundary with different material density (or acoustic impedance). When the ultrasound wave encounters the boundary at the medium, only a portion of energy is transmitted into the medium while the rest is reflected. The reflection coefficient R is expressed as [29]:

$$R = (\frac{Z_2 - Z_1}{Z_2 + Z_1})^2. \tag{2.1}$$

Where the Z_1 and Z_2 are the acoustic impedance of two materials sharing the same boundary. The energy reflection is zero when two materials have the matched acoustic impedance, leading to the maximum energy transmission efficiency.

Ultrasound image algorithms are based on the brightness-mode (B-Mode) imaging implementation. The brightness of each pixel of the image corresponds to an amplitude of an echo resulting from a given acoustic reflection in the tissue from an incoming pulsed wave. The final recorded image is a two-dimensional, cross-sectional reflection graph of the wave scanned area.

2.2. Beamforming

The beamforming technique is that the 2-D array transducers generates the phased wave that it has the focused spot. The electronics circuit output the pulsed voltage signal with the specific time-delayed pulse between the adjacent channels. Because the 2-D transducer matrix, we could have beamforming for both neuromodulation and imaging. The beamforming technique for imaging is illustrated at the Figure.2.1. At the transmit (TX) situation, the ultrasound (US) transducers generate by a electrical pulse with a specific delay, so the propagated wave are be controlled to scan at various angles and different focusing depth. For the receive (RX) situation, the system provides the same inversely delay at the signal receiving chain to sum up the signal. Because the summed signal holds stronger wanted echo swing while averaging the unwanted random noise, the final Singal-to-Noise ratio (SNR) of the readout signal after the beamforming is much boosted, allowing for a better image quality.

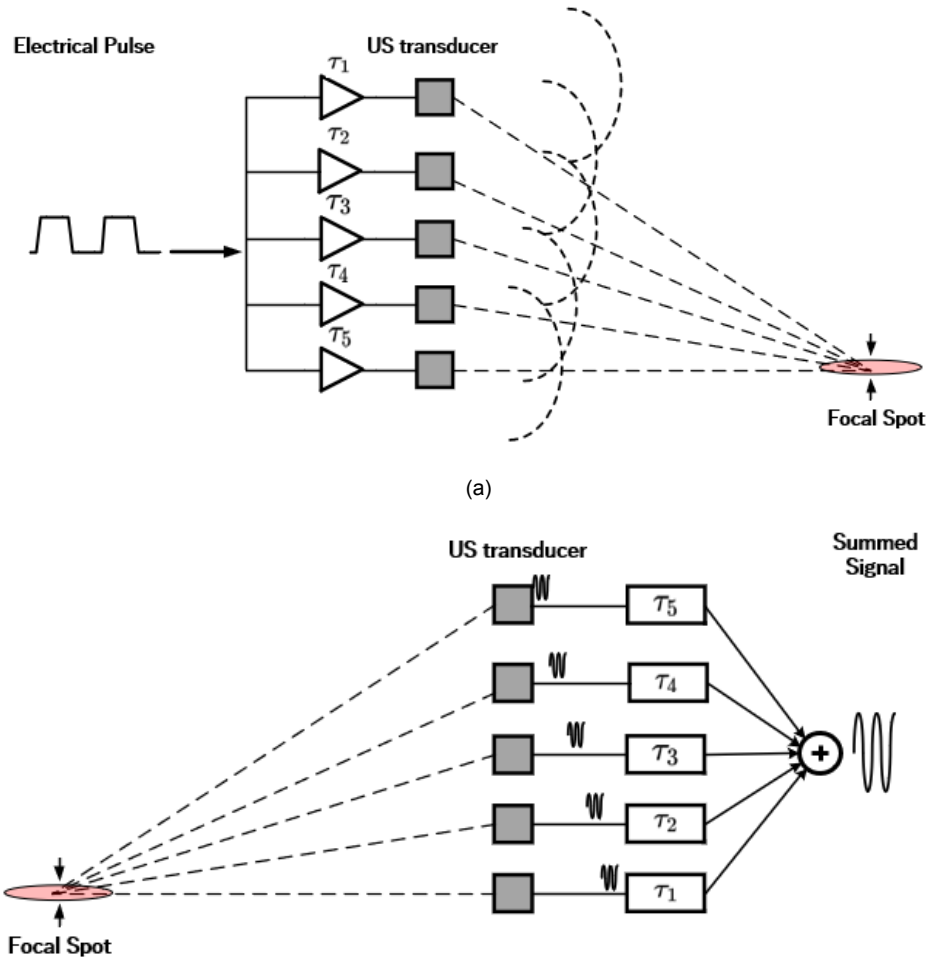


Figure 2.1: The beamforming technique illustration: (a) transmit beam-formed focusing. (b) receive beam-formed signal.

2.2.1. Digital Beamforming and Analog Beamforming

The delay function block in Figure.2.1 at the signal chain is normally achieved by using the capacitor to hold the received signal at specific instants until all channels are in phase. After the signals in all channels are in-phased, there is an analog sum-up function. The summing structure can be achieved by using the summing amplifier topology and the delay block is achieved by using the sample and hold (S/H) capacitor [3]. However, the drawback is the large area requirement of the sampling capacitors. Besides, when number of channels increases, the delay time between two adjacent channels become delicate. Any variant on capacitance will cause the delay-time deviation, making this implementation is hard to achieve when number of channel is large.

To overcome above situations, the micro-beamforming or subarray beamforming scheme has been used in recent years [3]. The transducer matrix is divided into N sub-arrays with each subarray containing M channels. The total delay is also distributed into the coarse delay and the fine delay that coarse delay differs from the different subarrays while the fine delay is produced by the signal chain inside the subarray. Another advantage is the number of out cable is much minimized, allowing for a simple routing out circuitry. Figure.2.2 shows the implementation of subarray beamforming techniques, the fine and coarse delay separation relax the delay lines function requirement. However, the final ADC structure needs to have a high dynamic range and resolution because the summed signal has the larger signal swing and the boosted SNR.

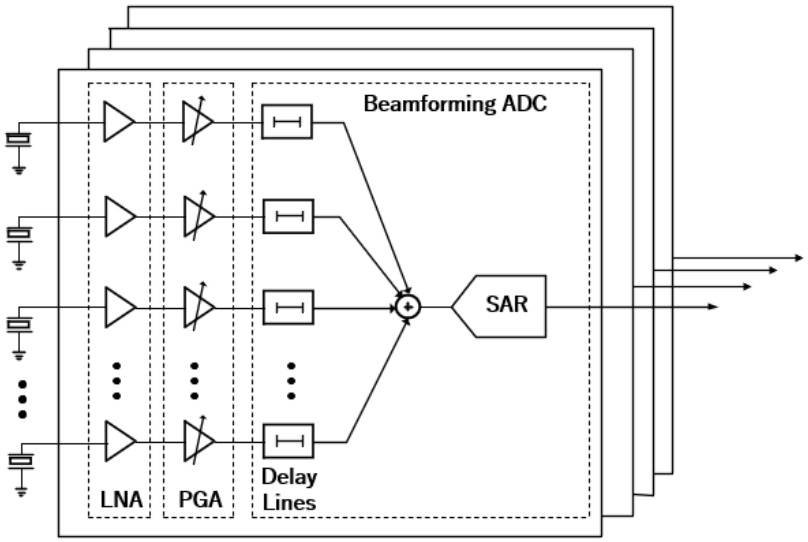


Figure 2.2: The subarray beamforming technique [3].

The digital beamformer operates the beamforming process in the digital domain at the back-end system. However, this requires one ADC per channel, imposing several constraints on both the area and power budget of each front-end. Thus, it comes to the biggest disadvantage that the digital beamforming system consumes a large amount of power when the A/D converter is power hungry. However, with the down

scaling of CMOS technology nodes, the A/D converter can be designed to be very power efficient. Besides, the power and area consumption of the ADC scales down with resolution decreasing. If the dynamic region of the channel is small, allowing a low resolution A/D converter to fully digitize the received analog signal. The total power and area consumption of signal chain and digitizer maybe be lower than the signal chain with the analog beamformer.

Another consideration is that the data routing may still be a problem if massive number of transducers are needed. The prior work solves the problem by using the multiplexer to combine some channels to minimise the total number of routing out cables [5]. The drawback of this implementation is the decreasing ratio of the routing-out cable also causes the imaging rate to be divide by the same ratio. Imaging the vagus needs to correct for movement of the nerve during neuromodulation. The movement of the vagus nerve primarily is related to the respiration, which is normally 20-30 times per minute for an adult [30]. This few seconds update interval makes a sufficient amount of time to fully receive the ultrasound echo sequentially by employing the multiplexer before the signal chain (Figure.2.3).

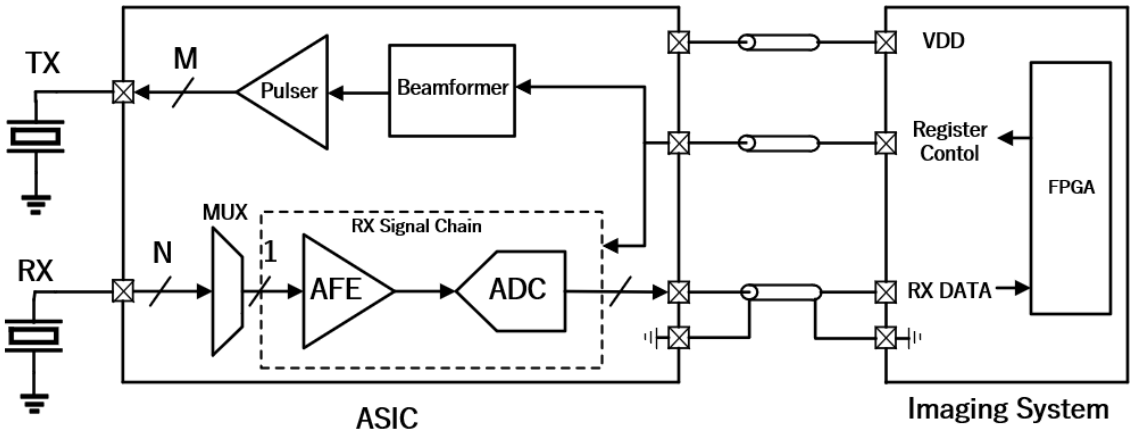


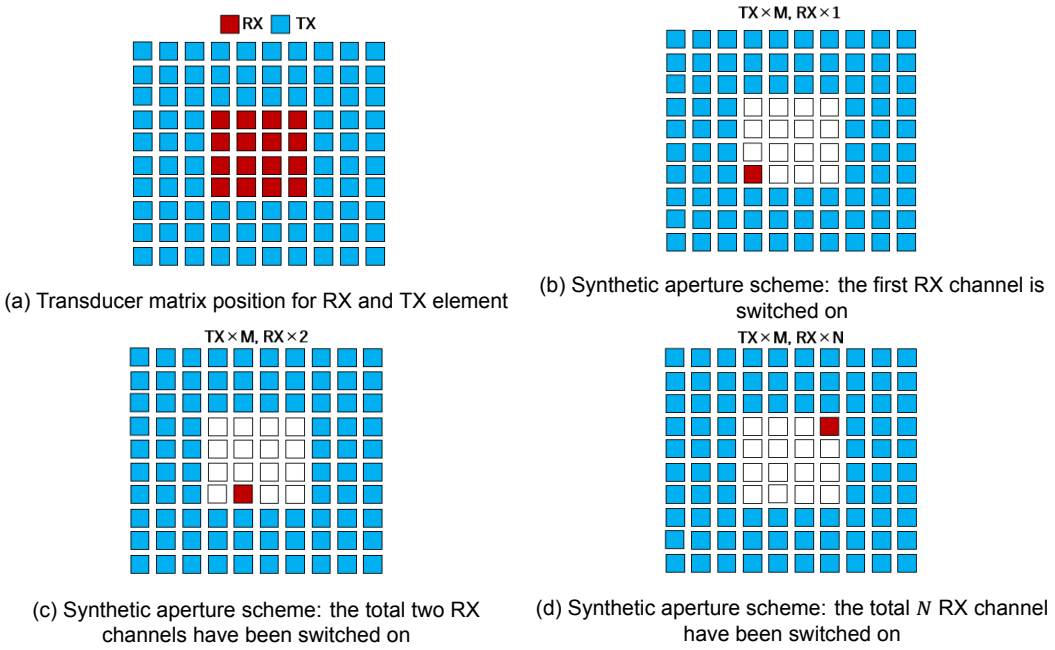
Figure 2.3: The proposed block diagram of the TX/RX system.

In this project, the primary challenge is the imaging quality. As some acoustic impedance figures are summarized in Table.2.1, the nerve and its contacting medium (soft tissue or blood) have the close acoustic impedance value. Based on the Equation.2.1, the ability of an ultrasound wave to transfer from one tissue type to another depends on the difference in impedance of the two tissues. If the difference is large, then the ultrasonic wave is adequately reflected. Comparing to the heart (1.89) or uterus (2.01) acoustic impedance, the received echo is smaller under the condition of vagus nerve modulation since the nerve has the close acoustic impedance value (1.75) comparing to the surrounding environment.

In order to have a high image resolution, the pressure intensity on focusing spot should be high, leading to the corresponding echoes also are stronger. Therefore, we designed to have the beamforming transmission circuit both for nerve stimulation and imaging to ensure the strong enough focusing pressure. Additionally, since the

Table 2.1: Sound velocity and acoustic impedance of some main mediums when engaging the vagus nerve modulation [13].

	Sound Velocity (m/sec)	Acoustic Impedance (10^6kg/m^2s)
water	1480	1.48
air	330	0.0004
blood	1570	1.61
fat	1450	1.37
muscle	1590	1.71
soft tissue	1540	1.62
nerve	1629.5	1.75
heart	1585	1.89
uterus	1629	2.01



(a) Transducer matrix position for RX and TX element

(b) Synthetic aperture scheme: the first RX channel is switched on

(c) Synthetic aperture scheme: the total two RX channels have been switched on

(d) Synthetic aperture scheme: the total N RX channel have been switched on

Figure 2.4: The example of the synthetic aperture scheme: the N RX channel is switched on sequentially and the total frame line is boosted into $M \times N$.

imaging frame-rate is relaxed, we could use the multiplexer structure to increase the frame line. As proposed in the recent work [5], the local digitization could work for the synthetic-aperture (SA) scheme. The synthetic aperture for a ultrasound imaging by the 2-D matrix transducer has been proved to be a good solution [31] [32]. Synthetic transmit aperture utilizes M number of transmit transducers (Figure.2.3) are all turned on while the sub-apertured number of N receive channels are receiving the echo. As shown in the Figure.2.4a, the position of the TX/RX transducer elements are partitioned into two parts: the RX channels are square-shape matrix at the center and TX channels are encircled the RX elements. The example synthetic aperture scheme can be seen as the Figure.2.4b-Figure.2.4d shows, the multiplexer sequentially turns on the RX from the first element to the final number N channel. This allows the total frame line to be boosted into $M \times N$, and accordingly, the DR of receive signals is dramatically increased. If employ the full phased SA imaging, the final SNR will be boosted by 20log$\sqrt{M * N}$ [5].

Compared with the sub-array technique (Figure.2.2), using the proposed local digitization with SA scheme imaging approach (Figure.2.3) directly brings four advantages:

- Good beamforming accuracy since the analog beamforming is heavily dependent on the matching performance.
- The analog beamforming in received signal chain will generate noise while the digital beamforming is noise-free.
- Instead of need a powerful A/D converter after each subarray chain and an analog beamformer block in very signal chain, the local digitizing may need less power and area since the requirement of the A/D converter is much relaxed.
- The much relaxed complexity of the circuit requirement, making the project objective reliable to achieve as we need massive number of transducer elements.

2.3. MATLAB Simulation

Ultrasound waves generated by the matrix of the 2-D transducers needs an accurate model to reflect the complex interactions with soft tissue. In this project we used the k-wave Matlab toolbox, which allows for spatio-temporal simulations of the propagation of ultrasound waves in heterogeneous media. A 3-D coordinate model is established, aiming for the most precise reflection on the in vivo neurolmodulation in the real environment. The Figure.2.5 illustrates the electrical pulse parameters and the matrix characteristics that will influence the the properties of the ultrasound focal spot, in terms of pressure, depth and spatial resolution.

Where the S_{res} is the focal spot diameter (later resolution) to image the vagus nerve. Considering the size of the vagus nerve, in order to properly image the boundary of the the vagus nerve system, the square resolution S_{res} is set to be hundreds of micrometer. The maximum focusing depth should cover the vagus nerve location.

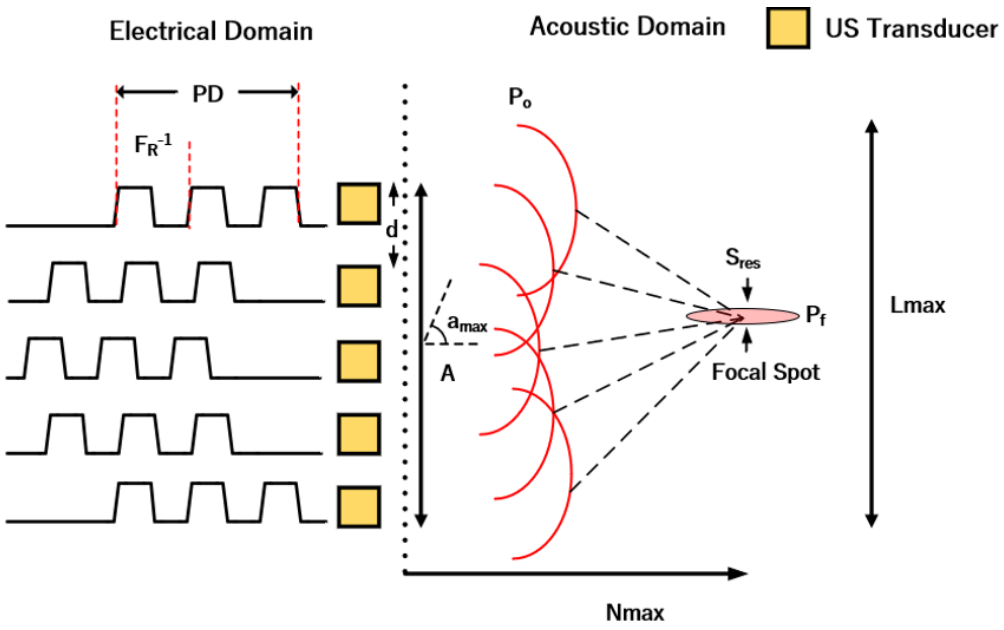
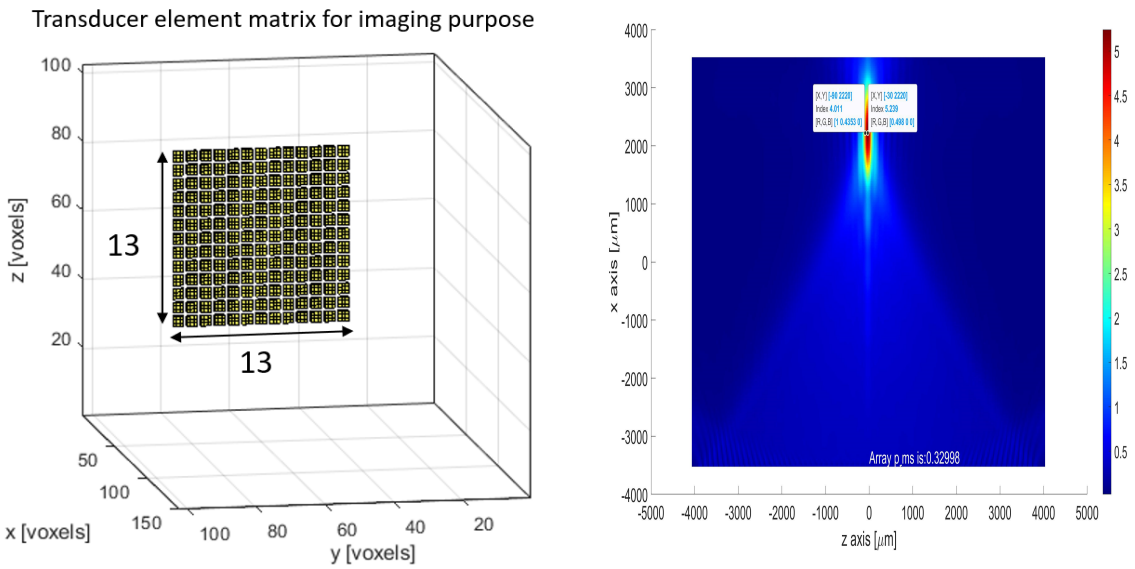


Figure 2.5: The parameters and factors effect the phased array focusing.

The average depth from epithelial tissue of the neck to left or right cervical vagus nerve is 7 mm [16], meaning the N_{max} to be at least 7 mm. The focused pressure P_{focus} should be at the region from 500 kPa to around 1 MPa for imaging purpose and over 1 Mpa for stimulation purpose [33]. d represents the pitch between transducers. It needs to be between $\frac{\lambda}{2}$ and λ in order to eliminate grating-lobes from appearing in the field of view of the image [3]. Based on the equations shown in the Figure.2.5, the ultrasound frequency (F_R^{-1}), the number of transducer element N and the total area of the transducer matrix A all decide the lateral resolution (S_{res}), focusing pressure (P_f) and focusing depth (N_{max}) .

In the real case of vagus nerve modulation and imaging, before the ultrasound wave is focused on the vagus nerve, it will encounter multiple layers including skin, fat, blood, soft tissue and the vagus nerve. Referencing to acoustic impedance values indicated in Table.2.1, parameters of different materials are set in the Matlab script code to mimic these medium layers. As the Figure.2.6 depicts, ultrasound waves are generated into the 3-D coordinates by a 2-D transducer elements. We have done the simulation for both nerve modulation and imaging purpose. This project is mainly responsible for the imaging setup. As seen from the Figure.2.6a, the 13×13 transducer elements matrix are used to generate the focusing spot. The Figure.2.6b shows the focusing ultrasound wave with the pressure index. The maximum pressure index locates at the center of the focusing beam. Based on the maximum value, the half value (-3 dB) of the pressure index represents the point where the pressured is halved. The distance between the -3 dB point and maximum centre spot represents the lateral resolution.



(a) The 13×13 transducer elements model in simulation.

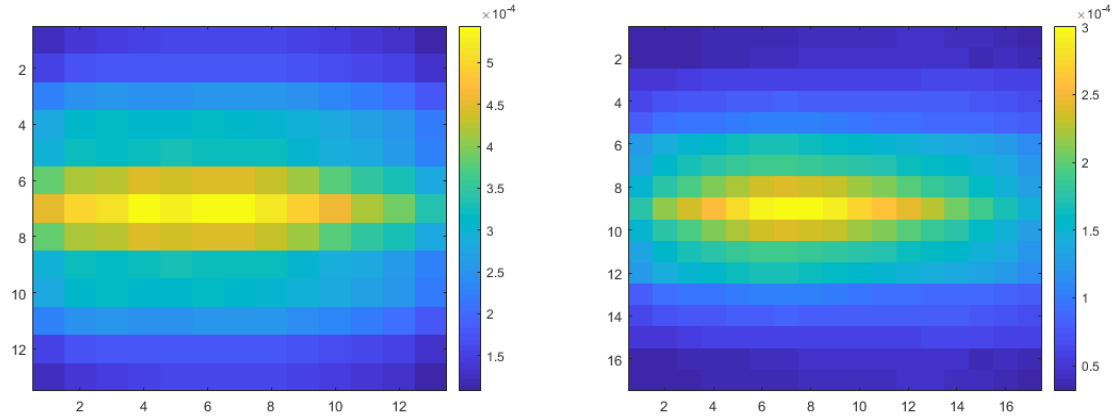
(b) The example focusing for nerve modulation purpose with the lateral resolution of 180 μm.

Figure 2.6: The 13×13 transducers for imaging and the focusing ultrasound waves.

The number of receiving transducer in the 2-D array is dependent on the wanted imaging quality. The imaging resolution is higher if the number of sensing transducer increases since the total scan line is enlarged if uses the synthetic aperture scheme. The Table.2.2 indicates the transducer specification in simulation for imaging implementation. In this project, in order to reach the imaging resolution pressure requirement, the 13×13 and 17×17 matrix arrays are tested. As the Figure.2.7 illustrates, the pressure index at individual element is recorded. In simulation, vagus nerve is located at the geometrical center of the square matrix with the 7 mm distance away from the array, therefore, as can be seen in the Figure.2.7, the maximum received pressure (plotted as yellow) is located at the center sensor elements. The pressure index recorded at each individual element can be used to calculate the electrical characteristics. This will be discussed in the next chapter.

Table 2.2: The summary of the MATLAB set-up requirements and the achieved conditions.

	Specification	**Value**
Imaging Implementation	Lateral Resolution	300-1000 μm
	Focus Depth	7 mm
	Focus Pressure	500kPa - 1Mpa
	Pitch distance	120 μm
	Transducer Length	90 μm
	Operation Frequency	12 MHz
	Number of element	13×13 17×17



(a) The 13×13 transducer elements senses the echoes.

(b) The 17×17 transducer elements senses the echoes.

Figure 2.7: The 13×13 transducers for imaging and the focusing ultrasound waves.

2.4. Sensing Material

The ultrasound transducer elements are operated based on the direct and reverse effects of piezoelectric materials, where an incoming pressure wave at the face of the transducer generates an electrical signal, and a driving electrical signal generates a pressure wave. Consequently, as the important part of the ultrasonic transducer, the properties of the piezo-materials dominate the transducer performance such as the generated wave pressure and received signal features such as the bandwidth and sensitivity.

Conventionally, the piezoelectric lead zirconate titanate (PZT) ceramic is the most widely used in the fabrication of ultrasonic transducers for the medical imaging. However, this material is limited by the lower longitudinal piezo-electrical coupling constant d_{33} (500-900 pC/N) and the electromechanical coupling coefficient k_{33} (<0.7) [34]. The d_{33} is the conversion ability of the vibration force produced by the material to charge. The k_{33} is the mechanical energy to electrical energy conversion efficient coefficient. If these two factors are low, means that it would be hard to improve the transducer sensitivity and image resolution.

More recently, binary relaxor-based ferroelectric single crystals $Pb(Mg_{1/3}Nb_{2/3})O3-PbTiO_3$ (PMN-PT) with compositions around the morphotropic phase boundary (MPB) have attracted considerable attention due to its better piezo-electrical coupling constant d_{33} and electromechanical coupling coefficient k_{33} (The average value: d_{33}= 2000 pC/N, K_{33}=0.92) [33]. Past few years, the fabrication of the PMN-PT improved a lot that the not only the single PMN-PT crystal has higher sensitivity, but also have the uniformly properties performance on 1-D and 2-D arrays [33]. Considering the weak echo signal based on the Matlab simulation result, the advanced PMN-PT material is the best choice to have a good imaging quality. The detail information of the received echo signal in electrical domain will be discussed in the chapter 3.

3

Signal Conditioning

Following the previous system-level considerations, this chapter introduces the design of the analog front-end (AFE) electronics circuit for interfacing the PMN-PT transducer. It consists of three major parts: the received PMN-PT electrical signal will be investigated at the first section. Then the second section is the design consideration of LNA. Lastly, the TGC system design and the whole analog signal chain is discussed.

3.1. Piezo-material Property

3.1.1. Transducer Geometry

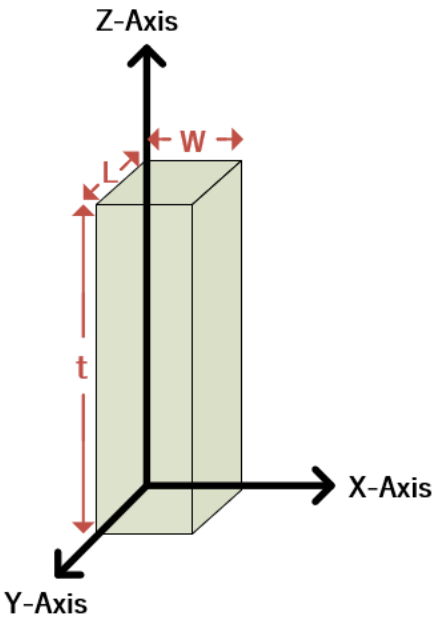


Figure 3.1: The TE-mode resonator.

Piezoelectric materials are anisotropic that their geometry mode is a 3-D block and it parameters are expressed in matrix notation. For a typical piezo-materials that are applied in imaging operation, the length extensional-mode (LE) is generally utilized as the Figure.3.1 depicted [35]. The LE mode occurs when the length L and width W are much smaller than the thickness t. The X-Y-Z coordinates plotted in the Figure.3.1 are indicated by the number 1, 2, 3 in equation. The subscript represents two associated quantities. For example, the PMN-PT d_{33}, the first subscript represents the induced polarization in the 3(Z) direction and the second one is the mechanical response in the 3(Z) direction. Many properties could be measured on a 3-D transducer. Among them, three of the material properties are the most critical in the ultrasonic transducer design [35] [36]:

$$C_{33}^{S} = \frac{\epsilon_{33}^{S} A}{t}. \tag{3.1}$$

$$f_0 = \frac{C_p}{t}. \tag{3.2}$$

$$k_t^2 = \frac{\pi}{2}\frac{f_o}{f_a} tan(\frac{\pi(f_a - f_r)}{2f_a}). \tag{3.3}$$

Where the C_{33}^{S} is the clamped parasite capacitance; ϵ_{33}^{S} is the dielectric permittivity; A is the surface area; t is the thickness of the transducer; f_r is the resonance frequency; c_p is the ultrasonic propagation speed inside the transducer; f_a is the anti-resonance frequency and k_t is the thickness-mode electromechanical coupling coefficient.

The piezoelectric materials can be seen as a capacitor and a resonator. The capacitance and resonant frequency is dominant by the clamped capacitor C_{33}^{S} and resonance frequency f_o respectively. And based on the Equation.3.1 and Equation.3.2, these parameters are decide by the W, L and t of a transducer. Besides, the electromechanical coupling coefficient k represents the effectiveness of the piezo-material converting electrical energy into mechanical vibration energy and vice versa. It is also influenced by the shape of the transducer. The LE-mode has the best shape structure to work as the transducer since its W, L and t are decided to have a high electromechanical coupling coefficient k_t.

3.1.2. Electrical Model

The Butterworth-van Dyke lumped-element impedance model is a reliable electrical model to mimic the characteristics in electrical domain of the piezo-material transducer, and has been used successfully [4].

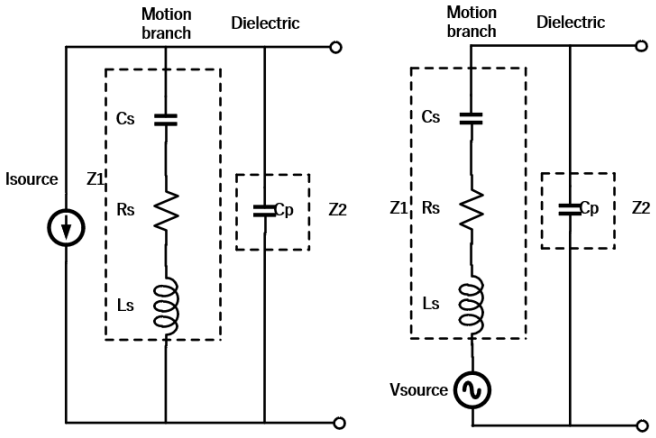


Figure 3.2: The transducer electrical model: the current source type (left) and the voltage source type (right). [4]

As the Figure.3.2 shows, it consists of a series of RCL branch, (R_s, C_s, L_s) that represents the mechanical part of the transducer and a shunting capacitor (C_p) that mimics the dielectric property. The RCL branch is called the motion branch, representing the piezo-material transducer's vibration performance. The impedance $Z1$ is formed by the RLC resonance tank and it is associated with the piezo-material physical properties. The resonance frequency is expressed as:

$$f_{resonance} = \frac{1}{2\pi\sqrt{L_s C_s}}. \tag{3.4}$$

The exact electrical property of the PMN-PT transducers is decided by the manufacture and transducer size. The following table shows some critical properties that we need to calculate the electrical property from the CTS corporation [14]. The data is the typical value of the product of the PMN-28% PT.

Table 3.1: Some important properties of the PMN-28% PT from CTS [14].

Property	Symbol	Units	Value
Piezoelectric Constants	d_{33}	pC/N	1350
Size	A	mm^2	0.0081
Dielectric Constants	ϵ_{33}	(ϵ_o)	5000
Wave Speed	c_p	m/s	4000

By adjusting the thickness of the transducer as the Equation.3.2 indicated, we could force the PMN-PT transducer to vibrate at 12 MHz. Based on the Table.3.1 shows, the ultrasonic speed in the transducer c_p is 4000m/s, the thickness t is calculated to be 330 μm. The C_s, L_s and R_s form the impedance spectrum with the centre operation frequency designed at 12 MHz. At the resonance frequency, the impedance

$Z1$ is dominated by the R_s, which its expression in LE structure is calculated as the Equation.3.5 shows [37].

$$R_s = \frac{|Z|_{\min}}{\sqrt{1 - \omega_0^2 C_0^2 |Z|_{\min}^2}}. \tag{3.5}$$

Where the $|Z|_{\min}$ is the minimum modolus value of the impedance and ω_0 is the series resonance angular frequency. Comparing with the PZT transducer, the value R_s in PMN-PT has the similar value which is normally larger than 30 KΩ [37]. However, for the impedance quality factor, the PMN-PT shows a over 50% less Q-factor value [37]. The Q-factor decides the frequency bandwidth and it is determined by the manufacture precision and material composition. In this design, we considered the worst condition of a maximum 50% frequency shift which results in the bandwidth is from 6 MHz to 18 MHz. The dielectric branch represents the parasitic capacitor C_p. It is related to the relative dielectric constant of the piezo-material that is in application. The C_p' expression is derived as:

$$C_p = \epsilon_o \epsilon_\phi \frac{A}{\frac{c_p}{f_0}}. \tag{3.6}$$

The ϵ_o is the vacuum dielectric and ϵ_ϕ is the relative dielectric constant, both indicated in the Table.3.1. The calculated parasitic capacitor C_p is approximately 5 pF. As the previous chapter introduced, the PMN-PT has has gained its interest for its high charge displacement property d_{33} comparing to other piezo-materials.

The model in Figure.3.2 can be transformed into a Thévenin equivalent circuit as shown in the Figure.3.3. The AC current source, I_{source}, is generated by the charge displacement factor, d_{33}, of the PMN-PT material. As the previous chapter introduced, the PMN-PT piezo-material has the best charge generation ability comparing to other capcitive micro-machined ultrasound transducers (CMUT) and piezoelectric micro-machined ultrasound transducers (PMUT). The generated current/charge and equivalent impedance Z_{source} is expressed as:

$$\begin{aligned} I_{source} &= \frac{d_{33} \times F_{echo}}{\Delta t} \\ Z_{source} &= \frac{1}{sC_p} \parallel R_s. \end{aligned} \tag{3.7}$$

Where the F_{echo} is the received echo ultrasound signal, as the previous chapter explained, it is derived from the MATLAB simulation. At the 12 MHz center frequency, the impedance generated by the C_p is around 2.5KΩ, which is 20 times smaller than the R_s. This case, it is can be assumed that the Z_{source} is dominated by the parasite capacitance C_p, which is 5 pF.

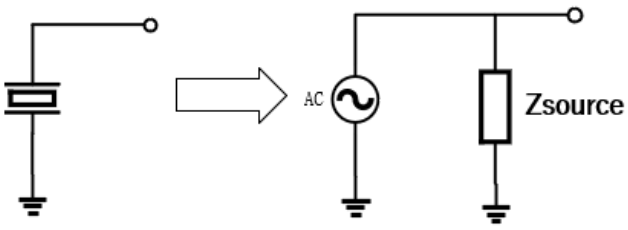


Figure 3.3: The Thévenin equivalent circuit for the received ultrasound signal.

3.2. Analog-Front-End Architecture

The transducer resonance frequency is around 12 MHz and the impedance at the operating frequency is approximately 2.5 $k\Omega$. The transducer source is seen as a charge source. In order to readout the generated charge from the transducer, a charge amplifier is required to transfer the charge into the voltage. A charge amplifier takes advantage of the high charge sensitivity of PMN-PT. As the Figure.3.4 shown, the AFE is responsible for transferring the received echo signals to the imaging system. As the previous chapter introduced, instead of using analog beamformer approaches, digitizing the echo signal locally to reach the maximum energy and area efficiency.

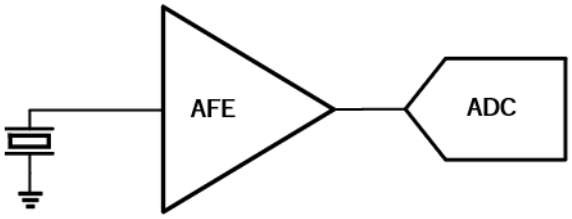


Figure 3.4: The block diagram of the signal chain.

The AFE circuit amplifies the echo signal with a programmable gain to match it to the input range of the ADC. In order to be convenient to evaluate the noise, gain and voltage swing, we use a voltage model for the piezo-material. Hence, the voltage swing of the received signal is expressed as the generated charge divided by the parasitic capacitance:

$$V_{echo} = \frac{d_{33} \times F_{echo}}{C_p} \tag{3.8}$$

The gain of the AFE is determined by the system input referred noise and the maximum input signal swing V_{echo}. The total input referred noise from the signal chain consists of two parts: amplifiers and the A/D converters noise, which is expressed as:

$$V_{n,signalchain}^2 = V_{n,AFE}^2 + \frac{V_{n,ADC}^2}{A^2}. \tag{3.9}$$

Where $V_{n,signalchain}$ is the input referred noise, $V_{n,AFE}$ is the input referred noise from the AFE, $V_{n,ADC}$ is the A/D converter noise and A is the gain of the AFE. The noise of transducers is primarily from the resistor R_s in the lumped-element impedance model (Figure.3.2). This means the noise from the resistor R_s is 4.8 μ V_{rms} . Based on results of the pressure index from Matlab simulation at each individual transducer element, we could find out the voltage swing range is from 0.4 mV to 1 mV. Therefore, the AFE should read out the 0.4 mV amplitude signal and sends it into the ADC. Designing a ADC with a small full scale range is very challenging because the small scale range of ADC leads to the small LSB, meaning that it may need powerful and complicated topology under the condition of small LSB value. Considering the 1.8 V supply voltage, in order to relax the ADC design to save the power and area, the 1 V input range is a reasonable value. This case, the minimum gain of the signal chain is set to be 1250 (62dB). Therefore, the quantization noise $\sqrt{1/12}\ V_{LSB}$ from a 6-bit ADC is approximately 4.5 m V_{rms}. The quantization noise is referred at the transducer side is attenuated by the AFE gain, which is 3.6 μ V_{rms}. This causes the noise from the A/D converter is smaller than the transducer noise.

$$V_{n,ADC} = \frac{V_{n,ADC}}{1250} = 3.6\mu V < V_{n,transducer} \tag{3.10}$$

However, the noise from the charge amplifier can not be neglected considering the received voltage swing is weak. The later section will show that the input referred noise from the AFE ($V_{n,AFE}$) is larger than the transducer noise ($V_{n,transducer}$) and the input referred quantization noise ($V_{n,ADC}$). This calls for the special consideration to design the charge amplifier since its noise performance will dominate the dynamic range of the signal chain.

To properly design the LNA with the noise and power trade-off consideration, the investigation on the transducer characteristic and the requirement on the output signal type is needed. Depending on the transducer, the amplification typologies are divided as a voltage gain, a current gain, a trans-impedance gain or a trans-conductance gain. The previous section tells that the parasite capacitance of the PMN-PT transducer is the dominate impedance source, and the final output wanted signal is the voltage signal that needs to be digitized. Therefore, the LNA interfaced with the transducer can be modelled as a Capacitive-Feedback Voltage Amplifier (CFA) structure.

As shown in the Figure.3.5, the ideal voltage amplifier has a voltage gain of G_V, an infinite input impedance and the input-referred noise V_n^2. A large feedback resistor for the DC biasing purpose is omitted. The input-referred voltage noise of the CFA can be expressed as:

$$V_{n,in,CFA}^2 = \left(1 + \frac{C_F}{C_I}\right)^2 V_{n,OTA}^2 \tag{3.11}$$

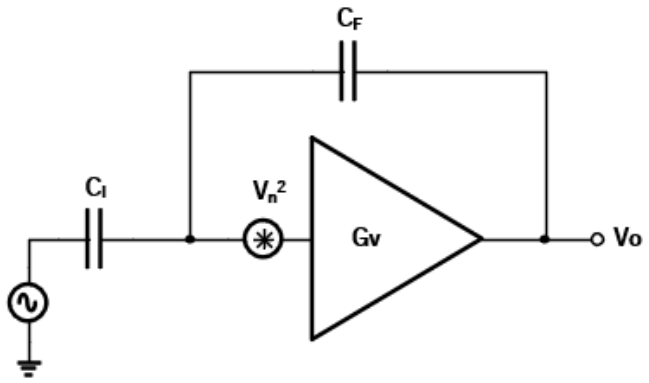


Figure 3.5: The Capacitive-Feedback voltage amplifier as the LNA interfaces the transducer.

The noise gain factor $1+\frac{C_F}{C_I}$ will increase the noise to the transducer from the OTA noise. It proves that in order to decrease the noise gain factor, a large mid-band gain $\frac{C_I}{C_F}$ is needed. The bandwidth of the CFA is approximately expressed as:

$$\mathrm{BW}_{CFA} \approx \frac{g_m}{2\pi C_I C_L / C_F} \tag{3.12}$$

where g_m is the transconductance of the OTA and the C_L is the load capacitance.

3.2.1. Full Structure and OTA Considerations

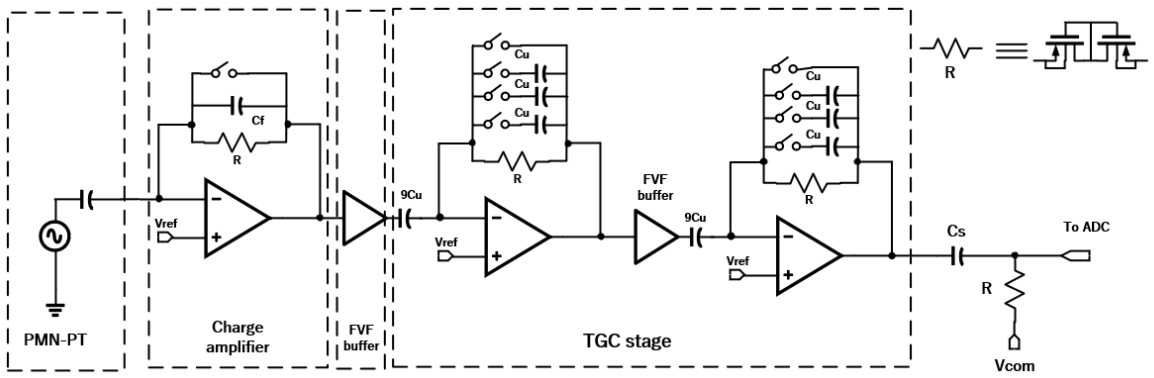


Figure 3.6: The schematic of the overall signal chain before the ADC.

Figure.3.6 depicts the overall analog front end function block. The V_{com} is 500 mV to provide the common voltage in order to obtain the full range of the ADC, which is from ground to 1 V. The resistance R is pseudo-resistor structure, and the DC blocking capacitor C_s with the value of 800 fF to ensure the fast settling time for the signal to have the swing from 0-1V with 500 mV common-mode voltage at 12MHz. This signal chain processing can provide up to 62dB voltage gain. The large final swing can relax the design requirement on the ADC stage. The buffer stage is used to isolate

each OTA network. The circuit implementation design of each block and reasons for choosing this structure will be introduced in the later sections.

The available architectures for the OTA include telescopic, folded cascode and inverter based OTA. Because the single-ended nature of the transducer elements, the common ground electrode can be shared by all elements. Therefore, the single-ended signal is the prior choice because the differential-ended input requires more power and its benefit is the lower harmonic distortion [5]. Since the high frequency harmonic distortions are out-of-band and will be filtered out by the OTA bandwidth, the single-ended amplification structure is selected.

The inverter-based OTA is already used in the previous works as the Figure.3.7 shows, the differential topology is used to increase the power supply rejection (PSR) and the single topology with the split capacitance feedback network. Comparing to the differential one, the single-ended inverter-based OTA uses half branch of current. In order to have the same PSR performance as the differential one, two regulators are used as the Figure.3.7b depicted. But the price is much more area consumption on the split capacitors structure and two more regulators [5] [6].

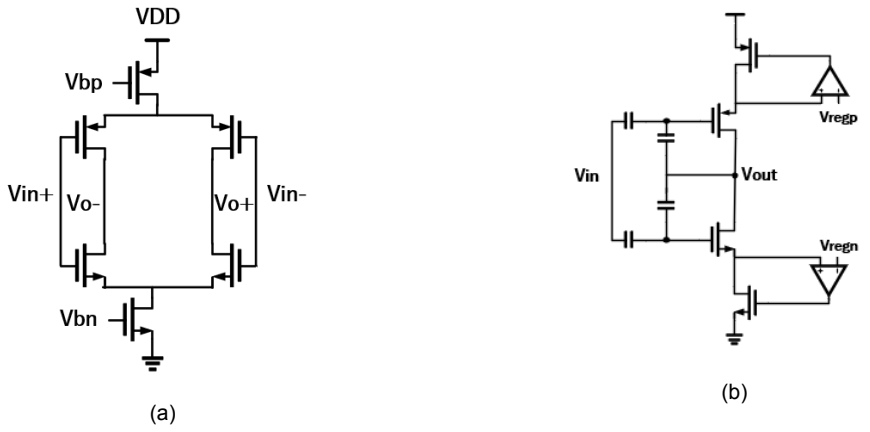


Figure 3.7: (a) The differential inverter-based OTA [5]. (b) The single-ended inverter-based OTA [6].

The above mentioned two structures are both limited by their available input range and output range. The limited input and output voltage swing constrains the available dynamic range of the the B-Mode ultrasonic imaging system. The reason is that the object that close to the transducer will generate a large echo signal. The close range of objects that are beyond the available input and output ranges of the OTA are unable to be distinguished by the B-Mode imaging algorithm. This case, the differential folded-cascoded OTA has the maximum input and output range among all these typologies. Besides, the folded structure achieves better PSR performance. However, the drawback is the standard differential folded-cascoded OTA does not have a good transconductance efficiency that may need more power to compensate for the same noise efficiency performance. To overcome this, a special power-saved design consideration is needed.

3.3. OTA Design

3.3.1. Folded Cascode

The schematic of the low-noise OTA is shown in Figure.3.8. It is a standard version of a folded-cascode topology. The OTA in Figure.3.8 is biased such that the currents of the transistors in the folded branch $M4$-$M9$ are only a small fraction of the current in the input differential pair transistors $M1$ and $M2$. For a standard folded-cascode topology, the current from the power supply, I_p, should be more than 2 times larger than the tail current I_{tail} to ensure the folded branch still has current if the input side has a huge step response. Besides, this also ensures the symmetric output swing [38]. In this design, the swing from the transducer is sinusoidal, without big transition signal, therefore the folded branch current is scaled to only $\frac{1}{3}$ of the current in $M1$ and $M2$. This directly takes two benefits: we scale down the power consumption simultaneously make the noise contributions from transistor $M4$ and $M5$ smaller. To maximize the G_m of the OTA, the NMOS transistors are selected because their higher electronic mobility. The benefit of using PMOS is less flicker noise, but the flicker noise (up to hundreds KHz) is out of our signal band (6M-18MHz) that can be filtered out after the digitization.

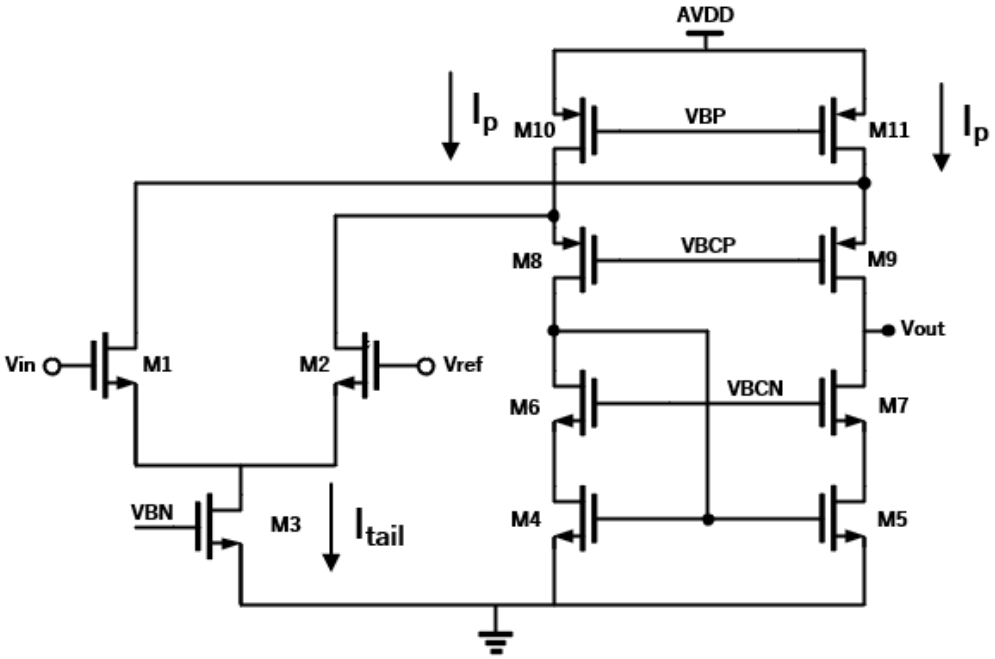


Figure 3.8: Schematic of the low-noise OTA used in the design.

The noise performance of the differential folded cascode OTA is not good as the inverter-based OTA. Not only the input transistors, the transistors $M5$ and $M11$ also generates noise to the output. The noise from the cascode stage $M_{6,7}$ and $M_{8,9}$ is

attenuated by the factor of $\frac{1}{(1+g_m r_o)^2}$, where the $g_m r_o$ is the intrinsic gain of the non-cascode transistor. Thus, the noise contributions from the cascode transistors are omitted. The input referred noise can be expressed as:

$$\overline{v_{n,in}^2} = \frac{8KT\gamma}{g_{m1}}\left(1 + \frac{g_{m5}}{g_{m1}} + \frac{g_{m11}}{g_{m1}}\right). \tag{3.13}$$

The Equation.3.13 tells that to minimize the input referred noise, the transconductance of $M5$ and $M11$ should be small. The available output swing is expressed as:

$$\begin{aligned} V_{\text{out(max)}} &= V_{DD} - V_{SD11} - V_{SD9} \\ V_{\text{out(min)}} &= V_{DS7} + V_{DS5} \end{aligned} \tag{3.14}$$

The OTA is designed to work for both the LNA and TGC stage. Therefore, the output swing should reach 1 V because the ADC has the 1 V scale range. The appropriate solution is that the $V_{SD11} + V_{SD9}$ and $V_{DS7} + V_{DS5}$ both have 400mV range that enable the output swings from 400mV to 1.4V with the common-voltage 900 mV. Equation.3.15 tells that a larger V_{DS} decides a smaller gm, thus the V_{DS5} and V_{DS11} are set to be 300 mV and V_{DS7} and V_{DS9} are set to be 100mV for the noise optimization design.

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}. \tag{3.15}$$

In order to ensure the enough bandwidth of the OTA, the input transistors should have the sufficient current. The final 60 μA current is selected as the input pairs operating current and the folded branches have 20 μA.

Table 3.2: The size, saturation current and over-drive voltage of transistors.

Transistor	I_D[μA]	V_{OD}[mV]	$\frac{W}{L}$[μm]
$M_{1,2}$	60	80	60/1
M_3	120	100	120/2
$M_{4,5}$	20	300	8/4
$M_{6,7}$	20	100	17.4/1
$M_{8,9}$	20	100	22.2/0.5
$M_{10,11}$	80	300	25/1

The -3 dB point of this OTA is designed to be beyond 20 MHz to cover the signal frequency range (6MHz - 18MHz). Thus, the phase margin needs be specially considered. The major second pole of the folded cascode topology is located at the folded node, the source of transistors M_8 and M_9. It relates to all parasite capacitance at the folded node and the transconductance of M_8 and M_9. The second pole is expressed as the Equation.3.16. Therefore, the length of M_8 and M_9 is 0.5 μm to shrink the overall size and further decrease the C_{GS9}.

$$P_{secondpole} \cong \frac{g_{m9}}{C_{GS9} + C_{DB1} + C_{DB11}}. \tag{3.16}$$

3.3.2. Biasing Network

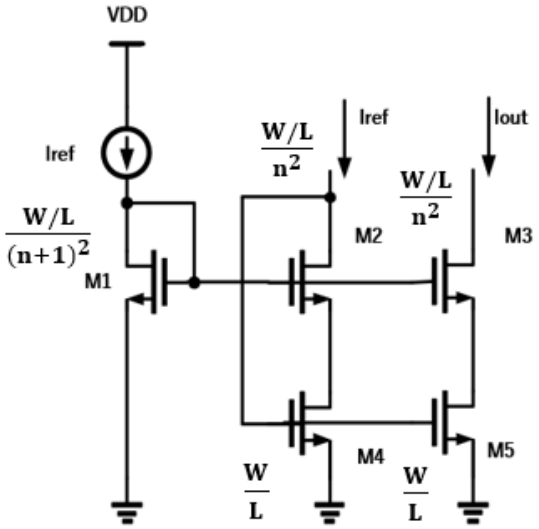


Figure 3.9: The wide swing cascode biasing topology.

The cascode stage should have the wide swing biasing voltage to ensure the available maximum output. The classic wide swing cascode biasing network is shown as the Figure.3.9. The size difference between M_1 and M_4 makes their over-drive voltage different:

$$V_{OD1} = (n+1)V_{V_{OD4}}. \tag{3.17}$$

Then, the cascode biasing voltage is expressed as:

$$\begin{aligned} V_{G1} &= V_{OD1} + V_T \\ &= (n+1)V_{OD4} + V_T. \end{aligned} \tag{3.18}$$

The source voltage of M_2 is:

$$\begin{aligned} V_{G1} &= V_{G2} - V_{GS2} \\ &= (n+1)V_{OD4} + V_T - (nV_{OD4} + V_T) \\ &= V_{OD4} \end{aligned} \tag{3.19}$$

Where the outcome is exact value of the over-drive voltage of the M_4. Because the current mirror effect, the transistor M_5 has the same size ratio and current with the M_4. Thus the V_{OD5} equals to the V_{OD4}, and the final output at the drain node of M_3 has its minimum available output:

$$\begin{aligned} V_{D3}(min) &= V_{G3} - V_T \\ &= (n+1)V_{OD4}. \end{aligned} \tag{3.20}$$

In our design, the V_{OD4} is 300mV and n is $\frac{1}{3}$. The Equation.3.20 tells us the calculated minimum output is: $\frac{4}{3} \times 300mV$, which equals 400mV. This value follows our design. The PMOS folded stage side has the same procedure.

3.4. Schematic and Post-layout Simulation Results

3.4.1. OTA Layout

The Figure.3.10 depicts the final layout of the folded cascode OTA. The input pair should have good matching performance to alleviate the offset voltage. Therefore, the input transistors M_1 and M_2 are used common-centroid placement. It will ensure the transistors M_1 and M_2 have the same doping shift effect. The place arrangement of transistors is designed to be compact and symmetric in order to have small overall size and good matching performance. As the Figure.3.10 shown, the wire distance on each folded branch is approximately the same due to the symmetric arrangement. This ensures that there is no pole discrepancy within the major unity gain frequency. The guarding ring is added to enable each pair of transistors to work under a isolated environment and prevent the latch-up effect. The total consumed area is: 53.24 μm ×42.89 μm = 2230 μm^2.

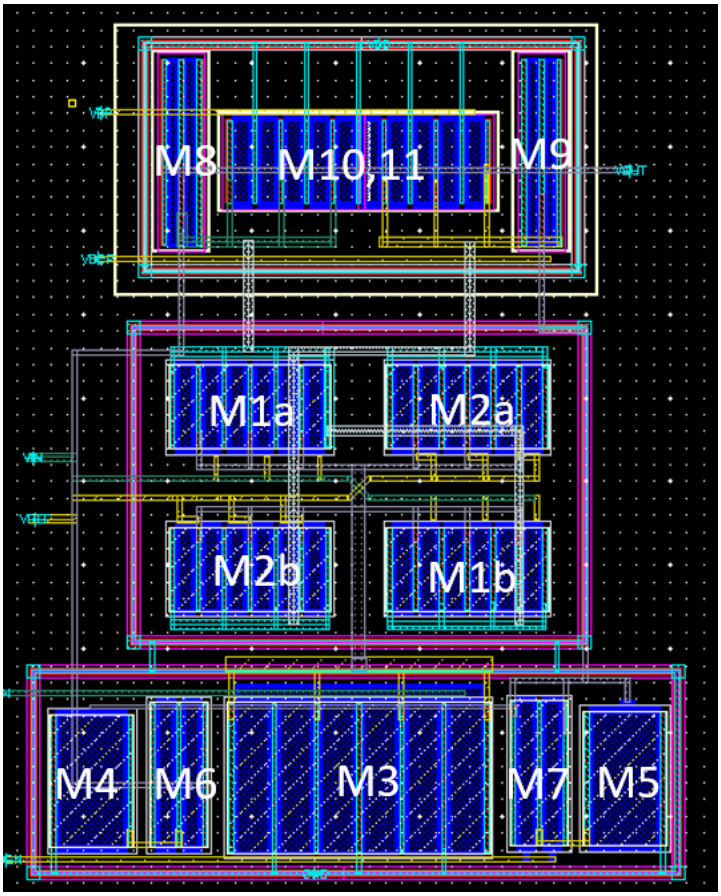


Figure 3.10: The low-noise OTA layout.

3.4.2. Schematic and Post-layout Simulation Comparing

As seen from the Equation.3.11, the value of the feedback capacitance affects the input-referred noise of the capacitive-feedback OTA topology. A smaller C_F leads to a lower input-referred noise since it provides with a higher amplifier gain. Considering the parasites capacitance at the input and output node of the OTA, the feedback capacitance should remain not too small if the gain accuracy is not heavily affected. The C_F is set to be 265 fF, designing for have 17 (25dB) amplitude gain at the low-noise amplification stage. As the Figure.3.11 depicted, the pseudo-resistor that has a resistance in the Giga-ohm range to offer the DC biasing. The pseudo-resistor also forms a high-pass pole at the low frequency range, and the pseudo-resistors are heavily PVT dependant. However, the corner simulation shows that the shifted range of the high-pass pole due to the temperature and process variation varies from few hertz to few hundreds hertz. This shift still is far smaller than the signal frequency. The V_{ref} voltage equals to half of the supply voltage V_{DD}, forcing the common mode voltage at the output node to be the same as the V_{ref}.

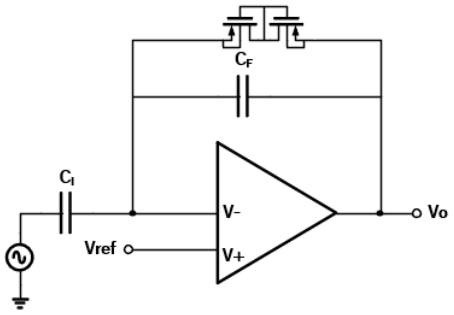
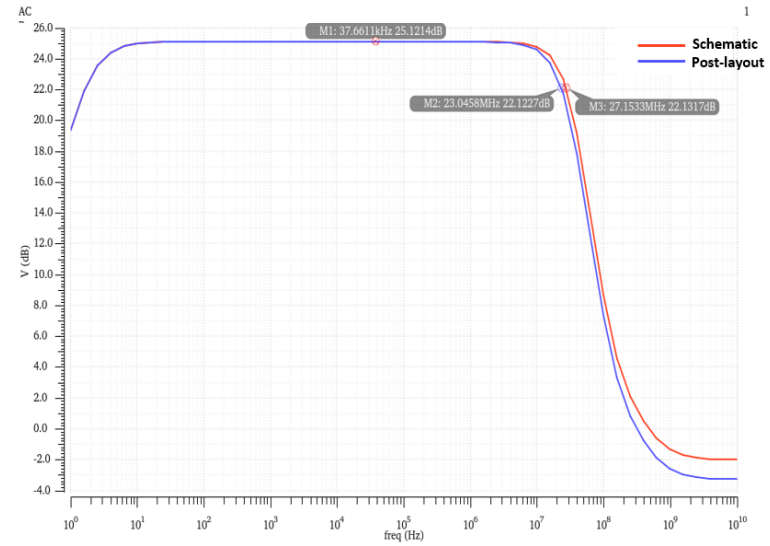


Figure 3.11: The pseudo-resistor structure offers the DC biasing.

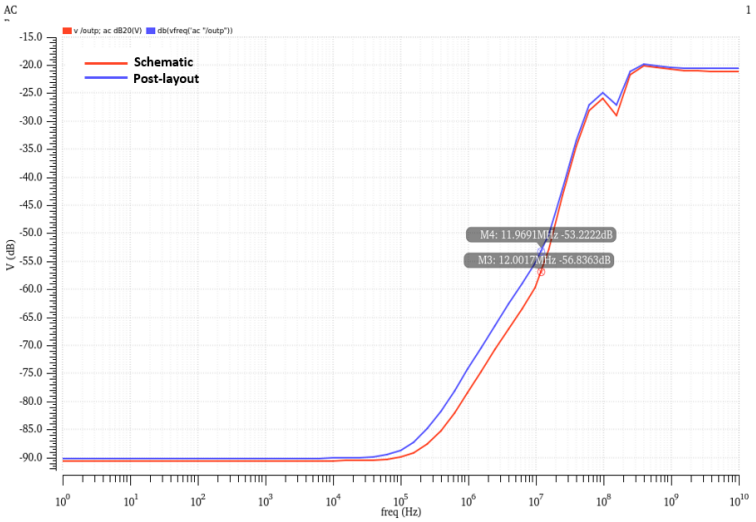
The post-layout simulation shows little difference comparing with the schematic simulation. As the Figure.3.12a shows, the close-loop simulation result indicates that the 25 dB gain holds to the 12 MHz and the -3 dB pole is still beyond 20 MHz in the post-layout simulation result. Both schematic and post-layout results meet our requirements. The Figure.3.12b indicates the power rejection performance of the OTA. The post-layout simulation shows that the power gain is less -50 dB at 12 MHz and -90 dB at DC. This result is also close to the schematic simulation.

Some other specifications from the post-layout simulation of the folded cascode low-noise amplifier is summarized at the Table.3.3. The offset voltage is measured by the Monte Carlo mismatch and process variation simulation.

To compare the power-noise trade-off among amplifiers, the Noise Efficiency Factor (NEF) parameter is widely used to compare the low-noise amplifier designs [39]:



(a)



(b)

Figure 3.12: (a) The close loop simulation results. (b) The power rejection performance simulation of the OTA (without capacitive network).

Parameter	Result
Supply voltage	1.8 V
Total Current	155.4μA
DC gain	79 dB
Bandwidth	21 MHz
Input-referred noise (6M-21M)	29 μV
Phase margin	50.72 Deg
Unity gain frequency	143.63 MHz
Offset voltage	12μV

Table 3.3: The post-layout simulation results.

$$\text{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{3.21}$$

where $V_{ni,rms}$ is the total input-referred noise, I_{tot} is the total supply current, and BW is the -3dB bandwidth respectively. Because the filtering work will be done on the signal, the noise that outside this signal band is neglected. The signal band is from 6M to the -3dB frequency 21 MHz, and the RMS input-referred noise in this frequency range is 29 μV. The I_{tot} is 155.4 μA and the BW is 12 MHz range. The calculated NEF is 3.61. Comparing with the received echo signal at the transducer, the input-referred noise from the low-noise amplifier is the dominant noise source, as the 29 μV is much larger than the transducer noise 4.8 μV and the input-referred quantization noise 3.6 μV. The maximum DR of the received signal is calculated as: $20log(\frac{1\times10^{-3}}{37\times10^{-6}}) = 29dB$.

3.5. Time-Gain-Compensation (TGC) Design

3.5.1. TGC Principle

When the ultrasonic wave is transmitting in the tissue, the power losses due to medium attenuation and wave spreading will occurs. As the Figure.3.13 shows, with the wave propagation, the received echo has different amplitude. Dependent on the distance, the closer target generates larger echo amplitudes [40]. In other word, the received signal will decrease with the propagation time or distance. The TGC stage is used to compensate this attenuation, by employing a gain stage increase with the time. The attenuation factor is medium dependant, for example, the average attenuation factor in blood is $0.2dB/cm/MHz$, in the fat is $0.38dB/cm/MHz$ and in muscle is $0.62dB/cm/MHz$ [13].

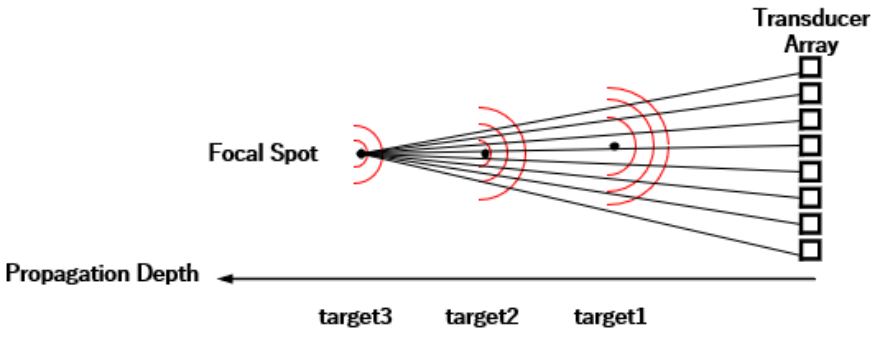


Figure 3.13: The principle of the received echo as the signal propagation into the focal spot.

In order to maintain the uniform image, the overall gain including the low-noise stage and the TGC stage should meet the full scale range of the ADC. The full range of the ADC is 1 V and the sinusoidal echo received at the transducer is ranged from 0.4 mV to 1mV. This means the overall gain should have the variable gain up to 1250

(62dB). The ideal TGC stage is formed by the OTA with the continuously linear increasing gain, shown as the Figure.3.14a. It needs a powerful exponential gain increasing property that draws too much current and takes a lot of area. Similar proposed in [5], the discrete gain step are applied to form the TGC stage. As the Figure.3.14b depicted, the compensated signal forms the saw wave and its fluctuation distance is dependant on the discrete gain interval. Since the vagus nerve is the primary target, the mediums in between do not need care about. So, our TGC is discretely controlled, since we only need to get echoes from structures around the vagus nerve. The non-exponentially increasing gain in TGC could heavily relax the circuit design requirement and hence saves power and chip area.

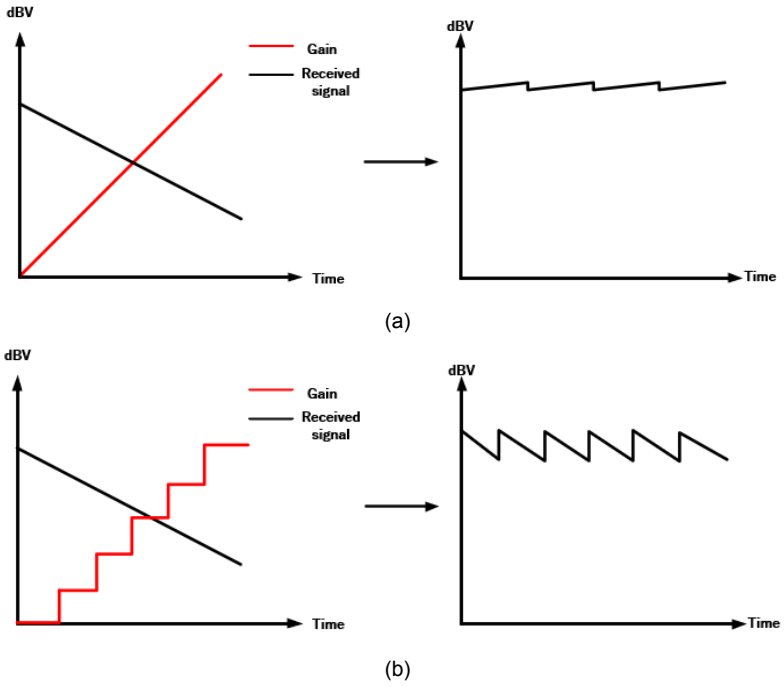


Figure 3.14: (a) The ideal time gain compensation. (b) Time gain compensation with 3 discrete gain steps.

The low-noise stage already has a gain of 17. In order to have the overall 1250 gain stage, the TGC has to offer the rest 80 (38dB) gain. It means for a voltage feedback OTA, a single stage OTA needs a large area to construct the capacitive gain network. In this case, this design uses two cascade OTA to produce the 80 gain. One of the first stage is shown as the Figure.3.15. It uses the smallest unit capacitance to have the maximum gain of 9. Two cascade stages will have the maximum gain of the needed 80. For the gain accuracy purpose, the unit capacitor is set to be 85fF. Based on the switch control, one stage can produce gain of 1 by bypassing the OTA stage, 3 by having all capacitors in parallel, 4.5 by having 2 parallel unit capacitors in the feedback and the maximum gain of 9 by using only one unit capacitor.

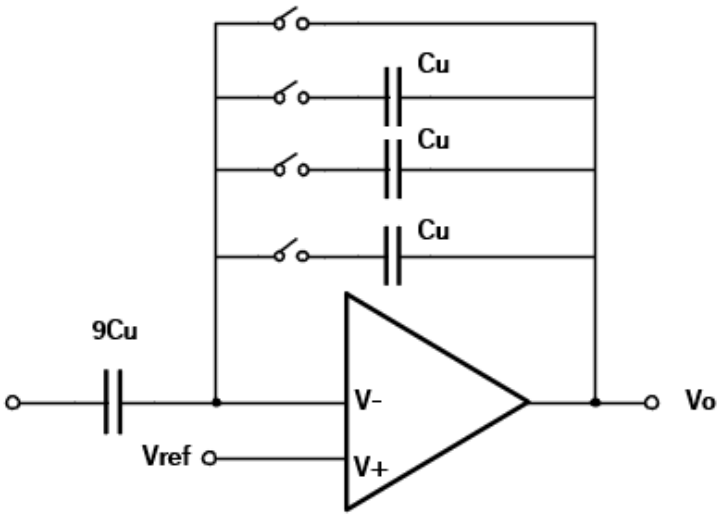


Figure 3.15: The switching capacitor variable gain OTA.

The another benefit with using two cascade switch capacitive OTA is the many gain steps from 1 to 81. The combination of the gain stage is summarized as the Table.3.4.

Gain Combination	Gain
1×1	1
1×3	3
1×4.5	4.5
3×3	9
3×4.5	13.5
4.5×4.5	20.25
9×3	27
9×4.5	40.5
9×9	81

Table 3.4: The gain step combinations.

3.5.2. Buffer Design

Because the input capacitance, $9 \times C_{unit}$, on the TGC stage will form the huge loading capacitance for the former stage's load, this distorts the former stage's gain accuracy. In order to alleviate the huge capacitance loading stage of each OTA network, a buffer is needed to isolate the output node from the later OTA's capacitors.

The proposed Flipped Voltage Follower (FVF) is shown in the Figure3.16. Compared to the conventional common-drain source follower, the FVF with a shunt feedback is able to source a large amount of current. The output node voltage is further decreased, which is approximately expressed as [41]:

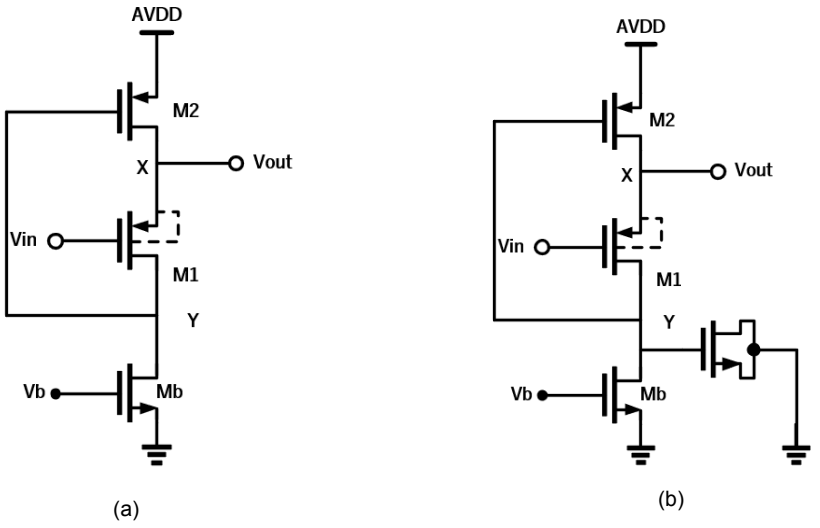


Figure 3.16: (a) The flipped voltage follower. (b) A MOS capacitor is added at the node Y for the loop stability.

$$r_o = \frac{1}{(g_{m1}g_{m2}r_{o1})}. \tag{3.22}$$

Where the g_{mi} and r_{oi} are the transconductance and output resistance of the transistor M_i depicted as the Figure.3.16a. This topology has the gain expression is:

$$\begin{aligned} A_V &= \frac{gmR_Y}{1+(gm+gmb)R_Y} \\ R_Y &= r_b \| gm_1 ro_1 ro_2. \end{aligned} \tag{3.23}$$

In order to obtain the unity gain, the the body-effect transconductance g_{mb} should be minimized. This is the reason the bulk node of M_1 is connected to the source in Figure.3.16a.

The M_2 provides the shunt feedback and forms a two pole negative feedback loop. The dominant pole is located at the node Y, $\omega_Y = 1/C_Y R_Y$, and a high-frequency pole at node X, $\omega_X = 1/C_X R_Y$. For stability consideration, the limit situation is:

$$C_Y > g_{m2}r_{o2}C_X. \tag{3.24}$$

Where the C_X is the load capacitance, which is dominated by the later stage OTA and it is a large value. In order to have the stable loop gain, the $g_{m2}r_{o2}$ should be low. There are two approaches to have a small $g_{m2}r_{o2}$. One is to decrease the g_{m2}. It requires a large over-drive voltage V_{OD2} that limits the saturation headroom. The another way is to increase the biasing current to decrease the r_{o2}. In order to have sufficient swing and small power consumption, it is designed to use a MOS capacitance to compensate the dominant pole. As the Figure.3.16b shown, the node Y has a MOS capacitance to stabilize the loop gain. The biasing current I_{mb} is set to be 30

μA and the -3 dB bandwidth is beyond 20 MHz. The Figure.3.17 depicts the layout of the flipped voltage follower. The MOS capacitor takes the most area.

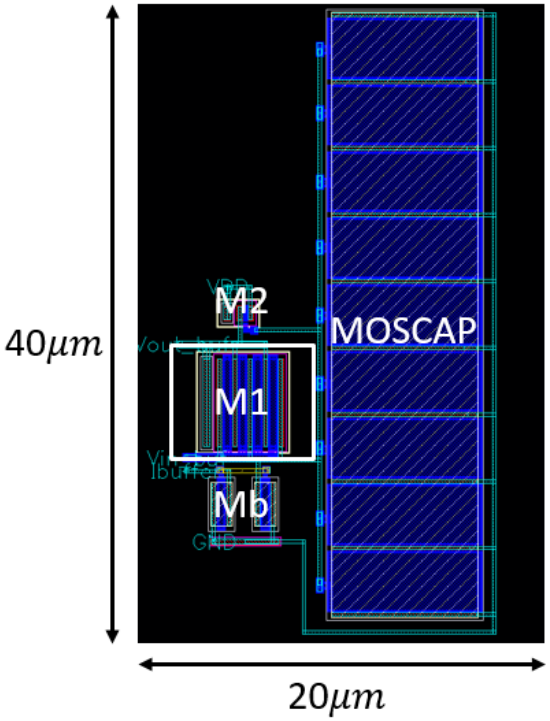


Figure 3.17: The layout of the flipped voltage follower.

3.6. Power and Corner Simulations

The total current consumption excluding the biasing network is summarized as the Table.3.5.

Table 3.5: The power consumption of each block.

Stage	**Supply Current**(μA)	**Power**(μW)
Low-noise amplifier	155.4	279.72
Buffer	29.5	53.1
Total	525.2	945.36

The temperature range for wearable ultrasound device is designed to be from 0 °C to 50 °C. The Figure.3.18 depicts the maximum 62 dB gain on different processes and temperatures corners. The pseudo-resistor has huge variations associated with the different corners: the high-pass pole located at low frequency varies from few hertz to hundreds hertz. This variation will be filtered out completely after the digitization. The gain and bandwidth variation is summarized at the Figure.3.19, which the gain is larger than 60 dB and bandwidth is beyond 20 MHz at all corner conditions.

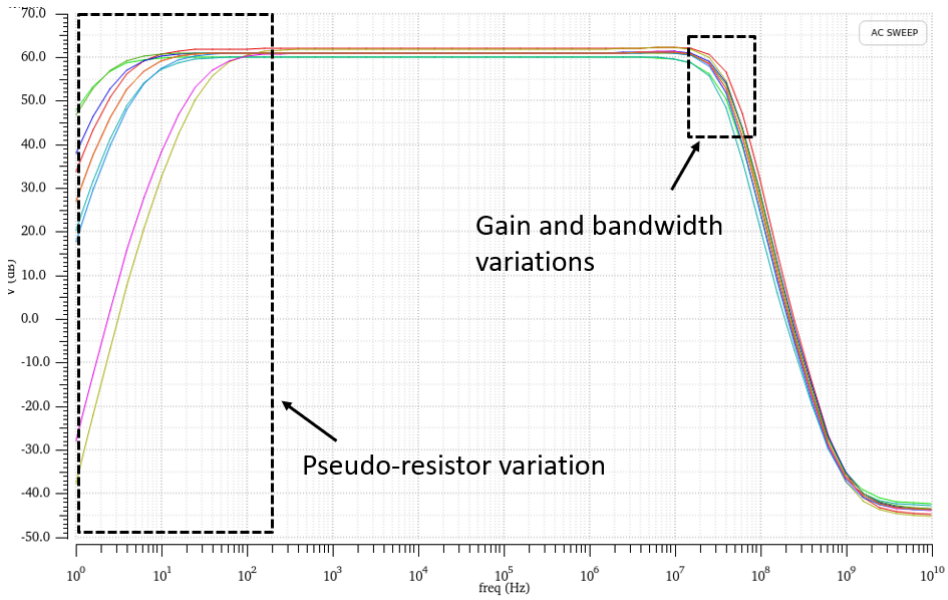


Figure 3.18: The corner simulation (process corners: tt, fs, ss, fs and sf; temperature corners: 27 °C, 0 °C and 50 °C) of the maximum 62 dB gain.

Parameter	Nominal						27	0 C_0	0 C_1	0 C_2	0 C_3	50 C_0	50 C_1	50 C_2	50 C_3
c018bcd_gen2...	pre_simu						nom	nom	nom	nom	nom	nom	nom	nom	nom
c018bcd_gen2...	tt_lib						tt_lib	fs_lib	sf_lib	ss_lib	ff_lib	ff_lib	fs_lib	sf_lib	ss_lib
temperature	27						27	0	0	0	0	50	50	50	50
Output	**Nominal**	**Spec**	**Weight**	**Pass/Fail**	**Min**	**Max**	**27**	**0 C_0**	**0 C_1**	**0 C_2**	**0 C_3**	**50 C_0**	**50 C_1**	**50 C_2**	**50 C_3**
Maximum Gain	61.23	> 60		pass	60.08	62.24	61.23	61	61.32	60.08	62.24	62.22	61.08	61.31	60.08
Bandwidth	26.89M	> 18M		pass	21.51M	31.33M	26.89M	27.87M	28.41M	22.66M	31.33M	28.18M	25.29M	25.63M	21.51M
transient															
AC SWEEP															

Figure 3.19: The summary of the bandwidths and gains on different corners.

4

Analog-to-Digital Converters Design

The previous chapter already produced the 1 V full-scale voltage for the ADC. This chapter will investigate and introduce the design principle of the ADC under the condition of that the whole system is area and energy efficient. This chapter is divided into 3 major sections. The first section is the introduction of the general definitions of the ADC and the system-level considerations to have a low power and small size ADC. The second section is the circuit design consideration including both digital blocks and analog blocks. The last section is the final test bench of ADC, the performance summary and the final system layout.

4.1. General Definition of ADC

The full-scale range of an ADC is defined as the range between the minimum and maximum value of the input signal without causing the saturation in the ADC operating process. For an N-bit ADC transfer characteristic, the FSR includes $2^N - 1$ transitions. However, for a large N, the Least Significant Bit (LSB) is more commonly calculated by 2^N transitions in the literature [42]:

$$\mathrm{V}_{LSB} = \frac{FSR}{2^N}. \tag{4.1}$$

Quantization noise is the deviation between the output code of an ADC and the ideal ADC output curve. For a 3-bit resolution example, the difference in the ideal finite 3-bit resolution transfer curve and the ideal infinite resolution transfer curve results in a quantization noise. As the Figure 4.1 illustrates, the best fit line represents the ideal output with the infinite steps. It deviates with the finite $2^3 = 8$ step transfer characteristics. This calls for a theoretical limit to the maximum achievable SNR for an ideal N-bit ADC. The quantization noise Q_{qn} within an LSB interval ($\pm\frac{V_{LSB}}{2}$) can be calculated as the rms quantization noise power as:

$$V_{rms} = \sqrt{\frac{1}{V_{LSB}} \times \int_{\frac{-V_{LSB}}{2}}^{V_{LSB}} Q_{qn}^2 dQ} = \frac{V_{LSB}}{\sqrt{12}} = \frac{FSR}{2^N \times \sqrt{12}}. \tag{4.2}$$

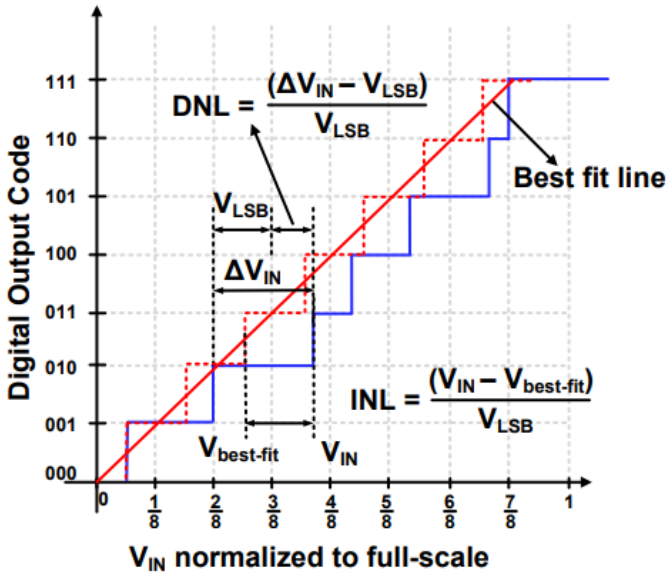


Figure 4.1: Transfer curve of a real 3-bit ADC (in blue). The dashed red line is the transfer characteristics of an ADC with finite 3-bit resolution. The best fit line is the transfer characteristics of an ADC with infinite resolution [7].

Based on the calculated noise on the above equation, the maximum SNR of an ideal ADC with no noise source and finite resolution N is defined as:

$$\mathrm{SNR} = 10 \cdot \log_{10}\left(\frac{P_{\mathrm{sig,rms}}}{\left(V_{\mathrm{qn,rms}}\right)^2}\right)[\mathrm{dB}]\,. \tag{4.3}$$

Where the P_{sig} is the rms input signal power. If the input signal is sinusoidal and the peak-to-peak value equals to the FSR, the SNR is calculated as:

$$\mathrm{SNR} = 10 \cdot \log_{10}\left(\frac{FSR/2\sqrt{2}}{FSR/2^N\sqrt{12}}\right)[\mathrm{dB}] = 6.02N + 1.76\,[\mathrm{dB}]\,. \tag{4.4}$$

The blue curve in Figure 4.1 shows the real 3-bit ADC with the static error. Compared to the ideal transfer line, it has non-linearity deviations. Differential Non-Linearity (DNL) is defined as the maximum difference between the analog input voltage step and the ideal width of the step ($\mathrm{V_{LSB}}$). The final result is normalized to $\mathrm{V_{LSB}}$ [42]:

$$\mathrm{DNL} = \left(\frac{\Delta V_{in} - V_{LSB}}{V_{LSB}}\right). \tag{4.5}$$

Integral Non-Linearity (INL) is the maximum difference between the analog input voltage that be digitized into the output code of a real ADC and the output code corresponding to the best-fit line, as plotted in the Figure.4.1. The result is also normalized to V_{LSB} [42]:

$$\mathrm{INL} = \frac{V_{in} - V_{best-fit}}{V_{LSB}}. \tag{4.6}$$

The dynamic performance of an ADC is a important characteristic. After the FFT spectrum of an ADC output code, the Signal-to-Noise-and-Distortion ratio (SNDR) is defined as the ratio of the rms signal power to the sum of the powers of all the unwanted components on the FFT spectrum, including distortion tones, noise sources, clock jitter etc. These unwanted components degrade the accuracy of the final output signal. The Effective Number of Bits (ENOB) is used to quantify the performance of the real ADC to the number of bits that can be resolved by an ideal ADC which has only the quantization noise. Based on the previously mentioned, the quantization noise of finite resolutions of an ideal ADC is inevitable, therefore, its SNDR equals to the SNR. But for a real ADC, the actual final obtained resolution is decided by the ability of suppressing all unwanted components. The ENOB is expressed as:

$$\mathrm{ENOB} = \frac{SNDR - 1.76}{6.02}. \tag{4.7}$$

Among these unwanted components, the Spurioust Free Dynamic Range (SFDR) is defined as the difference in the signal power level and the worst harmonic tone or spur with the highest power level in the output FFT spectrum of the ADC. SFDR is a useful term for ADCs as it defines the minimum wanted signal in dB that can be demodulated by the ADC in the presence of the unwanted interferes. Total Harmonic Distortion (THD) is defined as the ratio of the sum of all harmonic power of the input signal to the power of the fundamental tone (signal itself) within the bandwidth of interest.

4.2. ADC Figure-of-Merit and Energy Consideration

The Figure-of-Merit (FoM) is used to benchmark the performance of the ADCs for various resolution, speed, input bandwidth and energy consumption. There are two commonly used FoMs:

- Walden Figure-of-Merit (FoMw) [43]:

$$\mathrm{FoMw} = \frac{P_{ADC}}{min(2 \times BW_{in}, f_s) \times 2^{ENOB}} [Joule\ per\ conv - step]. \tag{4.8}$$

  Where P_{ADC} is the power consumed by the ADC and f_s is the clock frequency that the ADC needs to acquire the analog signal and convert it into digital.

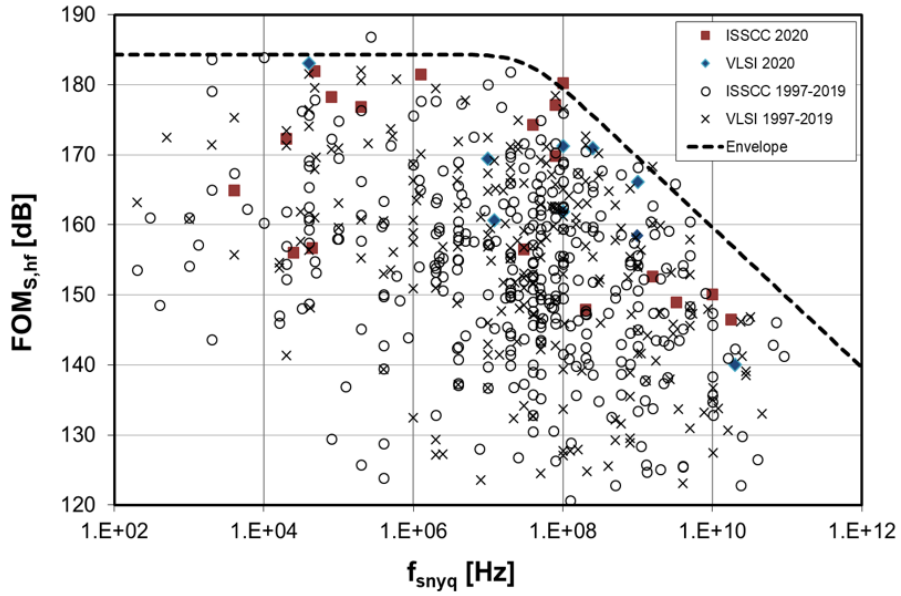
- Schreier Figure-of-Merit (FoMs) [44]:

$$\mathrm{FoMs} = SNDR + \log_{10}(\frac{BW_{in}}{P_{ADC}})[dB]. \tag{4.9}$$

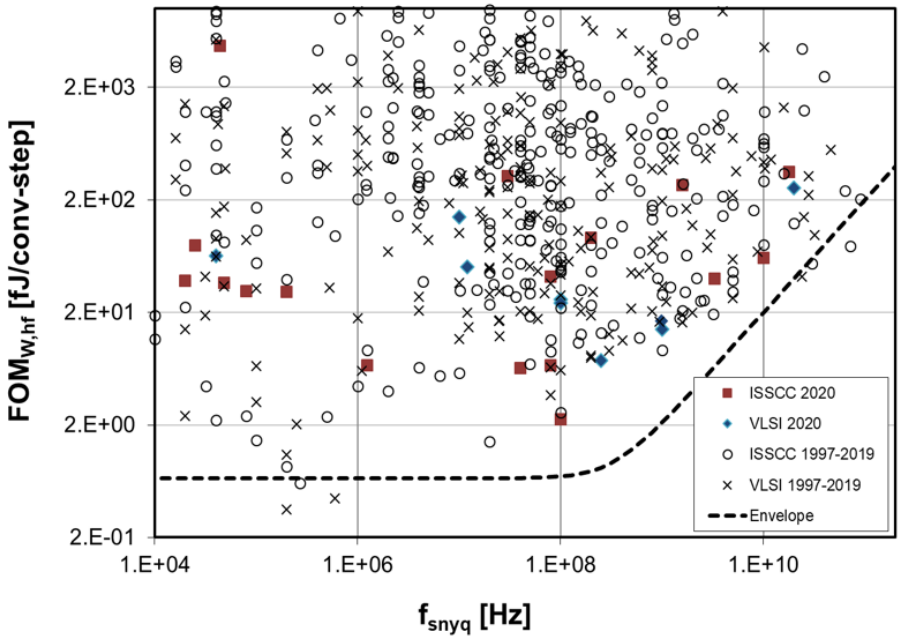
The difference between the FoMs in equation 4.9 and FoMw in equation 4.8 is that the SNDR in the latter is replaced by the 2^{ENOB} in the former. In addition, the ADC power supply, P_{ADC}, appears at the numerator in the FoMw and in the denominator for the FoMs. It means a lower FoMw value represents a higher power efficiency whereas for the FoMs benchmark, higher value is preferred for a higher energy efficiency. Generally, the FoMw indicates the energy consumption per conversion bit and is well suited for the ADC architectures that are not thermal noise limited but are constrained by the number of levels that can be quantized within a give supply voltage [42]. In general, the FoMs is preferred for designs with $SNDR > 50dB$ while the FoMw still has its place for low-resolution designs [45]. These two test approaches have something in common that they both mainly focus on three aspects: resolution, conversion rate and power dissipation.

Figure.4.2 indicates the latest trend of FoMs and FoMw, showing that for low resolution and SNDR, the energy efficiency can be improved to a high value within a low sampling speed. When the sampling speed exceeds the corner frequency, the theoretical best obtained benchmark occurs a roll-off. When the frequency goes beyond the corner frequency, the energy efficiency degrades with the 10 dB/dec. Figure.4.2a and Figure.4.2b both have their trend. Normally the breakthrough of the limit is achieved by more advanced technology and novel topologies. Although considering using the ideal transistor, there is also a ceiling point. The Schreier Figure-of-Merit can be improved to 194 dB under the condition that ideal transistors are in used, but under modern most advanced technology, the constrain allows it can be improved to close to 186 dB. To be noticed that, the achieved high energy efficiency of the A/D converters only include the energy required by the A/D converter itself that quantifies signal and not contain the energy that acquires the signal on the input capacitor. For most cases, the ADC needs an auxiliary circuit to condition the physical signal and sample the signal. Even use a reliable FoM to benchmark an ADC, they still do not explicitly provide any insight into the energy required to drive the ADCs' inputs. This results in a complicated consideration of overall low-energy design, that is, the energy required for input signal acquisition and the ADC supply energy for conversion.

Among all the ADC typologies, Successive Approximation Register (SAR) ADCs are the preferred choice for the ultra-low power applications [45]. There are many approaches to allow these SAR ADCs achieving high energy efficiency. Not only the SAR ADCs itself consumes power, normally the input drive circuitry is responsible to provide a stable physical signal for the signal acquisition and conversion. This calls for a special design on energy efficiency. Minimizing the power consumption of ADC is not the only option. Some considerations are also required to investigate how much energy needed for the driving its analog inputs to enable an overall low energy data acquisition system.



(a) Schreier FoM vs. speed



(b) Walden FoM vs. speed

Figure 4.2: The latest Figure-of-Merit trend [8].

4.3. Basic Operation of SAR ADC

The basic idea of SAR ADC is a calculation manner usually employs a binary search algorithm where a digital estimate an unknown signal. This is made by a series of successive comparisons with a sequence of known quantities. The basic block diagram for an N-bit SAR ADC is shown in Figure.4.3. The signal V_{SH} is acquired by the switch or the sample and hold function. The contents of the SAR logic are fed into the Digital-to-Analog Converter (DAC) that generates an analog voltage at its output corresponding to the input digital code and the reference voltage. The comparator compares the DAC output and the actual sampled signal. After each comparison, the shift registers in the SAR logic are updated, providing the new digital signal to the DAC to generate a new analog approximation as used to be compared with the V_{SH} again. The above process repeats in a sequential manner by changing the register bit per each comparison operation and make the analog approximation closer to the sampled input after each cycle. For an N-bit SAR ADC, the number of N cycles of comparisons are needed and done sequentially. At the end of the N-th comparison, the contents of shift register in SAR logic will output the N-bit quantization data. The N-bit SAR conversion repeats the digital approximation after when next signal comes in.

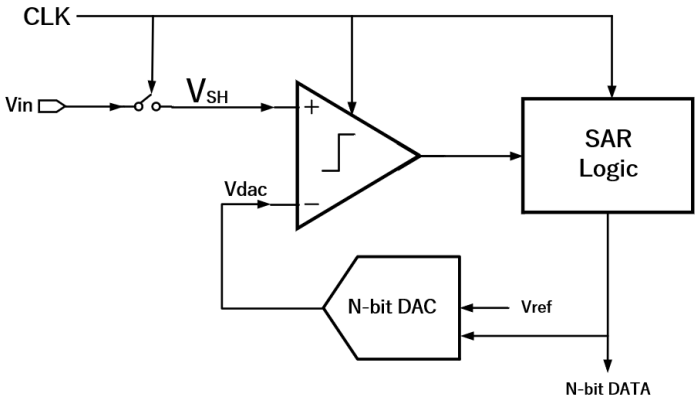


Figure 4.3: Successive-Approximation Register ADC block diagram

The DAC is used to generate a new analog signal corresponding to the updated digital code. Since the DAC has to provide an analog output, the loading effect of the succeeding stage, the power constraints of the ADC and the total area consuming limit the type of DAC that can be used.

The Resistive String and R-2R DAC requires a small value of resistance or a low output impedance voltage buffer in order to decrease the settling time. Normally, the resistive string and R-2R DAC type are power hungry. The advantage of this type is that it has an inherently monotonic behavior. The reason is all the resistors have the same value and the voltage across them changes in a unary manner. R-2R DAC consists of a ladder arrangement of resistance. This arrangement dramatically decreases the needed resistors comparing to the resistive DAC with the same amount of bits. However, this topology requires high accuracy of resistance. The inequality in

current splitting results in accuracy problem and non-linearity issue. For most cases, the R-2R DAC are only used in when low resolution is needed due to the non-linearity problem [46]. Furthermore, for low power consumption requirement, the resitive DAC is not a ideal choose.

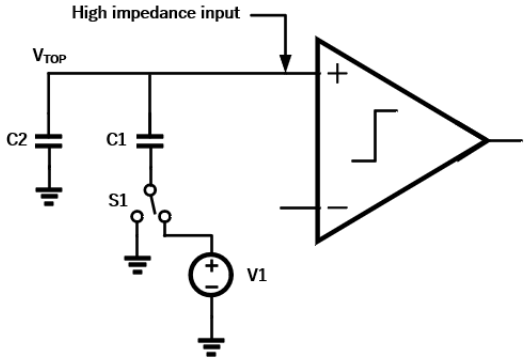


Figure 4.4: Simplified Circuit demonstrating the CR principle

Charge-redistribution DAC has higher energy efficiency because it utilizes charge instead of current. Furthermore, it is implemented by switches and capacitors, making the scale the structure friendly. In addition, it is easier to integrate with sample and hold switch that acts as an input interface circuitry to sample and hold the input signal. During the SAR conversion, the top or bottom plates of the capacitors are either connected to reference voltage or to the ground depending on the digital code from the SAR logic. This process results in a redistribution of charge at the end of conversion. In the Charge Redistribution (CR) scheme, the DAC output is set by varying the voltage on the bottom plate of the capacitors, while maintaining the total capacitance unchanged. In the example of shown in Figure.4.4, the operation is achieved by switching the S_1 between V_1 and ground. Since the comparator has a high input impedance, negligible current flows to V_{top}. The charge on the top plate is constant independently of the changes in S_1. The voltage V_{top} changes according to S_1. The amount of variation is also decided by the ratio of C_1 to the total capacitance $C_1 + C_2$.

Considering t_1 is the instant when the switch S_1 is disconnected from ground and connected to V_1, and t_0 represents the instant before t_1. t_2 is defined as the moment after the switching when the circuit has already settled. The total charge in the top-plate at the t_0 is expressed as:

$$\mathrm{Q_{TOP}}\,(t_0) = V_{\mathrm{TOP}}\,(t_0)\,(C_2 + C_1) \tag{4.10}$$

Similarly, the charge at the t_2 can be computed as:

$$\mathrm{Q_{TOP}}\,(t_2) = V_{\mathrm{TOP}}\,(t_2)\,C_2 + (V_{\mathrm{TOP}}\,(t_2) - V_1)\,C_1 \tag{4.11}$$

Since there is conservation of charge in the top plate, the equation 4.10 equals to 4.11. Then, the new top plate voltage is:

$$\mathrm{V_{TOP}}\,(t_2) = V_{\mathrm{TOP}}\,(t_0) + V_1 \frac{C_1}{C_1 + C_2} \tag{4.12}$$

By this switching algorithm, the ability to shift the voltage up and down in controlled steps is attained by using multiple capacitors with switchable bottom plates. For example, C_1 and C_2 have binary weights of capacitance. Similar to the R-2R ladder, the capacitors also can have C-2C structure. However, it has the same issue with the R-2R ladder mentioned previously. The non-linearity heavily constrains their output accuracy. The binary weighted CR DAC is the primary choice when the power-efficiency design is critical. However, as the number of bit increasing, it takes much more area because the total number of capacitors increase exponentially, which is 2^N for the N-bit DAC. To mitigate this area-consuming problem, other structures such as split-capacitors and hybrid DACs are used. This project chooses this class of binary weighted charge redistribution DACs due to its low-power characteristics. Based on the equation 4.7, the selected number of bit is decided by the input signal. In our case, the DR of our signal is relative low, which leads to a low-area requirement for the DAC.

4.4. Review of SAR ADC Switching Schemes

This section presents some switching techniques that have been used over the years, conventional, monotonic and V_{cm}-based, to reduce the energy consumption in various blocks inside a SAR ADC. All this switching techniques are based on the CR DAC as the previous section introduced.

4.4.1. Conventional Switching

The conventional SAR algorithm for a 3-bit fully differential implementation is depicted in Figure.4.5, where the energy required in each comparison cycle is also indicated.

During the tracking phase, the bottom plates of each half of the differential DAC are sampled respectively to the differential input signal and the top plates are reset to the common mode voltage, V_{cm}. Once the sampling period is finished, these capacitors are disconnected from the input node. Afterwards, the MSB capacitor is connected to V_{ref} while the remaining capacitors are grounded. For the bottom-plate array, the opposite procedures are done. As the Figure.4.5 shows, for the 3-bit case, the energy consumed by this switching process is $4CV_{ref}^2$. Next, the comparator is activated, and the result from the comparator is the digitized information that represents the MSB output. Depending on the outcome whether the MSB is low or high, the DAC's switch takes the "ON" or "OFF" decision, as depicted in Figure.4.5, the required energy consumes CV_{ref}^2 or $5CV_{ref}^2$ respectively. There are four possible trajectories and it depends on the input signal. This is not a very energy-efficient approach. At the second cycle, the down transition uses five times more energy than up transitions. Because each bit capacitor has to charged to V_{ref} for testing and if this transition results in a wrong or unsuccessful trial, then it has to be discharged to ground. Many switching algorithms have been proposed over the years in order to minimize the DAC switching energy. The average energy of a N-bit switching algorithm, assuming all codes are equiprobable, is derived as:

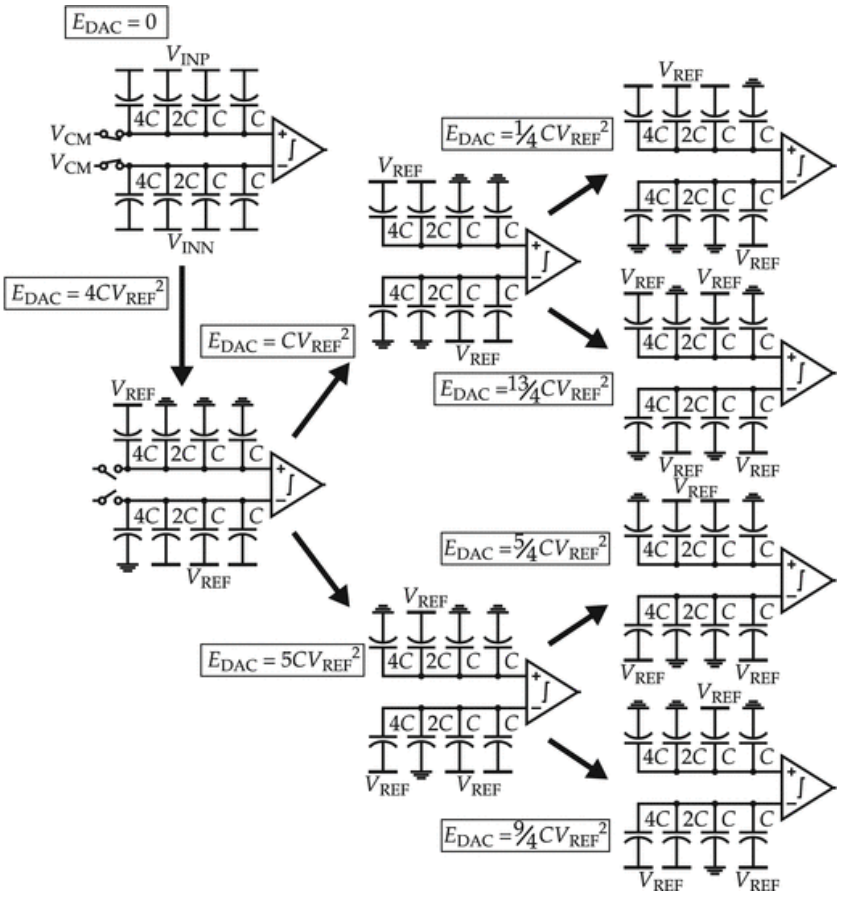


Figure 4.5: Conventional CR switching scheme waveform and conversion procedure [9].

$$\begin{aligned} \mathrm{E}_{\text{conventional}} &= \sum_{i=1}^{N} \left(2^{N+1-2i}\left(2^{i}-1\right)\right) CV_{\text{REF}}^2 \\ &= \left(\frac{2^{-N+}+2^{N+2}}{3}-2\right) CV_{\text{REF}}^2 . \end{aligned} \tag{4.13}$$

4.4.2. Monotonic Switching

The monotonic or ”Set-and-Down” switching scheme is depicted in Figure.4.6. The idea of operation of a monotonic switching scheme is based on having discharging cycles only. Besides this, it enables the top-plate sampling, hence it only requires 2^{N-1} capacitors instead of 2^{N}. The reason is the top-plate sampling enables the MSB to be obtained by directly comparing the input signal without switching any capacitor. This increasingly benefits the circuit that needs low-area structure.

During the sampling phase, the input signal is sampled onto the top plates of the capacitive array, and the bottom plates are connected to the reference voltage, V_{ref}. The MSB is directly obtained by the comparator, as the Figure.4.6 depicted. The comparison result of the MSB, whether is high or low, feeding into the SAR logic. For

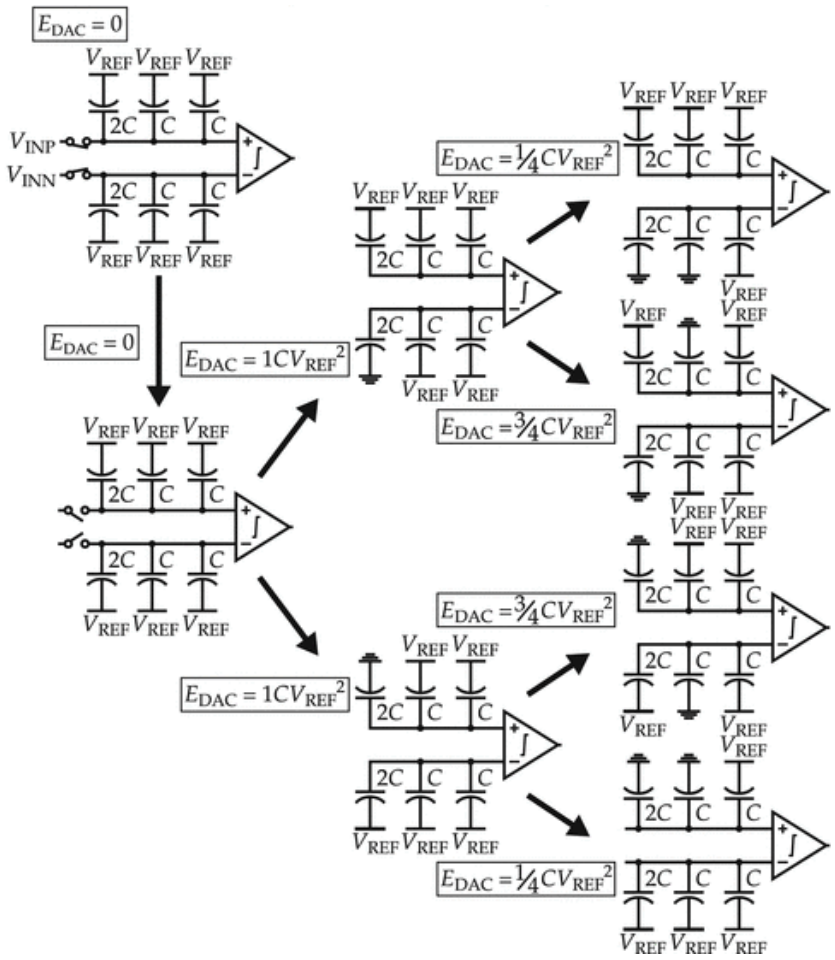


Figure 4.6: Monotonic Switching in a charge redistribution DAC operation and their required energy [9].

the positive side of capacitive array, the ”0” or ”1” from the MSB decides the bottom-plate if the capacitor connects to V_{ref} or ground respectively. For the negative side, the procedure is opposite. And this process is carried out sequentially for the remaining bits, reducing the differential voltage towards zero and the output bits are extracted from the comparator output. Comparing to the conventional switching scheme, the average energy consumed by the monotonic switching scheme is calculated as:

$$\begin{aligned} \mathrm{E}_{\text{monotonic}} &= \sum_{i=1}^{N-1} \left(2^{N-2-i}\right) CV_{\mathrm{REF}}^2 \\ &= \left(2^{N-2} - \frac{1}{2}\right) CV_{\mathrm{REF}}^2. \end{aligned} \tag{4.14}$$

4.4.3. Common-Voltage Based Capacitor Switching

The V_{cm}-based SAR ADC is shown the Figure.4.7. It is also called Merged Capacitor Switching (MCS) [47]. This switching scheme also employs the top-plate sampling. Similar to the monotonic switching scheme, the first comparison happens after the

sample and hold phase ends. Unlike the bottom-plate is connected to V_{ref} in monotonic scheme situation, the V_{cm}-based scheme is connected to the common-mode voltage instead. And after sequential cycles of comparisons, the top-plate voltage is close to the common-mode voltage in the V_{cm}-based scheme, while in monotonic case, based on previously mentioned, V_{top} is close to zero voltage. The MCS has the same advantages as the monotonic scheme, which requires only half of the capacitance for the same resolution, when compared to the conventional switching scheme. The another advantage of V_{cm}-based scheme is that it increasingly improves the energy efficiency by employing the voltage change only $(V_{ref} - V_{cm})$ in the top and bottom arrays, instead of a full V_{ref} step, as happens in the monotonic and the conventional procedure.

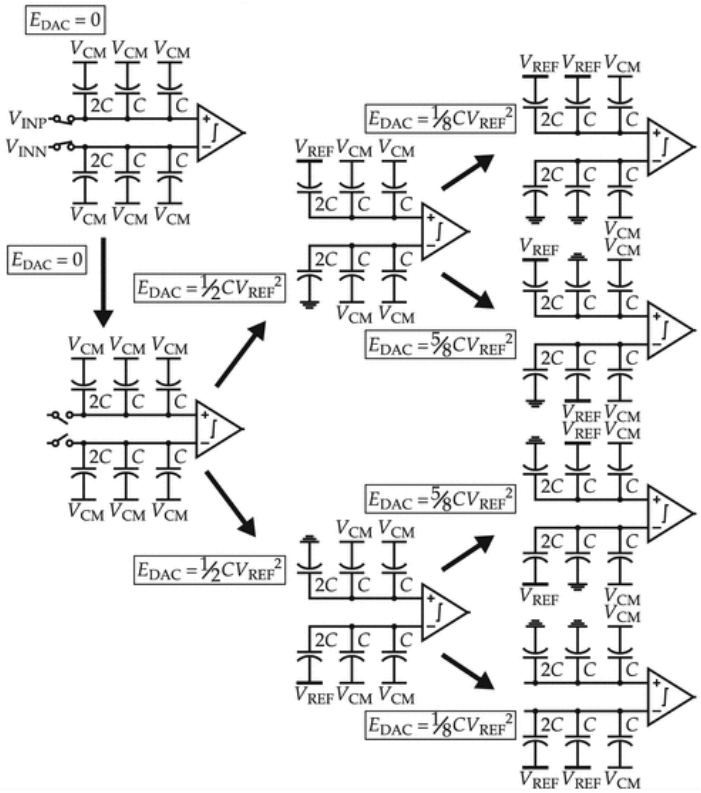


Figure 4.7: V_{cm}-based SAR ADC conversion procedure and consumed energy [9].

Generally, the energy consumption becomes $C(\frac{V_{ref}}{2})^2$ in the common-mode voltage switching scheme. It is a fourfold energy reduction achieved by each cycle. Although this structure needs another stable common-mode voltage in the circuitry, this scheme maintains the common-mode voltage of the input during the whole conversion, which will benefit the linearity of ADCs and relax the design of comparator [48]. The energy consumed by each conversion is shown in Figure.4.7. The average energy of a N-bit V_{cm}-based switching scheme is derived as:

$$\begin{aligned} \mathrm{E}_{\mathrm{Vcm-based}} &= \sum_{i=1}^{N-1} \left(2^{N-2-2i}\left(2^{i}-1\right)\right) CV_{\mathrm{REF}}^{2} \\ &= \left(\frac{2^{-N}+2^{N-1}}{3}-\frac{1}{2}\right) CV_{\mathrm{REF}}^{2}. \end{aligned} \tag{4.15}$$

For the 6-bit resolution as the example, the energy consumed by the monotonic switching scheme only takes 18.6% of the energy consumed by the conventional SAR. The MCS SAR consumes only 12.2% of conventional SAR based on using equations from Equation.4.13, 4.14 and 4.15 to calculate these results, where N is 6 and V_{REF} is 1 V.

Based on above analysis, the MCS SAR ADC is preferred due to its best energy-efficiency performance and the stable common-voltage on the bottom-plate. Although the V_{cm}-based scheme requires a clean common-mode voltage in the system, in our case, the common-mode voltage can be shared by multiple channels. Additional consideration is, based on previous section introducing, the echo signal received from the Analog-Front-End is single-ended that all channels share the ground and input voltage is above the ground. The swing is from 0 to full-scale of SAR ADC. Above mentioned scheme needs differential-ended input signal, meaning that we need a single-ended to differential-ended amplifier to drive the SAR ADC. Designing a new amplifier is heavily energy-consumed approach. Although differential SAR ADC has its benefit such as high linearity and the immunity to the offset from the comparator, however for the low resolution consideration (maximum DR of signal is around 30dB), single-ended SAR is preferred because it shrinks half size of required capacitor arrays, DAC logic and switches. And the MCS SAR ADC can be designed to as a single-ended structure with low-area and low-energy characteristics. The detail proposed structure will be introduced in following sections.

4.5. Structure Consideration

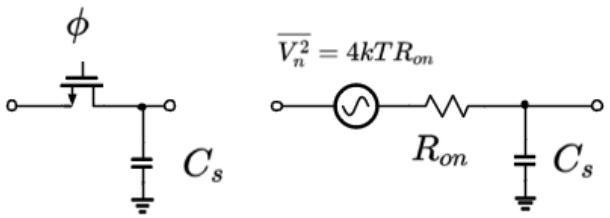
Based on previous sections analysis, in order to achieve a SAR ADC with the low-area and low-power performance, the V_{cm}-based switching scheme with the single capacitor array is selected. However, as previously mentioned, the best energy-efficiency structure of the ADC may not the best choice. Normally, SAR ADC needs a driver to enable the fast sampling speed. Of course, minimizing the amount of sampling capacitors is also an alternative option (τ =RC). However, the small sampling capacitor brings bigger KT/C noises and is sensitive to parasitic capacitance. This drawback heavily degrades the final achieved ENOB of the SAR ADC.

In the modern SAR ADC design, the bottleneck of designing a low-power high SNDR SAR ADC is not only the ADC structure itself, the driver amplifier plays more and more important role. In our case, the situation is different because the needed SNDR is not high (maximum 30dB) and signal works in a mid -frequency region

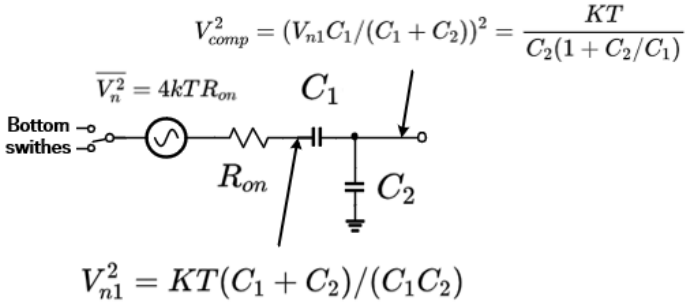
(12MHz). In this section, the investigation of overall structure of the SAR ADC will be introduced.

4.5.1. KT/C Noise and Capacitance Mismatch

As discussed in previous chapter, the dynamic range at the output of the AFE is around 30 dB. Normally, the 5-bit SAR ADC is enough for digitizing the signal based on the Equation.4.4 that the 5-bit ADC can reach 32 dB dynamic region. Consideration the KT/C noise, process corner and dynamic offset on the comparator, the 6-bit SAR ADC is used for a safe margin to ensure the SNDR is beyond the 30dB. The ADC sampling rate must be larger than 4 times the transducer central frequency to maintain a satisfactory side-lobe level [49]. Therefore, the SAR ADC is set to work at 50 Mega sample rate per second to meet the requirement under the case that the signal works 12 MHz operation frequency.



(a)



(b)

Figure 4.8: (a) Sampling equivalent circuit for calculation thermal noise. (b) Equivalent circuit for calculation the noise contribution to comparator from the switches on the bottom-plate.

In this design, the total needed capacitors for the 6-bit single-ended V_{cm}-based SAR are 2^5, which is $32C_{unit}$. The capacitor is a Metal-Insular-Metal (MIM) manufactured capacitor. Limited by the manufacture technique of TSMC's asic 180nm technology, the minimum available area is 4μ ×4μ with the value of 33.43fF. The noise contributions towards the comparator are from two sides: the signal input node and bottom-plate switch node. As the equivalent circuit plotted in Figure.4.8a, the noise model is a typical KT/C noise calculation. The sampling capacitor C_s is the total unit capacitors in the CDAC array. The KT/C noise from the sample and hold switch is derived as:

$$\text{Noise}_{\text{S/H}} = \frac{KT}{2^5 C_{unit}} = 3.85n\bar{V}^2. \tag{4.16}$$

Also, the bottom-plate switches contributes the noise towards the CDAC. The equivalent model is illustrated as the Figure.4.8. The bottom-plate noise contribution is express as:

$$\text{Noise}_{\text{bottom-plate}} = \frac{KT}{C_2(1 + C_2/C_1)}. \tag{4.17}$$

Where the C_1 is the capacitor which the switch is connected, while C_2 is the capacitance summed by all other capacitors. Therefore, the binary-weighted capacitor array is the sum of all contributions. In this design, the calculated the bottom-plate noise source from all 6-bit is: $0.05 \times KT/C_{unit} = 6.14n\bar{V}^2$.

The Full-Scale Range (FSR) of our signal is designed to 1 V. At the 6-bit situation, the LSB is 15.6mV. Based on the Equation.4.2, the quantization noise power is $2.03 \times 10^{-5}\ \bar{V}^2$. The calculated KT/C noise only takes 0.049% of total quantization noise. Comparing to the LSB, the noise amplitude on the top-plate is 0.1 mV, which is also much smaller than the LSB. It means that, in the 6-bit SAR ADC design, the minimum possible capacitance, 33.43fF, only contributes a trivial portion of noise compared to quantization noise of the ADC, additionally, it also has negligible influence on the comparator.

Another consideration is the capacitance mismatch. Generally, the capacitor mismatch can be model as:

$$\frac{\sigma_{\Delta C}}{C_{unit}} = \frac{A_C}{\sqrt{C}}. \tag{4.18}$$

The parameter of A_C depends on technology and capacitor type. The term $\frac{\sigma_{\Delta C}}{C}$ is the standard deviation of the difference of unit capacitance normalized to their absolute value C, with the value $A_C = 2.27\%\sqrt{fF}$ in TSMC 180nm technology [5]. The model shows that the less deviations if the larger capacitors are used. Based on the work of modeling the non-linearity of mismatch of capacitor array on CR SAR ADC [50], for the binary-weighted SAR structure, the worst case of voltage deviation due to the capacitor mismatch is limited within half of LSB. the distribution with the worst case method is depicted as the Figure.4.9.

The Figure.4.9 indicates in order to the 6-bit SAR ADC, the term $\frac{\sigma_{\Delta C}}{C}$ has the value of less than 0.01 for the worst case consideration. Based on the Equation.4.18, we can derive the minimum unity capacitance:

$$\begin{aligned} \text{C} &= \left(\frac{A_C\sqrt{f}}{0.01}\right)^2 \\ &= 7.3fF. \end{aligned} \tag{4.19}$$

The minimum available capacitance, 33.43 fF, is still 4 times larger than the value. This leads to the CDAC constructed by smallest unit capacitance has the lowest power and area consumption without heavily degrades the performance of the ADC.

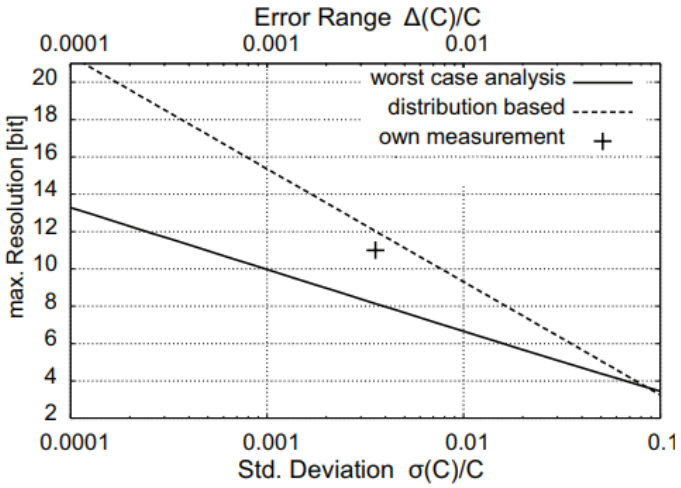


Figure 4.9: Maximum attainable resolution of a CR SAR ADC depending on the match of unit capacitor [10].

4.5.2. ADC Driver

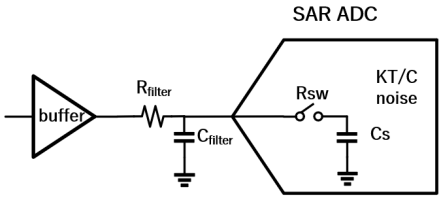


Figure 4.10: The SAR ADC with the driver structure.

An ADC needs a driver to ensure fast settling. As the Figure.4.10, for the time constant obtained by the sampling capacitance and switch ON resistance, it needs a powerful buffer to ensure this figure to be small, which is expressed as $R_{filter} \times (C_S + C_{filter})$. The minimum total sampling capacitance in our case is: $32\mathrm{C_{unit}} = 1.07\mathrm{pF}$ and the switch resistance is:

$$\mathrm{R_{ON}} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_G - V_T - \frac{V_S+V_D}{2})}. \tag{4.20}$$

The on-resistance of the NMOS switch is signal dependent. It means the the bootstrap switch is needed in order to eliminate the non-linearity caused by the varying switching resistance. Thus, V_{GS} is constant throughout the sampling period. The $\frac{W}{L}$ ratio can be large to make the time constant τ small. However, the penalty is the lager parasitic capacitance of the sampling switch, degrading the accuracy of the capacitor array if no advanced calibration and parasitic cancellation technique are used. In this design, the $\frac{W}{L}$ ratio is 8 and the time constant τ is around 0.4n seconds. The 5 times of time constant is very close to the target voltage. Thus, the final sample and hold period is around 2n seconds. The typical designed operation frequency is 50 MHz,

giving 20n seconds for each period for both signal acquisition and conversion. In order to ensure the sufficient tracking bandwidth, the signal acquisition period is set to be 3-4n seconds. It tells us the ON-resistance of bootstrap switch is mall enough that the data can be properly acquired on the top-plate of the capacitor array even without the buffer.

Benefiting from the small sampling capacitance, the SAR ADC takes less area and power consumption and enough time for signal acquisition. Based on the previous analysis, the trade-off of small sampling capacitance is higher noise and severer capacitance mismatch. The previous analysis demonstrates that these drawbacks are acceptable.

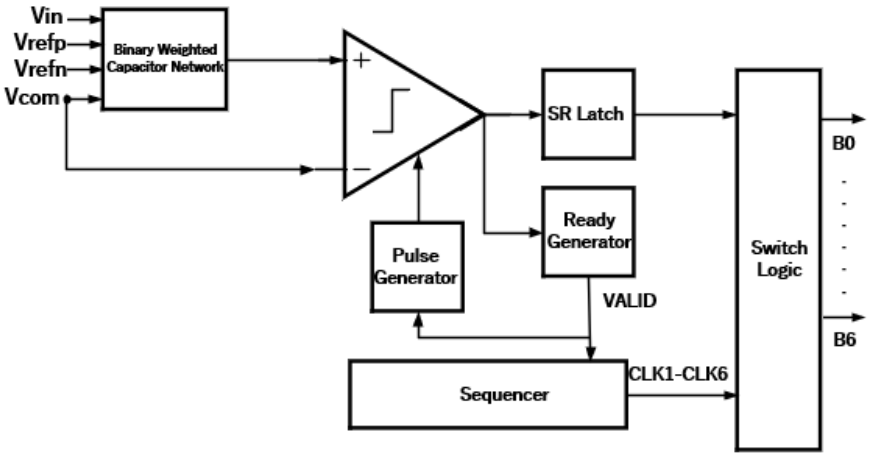
4.6. Overview of the SAR ADC

4.6.1. The asynchronous Operation

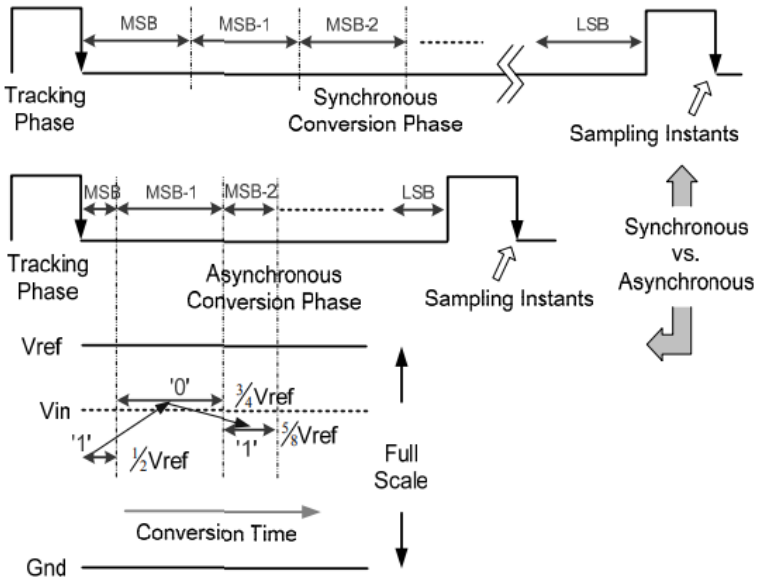
The concept of the asynchronous SAR logic was firstly proposed in 2006 [51], to reduce the power and increase the speed, dynamic open loop circuit are used with the charge redistribution network. This dynamic comparator eliminates the need to reduce the comparator offset, but the dynamic offset still needs to be carefully considered. Since the comparator must be reset at each comparison cycle, after each comparison, the complementary outputs of the comparator are used an NAND gate to create the ready signal called $VALID$. The $VALID$ signal is used to trigger a block of asynchronous switching logic. An external sampling signal is needed to reset the whole logic when each cycle of conversion is finished. The Figure.4.11a shows the architecture of the 6-bit asynchronous ADC. The dynamic comparator outputs the $VALID$ signal once the last bit trial is completed and the new comparison is finished. The sequencer internally generates the $CLK1$ to $CLK6$ to control the switch logic and the pulse generator and further control the comparator. This approach significantly saves the power and are easily trades off conversion speed with resolution without dramatically power increase.

As the Figure.4.11b showing, the ADC operation consists of tracking phase and conversion phase. During the conversion phase, there is bunch of bit trials that needs specific time. Conventionally, this specific time is constant throughout each bit trials during the conversion phase, but the asynchronous SAR enables the variable time depends on the state of the running speed of the comparator and DAC's capacitor charging or discharging speed. Previously mentioned structure tells that the ready signal is asserted once the comparator has a proper output. The bit trials in asynchronous conversion, shown as the Figure.4.11b, takes different time. The MSB trial takes a short amount of time, while MSB-1 trials needs more time because of the bigger voltage changes. Therefore, this idea brings advantages that can be summarized as following:

- Faster operation speed.



(a) The asynchronous ADC architecture



(b) The reduction of conversion time by implementing the asynchronous comparisons [51].

Figure 4.11: The asynchronous architecture block diagram (above) and the timing diagram of conversion (below) .

- Lower metastability rate. Because more times is automatically given to do the decision if the decision require more time.
- No need for high speed clock. Unlike the conventional synchronous structure, the required external clock is $N \times f_s$, which will consume a lot of power if the sampling speed and number of bit are both high. The asynchronous structure only needs one external clock at the same frequency as the sampling speed.

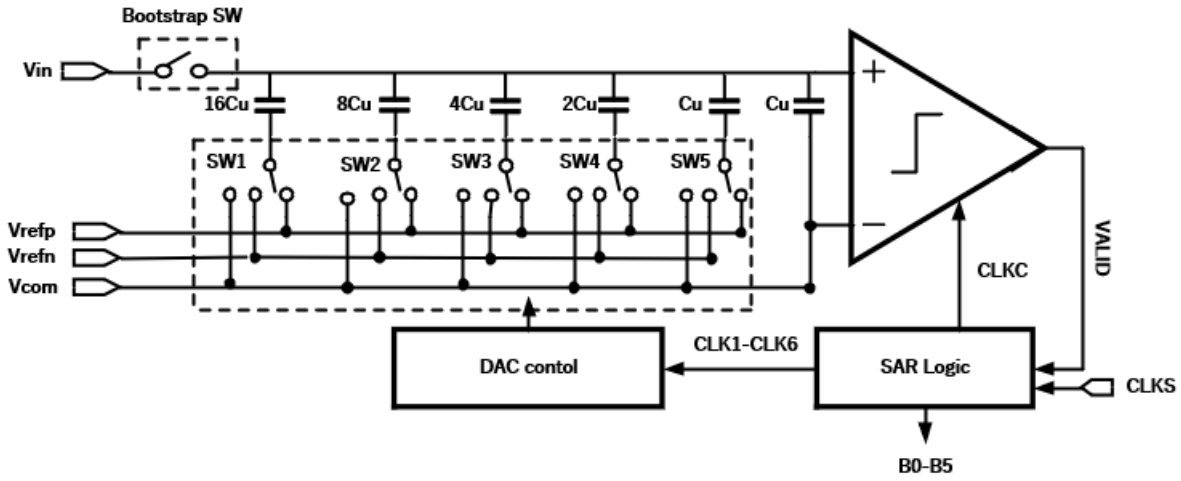


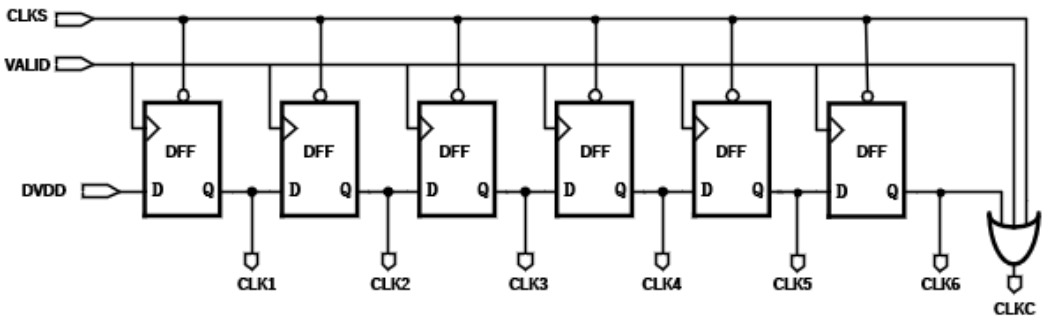
Figure 4.12: The proposed 6-bit single-ended SAR ADC.

4.6.2. The Asynchronous SAR Logic

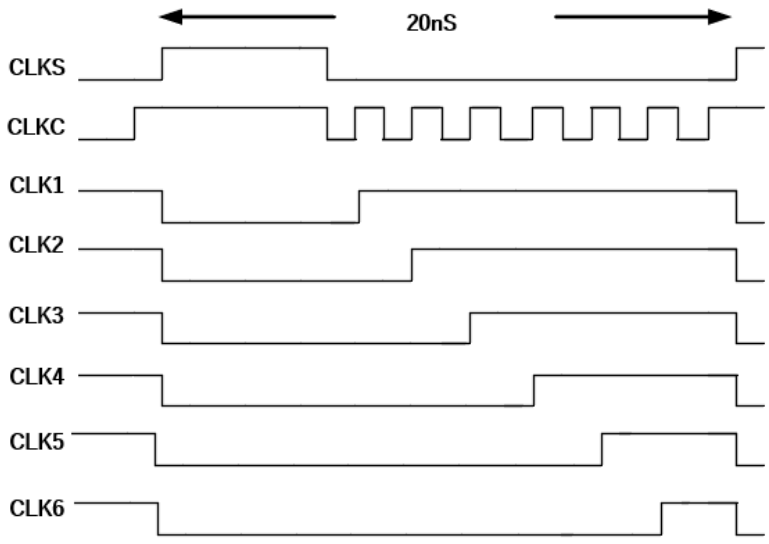
The schematic if the 6-it V_{cm}-based SAR ADC is shown as the Figure.4.12. Because it is a asynchronous operation ADC, only needs one external clock $CLKS$ to trigger all internal clock. The input signal is sampled by the bootstrap switch at the top-plate. As the previous section mentioned, there is no driver amplifier needed. Because the 1-V swing at the input, the FSR of the SAR is 1 V as 1 V for V_{refp}, ground for V_{refn} and 500mV for V_{com}.

The Figure.4.13a is the schematic of the asynchronous logic circuit. The dynamic comparator generates the $VALID$ signal. The $CLKS$ is the control signal of the sampling switches that turns on the comparator at low potential and turns on the comparator at high potential. The sampling phase is about 10% of the whole clock period, 20n second. The $CLK1$ to $CLK6$ are internally generated by the shift D-latches and can be shared by multiple channels.

To be noticed that the asynchronous SAR logic is heavily PVT dependent. The different processing corner and temperature will vary the speed of the D-flip-flops and other digital blocks. As the transient simulation shown in the Figure.4.14a, at the 27°C typical fast corner, the $CLK6$ is generated faster because the fast speed of D-flip-flops, while the condition of 50°C and slow-slow corner shows the $CLK1 - CLK6$ are much delayed. The final $CLK6$ is close to 20 nS. In this design, the 50°C slow-slow corner



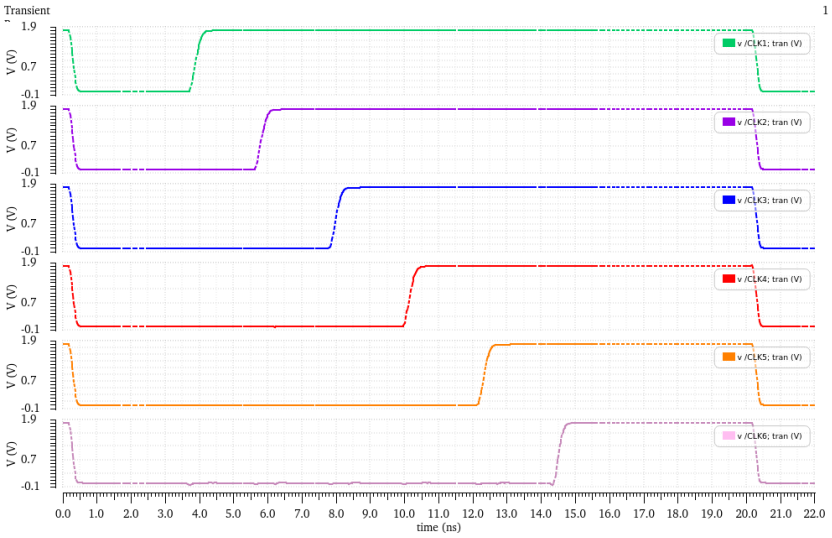
(a)



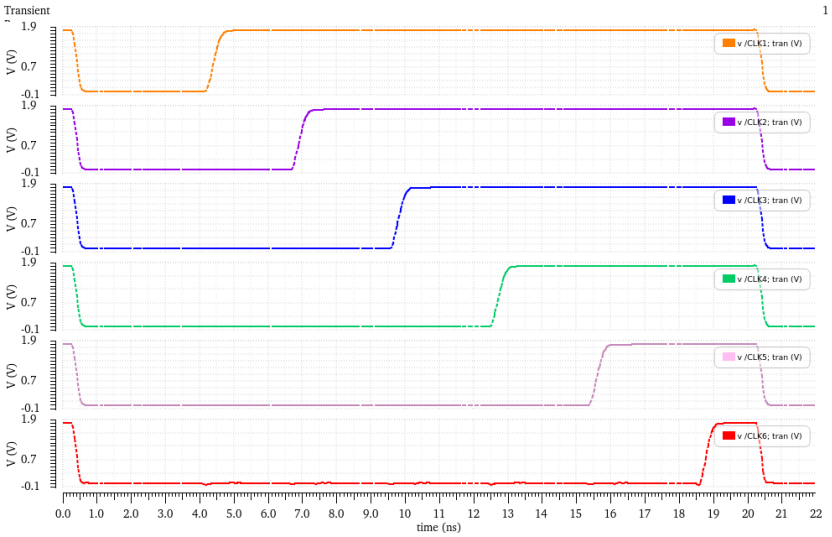
(b)

Figure 4.13: 6-bit asynchronous operation: (a) The schematic of asynchronous SAR logic. (b) The timing diagram of each clock.

is the worst case. the overall design should be carefully considered that the system should work on the worst corner situation.



(a) The time diagram at the condition of 27°C and tt corner



(b) The time diagram at the condition of 50°C and ss corner.

Figure 4.14: The transient simulation outcome of the $CLK1 - CLK6$.

4.7. Comparator

4.7.1. Proposed Comparator

The StrongARM latch topology is one of the most popular dynamic comparator. It has three major benefit: 1) It has no static current, 2) It has the rail-to-rail outputs and 3) the input-referred offset arises from primarily on differential pair [52].

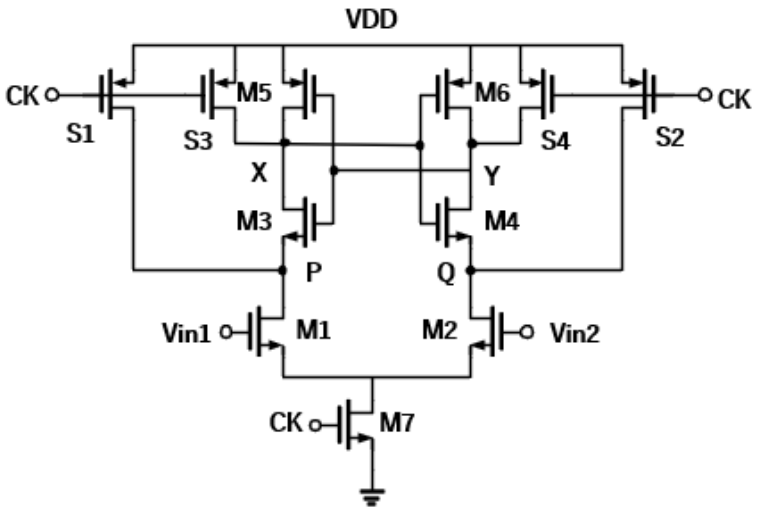


Figure 4.15: The proposed StrongArm comparator topology [11]

The Figure.4.15 indicates the typical StrongArm dynamic comparator. This topology consists of a differential pair $M1-M2$, two cross-coupled pairs $M3-M4$ and $M5-M6$ and four switches $S1-S4$ to precharge the nodes X, Y, P and Q. This circuit begins with the CK is low and the nodes X, Y, P and Q are charged to VDD. When the CK goes high, the circuit goes into amplification mode. Initially, the $M3-M6$ are all turned off. Depending on the input voltage difference, the $V_{in1}-V_{in2}$ will make the nodes voltage P and Q different. The decreased voltage on nodes P and Q will turn on the transistor $M3-M4$, allowing the node voltages on X and Y to decrease associated with the input voltage difference $V_{in1}-V_{in2}$. The last phase is the latch phase, the $M3-M6$ transistors are all turned on and forming the positive feedback and the regeneration time constant can be express as [11]:

$$\tau_{\mathrm{reg}}=\frac{C_{X,Y}}{g_{m_{3,4}}\left(1-C_{X,Y}/C_{P,Q}\right)}. \tag{4.21}$$

The advantage of this topology is that the switches, $S1-S4$, can improve the static offset and input-referred noise. Because most of the noise originated from $M1$ and $M2$ and the KT/C noise are stored by $S1$ and $S2$, and the other transistors come into play only after significant gain has assured. Therefore, the input-referred noise is derived as [53]:

$$\overline{V_{n,\mathrm{in}}^2}=\frac{(V_{\mathrm{GS}}-V_{\mathrm{THN}})_{1,2}}{V_{\mathrm{THN}}}\cdot\left[\frac{4kT\gamma}{C_{P,Q}}+\frac{(V_{\mathrm{GS}}-V_{\mathrm{THN}})_{1,2}}{V_{\mathrm{THN}}}\frac{kT}{2C_{P,Q}}\right]. \tag{4.22}$$

Based on the Equation.4.21 and Equation.4.22, the trade-off between power and noise occurs. Faster speed of the comparator needs less node capacitance on X and Y and larger gm, but all these options will increase the power consumption of the comparator.

The Figure.4.16 shows the p-type input pair StrongArm comparator. In order to work properly in a common-voltage range from $\frac{V_{ref}}{2}$ to ground, the comparator uses a

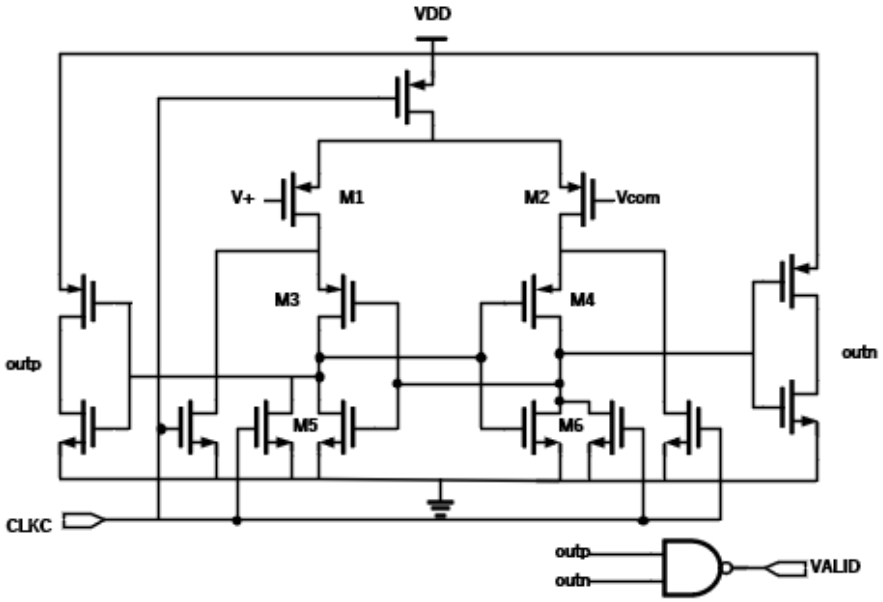


Figure 4.16: The schematic of used p-type StrongArm latch circuit.

p-type input pair. When the $CLKC$ is high, the $outp$ and $outn$ are both low, forming a invalid signal by the NAND gate. When the $CLKC$ is low, it processes the previously mentioned procedures. Once it is finished, the $outp$ and $outn$ has sufficient voltage difference to assert the $VALID$ signal.

The dynamic offset of the comparator must be lower than half of the LSB. Based on Figure.4.15, the switches $S1-S4$ keep $M3-M6$ off initially, thereby reducing their offset contributions. When transistors $M3-M6$ are turned on, their offset contributions are divided by the amplification stage, so, the dominant offset contributors are the input pair. The offset equation can be approximately expressed as:

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right). \tag{4.23}$$

Where the $\frac{\Delta R}{R}$ is the loading resistance formed by the transistor $M3-M6$ which contributes trivial amount of offset as above mentioned. The second term in the Equation.4.23 is the most important one because it is input-signal dependent. If there is no other offset-cancellation technique, the input pairs should have good matching performance and large area [54].

The kick-back of the StrongArm comparator is relatively large compared to other topology [11]. The kickback currents drawn from the inputs from several mechanism, as showing in the Figure.4.17. The node voltage V_p and V_Q fall at unequal rates and couple to the inputs through C_{GD1} and C_{GD2}. There is also a common-mode kickback that the $M7$ turns on and off by the $CLKS$ signal. The $CLKS$ is coupling to the input through C_{GD7} to C_{GS1}. To mitigate the kickback noise, use smaller transistor is the option, which the trade-off is the offset consideration.

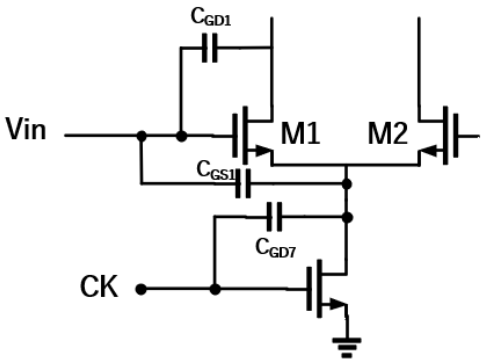


Figure 4.17: The kickback noise path.

4.8. Sample and Hold Switch

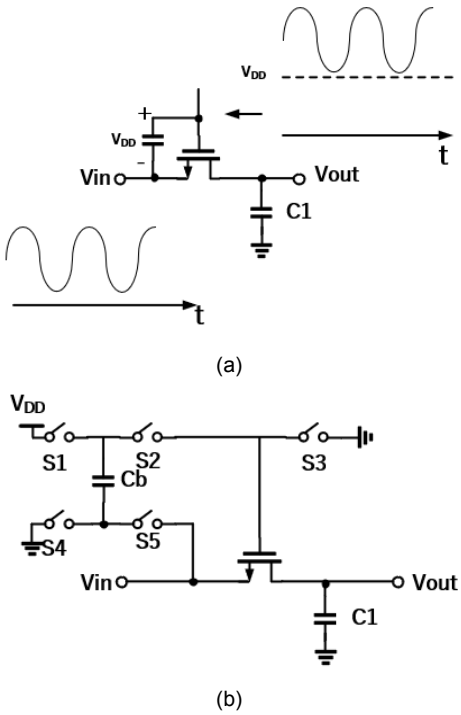


Figure 4.18: (a) Bootstrapping the gate to the input by a constant voltage source. (b) The use of a capacitor to replace the voltage source and switches to allow the transistor to run (on)off and (dis)charge the capacitor.

The principle of bootstrap switch consists on having a constant voltage source between the gate and source of a switch to keep the V_{GS} constant. As shown in Figure.4.18a [55], such topology allows the gate of the transistor above the supply voltage. The Figure.4.18b is the complete circuit for the bootstrapping operation. In the sampling mode, C_b keeps the transistor on. In the hold mode, the transistor is turned off and C_b is recharged to the power supply voltage. In the Figure.4.18b, the switch

$S3$ turns the transistor off, $S2$ and $S2$ disengage the C_b from the sample transistor and $S1$ and $S4$ are used to recharged the C_b.

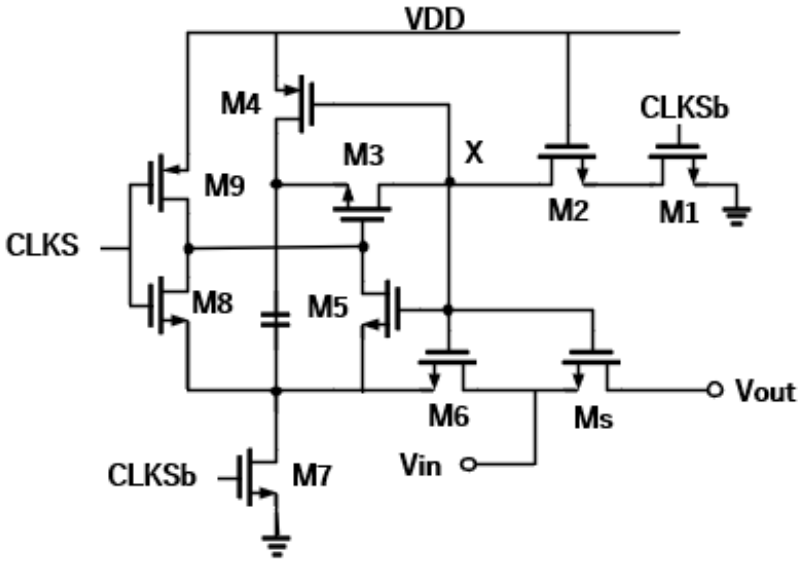


Figure 4.19: The schematic of the bootstrap circuit

The Figure.4.19 shows the complete schematic bootstrap switch. $CLKS$ and $CLKSb$ is a pair of non-overlapping clock signal. To be noticed that, the node X voltage, V_x rises above the V_{DD} in the sampling mode, $M1$ experiences drain-source and drain-gate voltages greater than V_{DD}. It will shorten the device lifetime and must be avoided [55]. This can be accomplished by use of a cascoded transistor, $M2$. Now, the $M2$ limits the V_{DS1} or V_{GS1} to about $V_{DD} - V_{TH2}$. This topology has been widely used in many A/D converter and has been proved to be a robust solution [56].

For the faster speed of sampling, we could use wider width of the M_s, however the drawback is the increased parasitic, C_{GD} and C_{GB}. The parasite capacitance will distort the comparison accuracy by damaging the capacitor array, thus degrades the nonliterary. The selected width is 4 μm, and its parasite capacitance on the drain is 1.4fF which is only 3% of the unity capacitance on the DAC array. The simulated outcome is indicated as the Figure.4.20, the 4 μm width of the sampling transistor M_s perfectly allow the sampling voltage (purple) following the input voltage (red) under the scenario that the total sampling capacitance is $2^6 C_{unit}$ within 2n second period of sampling mode. The gate voltage (orange) tracks the input voltage and is always larger than a supply voltage of 1.8 V. It keeps the V_{GS} of M_s constant to increase the linearity of the SAR ADC as previously explained.

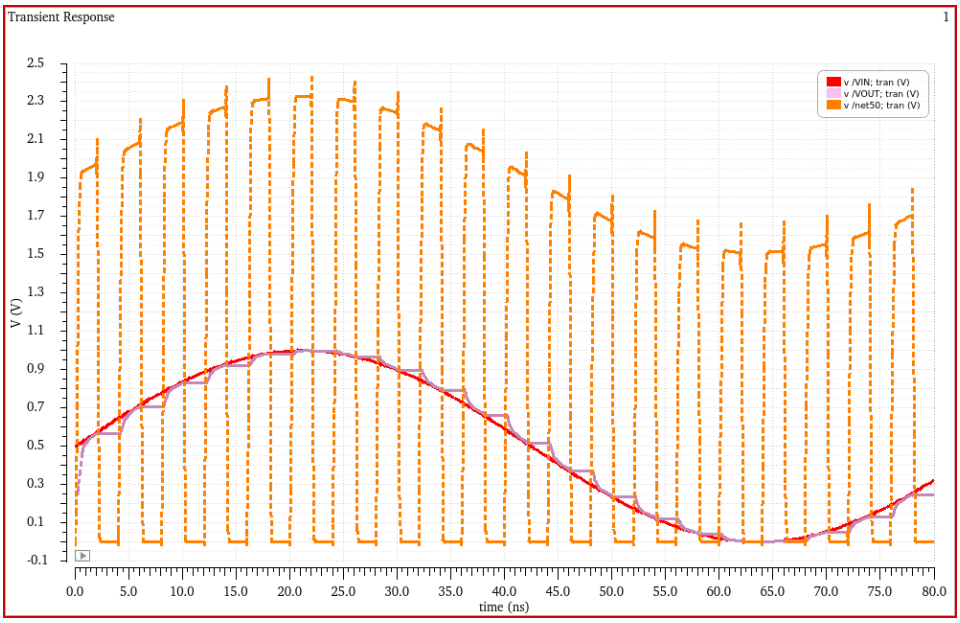


Figure 4.20: The simulated outcome of the bootstrapped switch: The 12MHz input signal (red); the gate voltage on the M_S sampling transistor (orange); the sampled output signal on the capacitor array (purple).

4.9. DAC Control Design

4.9.1. D-latch Design

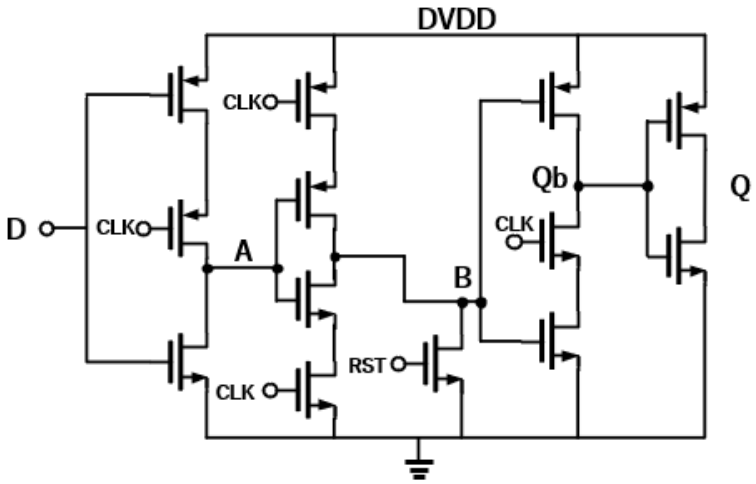


Figure 4.21: The schematic of the positive edge triggered TSPC DFF with the reset function [12].

The True Single-Phase Clock (TSPC) has been widely used in digital design. The TSPC structure consumes less power and occupies less area than other method. For eample, the Clocked CMOS (C2MOS) replaces more complex latch with a four-

transistor dynamic implementation. However, it requires two non-overlapping clock phases. This case, to produce the non-overlapping clock phases require a powerful clock generation function to deal with timing skews [57]. Therefore, making the single-phase clocking D-latch is more attractive.

The Figure.4.21 plots the proposed TSPC DFF structure. It has a positive edge triggered clock pin $CLKS$, and the reset pin RST. When the CLK signal is low and D is also low, node B and consequently the node Qb, maintain their previous state. If the input D changes to high, the node B is pre-charged to high but the output remains unaffected. When the CLK has a low-to-high transition, the output node, Qb will generate the low signal. After that, even if the input D changes to low again, the output will not be affected anymore. Effectively, the output is latched and is waited to output a new digital number when next positive edge clock. The $RESET$ function is activated high. Once the high signal exists on the $RESET$ node, the node B connects to to ground. After the next clock transition from low to high, the Qb will output high value and Q will keep the low value.

4.9.2. DAC Control Logic

Followed by the switching scheme algorithm as the previous section introduced, the DAC control logic circuits are designed to output the corresponding signal to trun on or off the bottom-plate switches from MSB to LSB sequentially. As the Figure.4.22 shows the schematic of the i^{th} bit DAC logic circuit. Based on the V_{cm} switching procedure, there are three switches are needed to be controlled based on the comparison output: the common-mode switch V_{com}, positive reference switch V_{refp} and the negative reference switch V_{refn}. Their voltage references are 500 mV, 1 V and 0 V respectively.

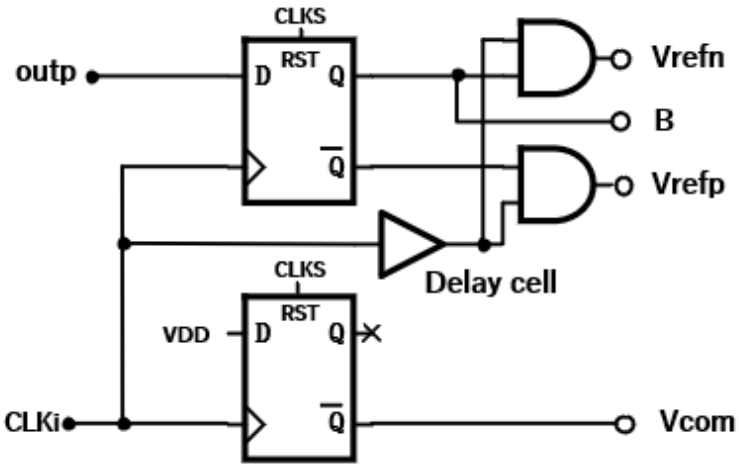


Figure 4.22: The schematic of the DAC control logic.

The V_{com} switches are initially connected to the bottom-plate of the capacitor array. After the comparison is finished by the comparator, the positive comparison output, $outp$, is asserted. The V_{com} switch is then immediately turned off. The state of V_{rn} switch and V_{rp} switch is decided by the $outp$. As the Figure.4.22 shown, the bottom

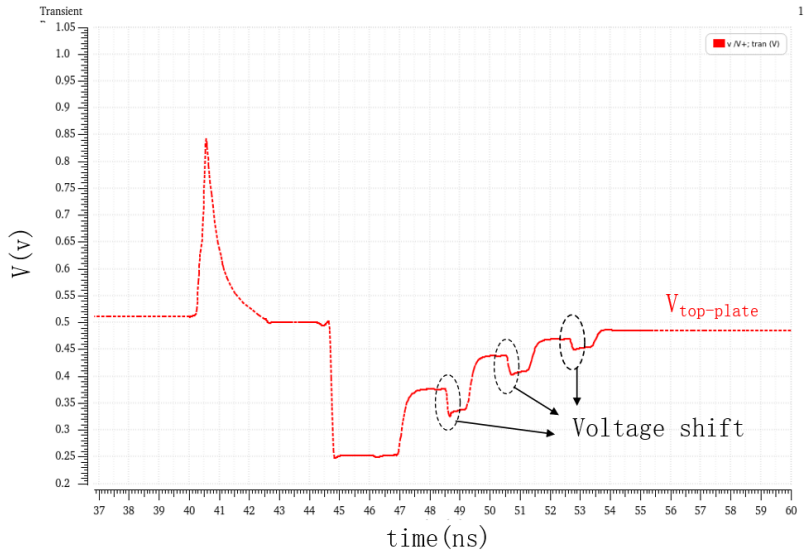


Figure 4.23: The voltage shift pattern on the top-plate due to the switch control timing.

D-latch Flip-Flop (DFF) is to control the V_{com} switch and above DFF is used to control the V_{rn} and V_{com} switch. And the $outp$ is the SAR ADC quantization output, B_i. A delay buffer is needed to eliminate the clock edge overlapping. The delay buffer's structure is a typical current-starved delay buffer that causes 300-600p seconds delay depending on the process corner and temperature. Th purpose of the delay buffer is to turn on the V_{rp} or V_{rn} only after the V_{com} is completely turned off. The Figure.4.23 shows the outcome of the top-plate voltage without the delay buffer. The rising edge and falling edge overlapping causes all switches are turned on. This leads to the charge leakage on the bottom-plate and reflects the voltage shift pattern on the top-plate. This voltage shift will cause the error comparison.

The Figure.4.24 illustrates the timing diagram of the MSB-bit ($i = 6$) DAC logic control outcome. The two different cases are depended on the $outp$, as previously introduced, the $outp$ is high will turn on the V_{rn} switch and is low will turn on the V_{rp} switch. The V_{com} is turned off correspondingly.

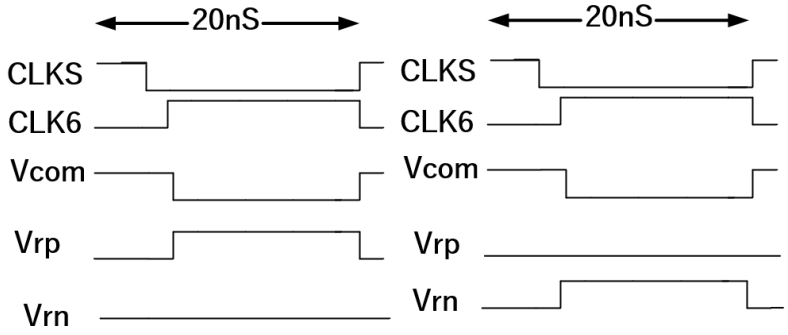


Figure 4.24: The case one: $outp$ is low (left). The case two: $outp$ is high (right).

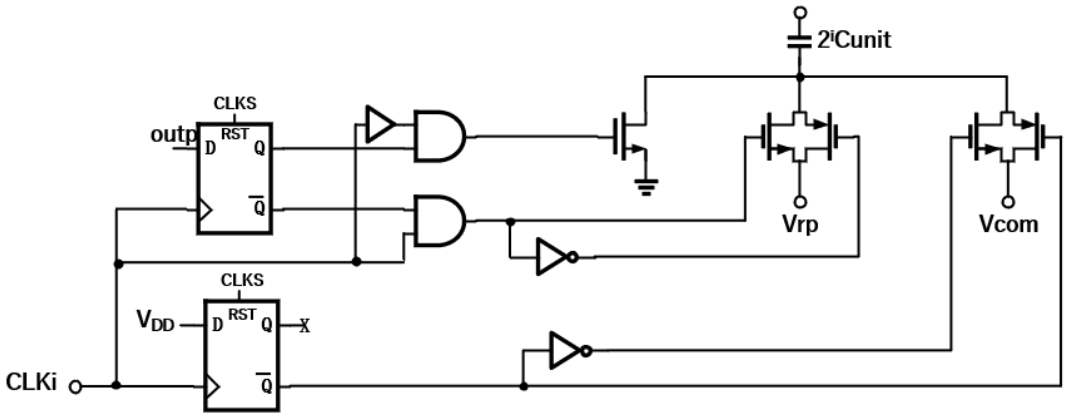


Figure 4.25: The switch control circuit.

The Figure.4.25 shows the overall bottom-plate switch control circuit. The V_{rp} and V_{com} use the transmission gate topology as the switch to have the smallest on-resistance and better charge-injection rejection performance. In order to have sufficient settling time on the bottom-plate at the time between two comparing periods interval, the width of the bottom switch should be larger for higher order bit. In this design, the 6-bit's bottom-plate switch has the width of 4 μm, 2 μm for the 5-bit, 1 μm for the 4-bit and 0.5 μm for the bit-3 to 1.

The Figure.4.26 plots the final measured top-plate voltage changes. As the 6-bit MCS SAR ADC algorithm, after the 6 cycles of comparison, the top-plate voltage is close to the 500 mV common-mode voltage V_{com} and the deviation between the V_{com} is less than the LSB.

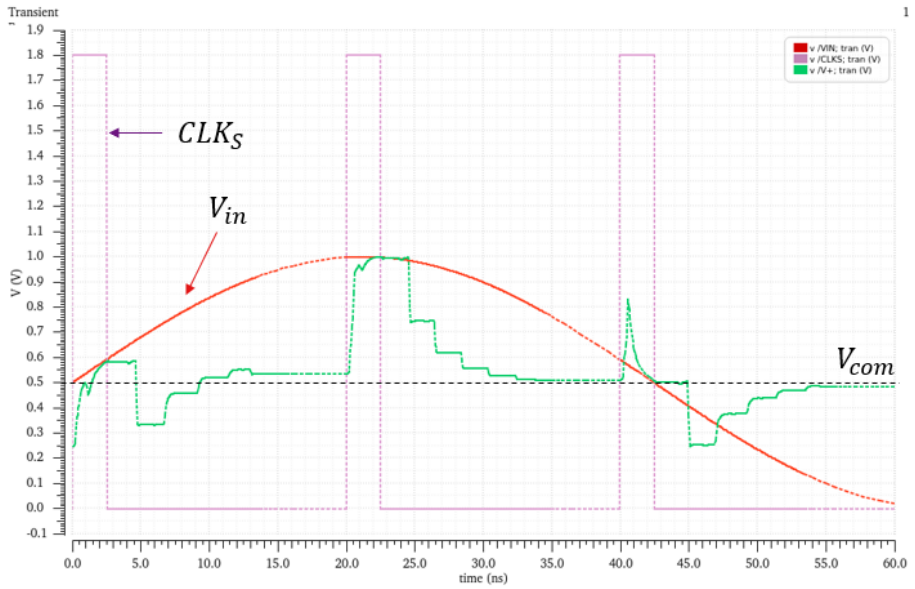


Figure 4.26: The top-plate voltage (green).

4.10. Measured Performance and Power Consumption

In order to find the dynamic performance of the ADC, the coherent sampling technique is needed. Based on the coherent sampling theory, the input frequency f_{in} and sampling frequency f_s has the following relationship [58]:

$$f_{in} = \frac{M \times F_s}{N}. \tag{4.24}$$

Where the N is the FFT resolution point. In this simulation, The N is set to be 1024. The M is the prime number. When the $M = 241$, the $f_{in} = 11.76MHz$, which is close to 12 MHz.

The dynamic performance based on the schematic simulation outcome is shown in the Figure.4.27. The ENOB is 5.89 bit that is close to the ideal 6-bit. For different corner and temperature, the performance is slightly different. The worst case is the 50°C ss corner that the SNDR is degraded to 35.6 dB. But it is still larger than the 30 dB signal DR. The Figure.4.28 plots the simulation under the condition of slow-slow corner (CDAC, bootstrap switch and comparator are based on post-layout), the SNDR is further degraded to 33.8 dB. Comparing with the ideal schematic simulation, the post-layout performance shows a 1.8 dB decreasing.

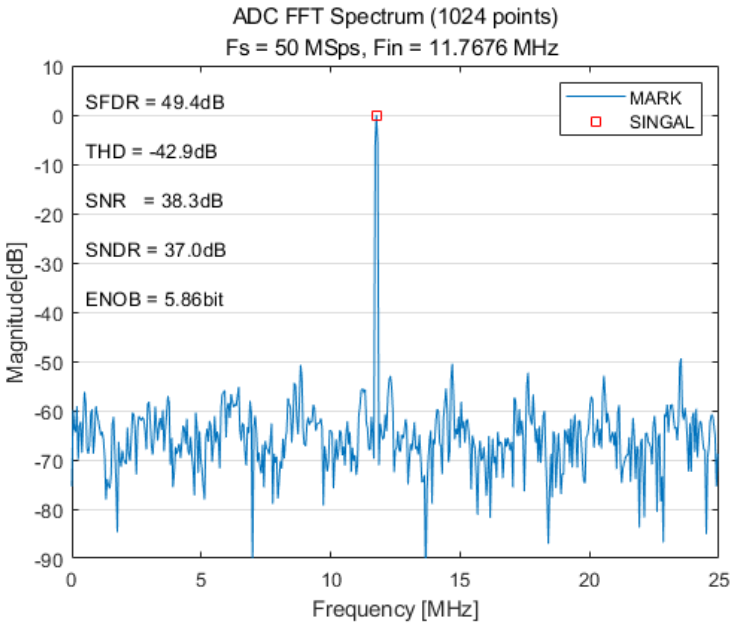


Figure 4.27: FFT of the digital output, as the input signal is a 11.76MHz full-scale sine wave sampled at 50 MS/s.

The power consumption of each block is summarized in table.4.1. And the power consumption from each block is plotted as the Figure.4.29. The digital block takes the most power percentage. The Table.4.2 is the summarized ADC performance.

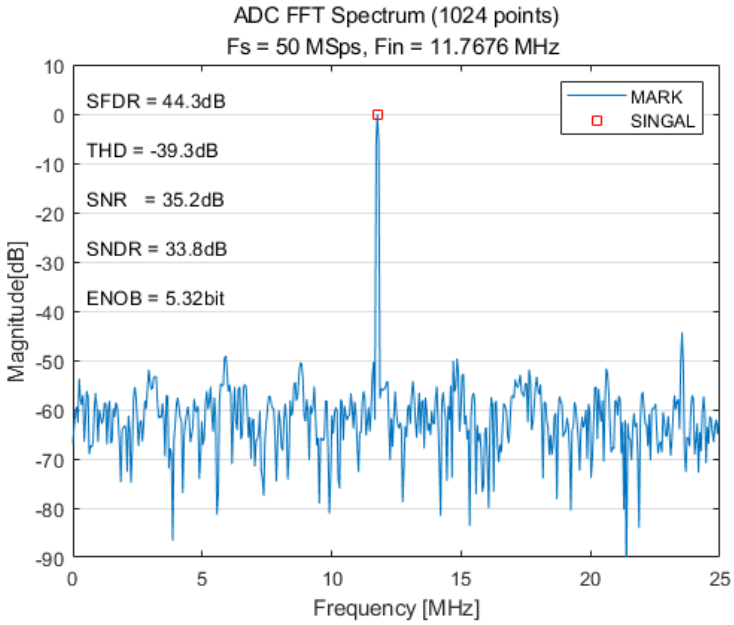


Figure 4.28: FFT of the digital output based on the post-layout of CDAC, bootstrap switch and comparator at ss corner.

Table 4.1: The measured power consumption.

Analog Current	42μA
Digital Current	180μA
DAC Current	9μA
Total Current	231μA
Total Power	415.8μW

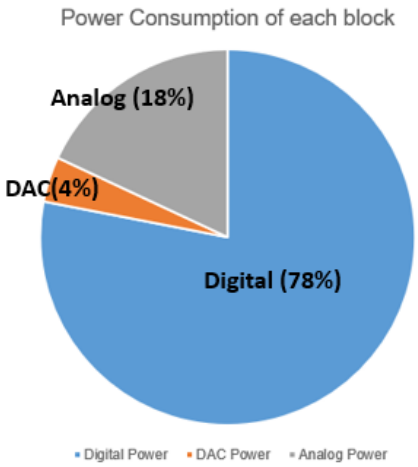


Figure 4.29: The power composition of the ADC.

Table 4.2: The summarized ADC performance.

Specification (unit)	result
Technology	0.18μm TSMC
Resolution (bit)	6
Sampling Rate (MS/s)	50
Input Range (Vp-p)	1
Supply Voltage (V)	1.8
Unit capacitance (fF)	33.43
Active Area (mm^2)	0.002
SFDR (dB)	49.4 (11.76MHz)
SNDR (dB)	37 (11.76MHz)
ENOB (bits)	5.86 (11.76MHz)
Power (μW)	415.8
FOMw (fJ/Conv.-step)	71.4

4.11. Layout Consideration

In order to ensure the minimum capacitance mismatch in the C-DAC, the unit-sized capacitors with surrounding dummy capacitors are generally used. This approach enables every unit capacitor sees the same surrounding environment. And in order to minimize the effects of the doping gradients, the common-centroid layout arrangement is also needed for good matching [59]. However, the surrounding dummy will increase the area, the used unit capacitance in this design already has a safe margin to tolerance the capacitance mismatch. The final C-DAC layout is shown as the Figure.4.30, each square block is the unit capacitance with the number of bit annotated at the center. The advantage of the floorplan is that it has the shortest routing-out wire.

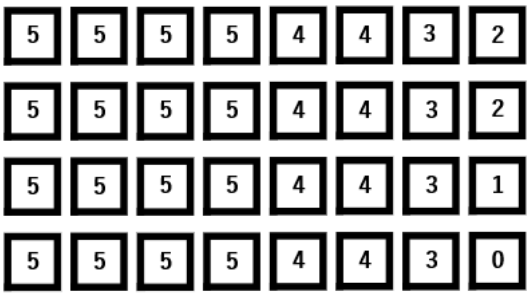


Figure 4.30: The C-DAC layout floor plan from bit-0 to 5.

4.12. Overall Layout

The overall layout should be compact and a square shape. As the Figure.4.31 shown, the AFE part and the ADC part together take 150μm×150μm of total chip area. The digital block is customized designing, therefore the layout of the digital block is not very area-efficient compared to the synthesis layout from the Verilog auto-generation function. But the area consumption of the SAR ADC is already very small which is comparable to the analog signal chain.

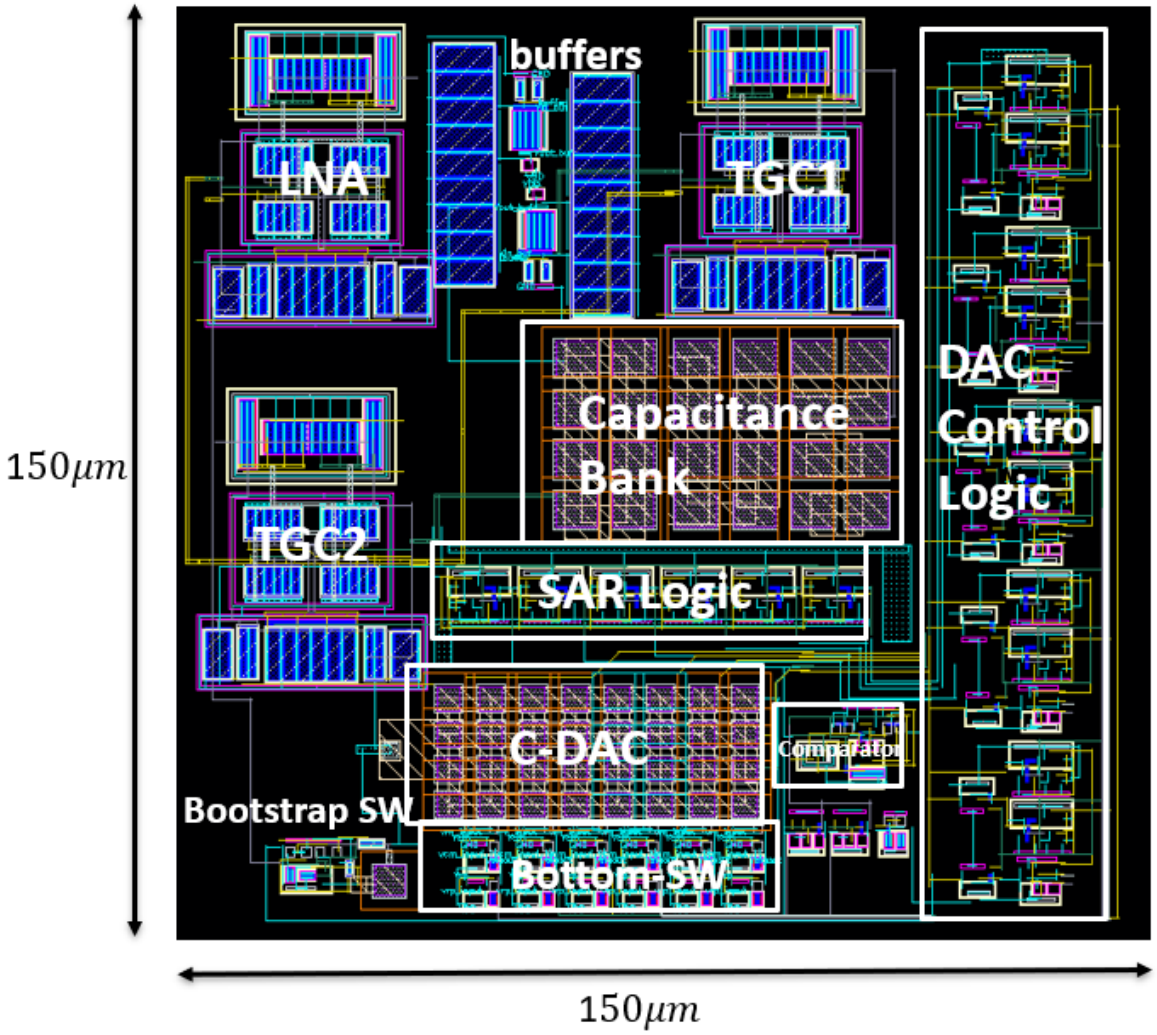


Figure 4.31: The final layout including the AFE and ADC.

5

Conclusions

In this thesis project, I worked as a research member of the Ultrasound Group team under the Bioelectronics department. My work is focused on the design of a front-end ASIC of interfacing the PMN-PT transducer for imaging of the vagus nerve. The signal chain enables the received echo to be digitized locally, allowing for the digital beamforming. The features of the imaging signal chain are:

- The area-efficient arrangement that uses two amplifiers to provide the variable gain allows the signal chain could provide up to 62 dB voltage gain and many gain steps.
- The single-ended asynchronous 6-bit SAR ADC is very power and area efficient. Comparing with the power consumption of 940 μW at the analog signal chain, the SAR ADC only consumes 415.8 μW and the consumed chip area of the SAR ADC is slightly less than the analog signal chain.
- The overall layout area is 150 $\mu\ m^2$ and total power consumption is below 1.5 mW (excluding the shared biasing network and external clock). Comparing with the prior works, it is the one of the best power-efficient approach considering the signal bandwidth.

5.1. Thesis Contribution

My contribution towards this project including:

- Literature study on the ultrasound neuromodulation system and advanced imaging circuit. Choose the best topology to fulfill the objective.
- Use MATLAB simulation to validate the process that the ultrasound wave focuses on the human's vagus nerve in the real case. The original MATLAB code is from the group supervisor. I worked on establishing the model to mimic the vagus nerve system and to find out the received echo.

- Schematic design and verification of the signal chain, including the low-noise amplifier, variable gain amplifiers and buffers. The verification includes the PVT corner and Monte-Carlo simulation and post-layout testing.
- System consideration and schematic design on a low-power and low-area SAR ADC including both the customized digital logic part and analog section. The final verification is also done on PVT corner testing and generate MATLAB script code to measure the dynamic performance.

5.2. Future work

After the final test bench and layout of the imaging signal chain, there are many potential improvements could be done in future system optimization, as the following summarized:

- The SAR ADC digital blocks are constructed by the customized digital cell. Using the Verilog approach to synthesis the digital block would allow the more compact area size and lower power consumption.
- In this design, the 6-bit 1-V full scale SAR ADC has a relaxed LSB with a wide safe margin that is far away from the noise, dynamic offset and kickback voltage combined. One way could do is decreasing the full scale of the SAR ADC to reach a smaller LSB without degrading the performance of the ADC severely. It also relaxes the requirement of voltage gain on LNA and TGC, causing the whole system to be more compact and consume less power.
- The current source, voltage source and digital output load are needed to complete the final system. In this thesis project, these elements are generated in the ideal condition.

The achievements of this project is only a signal chain for imaging purpose. The future work should investigate how to fully integrate the imaging and transmitting systems with 2-D array transducers. Because the wearable nerve probe needs thousands of independent piezo-material elements, the density of the elements makes their individual wiring very changeable. Based on the prior works of the high-intensity integrated circuit design, some approaches have been successfully demonstrated such as the ASIC circuit with the on-chip signal processing modules to reduce the fan-out cables [60]. In order to suppress the ringing and crosstalk of the piezo-elements, a specially designed interconnect layer between the 2-D array elements and the ASIC is designed to minimize the damping pattern that couples to neighboring channels [60]. For ASIC integrating with the PMN-PT piezo-material, the PMN-PT crystal construction also needs investigation. This is associated with the manufacturer to provide production with the stable capability to dice kerfs between two adjacent elements, ensuring the mechanical and electrical separation of the individual transducer elements.

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Acronyms