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Multiobjective Design and Benchmark of Wide Voltage Range Phase Shift Full-Bridge DC/DC Converters for EV Charging Application

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***Abstract*— This article presents an analysis, multiobjective design, and benchmark of three modified 3 phase shift full-bridge (PSFB) converters that are well-suited for electric vehicle (EV) battery charging applications, covering both typical battery voltage classes (400 and 800 V). These three modified PSFB converters, denoted as the t-PSFB, r-PSFB, and i-PSFB converters, have the ability to reconfigure and provide better efficiency performance in the wide voltage range necessary for public EV battery charging applications. In this article, the characteristics and design considerations of these reconfigurable PSFB converters are discussed in detail. A multiobjective converter design process is proposed to optimize the average efficiency, normalized cost, and power density of the magnetic components and heat sinks. This design process employs the correlations between the cost and performance indexes of the key components derived based on open and accessible components' data to estimate the design objectives. In this way, the design process is not constrained by certain component choices, making it easier to identify the most advantageous design. A benchmark study is conducted among the reconfigurable PSFB topologies and the conventional PSFB circuit using the proposed multiobjective design process. To validate the analysis, a close-to-Pareto-front 11-kW, 45-kHz r-PSFB converter prototype with 640–840-V input voltage and 250–1000-V output voltage ranges is developed and tested.**

***Index Terms*— DC/DC converter, electric vehicle (EV) charging, phase shift full bridge (PSFB), reconfiguration, wide voltage range.**

I. Introduction

THE phase shift full-bridge (PSFB) isolated dc/dc converter shown in Fig. 1(a) is a popular circuit in the application of electric vehicle (EV) charging, notably, because this circuit features a current source behavior, which facilitates the startup and the control of the battery charging profile. In addition, this circuit technology is mature, power efficient, simple to operate, and well-established in several other applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. Unfortunately, the conventional PSFB (conv-PSFB) topology is challenged to keep the high efficiency within an extensive output voltage range. The reason is that the efficiency of the PSFB technology drops as the phase shift angle increases (or equivalent duty cycle and, consequently, the output voltage decrease).

Most EVs launched last decade have a nominal battery voltage of around 400 V. As of today, the component technology for this voltage class is well-established with several automotive-qualified components available. Currently, the manufacturers of high-end EVs are moving toward the 800-V battery architectures [13], [14], [15], [16] because the higher voltage results in weight saving across the EV and the potential reduction of the battery charging time while using a public dc-fast charging infrastructures, i.e., as the current rating of the public charger cables is limited to 350 A, the high voltage will potentially enable higher power injection into the battery bank where the limits will be imposed by the public charger and the thermal management of the battery. Therefore, today, the public dc-type EV charging infrastructures should be able to supply power efficiently to both 400- and 800-V EV battery classes.

Studies have been conducted to extend the PSFB-type converter's voltage range while keeping high efficiency. The work developed in [3] proposes a hybrid-switching PSFB converter that provides for the H-bridge converter a wide zero-voltage switching (ZVS) range for the leading leg and zero-current switching (ZCS) for the lagging leg. Interestingly, the freewheeling circulating losses can also be improved, and the undesirable voltage overshoots at the rectifying stage can be clamped well. However, additional passive components (two diodes, a capacitor, and an inductor) are needed, and the complexity of the converter increases. The work in [4] proposes a secondary-side PSFB converter that extends the soft-switching operation and improves the circulating current losses, but it comes with the cost of two additional switches and complex control. In [9], a ZVS full-bridge dc/dc converter is proposed, incorporating a diode clamping circuitry on the primary side for the voltage ringing clamping, and uses an asymmetrical PWM modulation together with an additional auxiliary inductor to reduce circulating current losses. Unfortunately, none of these studies have investigated and proved with experimental results the high-efficiency performance in the voltage range of 400- and 800-V EV charging.

Based on the idea of a reconfigurable PSFB converter [17], [18], [19], [20], the study in [12] provides a solution for the

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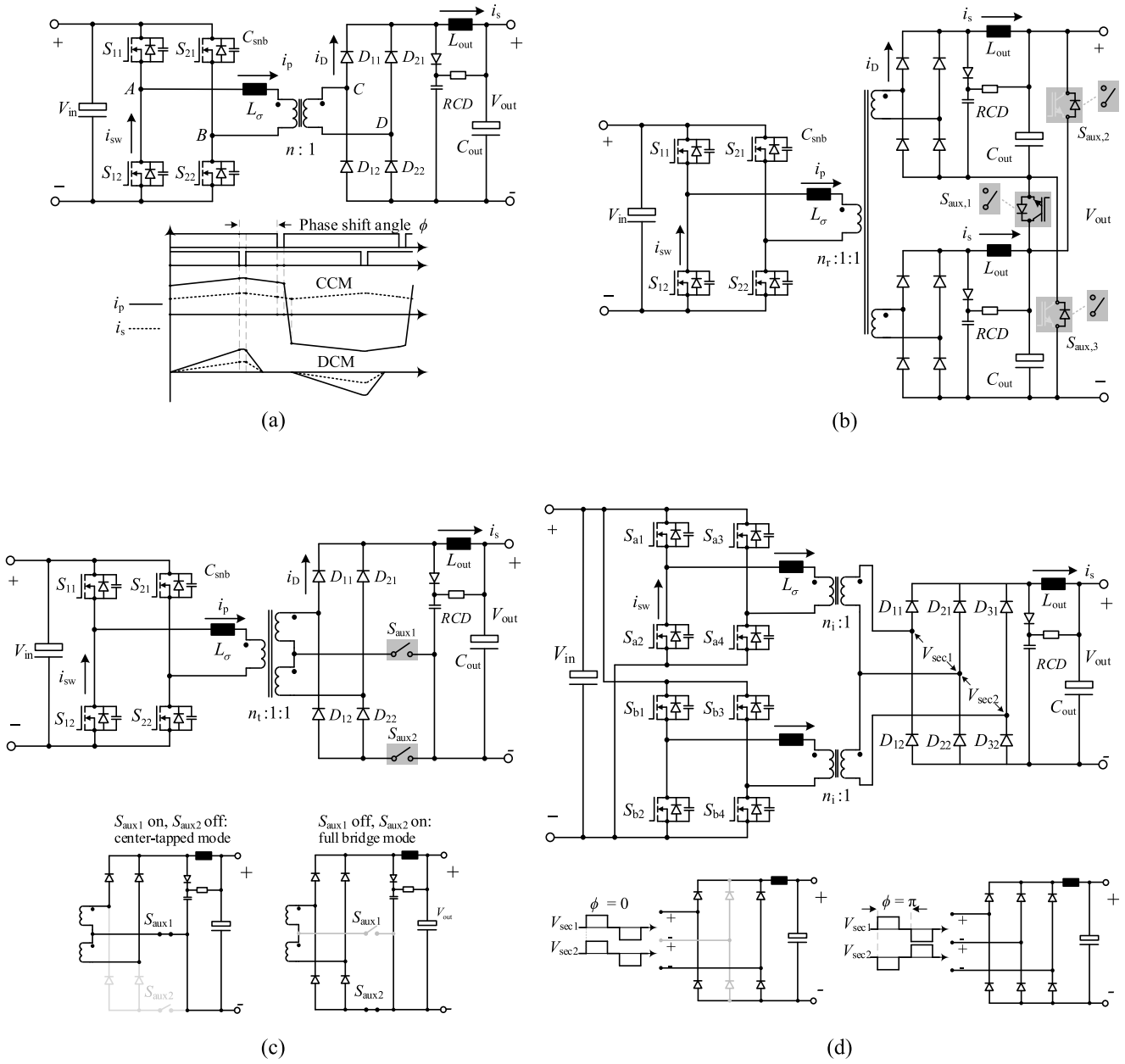

Fig. 1. Schematics of the conv-PSFB converter and three modified PSFB converters. (a) Conventional PSFB converter and its typical waveform in the CCM and the discontinuous conduction mode (DCM). (b) r-PSFB converter. (c) t-PSFB converter. (d) i-PSFB converter.

extensive voltage range necessary in today's market of public EV charging stations (e.g., 250–1000 V). This circuit, denoted here as the r-PSFB converter, employs a two-secondary-winding transformer, two diode rectifiers, and three auxiliary switches, as shown in Fig. 1(b). By controlling the connection of the auxiliary switches, the two secondary sides can be connected in series when the required output voltage is high or in parallel when the needed output voltage is low. As a result, rectifier diodes with a halved voltage rating and transistors with a halved current rating can be utilized. Most importantly, the range of the phase shift control angle needed for the wide voltage range is also halved.

Instead of using two diode rectifiers with the two-secondary-winding transformer like the r-PSFB converter, one single diode rectifier can be used together with two additional auxiliary switches to make a reconfigurable PSFB converter, as shown in Fig. 1(c). This converter, which is first introduced in the literature by this article, is denoted here as the t-PSFB converter. The two-secondary-winding transformer and diode bridge of the t-PSFB converter can be configured into a full-bridge mode or a center-tapped mode by the connection of the auxiliary switches. Similar to the r-PSFB circuit, this t-PSFB converter reduces the operational phase shift control angle for the wide voltage operation. The number of rectifier diodes needed is half compared to the r-PSFB circuit, but higher voltage rating rectifier diodes are required simultaneously.

In the study of Wu et al. [21], an *LLC* resonant converter with a hybrid rectifier is proposed. This *LLC* converter has two H-bridge inverters on the primary side, two transformers,

and a three-leg diode bridge rectifier. By controlling the phase shift of the PWM signals of the two H-bridge inverters, the LLC converter can be operated as if the two circuits are connected in series or parallel. With this idea, the PSFB converter can be modified into an interleaved PSFB converter with a hybrid rectifier, as shown in Fig. 1(d). This converter, denoted as the i-PSFB, has the same performance regarding the reduction of operational phase shift in a wide voltage range like the r/t-PSFB converters but has doubled transistor counts and different transformer designs. The 1700-V rating diodes are required for the EV charging application aiming at an 800-V class battery as load.

These converters shown in Fig. 1 are well-suited for the wide voltage range public EV charging application due to their characteristic of reconfiguration. However, the optimal design and benchmark of these converters in terms of cost, power density (PD), and efficiency performance have not been done. The cost estimation in the academic research of power electronics is challenging, primarily due to the poor availability of the components' cost data. In [22], component cost models of switched-mode power converters with an approximate rated power between 5 and 50 kW are derived. These models are useful for engineers as they can be incorporated into the converter design process, and they are also used in [23] and [24]. These component cost models are largely dependent on variables related to physical component properties, making them not so straightforward to implement. Moreover, a large database acquired from manufacturers is needed for a better fitting, which is not easily accessible.

This article aims to identify which one of the three modified PSFB converters is the most advantageous in the wide voltage range EV charging application, considering an 11-kW power rating, 30-A maximum output current, 640–840-V input voltage, and 250–1000-V output voltage range. To do so, a multiobjective design and benchmark process is proposed, with the normalized cost, average efficiency, and PD of the magnetic components and heatsink being the objectives of interest. First, the essential data of the components are collected from the easily accessible database of the redistributors. The data include the cost per commercial off-the-shelf (COTS) component, conduction resistance of the transistors and rectifier diodes ($R_{\mathrm{ds(on)}}$ and $R_{\mathrm{D(on)}}$), switching loss of the transistor ($E_{\mathrm{on/off}}$), the capacitive charge of the rectifier diodes (Q_{c}), and weight and volume of the magnetic cores (M_{c} and V_{c}). It is worth mentioning that the data need to cover various current and voltage ratings to compare topologies using different component requirements. Second, the correlation of cost versus the performance indexes of the components such as $R_{\mathrm{ds(on)}}$, $E_{\mathrm{on/off}}$, $R_{\mathrm{D(on)}}$, Q_{c}, M_{c}, and V_{c} is established by processing the data with curve-fitting methods. Different from the physical property-based cost models used in [22], [23], and [24], the correlations directly connect the cost information to the performance indexes of the components based on the open and accessible data, without having a model in between. Therefore, these correlations are more straightforward to implement. With the obtained correlations, a collection of the possible designs by sweeping through a range of $R_{\mathrm{ds(on)}}$, $E_{\mathrm{on/off}}$, $R_{\mathrm{D(on)}}$, Q_{c}, M_{c}, and V_{c} can be made. In this way, the designs are not limited by certain component choices, and the correlations can be directly utilized by other designers without components' database. The normalized cost of the possible designs, including the cost of semiconductors, magnetic components, gate drivers, heatsinks, and PCB boards, can be calculated, as well as the PD of the magnetic components and heatsinks. In addition, the average efficiency performance can be calculated based on the components chosen using the analytical models of the converters. As a result, a design space is formed based on the possible designs. Finally, the advantageous converter design can be selected.

The contribution of this article is given as follows.

1) The design guideline of three reconfigurable structure PSFB converters that are well-suited for the wide voltage range public EV charging application is elaborated. Among the three reconfigurable structure PSFB converters, the t-PSFB converter that utilizes two auxiliary switches with a three-winding transformer is a new PSFB converter topology that is first introduced in this article.
2) A multiobjective converter design process that considers the normalized cost, PD of the magnetic components and heatsinks, and the average efficiency performance is introduced. The accessible components' data from well-known redistributors are collected and processed to uncover the correlation between the cost and the performance factors of the components.
3) The multiobjective design and performance benchmark of the 11-kW t/r/i-PSFB converter and conv-PSFB converter for the wide output voltage range (250–1000 V) EV charging application is presented. This design benchmark is particularly important because it identifies the i-PSFB and r-PSFB converters as outstanding solutions for the future EV market.

This article is arranged as follows. In Section II, the operation principles of the three modified PSFB converters are introduced. Section III presents a basic comparison of the three converters at the circuitry level. In Section IV, the open and accessible data from the well-known redistributors are collected, based on which the correlations among the components' cost and performance indexes are calculated. In Section V, the multiobjective design process of the converters is introduced. The design space of the converters is formed based on the design process. The normalized cost, PD of the magnetic components and heatsinks, and the average efficiency performance of the converters designs are benchmarked and interpreted. Finally, a close-to-Pareto-front 45-kHz r-PSFB prototype converter is built to verify the design and benchmark results. The prototype's operational waveform, efficiency performance, cost, and PD information are also presented. The conclusion of the work is presented in Section VII.

II. Operation Principles of the Reconfigurable PSFB Converters

A. conv-PSFB Converter

The conv-PSFB converter, as shown in Fig. 1(a), consists of an H-bridge inverter, a high-frequency isolation transformer

with an equivalent leakage inductance L_σ referred to the primary side and a diode-bridge rectifier on the secondary side, and a second-order low-pass output passive filter consisting of L_{out} and C_{out}. Note that the diode-bridge rectifiers are sometimes replaced by a synchronous rectifier using unipolar transistors to reduce conduction losses. The optional lossless turn-off snubber capacitors C_{snb} at the full bridge are for reducing turn-off switching losses (but it will narrow the ZVS turn-on range), and a voltage clamping RCD snubber circuit is used at the secondary-side between the terminal C and D for limiting the voltage spikes on the secondary side diodes [25].

The PSFB converter is typically controlled with fixed switching frequency by phase shift modulation where the two half-bridge legs are operated with 50% duty cycle, as shown in the typical waveform depicted in Fig. 1(a). The phase shift angle Φ refers to the asynchronization between the operation of the two half-bridge legs. When Φ is null, the diagonal pair of transistors (S_{11} & S_{22}, or S_{12} & S_{21}) turn on and off synchronously, making the primary side voltage v_{AB} alternate between $+V_{\text{in}}$ and $-V_{\text{in}}$, which is equivalent to a bipolar modulation of the H-bridge inverter. When Φ is nonnull, the synchronization is broken, and the parallel pair of transistors (S_{11} & S_{21} and S_{12} & S_{22}) are able to be kept turned on at the same time, creating a third circuit state, that is, $v_{\text{AB}} = 0$ V, leading to a controllable unipolar modulation action. Due to the impressed i_{p} caused by L_σ and inverter bridge capacitance, the switching transition in each half-bridge leg creates a lowered di_{p}/dt and dv_{AB}/dt on the primary side, making the ZVS turn-on possible and lowering the turn-off losses of the transistors. A complete description of the operation of a PSFB converter can be found in [26].

B. r-PSFB Converter With Reconfigurable Secondary Side

Fig. 1(b) shows the schematic of the r-PSFB converter [12]. The three-winding transformer is used, with the turns ratio of n_{r}:1:1. The primary side is identical to that of the conv-PSFB converter. Each of the secondary sides is connected to a diode-bridge rectifier, an output filter (L_{out} and C_{out}), and an RCD snubber circuitry. Three auxiliary switches $S_{\text{aux},1,2,3}$ connect the two secondary sides and enable two different configurations according to their switching states. The auxiliary switches can be implemented by either mechanical switches or semiconductor transistors.

The reconfiguration of the r-PSFB converter operates as follows. When $S_{\text{aux},1}$ is kept on and $S_{\text{aux},2,3}$ are kept off, the two diode rectifiers are connected in series, making V_{out} twice the individual diode rectifier output voltage. When $S_{\text{aux},2,3}$ are kept on and $S_{\text{aux},1}$ is kept off, the two diode rectifiers are connected in parallel. As a result, V_{out} equals the individual diode rectifier output voltage, but the output current is shared by the two rectifiers.

C. t-PSFB Converter With Reconfigurable Secondary Side

Fig. 1(c) shows the schematic of the t-PSFB converter. A three-winding transformer is used, which has one primary and two secondary windings, with the turns ratio of n_{t}:1:1. The primary side is identical to that of the conv-PSFB converter. The additional secondary winding and auxiliary switches ($S_{\text{aux}1,2}$) allow the secondary side to be configured into a regular full-bridge diode rectifier or a center-tapped diode rectifier.

The reconfiguration of the t-PSFB converter operates as follows. When $S_{\text{aux}1}$ is kept off and $S_{\text{aux}2}$ is kept on, the two secondary windings are in series, and the t-PSFB works the same as a conv-PSFB converter with full-bridge diode rectifier. When $S_{\text{aux}1}$ is kept on and $S_{\text{aux}2}$ is kept off, the secondary side is configured into a center-tapped rectifier. This is shown in Fig. 1(c).

D. i-PSFB Converter With Hybrid Diode Rectifiers

Fig. 1(d) shows the schematic of the i-PSFB converter. Two H-bridge inverters fed by V_{in} are connected in parallel on the primary side, and they can be interleaved. A hybrid three-legs diode rectifier is connected to the two H-bridge inverters by two transformers with the turns ratio of n_{i}:1. Note that, instead of parallel connecting the H-bridge inverters, as shown in Fig. 1(d), these could be alternatively connected in series, for instance, when connected to a bipolar dc grid.

The interleaving of the i-PSFB converter operates as follows. The two H-bridge inverters operate the same as that of the conv-PSFB converter, with an interleaving phase shift ϕ between them. When $\phi = 0$, the upper side transformer secondary side voltage V_{sec1} is in phase with the lower side V_{sec2}, resulting in the series connection of the two transformers' secondary windings. In this series connection mode, the first and third diode bridge legs ($D_{11,12}$ & $D_{31,32}$) process all the current and rectify the sum of V_{sec1} and V_{sec2}, while the second diode bridge leg ($D_{21,22}$) is placed in the OFF-state. When $\phi = \pi$, V_{sec1} and V_{sec2} are in reverse polarity, resulting in the parallel connection of the two transformer's secondary windings, which is facilitated by the added diode bridge leg, as shown in Fig. 1(d). In this parallel connection mode, the first and third diode bridge legs are in parallel and share the inductor impressed current equally, while the second diode bridge leg processes the whole inductor current. Therefore, for even power loss balance in the rectifying stage, the diodes $D_{21,22}$ could be assembled with the hard paralleling of two diodes of the same technology used in the bridge legs containing $D_{11,12}$ and $D_{31,32}$.

III. Circuit-Level Comparison Among Conventional PSFB, r-PSFB, t-PSFB, and i-PSFB Converters

A general comparison of the components used among the conv-PSFB, r-PSFB, and i-PSFB converters is conducted. The comparison parameters include the component count and the voltage and current stresses of the components. With these parameters, the cost and losses can be calculated for these converters for a primary evaluation.

A. Transformer Turns Ratios n

The transformer's turns ratio n of the conv-PSFB converter can be determined with

$$n = k V_{\text{in(min)}} / V_{\text{out(max)}} \tag{1}$$

TABLE I
EQUIVALENT PARAMETERS OF THE T,R,I-PSFB CONVERTERS

conv-PSFB	t-PSFB		r-PSFB		i-PSFB	
	series	parallel	series	parallel	series	parallel
n_{eff}	$n/2$	n	$n/2$	n	$n/2$	n
$L_{\text{out(eff)}}$	L_{out}	L_{out}	$2L_{\text{out}}$	$L_{\text{out}}/2$	L_{out}	L_{out}
$C_{\text{out(eff)}}$	C_{out}	C_{out}	$C_{\text{out}}/2$	$2C_{\text{out}}$	C_{out}	C_{out}
$i_{\text{D(eff)}}$	i_{D}	i_{D}	i_{D}	$2i_{\text{D}}$	i_{D}	i_{D}
$i_{\text{s(eff)}}$	i_{s}	i_{s}	i_{s}	$2i_{\text{s}}$	i_{s}	i_{s}
$i_{\text{SW(eff)}}$	i_{SW}	i_{SW}	i_{SW}	i_{SW}	$i_{\text{SW}}/2$	$i_{\text{SW}}/2$

where k is a tuning factor used to compensate for the voltage drop across the circuit components and also to give a margin for the feedback control dynamics. Practically, k is typically set between $k = 0.85, \ldots, 0.95$.

For the t-PSFB, r-PSFB, and i-PSFB converters, the transformer's turns ratios ($n_{\text{t,r,i}}$) are doubled compared to n since the secondary sides of these converters can operate in modes where the two secondary windings are connected in series. This information is summarized in Table I.

B. Output Filter L_{out} and C_{out}

The output filter L_{out} and C_{out} can be determined by a maximum allowed current and voltage ripple stress across the converter.

1) Output Inductance L_{out}: For the conv-PSFB converter, the peak-to-peak output current ripple $I_{\text{out,ripple}}$ across L_{out} in the continuous conduction mode (CCM) operation can be calculated by

$$I_{\text{out,ripple}} = \frac{V_{\text{in}} D(1-D)}{2n L_{\text{out}} f_{\text{sw}}}. \tag{2}$$

The maximum output inductor ripple ($I_{\text{out,ripple(max)}}$) happens when $D = 0.5$ and $V_{\text{in}} = V_{\text{in(max)}}$. Thus, $L_{\text{out(min)}}$ could be calculated as

$$L_{\text{out}} \geq L_{\text{out(min)}} = \frac{V_{\text{in(max)}}}{8n I_{\text{out,ripple(max)}} f_{\text{sw}}}. \tag{3}$$

For the t-PSFB converter, the minimum output inductance $L_{\text{out(min),t}}$ equals the $L_{\text{out(min)}}$ calculated in (3) in order to satisfy the current ripple requirement in both the full-bridge and center-tapped modes. $I_{\text{out,ripple(max)}}$ for the t-PSFB converter happens when it is in the full-bridge mode, $D = 0.5$, and $V_{\text{in}} = V_{\text{in(max)}}$. When the t-PSFB converter is in the center-tapped mode, the worst case current ripple equals $0.5I_{\text{out,ripple(max)}}$.

For the r-PSFB converter, the minimum output inductance $L_{\text{out(min),r}}$ equals the $L_{\text{out(min)}}$ calculated in (3) in order to satisfy the current ripple requirement in both the series and parallel connection modes. $I_{\text{out,ripple(max)}}$ happens when the r-PSFB is in the parallel connection mode, and in the series connection mode, the worst case output current ripple is only $0.5I_{\text{out,ripple(max)}}$.

For the i-PSFB converter, the minimum output inductance $L_{\text{out(min),i}}$ equals the $L_{\text{out(min)}}$ calculated in (3) in order to satisfy the current ripple requirement in both the series and parallel connection modes. Therefore, the worst case current ripple in the series connection mode is $I_{\text{out,ripple(max)}}$, while, in the parallel connection mode, is $0.5I_{\text{out,ripple(max)}}$.

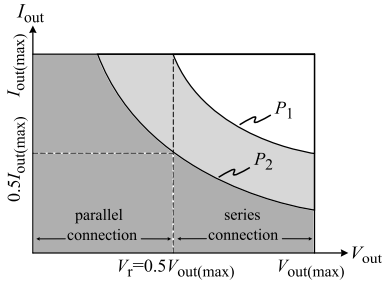

Fig. 2. Operation range of the converters and the power limitation.

2) Output Capacitance C_{out}: For the conv-PSFB converter, the peak-to-peak output voltage ripple $V_{\text{out,ripple}}$ on C_{out} in CCM can be determined by

$$V_{\text{out,ripple}} = \frac{I_{\text{out,ripple}}}{16 f_{\text{sw}} C_{\text{out}}}. \tag{4}$$

The maximum voltage ripple ($V_{\text{out,ripple(max)}}$) happens at $I_{\text{out,ripple(max)}}$. Thus, $C_{\text{out(min)}}$ can be calculated as

$$C_{\text{out}} \geq C_{\text{out(min)}} = \frac{I_{\text{out,ripple(max)}}}{16 f_{\text{sw}} V_{\text{out,ripple(max)}}}. \tag{5}$$

For the t-PSFB converter, the minimum output capacitance value equals $C_{\text{out(min)}}$ calculated in (5). $V_{\text{out,ripple(max)}}$ for the t-PSFB converter happens when the converter is in the full-bridge mode, and the worst voltage ripple that can happen in the center-tapped mode is $0.5V_{\text{out,ripple(max)}}$. For the r-PSFB converter, the minimum output capacitance value equals $C_{\text{out(min)}}$ calculated in (5). $V_{\text{out,ripple(max)}}$ for the r-PSFB converter happens when it is in the series connection mode, and in the parallel connection mode, the worst voltage ripple is $0.5V_{\text{out,ripple(max)}}$. For the i-PSFB converter, the minimum output capacitance value equals $C_{\text{out(min)}}$ calculated in (5).

These information are summarized in Table I.

C. Voltage Stress of C_{out} and Current Stress of L_{out}

The voltage stress of C_{out} is the same for the conv-PSFB, t-PSFB, and i-PSFB converters, as the output capacitor in these converters needs to withstand the full output voltage V_{out}. However, for the r-PSFB converter, each of the output capacitors only needs to block $0.5V_{\text{out}}$.

The current stress of L_{out} depends on how the voltage, current, and power rating of the converter is set. Fig. 2 shows the operation range of the converter. If the power rating is equal to or higher than P_1, which allows the maximum output current value to be reached in the series connection mode, i.e., $P_1 = (1/2)V_{\text{out(max)}}I_{\text{out(max)}}$, then the current stresses on L_{out} is identical for all four converters because, in the series connection mode, all of the inductors of the four converters need to conduct the whole output current i_s plus the current ripple. If the power rating is smaller than P_2, which means that the maximum output current that can be reached during the series connection mode is $0.5I_{\text{out(max)}}$ (i.e., $P_2 = (1/2)\ V_{\text{out(max)}}(1/2)I_{\text{out(max)}}$), then the current stresses on the inductors of r-PSFB converter will be half of the other PSFB converter or even less. This information is summarized in Table II.

TABLE II
SUMMARY OF THE COMPONENTS' REQUIREMENTS FOR THE FOUR STUDIED PSFB CONVERTERS

	items	conv-PSFB	t-PSFB	r-PSFB	i-PSFB
transformer	turns ratio rated to n	1	2	2	2
output filter	L_{out} count	1	1	2×1	1
	C_{out} count	1	1	2×1	1
	V_{stress} of C_{out} rated to V_{out}	1	1	0.5	1
	I_{stress} of L_{out} rated to i_s	1	1	0.5 - 1	1
RCD	V_{stress} of D, C_{RCD} rated to V_{cp}	1	1	0.5	1
D_{rec}	V_{stress} of D_{rec} rated to V_{sec}	1	1	0.5	1

D. Voltage Stress of the RCD Snubber Circuitry

Due to the resonance between L_σ and the parasitic capacitance from the transformer and rectifier diodes, a voltage ringing will happen on the secondary side diodes, with a peak voltage value that could reach twice the nominal value of the secondary winding voltage [25] and [12]. This can be critical for the safe operation of the rectifier diodes, and it is particularly critical for the voltage class (V_{class}) requirement of the fast-recovery diodes. Therefore, the RCD voltage clamp snubber circuitry is designed to limit the blocking voltage ringing to a reasonable value, V_{cp}, so that a safe operation for the rectifier diodes is ensured, e.g., $V_{\text{cp}} \leq 0.85 V_{\text{class}}$.

The voltage stress of D_{RCD} and C_{RCD} equals to V_{cp} for the conv-PSFB converter, which could reach $2V_{\text{sec}}$ if no clamp snubber circuit is used. For the t-PSFB and i-PSFB converters, the voltage stress of D_{RCD} and C_{RCD} equals to V_{cp} as well since its series connection mode is equivalent to the conv-PSFB converter. For the r-PSFB converter, the RCD circuitry only needs to block half of the voltage compared to the conv-PSFB converter. However, the tradeoff is that it has two sets of RCD circuitry. This information is summarized in Table II. The sizing of the resistance value and the power loss calculation of the RCD snubber follows the methodology explained in [12].

E. Voltage and Current Stresses of the Rectifier Diodes and Transistors

The voltage class of the rectifier diode of the PSFB converter needs to be paired with V_{cp} of the RCD circuitry. Therefore, for the r-PSFB converter, the voltage class of the rectifier diode is halved compared to the other analyzed PSFB converters. This information is summarized in Table II.

After designing the transformer turns ratio and output filter, as introduced in Sections III-A and III-B, the steady-state current stresses of the rectifier diodes and transistors of the t,r,i-PSFB and the conv-PSFB converter can be calculated using the steady-state analytical model of the PSFB converter introduced in [12] together with the equivalent parameters of the t,r,i-PSFB converters shown in Table I. Considering an 11-kW power rating, 30-A maximum output current, 640–840-V input voltage, and 250–1000-V output voltage range, the current stresses are summarized in Table III. As it can be seen from Table III, the worst case $I_{\text{p/sw,rms}}$ of the t-PSFB and r-PSFB is lower than that of the conv-PSFB converter, and those of the i-PSFB converter is approximately half of those of the t-PSFB and r-PSFB. This is because the reconfiguration ability of the t/r/i-PSFB converter can reduce the current stresses to the minimum half of those of the conv-PSFB converter if the power rating is chosen to be P_2 shown in Fig. 2. However, since the chosen power rating of the benchmark study is 11 kW, it lays between P_2 and P_1. Thus, the current stress of the t/r/i-PSFB converter is lower than the conv-PSFB but not as low as half, as in the case shown in Table III.

TABLE III
WORST CASE CURRENT STRESSES OF THE 11-KW, 30-A CONVERTERS

	conv-PSFB	t-PSFB	r-PSFB	i-PSFB
$I_{\text{p,rms}}$ [A]	48.9	36.1	34.3	18
$I_{\text{sw,rms}}$ [A]	34.6	25.5	24.3	12.8
$I_{\text{D,rms}}$ [A]	21.1	21.2	14.8	21.2
$I_{\text{D,avg}}$ [A]	15	15	10.5	15

IV. KEY COMPONENTS' DATA COLLECTION AND PROCESSING

In order to better evaluate the performance of the PSFB converters with different circuit component requirements, data of the necessary components are obtained from the website of the well-known redistributors, and they are further processed using a python script to obtain the correlation among the parameters regarding efficiency performance, PD, and cost, as shown in Fig. 3. Using this approach, it is no longer necessary to extract the essential data from the datasheets of components, which is highly time-consuming. Since this method is purely based on data analysis and interpretation, physical models for cost estimation are not required. Other designers can incorporate the method to process their own components' database, or they can directly use the numerical coefficients presented in this article for a primary estimation in their design stage.

The unit price per piece from the redistributors' website is used as the cost data of the components. This data is valuable for two reasons. First, it is the most accessible price data. Mass production price information is usually only available from company quotes or specific supply chains. Thus, it is hard to access especially for academic researchers and engineers in small-scale companies. Each company will also have different mass production prices based on the size of the enterprise and its negotiation power. However, for prototyping or small-scale production, the price information provided online by these redistributors is extremely valuable for the primary estimation of the cost. Second, the normalized price calculated based on the price per piece is similar to the one calculated using the price for large purchase quantities. To demonstrate this idea, the price information of 12 SiC MOSFETs in the package of TO-247 from three different manufacturers, GeneSiC, Infineon, and Wolfspeed is collected from the website of the redistributor Digikey. The part number and the price information are shown in Table IV, where price_1 stands for the unit price if the purchase quantity is 1, price_{1000}

TABLE IV
PRICE OF SIC MOSFETS FOR DIFFERENT PURCHASE QUANTITIES COLLECTED ON JANUARY 3, 2023

part_num	mfr	$R_{ds(on)}$[mΩ]	price$_1$[€]	price$_{10}$[€]	price$_{100}$[€]	price$_{500}$[€]	price$_{1000}$[€]
G3R350MT12D	GeneSiC	420.0	4.80	4.261	3.7815	3.47872	3.35618
G3R160MT12D	GeneSiC	192.0	6.61	5.921	5.3067	4.91578	4.75678
G3R75MT12D	GeneSiC	90.0	10.64	9.580	8.6284	8.01880	7.77066
G3R40MT12D	GeneSiC	48.0	17.64	16.102	14.7000	13.79436	NaN
IMW120R220M1H	Infineon	286.0	9.98	9.019	7.4672	6.50228	5.66326
IMW120R090M1H	Infineon	117.0	12.42	11.414	9.6395	8.57498	7.86534
IMZ120R060M1H	Infineon	78.0	17.37	15.969	13.4866	11.99730	NaN
IMW120R040M1H	Infineon	54.4	22.50	20.682	17.4668	15.53798	NaN
C3M0160120D	Wolfspeed	208.0	9.65	8.709	7.2106	6.27890	5.46872
C3M0075120D	Wolfspeed	90.0	17.09	15.711	13.2688	11.80356	NaN
C3M0032120D	Wolfspeed	43.0	31.42	28.979	24.7468	NaN	NaN
C3M0021120D	Wolfspeed	28.8	35.62	33.229	28.8516	NaN	NaN

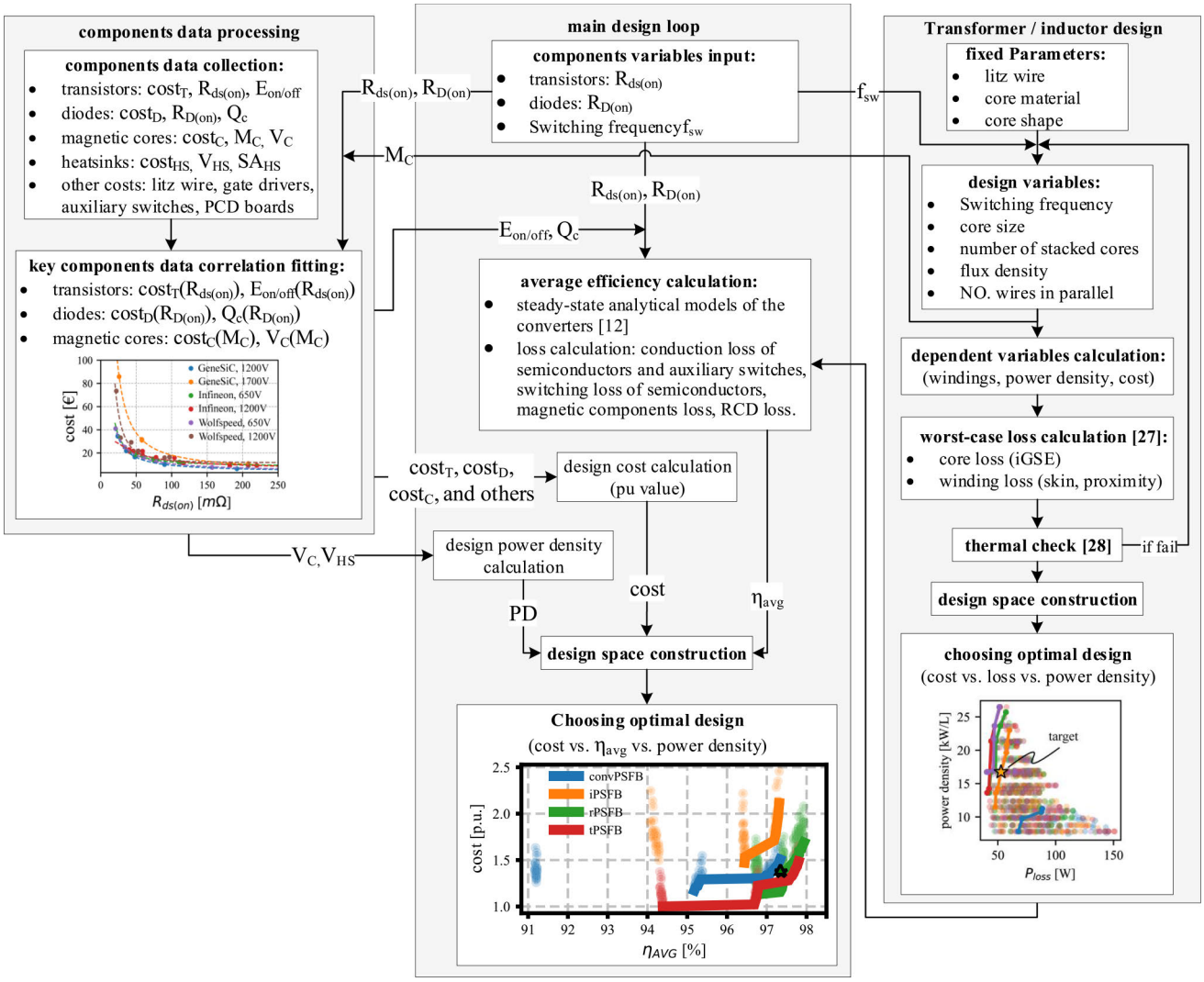

Fig. 3. Multiobjective design process of the converters.

means the unit price if buying 1000 pieces, and so on. Plotting the unit price of different purchase quantities in Fig. 4, one can see that the unit price for larger purchase quantities drops considerably. However, instead of the exact price, this article emphasis predicting the normalized cost of design, i.e., how much cheaper or more expensive is one certain converter design compared to the others. By calculating the p.u. value of the prices for different purchase quantities, Fig. 5 shows that the normalized cost calculated using different purchase quantities remains similar. Thus, the easy-to-access unit price information from the well-known redistributors enables the estimation of the relative price of the converter designs, which is insightful for academic researchers and small-scale company engineers to make design decisions. Moreover, this price

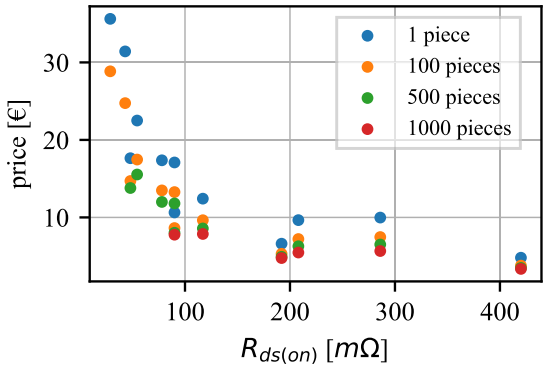

Fig. 4. Unit price of the SiC MOSFETs in Euros. Data were collected on January 3, 2023.

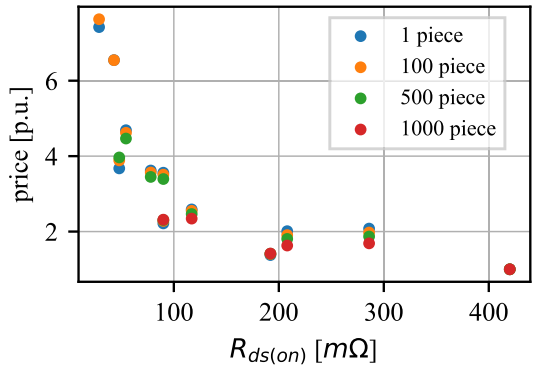

Fig. 5. Unit price of the SiC MOSFETs in p.u. values. Data were collected on January 3, 2023.

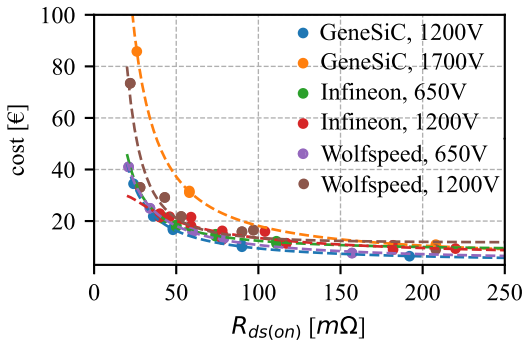

Fig. 6. SiC MOSFET price and $R_{ds(on)}$ trend, depending on the device voltage ratings. The plotted dots are the data of a commercially available device acquired from the Digikey website on February 2, 2022, containing SiC MOSFET from "GeneSiC," "Infineon," and "Wolfspeed." The device package is limited to TO-247. The dashed lines are the obtained curve-fitting correlations, whose method and coefficients are shown in Table V.

information can still be used with a scaling factor by the companies to predict the mass production price.

A. Active Semiconductors

For SiC MOSFETs, the ON-state (static) losses can be determined by their ON-resistance R_{dson}, and the switching (or dynamic) losses can be modeled by the accumulative energy dissipated during the ON/OFF switching transition ($E_{on/off}$). Their cost data can be collected directly on the website of their redistributors, e.g., the Digikey website. In this work, only semiconductor devices employing TO-247 packaging are considered in the analysis. Several SiC MOSFET manufacturers are evaluated, and a statistic curve-fitting method is used to model the important parameters for the calculation of the selected design performance metrics.

TABLE V

CURVE-FITTING METHOD AND COEFFICIENTS FOR THE RELATION BETWEEN PRICE AND R_{DSON} OF THE SIC MOSFETS DEPENDING ON THE MANUFACTURERS AND VOLTAGE RATINGS. DATA ONLY INCLUDE THOSE WITH $R_{DS(ON)} < 300$ mΩ

fitting method	$\text{cost}_T = a \cdot (1/R_{ds(on)})^2 + b \cdot (1/R_{ds(on)}) + c$					
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	650	1200
a	7.91e+03	-8.33e+03	4.71e+03	2.53e+04	2.15e+03	2.99e+04
b	3.66e+02	9.08e+02	5.44e+02	1.15e+03	6.78e+02	-1.34e+02
c	7.89e+00	5.21e+00	3.47e+00	4.10e+00	3.72e+00	1.19e+01

TABLE VI

CURVE-FITTING METHOD AND COEFFICIENTS FOR THE RELATION BETWEEN $E_{ON/OFF}$ AND R_{DSON} OF THE 1200-V SIC MOSFETS. DATA INCLUDES THOSE FROM "WOLFSPEED"

fitting method	$E_{on/off} = a \cdot R_{dson} + b$	
parameter	E_{on}	E_{off}
a	-1.66e-02	-7.11e-03
b	2.23e+00	6.67e-01

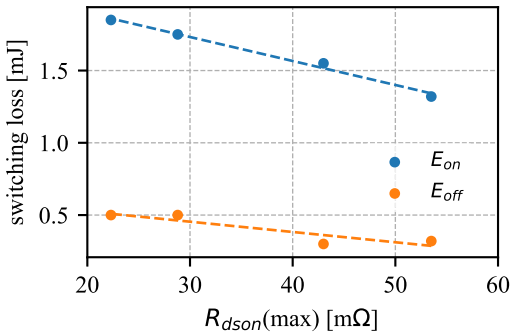

Fig. 7. SiC MOSFET $E_{on/off}$ and $R_{ds(on)}$ trend. The dots are the data acquired from the datasheets of 1200-V SiC MOSFET from "Wolfspeed," and the condition is at 800 V, 30 A, and 25 °C of junction temperature, 5-Ω gate resistance, and 15-V/−5-V gate driving voltage. The package is limited to TO-247. The dashed lines are the curve-fitting correlations, whose method and coefficients are shown in Table VI.

Fig. 6 shows the correlation between R_{dson} and cost of the transistors with three voltage class devices, and Table V shows the curve-fitting numerical parameters of the plotted logarithmic equation. It can be seen that, with the same R_{dson}, the SiC MOSFETs with higher voltage ratings generally cost more. At low R_{dson}, the cost difference between the 1700-, 1200-, and 650-V classes is more significant. This may imply that circuits designed for a given target efficiency that employ 1700-V semiconductors could have higher costs than the ones employing 1200- or 650-V devices, but one should be careful because the total cost of a power electronic converter is highly dependent on the circuit topology selection and the complexity of the circuit. It is interesting to note that there are fewer options for the 1700-V semiconductor market compared to the 650- and 1200-V classes. This indicates that topologies using 1700-V SiC transistors will be more prone to supply chain problems.

The correlation between switching losses $E_{on/off}$ and R_{dson} of several commercially available 1200-V SiC MOSFETs from Wolfspeed is given in Fig. 7. Herein, the data consider the device datasheet information: $E_{on/off}$ at 800 V, 30 A, 25 °C of junction temperature, 5-Ω external gate resistance, and a 15-/−5-V gate driving voltage. Table VI shows the numerical coefficients of the curve-fitting first-order linear equation.

TABLE VII

CURVE-FITTING METHOD AND COEFFICIENTS FOR THE RELATION BETWEEN PRICE AND R_{DON} OF THE SIC DIODES DEPENDING ON THE MANUFACTURERS AND VOLTAGE RATINGS

fitting method	$\mathrm{cost_D} = a \cdot (1/R_{\mathrm{D(on)}})^2 + b \cdot (1/R_{\mathrm{D(on)}}) + c$				
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	1200
a	-4.34e+02	-2.72e+02	-4.98e+03	1.11e+02	-6.17e+03
b	2.47e+02	2.97e+02	7.48e+02	5.29e+02	6.78e+02
c	3.23e+00	2.55e+00	-3.96e+00	2.30e+00	5.61e+00

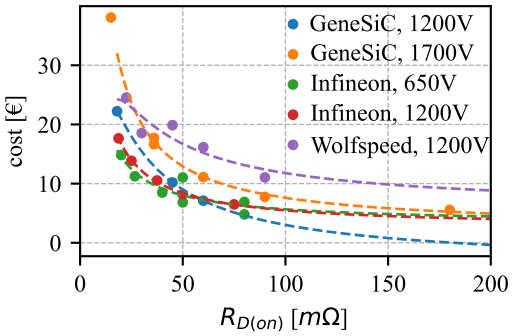

Fig. 8. SiC rectifier diode price and R_{Don} trend. The dots are the data acquired from Digikey on February 2, 2022, containing SiC diodes from "GeneSiC," "Infineon" IDW series, and "Wolfspeed." The package is limited to TO-247. The dashed lines are the curve-fitting trends of the SiC rectifier diodes, whose method and coefficients are shown in Table VII.

TABLE VIII

CURVE-FITTING METHOD AND COEFFICIENTS FOR THE RELATION BETWEEN Q_c AND R_{DON} OF THE SIC DIODES DEPENDING ON THE MANUFACTURERS AND VOLTAGE RATINGS

fitting method	$Q_{\mathrm{c}} = a \cdot (1/R_{\mathrm{D(on)}})^2 + b \cdot (1/R_{\mathrm{D(on)}}) + c$				
Mfr	Infineon	Infineon	GeneSiC	GeneSiC	Wolfspeed
V_{rating} [V]	650	1200	1200	1700	1200
a	-1.19e+03	-1.52e+03	-1.54e+03	-2.38e+04	-6.40e+04
b	1.14e+03	3.72e+03	4.92e+03	9.75e+03	7.17e+03
c	8.33e-01	7.90e+00	-1.57e+00	-1.95e+01	-2.27e+01

It is worth mentioning that the data collected from the datasheet are under the specific conditions of 800 V and 30 A. Therefore, $E_{\mathrm{on/off}}$ for other operating points can be scaled proportionally based on the actual blocking voltage and switching current, as shown in the following equation:

$$E_{\mathrm{on/off}}(t) = \frac{V_{\mathrm{block}}(t)}{800\ \mathrm{V}} \cdot \frac{I_{\mathrm{sw}}(t)}{30\ \mathrm{A}} E_{\mathrm{on/off(fit)}}. \tag{6}$$

B. SiC Rectifier Diodes

Discrete TO-247 SiC diodes from various manufacturers from 650 to 1700 V are compared using the information provided on their datasheets. The conduction loss of the diodes is typically calculated by (7), where R_{Don} and V_{D} are the ON-resistance and forward voltage drop. R_{Don} is taken from the ON-state I–V curve of the device by the difference in voltage drop for two reference current values, e.g., one at half-rated current and another at full-rated current. V_{D} is the voltage drop value taken when the device conducts only a tiny fraction of the rated current

$$P_{\mathrm{D}} = I_{\mathrm{D,rms}}^2 \cdot R_{\mathrm{Don}} + I_{\mathrm{D,avg}} \cdot V_{\mathrm{D}}. \tag{7}$$

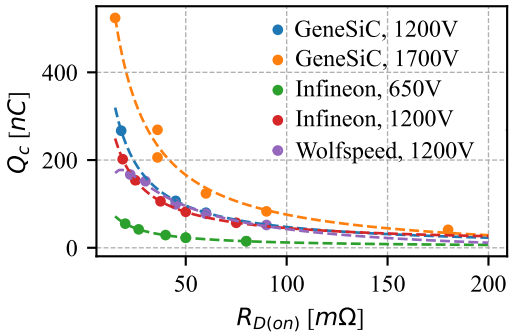

Fig. 9. SiC rectifier diode Q_{c} and R_{Don} trend. The dots contain SiC diodes from "GeneSiC," "Infineon" IDW series, and "Wolfspeed." The package is limited to TO-247. The dashed lines are the curve-fitting trends of the SiC rectifier diodes, whose method and coefficients are shown in Table VIII.

TABLE IX

CURVE-FITTING METHOD AND COEFFICIENTS OF THE MAGNETIC CORES

fitting method	$\mathrm{cost_C} = a \cdot \mathrm{M_C} + b$			
material	Metglas Alloy	N27	N87	N95
a	22.85	47.31	48.29	107.97
b	12.39	-1.76	-0.73	-8.83

Fig. 8 shows the correlation between price and R_{Don} of the rectifier diodes, grouped by the device voltage class. Note that, since the SiC diodes benchmarked are of the same technology, their equivalent constant voltage drops V_{D} are similar and closely independent of the chip die area (or rated current of the device). Therefore, the R_{Don} parameter has a more logical relationship with the chip die size (or current ratings) and, thus, relates better with the device cost.

The switching loss of the diodes is typically calculated by (8), where Q_{c} is the capacitive charge of the diodes. Fig. 9 shows the correlation between R_{Don} and Q_{c}

$$P_{\mathrm{D(sw)}} = 0.5 \cdot Q_{\mathrm{c}} \cdot V_{\mathrm{D}} \cdot f_{\mathrm{sw}}. \tag{8}$$

C. Magnetic Core Material and Litz Wire

Magnetic components account for a significant part of the cost, loss, and PD of a power electronic converter. The magnetic core loss is generally calculated by iGSE for nonsinusoidal excitation, which requires the Steinmetz coefficients measured for sinusoidal excitation that need to be curve-fit based on the datasheet figures. The cost of the magnetic cores for various core shapes can be obtained through suppliers' websites, such as Digikey, and the trend of the core cost and core mass is shown in Fig. 10. It can be seen that the core cost has a linear correlation with the amount of core material used. Table IX shows the curve-fitting coefficients of the magnetic cores.

For the Litz wire used in the magnetic components, €5.38 per kilogram is used to estimate the cost of it based on the amount of copper used. The weight of the copper can be calculated based on the number of turns and the mean-length-per-turn of the design.

D. Heatsink

The heatsink is necessary for the thermal management of the semiconductors used in the studied PSFB converters.

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TABLE X

DETAILS OF THE HEATSINKS CONSIDERED FOR THE FOUR CONVERTERS. THE PRICE INFORMATION IS COLLECTED FROM FARNELL ON OCTOBER 24, 2022

topology	heatsink	SA[m^2]	volume[L]	cost[€]
conv/t-PSFB	890SP-01000-A-100	0.010	0.325	50.87
r-PSFB	890SP-01500-A-100	0.015	0.488	67.87
i-PSFB	890SP-02000-A-100	0.020	0.650	79.70

Therefore, its size will be mostly defined by the critical point in which the system can be placed into operation where the semiconductor losses are maximum. Independently on the performance of the heatsink, its minimal size will be defined by the sum of surface area required to accommodate each used TO-247 packaged device. The thermal resistance of the heatsink depends on the material used, available surface area, airflow, and equivalent pressure drop. For simplicity of comparison, only the aluminum heatsinks that are rectangular in shape with the same fin height and arrangement from the same manufacturer HS Marston are considered. Table X shows the details of the chosen heatsinks. Due to the excellent performance of the selected heatsinks, the needed surface area for placing the semiconductors of each studied circuit topology defines their required size.

E. Gate Driver, Relay, and PCB

The high-side gate driver ISO5852 is considered in the benchmark study. The price per unit is €7. For the conv/t/r-PSFB converter, four gate drivers are required. For the i-PSFB converter, eight are required. For the digital controller, the Texas Instruments TMS320F28379D is considered. The price is €27. The relays used in the r/t-PSFB converter are chosen to be the T9GV1L14-5, which is a 30-A power relay with a unit price of €7.4 and a conduction resistance of about 10 mΩ. These prices are based on the data from the Mouser/Farnell website acquired on October 24, 2022.

The price of the PCB board depends mainly on the number of conductive layers and the size of the board. Assuming that 1 m^2 of the standard four-layer 1-oz copper PCB is used, and the size of the PCB equals the size of the heatsink, the prices of the single PCB boards for the four converters are estimated to be €8.5 for the conv/t-PSFB, €13.1 for the r-PSFB, and €17.4 for the i-PSFB. This price was obtained from the manufacturer Eurocircuits on October 24, 2022.

V. MULTIOBJECTIVE DESIGN OF THE CONVERTERS

To benchmark the four studied PSFB topologies in the EV battery charging application, a multiobjective design process is performed in all circuits while considering an 11-kW power rating, 30-A maximum output current, 640–840-V input voltage, and 250–1000-V output voltage range. For the EV charging application where the converter operates in a wide output voltage range and mostly in full-power/current, the averaged full-power/current efficiency η_{AVG} is used as the indicator of

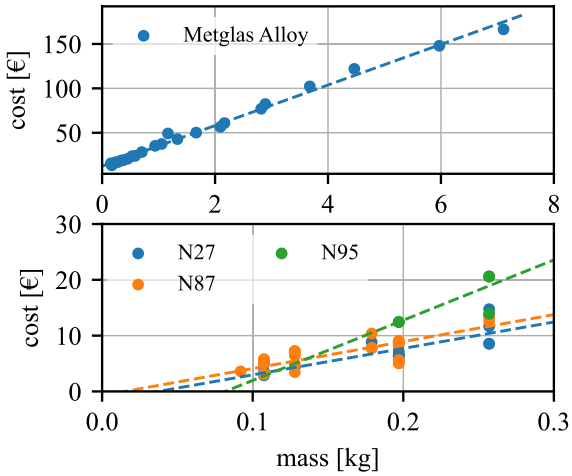


Fig. 10. Magnetic core trend. The dots are the data acquired from Digikey on February 2, 2022, containing E-shaped cores for the ferrite material N27, N87, N95, and U-shaped AMCC cores for the Metglas Alloy material.

the system efficiency performance instead of the efficiency value for a single operational point. η_{AVG} is the average value of the steady-state efficiencies of a certain number of sampling operational points. These sampling operational points start from the minimum output voltage and maximum output current to the maximum output voltage and maximum power, with a constant output voltage increment between two neighboring points. In this article, eight points are considered for the calculation. The first point is when $V_{out} = 300$ V and $I_{out} = 30$ A; the second is $V_{out} = 400$ V and $P = 11$ kW; the third is $V_{out} = 500$ V, $P = 11$ kW, and so on; and the final point is when $V_{out} = 1000$ V and $P = 11$ kW. The objectives of interest are the average efficiency performance, PD of the magnetic components and heatsinks, and normalized cost. Fig. 3 shows the flowchart of the multiobjective design process.

The first step of the multiobjective design process is to design the magnetic components of the converters. Since the switching frequency f_{sw} of the converter has a significant impact on the design of the magnetic components, the magnetic components are designed for f_{sw} from 15 to 105 kHz, and assume the worst case scenario in terms of losses. The design spaces of the magnetic components will be formed for each of the converters, with the loss, PD, and cost being the figures of merit. Then, based on the design spaces, some advantageous transformer and inductor designs will be selected for further converter design.

The second step is to sweep through a range of $R_{ds(on)}$ and $R_{D(on)}$. Using the components correlation derived and the analytical models of the converters, the total cost and the average efficiency of the converter designs can be calculated. The calculated total costs can be further processed to obtain the normalized costs by taking the minimum value of the cost as 1. By using the normalized costs, the designs with the cost advantage can be identified, while the error of cost estimation brought by the changing market price can be reduced at the same time. As a result, the design spaces for the converters

can be formed, and the advantageous converter topology and component designs can be chosen.

A. Magnetic Components Designs

The design of the magnetic components follows the process illustrated in Fig. 3. In order to avoid an overly large number of solutions, the Litz wire considered in the design is set to be AWG 41 and 600 strands; the core material for the transformer is the ferrite N87 and for the inductor is the Metglas Amorphous Cut Core; and the core shape for the transformer is the EE cores and for the inductor are the UU cores. Five design variables are considered for finding the optimal design; they are the switching frequency, the core size, the number of stacked cores, flux density, and the number of Litz wires that can be put in parallel. The number of stacked cores can change from 1 to 8 for transformer design and 1 to 5 for inductor design. The allowed flux density is from 10% to 80% of B_{sat} of the core material. The number of Litz wires that can be paralleled can be 1 or 2 for the ease of winding assembly. The worst case scenarios for the designs of the magnetic components happen when the winding currents are the maximum, which results in the most losses. For the transformer design, the worst case scenario for the conv-PSFB converter is when $V_{\text{in}} = 840$ V, $I_{\text{out}} = 30$ A, and $V_{\text{out}} = 366$ V and for the t/r/i-PSFB converter is when $V_{\text{in}} = 840$ V, $I_{\text{out}} = 22$ A, and $V_{\text{out}} = 500$ V. For the inductor design, the worst case scenario for the r-PSFB converter is when $V_{\text{in}} = 840$ V, $I_{\text{out}} = 22$ A, and $V_{\text{out}} = 366$ V and for the conv/t/i-PSFB converter is when $V_{\text{in}} = 840$ V, $I_{\text{out}} = 30$ A, and $V_{\text{out}} = 366$ V. The loss calculation is conducted using the method from [27]. Combining the total losses P_{mag} (W) and surface area A_{mag} (m^2) of the magnetic components, the temperature rise ΔT is estimated based on the following equation [28]:

$$\Delta T = \left(\frac{P_{\text{mag}}}{10 \cdot A_{\text{mag}}} \right)^{0.833}. \tag{9}$$

This temperature rise estimation equation is obtained by lumping the winding losses together with the core losses, and assume that the thermal energy is dissipated uniformly throughout the surface area of the core and winding assembly at all ambient temperatures. This assumption is effective because the majority of the transformer's surface area is ferrite core area rather than winding area, and the thermal conductivity of ferrite (around 40 mW/cm/°C) is poor at any temperature. Since the transformer uses several pairs of ferrite cores stacked together, the magnetic cores are carefully fixed together so that the airgap is uniformed in the whole transformer. In this way, the magnetic flux and, thus, the core loss can be more evenly distributed among the cores, which helps avoid creating a hotspot. Moreover, the windings are tightly winded on the bobbin, and the gaps among the wires are kept as uniformly as possible so that the winding losses are also distributed evenly in the winding area.

Fig. 11 shows the worst case transformer loss P_{loss} and the PD values of the transformer designs for all four topologies,

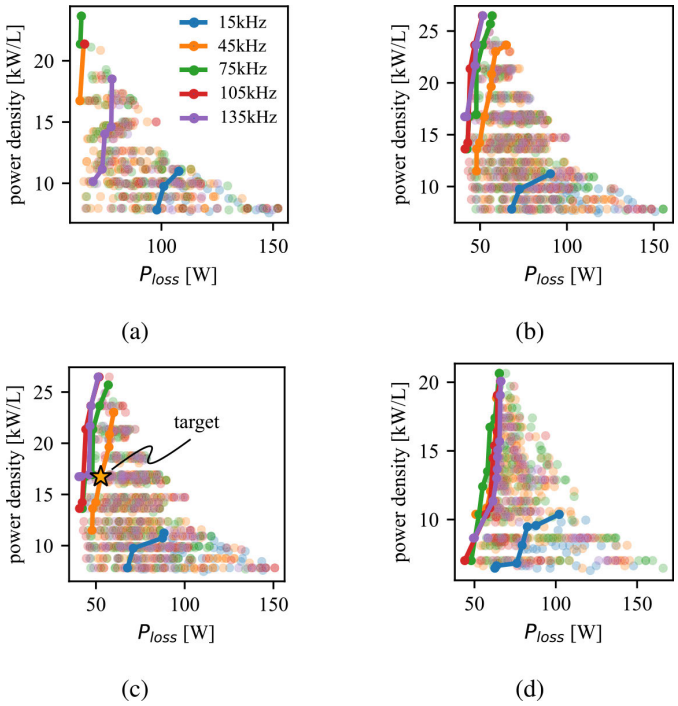


Fig. 11. Transformer designs for the four PSFB topologies at f_{sw} = 15, 45, 75, 105, and 135 kHz. The design constrains are target transformer leakage inductance $L_\sigma = 10$ μH (referred to the primary side), N87 as core material, and the winding layer arrangement is limited to first primary and then secondary 1 and secondary 2 side-by-side, calculated temperature rising limited to 80 °C. (a) conv-PSFB. (b) t-PSFB. (c) r-PSFB. (d) i-PSFB.

with the switching frequency changing from 15 to 135 kHz. It can be seen that, by increasing f_{sw} from 15 to 75 kHz, P_{loss} decreases and PD increases for all of the topologies. However, there is no apparent improvement on P_{loss} and PD anymore when f_{sw} further increases above 75 kHz.

The underlining reason is that, by increasing f_{sw}, less number of turns is needed for the transformer to operate with the desired value of magnetic flux density B. As a result, a smaller winding area, which naturally means a smaller core shape, is needed to make a transformer with a higher f_{sw}. The reduced winding length and core size further contribute to the reduction of core loss. However, there is a limit to how small the transformer can become with the increase of f_{sw}, which is mostly regulated by the thermal management performance of the component. One can argue that a smaller flux density B should be used for the transformer with higher f_{sw} so that the loss-per-volume of the core does not result in overheating. Unfortunately, a smaller flux density can only be achieved with an increased number of turns, which, again, calls for a larger winding area, as well as a larger core size. In summary, there is an optimal f_{sw}, with which the transformer design yields the advantageous P_{loss} and PD without having an overheating problem. From Fig. 11, it is clear that the optimal f_{sw} for the transformer designs is around 75 kHz.

Based on the results shown in Fig. 11, three advantageous transformer designs that have the highest PD and lowest power losses at f_{sw} of 15, 45, and 75 kHz are collected for each one of the PSFB topologies. Table XI shows the chosen

TABLE XI
DETAILED INFORMATION OF THE TRANSFORMER DESIGNS THAT ARE CHOSEN FOR THE MULTIOBJECTIVE DESIGN PROCESS. P_{LOSS}, PD, AND COST ARE CALCULATED FOR ALL THE TRANSFORMERS

topology	f_{sw} [kHz]	P_{loss} [W]	PD [kW/L]	cost [€]	ΔT [°C]	shape [E core]	N_{core}	$N_{\mathrm{w,prim}}$	$N_{\mathrm{w,sec}}$	N_{prim}	N_{sec}	B_{op} [T]
convPSFB	15.0	107.8	11.0	123.4	78.4	E 70/33/32	5	2	2	12	19	0.248
convPSFB	45.0	65.2	21.4	66.3	73.0	E 56/24/19	8	2	2	5	8	0.248
convPSFB	75.0	64.1	23.6	58.2	78.8	E 56/24/19	7	2	2	5	9	0.155
tPSFB	15.0	90.5	11.2	122.5	69.2	E 70/33/32	5	2	1	12	10	0.248
tPSFB	45.0	56.4	19.6	56.4	72.5	E 65/32/27	3	2	2	10	8	0.217
tPSFB	75.0	52.6	21.7	49.2	77.7	E 70/33/32	2	2	2	8	7	0.186
rPSFB	15.0	88.3	11.2	122.5	67.8	E 70/33/32	5	2	1	12	10	0.248
rPSFB	45.0	57.4	19.6	56.4	73.5	E 65/32/27	3	2	2	10	8	0.217
rPSFB	75.0	53.2	21.7	49.2	78.6	E 70/33/32	2	2	2	8	7	0.186
iPSFB	15.0	102.1	10.4	99.1	72.9	E 70/33/32	2	1	1	31	25	0.248
iPSFB	45.0	71.7	18.7	40.9	76.3	E 55/28/21	2	1	2	22	18	0.217
iPSFB	75.0	65.3	20.6	50.1	74.8	E 56/24/19	3	1	2	10	9	0.186

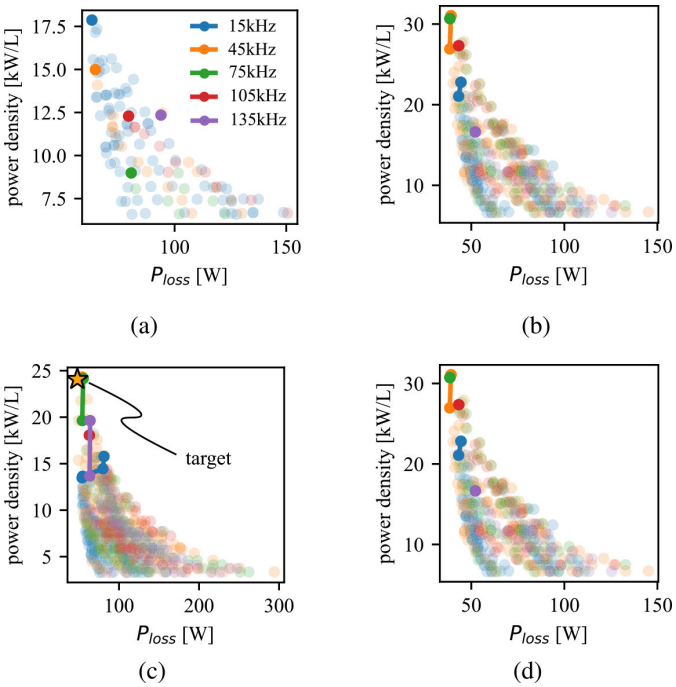


Fig. 12. Inductor designs for the four PSFB topologies at f_{sw} = 15, 45, 75, 105, and 135 kHz. The design constrains are Metglas as core material and maximum temperature rising lower than 80 °C. Note that, here, f_{sw} is defined as the MOSFET switching frequency; therefore, in any of the studied PSFB, the equivalent frequency seen by the inductor will be twice f_{sw}. (a) conv-PSFB. (b) t-PSFB. (c) r-PSFB. (d) i-PSFB.

transformer designs. It can be seen from Fig. 11 and Table XI that the transformer designs of the t-PSFB and r-PSFB are able to have lower power losses compared to the conv-PSFB and i-PSFB. This is because the winding current stresses of these two topologies are less, as can be seen from Table III. Despite having two transformers, the total cost of the transformers of the i-PSFB converter can be even cheaper than the other three PSFB converters in 15 and 45 kHz. However, due to the added winding volume of the two transformers, the total PD of the transformers is slightly lower than the other three options.

Fig. 12 shows the worst case loss and PD values of the inductor designs for all four PSFB topologies, with f_{sw} in the range from 15 to 135 kHz. Note that, here, f_{sw} is defined as the MOSFET switching frequency; therefore, in any of the studied PSFB, the equivalent frequency seen by the inductor will be twice f_{sw}. It can be seen that, similar to the transformer design, the inductor designs have their optimal f_{sw} for achieving the optimal loss and PD values. The conv-PSFB converter has the best inductor design at f_{sw} = 15 kHz, and with higher f_{sw}, the loss increases and PD decreases. For the t/r/i-PSFB converters, the optimal inductor designs occur around f_{sw} = 45 kHz. This is because the inductor of the conv-PSFB converter suffers from higher dB/dt stress compared to the other reconfigurable structure PSFB converters despite that the current stresses on the inductors for the conv/t/i-PSFB are the same. This results in an increased core loss on the inductor according to the iGSE equation [27].

Table XII shows the selected inductor designs that have the optimal loss and PD values for f_{sw} of 15, 45, and 75 kHz for all topologies. It can be seen based on Fig. 12 and Table XII that the inductor designs of the conv-PSFB converter perform worse in terms of power losses due to the high dB/dt stress explained before. In comparison, the t-PSFB and i-PSFB have similar inductor designs that are the most advantageous in terms of power losses, PD, and cost. For the r-PSFB converter, the total PD of the two inductors is less, and the total power losses are higher than that of the t-PSFB and i-PSFB. This is reasonable since the chosen power rating of 11 kW and the output current limitation of 30 A makes the r-PSFB design right in between P_1 and P_2 in Fig. 2. This makes the worst-case current stress on each of the inductors of the r-PSFB converter to be less than that of the conv/t/i-PSFB converter but also more than half of it. Therefore, the two inductors of the r-PSFB together have higher losses in the worst case and lower PD.

B. Multiobjective Design Results

With the magnetic components at different f_{sw}'s designed, the performance of these converters in different f_{sw}'s can be benchmarked. A range of $R_{\mathrm{ds(on)}}$ and $R_{\mathrm{D(on)}}$ is swept through. Based on the cost and performance correlations of the key components and information about miscellaneous parts obtained in Section IV, the relative cost and losses of every design can be estimated for the different choice of components.

TABLE XII
DETAILED INFORMATION OF THE INDUCTOR DESIGNS THAT ARE CHOSEN FOR THE MULTIOBJECTIVE DESIGN PROCESS. P_{LOSS}, PD, AND COST ARE CALCULATED FOR ALL THE INDUCTORS

topology	f_{sw} [kHz]	P_{loss} [W]	PD [kW/L]	cost [€]	ΔT [°C]	shape [U core]	N_{core}	$N_{\text{w,prim}}$	N_{prim}	B_{op} [T]
convPSFB	15.0	63.0	17.9	86.6	79.7	U AMCC-25	4	2	42	0.936
convPSFB	45.0	64.5	15.0	99.5	67.5	U AMCC-40	4	2	21	0.468
convPSFB	75.0	80.6	9.0	136.5	60.0	U AMCC-80	4	2	14	0.312
tPSFB	15.0	44.4	22.8	65.0	70.8	U AMCC-25	3	2	42	1.248
tPSFB	45.0	39.1	31.0	43.1	79.1	U AMCC-25	2	2	29	0.936
tPSFB	75.0	38.5	30.7	43.0	78.1	U AMCC-25	2	2	27	0.624
rPSFB	15.0	53.8	13.5	87.7	54.4	U AMCC-25	2	2	49	1.248
rPSFB	45.0	48.0	24.1	44.1	70.8	U AMCC-25	1	2	45	0.936
rPSFB	75.0	55.2	24.2	43.6	79.6	U AMCC-25	1	2	34	0.780
iPSFB	15.0	44.4	22.8	65.0	70.8	U AMCC-25	3	2	42	1.248
iPSFB	45.0	39.1	31.1	43.1	79.1	U AMCC-25	2	2	29	0.936
iPSFB	75.0	38.5	30.7	43.0	78.1	U AMCC-25	2	2	27	0.624

TABLE XIII
DETAILED INFORMATION OF THE EFFICIENCY AND COST ADVANTAGEOUS DESIGNS BASED ON FIG. 13. PD_{T} IS THE POWER DENSITY OF THE TRANSFORMERS, PD_{L} IS THE POWER DENSITY OF THE INDUCTORS, AND PD IS THE POWER DENSITY OF THE MAGNETIC COMPONENTS TOGETHER WITH THE HEATSINKS

topology	f_{sw}[kHz]	η_{AVG}[%]	cost[pu]	transistor[mΩ]	rec diode[mΩ]	PD_{T}[kW/L]	PD_{L}	PD
conv-PSFB	15	97.33	1.51	Infineon,30	GeneSiC, 30	11.0	17.9	5.67
conv-PSFB	45	95.38	1.38	Infineon, 30	GeneSiC, 30	21.4	15.0	7.00
t-PSFB	15	97.80	1.48	Infineon, 30	GeneSiC, 30	11.2	22.8	6.15
t-PSFB	45	96.78	1.22	Infineon, 30	GeneSiC, 30	19.6	31.0	8.86
r-PSFB	15	97.72	1.69	Infineon, 30	Infineon, 30	11.2	13.5	4.81
r-PSFB	45	97.24	1.36	Infineon, 30	Infineon, 30	19.6	24.1	7.31
i-PSFB	15	97.31	2.11	Infineon, 30	GeneSiC, 30	10.4	22.8	5.02
i-PSFB	45	96.45	1.53	GeneSiC, 50	GeneSiC, 40	18.7	31.1	6.91

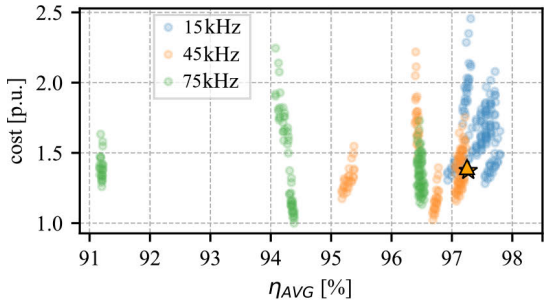
Then, combined with the magnetic components and the RCD snubber circuit, the system efficiency performance can be estimated using the analytical models of the converters. The detailed analytical model of the PSFB type converter used in this article is presented in [12].

Fig. 13 shows η_{AVG} and the relative cost of all the possible designs. First of all, it can be seen from Fig. 13(a) and (b) that, by increasing the switching frequency, the cost will drop, and the PD of the magnetics will increase. However, η_{AVG} will also drop. This tradeoff mainly comes from the reduction of magnetic components material and the increase of switching loss of the semiconductors when increasing f_{sw}. At 15 kHz, the optimal design can be obtained from the t-PSFB converter. When f_{sw} increases to 45 kHz, the designs of the r-PSFB converter start to be competitive since the PD increases and cost reduces considerably, while η_{AVG} suffers less reduction compared to the other topologies. When f_{sw} further increases to 75 kHz, the gain on the PD increase and cost saving is limited, while η_{AVG} drops significantly for the conv/t/i-PSFB converters.

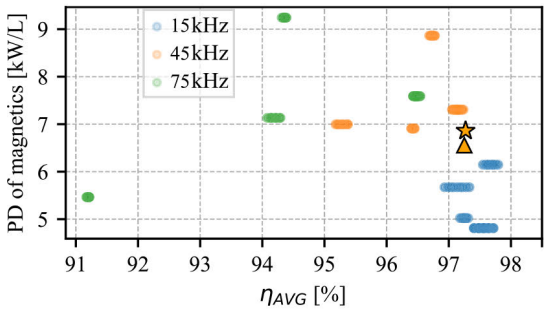
Second, in terms of the PD of the magnetic components, heatsinks, and normalized price of the converters, the t-PSFB converter is able to deliver the lowest cost and highest PD designs from 15 to 75 kHz. Even though the conv-PSFB has the same components count as the t-PSFB, the current stress of the transformer and the dV/dt stress of the inductor of the t-PSFB is less than that of the conv-PSFB due to the feature of reconfiguration. This factor benefits the t-PSFB converter to have more power-efficient, smaller, and cheaper designs of magnetic components. The i-PSFB converter is the most expensive one due to the high component account. The r-PSFB converter that has eight rectifier diodes with 1200-V voltage ratings is slightly more expensive than the t-PSFB, which has four rectifier diodes with a 1700-V voltage rating. This corresponds to the trend shown in Fig. 6 that the cost of the 1200-V rectifier diodes are less expensive than the 1700-V ones with the same $R_{\text{D(on)}}$ but not less than half.

Third, in terms of η_{AVG}, the i-PSFB and r-PSFB topologies are able to provide the η_{AVG}-advantageous designs in 15 kHz. The conv-PSFB generally has lower η_{AVG}, especially when f_{sw} increases. To better interpret the η_{AVG} performance of these converters, two designs of each converter topology that have the highest η_{AVG} and lowest normalized costs in 15 and 45 kHz are selected for further analysis. The detailed information about these designs is summarized in Table XIII, and the breakdown of the averaged losses of these designs are illustrated in Fig. 14.

From Fig. 14, it can be seen that the averaged conduction loss and switching loss on the transistors of the t/r/i-PSFB designs are less than that of the conv-PSFB design. This is due



(a)



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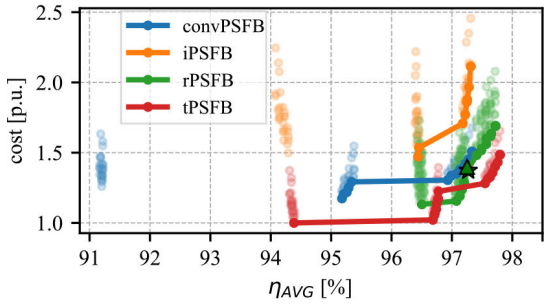

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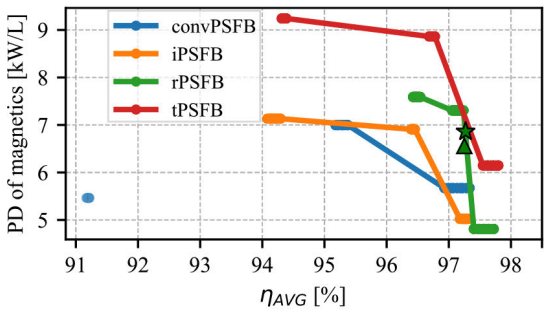

(d)

Fig. 13. Averaged full-power/current efficiency (η_{AVG}), the cost, and the PD of the magnetic components and heatsink of the possible designs of all four PSFB topologies. The target design and the actual prototype design are marked as the star and the triangle, respectively. (a) Cost (p.u. value) versus η_{AVG}. (b) PD of the magnetic components and heatsink versus η_{AVG}. (c) Cost (p.u. value) versus η_{AVG}. (d) PD of the magnetic components and heatsink versus η_{AVG}.

to the reconfiguration ability, and the t/r/i-PSFB topologies are able to have less current stress on the transistors in the low output voltage operation. This point is also revealed in the worst case current stresses listed in Table III. It is an interesting

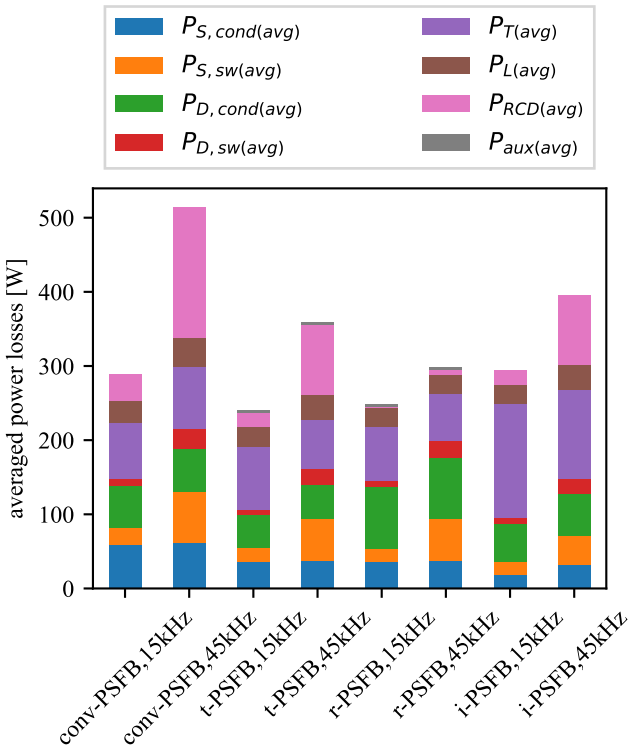

Fig. 14. Breakdown of the averaged losses of the advantageous designs from Fig. 13. $P_{\mathrm{S,cond(avg)}}$ and $P_{\mathrm{D,cond(avg)}}$ are the averaged conduction losses on the transistors and rectifier diodes, $P_{\mathrm{S,sw(avg)}}$ and $P_{\mathrm{D,sw(avg)}}$ are the averaged switching losses on the transistors and rectifier diodes, $P_{\mathrm{T(avg)}}$ and $P_{\mathrm{L(avg)}}$ are the averaged transformer losses and inductor losses, $P_{\mathrm{RCD(avg)}}$ is the averaged RCD snubber circuitry loss, and $P_{\mathrm{aux(avg)}}$ is the averaged auxiliary switch conduction losses.

observation that the i-PSFB converter has the lowest transistor losses. The first reason is that the i-PSFB converter has shared current stresses on the two full bridges, which potentially lowers the total conduction loss according to the resistive loss calculation $P_{\mathrm{Ohmic}} = I^2R$. The second reason is that the use of transistors with relatively high $R_{\mathrm{ds(on)}}$ brings less switching losses, as shown in Fig. 7. The r-PSFB converter designs have higher losses on the rectifier diodes. This is mainly due to the doubled amount of diodes on the conduction path, and the current is shared only during the parallel-connection configuration when V_{out} is low. The i-PSFB converter designs have the highest transformer losses even though the current is shared between the two transformers. The main reason is that the dB/dt stress on the transformers is not shared. In terms of inductor losses, the r-PSFB converter performs better than the other three converters. By having two secondary sides, the dB/dt stress on the two inductors of the r-PSFB converter is halved in the series connection operation due to the voltage sharing, which helps reduce the averaged inductor core losses. The most significant difference in losses lies in the snubber circuitry loss $P_{\mathrm{RCD(avg)}}$. The r-PSFB converter has significantly less $P_{\mathrm{RCD(avg)}}$ compared to the others, while the conv-PSFB suffers the highest $P_{\mathrm{RCD(avg)}}$. This can be explained by the equations used for calculating the resistance value and the power loss of the RCD snubber circuitry, whose details can be found in [12], [25]. Due to the split secondary sides, not only high resistance value can be used for the RCD snubber circuits of the r-PSFB converter, but also the voltage stress on the R_{RCD} is much less compared to the other topology.

TABLE XIV
SPECIFICATIONS OF THE PROTOTYPE

input voltage [V]	640-840
output voltage [V]	250-1000
power rating [kW]	11
f_{sw} [kHz]	45
MAX output current [A]	30
transistor	IMW120R030M1H
rectifier diode	IDW30G120C5B
transformer core material	N87
transformer core shape	3xEE70/33/32
transformer N_{prim}: N_{sec}	8:7
inductor design	refer to Table XII
gate driver	ISO5852
DSP controller	TMS320F28379D

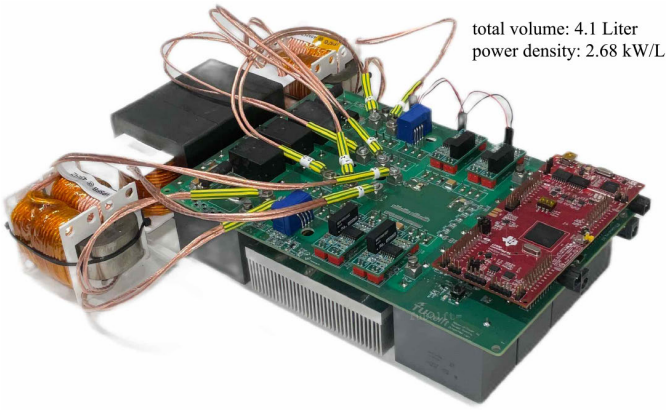

Fig. 15. Prototype of the 45-kHz r-PSFB converter.

In practical implementation, this splitting structure of r-PSFB topology also brings the benefit of loss sharing on the two RCD circuitries, which means simpler thermal design as well.

Based on these observations of the multiobjective design results, the t-PSFB converter operating at 15 kHz and the r-PSFB converter at 45 kHz with the right choices of semiconductor components stands out as the most advantageous converter designs in terms of the normalized cost, PD of magnetics and heatsinks, and η_{AVG} performance.

VI. EXPERIMENTAL VERIFICATION

In order to verify the multiobjective design prediction, a close-to-Pareto-front 45-kHz r-PSFB prototype converter is built based on the multiobjective optimization design process described previously. Due to the availability issue of the components in today's market, the prototype converter has to be built with some adjustments on the selection of components. The ferrite core shape used for the transformer design changes from the intended EE65/32/27 from Table XI to the EE70/33/32 since the prior was out of stock in our trusted suppliers. The MOSFETs and rectifier diodes used in the prototype are IMW120R030M1H and IDW30G120C5B from Infineon, which were immediately available in the laboratory of the authors. The inductors are designed according to the optimal inductor design in Table XII. Table XIV shows the detailed parameters and components used for the prototype converter. As a result, the target design is marked as the star shown in Fig. 13, which is close to the obtained Pareto front of the design space.

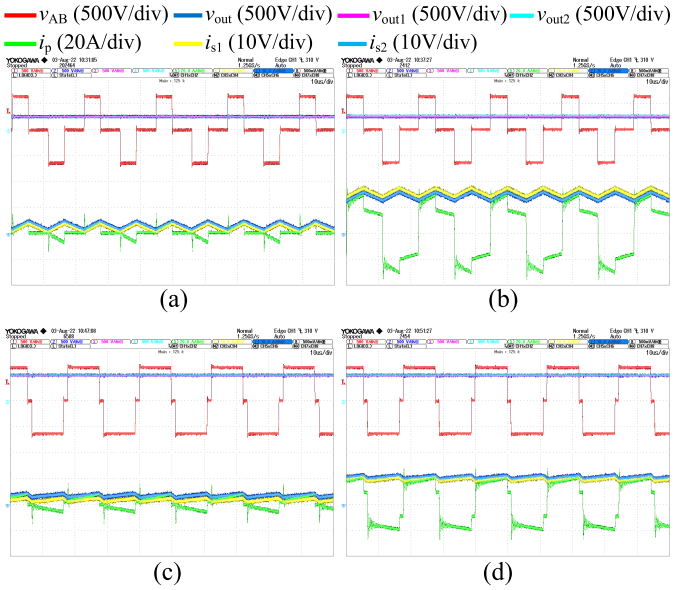

Fig. 16. Operational waveform of the r-PSFB converter in parallel connection mode with V_{in} = 640 V. $v_{out1/2}$ and $i_{s1/2}$ are the output voltage and current of the two secondary side rectifiers, measured after the RCD circuitry and on the output inductors, respectively. (a) V_{out} = 250 V and I_{out} = 5 A. (b) V_{out} = 250 V and I_{out} = 30 A. (c) V_{out} = 490 V and I_{out} = 5 A. (d) V_{out} = 490 V and I_{out} = 20 A.

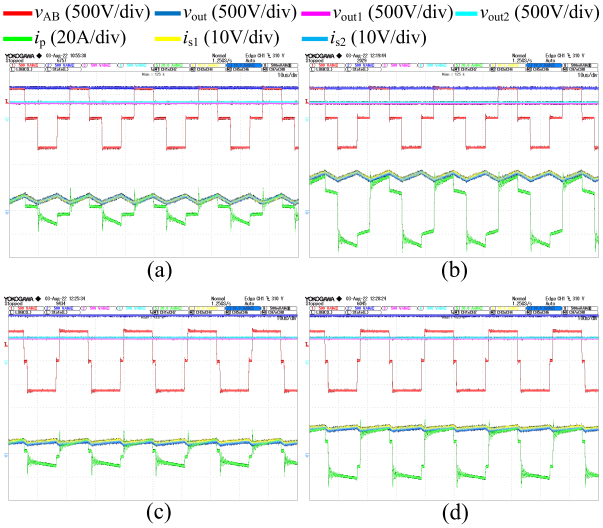

Fig. 17. Operational waveform of the r-PSFB converter in the series connection mode with V_{in} = 640 V. (a) V_{out} = 600 V and I_{out} = 5 A. (b) V_{out} = 660 V and I_{out} = 15 A. (c) V_{out} = 1000 V and I_{out} = 5 A. (d) V_{out} = 1000 V and I_{out} = 11 A.

Fig. 15 shows the picture of the 45-kHz r-PSFB prototype converter. The prototype converter has a PD of 2.68 kW/L. Figs. 16 and 17 show the operational waveform of the prototype in parallel and series connection mode with different V_{out}'s and I_{out}'s. Fig. 18 shows the waveform of the RCD clamping circuitry of the r-PSFB prototype. It can be seen that the prototype converter is able to operate in an extensive output voltage range from 250 to 1000 V with different output current conditions, and the voltage clamping circuitry functions well.

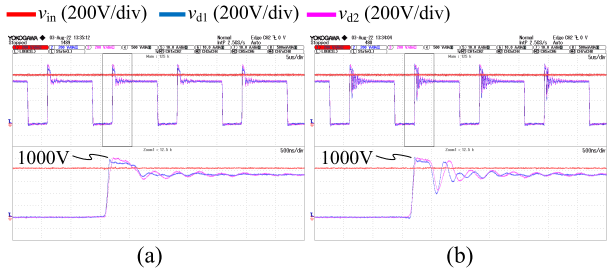

Fig. 18. Voltage clamping waveform of the RCD snubber circuitry, with $V_{in} = 840$ V. $v_{d1,2}$ are the diode voltage of the two secondary sides. (a) Parallel connection. (b) Series connection.

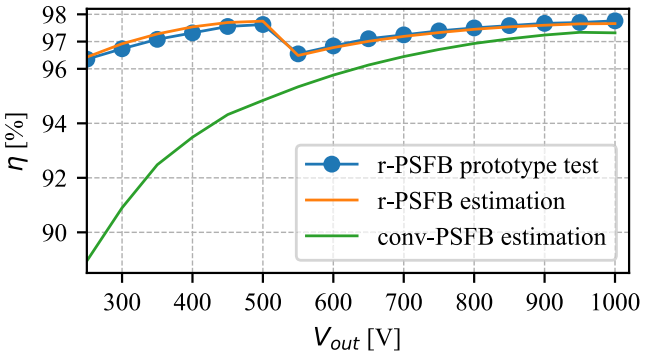

Fig. 19. Estimated efficiency of the 45-kHz r-PSFB and conv-PSFB converter designs and the test efficiency of the 45-kHz r-PSFB prototype converter with full power or maximum output current, $V_{in} = 640$ V.

TABLE XV

DETAILED INFORMATION OF THE TARGET R-PSFB DESIGN AND THE ACHIEVED R-PSFB PROTOTYPE DESIGN FROM FIG. 13

	f_{sw}[kHz]	η_{avg} [%]	cost [p.u.]	Magnetics&heatsink PD
target	45	97.27	1.37	6.86 [kW/L]
prototype	45	97.25	1.40	6.56 [kW/L]

In order to verify the efficiency performance of the 45-kHz r-PSFB prototype converter, the full-power/current efficiency is tested and plotted together with the estimated efficiency in Fig. 19. In addition, the estimated efficiency of the optimal conv-PSFB converter design at 45 kHz, as listed in Table XIII, is also plotted for comparison. It can be seen that the test efficiency of the r-PSFB prototype matches well with the estimation. The peak efficiency achieved is 97.76%. The tested average full power/current efficiency is 97.25%, which is very close to the estimated value of 97.27%. The error in loss prediction is mainly due to the simplification of both analytical models for the conduction and switching losses of the semiconductors. The actual cost, average efficiency, and the power density of the magentic components and heatsink of the prototype are summarized in Table XV, and they are plotted in Fig. 13 as the triangle. It can be seen that the prototype implementation is very close to the target. The efficiency of the r-PSFB converter drops as V_{out} decreases from 1000 to 500 V due to the increasing phase shift angle and associated circulating losses. However, when V_{out} decreases further below 500 V, the r-PSFB converter reconfigures from a series connection to a parallel connection, resetting the phase shift angle and bringing up the efficiency. In comparison, the efficiency of the 45-kHz optimal conv-PSFB design drops constantly as V_{out} decreases. This demonstrates the efficiency benefit of the reconfigurable structure PSFB converters.

VII. CONCLUSION

In this article, three reconfigurable structure PSFB converters are analyzed and benchmarked for the extended wide voltage range public EV charging application. A multiobjective converter design process that considers the normalized cost, PD of the magnetic components and heatsinks, and the average efficiency performance is introduced. In this proposed design process, well-accessible data provided by the components redistributors are utilized to establish the correlations between the cost and loss performance of the components, which are used in the design process to determine the most advantageous converter in terms of the cost, PD of the magnetics and heatsink, and the averaged efficiency. Based on the resulted design space of the converters, a close-to-Pareto-front 45-kHz r-PSFB prototype converter is built to verify the analysis, and the actual cost, PD of the magnetics and heatsink, and averaged efficiency match with the design well. This proves the feasibility of the proposed multiobjective design and benchmark process, and identifies the t-PSFB and r-PSFB converters to be the outstanding solutions in the wide voltage range public EV charging application.

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