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DOI
10.1109/LMWC.2022.3170929

Publication date
2022

Document Version
Final published version

Published in
IEEE Microwave and Wireless Components Letters

A 76.5–92.6 GHz CMOS LNA Using Two-Port kQ-Product Theory for Transformer Design

Youming Zhang, *Member, IEEE*, Zhennan Wei, Xusheng Tang, Linghan Zhang, and Fengyi Huang, *Member, IEEE*

***Abstract*— This letter presents a convenient approach based on the two-port kQ-product theory to analyze the influence of interwinding capacitive coupling on the efficiency of the transformer. It is demonstrated that a transformer with proper size can benefit from the interwinding capacitive coupling to maximize its efficiency at a desired frequency. The proposed design approach is used in a W-band low-noise amplifier (LNA) fabricated with the 40-nm CMOS process to optimize the insertion loss of the input transformer-based balun. Thanks to the approach, the W-band LNA achieves a minimum noise figure of 5.7 dB, a maximum gain of 18.5 dB, and a 3-dB bandwidth of 76.5–92.6 GHz, while consuming 23.4 mW from a 0.9-V supply.**

***Index Terms*— kQ-product, low-noise amplifier, millimeter-wave (mmWave), transformer, W-band.**

I. Introduction

RECENTLY there has been an emerging demand for millimeter-wave (mmWave) integrated circuits for wireless communication and radar applications such as the E-band high date rate communication and the 77-GHz/79-GHz/90-GHz radar. As the first block in a receiver, the low-noise amplifier (LNA) plays a critical role in the performance of the whole system. LNA is required to provide sufficient gain with a low noise figure (NF) to improve the receiver's sensitivity.

In the LNA design, the differential configuration is usually preferred due to its immunity to common-mode noise from the ground and supply. In this case, an input balun, which is mostly made by an on-chip transformer in mmWave circuits, is needed for single-end-to-differential conversion. However, as the first stage, the transformer-based input balun contributes a significant part to the LNA's NF. Hence, it is important to design a transformer with low insertion loss (IL) and high efficiency to minimize its NF degradation to LNA.

Several efforts have been made to elaborate the transformer's efficiency at mmWave frequencies. Zhao and Reynaert [1] show by simulation that transformers with larger size tend to exhibit higher maximum efficiency (or lower IL) due to larger magnetic coupling between the two windings. As an improvement, the formula of transformers' maximum efficiency $\eta_{\max}$ was declared in [2]. It shows that the maximum efficiency is positively related to the product of the coupling coefficient k and the quality factor Q of the winding. In fact, as early as 2007, Kurs *et al.* [3] revealed that not k alone but the kQ-product plays a pivotal role in coupled resonant coils [3], Then, the kQ-product theory has become a powerful tool and actually been extended to represent general two-port systems' transfer characteristics [4], [5].

However, articles no matter about circuit design or two-port system analysis generally did not consider the nonignorable capacitive coupling between the two windings of a transformer to facilitate transformers' maximum efficiency. Intuitively, the interwinding capacitive coupling creates a new path for power transmission, and thus it is possible to be used to enhance the efficiency of the transformer. So far, a thorough design methodology about interwinding capacitive coupling effect for maximizing on-chip transformer efficiency is still lacking.

Therefore, in this letter, we present an approach based on the two-port kQ-product theory to analyze the effects of capacitive coupling in an on-chip transformer, so as to provide a more convenient way to facilitate efficiency optimization of the on-chip transformer. To validate it, a W-band LNA is designed with transformer-based input balun implemented in the 40-nm CMOS process. The LNA achieves competitive overall performances with a minimum NF of 5.7 dB at 91 GHz, a maximum gain of 18.5 dB, a 3-dB BW of 76.5–92.6 GHz, and a compact chip area.

II. Transformer Efficiency Optimization Design Based on kQ-Product Theory

To analyze the effects of interwinding capacitive coupling on the maximum efficiency ($\eta_{\max} = 10^{G_{\max}/10}$) of a transformer, the two-port kQ-product theory has been introduced in this letter. In [5], the definition of kQ-product is extended as a general metric for the power transfer potentiality of all two-port systems. The larger kQ-product that a two-port system has, the higher $\eta_{\max}$ will be achieved. The definition of kQ-product in [5] is expressed as below:

$$kQ = |Z_{21}|/\mathrm{ESR}. \tag{1}$$

In this equation, ESR is called the *equivalent scalar resistance* of a two-port system and indicates the system's loss assessment in the immittance domain [5]. It is formulated as

$$\mathrm{ESR} = \sqrt{\mathrm{Re}[Z_{11}]\mathrm{Re}[Z_{22}] - \mathrm{Re}[Z_{12}]\mathrm{Re}[Z_{21}]}. \tag{2}$$

Manuscript received 19 March 2022; accepted 24 April 2022. Date of publication 5 May 2022; date of current version 7 October 2022. *(Corresponding author: Youming Zhang.)*

Youming Zhang, Xusheng Tang, and Fengyi Huang are with the School of Cyber Science and Engineering, School of Microelectronics, Southeast University, Nanjing 210096, China, and also with the Purple Mountain Laboratories, Nanjing 211111, China (e-mail: zhangyouming@seu.edu.cn).

Zhennan Wei is with the School of Information Science and Engineering, Southeast University, Nanjing 210096, China.

Linghan Zhang was with the School of Information Science and Engineering, Southeast University, Nanjing 210096, China. He is now with the Department of Microelectronics, Technische Universiteit Delft, 2628 Delft, The Netherlands.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2022.3170929.

Digital Object Identifier 10.1109/LMWC.2022.3170929

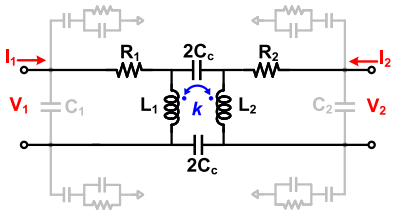


Fig. 1. Simplified equivalent circuit model of the transformer.

The simplified equivalent circuit model of the transformer is shown in Fig. 1. In this model, the interwinding capacitive coupling effect is modeled as two capacitors (C_c) between the primary and secondary windings. For simplicity, the substrate parasitic elements are neglected, and symmetry assumption is made to this model, namely, $L_1 = L_2 = L$ and $R_1 = R_2 = R$. In addition, because shunt capacitance C_1 and C_2 can be absorbed into the forward and rear matching networks, they will not be included in the kQ-product equation. Thus, we can obtain

$$Z_{11} = Z_{22} = R + j\omega L \frac{-\omega^2(1-k^2)LC_c}{1-2\omega^2(1-k)LC_c} \tag{3}$$

$$Z_{12} = Z_{21} = j\omega L \frac{k-\omega^2(1-k^2)LC_c}{1-2\omega^2(1-k)LC_c}. \tag{4}$$

Then, the kQ-product of the transformer can be expressed as

$$kQ = \frac{\omega L}{R}\left|\frac{k-\omega^2(1-k^2)LC_c}{1-2\omega^2(1-k)LC_c}\right|. \tag{5}$$

Since $\omega L/R$ is the Q-factor of the windings, it can be obviously found that if C_c is neglected, the right side of (5) will become $(\omega L/R)k$ and less than the Q-factor of the windings. However, when C_c is considered, the equivalent coupling effects of the transformer are boosted and the kQ-product exhibits a maximum value at

$$f_{\text{peak}} = \frac{1}{2\pi\sqrt{2(1-k)LC_c}} \tag{6}$$

which means that a peak $\eta_{\max}$ can be achieved at f_{peak}. It just reflects that interwinding capacitive coupling is potential to boost the efficiency of the transformer at appropriate operating frequency band. Note that although the right side of (5) approximates to infinity at f_{peak}, due to the substrate loss and the effects from other high-order parasitic elements, the peak kQ-product at fpeak of a real transformer will actually be a finite value.

To validate the above analysis approach, two on-chip transformers are inserted into electro-magnetic (EM) simulator, and the kQ-product and $\eta_{\max}$ are shown in Fig. 2. The two transformers have the same diameter and trace width but different signs of k-factor. It can be seen that the curves of the kQ-product and $\eta_{\max}$ of the transformer have the same peak frequency and trend. The inverting ($k < 0$) and noninverting ($k > 0$) transformers exhibit peak kQ-product and $\eta_{\max}$ at f_{peak1} and f_{peak2}, respectively, while the inverting transformer has a lower f_{peak} than its noninverting counterpart, which can also be derived from the equation of f_{peak}. Thus, the

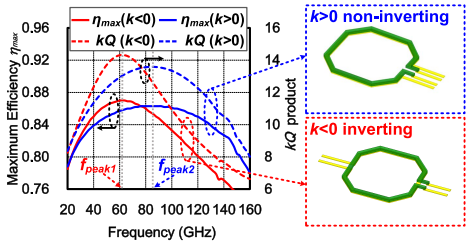
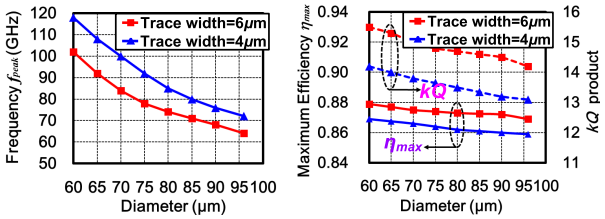


Fig. 2. Simulated kQ-product and $\eta_{\max}$ of transformers.



(a) (b)

Fig. 3. Simulated (a) f_{peak} and (b) $\eta_{\max}$ and kQ-product versus diameters under different trace widths of the one-coil transformers with stacked top two thick metal layers.

kQ-product is able to be used to characterize the power transfer potentiality of on-chip transformers.

As shown in (5) and (6), the kQ-product (or $\eta_{\max}$) of a transformer can be maximized at f_{peak} by choosing proper winding inductance L, k and interwinding capacitance C_c. Since parameters L, k, and C_c are closely related to the sizing parameters of a transformer, geometrical size such as the diameter and trace width needs to be properly designed.

For the W-band application, the top two thick metal layers are used to construct stacked one-coil transformer to reduce the parasitic resistance and the substrate parasitic effect resulting in enhanced kQ-product. The f_{peak} for the trace width varying from 4 to 6 μm and the diameter in the range of 60–100 μm are plotted in Fig. 3(a). The corresponding kQ-product and $\eta_{\max}$ are plotted in Fig. 3(b). We can easily pick and choose the transformer with diameter of 75 μm and trace width of 6 μm that achieves a f_{peak} of roughly 80 GHz and a $\eta_{\max}$ of 0.87, which translates to a minimum IL of only 0.6 dB.

III. W-Band LNA Design

Fig. 4 shows the schematic of the proposed W-band LNA with important device parameters. LNA consists of three stages of pseudo-differential common-source amplifiers. The capacitive neutralization technique is adopted in the second and third stages to improve LNA's gain and stability. The input matching network is implemented with a transformer-based balun in series with transmission lines (TLs) for broadband matching.

The proposed transformer design approach based on the two-port kQ-product theory is used to minimize the IL of the transformer. In the transformer design, the stack structure is chosen to realize proper interwinding capacitance to obtain the peak $\eta_{\max}$ at the desired frequency.

Since interwinding capacitance of the transformer-based balun can lead to differential imbalance, bypass capacitance CB is implemented with metal-oxide-metal (MOM) capacitors to short the center tap to ac ground to mitigate the imbalance, and with custom-designed MOS capacitors to enhance

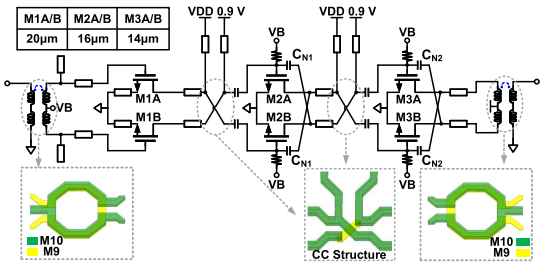


Fig. 4. Schematic of the proposed LNA.

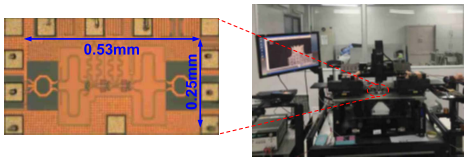


Fig. 5. Measurement setup and chip micrograph of the proposed LNA.

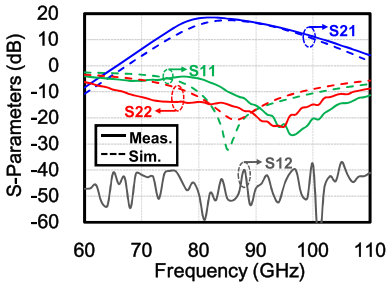


Fig. 6. Measured and simulated S-parameters of the proposed LNA.

stability of LNA. The cross-coupling (CC) structures are used to mitigate the asymmetry introduced by interstage TLs.

To further improve LNA's gain and NF performance, the bottom two metal layers ($M1$ and $M2$) are stacked together to make the ground plane of the microstrip lines, which reduces the ohmic loss in the ground plane. Simulation shows that compared with single metal later ($M1$), $M1$ and $M2$ stacking structure can improve the gain and NF of LNA by 0.9 and 0.4 dB, respectively.

IV. Implementation and Measurement

The W-band LNA is implemented in the 40-nm CMOS technology. Fig. 5 shows the measurement setup and the chip micrograph. The LNA occupies a core chip area of 0.53×0.25 mm^2 and consumes 23.4 mW from a 0.9-V supply. On-wafer S-parameter measurement is shown in Fig. 6. The maximum S21 is 18.5 dB at 84 GHz with a 3-dB BW of 76.5–92.6 GHz. The discrepancy between the measurement and simulation results mainly attributes to modeling inaccuracies in EM simulation. Rollett stability factor Kf and Δ are shown in Fig. 7(a) indicating unconditional stable. A simulated IP1 dB of above -19 dBm is achieved and shown in Fig. 7(b). A 75–110-GHz noise source and a Keysight N8975A NF analyzer are used to measure NF in Fig. 8. A W-band preamplifier is used following LNA to provide enough gain to improve the system noise floor. IL of ground-signal-ground (GSG) probes and noise of the preamplifier can be calibrated out. The measured NF ranges from 5.7 to 7.3 dB in the 3-dB BW with a minimum value of 5.7 dB at 91 GHz.

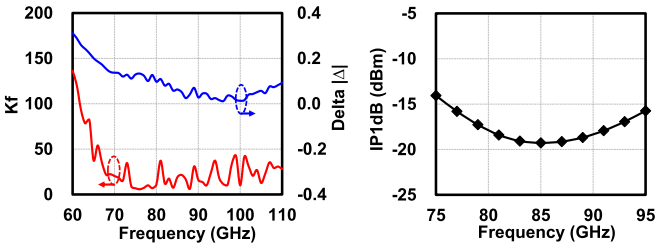


Fig. 7. (a) Measured stability factor Kf and Δ. (b) Simulated IP1 dB.

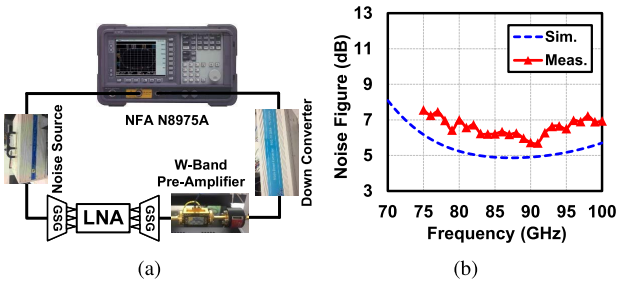


Fig. 8. (a) NF measurement setup. (b) Measured and simulated NF.

TABLE I
COMPARISON WITH PRESENTED CMOS MMWAVE LNAS

Ref.	**This Work**	[6] MWCL'16	[7] JSSC'17		[8] TMTT'20		[9] IMS'20
Process (nm)	**40-nm CMOS**	65-nm CMOS	65-nm CMOS		22-nm FD-SOI		55-nm CMOS
f_0 (GHz)	**84**	104	77.25	77.5	77	92	82.7
BW (GHz)	**16.1**	21.5	27.5	30	13	31	7.6[+]
Gain (dB)	**18.5**	16.7	13.3	18.5	24	18.2	15
NF (dB)	**5.7–7.3**	7.2–9.0	6.4–8.5	5.5–7.9	4.6[#]	5.8–7.5[#]	5.0–7.5
Supply (V)	**0.9**	1.8	1.2	1.8	1.6	1.6	1.2 & 2.0
Power (mW)	**23.4**	45	12	27	16	16	72.7
Area (mm^2)	**0.174**	0.29	0.24		0.35	0.43	0.106
FoM[*] (dB)	**2.5 – 6.6**	-6.5 – -2.3	4.8–10.0	5.1–11.3	16.7	10.6–15.0	-17.9 – -11.3

[+] 5-dB BW is 23.5 GHz.
[#] 4.6dB is the Minimum NF, and 5.8–7.5 dB is partial frequency band (90–96 GHz) NF.
[*] $\text{FoM} = 20\log_{10}\left(\frac{Gain[\text{lin.}]\cdot \text{BW[GHz]}}{P_{dc}[\text{mW}]\cdot(\text{NF[lin.}]-1)}\right)$

The measured results are summarized and compared with the prior arts [6]–[9] in Table I. Thanks to the proposed approach using two-port kQ-product theory for transformer design, the W-band LNA in this letter exhibits competitive overall performances with an excellent NF under low supply voltage and compact chip area.

V. Conclusion

This letter presents a convenient approach to evaluate and optimized the effects of interwinding capacitive coupling on a transformer. By properly designing the winding inductances, k-factor, and interwinding capacitances, the efficiency of the transformer can be maximized at the desired frequency. This design approach is then validated in a W-band CMOS LNA as to optimize the transformer-based balun. Under a low supply voltage of 0.9 V, LNA presents good overall performances with a measured NF of 5.7–7.3 dB, a maximum gain of 18.5 dB, a 3-dB BW of 76.5–92.6 GHz, and a 23.4-mW power consumption, as well as a compact chip area.

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