A Wideband Millimeter-Wave Power Amplifier With 20 dB Linear Power Gain and +8 dBm Maximum Saturated Output Power

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***Abstract*—A millimeter-wave power amplifier fabricated in 90 nm bulk CMOS technology consists of 3 identical cascode stages and on-chip matching networks (inter-stage, input, and output) implemented with wide-gap coplanar waveguides and M6-M5 (MIM) capacitors. The amplifier realizes a linear power gain of 19.7 dB at 52.4 GHz and 10.3 dB at 60 GHz. Maximum saturated output power and output-referred −1 dB compression point are +8.2 dBm and 3.1 dBm, respectively. Peak PAE is 4.2%. The 1.18 × 0.96 mm² die consumes 75 mA when operating from a 2 V supply.**

***Index Terms*—CMOS power amplifier, millimeter-wave (mm-wave) power amplifier, power amplifier (PA), 60 GHz circuits, wideband.**

I. Introduction

THE rapid growth of wireless communications for broadband wireless personal area networks (WPANs), has sparked interest in the exploitation of millimeter-wave (mm-wave) bands using silicon RF integrated circuits [1]–[7]. Other potential applications in the mm-wave frequency range are: automotive long-range (77/79 GHz) radars for collision avoidance, security (e.g., radio imaging at 94 GHz) and extreme wideband communication in the 120 GHz band.

Realizing Gbits/s data throughput with a relaxed requirement on spectral efficiency may require much greater channel bandwidth than is currently used by even ultra-wideband (UWB) radios operating in the 3.6–10.1 GHz frequency range (e.g., 480 Mb/s MB-OFDM links). The 3 GHz of bandwidth available worldwide between 59 and 62 GHz could be exploited for this purpose [8]. Fig. 1 shows channel capacity and the spectral allocations for different wireless standards. Spectral efficiency and channel bandwidth can be increased in order to increase this capacity, as predicted by Shannon's theorem [9]. A wireless system such as Bluetooth (e.g., Version 2.0+EDR) is limited to a maximum throughput of 2.1 Mb/s by its relatively low spectral efficiency of approximately 0.5 bits/s/Hz of channel bandwidth. The latest 802.11.n WLAN systems realizes an order of magnitude higher spectral efficiency (∼5 bits/s/Hz) by utilizing multi-input/multi-output (MIMO) antenna diversity, and can support data rates up to 248 Mb/s. Thus, greater spectral efficiency is typically achieved at the cost of implementation complexity, which can affect the system's robustness.

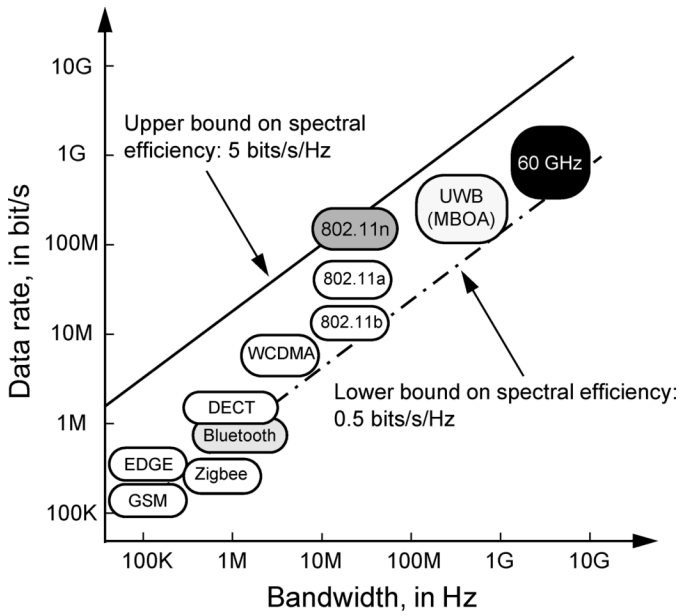

Fig. 1. Spectral efficiency requirement for various wireless standards with different data rates and bandwidths.

The 60 GHz band is also of interest for short-range communications (i.e., within 10 m range), because the free-space attenuation of at least 10–15 dB/km isolates cells in a local-area network. Co-channel interference is low as a result of directional antennas and high path loss at 60 GHz, which makes in-room broadband transmission feasible. Millimeter-wave links typically require physically small antennas because of the short wavelength, however, their directionality may require mechanical or electrical beam steering in order to enhance the antenna gain [2], [10].

The IEEE 802.15.3.c and WirelessHD groups have developed a standard for 60 GHz broadband data communication radios [11], [12]. According to their preliminary proposals, an antenna gain of up to 30 dBi and 10 dBm transmit power into the antenna could satisfy the global requirement of the electromagnetic field emission [13]. Hence, 10 dBm output power was selected as the target for the power amplifier (PA) prototype developed in this work.

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Silicon CMOS technology is evolving rapidly and offers lower cost per chip in volume manufacture together and the potential for VLSI integration of digital baseband and RF/mixed-signal circuits. Moreover, high throughput (>4 Gb/s) for burst data transfers requires high-speed digital signal processing that is best realized in the fastest baseline CMOS processes. Approximately 9 dB power gain in the 60 GHz band has been demonstrated by 90 nm nMOS transistors, with unity-current gain frequency f_T and unity-power gain frequency $f_{\max}$ on the order of 120 GHz/280 GHz, respectively. The passive components in CMOS technologies, such as inductors, transmission lines and metal–insulator–metal (MIM) capacitors, scale with increasing operating frequency, and complement the operation of active devices by optimizing gain over a reduced bandwidth (e.g., using a resonant loads). The combined effects of frequency and device scaling with potential mm-wave applications are stimulating many new research activities [3]–[6], [16]–[20], [24]–[26].

The prime objective of this work is to benchmark the 90 nm CMOS technology and its design kit in a mm-wave application that could be used to further improve computer simulation models and identify potential problems in the design flow.

In the following sections, the design of a PA with close to 20 dB linear power gain at 52.4 GHz and $+8$ dBm saturated output power is described. The circuit is realized in a baseline bulk CMOS090 LP technology [14], which features six damascene copper metal layers (five thin and one thick), and low-k ($\varepsilon_{\rm r} < 3.0$) inter-metal dielectric between the thin metal layers. MIM capacitors were designed completely from interconnect metals, hence no additional process options (e.g., dedicated MIM capacitors or trimmed polysilicon resistors) are used. Section II of this paper presents the CMOS PA topology and the circuit choices, and the experimental results of the amplifier are summarized in Section III.

II. Circuit Topology and Design

A peak transmit power of approximately 10 dBm and 20 dB power gain is the design goal for the prototype. The peak f_T of nMOSFETs in the 90 nm CMOS technology chosen for this work is less than 150 GHz, so a multi-stage amplifier is required in order to achieve 20 dB gain at 60 GHz.

On-chip passive components implement the input, inter-stage and output matching networks. A wide-gap coplanar waveguide (CPW) over ground plane (which implements a microstrip type transmission line) and MIM capacitors implemented in top (M6) and M5 metals were characterized in a separate fabrication run. This data was used to extract circuit models for the key RF passives and thereby improve simulation accuracy for the passives in the PA prototype.

This section begins with a discussion of mm-wave PA circuit topologies for a single-ended PA. The output stage design is then considered, where load-pull simulations are used to find the optimal load impedance for maximum power transfer to the antenna at approximately 10 dBm output. The required impedance matching networks are then synthesized, and two pre-driver stages with inter-stage matching are added to realize an overall power gain of 20 dB from the amplifier.

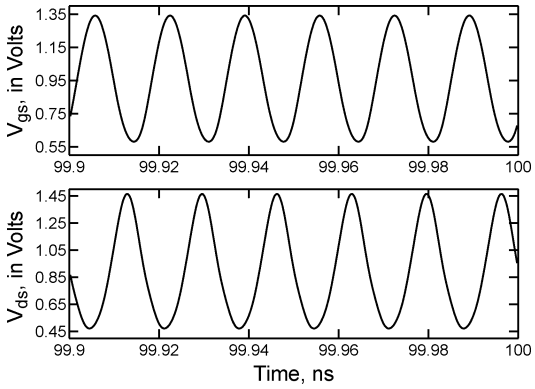

Fig. 2. Simulated steady-state $V_{\rm gs}$ and $V_{\rm ds}$ versus time for the cascode transistor in the output stage of Fig. 4 ($V_{\rm DD} = 2$ V, $\rm P_{out} = +7$ dBm and $V_{\rm GS\text{-}breakdown} = 1.6$ V).

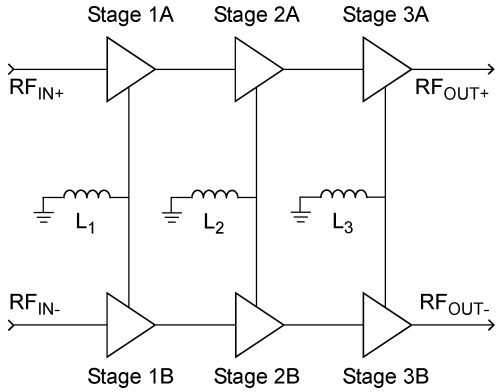

Fig. 3. Simplified schematic for the differential three-stage cascode power amplifier (note each stage is topologically similar to the output stage as shown in Fig. 4).

A. Millimeter-Wave PA Topology

Class-A biased stages were chosen for the PA prototype [21]. In order to maximize isolation and quench any tendency for parasitic oscillation, cascode gain stages are used. The cascode also reduces voltage stress on each transistor that can lead to breakdown and failure. In order to compensate for the loss of headroom at the drain of the output transistor (i.e., common-gate) in the cascode, the supply voltage is increased to 2 V. However, no degradation in reliability is expected in continuous operation. Fig. 2 shows the simulated steady-state $V_{\rm gs}$ and $V_{\rm ds}$ versus time of the cascode transistor in the output stage (schematic of Fig. 4) for $V_{\rm DD} = 2$ V and $+7$ dBm output power. From specifications for the 90 nm technology, the gate-source breakdown voltage is lower than the drain-source breakdown voltage (making $V_{\rm gs}$ the worst-case condition) and $V_{\rm gs}$ must not exceed 1.6 V in order to avoid breakdown. As seen from the plots, peak-$V_{\rm gs}$ of the cascode transistor (which is the worst case) is well below the specified breakdown voltage. To further guard against potential instability, the gate bias of cascode transistors is decoupled using a high quality capacitor to provide a low impedance path to the AC ground.

Both single-ended and differential topologies are commonly used in RF Class-A amplifiers. The performance of 60 GHz PAs in both configurations from simulation is compared in Table I. The differential PA consists of two single-ended amplifiers,

TABLE I
SIMULATED PA PERFORMANCE SUMMARY ($f_{\rm out} = 60$ GHz, $V_{\rm DD} = 1.5$ V)

PA topology	$\lvert S_{21}\rvert_{\max}$ in dB	$P_{-1dBout}$ in dBm	P_{sat} in dBm	P_{DC} in mW	PAE_{pk} in %	Chip area (+bondpads) in mm^2
Single-ended	25	3.2	9.6	109.5	8.4	1.18×0.96
Differential	32	7	12	150.3	10.8	1.18×1.78

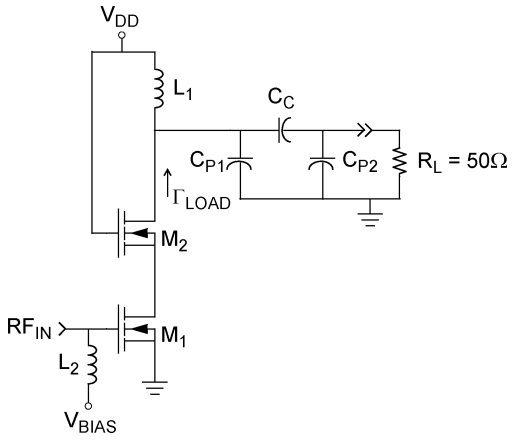

Fig. 4. PA output stage with its *LC* output matching network.

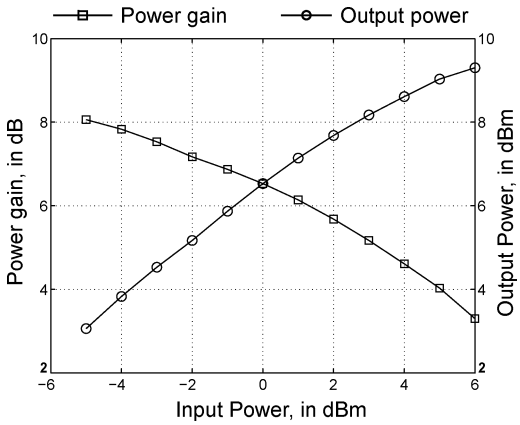

Fig. 5. Output power and gain of output stage from load-pull simulations.

but with additional inductors at the virtual ground to reject the common-mode interferences (see Fig. 3). Compared to a single-ended PA, the differential counterpart with 100 Ω source and load impedances (i.e., without input or output baluns) delivers approximately 3 dB more saturated output power and has a higher output-referred -1 dB compression point (i.e., $P_{\rm sat}$ and $P_{-1{\rm dBout}}$ in Table I), but occupies more than double the chip area (ignoring bondpads). In addition, the differential PA consumes 50% more DC power (i.e., $P_{\rm DC}$ in Table I) compared to its single-ended counterpart. Integration of a low-loss differential antenna is an additional design complication, whereas a power-combining output balun would reduce the output power which can be realized [20]. Single-ended PAs can directly feed a 50 Ω antenna without need for a balun or differential antenna, making them more cost-effective and easier to integrate.

Parasitics in the supply and ground paths can have an adverse effect upon the performance of a single-ended design. For example, a 10 pH inductor contributes about 4 Ω reactance at 60 GHz, which is comparable (in magnitude) to the optimal load for the PA output stage (i.e., in the range of 7–15 Ω). Amplifier degeneration caused by parasitics such as stray inductance would therefore reduce the power gain and power-added efficiency (PAE) of the PA. Also, ground bounce [22] caused by parasitic inductance in the ground path on-chip in a multistage amplifier may also cause instability. Therefore, the physical layout of the ground plane for single-ended amplifiers must reduce the unwanted ground inductance to an acceptable level.

B. Output Stage Design

The output stage is critical to the overall PA design, as the output power and design of the driver stages and key passive components depend upon this stage. Fig. 4 shows a simplified schematic of the output stage with its *LC* matching network. Due to nonlinear behavior of the active devices at the desired output power level, load-pull simulations [21] are used to determine the optimal load impedance. Output power versus load impedance contours obtained from load-pull simulations provide insight into how the load power changes as the load impedance varies.

Fig. 5 illustrates the output stage power transfer characteristic obtained from load-pull simulations. As a compromise between output power and gain, the amplifier output stage will be operated at a nominal input power between -1 dBm and 1 dBm. A power gain between 6.9 dB and 6.1 dB is therefore required. The optimal impedance for the load in this case is $13.27 + {\rm j}34.64\ \Omega$.

C. Millimeter-Wave Passive Components

Although the silicon substrate is lossy, passive elements with an acceptable quality factor (i.e., above 10 at 60 GHz) are still feasible. In the PA design, wide-gap CPW lines consisting of a first metal ground plane (M1 in Fig. 6) and topmetal M6 as the signal/topside-ground implement matching networks and resonant circuits. For isolation between adjacent lines, M6 ground strips on both sides of the signal line are used. The distance from signal to the topmetal ground (S) is much greater than the distance to the M1 ground plane (H). The wide gap (i.e., $S \gg H$) reduces the topmetal metal-to-metal parasitic capacitance and increases the signal line inductance, so that the M6 signal/M1 ground behaves like a simple microstrip transmission line. As shown in Fig. 6, topmetal ground lines are connected to the M1

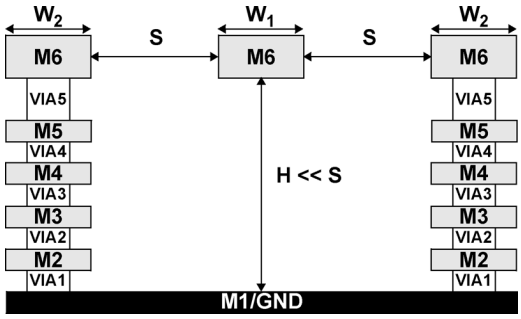

Fig. 6. Cross section of the wide-gap CPW with underlying ground plane.

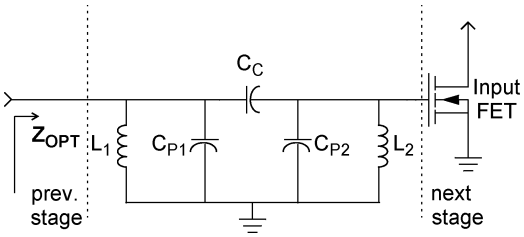

Fig. 7. Inter-stage matching network.

ground plane by numerous vias through the metal stack. This structure provides a well-defined ground plane and satisfies the metal pattern design rules for manufacturing.

Inductors may be implemented using a short-circuit transmission line, which is easier to model accurately and are therefore better suited to realize small inductance values at mm-wave frequencies than spiral inductors. The lossy silicon substrate has little effect on these transmission line inductors, as they are shielded from the underlying substrate by the bottom ground plane. An inductor with a Q-factor of approximately 10 can be realized in this way on-chip.

High-Q MIM capacitors are realized using M6 and M5 layers, which are separated by an intermetal dielectric with higher-k than the other interconnect metals, yielding a greater capacitance density. M1 is also used as a ground for the MIM capacitors in order to shield the bottom metal plate from the silicon substrate at the cost of a slight increase in bottom plate parasitic capacitance. The parasitic capacitances between M5 and M1 and between M6 and M1 are well-defined. To characterize the M6–M5 capacitors systematically, a capacitor unit cell with 10 μm perimeter was designed. M6 has slightly smaller area than M5 in the layout, to minimize the fringing field component. Due to the relatively low capacitance density, multiple unit cells are connected in parallel in order to realize the desired capacitance value [e.g., see Fig. 12(a)].

D. Matching Network Design

For the output matching network, the *LC* network of Fig. 4 was designed to transform the 50 Ω (antenna) load to the optimal impedance obtained from the load-pull simulation (i.e., $13.27 + \mathrm{j}34.64\,\Omega$). Optimization was used to choose the inductance and capacitance values that minimize the area required by all of the elements for the output, input and inter-stage matching

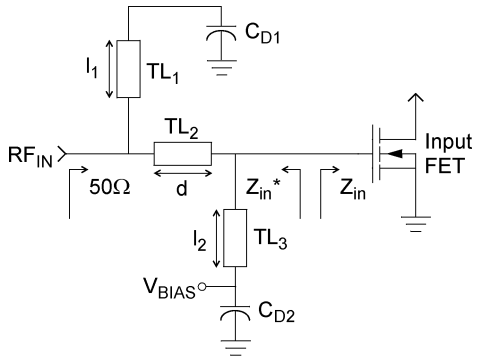

Fig. 8. Input double-stub matching network.

networks given the anticipated processing tolerances. For example, the parasitics of the M6-M5 MIM capacitors are connected so that the transmission lines required to implement the matching networks are as short in length as possible. This minimizes the total chip area required for the passive components with a given capacitor size.

The inter-stage matching network illustrated in Fig. 7 transforms the input impedance of the load stage to the desired optimal load for the driving stage. The inter-stage matching network configuration is topologically similar to the output-matching network, except that an additional inductor is added to bias the gate of the input transistor, as shown in Fig. 7.

For input matching, a double-stub network (see Fig. 8) was adopted. The advantage over a single stub design is the wider range of input impedances (i.e., $\mathrm{Z_{in}}$) that can be matched to 50 Ω. Both stubs (i.e., $\mathrm{TL_1}$ and $\mathrm{TL_3}$ in Fig. 8) are implemented using short-circuited microstrip transmission lines and the lengths of the three transmission lines in the pi-network ($\mathrm{l_1}$, d, and $\mathrm{l_2}$) are optimized in order to reduce the chip area required. Short-circuited stub $\mathrm{TL_3}$ (see Fig. 8) is closest to the first power stage and therefore can be used to DC bias the input transistor gate.

E. Multi-Stage PA Design

Fig. 9 shows a simplified schematic for the single-ended PA which consists of three identical cascode stages with resonant loads (note that parasitics of the MIM capacitors not indicated). All of the transistors are identical, using the minimum gate length of 90 nm and 40 fingers of 2 μm width. When operated at a current density of 0.2 mA/μm, the f_T, $f_{\max}$ and maximum transducer power gain $\mathrm{G_{max}}$ are 110 GHz, 280 GHz, and 8.2 dB (as predicted from simulation). Each stage is biased by an external current source; the bias current is a scaled replica of the current I_{BIAS} (see Fig. 9).

The double-stub input matching network was modelled by lumped elements for simulations. The lumped element models were extracted from characterization of passive test structures fabricated on a separate testchip. The supply and gate of cascode transistors are decoupled by 5 pF capacitors realized as a parallel-series combination of drain/source-shorted MOS transistor capacitors. To improve the quality of this short circuit at mm-wave frequencies, a 100 fF M5-M6 capacitor is used. Matching network transmission lines $\mathrm{TL_1}$ (and $\mathrm{TL_3}$) and $\mathrm{TL_{4-8}}$ are implemented with 250 μm and 200 μm lengths,

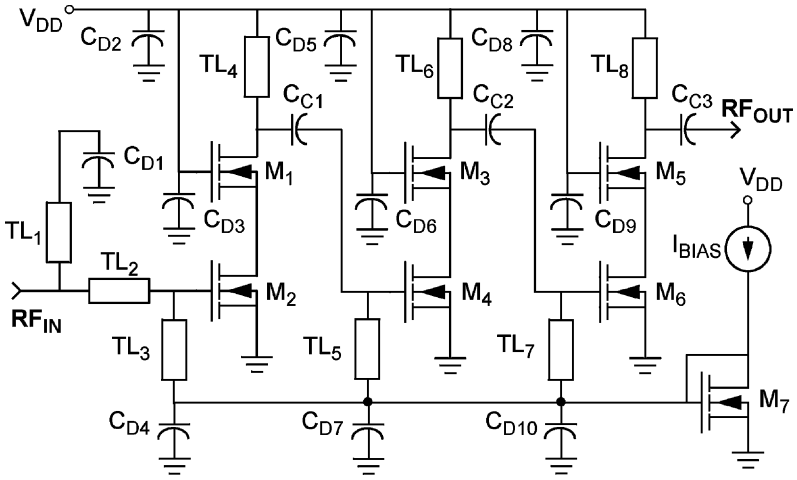

Fig. 9. Simplified schematic for the single-ended 3-stage cascode PA.

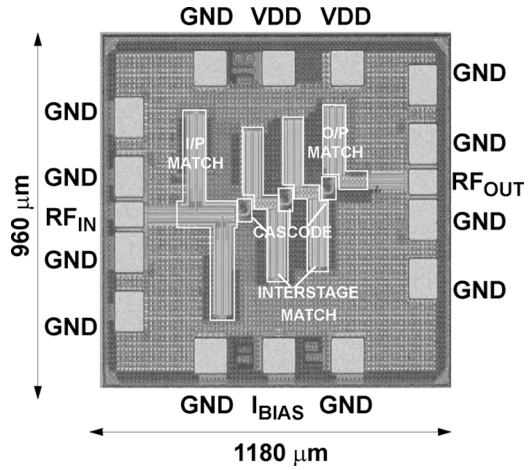

Fig. 10. Die photomicrograph.

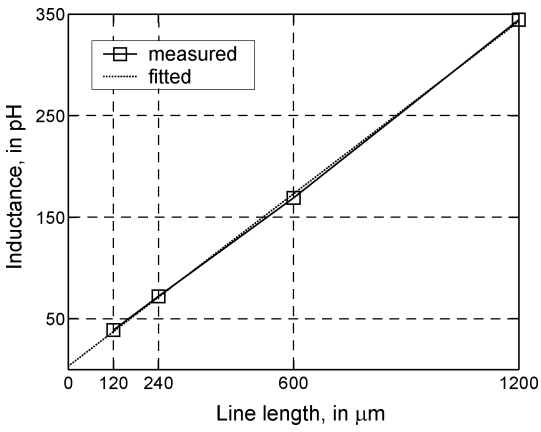

Fig. 11. Measured inductance of the wide-gap CPW (see Fig. 6) versus line length.

providing inductances of 71 pH and 56 pH, respectively. These lines are decoupled to ground by a parallel combination of 5 pF and 100 fF metal–metal capacitors (i.e, C_{D1-10}). Transmission line TL_2 (i.e., in the double-stub network) is 53 μm long.

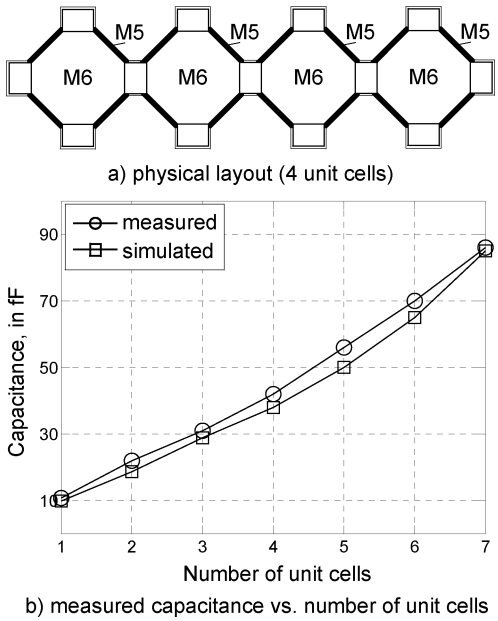

Fig. 12. M6–M5 metal-insulator-metal capacitors.

Capacitors C_{C1}/C_{C2}, and C_{C3} are realized by parallel MIM unit cells with capacitances of 57 fF and 87 fF, respectively.

III. Experimental Results

The PA was fabricated in a digital 90 nm CMOS technology (i.e., 21 Å thick gate oxide), with N-well and deep N-well [14] available for improved isolation between circuit blocks. The source and bulk of the MOS transistors may therefore be connected together in order to eliminate the body effect in both transistors of the cascode. The measured f_T and $f_{\max}$ for the transistors ($W = 80$ μm, $L = 100$ nm) at a current density of 0.2 mA/μm is 107 GHz and 180 GHz, respectively.

The total die area (including bondpads) is 1180×960 μm^2, as shown in the photomicrograph of Fig. 10. A ground-signal-ground pad configuration and microstrip interconnect lines are used at the input and output interfaces to the PA test circuit. The 80×110 μm^2 RF signal pads have a parasitic capacitance

TABLE II
WIDE-GAP CPW CHARACTERISTICS AT 60 GHz (SEE FIG. 6)

Parameter	Simulated	Measured
Characteristic impedance, in Ω	47.0	43.3
Quality factor	11.2	9.9
Loss, in dB/mm	0.88	1.10
Inductance, in pH/mm	282.3	281.8
Capacitance, in fF/mm	128.2	150.4
Resistance, in Ω/mm	9.55	17.32

of approximately 30 fF. An all-metal ground mesh ensures a low impedance on-chip to the ground terminals and substrate shielding, which minimizes unwanted effects such as ground bounce.

In the following sections, measurement results from characterization of the wide-gap CPW and M6-M5 MIM capacitor are summarized. Then, experiment results of the single-ended PA including S-parameters, and input-output power transfer characteristic are described.

Although the MIM capacitors and wide-gap CPW transmission lines were characterized prior to the design of this testchip, discrepancies between measurement and simulation for the overall PA performance were expected. A preliminary version of the 90 nm CMOS design kit for mixed-signal/RF applications was provided by the foundry with MOSFET model parameters that were extracted from measurements made at frequencies well below 60 GHz. In addition, n-well and deep n-well diffusions were added in order to increase isolation of the RF-MOS devices from other circuits, and the parasitics of these transistor layouts were not included in the model. Therefore, excellent agreement between experiment and simulation is not expected, although measures to improve the accuracy of the simulations (e.g., pre-characterization of the passives) were taken.

One of the objectives of this work is to benchmark the 90 nm CMOS technology and its design kit in a mm-wave application which could be used to motivate further improvements in the computer simulation models and identify potential problems in the design flow.

The inductance of the wide-gap CPW (refer to Fig. 6) versus transmission line length extracted from measurements of the dedicated passive test structures is plotted in Fig. 11. The dimensions of the 600 μm long transmission line used for characterization are: 7 μm wide M6 signal line (W_1), 12 μm wide M6 ground (W_2), and 19.5 μm topmetal spacing (S). Other parameters of the transmission line determined from 2-port S-parameter measurements are listed in Table II. The effect of pad parasitics on the measurement were de-embedded from the data using a test structure with a shorter length of transmission line, according to the method described in [23]. The inductance is directly proportional to the length (i.e., 281.8 pH/mm), as expected. The insertion loss measured at 60 GHz is 1.1 dB/mm, which is slightly larger than the 0.8 dB/mm predicted from simulation due to metal losses that are not accounted for in the simulation. Due to the same reason, the measured Q-factor at 60 GHz is 9.9, which is slightly smaller than the simulated result (i.e., 11.2).

M6–M5 MIM capacitor unit cells of about 10 fF are used to generate larger capacitance values needed for the decoupling and matching networks. As expected, the total capacitance and the parasitics to the M1 shield scale almost linearly with the number of cells [see Fig. 12(b)]. The discrepancy between the measurement and simulation is attributed to the effect of a global fill layer above M6 from a process option not used for the PA testchip. For fewer than 4 unit cells, both the measured and simulated capacitance scaled linearly with the number of cells in parallel. As the number of unit cells increases, however, fringing capacitance of the interconnections between the cells affects scalability. The measured capacitance density is approximately 0.1 fF/μm^2. Parasitic capacitances (i.e., M5–M1 and M6–M1) are approximately 30% and 10% of the M6–M5 capacitance, respectively. This difference in parasitic capacitance seen at each terminal of the MIM capacitor was accounted for in the matching network design. The capacitors are connected so that the transmission lines required to implement the matching networks are as short as possible, thereby minimizing the total chip area required by the passive components for a given capacitor size.

The PA measurements reported here are from on-wafer probing of first-pass silicon without de-embedding.

The measured small-signal gain $|S_{21}|$ (50 Ω load and source impedances) versus frequency is plotted in Fig. 13 for several supply voltages. The biasing mirror current was fixed as 20 mA for these measurements. For a 2 V supply, the peak power gain is 19.7 dB at 52.4 GHz, and drops to 10.3 dB at 60 GHz. The −3 dB bandwidth of the amplifier is 7.8 GHz (i.e., 48–55.8 GHz), while small-signal gain is greater than 10 dB over the range from 42.3–60.2 GHz. At 1.8 V and 1.5 V supply voltages, peak gain drops to 18.9 dB and 16.7 dB, respectively, while the −3 dB bandwidth increases slightly (to 8.0 GHz at 1.8 V and 8.2 GHz at 1.5 V). At the nominal digital CMOS supply voltage of 1.2 V, peak $|S_{21}|$ is 10.1 dB, which is 9.6 dB lower than the small-signal gain measured at 2 V. A drop in gain is expected as the supply decreases, as the drain-source bias voltage across the driver transistor in each cascode stage approaches the triode region. In all of these cases, the frequency for peak gain is approximately 52 GHz (±0.5 GHz variation seen as V_{DD} varies from 1.2–2 V).

The variation in peak gain (i.e., maximum $|S_{21}|$) at various bias settings (i.e., bias current and supply voltage) is plotted in Fig. 14. The bias current was varied from 15 to 20 mA at supply voltages of 1.5, 1.8, and 2 V. The peak $|S_{21}|$ increases by 0.4–0.6 dB as the bias current increases from 15 to 20 mA except at a 1.2 V supply, where the low voltage headroom in the

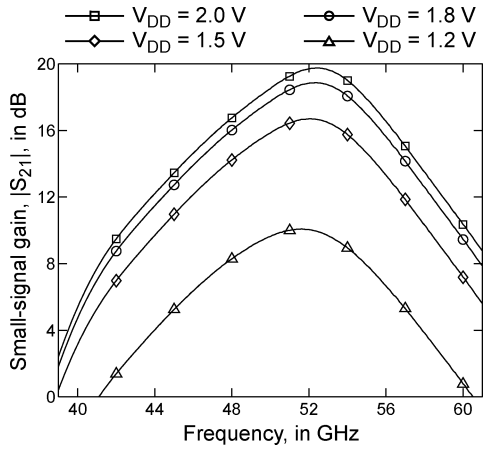

Fig. 13. Measured magnitude of small-signal forward gain, $|S_{21}|$, versus frequency at various supply voltages.

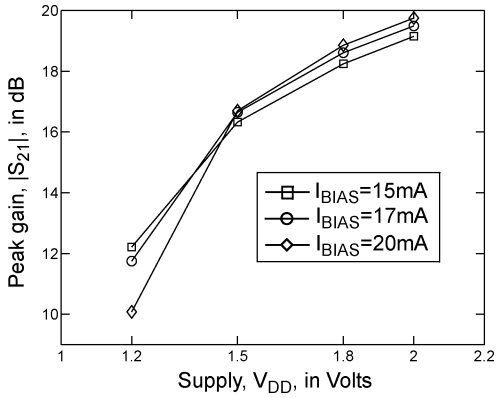

Fig. 14. Measured peak $|S_{21}|$ versus supply voltage for various bias currents.

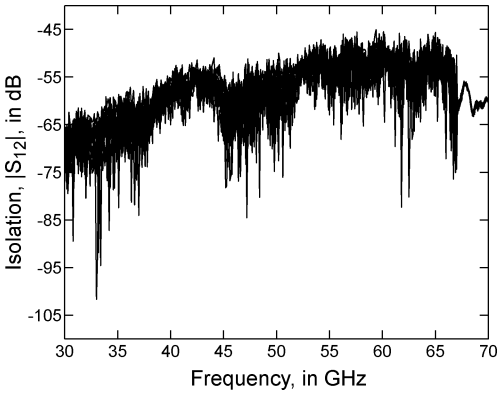

Fig. 15. Measured isolation, $|S_{12}|$, versus frequency.

cascode causes a decrease of more than 2 dB in peak $|S_{21}|$ when the bias current increases.

The small-signal isolation, $|S_{12}|$, of twelve different biasing conditions is shown in Fig. 15. The $|S_{12}|$ is below -45 dB from 30 to 70 GHz thanks to the 3 cascode stages.

The measured input and output reflection coefficients $|S_{11}|$ and $|S_{22}|$ versus frequency for V_{DD} of 1.5 V and 2 V and a fixed bias current of 20 mA are shown in Figs. 16 and 17, respectively. $|S_{11}|$ is below -6 dB across the band where the amplifier develops useful gain, and the in-band variation is ± 2 dB.

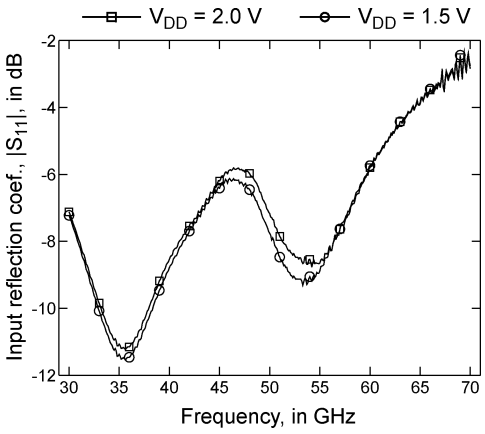

Fig. 16. Measured input reflection coefficient, $|S_{11}|$, versus frequency.

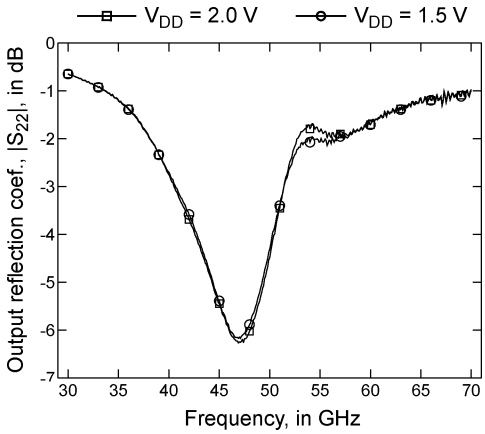

Fig. 17. Measured output reflection coefficient, $|S_{22}|$, versus frequency.

The $|S_{11}|$ is less than -10 dB after de-embedding the RF signal pad capacitance (i.e., $\sim$30 fF) and the 120 μm input transmission line, which were not accounted for in the PA design. The measured $|S_{22}|$ ranges from -6 to -2 dB in-band, however, it should be noted that the amplifier output impedance was designed for maximum power transfer (i.e., based on load-pull simulation) and not for a 50 Ω impedance match.

The swept power transfer curve of the amplifier (see Fig. 18) operating at 51.2 GHz shows a maximum output power of approximately $+8.2$ dBm. The measurement was limited by the maximum source power of -5.6 dBm available to drive the PA input from the test set-up. However, as seen from saturation of the output power curve of Fig. 18, only a slight increase in output power may be expected if the input were overdriven further. Peak PAE of 4.2% (including current consumption from driver stages and biasing current mirror) occurs at the maximum output power of 8.2 dBm, where 13.8 dB of power gain is realized. The measured -1 dB compression point (output-referred) is 3.1 dBm (-16 dBm RF input power), for a supply voltage of 2 V. The same amplifier operating from a 1.5 V supply produces a maximum saturated output power of $+4.5$ dBm.

As noted at the beginning of this section, discrepancies between measurement and simulation for the overall PA performance were expected. When compared to simulations, the measured small-signal power gain ($|S_{21}|$) is 5 dB lower. The

TABLE III
MM-WAVE PA COMPARISON FROM RECENT LITERATURE

Technology (Topology)	Freq in GHz	$\|S_{21}\|_{max}$ in dB	$P_{-1dBout}$ in dBm	G_{sat} in dB	P_{sat} in dBm	P_{DC} in mW (V_{DD})	PAE_{pk} in %
90nm CMOS (3-stage cascode) [this work]	51.2	19.5	3.1	13.8	+8.2	150 (2V)	4.2
90nm CMOS (3-stage CS) [24]	60	13.3	10.5	11.3	11.3	150 (1V)	8.2
90nm CMOS (2-stage diff.) [25]	60[1]	5.6	9	2.3	12.3	78[2] (1V)	8.8
90nm CMOS (4-stage CS) [26]	60	8.3	8.2	0.6	10.6	228.6 (1.2V)	2.4[3]
90nm CMOS (3-stage CS) [4]	61	5.2	6.4	0	9.3	39.75 (1.5V)	7.4
0.13μm SiGe (push-pull) [15]	60	18	13.1	4.5	20	248 (4V)	12.7

1. peak small-signal gain of 7.7dB occurs at 48GHz as indicated in [25].
2. determined from the data provided in [25].
3. inferred from power transfer curve shown in [26].

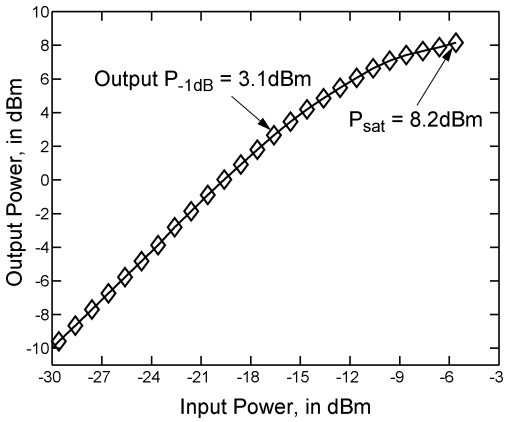

Fig. 18. Measured output versus input power transfer curve at 51.2 GHz.

frequency where the peak power gain occurs is 8 GHz lower than that predicted from simulations. These results indicate that the PA circuit is sensitive to layout parasitics present at critical nodes in the RF signal path. Parasitics present in the circuit layout that are not accurately captured in the transistor models or by parasitic extraction tools can cause substantial changes in the gain, frequency response and saturated output power. Further refinement of the active device model parameters is therefore required in order to improve the model accuracy, and proper extraction of capacitive parasitics from the physical layout is also necessary in order to account for their effects on the amplifier's behavior.

The performance of the PA presented in this paper is compared to state-of-the-art mm-wave PAs designed in both 90 nm CMOS and 0.13 mm SiGe-BiCMOS technologies (from the most recent literature) in Table III. Operating from a 2 V supply, the PA described in this work realizes greater small-signal and saturated output power gains (i.e., $|S_{21}|_{max}$ and power gain at maximum saturated output power, G_{sat}, in Table III) than the other CMOS mm-wave designs. The peak saturated output power is $+8.2$ dBm.

The relevant RF power output parameters (i.e., $P_{-1dBout}$, P_{sat} and PAE_{pk} in Table III) reported for some of the other PAs in [4] and [25] are higher than what is achieved by the PA developed in this work. However, it should be noted that all of the 60 GHz CMOS power amplifiers listed in the table are within approximately 2 dB (i.e., ± 2 dB) of $+10$ dBm maximum saturated output power (P_{sat}).

CMOS PAs [4], [26] listed in Table III do not develop their peak PAE at maximum output power. PAE is gain dependent, as it quantifies the ratio of power added to the signal by the amplifier to the DC power it consumes. Thus, amplifiers with low power gain G_{sat} add little power to the signal and suffer from a lower PAE at maximum output power. This is not the case for the amplifier developed in this work.

PA gain greater than 15 dB is desirable in order to compensate for losses in the upconversion chain of the transmitter. Extra driver stages that are required to increase gain consume additional DC power, thereby reducing the PAE. Thus, the efficiency of some of the other CMOS PAs listed in Table III will likely decrease by a few percent if extra stages were added in order to increase the overall gain to 15–20 dB.

The isolation of the power amplifier should be considered. One reason for choosing the cascode topology as a building block is its high isolation between output and input, which may be difficult to realize by other means at mm-wave frequencies. The inferior isolation inherent in a simple common-source (CS) CMOS gain stage may result in parasitic oscillation when a higher PA gain is selected for a 60 GHz integrated transceiver module, or undesired feedback from the antenna to the transmitter. For example, the isolation of the CS amplifier reported in [4] is 15 dB less than the PA presented in this work. On the other hand, the CS amplifiers listed in Table III (e.g., [24]) offer similar levels of saturated output power at a supply voltage on the order of 1 V, rather than the 2 V supply used for the cascode PA. Thus, cascode pre-driver stages connected to a CS output stage may offer a reasonable compromise between gain, isolation and output power for a mm-wave CMOS PA.

The SiGe-based PA as described in [15] is also included for completeness. With the higher voltage swing available from a SiGe-bipolar transistor, the SiGe-PA outperforms all of the CMOS designs reported to date for almost all performance specifications. However, integration of a 60 GHz transceiver including the PA will likely use bulk CMOS as the technology platform as previously discussed in Section I of this paper, and its operating range (i.e., span of the radio link) will therefore be constrained by the relatively low transmit power available from a deep submicron CMOS PA.

IV. Conclusion

A CMOS mm-wave power amplifier, with close to 20 dB linear power gain and +8 dBm saturated output power was presented. The single-ended PA consists of three identical cascode stages, which provide in-band isolation better than 45 dB between output and input, and on-chip matching networks (interstage, input and output) implemented by coplanar waveguides (wide-gap CPW) and M6-M5 (MIM) capacitors. The (small-signal) −3 dB bandwidth is 48 to 55.8 GHz, with a peak gain of 19.7 dB at 52.4 GHz, and 10.5 dB gain at 60 GHz. The −1 dB compression point (output-referred) is 3.1 dBm. The peak, measured PAE of 4.2% occurs at an output power of 8.2 dBm, where 13.8 dB of power gain is realized. The $1.18 \times 0.96\ \text{mm}^2$ die consumes 75 mA from a 2 V supply when operating at full output power. The results obtained for this mm-wave PA prototype do not completely agree with the predictions of simulation, indicating that further refinement of active device model parameters and proper extraction of capacitive parasitics from the physical layout in order to realize a robust design. However, it is clear from examination of these results (and others reported in the recent literature for mm-wave CMOS PAs) that deep-submicron CMOS can supply the 10 dBm output power at 60 GHz required by the IEEE 802.15.3c wireless networking standard.

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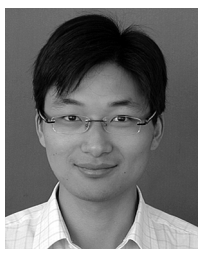

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