In Situ Annealing of Boron-Doped Amorphous Silicon Layers Using APCVD Technology

Kuruganti, Vaibhav V.; Mazurov, Alexander; Seren, Sven; Isabella, Olindo; Mihailetchi, Valentin D.

DOI
10.1109/JPHOTOV.2023.3323788

Publication date
2023

Document Version
Final published version

Published in
IEEE Journal of Photovoltaics

In Situ Annealing of Boron-Doped Amorphous Silicon Layers Using APCVD Technology

Vaibhav V. Kuruganti, Alexander Mazurov, Sven Seren, Olindo Isabella, and Valentin D. Mihailetchi

***Abstract*—In this work, we developed an in situ annealing process to crystallize boron-doped amorphous silicon [a-Si(p^+)] layers deposited by atmospheric pressure chemical vapour deposition (APCVD) to form boron-doped polycrystalline silicon [poly-Si(p^+)] layers. The influence of the temperature profiles during a-Si(p^+) in-line deposition on structural, electrical, and passivation properties was studied in detail. The results show that a-Si(p^+) layers can be successfully crystallized by fine-tuning the temperature profiles in the postdeposition zones of the APCVD tool. It was observed that the hydrogenation processes during the fast firing play a significant role in enhancing the passivation quality as well as the electrical properties of the in situ annealed poly-Si(p^+) layers. The sheet resistance (R_{sh}) and implied open circuit voltage (iV_{oc}) of the best in situ annealed poly-Si(p^+) layers were found to be comparable to the ones that were ex situ annealed in the tube furnace at 950 °C for 30 min. The sheet resistance of 200 Ω/□ could be obtained on 150-nm thick poly-Si(p^+) layers with an (iV_{oc}) of 718 mV. The use of this novel in situ annealing process to form poly-Si(p^+) layers opens a new horizon for a lean process sequence without the additional high-temperature annealing step for fabricating solar cells concepts based on passivating contact.**

***Index Terms*—Atmospheric pressure chemical vapour deposition (APCVD) technology, annealing, polysilicon, tunnel oxide passivated contacts (TOPCon).**

I. Introduction

TUNNEL oxide passivated contacts (TOPCon) solar cells [1] are a promising technology for the next generation of c-Si solar cells. The TOPCon design is based on the principle of separating the carrier extraction zone from the carrier generation zone using a thin interfacial silicon dioxide layer and highly doped polycrystalline silicon (SiO_2/poly-Si) layer [2]. One of the major advantage of this solar cell concept over the conventional passivated emitter and rear cells (PERC) technology is the reduced recombination losses, especially at the metal–semiconductor interface [3]. These passivated contact solar cells are touted as the next technological upgrade for PERC manufacture as they require only a few changes to the current cell process flow, making them an attractive upgrade option [4]. The potential of this technology has been well-demonstrated in research laboratories, achieving a conversion efficiency of 26.1% on interdigitated back contact cells (IBC) [5] and 26.4% on front and rear contact solar cells [6]. In addition, the industrial adoption of this technology by PV manufacturers has shown promising results [7], [8].

The intended industrial TOPCon process routes consist of process steps that are either entirely or partially transferable from the PERC cell, along with a few additional process steps such formation of tunnel oxide and deposition of intrinsic/doped amorphous silicon layers that are required to increase the conversion efficiency [3]. The tunnel oxide layer can be deposited by thermal oxidation, ozone oxidation, chemical oxidation or plasma-enhanced chemical vapour deposition (PECVD) techniques [9], though in industry thermal oxide is preferred due to its higher thermal stability and structural integrity [10]. The intrinsic/doped silicon layers can be deposited by sputtering [11], low-pressure chemical vapor deposition (LPCVD) [12], atmospheric pressure chemical vapour deposition (APCVD) [13] or PECVD technique [14]. Currently, the industry is transitioning from LPCVD to PECVD technology due to its high deposition rates, single-sided depositions, lower thermal budget, and lower equipment and maintenance costs [15]. Irrespective of the deposition technology, all the intrinsic/doped amorphous silicon layers need a high-temperature annealing step, either combined in the diffusion step in case of ex situ doping of poly-Si layers [16] or a separate annealing step at temperatures of 800 °C –1000 °C, with dwell times typically in the range of 10–30 min in case of in situ doping of poly-Si layers [17]. During the high-temperature annealing step, the deposited amorphous silicon layer crystallizes to form a polycrystalline silicon layer [18], and dopants get activated and homogeneously distributed in the poly-Si layer [19]. Studies have shown that during the high-temperature annealing step, the passivation quality of the

Manuscript received 12 August 2023; revised 25 September 2023; accepted 29 September 2023. Date of publication 23 October 2023; date of current version 18 December 2023. This work was supported by the German Federal Ministry for Economic Affairs and Climate Action (BMWK) through the HoBIT project under Grant 03EE1121B. *(Corresponding author: Vaibhav V. Kuruganti.)*

Vaibhav V. Kuruganti is with the International Solar Energy Research Center (ISC) Konstanz, D-78467 Konstanz, Germany, and also with the Photovoltaic Materials and Devices Group, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: vaibhav.kuruganti@isc-konstanz.de).

Alexander Mazurov and Sven Seren are with SCHMID Group, 72250 Freudenstadt, Germany (e-mail: mazurov.al@schmid-group.com; Seren.Sv@schmid-group.com).

Olindo Isabella is with the Photovoltaic Materials and Devices Group, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: o.isabella@tudelft.nl).

Valentin D. Mihailetchi is with the International Solar Energy Research Center (ISC) Konstanz, D-78467 Konstanz, Germany (e-mail: valentin.mihailetchi@isc-konstanz.de).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JPHOTOV.2023.3323788.

Digital Object Identifier 10.1109/JPHOTOV.2023.3323788

layer stack is improved due to interfacial oxide restructuring [20] and the formation of subnanometer pits through the interfacial oxide [21].

Though the high-temperature annealing step is found to be benevolent in many ways, it does increase the overall thermal budget of the process sequence thereby increasing the levelized cost of electricity (LCOE) of TOPCon solar cells in comparison to PERC solar cells [3]. Driessen et al. [22] have presented streamlined processing of TOPCon solar cells by reducing the number of high-temperature process steps, using simultaneous boron emitter diffusion and annealing of tunnel oxide passivated contacts via rapid vapour-phase direct doping. Similar work was also presented by Du et al. [23], where front emitter and rear passivating contacts via continuous PECVD deposition were concurrently prepared in a single high-temperature step. Arpan et al. [24] have shown that rapid thermal annealing (RTA) can be used for annealing purposes in a-Si(p^+) layers. RTA has the fundamental advantage of a short period of annealing time as compared to tube-furnace annealing. Alternatively, Ingenito et al. [25] have demonstrated an innovative fired silicon-based heterojunction (FlaSH) contact formed by a tunnel silicon oxide (SiO_2) capped with a doped silicon-based layer in which the long and slow thermal postannealing is replaced by a quick fast-firing treatment. In this article, we present a new and novel way to anneal amorphous silicon layers using APCVD technology. This method is called "in situ annealing," where the layer is annealed in the APCVD tool during deposition, thereby avoiding additional high-temperature steps. Solar cell architectures such as rear junction TOPCon (RJ-TOPCon) [26] or fully passivated IBC solar cells [27] can be fabricated in a cost-effective way using the APCVD in situ annealed poly-Si(p^+) layers.

II. Experimental Details

A. Sample Preparation for XRD Measurements

We use 100 Ω·cm phosphorous-doped n-type polished 5-inch Fz wafers with a thickness of 250 μm. After the standard piranha cleaning, the samples are coated with a 75-nm thick PECVD SiN_x layer on both sides. The a-Si(p^+) layers with the three different temperature profiles (T1, T2, and T3) are deposited symmetrically on both sides using the SCHMID APCVD equipment. The as-deposited APCVD layers without any subsequent high-temperature step are referred to as in situ annealed samples in this work. Post APCVD layer deposition, half of the samples undergo an additional high-temperature annealing step in a quartz tube furnace at a temperature of 950 °C for 30 min and are referred to as ex situ annealed samples. The native oxide on poly-Si(p^+) is removed in HF solution before performing the XRD measurements. The XRD measurements were performed on the Rigaku D/MAX X-ray diffractometer in the θ - 2θ mode with a CuK α source ($\lambda = 1.5418$ A°).

B. Sample Preparation for Sheet Resistance (R_{sh}) and Lifetime (LT) Measurements

Fig. 1 indicates the schematic fabrication process of the *LT* and R_{sh} samples. We use 30 Ω·cm phosphorous-doped n-type Cz c-Si M6 format substrate wafers with a thickness of 180 μm. The samples are saw-damage etched in alkaline NaOH solution followed by Pirahna cleaning to remove the saw-cutting-induced damages and organic and inorganic impurities, respectively. To obtain a 1.6-nm thick interfacial SiO_2 layer, dry thermal oxidation is performed in a quartz tube furnace at a temperature of 600 °C for 10 min in a 100% oxygen environment followed by 15 min of annealing in a 100% nitrogen environment. The in situ doped poly-Si(p^+) layer is deposited using the SCHMID APCVD system. The thickness of the layers and the dopant concentrations can be controlled by adjusting the temperature, gas flows, and belt speed. The APCVD in situ doped poly-Si(p^+) layer's process parameters are tabulated in Table I. In order to perform in situ annealing of the a-Si(p^+) layers during the deposition, three different temperature profiles (T1, T2, and T3) are chosen, while the gas flow rates and belt speeds are kept constant in all the recipes. Similar to XRD measurement samples, half of the samples from each temperature profile group are externally annealed in a quartz tube furnace at a temperature of 950 °C for 30 min, i.e., ex situ annealed samples. The native oxide grown on the poly-Si layers during the APCVD deposition and external annealing is removed in an HF solution to measure the electrical properties of the poly-Si(p^+) layers. The sheet

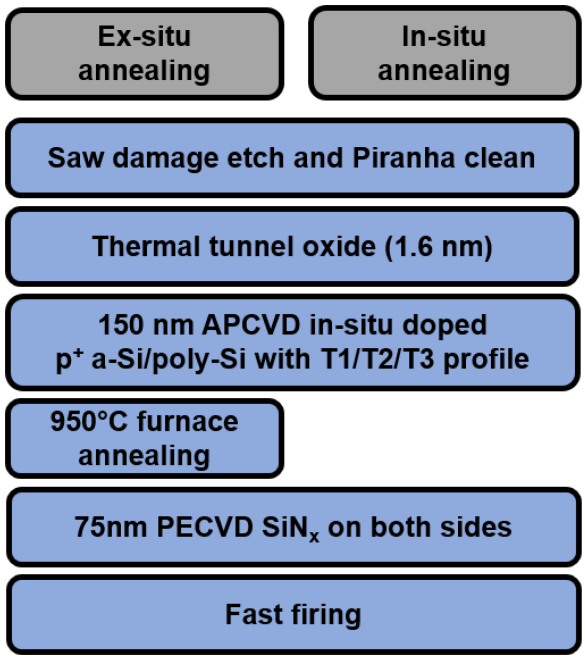

Fig. 1. Simplified process sequence for the sheet resistance and lifetime measurement samples.

TABLE I
APCVD Deposition Parameters Used in This Study

Process parameter	Input
B_2H_6 flow	48 sccm
SiH_4 flow	120 sccm
Deposition belt speed	12 ipm
Temperature in deposition zone	695°C
Overall deposition time	12 min

resistance is measured using the four-point probe tool from GP Solar.

The process sequence of the symmetrical lifetime samples is similar to that of the abovementioned R_{sh} samples until the removal of the native oxide after annealing, except that the APCVD poly-Si(p^+) layers are deposited on both sides of the wafer. Subsequently, the samples receive a 75-nm thick PECVD SiN_x layer. The hydrogenation of these samples is done using a Centrotherm fast-firing furnace with a peak set temperature of 820 °C and at the belt speed of 3 m/min. For measuring the (iV_{oc}) of the poly-Si(p^+) layers, we used a WCT-120 lifetime tester from Sinton Instruments. For the QSSPC measurements, we used wafers with a base resistivity of $\rho_B = 30\ \Omega$·cm and thickness t of 165 μm. For the flat passivated symmetrical lifetime samples, an optical constant of 0.95 was selected.

III. Results and Discussion

The APCVD equipment used in this study is a SCHMID belt transport system with multiple deposition chambers. The injector head consists of a line source with a separated supply of (SiH_4, B_2H_6, and N_2). The N_2 gas flow in the deposition chamber assures an atmosphere with minimal oxygen (O_2) content. The fundamental principle governing the APCVD silicon layer depositions relies on the fact that thermally dissociated SiH_4 in the deposition chamber would precipitate as an amorphous silicon layer on the hot moving substrate [13]. The belt transport system APCVD system can be categorized into three main zones, namely: predeposition zones, deposition zones, and postdeposition zones. A systematic study was carried out to understand the influence of each zone on the crystallinity of the as-deposited silicon layers, with the results showing that the postdeposition zone temperature profile is the main parameter that influences layer crystallinity. Using this knowledge, in this study, three temperature profiles (T1, T2, and T3) for the layer deposition were shortlisted, in which the predeposition temperature profiles were kept constant and the postdeposition temperature profiles were altered keeping the belt speed constant at 12 ipm and are depicted in Fig. 2.

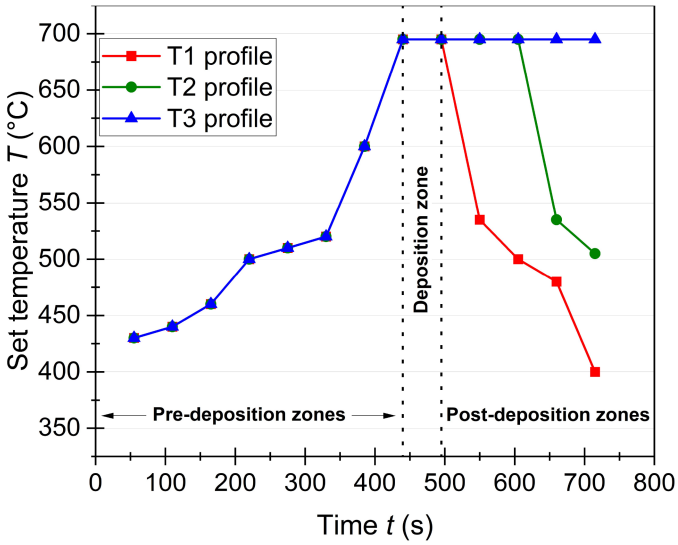

Fig. 2. T1, T2, and T3 temperature profiles (see legend) of APCVD poly-Si(p^+) layers studied in this work. The set temperature in pre-deposition and deposition zones was kept constant while only the postdeposition set temperature was varied in the T1, T2, and T3 temperature profiles.

A. Crystallization Assessment by XRD Measurements

To study the crystal structure of a-Si/poly-Si(p^+) layers, X-ray diffraction (XRD) has been performed in a θ - 2θ configuration, using the CuK α radiation. All measurements were performed with 2θ values between 20° and 50° in a continuous mode of 5° per min with a step size of 0.02° on an X-ray tube operating at 40 kV and 30 mA. In Fig. 3, the XRD pattern of in situ annealed APCVD silicon films deposited using the different temperature profiles (T1, T2, and T3) is presented alongside an ex situ annealed APCVD silicon films deposited at the T3 temperature profile and background pattern coming from the bare Fz wafer with SiN_x. There are two major peaks observed on the bare substrate Fz wafers with SiN_x at 2θ values of 33·06° and 47·74°, which correspond to (200) and (220) silicon crystallographic planes, respectively [28]. The XRD pattern after the APCVD layer deposition and annealing (in situ/ex situ) in most cases, shows three dominant peaks at 2θ values of

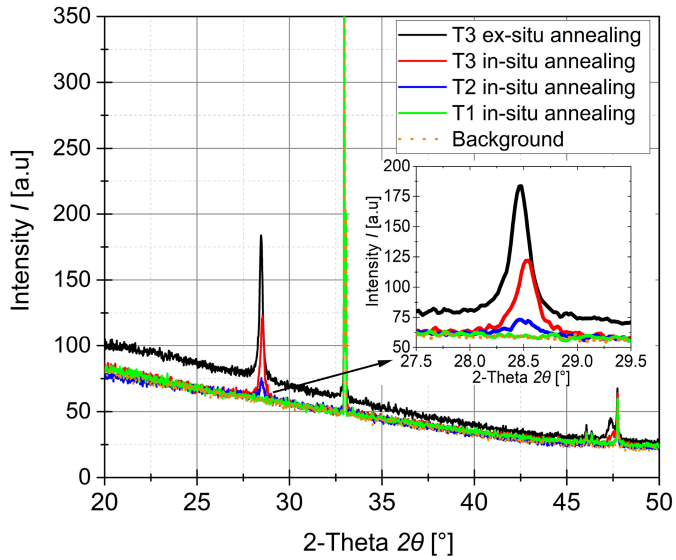

Fig. 3. XRD spectra of in situ and ex situ (see legend) annealed poly-Si(p^+) layers deposited with T1, T2, and T3 temperature profiles alongside the background measurements on bare Fz wafer.

28·4°, 33·0°, and 47·7°, which correspond to (111), (200), and (220) silicon crystallographic planes, respectively. The annealed APCVD layers tend to show a (111) preferential orientation attributed to the anisotropic crystallization [29]. This additional peak at 28·4° 2θ was observed for T3 ex situ annealing APCVD layers, T3 in situ annealing APCVD layers, T2 in situ annealing APCVD layers with decreasing order of the peak intensity owing to its decreasing crystallinity order [30]. In the case of T1, in situ annealed APCVD layers, we do not observe any peak at 28·4° 2θ and the overall profile resembles that of the background, proving that the T1 in situ annealed APCVD layers are amorphous in

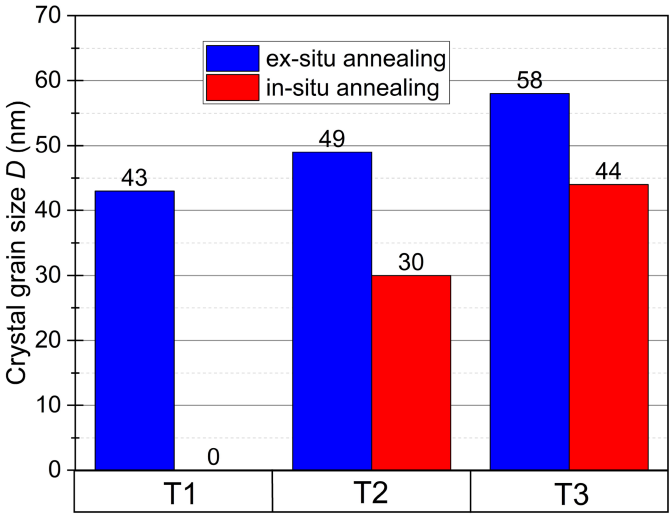

Fig. 4. Particle of in situ and ex situ (see legend) annealed poly-Si(p^+) layers as a function of deposition temperature profiles T1, T2, and T3, respectively.

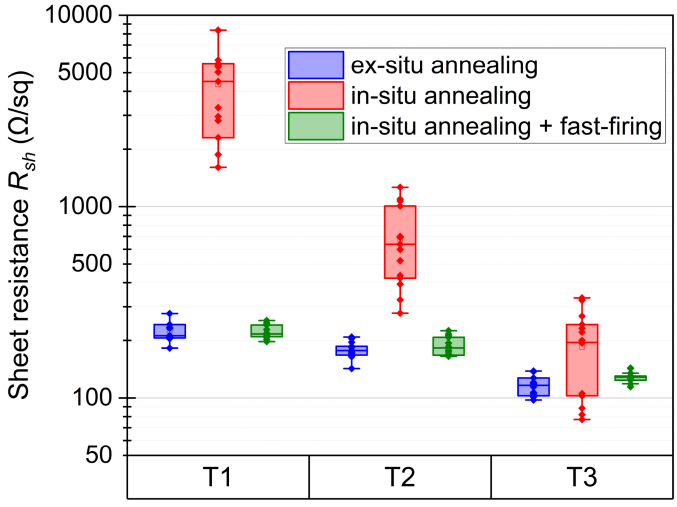

Fig. 5. Sheet resistance (R_{sh}) of in situ and ex situ annealed poly-Si(p^+) layers and in situ annealed poly-Si(p^+) layers after fast-firing (see legend) as a function of deposition temperature profiles T1, T2, and T3, respectively.

nature and the overall thermal budget of the T1 profile was not sufficient to crystallize the APCVD amorphous silicon layers.

From the full width at half maximum (FWHM) of the XRD peaks and the wavelength of the X-Ray, the crystallite grain size can be determined using the Debye Scherrer equation [31]. The calculated crystallite grain size from the in situ and ex situ annealed APCVD layers deposited at T1, T2, and T3 temperature profiles are depicted in Fig. 4. In the case of ex situ annealed APCVD poly-Si layers, due to the additional annealing, we observe a formation of crystal sizes in the range of 43–58 nm for the deposition temperature profiles T1 and T3, respectively. In the case of in situ annealing of APCVD silicon layers, the T1 temperature profile remains amorphous, whereas for the T2 and T3 temperature profiles, a detectable crystal size from 30 to 44 nm was observed, respectively. The enhanced crystallization of the T3 temperature profile is due to the higher thermal budget in the postdeposition zones.

B. Electrical Properties of the Polysilicon Layers

As described in the experimental section, sheet resistance samples were used to study the electrical properties of the poly-Si(p^+) layers. Fig. 5 depicts the R_{sh} data of in situ annealed poly-Si(p^+) layer, ex situ annealed poly-Si(p^+) layer and in situ annealed poly-Si(p^+) layer after fast-firing as a function of the APCVD layer's deposition temperature profiles. Since the R_{sh} values of the ex situ annealed poly-Si(p^+) layer upon fast firing does not change, they were not presented in Fig. 5. The additional extensive annealing in the quartz tube furnace for 30 min at 950 °C for the ex situ annealed layers leads to better crystallization and dopant activation yielding high-conductive and homogeneous layers in comparison to in situ annealed layers [16].

Progressing from T1 to T3 temperature profiles, the overall thermal budget during the deposition increases and it strongly influences the in situ annealed layers (prior to fast-firing) when compared to ex situ annealed layers. We obtain highly nonconductive layers with mean R_{sh} of 4000 Ω/□ at the T1 temperature profile to very conductive 195 Ω/□ layers with the T3 temperature profile in the case of in situ annealed layers. The substantial decrease in the R_{sh} in order of magnitude explains the influence of the temperature in the postdeposition zones of the APCVD system on the deposited layer's crystallinity and electrical properties. The higher mean R_{sh} values and higher standard deviation of the in situ annealed poly-Si(p^+) over the ex situ annealed poly-Si(p^+) layer deposited with the T3 temperature profile can be explained by its lower crystallinity, as also observed from the XRD peaks at 28·4° 2θ in Fig. 3. The crystallinity of this in situ annealed poly-Si (p^+) layers can further be enhanced by increasing the thermal budget in the postdeposition zones by either increasing the set temperature values in the postdeposition zones or by increasing the total number of postdeposition zones.

Interestingly, the difference in the conductivity and homogeneity of the in situ annealed poly-Si(p^+) layer and ex situ annealed poly-Si(p^+) layer diminishes upon fast-firing. The observed phenomenon implies that the thermal budget used in the fast-firing was sufficient for the dopant activation and crystallization of the in situ annealed poly-Si(p^+) layer. This significant improvement in the in-situ annealed poly-Si(p^+) layer's conductivity is speculated to be due to higher peak set temperature (820 °C) during fast-firing as compared to the set temperature in the APCVD deposition zone (695 °C).

C. Passivation Study on the Symmetrical Lifetime Samples

As described in the experimental section, symmetrical lifetime samples were used to study the passivation quality of the poly-Si(p^+) layers. Fig. 6 compares the measured iV_{oc} of the samples with in situ and ex situ annealing and their influence on fast firing as a function of the APCVD deposition temperature profiles T1, T2, and T3, respectively. Regardless of the temperature profile, very low iV_{oc} values of 610–645 mV are

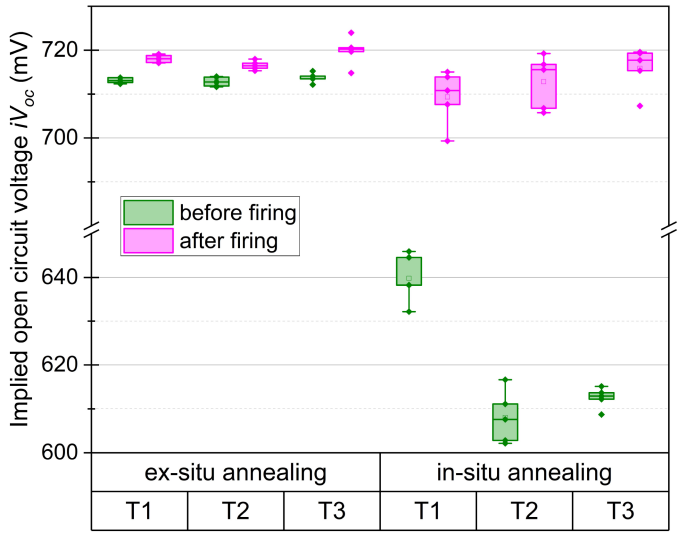

Fig. 6. Implied open circuit voltage (iV_{oc}) of in situ and ex situ annealed poly-Si(p^+) layers before and after fast firing as a function of deposition temperature profiles T1, T2, and T3, respectively.

observed for all in situ annealed samples prior to fast-firing, whereas samples with ex situ annealing exhibit much superior passivation quality with iV_{oc} value in the range of 710–715 mV. The difference in the passivation quality prior to fast-firing is speculated to be due to the additional high-temperature step at 950 °C for 30 min in the case of ex situ annealed poly-Si layers. It was demonstrated in Liu et al. [20] and Peibst et al. [21] that during the high-temperature annealing step, the chemical passivation quality is enhanced due to interfacial oxide restructuring thereby reducing acceptor-like state density and the formation of subnanometer pits on the interfacial oxide improves the field-effect passivation. Interestingly, after firing, there is a substantial increase in the passivation quality of the in situ annealed poly-Si(p^+) layers in comparison to the ex situ annealed poly-Si layers. This enhancement of the passivation quality is expected to be attributed to the hydrogen effusion from the in situ annealed poly-Si(p^+) layer and the SiN_x layer in passivating defects at the c-Si/SiO_2 interface [32] during the firing process, as also observed in the fired passivating contacts [25]. Consequently, we obtained the same passivation quality with iV_{oc} of 715–720 mV after fast-firing for both in situ and ex situ annealed poly-Si layers deposited with T3 temperature profiles.

In this work, we have demonstrated excellent passivation and electrical properties of in situ annealed poly-Si(p^+) layers. The in situ annealing concept described here for boron-doped poly-Si (p^+) layers can also be applied to phosphorous-doped poly-Si(n^+) layers. The diffusion/annealing and metallization represent a significant fraction of TOPCon solar cell production costs [3]. By using the novel in situ annealing of poly-Si layers using APCVD technology, the additional high-temperature annealing step currently used in industry for crystallization of amorphous layer and dopant activation [18] can be omitted from the process sequence thereby lowering the production costs and simplifying the process sequence of the solar cells concepts based on passivating contact.

IV. Summary

APCVD technology can be used to perform in situ annealing on boron-doped amorphous Si layers to obtain highly conductive and crystallized poly-Si with good passivation quality. The temperature profile in the postdeposition heat zones of the SCHMID APCVD system was found to be the most important parameter of the in situ annealing process. In this work, three different deposition temperature profiles were studied. The in situ/ex situ annealed APCVD layers showed a (111) preferential silicon crystallographic orientation with increasing peak intensity owing to its increasing crystallinity order progressing from T1 to T3 deposition temperature profiles. Similar to the structural properties, the sheet resistance measurements show an increase in conductivity when progressing from T1 to T3. It was also observed that fast-firing plays a vital role in enhancing the conductivity of the in situ annealing poly-Si layers. The reason for the observed phenomenon is speculated due to the higher set temperature during fast-firing (820 °C) as compared to that of the APCVD deposition temperature (695 °C). In conclusion, both in situ and ex situ, annealed poly-Si layers deposited with a T3 temperature profile yield comparable crystal sizes and sheet resistance values.

Prior to fast-firing, the in situ annealed poly-Si(p^+) layers exhibited poor passivation quality but postfast-firing both in-situ and ex situ annealed poly-Si layers exhibit excellent passivation quality with an iV_{oc} of 715–720 mV. This enhancement in the passivation quality especially for in situ annealed poly-Si(p^+) layers post fast-firing is expected to be attributed to the hydrogen diffusion from the poly-Si(p^+)layer and the SiN_x layer in passivating defects at the c-Si/SiO_x interface. In conclusion, we have demonstrated a novel method for annealing amorphous silicon layers during layer deposition with comparable structural, electrical, and passivation quality to that of ex situ annealing of poly-Si silicon layers in a quartz tube furnace at 950 °C for 30 min. These in situ annealed layers deposited with APCVD technology can be used for lean process sequence and cost-effective way for fabricating solar cell concepts like RJ-TOPCon and fully passivated IBC solar cell.

References

[1] F. Feldmann, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics," *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 270–274, 2014.
[2] S. W. Glunz and F. Feldmann, "Sio2 surface passivation layers–a key technology for silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 185, pp. 260–269, 2018.
[3] B. Kafle et al., "Topcon–technology options for cost efficient industrial manufacturing," *Sol. Energy Mater. Sol. Cells*, vol. 227, 2021, Art. no. 111100.
[4] H. Ullah et al., "Crystalline silicon (c-Si)-based tunnel oxide passivated contact (topcon) solar cells: A review," *Energies*, vol. 16, no. 2, 2023, Art. no. 715.
[5] C. Hollemann et al., "Separating the two polarities of the polo contacts of an 26.1%-efficient IBC solar cell," *Sci. Rep.*, vol. 10, no. 1, pp. 1–15, 2020.
[6] Vincent, "Chinese pv industry brief: Jinkosolar achieves 26.4% efficiency for n-type topcon solar cell," pv magazine. [Online]. Available: https://www.pv-magazine.com/2022/12/09/

[7] D. Chen et al., "24.58% total area efficiency of screen-printed, large area industrial silicon solar cells with the tunnel oxide passivated contacts (i-topcon) design," *Sol. Energy Mater. Sol. Cells*, vol. 206, 2020, Art. no. 110258.
[8] J. Bao et al., "Towards 24% efficiency for industrial n-type bifacial passivating-contact solar cells with homogeneous emitter," in *Proc. 37th Eur. Photovolt. Conf. WIP*, 2020, pp. 160–163.
[9] H. Yousuf et al., "Tunnel oxide deposition techniques and their parametric influence on nano-scaled Siox layer of topcon solar cell: A review," *Energies*, vol. 15, no. 15, Art. no. 5753, 2022.
[10] A. Moldovan et al., "Tunnel oxide passivated carrier-selective contacts based on ultra-thin Sio2 layers grown by photo-oxidation or wet-chemical oxidation in ozonized water," in *Proc. IEEE 42nd Photovolt. Specialist Conf.*, 2015, pp. 1–6.
[11] J. Hoß et al., "Sputtering of silicon thin films for passivated contacts," in *Proc. AIP Conf. Proc.*, vol. 2147, no. 1. AIP Publishing, 2019, pp. 040007-1–040007-5.
[12] F. Haase et al., "Laser contact openings for local poly-si-metal contacts enabling 26.1%-efficient polo-IBC solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 186, pp. 184–193, 2018.
[13] A. Merkle et al., "Atmospheric pressure chemical vapor deposition of in-situ doped amorphous silicon layers for passivating contacts," in *Proc. 35th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2018, pp. 785–791.
[14] B. Steinhauser, J.-I. Polzin, F. Feldmann, M. Hermle, and S. W. Glunz, "Excellent surface passivation quality on crystalline silicon using industrial-scale direct-plasma topcon deposition technology," *Sol. RRL*, vol. 2, no. 7, 2018, Art. no. 1800068.
[15] F. Feldmann et al., "Large area topcon cells realized by a PECVD tube process," in *Proc. 36th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2019, pp. 304–308.
[16] X. Yan et al., "Process development and integration of double-side poly-Si passivated solar cells with printed contacts via LPCVD and ex-situ tube diffusion," *Sol. Energy Mater. Sol. Cells*, vol. 230, 2021, Art. no. 111249.
[17] M. Fırat et al., "Large-area bifacial n-TOPCon solar cells with in situ phosphorus-doped LPCVD poly-Si passivating contacts," *Sol. Energy Mater. Sol. Cells*, vol. 236, 2022, Art. no. 111544.
[18] G. Marcins et al., "Crystallization processes of amorphous Si by thermal annealing and pulsed laser processing," in *Proc. IOP Conf. Series, Mater. Sci. Eng.*, vol. 23, no. 1. IOP Publishing, 2011, Art. no. 012035.
[19] R. C. Germanicus et al., "Dopant activity for highly in-situ doped polycrystalline silicon: Hall, XRD, scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM)," *Nano Exp.*, vol. 2, no. 1, 2021, Art. no. 010037.
[20] W. Liu et al., "Polysilicon passivating contacts for silicon solar cells: Interface passivation and carrier transport mechanism," *ACS Appl. Energy Mater.*, vol. 2, no. 7, pp. 4609–4617, 2019.
[21] R. Peibst et al., "Working principle of carrier selective poly-Si/C-Si junctions: Is tunnelling the whole story?," *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 60–67, 2016.
[22] M. Drießen et al., "Simultaneous boron emitter diffusion and annealing of tunnel oxide passivated contacts via rapid vapor-phase direct doping," *IEEE J. Photovolt.*, vol. 12, no. 5, pp. 1142–1148, Sep. 2022.
[23] H. Du et al., "Concurrently preparing front emitter and rear passivating contact via continuous pecvd deposition plus one-step annealing for high-efficiency tunnel oxide passivating contact solar cells," *Sol. RRL*, vol. 7, no. 7, 2023, Art. no. 2201082.
[24] A. Sinha, S. Dasgupta, A. Rohatgi, and M. C. Gupta, "Rapid thermal annealing of p-type polysilicon passivated contacts silicon solar cells," *IEEE J. Photovolt.*, vol. 13, no. 3, pp. 355–364, May 2023.
[25] A. Ingenito et al., "A passivating contact for silicon solar cells formed during a single firing thermal annealing," *Nature Energy*, vol. 3, no. 9, pp. 800–808, 2018.
[26] A. Richter et al., "Design rules for high-efficiency both-sides-contacted silicon solar cells with balanced charge carrier transport and recombination losses," *Nature Energy*, vol. 6, no. 4, pp. 429–438, 2021.
[27] J. Linke et al., "Fully passivating contact IBC solar cells using laser processing," in *Proc. 8th World Conf. Photovolt. Energy Convers.*, Milan, Italy, 2022.
[28] S. Sedky et al., "Structural and mechanical properties of polycrystalline silicon germanium for micromachining applications," *J. Microelectromech. Syst.*, vol. 7, no. 4, pp. 365–372, 1998.
[29] J. Poortmans and V. Arkhipov, *Thin Film Solar Cells: Fabrication, Characterization and Applications*, vol. 18. Hoboken, NJ, USA: Wiley, 2006.
[30] J. Westra, V. Vavruňková, P. Šutta, R. Van Swaaij, and M. Zeman, "Formation of thin-film crystalline silicon on glass observed by in-situ XRD," *Energy Procedia*, vol. 2, no. 1, pp. 235–241, 2010.
[31] P. Scherrer, "Bestimmung der grosse und inneren struktur von kolloidteilchen mittels rontgenstrahlen," *Nach Ges Wiss Gottingen*, vol. 2, pp. 8–100, 1918.
[32] A. Stesmans, "Interaction of p b defects at the (111) Si/SiO 2 interface with molecular hydrogen: Simultaneous action of passivation and dissociation," *J. Appl. Phys.*, vol. 88, no. 1, pp. 489–497, 2000.