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# A 117dB In-band CMRR 98.5dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing with an Electrically Floating Target

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**Abstract**

This paper describes a high-performance Capacitance-to-Digital Converter (CDC) for sub-nm displacement sensing with an electrically floating target. Intended to be integrated into a displacement sensor probe, the CDC consumes only 560µW. It achieves 98.5dB SNR in a 1ms conversion time, which is 34 times more energy-efficient than the prior art. Moreover, it also offers a 117dB in-band (1kHz) Common-mode Rejection Ratio (CMRR), providing decent electric field interference immunity.

## Introduction

Capacitive sensors are preferred for small range displacement sensing with sub-nm resolution in advanced industrial machines [1,2]. However, the conventional capacitive sensor readouts operate by wiring the target in a closed-loop configuration (e.g. via ground, Fig. 1a) [1-4]. This loop is susceptible to magnetic interference and also acts as a source of parasitic capacitance. These effects degrade the sensor's performance in industrial environments.

To minimize the loop while offering fully contactless displacement sensing, readouts with electrically floating targets have been proposed [5,6]. However, they are relatively power-hungry compared to conventional CDCs [1-4]. This often results in additional errors due to the self-heating when such readout is integrated into the sensor probe [2]. Moreover, any mismatch between the two sensing electrodes degrades the readout's CMRR and thus its electric field interference immunity [5]. This paper presents a CDC that overcomes these challenges while demonstrating an energy-efficiency comparable to the state-of-the-art CDCs that cannot use electrically floating targets [1-4].

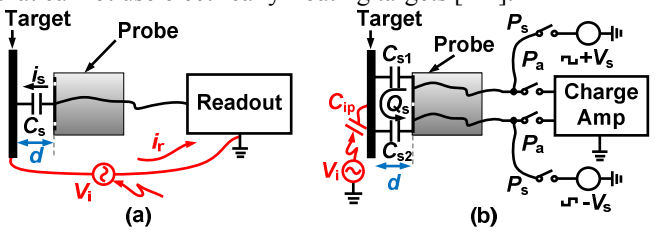


Fig. 1. Conventional capacitive displacement sensing system (a), Contactless capacitive displacement sensing with floating target (b).

## Proposed Design

Fig. 1b shows the operating principle of a displacement sensor with an electrically floating target [5]. The sensor readout employs two identical capacitive sensing electrodes, positioned close to the target electrode. This results in two capacitors in series ($C_{s1}$=$C_{s2}$=$C_s$), whose magnitudes equally vary with the distance ($d$) to the target. By exciting the capacitors with anti-phase voltages $\pm V_s$, the value of $C_s$ can be obtained by measuring the charge $Q_s$. Compared to the conventional capacitive readout approach, it significantly reduces the area of the sensing loop and thus minimizes the error caused by interfering magnetic fields [1-4]. Moreover, it enables the fully contactless displacement sensing using a capacitive sensor.

In practical implementations, the parasitic capacitance $C_{ip}$ (<500fF), between the floating target and its surrounding environment introduces a major challenge. It forms a path for interfering electric fields, primarily created by mains lines (50/60Hz). As shown in Fig. 2, the sensor's front-end consists of a differential charge integrator with switched-capacitor excitation. $C_{s1}$ and $C_{s2}$ are periodically charged, delivering a signal charge $Q_s$=$C_sV_{dd}$/2 to the integrator. An interfering signal $V_i$ then couples into the target electrode via $C_{ip}$, resulting in a common-mode signal that will be rejected by the differential charge integrator.

However, a mismatch between the sensing electrodes ($C_{s1}$≠$C_{s2}$), due to fabrication errors and/or alignment errors ($\theta$), results in a deteriorated CMRR [5]. In this work, a high CMRR is achieved, even with mismatched electrodes, by chopping the signal charge $Q_s$ and the charge integrator capacitors ($C_{inta}$ and $C_{intb}$). As shown in Fig. 2, the input switches $P_1$-$P_3$ are controlled by the chopping signal $P_{ch}$, preserving the integration operation for $C_s$ measurement. Due to the action of the input chopper, $C_{inta}$ and $C_{intb}$ continuously swap their position, such that $C_{inta}$ always accumulates negative charge ($Q_{sa}$), while $C_{intb}$ always accumulates positive charge ($Q_{sb}$). At the same time, the mismatched interference charges ($Q_{i1}$ and $Q_{i2}$), as well as the offset and the 1/$f$ noise of the integrator, are up-modulated to the out-of-band.

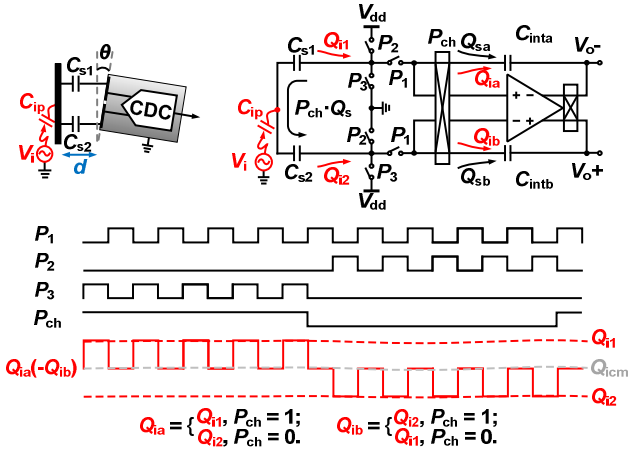


Fig. 2. Differential charge integrator with mismatched electrodes.

In contrast to [5], which first converts $Q_s$ into a proportional voltage and then digitizes it, this work directly embeds the charge integrator with sensing electrodes into a CDC, improving energy-efficiency and reducing the number of potential error sources [1,2]. As shown in Fig. 3, the CDC is based on a second-order feedforward 1-bit sigma-delta modulator. The first integrator is based on a folded-cascode OTA with 84dB DC gain. The second integrator and the passive adder are based on switched-capacitor circuits. The differential signal charge $Q_s$ is counterbalanced by a feedback DAC, in which $C_{fb}$=10pF. Depending on the output bitstream, it delivers a charge of $\pm C_{fb}V_{dd}$/2. This charge-balancing results in an output bitstream with an